Programmable Logic: Accelerating Automotive Applications

INTRODUCTION

Automotive applications are increasingly reliant on advanced technology to implement automated functionality. Automated capability is a complex area that spans a range of capabilities from fully automated operation to shared control with the driver. To classify the different automated capabilities, the Society of Automotive Engineers (SAE) has defined several levels that outline autonomy:

SAE Level	Name	Examples	Vehicle Control	Monitoring	Fall Back Control	Vehicle Capability
0	No Automation	N/A	Human Driver	Human Driver	Human Driver	N/A
1	Driver Assistance	Adaptive Cruise Control / Lane Keeping & Parking Assist	Human Driver & Vehicle	Human Driver	Human Driver	Some Driving Modes
2	Partial Automation	Traffic Jam Assist	Vehicle	Human Driver	Human Driver	Some Driving Modes
3	Conditional Automation	Full Stop & Go Highway Driving Self-Parking	Vehicle	Vehicle	Human Driver	Some Driving Modes
4	High Automation	Automated Driving	Vehicle	Vehicle	Vehicle	Some Driving Modes
5	Full Automation	Driverless Vehicle Operation	Vehicle	Vehicle	Vehicle	All Driving Modes

Automated capability requires the deployment of several key technologies, including vehicle-to-vehicle and vehicle-to-infrastructure communication, sensor interfacing and fusion, LiDAR, 4D RADAR, automotive vision and occupant monitoring.

ACHIEVING THIS CAPABILITY PRESENTS SEVERAL DIVERSE CHALLENGES TO THE SYSTEM DEVELOPER. THESE CHALLENGES CAN BE SEGMENTED INTO SYSTEM-OF-SYSTEM, SYSTEM AND MODULE LEVEL.

Challenges at the system-of-system level include the critical ability to adapt easily to new standards as draft standards are ratified. These evolving standards include protocols used for both intra-vehicle communication between subsystems and inter-vehicle communication between vehicles and infrastructure. Vehicle-to-vehicle and vehicle-to-infrastructure solutions must also be capable of working across a range of geographic locations, which may require the use of different frequency plans for different regions.

System-level challenges include achieving the necessary safety and security certifications to demonstrate compliance with ISO 26262, while also limiting the ability of unauthorized parties to make modifications. In addition to safety and security, the system must also be able to achieve demanding real-time performance to enable safe interaction with the vehicle's environment.

At the module level, the designer faces challenges to achieve not only the performance requirements but also to achieve size, weight and power, and cost targets (SWaP-C). Of course, these requirements must also be achieved within the demanding time-to-market.

XILINX AUTOMOTIVE TECHNOLOGY

The Xilinx Automotive (XA) portfolio, which includes the XA Artix-7 and XA Spartan-7 FPGA families, as well as in the XA Zynq-7000 SoC and XA Zynq UltraScale+ MPSoC families, along with associated tool chains. All the devices in the XA portfolio are tested in accordance with AEC-Q100 for part approval. This increased component quality helps with the overall reliability that supports the functional safety of the system.

To enable certification against Automotive Safety Integrity Level (ASIL) as defined by ISO 26262 Xilinx provides a range of certified tool chains and software tools.

In order to achieve the requirements within a power- and cost-efficient solution requires the selection of the correct device for the applications. Devices in the XA Artix-7 and XA Spartan-7 families offer a traditional FPGA-based approach, with the ability to implement softcore processors if sequential processing is required.

For more demanding solutions, Xilinx XA Zynq UltraScale+ MPSoCs and XA Zynq-7000 heterogeneous SoCs provide a great combination of processing system (PS) and programmable logic (PL).

Xilinx XA Zynq UltraScale+ MPSoC devices feature:

- PS containing a quad core 64-bit Arm Cortex-A53 processor capable of operation at up to 1.2GHz (FMax) and a real-time processing unit that contains dual 32-bit Lockstep Arm Cortex-R5 processors capable of operation at up to 500MHz (Fmax)

- PL based on 16nm UltraScale+ architecture that contains configurable logic block, Block RAM and DSP elements, which can operate at up to 645MHz (Fmax)

Xilinx XA Zynq SoC devices feature:

- PS containing a 32-bit dual core Arm Cortex-A9 processor capable of operating at up to 667MHz FMAX

- PL based on 28nm architecture containing configurable logic blocks, Block RAM and DSP elements, which can operate at up to 464MHz (Fmax)

The tightly coupled PS and PL provided by the Zynq UltraScale+ MPSoC and Zynq-7000 can be leveraged to achieve the demands of modern automotive applications.

Both FPGA and heterogeneous SoC solutions provide PL that enables parallelization of algorithms. This provides a lower latency and more deterministic implementation of the algorithm. PL also enables any-to-any interfacing with the right PHY, along with providing the flexibility to adapt to standards as they evolve compared to a CPU, GPU or ASIC solution.

XILINX TOOL CHAINS

Development of solutions using Xilinx XA devices is performed using Vivado Design Suite to define the configuration of the PS and the PL design.

Vivado provides the complete PL development experience, including support for synthesis, place and route, and with simulation. One of the key aspects of Vivado is the support for design reuse from existing IP to complete designs. Using Vivado, the designer can configure the processing systems in XA Zynq-7000 SoC and XA Zynq UltraScale+ MPSoC devices, along with implementing the PL design leveraging IP from the extensive IP catalog.

If custom IP blocks are required, these can be created using a hardware description language such as VHDL or Verilog. Additionally, Vivado High Level Synthesis also enables designs in C or C++ to be implemented within the PL.

When it comes to developing software solutions, Vitis is a unified software development platform that enables the creation of software for the Cortex-A9, A53, R5 and MicroBlaze softcore processors.

Vitis provides support for Embedded Linux development using PetaLinux, while also providing support for real-time operating systems such as FreeRTOS. Frameworks are provided to enable operation in a multi-processor environment such as OpenAMP for communication and lifecycle management.

IN ADDITION TO SYSTEM DEVELOPMENT CAPABILITIES, **VITIS ALSO PROVIDES SUPPORT FOR ACCELERATION USING OpenCL.**

OpenCL enables acceleration kernels to be deployed within the PL under the control of the application processing unit (APU). This means algorithm acceleration does not have to be implemented only by electronic engineers. Instead, higher-level synthesis based on C/C++ can be used in the algorithm. Performance optimizations can then be implemented in the algorithm using pragmas to leverage the parallel architecture of PL.

SECURITY

All Xilinx XA devices provide facilities for secure configuration of the device using an encrypted bit stream based on the Advanced Encryption Standard (AES). When XA Zynq-7000 SoC or XA Zynq UltraScale+ MPSoC devices are selected, the configuration security solution is more comprehensive due to the combination of the processor system and programmable logic.

The XA Zynq UltraScale+ MPSoC family of devices further enforces the security solution with the ability of the configuration security unit (CSU) within the PS to implement a layered security solution. This enables a secure configuration of the device thanks to the CSU's support of AES 256-GCM, 4096 RSA Multiplier, and SHA-384 providing confidentiality, authentication and integrity of the solution.

The CSU encryption engines AES, RSA and SHA blocks can also be leveraged at runtime to implement confidentiality, authentication and integrity functions. The DMA in the CSU provides very efficient processing. The CSU is also capable of implementing key management, including enabling key rolling to protect against differential power analysis key attacks.

Run-time security support includes the provision of anti-tamper response through the inbuilt system monitor (both FPGA and SoC devices), which enables device voltages and die temperature to be monitored with alarms raised if limits are exceeded. The system monitor also has external connections, which can be used for more physical anti-tamper protection at the enclosure level.

SAFETY

One of the significant challenges faced by manufacturers of automotive systems is achieving a safe system that complies with the relevant safety and quality standards.

For functional safety in the automotive world, this means compliance with one of four ISO 26262 Automotive Safety Integrity Levels (ASIL) that indicate the level of hazard of the system.

ASIL	Criticality	Failure In TIme	Metric	Consequence
ASIL-D	Most Critical	< 10 FIT	Single Point Failure Metric > 99% Latent Fault Metric > 90%	Possible Fatalities in Community
ASIL-C		< 100 FIT	Single Point Failure Metric > 97% Latent Fault Metric > 80%	Possible Fatalities
ASIL-B		< 100 FIT	Single Point Failure Metric > 90% Latent Fault Metric > 60%	Possible for Minor Injuries
ASIL-A	Least Critical	< 1000 FIT	Single Point Failure Metric < 90% Latent Fault Metric < 60%	Potential for Minor Injuries
QM	Quality Managed	NA	Not Safety Related	

The Single Point Failure Metric is the ability of the safety design to prevent risk from single point failures, while the latent fault metric is about multiple point failures that are not detected by the safety design. The Failure In Time (FIT) Metric defines the number of failures for equipment that can be expected in 1 billion hours. A lower FIT rate is required for more critical systems and presents a challenging target for the designer to achieve.

The ASIL for a system is determined by performing a hazard analysis that addresses:

- Severity – What are the potential injuries to the occupants

- Exposure – How often is the system/vehicle exposed to the hazard

- Controllability – What action can the driver/vehicle take to prevent the injury

As such, each system in a vehicle will have a different ASIL rating. For example, critical systems such as braking, steering and airbags are typically ASIL-D, while systems like headlights and ADAS systems are typically ASIL-B.

Creating a design that achieves the desired ASIL requires significant design analysis and failure-mode consideration to be able to detect and mitigate single point and latent failures.

INTELLECTUAL PROPERTY CORES, DEVICE ARCHITECTURE AND DOCUMENTATION SUPPORT PROVIDED BY **XILINX HELP ACHIEVE THE DESIRED FUNCTIONAL SAFETY LEVEL.**

Programmable logic low-level support for reliable logic design is provided, including error detection and correction on Block RAMs. Triple Modular Redundant (TMR) or Lockstep MicroBlaze softcore processors are often deployed in the PL to provide a diverse implementation, while the XADC and Sysmon can be used to monitor device supply rails and die temperature with alarms raised if limits are exceeded.

Isolation between functions within the PL can be implemented using Xilinx Isolation Design Flow and Vivado Isolation Verifier, which will ensure isolation between functions implemented within the PL.

The XA Zynq UltraScale+ MPSoC low power domain, real-time processing unit and safety manual have recently been certified against ISO 26262:2011 to ASIL-C. The architectural features that enable the implementation of ASIL-C solutions include:

- Three independent domains in the low power, full power and PL. Each domain has its own power supply and clocking providing hardware fault tolerance.

- TMR boot safety, power and error management processor in the platform management unit

- Lockstep ARM Cortex-R5 processors within the low power domain

- Memory and peripheral protection units, enabling isolation of the PS

- Error correction codes on critical memories

- Testable architecture including logic and memory built-in self-test, error injection and software test libraries

If certification is required, the Xilinx Automotive portfolio of devices is supported by tools certified to ISO 26262-8:2011.

The availability of certified tools enables developers to reduce the overall development time, helping to achieve delivery of the project on time, with high quality and lower cost.

Xilinx also provides system and analysis tools that are designed to help achieve certification, including safety manuals, software safety user guides, FMEDA tool and examples along with regular reliability reports. These resources are available via the Xilinx Functional Safety Package.

Using these development tools coupled with the Xilinx Automotive devices enables developers to address the challenges of modern automotive development.

ANY-TO-ANY INTERFACING

At the heart of implementing an automated capability is the ability to interface with sensors of different modalities, actuators and diverse communication interfaces. Once the data is received from the sensors, it requires processing to enable the vehicle to act.

One key challenge presented by the sensor interfacing and processing is the ability to work with a range of different high-bandwidth sensor modalities, all of which come with differing interface standards. A typical solution will receive data from a range of sensor modalities that use high-speed interfaces, such as MIPI, JESD204B, LVDS and GigE, for high-bandwidth sensors, such as cameras, RADAR and LiDAR. The sensor interfacing and processing will also be required to interface with lower-bandwidth sensors that use standards such as CAN, SPI, I2C and UARTs for accelerometers, etc.

The PS and PL of the Zynq UltraScale+ MPSoC provide support for a range of industry-standard interfaces, including CAN, SPI, I2C, UART and GigE, while the flexibility of the PL I/O enables direct interfacing with MIPI, LVDS and Giga Bit Serial Links, allowing higher levels of the protocol to be implemented within the PL, often using IP cores. Implementation of the protocol within the PL also enables standards revisions to be easily incorporated, along with providing flexibility as to the number of specific sensor interfaces supported within a solution. The PL also provides the ability to implement any interface with the provision of the correct PHY in the hardware design, providing a true any-to-any interfacing capability.

ACCELERATING IMAGE PROCESSING

Image processing is at the heart of many automotive applications, from navigation to occupant monitoring. Typically, the algorithms used for these systems are created and modelled in high-level frameworks, such as OpenCV.

> PL SOLUTIONS ENABLE A SIGNIFICANTLY **INCREASED PERFORMANCE FOR IMAGE-PROCESSING APPLICATIONS,** AS A TRUE IMAGE-PROCESSING PIPELINE CAN BE CONSTRUCTED IN THE LOGIC. THIS PIPELINE LEVERAGES THE PARALLEL NATURE OF PL.

To be able to leverage the high-level algorithmic models created in frameworks, such as OpenCV, without the need to recreate everything using an HDL, Xilinx provides the XF::OpenCV library. The XF::OpenCV library contains several commonly used OpenCV functions that can be synthesized using high-level synthesis in the Vitis Unified Software Development Platform into the PL. This enables high-level modelling to take place using OpenCV and then quickly and easily the same functions to be implemented within the PL pipeline without the need to write a line of hardware description language.

Should the image processing or downstream processing require H.264/H.265 encoding or decoding, the EV variant of the XA Zynq UltraScale+ MPSoC offers a built-in video CODEC unit along with associated UltraRAM for buffering streams.

ACCELERATING NEURAL NETWORKS

Following on from image processing, machine learning is another critical technology to enable the development of automated applications. For example, machine learning can be used to classify objects on the highway or observe and monitor occupants.

Implementation and acceleration of the neural network can leverage Vitis AI. Vitis AI enables the acceleration of commonly used ML/AI frameworks, including Caffe and TensorFlow, using PL. To enable this, Vitis AI provides a Model Zoo, AI Compiler, Optimizer, Quantizer and Profiler to deploy applications onto the Deep Learning Processing Unit.

MIXED SIGNAL CAPABILITIES

RADAR is the only sensor technology that works across all lighting and weather conditions, including fog and heavy rain. To provide sufficiently accurate information for operation at higher SAE automated levels, four-dimensional RADAR is often used.

4D RADAR provides information on azimuth, elevation and slant range but also the Doppler frequency. The Doppler frequency enables the determination of the target's velocity to be detected. 4D RADAR therefore provides a system that can have a large field of view (100 degrees), fine spatial resolution (1 degree) and longer-range capabilities (circa 300m). This enables automated operation at SAE levels 2 and 3 with capabilities such as Traffic Jam Assist, Highway Driving and Self-Parking.

Traditionally, RADAR solutions require the use of baseband digital processing for signal generation and processing long with a RF front end to provide the up and down conversion. Baseband signals are converted to and from the analog domain using analog-to-digital converters (ADC) and digital-to-analog converters (DAC).

The Xilinx Zynq UltraScale+ RFSoC portfolio of devices contain not only a PS with high-performance quad core Arm Cortex-A53 64-bit processors, but also PL that includes gigasample per second (GSPS) ADC and DAC along with necessary supporting infrastructure, including up and down converters, complex mixers and interpolators and decimators. This significantly minimizes the complexity of interfacing with the RF front end, while also reducing the overall required implementation area.

The main elements of the Xilinx Zynq UltraScale+ RFSoC are the ADC and DAC converters, which can operate at GSPS sampling rates. Depending on the generation, this sample rate can vary between 2 GSPS for the ADCs in generation one to 5 GSPS for generation-three devices, with supporting RF input bandwidth to enable operation across all four Nyquist zones. Sampling rates for the DAC range from 6.5 GSPS in generation one to 10 GSPS in generation two. This combination of sampling rate and wide RF input bandwidth enables a significant reduction in the complexity of the RF Tx and Rx Paths.

CONCLUSION

As the demands on automotive capability increase, the Xilinx XA portfolio of automotive devices and supporting tool chains provide designers with the ability to achieve not only the desired performance, but also the quality, functional safety and security required.

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