Practical Design Guidelines on the Usage of an Isolated Gate Driver

AND90180/D

This application note provides guidance on how to select and practical application design the right isolated gate driver for power switching devices in power electronic applications.

onsemi's isolated gate drivers are suitable designed for the highest switching speeds and system size constrains required by technologies such as SiC (Silicon carbide) and GaN (Gallium nitride), by providing reliable control over MOSFET. Many designers in the power electronic industry are already expert users of Si MOSFET, SiC, and GaN MOSFET in many types of power electronic applications. System manufacturers are increasingly interested in increasing the power efficiency of their designs; the combination of energy efficiency and reduced costs is becoming critical to market leadership. Considerable progress has been made in this area from a semiconductor materials perspective, and there are now products that can switch at high speeds, providing improved system−level efficiency while reducing size.

Gate Driver – What, Why and How?

The power MOSFET is a voltage−controlled device that is used as a switching element in power supply circuits and motor drives, amongst other systems.

The gate is the electrically isolated control terminal for each device. The other terminals of a MOSFET are source and drain.

To operate a MOSFET, typically a voltage has to be applied to the gate that is relative to the source or emitter of the device. Dedicated drivers are used to apply voltage and provide drive current to the gate of the power device.

The Gate Driver serves to turn the power device on and off, respectively. In order to do so, the gate driver charges the gate of the power device up to its final turn−on voltage $V_{GS(ON)}$, or the drive circuit discharges the gate down to its final turn−off voltage $V_{GS(OFF)}$. The transition between the two gate voltage levels requires a certain amount of power to be dissipated in the loop between gate driver, gate resistors and power device.

Today, high−frequency converters for low and medium−power application are predominantly making use of the gate voltage−controlled device, such as power metal−oxide−semiconductor field effect transistors (MOSFETs).

For High Power Applications the best devices in use today is Silicon Carbide (SiC) MOSFETs that is the higher driving current is required to fast turn ON/OFF a power switch. Gate Drivers are not just for MOSFET's but also for fairly new and esoteric devise from Wide Band Gap group such as Silicon Carbide (SiC) FET's and Gallium Nitride (GaN) FET's as well.

It is a power amplifier that accepts allow power input from a controller IC and produces the appropriate high−current gate drive for a power switching devices.

The following is a short summary reason why to use the gate driver:

- Gate Drive Impedance – The gate driver's function is to turn the power device – ON and OFF respectively (usually quickly) in order to reduce losses.
  To avoid cross conduction losses due to the Miller effect or due to slow switching with some loads, it is important for the driver to assert the off state with a lower impedance than the on−state drive on the opposing transistor. The negative gate drive margin plays an important part in reducing these losses
- Source Inductance – This is the inductance shared by the gate driver current loop and the output current loop.
  The negative gate drive voltage margin combined with the source lead inductance have a direct effect on the switching speed of the output under load.
  This is due to the source degeneration effect of the source inductance (the source lead inductance couples the output switching current back to the gate drive, slowing the gate drive).

Gate Driver device applies voltage signal (V_{GS}) between Gate (G) & Source (S) of power MOSFET, while providing a high−current pulse as shown in Figure 1.

- To charge/discharge C_{GS}, C_{GD} Quickly
- To switch ON/OFF power MOSFET Quickly

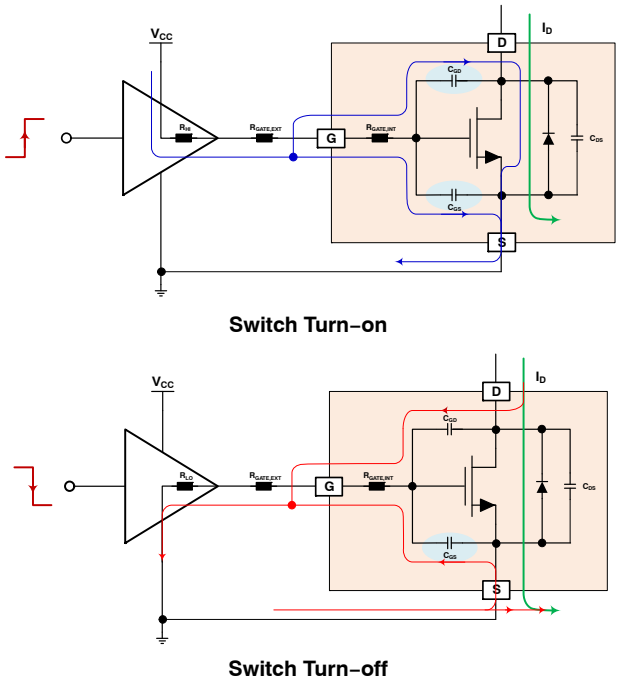


Figure 1. Gate Driving Current Path

Why use the Galvanic Isolation?

In high−power applications, galvanic isolation is required to prevent the triggering of dangerous ground loops that can cause noise that can compromise the safety of the system when the grounding of both circuits is at different potentials. In this type of system, current flow can be fatal to humans, so it is essential to ensure the highest level of safety. Electrical or galvanic isolation refers to a state in which DC circulation does not occur between two points with different potentials. More precisely, it is not possible to move charge carriers from one point to another while electrical energy (or a signal) can still be exchanged by other physical phenomena, such as electromagnetic induction, capacitive coupling, or light. This condition is equivalent to an infinite electrical resistance between the two points, even if in practice, a resistance on the order of 100 MΩ is sufficient. If the damage is limited to electronic components, then safety isolation may not be necessary, but galvanic isolation is a requirement between the high−power side and low voltage control circuit if there is any human involvement on the control side. It provides protection against any fault on the high voltage side as the isolation barrier blocks electrical power from reaching the user despite component damage or failure. Isolation is mandated by regulatory and safety certification agencies to prevent shock hazard. The following is a summary why used reason and method of galvanic isolation in many power applications.

- To protect from and safely withstand high voltage surges that would damage equipment or harm humans.
- To protect expensive controllers –intelligent systems
- To tolerate large ground potential differences and disruptive ground loops in circuits that have high energy or are separated by large distance
- To communicate reliably with high side components in high−voltage high performance solutions

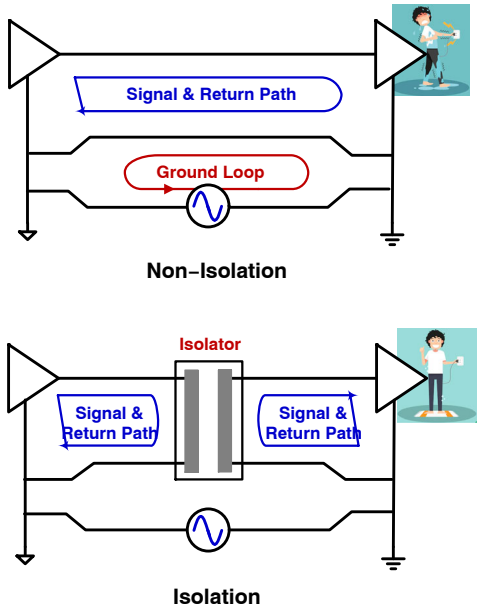


Figure 2. Non−Isolation vs. Isolation

Isolated Gate Driver Selection Guide

The following is a key selection guides of an isolated gate driver: For example, the system with low operating voltage, switching component can directly connect to the controller, as long as the withstand voltage of the controller is within the allowable range. However, gate drivers are common elements in most power converters. Since the control circuitry operates at low voltages, controllers cannot provide sufficient power to quickly and securely open or close the power switch. As a result, the signals from the controller are sent to the gate driver, which can withstand much higher power and can drive the MOSFET's gate as needed. When working in high−power or high−voltage applications, the elements in the circuit are subject to large voltage shifts and high currents. If there is a current leak from the power MOSFET to the control circuitry, the high voltages and currents involved in the power conversion circuit could easily cause a massive breakdown of the control circuit by frying the transistors. In addition, high−power applications having galvanic isolation between the input and output to protect both the user and any other devices is essential.

Gate Driving Voltage Ranges

The operating voltage of converter is determined by the specifications of the switching element, such as Si MOSFET, or SiC MOSFET. It must be confirmed that the converter output voltage does not exceed the maximum value of the gate voltage for switching elements.

The positive voltage of the gate drive should be high enough to ensure that the gate is fully turned on. Also need to make sure drive voltage not to exceed the absolute maximum gate voltage. Si−MOSFET typical using +12V to drive, +15V is commonly used to drive SiC, and the gate voltage for GaN is +5V. When the gate voltage is 0−V, it can meet the turn off condition for all devices. Generally, negative bias gate drive is not required for MOSFETs, sometimes used for SiC and GaN MOSFET devices. It is highly recommended to use a negative bias gate drive with SiC and GaN MOSFETs in switching applications because there could be ringing in the gate−source drive voltage of the power transistor during high di/dt and dv/dt switching cause of parasitic inductances are introduced by non−ideal PCB layout. The following is the applicable gate driving voltages for each switching devices.

	Si MOSFET	SiC MOSFET	GaN
Positive	10 V to 15 V	1 5 V to 20 V	5 V to 6 V
Negative	0 V	−2 V to −5 V	0 V to −3 V
Common Drive Voltage	+12 V / 0 V	+15 V / −3 V	+5 V / 0 V
	−	+15 V / −5 V	+6 V / −3 V

Isolation Capability

This item is determined by the operating voltage of the system. System operating voltage is proportional to Isolation Capability. One of the key parameters for isolated gate drivers is its isolation voltage rating. Having the right isolation rating is crucial for protecting the user from potentially harmful current discharges, as it aims to avoid unexpected voltage transients from destroying other circuits connected to the supply. In addition, this rating can maintain signals within the converter free from the interferences caused by noise or unexpected common−mode voltage transients. Isolation is usually expressed as the amount of voltage the isolation layer can withstand. In most isolated gate driver datasheets, the isolation voltages are introduced as parameters such as the maximum repetitive peak isolation voltage (V_{IORM}), working isolation voltage (V_{IOWM}), maximum transient isolation voltage (V_{IOTM}), maximum surge isolation Voltage (V_{IOSM}), and RMS isolation voltage (V_{ISO}). The higher the system operating voltage, the higher converter isolation capability needed.

onsemi's isolated gate driver isolation is tested on an MPS tester (Model MSPS−20) at production.

Isolation Capacitance

Isolation capacitance is the parasitic capacitance between the converter input and output side. Through the following formula, it can be found that the isolation capacitance is proportional to the leakage current.

$$I_{leak} = 2 \times \pi \times f_S \times C_{ISO} \times V_{SYS}$$

where: I_{leak}: Leakage current, f_S: Operating frequency C_{ISO}: Isolation capacitance. V_{SYS}: System operating voltage

The power loss is proportional to leakage current. If the system needs to operate at high operating frequencies and high voltages, we need to pay more attention on the size of the insulation capacitor of the converter, to avoid too much temperature increasing.

Common−Mode Transient Immunity (CMTI)

Common−Mode Transient Immunity (CMTI) is one of key characteristics associated with isolated gate drivers, especially when system operating at high switching frequency. It is important because high-slew-rate (high-frequency) transients can corrupt data transmission across the isolation barrier. The capacitance across the barrier (i.e., between the isolated ground planes) provides the path for these fast transients to cross the isolation barrier and corrupt the output waveform. The unit is normally in kV/uS.

If the CMTI is not sufficiently high, the high−power noise could be coupled across the isolated gate driver, generating a current loop and causing charge to appear at the switch gate. If this charge is large enough, it could cause the gate driver to misinterpret this noise for a driving signal, causing a severe circuit malfunction due to shoot−through.

Current Driving Capability Consideration

Gate drivers capable of sourcing/sink higher gate currents for a short period of time produces lower switching time, resulting in lower switching power loss within the driven transistor.

Peak source and sink currents (I_{SOURCE}, and I_{SINK}) capability should be larger than average current ($I_{G,AV}$) as shown in Figure 3.

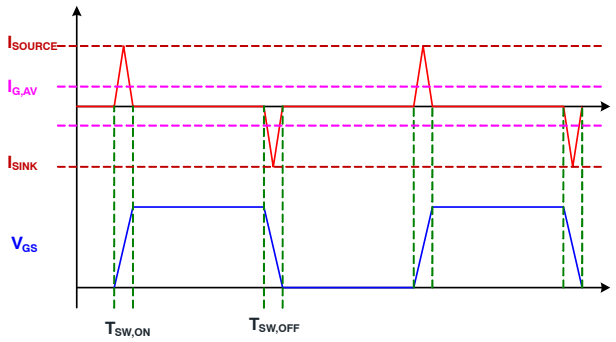


Figure 3. Definition of Current Driving Capability

The approximate maximum gate charge Q_G that can be switched in the indicated time for each driver current rating may be calculated: Needed driver current ratings depend on what gate charge Q_G must be moved in what switching time

$t_{SW-ON/OFF}$ because average gate current during switching is I_G.

$$I_{G.AV} = \frac{Q_G}{t_{SW,ON/OFF}}$$

where, $t_{SW,ON/OFF}$ is how fast the MOSFET should be switched. If unknown, start with 2% of the switching period t_{SW}.

The approximate gate driver source and sink peak currents can be calculated as below equations.

At turn−on (Sourcing current)

$$I_{SOURCE} \geq 1.5 \times \frac{Q_G}{t_{SW,ON}}$$

At turn−off (Sinking current)

$$I_{SINK} \geq 1.5 \times \frac{Q_G}{t_{SW,OFF}}$$

where, Q_G = Gate charge at $V_{GS} = V_{CC}$
$t_{SW, ON/OFF}$ = Switch On / Off time
1.5 = empirically determined factor
(Influenced by delay through the driver input stage and parasitic elements)

Consideration of Gate Resistor

The gate resistor is also sized to reduce ringing voltage by parasitic inductances and capacitances. However, it limits the current capability of the gate driver output. The limited current capability value induced by turn−on and off gate resistors can be obtained with below equation.

$$I_{SOURCE} = \frac{V_{CC} - V_{ON}}{R_{G,ON}}$$

$$I_{SINK} = \frac{V_{CC} - V_{OL}}{R_{G,OFF}}$$

where: I_{SOURCE}: Source peak current
I_{SINK}: Sink peak current.
V_{OH}: High level output voltage drop
V_{OL}: Low level output voltage drop

What is the onsemi' s Isolated Gate Driver?

onsemi provides various isolated gate drivers based on an integrated magnetically − coupled coreless transformer suitable designed for the highest switching speeds and system size constrains required by technologies and reliable control over Si MOSFET, and SiC FETs.

We offer functional, and reinforced isolation product certified from UL 1577, SGS FIMKO for IEC 62368−1 and CQC GB 4943.1. Our isolated gate drivers are available both industrial and automotive qualified products.

These are isolated gate drivers with integrated variety features, withstand high CMTI level, multiple UVLO choices and provide fast propagation delay including short delay mismatching and shortest pulse width distortion.

Specially, the NCP51752 provides a simple way to generate negative bias in the gate drive loop suited to drive SiC MOSFETs. This negative bias is very useful in case of PCB layout and/or package leads generating high ringing in power transistor Vgs. This ringing of the gate voltage generally occurs under high di/dt and dv/dt switching conditions. To keep the ringing below threshold voltage to prevent spurious turn−on generally applies a negative bias on the gate drive. The NCP51752 offers different options to generate −2 V, −3 V, −4 V and −5 V to accommodate all configurations. **onsemi**'s isolated gate driver provides various package option include small LGA as well as SOIC 8−pin to 16−pin variants.

The following is key features, electrical specifications and Safety−Related certifications of **onsemi**'s isolated gate driver family.

Table 1.

Function / Property		Single Channel		Dual Channel			
		NCP51152*	NCP51752*	NCP51560	NCP51561	NCP51562*	NCP51563
Package type		SOIC−8 NB	SOIC−8 NB	SOIC−16 WB	SOIC−16 WB	LGA−13 SOIC−16 NB	SOIC−16 WB
Automotive (NCV part)		✓	✓	—	✓	—	✓
Isolation rating [kV_{RMS}]		3.75	3.75	5	5	2.5	5
Max. input supply [V]		25	25	5.5	5.5	25	5.5
Max. output supply [V]		33	33	33	33	33	33
Peak driving current [A]		4.5 / −9.0	4.5 / −9.0	4.5 / −9.0	4.5 / −9.0	4.5 / −6.0	4.5 / −9.0
Typ. propagation delay [ns]		45	45	36	36	36	36
Max. pulse distortion [ns]		5	5	5	5	5	5
CMTI [kV/us]		200	200	200	200	100	200
UVLO	5−V	**	**	✓	**	✓	**
	8−V	✓	**	✓	✓	✓	✓
	12−V	✓	✓	**	**	**	✓
	17−V	**	✓	**	✓	**	**

Table 1.

Function / Property		Single Channel		Dual Channel			
		NCP51152*	NCP51752*	NCP51560	NCP51561	NCP51562*	NCP51563
ENABLE or DISABLE		✓	✓	✓	✓	✓	✓
Dead time control		—	—	✓	✓	✓	✓
ANB function		—	—	—	✓	—	✓
Negative gate voltage		✓	✓	—	—	—	—
Integrated negative bias		—	✓	—	—	—	—
Split Source /Sink output		✓	—	—	—	—	—
Isolation & Safety	UL/CSA	***	***	***	✓	***	✓
	SGS FIMKO	***	***	✓	✓	***	✓
	CQC	***	***	✓	✓	***	✓
	UL/CSA File number: E509109 CQC Certification number: CQC21001309168 SGS FIMO Certification number: FI/41310						

* Under development
** Option on demand
*** Planned

Isolated Gate Driver Support Tools:

- Our galvanic isolated gate driver allows you to see all documents available on the **onsemi** home page, Datasheet, Design & Development Tools, Simulation Models, Application Notes, Evaluation Board Documents and Conformance Reports

Main related drives are:

- NCP51560
- NCP51561 & NCV51561
- NCP51563 & NCV51563
- NCP51562
- NCP51152
- NCP51752

Application Design Guidance for an Isolated Gate Driver

The following is some application design guidance when using the **onsemi**'s isolated gate driver:

Power Supply Recommendations

The following is some recommendations that should be noted when using an isolated gate driver power supply.

Bypass capacitors for V_{DD}, and V_{CC} are essential for achieving reliable isolated gate driver's performance.

It is recommended that one choose low ESR and low ESL surface−mount multi−layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. The output bias supply pin of gate driver should be needs to bypass capacitor with a value of at least ten times the gate capacitance of the switching device, and no less than 100 nF and located as close to the device as possible for the purpose of decoupling. We recommend using 2 capacitors; a 100 nF ceramic surface−mount capacitor, and another capacitor of few microfarads added in parallel as shown in Figure 4.

Similarly, a bypass capacitor should also be placed between the V_{DD} and GND pins in input side. Given the small amount of current drawn by the logic circuitry within the input side, this bypass capacitor has a minimum recommended value of 100 nF.

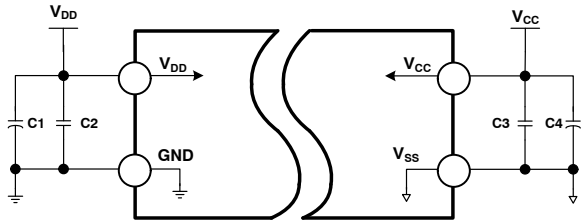


Figure 4. Schematics of the Power Supply

Input filtering design when using the Isolated Gate Driver?

In order to have good signal quality and noise immunity, an input filter RC network could be placed between microcontroller and gate driver inputs as shown in Figure 5.

There are two ways of filtering often used in power electronic applications:

- RC−filters at control input terminals
- Combination of a RC−filter with short delay time and a precise integrated filter in the gate driver itself.

The RC value will depend on input frequency range, duty cycle, and time delay according to system requirement.

- A small capacitive filter with up to 100 pF and up to 100 Ω suppresses high frequency noise on the input terminals of the driver. The filter capacitor rejects common−mode noise.
- The filter resistor helps protect the controller. The series resistance limits the current to or from the controller during ground bouncing, damps any parasitic inductance in the gate drive line which may contribute to ringing, and helps to suppress any EMI absorbed by long input traces.
- This RC filter needs to place the gate driver pin lead as closed as possible. The common mode transient noise can be interfering from high voltage output circuit to the low voltage input side. The digital control inputs should have low impedance signal source to prevent the glitch or unexpected switching.

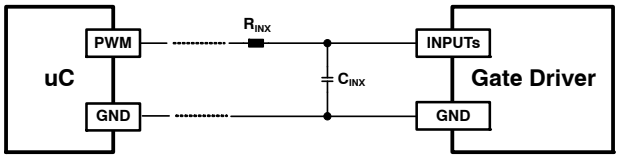
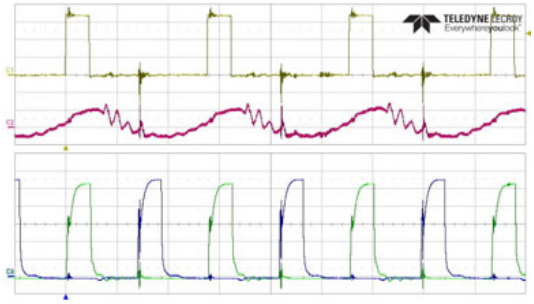


Figure 5. Example of RC Networks for Input Signals

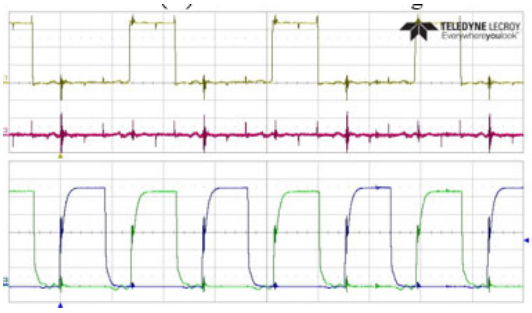
The other input pins (e.g., ANB, DT, and ENA/DIS) also need to be properly filtered to create a robust system. Improper input filtering can lead to a variety of undesirable effects as a result of electromagnetic interference (EMI) from power stage transient voltages and currents.

For example, Figure 6 shows an operation waveform when an ANB pin is floating where there is no filtering on the upper and proper filtering on the bottom figure. As shown in experimental result, noise signal has observed without bypass capacitor and the noise signal disappears with bypass using above 1−nF capacitor close to this pin.

The input signal pins impedance is 200 kΩ typically and the ANB and ENA/DIS pins for DISABLE is pulled to GND pin as shown in Figure 7. Whereas the ENA/DIS pin for ENABLE feature has pulled to V_{DD} pin as shown in Figure 8 (B).



(A) In case of no filtering



(B) In case of proper filtering
CH1: INA (1V/div), CH2: ANB(1V/div),
CH3: OUTB(2V/div), and CH4: OUTA(2V/div)

Figure 6. Effect of Component Filtering on ANB Pin

Noise from the driver pin can couple onto the input pins (ANB, and ENA/DIS), causing the driver to react to transients instead of input PWM signals. This can result in unwanted behavior on the driver input and output and can be reduced system performance as well.

In addition, if driver have long distance with the ANB, and ENA/DIS pins and the driver requires more caution for layout and filtering in order to avoid this unwanted behavior.

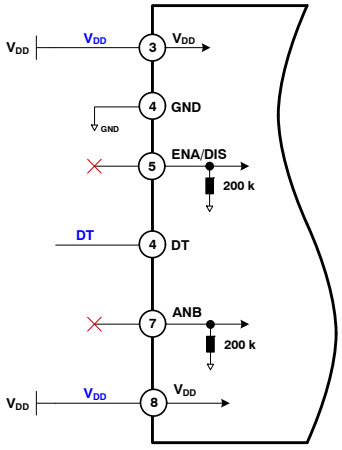


Figure 7. Example of AND, and ENA/DIS Pins are Floating

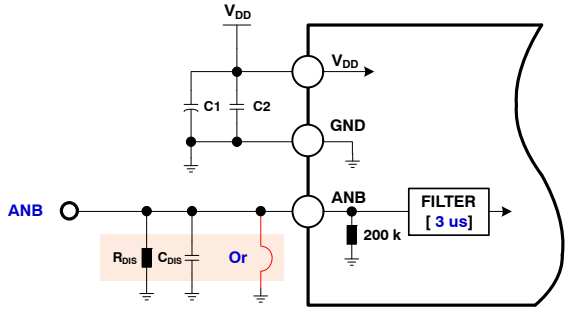
If the ENA/DIS for DISABLE and ANB functions are required, use a low ESR/ESL capacitor with a value of approximately 1nF for overall improved system performance. The following is summary of considerations when use the ENA/DIS and ANB pin are floating.

ENA/DIS pin: Tie directly to V_{DD} or GND pin for ENABLE and DISABLE feature respectively, if the ENA/DIS pin is unused. If it is not possible to connect ENA/DIS pin to V_{DD} or GND then external pull−up or pull−down resistor few ten kΩ (e.g.,10 kΩ~ 47 kΩ) with V_{DD} or GND pin is recommended to achieve better noise immunity when using an ENA/DIS pin as an ENABLE or DISABLE feature respectively as shown in Figure 8 (B) and (C).

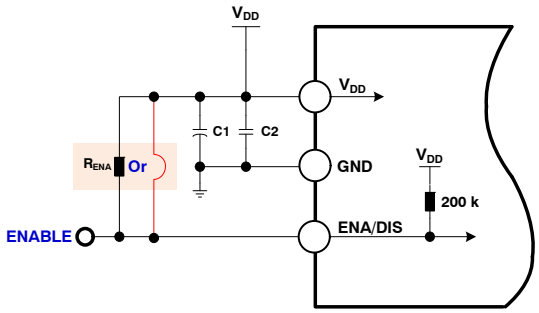
When using a controller to drive the ENA/DIS pin over a few inches or more, it's requiring a 1−nF capacitor with low ESR/ESL, placed close to the pins.

In cases where fast disable response time is required, place the controller closer to the driver, use high drive strength outputs, and minimize stray inductance in the gate driving loop.

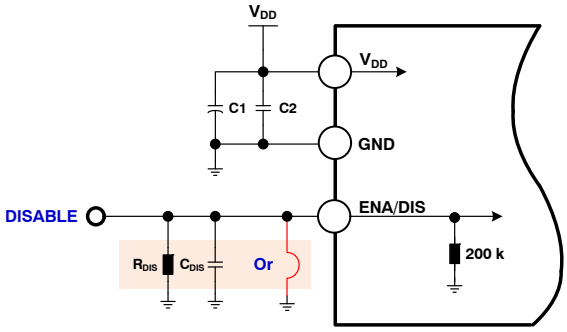
ANB pin: Tie to directly GND pin, or use a 1−nF capacitor, if the ANB pin is unused. If it is not possible to connect ANB pin to GND then external pull−down resistor few ten kΩ (e.g.,10 kΩ~47 kΩ) is recommended to prevent unwanted ANB function activation by external interference as despite its internal 3.3 μs filter as shown in Figure 8 (A).



(A) Example of ANB pin



(B) Example of ENA/DIS pin for ENABLE



(C) Example of ENA/DIS pin for DISABLE

Figure 8. Example of Proper Filtering for ANB, ENA/DIS Pins

Programmable Dead−Time Control

Dead time is automatically inserted whenever the dead time of the external two input signals (between INA and INB signals) is shorter than internal setting dead times (DT1 and DT2). Otherwise, if the external input signal dead times are larger than internal dead− time, the dead time is not modified by the gate driver and internal dead−time definition as shown in Figure 9.

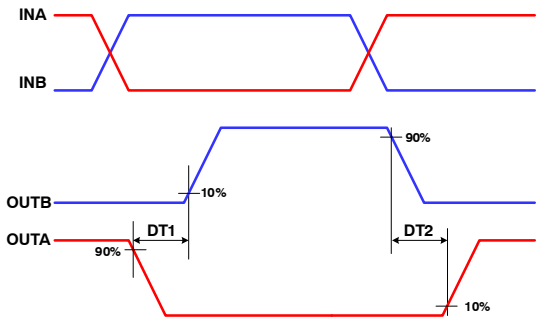
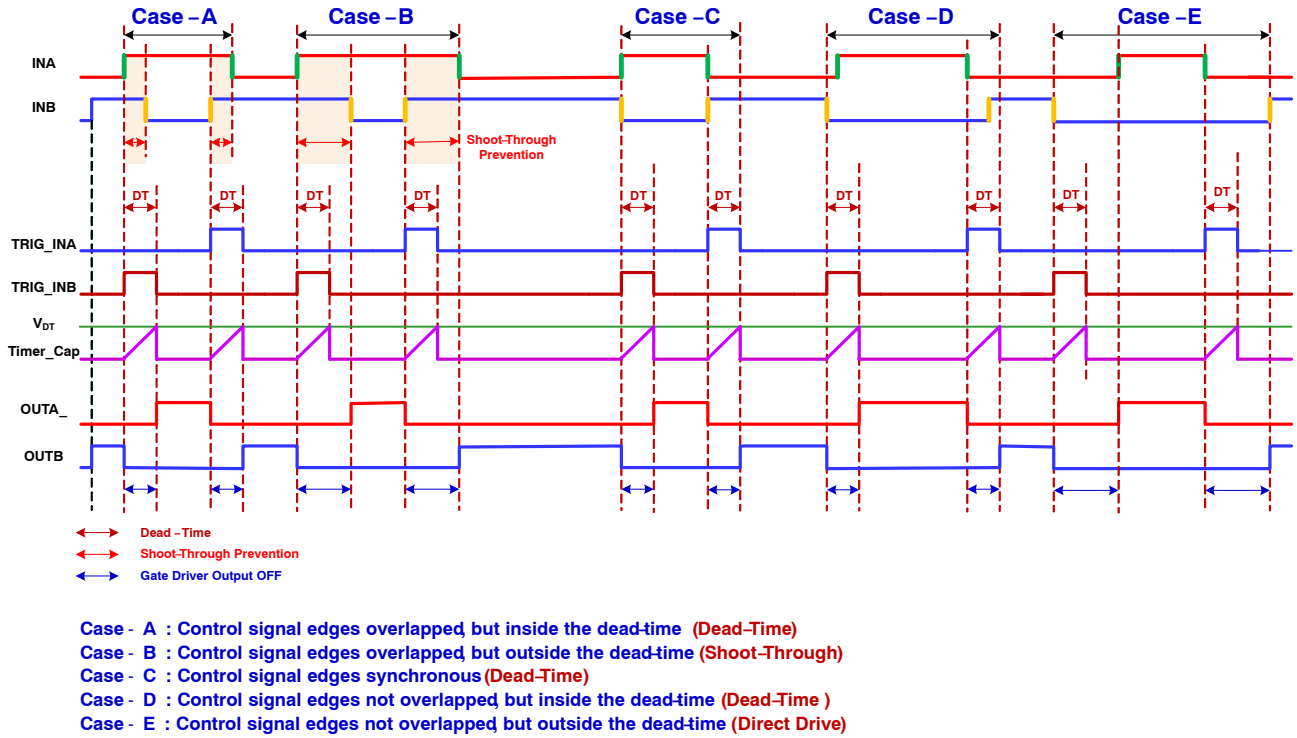


Figure 9. Internal Dead−Time Definitions

Figure 10 shows the definition of internal dead time and shoot−through prevention when input signals applied at same time.



Case - A : Control signal edges overlapped, but inside the dead-time (Dead-Time)
Case - B : Control signal edges overlapped, but outside the dead-time (Shoot-Through)
Case - C : Control signal edges synchronous (Dead-Time)
Case - D : Control signal edges not overlapped, but inside the dead-time (Dead-Time)
Case - E : Control signal edges not overlapped, but outside the dead-time (Direct Drive)

Figure 10. Internal Dead−Time Definitions

Cross−conduction between both driver outputs (OUTA, and OUTB) is not allowed with minimum dead time (t_{DTMIN}) typically 10 ns when the DT pin is open in the **MODE−A.** External resistance (R_{DT}) controls dead time when the DT pin resistor between 1 kΩ and 300 kΩ in the **MODE−B**.

Overlap is not allowed when the dead time (DT) control mode is activated.

The dead time (DT) between both outputs is set according to: DT (in ns) = 10 × R_{DT} (in kΩ).

Overlap is allowed for both outputs when the DT pin is pulled to V_{DD} in the **MODE−C**, as shown in Figure 11.

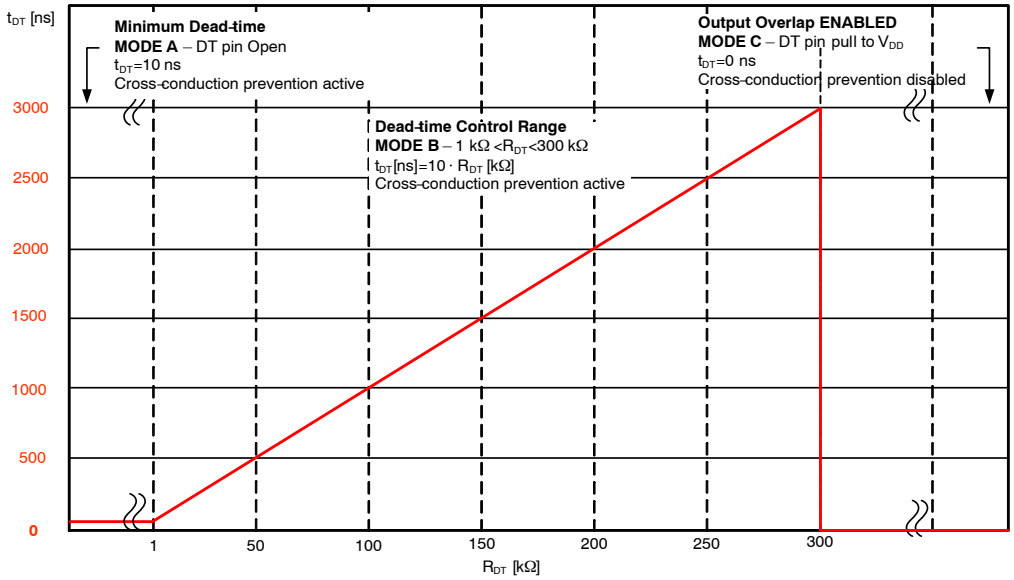
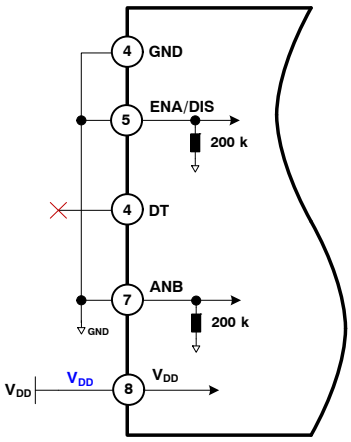


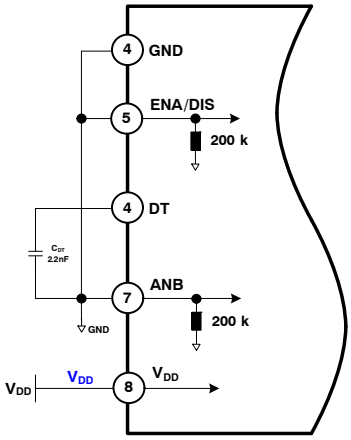
Figure 11. Timing Chart of Dead−Time Mode Control

Dead−time (DT) Pin is Floating

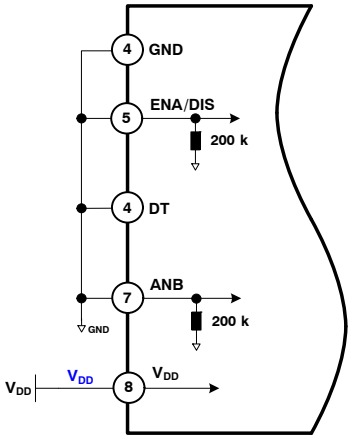
It is recommended the DT pin tied directly to the GND pin or use a 2.2−nF capacitor when the DT pin is floating as shown in Figure 12 on the middle and bottom figures respectively.



(A) In case of no filtering for DT pin



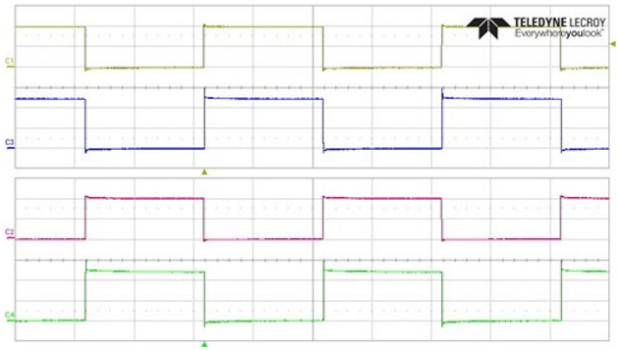
(B) In case of proper filtering for DT pin



(C) Connect to GND

Figure 12. Example of Proper Filtering for ANB, ENA/DIS Pins

Cross−conduction between both driver outputs (OUTA, and OUTB) is not allowed with minimum dead time (t_{DTMIN}) typically 10 ns when thew DT pin is floating as shown in Figure 13.



CH1: INA(2V/div), CH2: OUTA (5V/div),
CH3: INB (2V/div), and CH4: OUTB (5V/div)

Figure 13. Experimental Waveforms when DT Pin is Floating

Programmable Dead−time (DT)

If programming the dead−time through a dead−time control resistor, place a capacitor in parallel with a value greater than 2.2nF to increase noise immunity during fast switching transients as shown in Figure 14.

External resistance (R_{DT}) controls dead time when the DT pin resistor between 1 kΩ and 300 kΩ. Figure 15 shows experimental result when the DT pin with 100 kΩ.

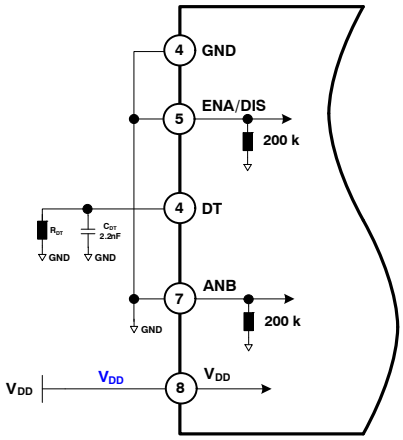
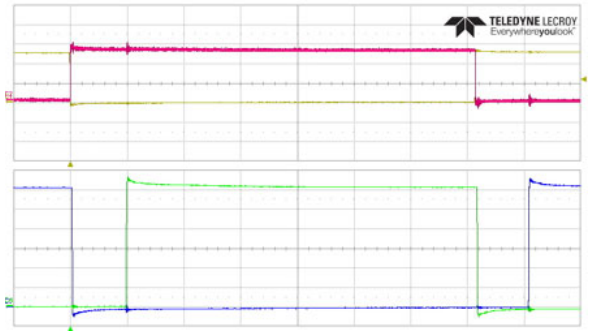


Figure 14. Example of Proper for Dead−Time Pin



CH1: INA(2V/div), CH2: INB (2V/div),
CH3: INB OUTA (5V/div) and CH4: OUTB (5V/div)

Figure 15. Experimental Waveforms when DT Pin with 100 kΩ

No Dead−time for Allowed Cross Conduction

If no dead time is required, tie the dead time pin to V_{DD} to deactivate the DT circuit as shown in Figure 16 and experimental result as shown in Figure 17.

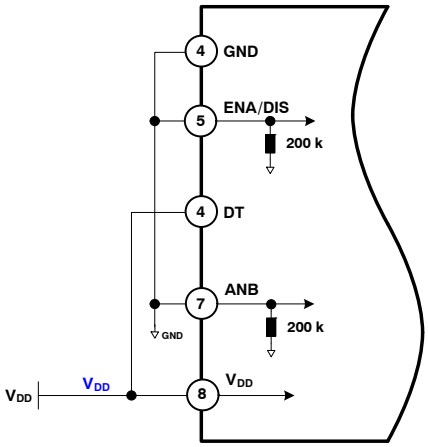
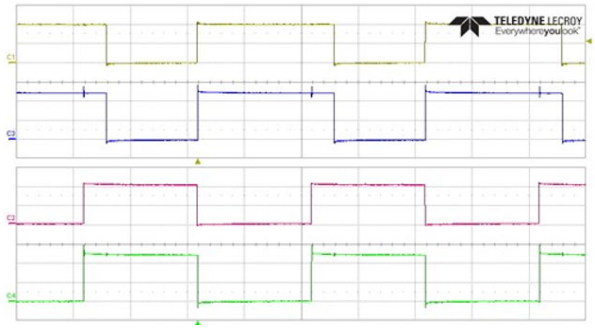


Figure 16. Example of Deactivation of DT Pin by tying to V_{DD} Pin



CH1: INA(2V/div), CH2: OUTA (5V/div),
CH3: INB (2V/div), and CH4: OUTB (5V/div)

Figure 17. Experimental Waveforms when DT Pin shorted V_{DD}

Consideration of Dead−time (DT) Pin is Floating

The dead−time control function provides three kinds of operating mode according to the DT pin voltage.

It's possible to have the abnormal noise on the DT pin during surge test, such as lightning surge when the DT pin is floating. If the DT pin voltage exceed the specified voltage level affected by noise signal, the dead−time control mode is changed to MODE−C as despite its internal 3 μs and 2 μs filtering time for DT pin open and short detection respectively because the dead−time control mode changes according to the DT pin voltage.

For example, if the DT pin voltage below $0.9 \times V_{DD}$, the dead−time has minimum value (typ. 10 ns) when used DT pin is floating and steady state voltage at DT pin is around 0.8 V.

If the DT pin voltage exceed the $0.9 \times V_{DD}$ with above 3 μs period caused by noise, dead−time control mode is disable that means no dead−time between dual channels as shown in Figure 18.

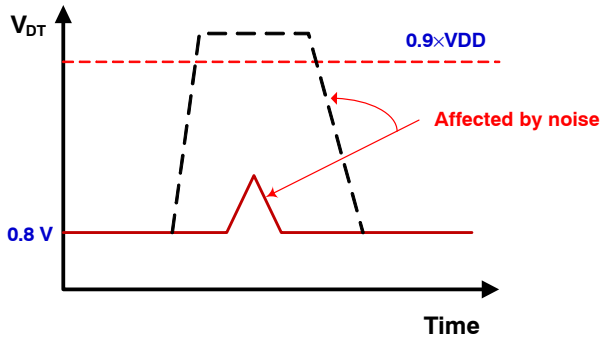


Figure 18. Defined Abnormal Waveforms when DT Pin is Floating

Therefore, it is recommended that add to the ceramic capacitor (C_{DT}), 2.2nF or above, close to the chip with R_{DT} to achieve better noise immunity and better dead−time matching between two channels as shown in Figure 19.

The major consideration is that the current through the R_{DT} is used to set the dead time, and this current decreases as R_{DT} value is increases.

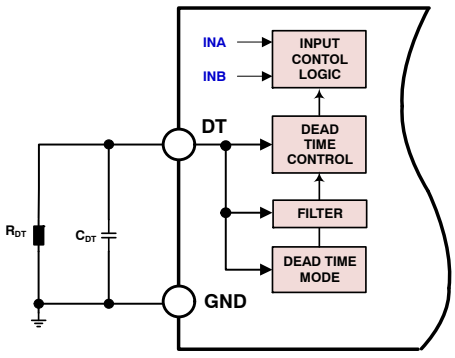
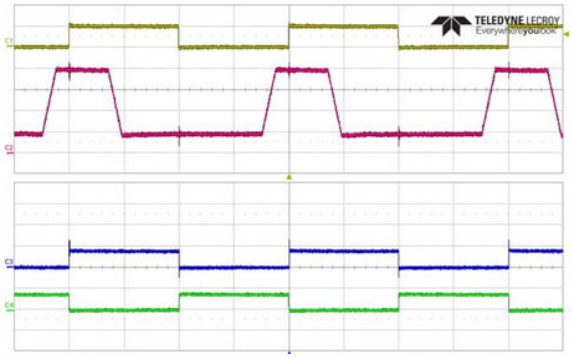


Figure 19. More Detailed Block Diagram of Dead−Time

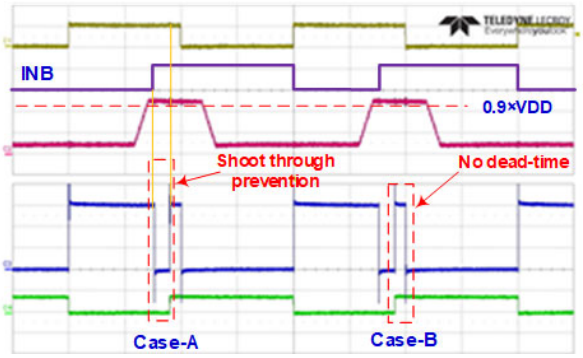
As test result, dead−time control mode does not change, i.e., keep going MODE−A mode, even though externally applied voltage below 0.9 × V_{DD} at V_{DD} for 5−V condition when used the DT pin is floating as shown in Figure 20.



CH1: INA and INB is inverted INA with 50% duty (5V/div), CH2: DT (1V/div), CH3: OUTA (20V/div), and CH4: OUTB (20V/div)

Figure 20. Experimental Waveforms when Externally Applied Voltage below 0.9 × V_{DD} at DT Pin is Floating

Whereas the dead−time mode change to MODE−C from MODE−A mode such as Case−B, i.e., cross−conduction both channel outputs is allowed, when externally applied voltage above 0.9 × V_{DD} with above 3 μs period at V_{DD} for 5−V condition when used the DT pin is floating as shown in Figure 21. As shown in Case−A, Shoot−through prevention feature is still operating because the dead−time control mode does not change due to internal 3 μs filter time for DT pin open detection.

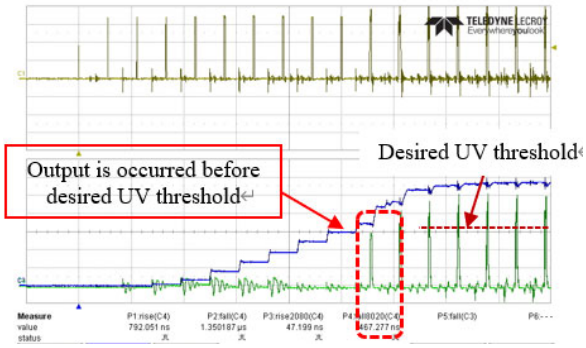


CH1: INA(5V/div), CH2: DT(2V/div), CH3: OUTA (5V/div), and CH4: OUTB (20V/div)

Figure 21. Experimental Waveforms when Externally Applied Voltage above 0.9 × V_{DD} at DT Pin is Floating

What do I need to know about power up delay when designing a driver V_{CC}?

Startup time is important factor in designing a circuit that is both energy efficient and fast for the driver used. So that minimal startup time is required. However, the startup time is limited by the power up delay, defined as the time the driver is enabled to the first gate output. As with many circuits, the minimal power up delay for the driver used, and can be found in the datasheet and it is defined as $t_{VPOR\ to\ OUT}$. For example, the **onsemi**'s isolated gate driver has a V_{CC} power−up delay time of typically 18 μs. It is recommends allowing some margin before driving input signals, to ensure the driver V_{CC} bias supplies are fully activated. Especially, NCP51561 and NCP51563 are recommended that the VCC power−up delay time allow for proper margin. For example, the VCC power−up time is required at least 30 μs or above during initial start−up after any VCC POR as shown in Figure 23 (B). If the V_{CCX} power up slope is such that the V_{CCX} rising time is less than $t_{VPOR\ to\ OUT}$ and there are PWM signals on INx pins, the outputs will start switching before V_{CC} reached its actual UVLO threshold whenever the V_{CCX} supply cross above the preset UVLO threshold (e.g., V_{CC}=6−V) and then stop till UVLO level is reached and experimental result as shown in Figure 22.



CH1: INA, CH3: VCCA, and CH4: OUTA_VSSA

Figure 22. Waveform when V_{CC} Power−up time less than $t_{VPOR\ to\ OUT}$

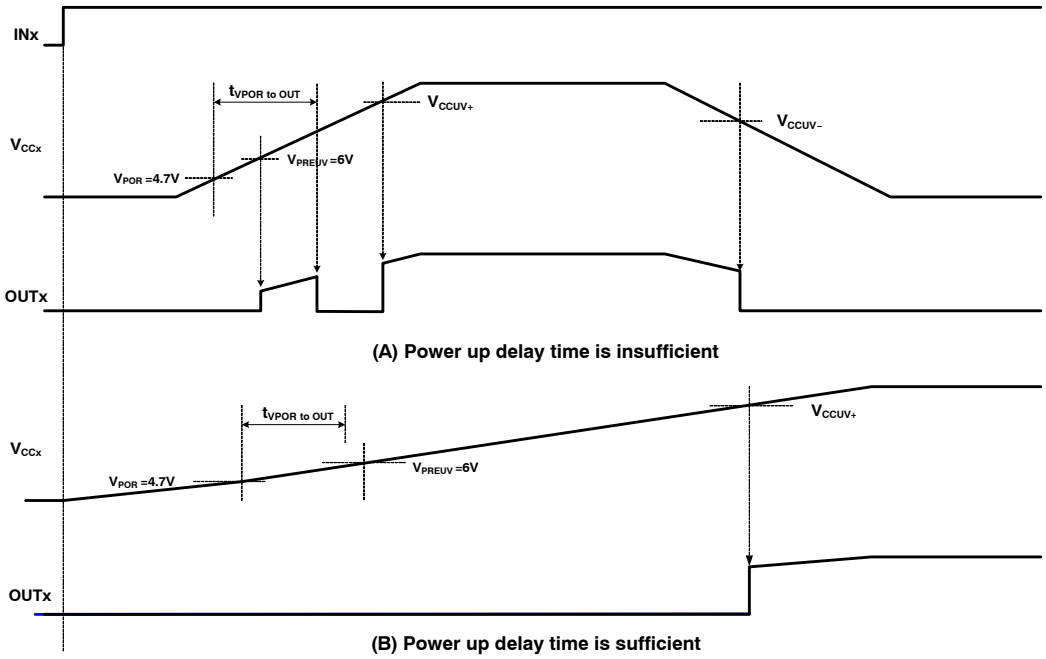


Figure 23. V_{CC} Power−up Delay Time

NCP51560 provides modified the V_{CC} power−up delay time control method to solve the problem above mentioned before as shown in Figure 24. Before the gate driver is ready to deliver a proper output state, there is a power−up delay time from the V_{CC} power−on reset (POR) threshold to output and it is defined as $t_{VPOR\ to\ OUT}$. (e.g. typically 18 μs).

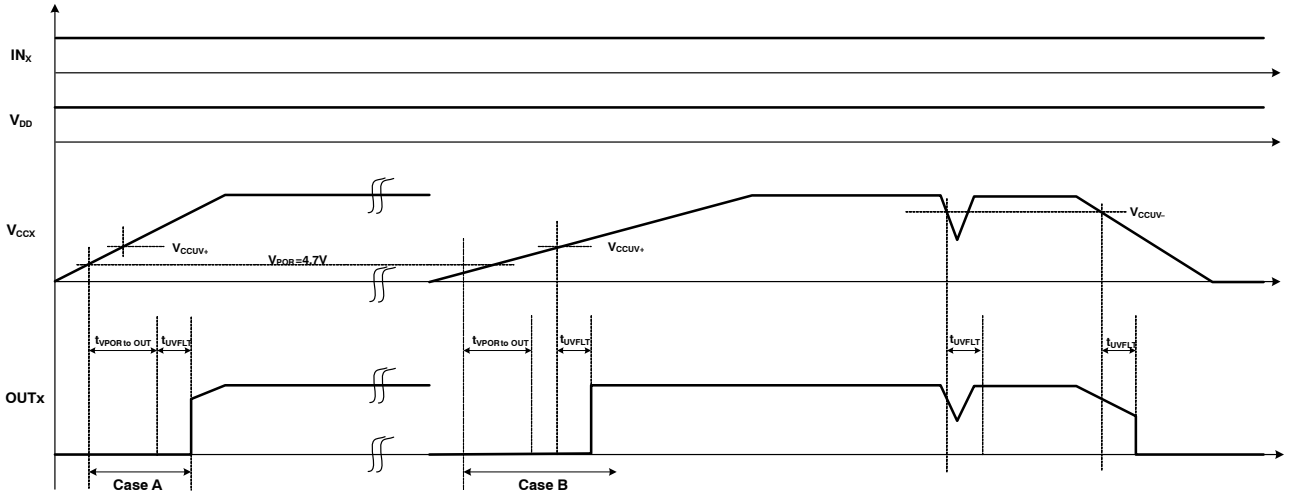
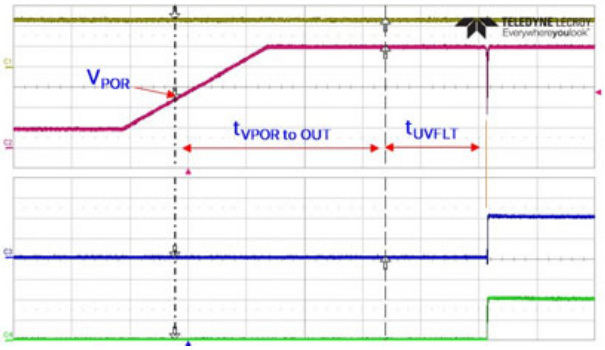


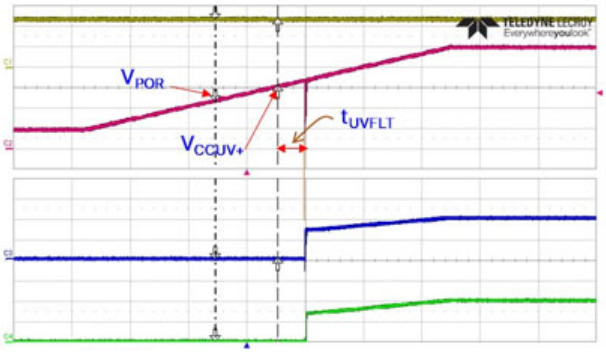
Figure 24. Newly Concept of V_{CC} Power−up Delay Time

If the V_{CC} power−up time is less than the $t_{VPOR\ to\ OUT}$ condition at the initial V_{CC} start−up, the output turns on after power−up delay time as shown in Figure 25 (A).

Whereas if the V_{CC} power−up time is longer than the $t_{VPOR\ to\ OUT}$ condition at the initial V_{CC} start−up, the output turns on when the V_{CC} supply is greater than the UVLO positive threshold voltage as shown in Figure 25 (B).



(A) In case of V_{CC} power−up time less than $t_{VPOR\ to\ OUT}$



(B) In case of V_{CC} power−up time longer than $t_{VPOR\ to\ OUT}$
CH1: Inx (2V/div), CH3: VCC (2V/div), CH3: OUTA and CH4: OUTB (5V/div)

Figure 25. Waveform of V_{CC} Power−up Time

Common Mode Transient Immunity (CMTI) Test

Figure 26 shows a simplified diagram od the CMTI testing configuration.

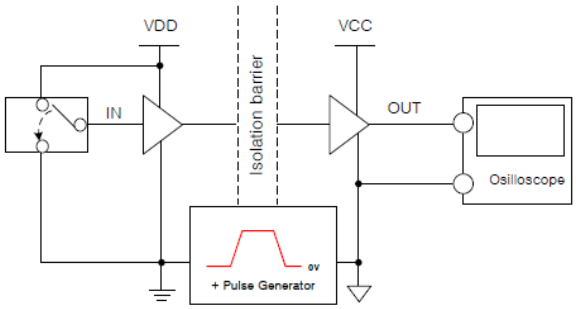
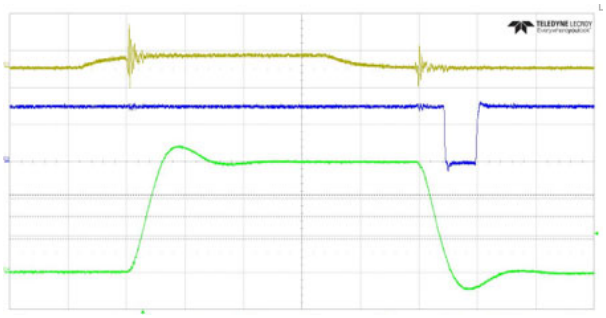


Figure 26. Simplified CMTI Testing Setup

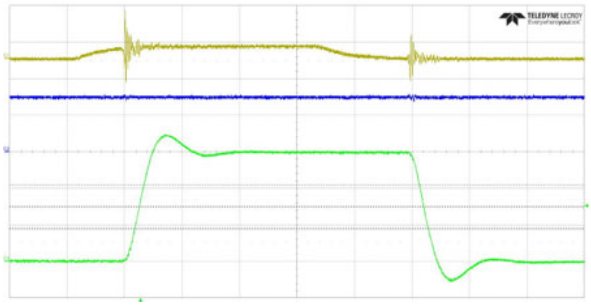
CMTI level is the maximum sustainable common−mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common−mode voltage edges. CMTI is tested with the transient generator connected between GND and V_{SSA} and V_{SSB}.

For example, some isolated gate drivers show the poor characteristics against the common-mode transient noise immunity. As a test result, output state change to low from high state at the falling dV/dt slope as shown in Figure 27 (A).

However, most of the **onsemi**'s isolated gate drivers have immune to common-mode transients as high as up to 200 kV/μs as shown in Figure 27 (B).



(A) Examples of failure at CMTI test



(B) Examples of no failure at CMTI test
CH1: INPUT (20V/div), CH3: OUTPUT (10V/div), and CH4: Applied dV/dt voltage (500V/div)

Figure 27. Waveform of CMTI Test

Output Load Characteristics

Isolated gate driver output signals depend on the characteristics of the output load, which is typically an N−channel MOSFET. The driver output response to an N−channel MOSFET load can be modeled with a switch output resistance (R_{SW}), an inductance due to the printed circuit board trace (L_{TRACE}), a series gate resistor (R_{GATE}), and a gate−to−source capacitance (C_{GS}), as shown in Figure 28.

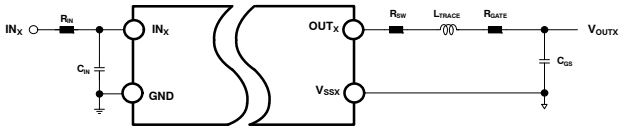


Figure 28. RLC Model of the Gate Drive with the MOSFET

R_{SW} is the switch resistance of the internal isolated gate driver output, which is typically about 1.4 Ω. R_{GATE} is the

intrinsic gate resistance of the MOSFET and any external series resistance.

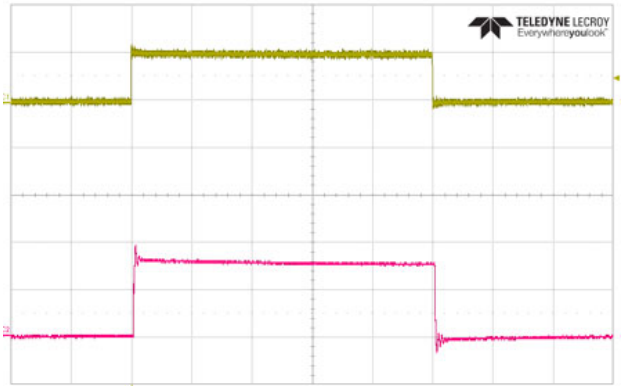
L_{TRACE} is the inductance of the printed circuit board trace, typically a value of 5 nH or less for a well−designed layout with a very short and wide connection from the isolated gate driver output to the gate of the MOSFET.

The following equation defines the Q factor of the RLC circuit, which indicates how the gate driver output responds to a step change. For a well−damped output, Q is less than 1. Adding a series gate resistance dampens the output response.

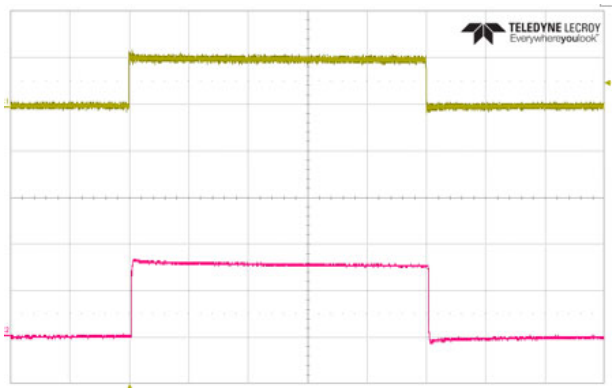
$$Q = \frac{1}{(R_{SW} + R_{GATE})} \times \sqrt{\frac{L_{TRACE}}{C_{GS}}}$$

An isolated gate driver output waveforms shows the small amount of ringing of the output with C_{GS} of 2 nF, R_{SW} of 1.4 Ω, and R_{GATE} of 0 Ω at 15 V output supply as shown in Figure 29 (A). Output ringing can be reduced by adding a series gate resistance to dampen the response.

For example, it is recommended to add a series gate resistor of about 2 Ω to 5 Ω and output waveform for a C_{GS} of 2 nF with 5 Ω series resistance as shown in Figure 29 (B).



(A) 2 nF load without series gate resistance



(B) 2 nF Load with 5 Ω series gate resistance
CH1: IN (5V/div), and CH2: OUTPUT (10V/div)

Figure 29. Output Waveform for 2 nF Load Capacitance

CONSIDERATION OF BOOTSTRAP APPLICATION CIRCUITS

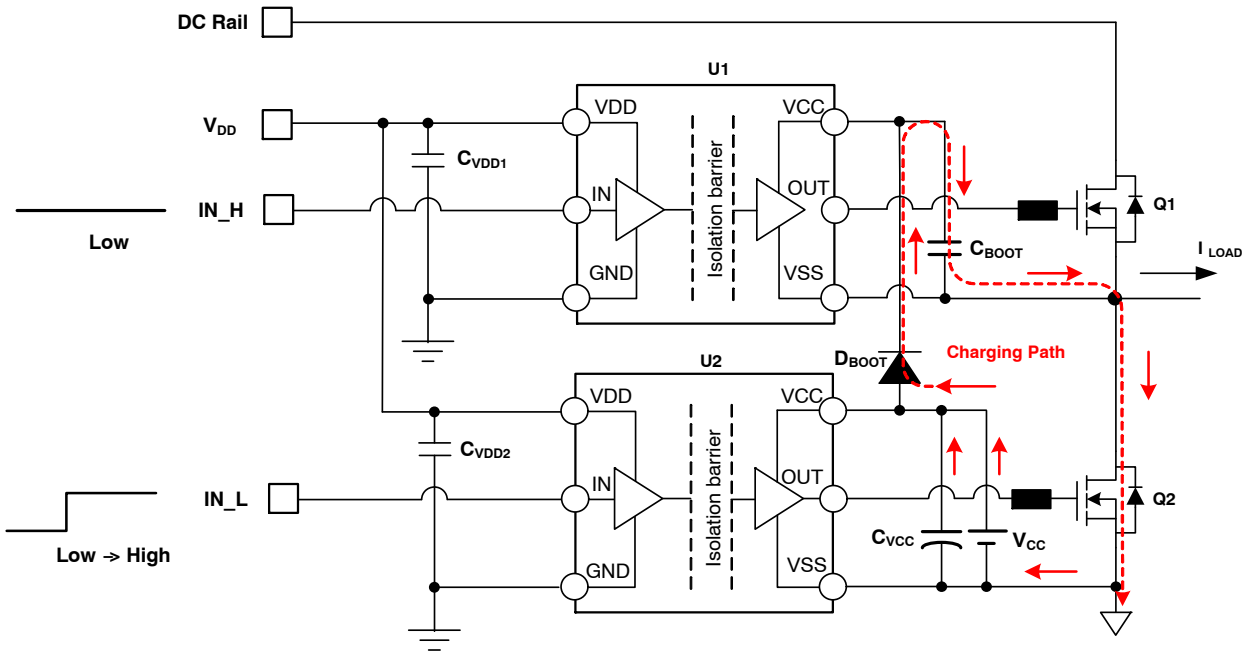


Figure 30. Current Path of Charging CBOOT in the Bootstrap Circuit

The bootstrap circuit can be considered in the half−bridge structure to supply V_{DD} as an inexpensive and simple solution. But it has some with limitations, such as, the duty cycle and on−time are both constrained by the need to refresh the bootstrap capacitor, C_{BOOT}.

The current path of charging C_{BOOT} is describes in Figure 30. When the VCC of U1 goes below the V_{CC} supply of U2 (Q2 is turned on and Q1 is turned off).

The C_{BOOT} charges through the bootstrap resistor (R_{BOOT}), and bootstrap diode (D_{BOOT}) from the V_{CC} power supply, as shown in Figure 30. When Q2 is turned off and Q1 is turned on, charged voltage on C_{BOOT} floats and D_{BOOT} protects U2 supply (V_{CC}) from DC rail voltage after reverse recovery time.

In addition, C_{BOOT} can be recharged during the low−side freewheeling recirculation even in the deadtime period when both Q1 and Q2 are off.

Bootstrap Components

The bootstrap resistor (R_{BOOT}) must be considered in sizing the bootstrap resistance and the current developed during initial bootstrap charge. The duty−cycle is limited by the requirement to refresh the charge in the C_{BOOT}, and there are startup problems. The C_{BOOT} uses a low−ESR capacitor, such as ceramic capacitor. The capacitor from VCC to VSS, (C_{VCC}) supports both the low−side driver, U1, and bootstrap recharge. A value at least ten times higher than the C_{BOOT} is recommended. The D_{BOOT} must use a lower forward voltage drop and switching time as soon as possible for fast recovery, such as ultra−fast.

Select the Bootstrap Capacitor

The C_{BOOT} is charged with repetitive cycle while VCC of U1 goes below the V_{CC} supply of U2 after turning on the low−side driver (U2). The bootstrap capacitor is discharged only when the high−side switch is turned on. Figure 31 describes simplified bootstrap circuit.

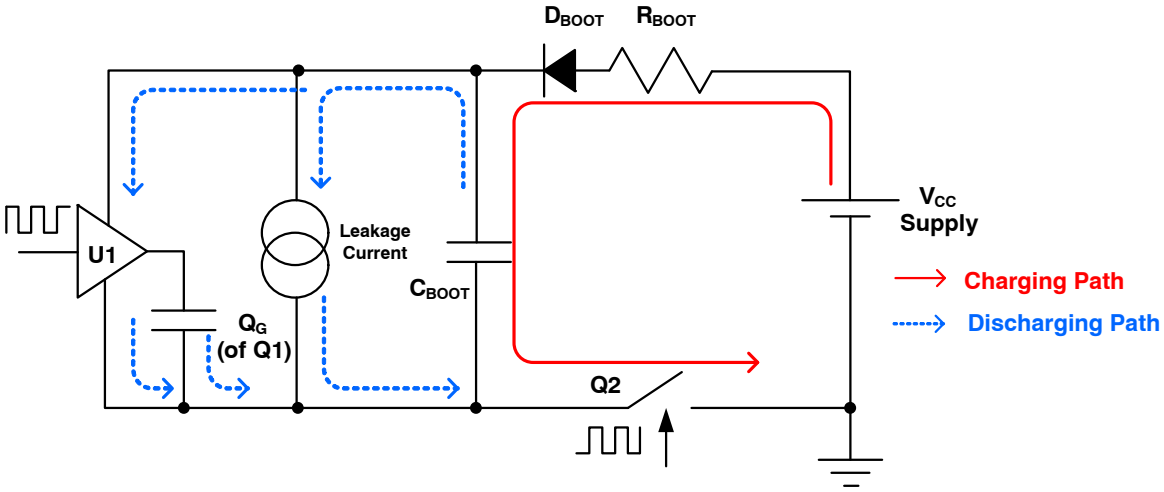


Figure 31. Simplified Bootstrap Circuit

If the voltage charged in C_{BOOT} is defined as V_{BOOT}, The first parameter to take into account is the maximum allowable voltage drop of V_{BOOT} to drive MOSFET properly. The maximum allowable voltage drop (V_{BOOT}) depends on the minimum gate drive voltage (for the high−side switch).

The value of bootstrap capacitor can be obtained with the below equation.

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}}$$

Where, Q_{TOTAL} is the total amount of the charge supplied by the capacitor.

The total charge supplied by the bootstrap capacitor is as shown in the below equation.

$$Q_{TOTAL} = Q_{GATE} + (I_{LKCAP} + I_{LKGS} + I_{QVCC} + I_{LKDIODE}) \times t_{ON}$$

where:

Q_{GATE} = Total gate charge;
I_{LKGS} = Switch gate−source leakage current;
I_{LKCAP} = Bootstrap capacitor leakage current;
I_{QVCC} = Quiescent current of gate driver;
t_{ON} = High−side switch on time; and
$I_{LKDIODE}$ = Bootstrap diode leakage current.

The capacitor leakage current is important only if an electrolytic capacitor is used; otherwise, this can be neglected.

For example:

The following is the sample of calculation to examine proper value of bootstrap capacitor when the external bootstrap diode used.

- Gate Drive IC = NCP51561 (**onsemi**)
- Switching Device = NVH4L020N120SC1 (**onsemi**)
- Bootstrap Diode = STTH112 (ST)
- V_{CC} = 18 V
- Q_{GATE} = 264 nC (Typ x 1.2)

- I_{LKGS} = 1 μA (Maximum)
- I_{LKCAP} = 0 (Ceramic Capacitor)
- I_{QVCC} = 600 μA (Maximum)
- t_{ON} = 7 μs (Duty = 70% at fs = 100 kHz)
- $I_{LKDIODE}$ = 50 μA

If the maximum allowable voltage drop on the bootstrap capacitor is 1.0 V during the high side switch on state, the total charge is able to calculate.

$Q_{TOTAL} = 264 \times 10^{-9} + (0 + 1 \times 10^{-6} + 600 \times 10^{-6} + 50 \times 10^{-6}) \times 7 \times 10^{-6} = 268.6 \times 10^{-9}$ [C]

The value of bootstrap capacitor is

$C_{BOOT} = Q_{TOTAL} / \Delta V_{BOOT} = 268.6 \times 10^{-9}/1 \approx 270$ [nF]

The voltage drop due to the external diode is nearly 0.7 V. Assume the capacitor charging time is equal to the high−side on−time (duty cycle 70%). According to different bootstrap capacitor values, the following equation applies:

$$\Delta V_{BOOT} = \frac{Q_{TOTAL}}{C_{BOOT}}$$

220 nF → ΔV_{BOOT} = 1.22 [V]
330 nF → ΔV_{BOOT} = 0.81 [V]
470 nF → ΔV_{BOOT} = 0.57 [V]
1000 nF → ΔV_{BOOT} = 0.27 [V]

Suggested values are within the range of 470 nF ~ 1000 nF, but the right value must be selected according to the application in which the device is used. When the capacitor value is too large, the bootstrap charging time slows and the low−side on time might be not long enough to reach the bootstrap voltage.

Select the Bootstrap Resistor

When the external bootstrap resistor is used, the resistance, R_{BOOT}, introduces an additional voltage drop:

$$V_{RBOOT} = \frac{I_{CHARGE} \times R_{BOOT}}{t_{CHARGE}}$$

where:
I_{CHARGE} = Bootstrap capacitor charging current;
R_{BOOT} = Bootstrap resistance; and
t_{CHARGE} = Bootstrap capacitor charging time (the low−side turn−on time).

Do not exceed the ohms (typically 5~10 Ω) that increase the VBS time constant. This voltage drop of bootstrap diode must be taken into account when the maximum allowable voltage drop (V_{BOOT}) is calculated. If this drop is too high or the circuit topology does not allow a sufficient charging time, a fast recovery or ultra−fast recovery diode can be used.

Calculation for Min Duty Cycle

The charged and discharged voltage of V_{BOOT} is varied by controlling Q1 and Q2.

Figure 32 describes timing chart of bootstrap charging cycle of V_{BOOT}.

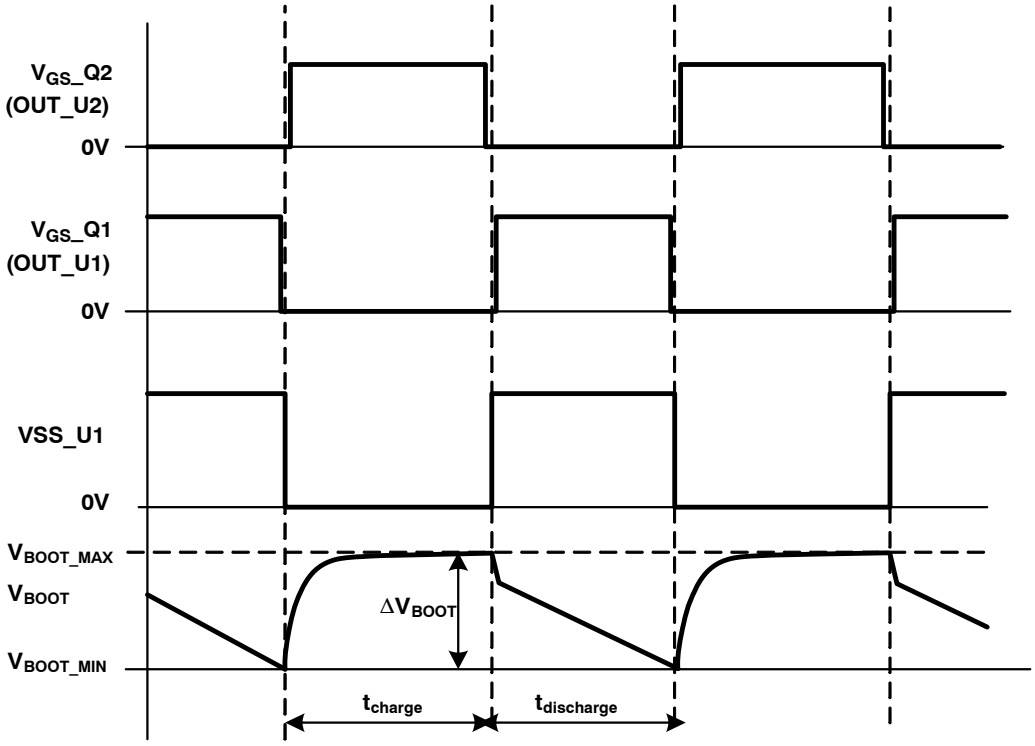


Figure 32. Timing Chart of Bootstrap Charging Cycle

To ensure proper charging C_{BOOT} in Figure 30, the minimum duty cycle of Q2, low−side MOSFET, should be considered.

The increased voltage of C_{BOOT} during charging time (t) can be calculated.

$$V_{BOOT}(t) = \left(V_{CC} - V_{BOOT\_MIN} - V_F - V_{LS}\right) \times \left(1 - e^{-\frac{t}{R_S \times C_{BOOT}}}\right)$$

V_{BOOT_MIN} is minimum Voltage of C_{BOOT} at the end of discharge, and R_S is the equivalent series resistance of the bootstrap circuit including the on−resistance of V_{BOOT}.

If C_{BOOT} is charged whenever Q2 is tuned on, the charged voltage of C_{BOOT} (V_{CBOOT}) should higher than the voltage drop of V_{BOOT} when Q1 is turned on

$$V_{BOOT}(t) > \Delta V_{BOOT}$$

If the maximum and minimum values charged to Cboot are defined as V_{BOOT_MAX} and V_{BOOT_MIN} respectively, the below equation is established.

$$V_{BOOT\_MIN} = V_{BOOT\_MAX} - \Delta V_{BOOT}$$

Since ΔV_{BOOT} is obtained by Q_{TOTAL}/ C_{BOOT}, it can be explained by the formula below.

$$D_{MIN} > -\ln\left(1 - \frac{\frac{Q_{TOTAL}}{C_{BOOT}}}{V_{CC} - V_F - V_{LS} - \left(V_{BOOT\_MAX} - \frac{Q_{TOTAL}}{C_{BOOT}}\right)}\right) \times f_{SW} \times R_S \times C_{BOOT}$$

where:

C_{BOOT} = Bootstrap capacitor;

Q_{TOTAL}= The total charge supplied by the C_{BOOT};

V_{BOOT}= Voltage of C_{BOOT};

V_{BOOT_MIN}= Minimum voltage of C_{BOOT} at the end of discharge phase;

V_{BOOT_MAX}= Maximum voltage of C_{BOOT} at the end of discharge phase;

V_F= Forward voltage drop of D_{BOOT};

V_{LS}= Voltage drop across the low−side MOSFET;

f_{SW}= Switching frequency; and

R_S = the equivalent series resistance of the bootstrap circuit including the on−resistance of V_{BOOT}

For high−speed switching applications, the Rs value should be minimized to ensure sufficient charging time.

For example:

The following is the sample of calculation to examine proper value of min duty cycle of low−side MOSFET in a half−bridge circuit as shown in Figure 30.

In this particular case, V_{BOOT_MAX} is assumed to be 95% of (V_{CC}−V_F).

- Gate Drive IC = NCP51561 (**onsemi**)
- Switching Device = NVH4L020N120SC1 (**onsemi**)
- Bootstrap Diode = STTH112 (ST)
- V_{CC} = 18 V
- C_{BOOT} = 470 nF
- Q_{TOTAL}= 268.6 nC
- V_{BOOT_MAX} = 16.6 V
- V_F= 0.5 V
- V_{LS}= 0.3 V
- f_{SW}= 100 kHz
- R_S = 1 Ω

The required min duty cycle of low−side MOSFET is

$$-\ln\left(1 - \frac{\frac{Q_{TOTAL}}{C_{BOOT}}}{V_{CC} - V_F - V_{LS} - \left(V_{BOOT\_MAX} - \frac{Q_{TOTAL}}{C_{BOOT}}\right)}\right) \times f_{SW} \times R_S \times C_{BOOT} = 3.24\ [\%]$$

Consideration for Bootstrap Circuit

Since the Bootstrap method has limitations, it should be applied to the application in consideration of this. Table 2 below shows the limitation for each topology when applying the bootstrap method in comparison to other alternative methods.

Table 2. APPLICABLE METHOD FOR H/S POWER SUPPLY

	PWM Topology	PFM Topology (50% duty)
Bootstrap Method	Applicable with limitations; Limited by duty cycle, R_{BOOT} and C_{BOOT}	Applicable with limitations; Limited by R_{BOOT} and C_{BOOT}
Isolated Power supply, Charging Pump (for 100% duty)	Applicable without limitations (except for current capability)	

Consideration of the Gate Driver Power Loss

Estimating Gate driver Powe Loss

The supply current at a given channel of an isolated gate driver is a function of the supply voltage, switching frequency, and output load. In generally, gate driving total power loss, P_{GDRV}, consist of static power loss, P_{GDQ}, and dynamic power loss, P_{GDSW}.

Bootstrap diode loss is not included in total loss, P_{GDRV}, and not discussed in this section. The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self−power consumption when operating switching frequency.

P_{GDQ} is measured on the bench with no load connected to OUTA and OUTB at a given V_{DD}, V_{CCA}/V_{CCB}, switching frequency and ambient temperature.

$$P_{GDQ} = (V_{DD} \times I_{DD}) + 2 \times (V_{CC} \times I_{CC})$$

where: I_{DD} and I_{CC} are measured current at supply voltages (V_{DD} and V_{CC}) and target switching frequency

The second component is the dynamic operation loss, P_{GDSW}, with load capacitance which the driver charges and discharges the load during each switching cycle.

For example, the gate of a MOSFET can be simulated approximately as a capacitive load.

Due to miller capacitance, C_{GD}, and other nonlinearities, it is common practice to take the stated input capacitance, C_{iss}, of a given MOSFET and multiply it by a factor of 5 at a conservative estimate to approximate the load being driven.

$$P_{GDSW} = C_{EST} \times V_{CC}X^2 \times f_{SW}$$

where: $C_{EST} = C_{iss} \times 5$. f_{SW} is the switching frequency.

Alternately, use the gate charge to obtain a more precise value for P_{GDSW}.

$$P_{GDSW} = V_{CC} \times Q_G \times f_{SW}$$

where: Q_G is the total gate charge of switching device. f_{SW} is the switching frequency.

Therefore, total gate driving power loss, P_{GDRV}, can be calculated

$$P_{GDRV} = P_{GDQ} + P_{GDSW}\ [W]$$

In this example, V_{DD} = 5 V, V_{CC} = 25 V and Q_G = 50 nC. The current on each power supply, with INA and INB switching from 0 V to 5 V at 250 kHz is measured to be I_{DD} = 6.5 mA, and $I_{CCA} = I_{CCB}$ = 2.7 mA.

Therefore, the total power loss, P_{GDRV}, can be calculated with

$P_{GDRV} = P_{GDQ} + P_{GDSW}$ = (5 V × 6.5 mA) + (2 × 25 V × 2.7 mA) + (2 × 25 V × 50 nC × 250 kHz) = 782 mW

An isolated gate driver loss on the output stage, P_{GDO}, is part of P_{GDSW}. P_{GDO} will be equal to P_{GDSW} if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside an isolated gate driver.

If there are external turn−on and turn−off resistances, this power dissipation is shared between the internal on resistances of the gate driver switches and the external gate resistances, R_{ON} and R_{OFF}. The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within an isolated gate drive chips per channel.

$$P_{GDO} = \frac{P_{GDSW}}{2} \times \left(\frac{R_{PMOS}}{R_{ON} + R_{GFET\_int}} + \frac{R_{NMOS}}{R_{OFF} + R_{GFET\_int}} \right)$$

Therefore, total gate driver loss dissipated in the gate driver, P_{GDRV}, is:

$$P_{GDRV} = P_{GDQ} + P_{GDO}\ [W]$$

Estimating Junction Temperature

Taking the power dissipation found inside the chip and multiplying it by $R_{\theta JA}$ gives the rise above ambient temperature that an isolated gate driver can be estimated with:

$$T_J = R_{\theta JA} \times P_{GDRV} + T_A \quad \text{Or}$$

$$T_J = T_C + \psi_{JT} + P_{GDRV}$$

where: $R_{\theta JA}$ is the thermal resistance junction−air from the thermal information table in datasheet.

T_C is an isolated gate drive IC case−top temperature measured with a thermocouple or some other instrument.

Ψ_{JT} is the Junction−to−top characterization parameter from the thermal information table in datasheet.

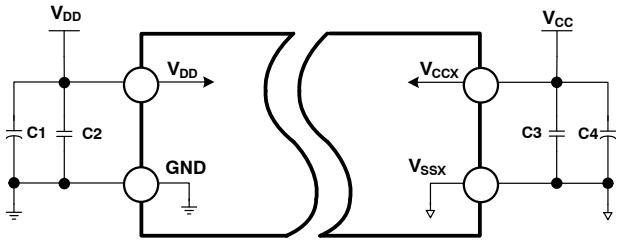
For the device to remain within specification, T_J must not exceed 125°C.

PCB Layout Guideline

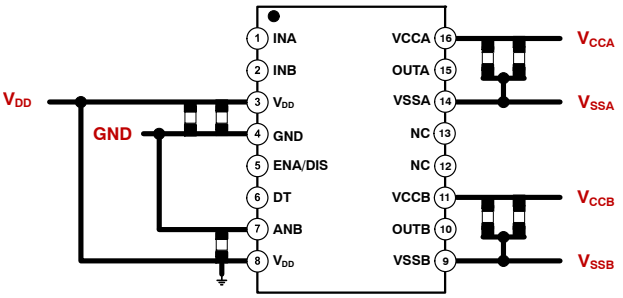
Isolated gate drivers do not require an external interface circuitry for the logic interfaces.

The input and output supply pins require supply bypass capacitors as shown in Figure 33.

Specially, the bypass capacitor on the output supply pin use of vias must be avoided or multiple vias must be employed to reduce the inductance in the bypassing. Placement and routing for supply bypass capacitors for V_{DD} and V_{CCA}, or V_{CCB} need to be located as close as possible to the power supply pins.



(A) Recommended Power Supply Bypass Capacitance



(B) Recommended Placement of Bypass Capacitor

Figure 33. Recommended Supply Bypass Capacitor

To improve the switching characteristics and efficiency of design, the following should be considered before beginning a PCB layout.

Component Placement

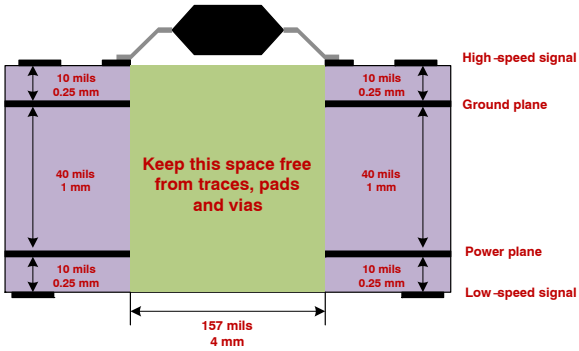
- Keep the input/output traces as short as possible. Minimize influence of the parasitic inductance and capacitance on the layout. (To maintain low signal−path inductance, avoid using via.)
- Placement and routing for supply bypass capacitors for V_{DD} and V_{CCA}, or V_{CCB} and gate resistors need to be located as close as possible to the gate driver.
- The gate driver should be located switching device as close as possible to decrease the trace inductance and avoid output ringing.

Grounding Consideration

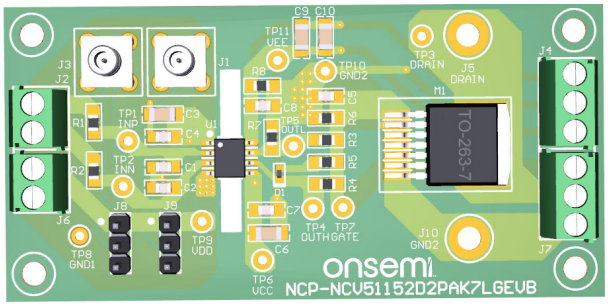
- Have a solid ground plane underneath the high−speed signal layer.
- Have a solid ground plane next to V_{SSA} and V_{SSB} pins with multiple V_{SSA} and V_{SSB} vias to reduce the parasitic inductance and minimize the ringing on the output signals.

High−Voltage (V_{ISO}) Consideration

- To ensure isolation performance between the primary and secondary side, any PCB traces or copper should be not place under the driver device for narrow and wide body packages respectively as shown in Figure 34 and Figure 35. A PCB cutout is recommended to prevent contamination that may impair the isolation performance of the isolated gate driver.

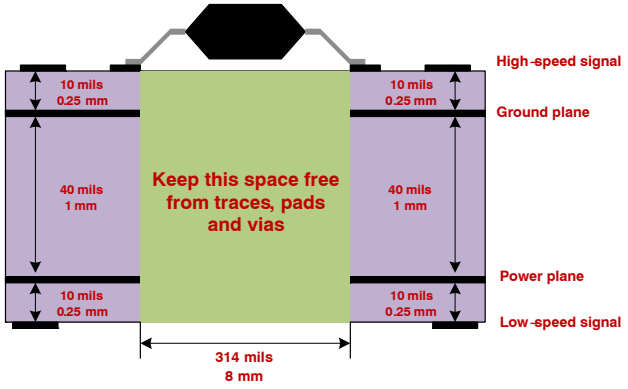


(A) Recommended Layer Stack

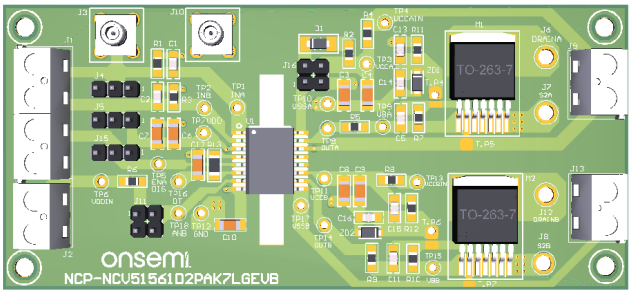


(B) Example of evaluation board

Figure 34. Recommended PCB Layout of the Narrow−body Package



(C) Recommended Layer Stack



(D) Example of evaluation board

Figure 35. Recommended PCB Layout of the Wide−body Package

Reference

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