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TSic 716 TO92

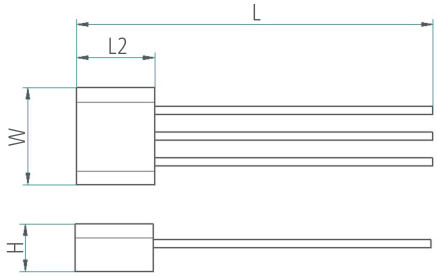
Temperature Sensor IC

For a fully calibrated and extremely accurate low power temperature measurement

Benefits & Characteristics

- Easy to integrate (digital output signal)
- Outstanding accuracy of ±0.07 K
- Very low power consumption
- Fully calibrated
- Excellent long-term stability
- Accuracy range of 20 K can be shifted (default: +25 °C to +45 °C)
- Capable of communicating over a distance of > 10 m

Illustration

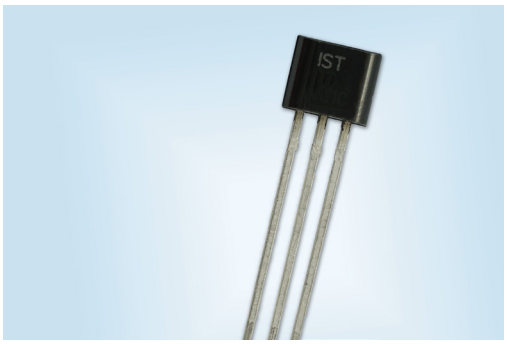


Technical Data

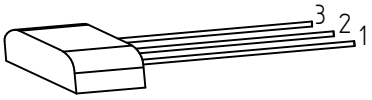
Dimensions (L / L2 x W x H in mm): [2)]	17.30 / 3.81 x 4.57 x 2.3
Operating temperature range:*	-10 °C to +60 °C (-7 °C to +57 °C guaranteed)
Accuracy:*	±0.07 K in the range of +25 °C to +45 °C
Resolution:*	4 mK
Sampling rate:*	1 Hz
Supply voltage:	4.5 V to 5.5 V
Supply current:	typ. 45 µA at 25 °C and 5 V for minimal self-heating
Packaging:*	TO92
Output signal:	14 bit ZACWire - see application note ATTSic_E

2) For tolerances, see Application Note

Product Photo



Pin Assignment



	Pin 1	Pin 2	Pin 3
TO92	GND	Signal	V_{dd}, Supply voltage (3 V to 5.5 V)

Absolute maximal ratings

	Min	Max
Supply voltage (V_{dd})	-0.3 V	6 V
Voltages to analog I/O – Pins (V_{SIG}, V_{GND})	-0.3 V	V_{dd}+0.3 V
Storage temperature range (T_{STOR})	-10 °C	+60 °C
Non-operating temperature range		

Operating conditions

	Min	Typ	Max
Supply voltage to GND (V^+)	2.97 V	5 V	5.5 V
Supply current (I_{Vdd}) at V_{dd} = 3.3 V, RT	30 µA	45 µA	80 µA
Operating temperature range (T_{amb})	-10 °C		+60 °C
Output load capacitance (C_L)			15 nF
External capacitance between V_{dd} and GND[1)]	100 nF (recommended)		
Output load resistance between signal and GND (or V_{dd})	47 kΩ		

[1)] Recommended as close to TSic V_{dd} and GND-Pins as possible

Temperature accuracies[2)]

T1: +25 °C to +45 °C	±0.07 K
T2: -10 °C to +60 °C	±0.2 K

[2)] The sensor is calibrated at 5 V. The provided accuracy is applicable for a supply voltage between 4.5 V and 5.5 V. The accuracy is smaller with a supply voltage between 2.97 V and 4.5 V. For applications where the best accuracy at 3 V is requested, ask for a custom specific, 3 V calibrated device. Other TSic products with custom specific calibrations are available upon request e.g. other temperature range for high accuracy. Accuracy at delivery; the assembly method can influence the accuracy!

Order Information

Description:	Item number:	Former main reference:
TSic 716 TO92	103493	030.00048

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Application Note
Temperature Sensor IC
Content

1. TSic 206/203/201/306/316/303/301

The TSic series of temperature sensor ICs are specifically designed as a low-power solution for temperature measurement in building automation, medical/pharma technologies, industrial and mobile applications. The TSic provides a simple temperature measurement and achieves outstanding accuracy combined with long term stability.

The TSic has a high precision bandgap reference with a PTAT (proportional-to-absolute-temperature) output, a low-power and high-precision ADC and an on-chip DSP core with an EEPROM for the precisely calibrated output signal. The TSic temperature sensor is fully calibrated, meaning no further calibration effort is required by the customer.

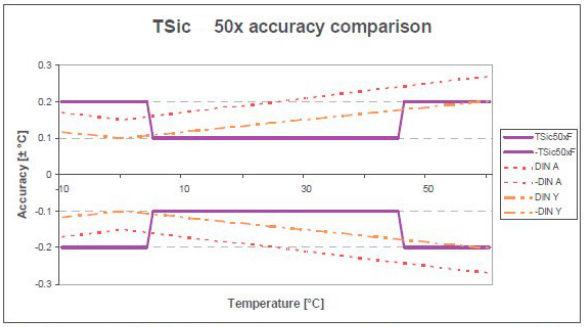


Figure 1: Comparison of TSic <--> platinum sensor accuracy

Extended long wires (> 10 m) will not influence the accuracy. The TSic is available with digital (ZacWire™, TSic x06), analog (0 V to 1V, TSic x01) or ratiometric (10 % to 90 % V+, TSic x03) output signal. The low power consumption of about 35 µA makes it suitable for many applications.

With an accuracy of ±0.3 K in a temperature range of 80 K (e.g. +10 °C to +90 °C), the TSic sensors are more accurate than a class F0.3 (IEC60751) platinum sensor. The tolerances of the TSic and F 0.3 and F 0.15 platinum sensors are compared in Figure 1. With a standard calibration, the TSic 30x is more accurate than a F 0.3 platinum sensor in the range of +10 °C to +110 °C. The range can be shifted up or downwards to reach a high accuracy between e.g.
-30 °C to +50 °C.

Output examples	Temperature Range: -50 °C to +150 °C		
Temp (°C)	Digital Values (TSic x06)	Analog 0 V to 1 V (TSic x01)	Analog Ratiometric 10 % to 90 % (V+ = 5.0 V) (TSic x03)
-50 [1]	0x000	0.000	10 % V+ (0.5 V)
-10	0x199	0.200	26 % V+ (1.3 V)
0	0x200	0.250	30 % V+ (1.5 V)
25	0x2FF	0.375	40 % V+ (2.0 V)
60	0x465	0.550	54 % V+ (2.7 V)
125	0x6FE	0.875	80 % V+ (4.0 V)
150 [2]	0x7FF	1.000	90 % V+ (4.5 V)

1) LT = -50 2) HT = 150 as standard value for the temperature calculation

Formulas for the output signal [°C]:

Analog output (0 V to 1 V): $T = Sig\,[V] \times (HT - LT) + LT\,[°C]$

Ratiometric output (10 % to 90 %): $T = \frac{\frac{Sig\,[V]}{V^+\,[V]} - 0.1}{0.8} \times (HT - LT) + LT \quad [°C]$

Digital output - 11 bit: $T = \frac{Digital\ signal}{2047} \times (HT - LT) + LT\,[°C]$

Digital output - 14 bit (TSic 316): $T = \frac{Digital\ signal}{16383} \times (HT - LT) + LT\,[°C]$

LT: Lower temperature limit [= -50 °C]
HT: Higher temperature limit [= +150 °C]
V^+: Supply voltage [V]
Sig[V]: Analog/ratiometric output signal [V]

2. TSic 506F/503F/516/501F

The TSic series of temperature sensor ICs are specifically designed as a low-power solution for temperature measurement in building automation, medical / pharma technologies, industrial and mobile applications. The TSic provides a simple temperature measurement and achieves outstanding accuracy combined with long term stability.
The TSic has a high precision bandgap reference with a PTAT (proportional-to-absolute-temperature) output, a low-power and high-precision ADC and an on-chip DSP core with an EEPROM for the precisely calibrated output signal.

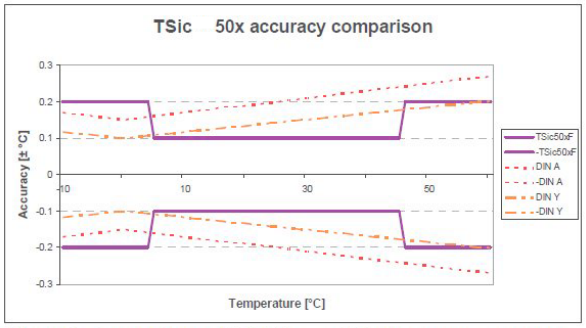


Figure 1: Comparison of TSic <--> platinum sensor accuracy

The TSic temperature sensor is fully calibrated, meaning no further calibration effort is required by the customer. With an accuracy of ±0.1 K in a range of 40 K (e.g. +5 °C to +45 °C), the sensor is more accurate than a class F0.1 (IEC 60751) platinum sensor. Extended long wires (> 10 m) will not influence the accuracy. The TSic is available with digital (ZacWire™, TSic 506F),analog (0 V to 1 V, TSic 501F) or ratiometric (10 % to 90 % V+, TSic 503F) output signal. The low power consumption of about 35 µA makes it suitable for many applications.

Output Examples	Temperature Range: -10 °C to +60 °C		
Temp (°C)	Digital Values (TSic x06)	Analog 0 V to 1 V (TSic x01)	Analog Ratiometric 10 % to 90 % (V+ = 5.0 V) (TSic x03)
< -10 to -10[1)]	0x000	0.000	10 % V+ (0.5 V)
0	0x124	0.143	21.4 % V+ (1.07 V)
25	0x3FF	0.500	50 % V+ (2.5 V)
+60[2] to > +60	0x7FF	1.000	90 % V+ (4.5 V)

1) LT = -10

2) HT = 60 as standard value for the temperature calculation

Formulas for the output signal [°C]:

Analog output (0 V to 1 V):

$$T = Sig\,[V] \times (HT - LT) + LT\,[°C]$$

Ratiometric output (10 % to 90 %):

$$T = \frac{\frac{Sig\,[V]}{V^+\,[V]} - 0.1}{0.8} \times (HT - LT) + LT \quad [°C]$$

Digital output - 11 bit:

$$T = \frac{Digital\ signal}{2047} \times (HT - LT) + LT\,[°C]$$

Digital output - 14 bit (TSic 516):

$$T = \frac{Digital\ signal}{16383} \times (HT - LT) + LT\,[°C]$$

LT: Lower temperature limit [= -10 °C]
HT: Higher temperature limit [= +60 °C]

V+: Supply voltage [V]
Sig[V]: Analog/ratiometric output signal [V]

3. TSic 716

The TSic series of temperature sensor ICs are specifically designed as a low-power solution for temperature measurement in building automation, medical/pharma technologies, industrial and mobile applications. The TSic provides a simple temperature measurement and achieves outstanding accuracy combined with long term stability. The TSic has a high precision bandgap reference with a PTAT (proportional-to-absolute-temperature) output, a low-power and high-precision ADC and an on-chip DSP core with an EEPROM for the precisely calibrated output signal. The IST AG TSic sensor is fully tested and calibrated to ensure the guaranteed accuracy.

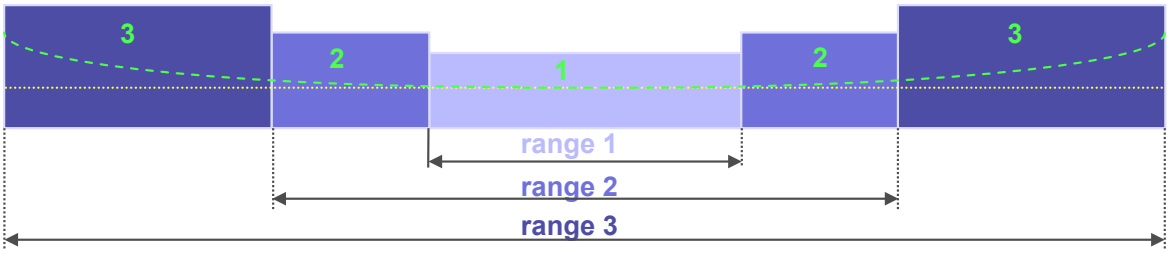
Output Examples	Temperature Range: -10 °C to +60 °C
Temp (°C)	Digital
+35	0x2925
+40	0x2DB7
+45	0x3249

Formulas for the output signal [°C]:

Digital output: $T = \frac{\text{Digital signal}}{16383} \times (HT - LT) + LT\ [°C]$

LT: Lower temperature limit [= -10 °C]
HT: Higher temperature limit [= +60 °C]
V+: Supply voltage [V]

4. TSic Accuracy Overview[1)]



Product	Resolution	Range 1	Accuracy 1	Range 2	Accuracy 2	Range 3	Accuracy 3
TSic 20x	0.1 °C	+10 °C to +90 °C	±0.5 °C	-20 °C to +110 °C	±1 °C	-50 °C to +150 °C	±2 °C
TSic 30x	0.1 °C	+10 °C to +90 °C	±0.3 °C	-20 °C to +110 °C	±0.6 °C	-50 °C to +150 °C	±1.2 °C
TSic 50x	0.034 °C	+5 °C to +45 °C	±0.1 °C	-	-	-10 °C to +60 °C	±0.2 °C
TSic 716	0.004 °C	+25 °C to +45 °C	±0.07 °C	-	-	-10 °C to +60 °C	±0.2 °C

1) Range 1 can be shifted to a customer specific temperature

5. ZACwire™ Digital Output

5.1 TSic ZACwire™ Communication Protocol

ZACwire™ is a single wire bi-directional communication protocol. The bit encoding is similar to Manchester in that clocking information is embedded into the signal (falling edges of the signal happen at regular periods). This allows the protocol to be largely insensitive to baud rate differences between the two ICs communicating. In end-user applications, the TSic will be transmitting temperature information, and another IC in the system (most likely a µController) will be reading the temperature data over the ZACwire™.

5.2 Temperature Transmission Packet from a TSic

The TSic transmits 1-byte packets. These packets consist of a start bit, 8 data bits, and a parity bit. The nominal baud rate is 8 kHz (125 µsec bit window). The signal is normally high. When a transmission occurs, the start bit occurs first followed by the data bits (MSB first, LSB last). The packet ends with an even parity bit.

Figure 1.1 – ZACwire™ Transmission Packet

The TSic provides temperature data with 11-bit or 14-bit resolution, and obviously these 11 bits or 14-bit of information cannot be conveyed in a single packet. A complete temperature transmission from the TSic consists of two packets. The first packet contains the most significant 3 bits or 6 bits of temperature information, and the second packet contains the least significant 8 bits of temperature information. There is a single bit window of high signal (stop bit) between the end of the first transmission and the start of the second transmission.

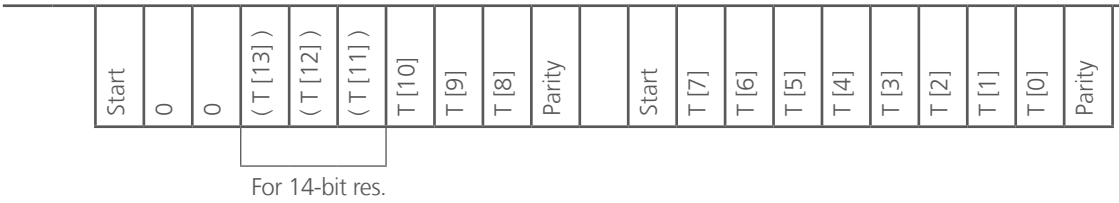
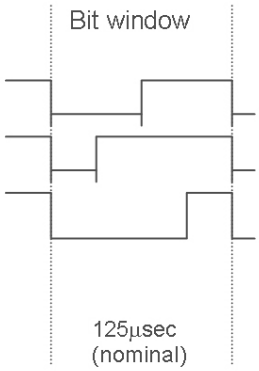


Figure 1.2 – Full ZACwire™ Temperature Transmission from TSic

5.3 Bit Encoding

The bit format is duty cycle encoded:

Start bit => 50 % duty cycle used to set up strobe time
Logic 1 => 75 % duty cycle
Logic 0 => 25 % duty cycle



Perhaps the best way to show the bit encoding is with an oscilloscope trace of a ZACwire™ transmission. The following shows a single packet of 96 Hex being transmitted. Because 96 Hex is already even parity, the parity bit is zero.

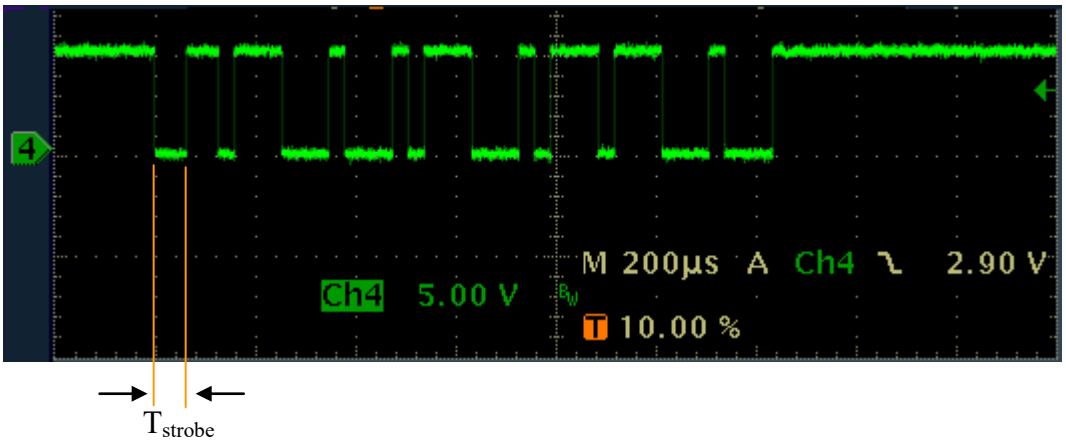


Figure 1.3 – ZACwire™ Transmission

5.4 How to Read a Packet

When the falling edge of the start bit occurs, measure the time until the rising edge of the start bit. This time (T_{strobe}) is the strobe time. When the next falling edge occurs, wait for a time period equal to T_{strobe}, and then sample the ZACwire™ signal. The data present on the signal at this time is the bit being transmitted. Because every bit starts with a falling edge, the sampling window is reset with every bit transmission. This means errors will not accrue for bits downstream from the start bit, as it would with a protocol such as RS232. It is recommended, however, that the sampling rate of the ZACwire™ signal when acquiring the start bit be at least 16x the nominal baud rate. Because the nominal baud rate is 8 kHz, a 128 kHz sampling rate is recommended when acquiring Tstrobe.

5.5 How to Read a Packet using a µController

It is best to connect the ZACwire™ signal to a pin of the µController that is capable of causing an interrupt on a falling edge. When the falling edge of the start bit occurs, it causes the µController to branch to its ISR. The ISR enters a counting loop incrementing a memory location (T_{strobe}) until it sees a rise on the ZACwire™ signal. When T_{strobe} has been acquired, the ISR can simply wait for the next 9 falling edges (8-data, 1-parity). After each falling edge, it waits for T_{strobe} to expire and then sample the next bit.
The ZACwire™ line is driven by a strong CMOS push/pull driver. The parity bit is intended for use when the ZACwire™ is driving long (> 2 m) interconnects to the µController in a noisy environment. For systems in which the "noise environment is more friendly", the user can choose to have the µController ignore the parity bit. In the appendix of this document is sample code for reading a TSic ZACwire™ transmission using a PIC16F627 µController.

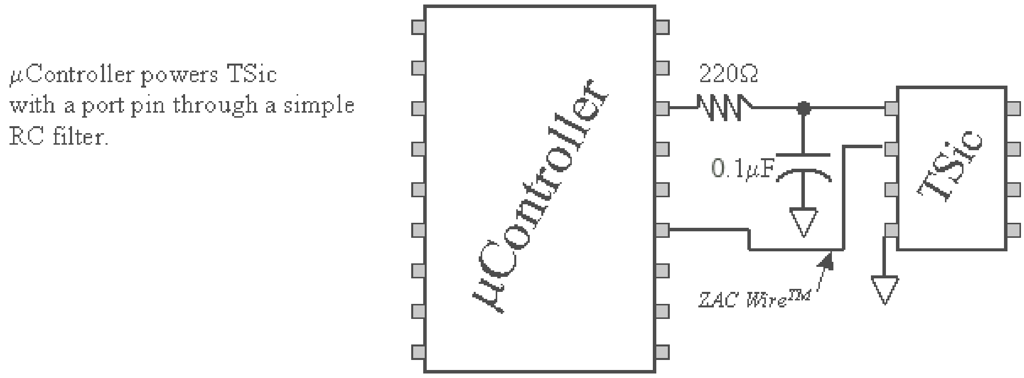
5.6 How Often Does the TSic Transmit?

If the TSic is being read via an ISR, how often is it interrupting the µController with data? The update rate of the TSic can be programmed to one of 4 different settings: 250 Hz, 10 Hz, 1 Hz, and 0.1 Hz. This is done during calibration of the sensor on IST AG side. The standard update rate is 10 Hz (TSic 206, TSic 306, TSic 506) or 1 Hz (TSic 716). For other update rates please contact IST AG. Servicing a temperature-read ISR requires about 2.7 ms. If the update rate of the TSic is programmed to 250 Hz, then the µController spends about 66 % of its time reading the temperature transmissions. If, however, the update rate is programmed to something more reasonable like 1 Hz, then the µController spends about 0.27 % of its time reading the temperature transmissions.

5.7 Solutions if Real Time System Cannot Tolerate the TSic Interrupting the µController

Some real time systems cannot tolerate the TSic interrupting the µController. The µController must initiate the temperature read. This can be accomplished by using another pin of the µController to supply V_{DD} to the TSic. The TSic will transmit its first temperature reading approximately 65-85 ms [1] (@RT) after power up. When the µController wants to read the temperature, it first powers the TSic using one of its port pins. It will receive a temperature transmission approximately 65 ms to 85 ms later. If during that 85 ms, a higher priority interrupt occurs, the µController can simply power down the TSic to ensure it will not cause an interrupt or be in the middle of a transmission when the high priority ISR finishes. This method of powering the TSic has the additional benefit of acting like a power down mode and reducing the quiescent current from a nominal 45 µA to zero. The TSic is a mixed signal IC and provides best performance with a clean V_{DD} supply. Powering through a µController pin does subject it to the digital noise present on the µController's power supply. Therefore it is best to use a simple RC filter when powering the TSic with a µController port pin. See the diagram below

1) This value is depending on the temperature. In lower temperatures this value can be lower too



5.8 Appendix A: An Example of PIC1 Assembly Code for Reading the ZACwire™

In the following code example, it is assumed that the ZACwire™ pin is connected to the interrupt pin (PORTB, 0) of the PIC and that the interrupt is configured for falling edge interruption.
This code should work for a PIC running between 2 MHz to12 MHz.

```
TEMP_HIGH      EQU     0X24      ;; MEMORY LOCATION RESERVED FOR TEMP HIGH BYTE
TEMP_LOW       EQU     0X25      ;; MEMORY LOCATION RESERVED FOR TEMP LOW BYTE
                                 ;; THIS BYTE MUST BE CONSECUTIVE FROM TEMP_HIGH
LAST_LOC       EQU     0X26      ;; THIS BYTE MUST BE CONSECUTIVE FROM TEMP_LOW
TSTROBE        EQU     0X26      ;; LOCATION TO STORE START BIT STROBE TIME
ORG            0X004             ;; ISR LOCATION

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

CODE TO SAVE ANY NEEDED STATE AND TO DETERMINE THE SOURCE OF THE ISR GOES HERE. ONCE YOU HAVE
DETERMINED THE SOURCE IF THE INTERRUPT WAS A ZAC WIRE TRANSMISSION THEN YOU BRANCH TO ZAC_TX

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

ZAC_TX:        MOVLW TEMP_HIGH         ;; MOVE ADDRESS OF TEMP_HIGH (0X24) TO W REG
               MOVWF FSR               ;; FSR = INDIRECT POINTER, NOW POINTING TO TEMP_HIGH
GET_TLOW:      MOVLW  0X02             ;; START TSTROBE COUNTER AT 02 TO ACCOUNT FOR
               MOVWF  TSTROBE          ;; OVERHEAD IN GETTING TO THIS POINT OF ISR
               CLRF   INDF             ;; CLEAR THE MEMORY LOCATION POINTED TO BY FS
```

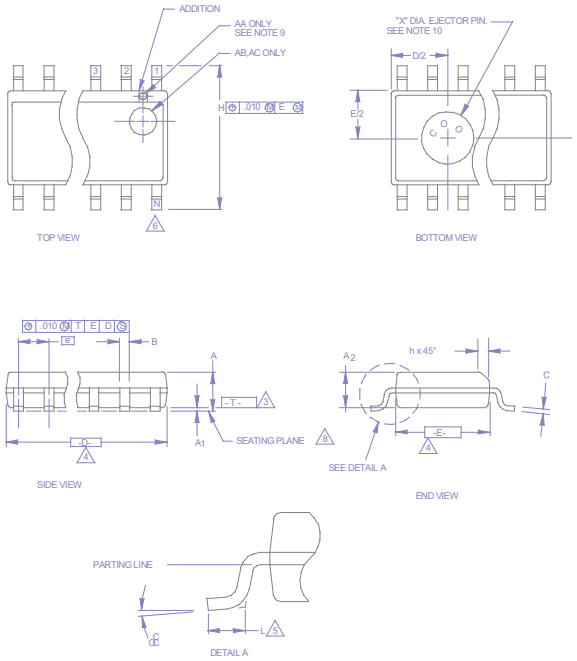
```
STRB:       INCF    TSTROBE,1       ;; INCREMENT TSTROBE
            BTFSC   STATUS,Z        ;; IF TSTROBE OVERFLOWED TO ZERO THEN
            GOTO    RTI             ;; SOMETHING WRONG AND RETURN FROM INTERRUPT
            BTFSS   PORTB,0         ;; LOOK FOR RISE ON ZAC WIRE
            GOTO    STRB            ;; IF RISE HAS NOT YET HAPPENED INCREMENT TSTROBE

            CLRF    BIT_CNT         ;; MEMORY LOCATION USED AS BIT COUNTER
BIT_LOOP:   CLRF    STRB_CNT        ;; MEMORY LOCATION USED AS STROBE COUNTER
            CLRF    TIME_OUT        ;; MEMORY LOCATION USED FOR EDGE TIME OUT
WAIT_FALL:  BTFSS   PORTB,0         ;; WAIT FOR FALL OF ZAC WIRE
            GOTO    PAUSE_STRB      ;; NEXT FALLING EDGE OCCURRED
            INCFSZ  TIME_OUT,1      ;; CHECK IF EDGE TIME OUT COUNTER OVERFLOWED
            GOTO    WAIT_FALL
            GOTO    RTI             ;; EDGE TIME OUT OCCURRED


PAUSE_STRB: INCF    STRB_CNT,1      ;; INCREMENT THE STROBE COUNTER
            MOVF    TSTROBE,0       ;; MOVE TSTROBE TO W REG
            SUBWF   STRB_CNT,0      ;; COMPARE STRB_CNT TO TSTROBE
            BTFSS   STATUS,Z        ;;  IF EQUAL THEN IT IS TIME TO STROBE
            GOTO    PAUSE_STRB      ;; ZAC WIRE FOR DATA, OTHERWISE KEEP COUNTING
                    ;; LENGTH OF THIS LOOP IS 6-STATES.  THIS HAS TO
                    ;; MATCH THE LENGTH OF THE LOOP THAT ACQUIRED TSTROBE
            BCF     STATUS,C        ;; CLEAR THE CARRY
            BTFSC   PORTB,0         ;;  SAMPLE THE ZAC WIRE INPUT
            BSF     STATUS,C        ;; IF ZAC WIRE WAS HIGH THEN SET THE CARRY
            RLF     INDF,1          ;; ROTATE CARRY=ZAC WIRE INTO LSB OF REGISTER
                                    ;; THAT FSR CURRENTLY POINTS TO
            CLRF    TIME_OUT        ;; CLEAR THE EDGE TIMEOUT COUN
WAIT_RISE:  BTFSC   PORTB,0         ;;  IF RISE HAS OCCURRED THEN WE ARE DONE
            GOTO    NEXT_BIT
            INCFSZ TIME_OUT,1       ;; INCREMENT THE EDGE TIME OUT COUNTER
            GOTO    WAIT_RISE
            GOTO    RTI             ;; EDGE TIME OUT OCCURRED.

NEXT_BIT:   INCF    BIT_CNT,1       ;; INCREMENT BIT COUNTER
            MOVLW   0X08            ;; THERE ARE 8-BITS OF DATA
            SUBWF   BIT_CNT,0       ;; TEST IF BIT COUNTER AT LIMIT
            BTFSS   STATUS,Z        ;;  IF NOT ZERO THEN GET NEXT BIT
            GOTO    BIT_LOOP

            CLRF    TIME_OUT        ;; CLEAR THE EDGE TIME OUT COUNTER
WAIT_PF:    BTFSS   PORTB,0         ;;  WAIT FOR FALL OF PARITY
            GOTO    P_RISE
            INCFSZ  TIME_OUT,1      ;; INCREMENT TIME_OUT COUNTER
            GOTO    WAIT_PF
            GOTO    RTI             ;; EDGE TIMEOUT OCCURRED

P_RISE:     CLRF    TIME_OUT        ;; CLEAR THE EDGE TIME OUT COUNTER
WAIT_PR:    BTFSC   PORTB,0         ;;  WAIT FOR RISE OF PARITY
            GOTO    NEXT_BYTE
            INCFSZ  TIME_OUT,1      ;; INCREMENT EDGE TIME OUT COUNTER
            GOTO    WAIT_PR
            GOTO    RTI             ;; EDGE TIME OUT OCCURRED
```

```
NEXT_BYTE:      INCF    FSR,1           ;; INCREMENT THE INDF POINTER
                MOVLW   LAST_LOC
                SUBWF   FSR,0           ;; COMPARE FSR TO LAST_LOC
                BTFSS   STATUS,Z        ;;  IF EQUAL THEN DONE
                GOTO    WAIT_TLOW

        ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                ;; IF HERE YOU ARE DONE READING THE ZAC WIRE AND HAVE THE DATA ;;
                ;; IN TEMP_HIGH & TEMP_LOW                                      ;;
        ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

WAIT_TLOW:      CLRF    TIME_OUT
WAIT_TLF:       BTFSS   PORTB,0         ; WAIT FOR FALL OF PORTB,0 INDICATING
                GOTO    GET_TLOW        ; START OF TEMP LOW BYTE
                INCFSZ  TIME_OUT
                GOTO    WAIT_TLF
                GOTO    RTI             ; EDGE TIMEOUT OCCURRED

RTI:            ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                ;; RESTORE ANY STATE SAVED OFF AT BEGINNING OF ISR ;;
                ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
                BCF     INTCON,INTF     ;; CLEAR INTERRUPT FLAG
                BSF     INTCON,INTE     ;; ENSURE INTERRUPT RE-ENABLED
                RETFIE                  ;; RETURN FROM INTERRUPT

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
```

6. Die and Package Specifications

6.1 SOP-8

The following dimensional drawings are for the TSic Series SOP-8 (SOIC Narrow, 0.150) package. See Table 1.1 and Table 1.2 on the next page for the dimensions labeled in these diagrams. Unless specified otherwise, dimensions are in inches.



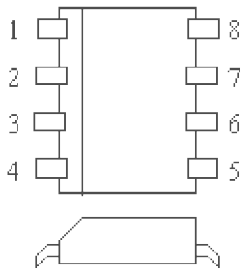
Notes:

1. Maximum thickness allowed is 0.015
2. Dimensioning and tolerances:

Decimal	Angular	3rd Angle Projection
.xx ±0.01"	±1 °C	
.xxx ±0.002"		
.xxxx ±0.0010"		

3. "T" is a reference datum
4. "D" & "E" are reference datums and do not include mold flash or protrusions but do include mold mismatch and are measured at the mold parting line. Mold flash and protrusions do not exceed 0.006 inches at the end and 0.01 " at the window
5. "L" is the length of the terminal for soldering to a substrate
6. "N" is the number of terminal positions
7. Terminal positions are shown for reference only
8. Formed leads are planar with respect to one another within 0.03 " at the seating plane
9. The appearance of the pin 1 marker is optionally either the round type or the rectangular type
10. Country of origin location on package bottom is optional and depends on assembly location
11. Controlling dimension: Inches
12. This part is compliant with JEDEC Standard MS-012, Variation AA, AB & AC

6.1.1 SOP-8 Pin Assignment



Pin	Name	Description
1	V^+	Supply voltage (3 V to 5.5 V)
2	Signal	Temperature output signal
4	Gnd	Ground
3,5-8	TP/NC	Test pin / NC Do not connect

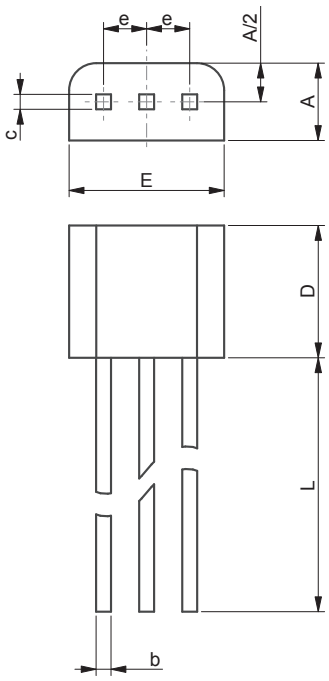
6.1.2 Inches

	Common Dimensions			Note	Note	3			S
					Variations	D			N
	MIN	NOM	MAX			MIN	NOM	MAX	
A	0.061	0.064	0.068		AA	0.189	0.194	0.196	8
A1	0.004	0.006	0.0098		AB	0.337	0.342	0.344	14
A2	0.055	0.058	0.061		AC	0.386	0.391	0.393	16
B	0.0138	0.016	0.0192						
C	0.0075	0.008	0.0098						
D		See variations		3					
E	0.15	0.155	0.0157						
e		0.050 BSC							
H	0.23	0.236	0.244						
h	0.01	0.013	0.016						
L	0.016	0.25	0.035						
N		See variations		5					
	0 °	5 °	8 °						
X	0.085	0.093	0.1						

6.1.3 Millimeters

	Common Dimensions			Note	Note	3			S
					Variations	D			N
	MIN	NOM	MAX			MIN	NOM	MAX	
A	1.55	1.63	1.73		AA	4.8	4.93	4.98	8
A1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A2	1.4	1.47	1.55		AC	9.8	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.2	0.25						
D		See variations		3					
E	3.81	3.94	3.99						
e		1.27 BSC							
H	5.84	5.99	6.2						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N		See variations		5					
	0 °	5 °	8 °						
X	2.16	2.36	2.54						

6.2 TO92

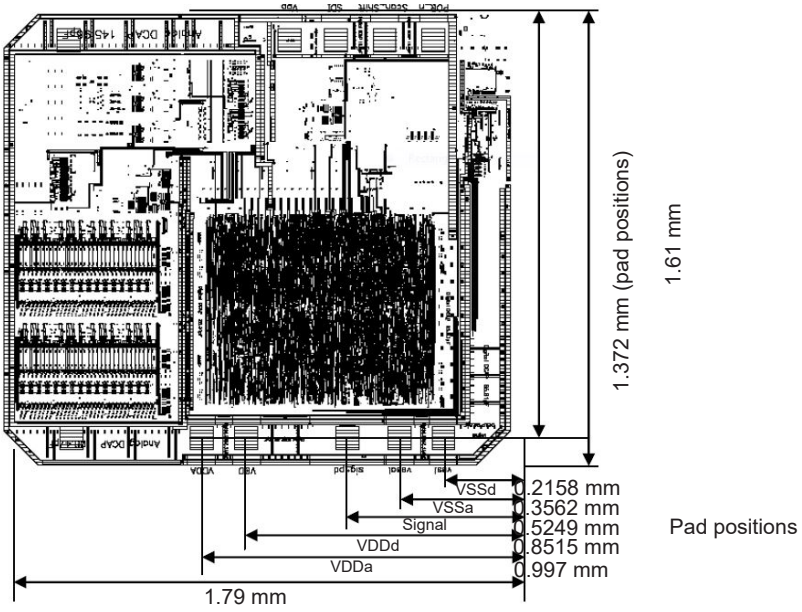


	Millimeters		Inches	
Dimensions	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
b	0.41	0.495	0.016	0.0195
c	0.41	0.495	0.016	0.0195
D	3.61	4.01	0.14	0.16
E	4.37	4.77	0.172	0.188
e	NOM. 1.27		NOM. 0.05	
L	13	13.97	0.512	0.550

6.2.1 TO92 Pin Assignment

Pin	Name	Description
3	V+ (V_{DD})	Supply Voltage (3 V to 5.5 V)
2	Signal	Temperature Output Signal
1	Gnd (V_{SS})	Ground

6.3 Bare Die



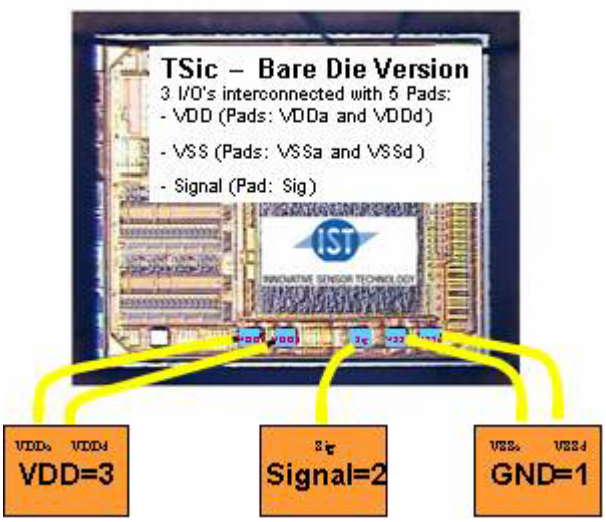
Pad positions

6.3.1 Bare Die Pin Assignment

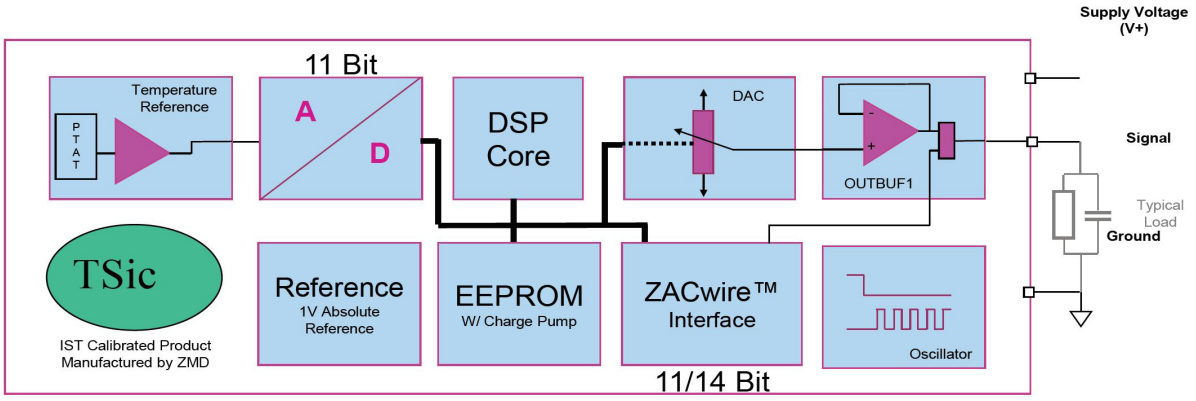
Pin	Name	Description
3	V^+ (V_{DD})	Supply Voltage (3 V to 5.5 V)
2	Signal	Temperature Output Signal
1	Gnd (V_{SS})	Ground

Die Thickness:	390 µm
Pad size:	68 µm x 68 µm

The analog and digital power and ground of the chip are wired to same substrate or Flex-Pad: V_{DDA} and V_{DD} are wired to V_{DD}, and V_{SSA} and V_{SS} are wired to Ground. The Signal pin needs only one wire.



7. TSic Block Diagram



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