APPLICATION NOTE
www.onsemi.com

onsemi EliteSiC Gen 2 1200 V SiC MOSFET M3S Series

AND90204/D

Abstract

onsemi released 2nd generation of 1200 V silicon carbide (SiC) MOSFET, named M3S, S means switching. M3S−series is focused on improvement in switching performance than 1st generation of 1200 V SiC MOSFET, in addition to the reduction in specific resistance, R_{SP}, defined as $R_{DS(ON)}$*Area. M3S is optimized for providing the better performance in high power applications for industrial power system such as solar inverters, ESS, UPS and off−board electric vehicle chargers. It can help designers to increase the switching frequency with high system efficiency. This application note describes the key characteristics of M3S, how much improved compare to Gen 1 and provides useful design tips.

Introduction

SiC power devices are getting adopted fast in the Energy−infrastructure segment which includes solar, UPS, energy storage and EV charging system to improve efficiency or increase power density. Lower switching losses enable higher efficiency with less cooling efforts or higher switching frequency with reduced size and value of passive components. These benefits can justify the higher costs of SiC power devices.

onsemi had already released the first generation of 1200 V SiC MOSFET products, named SC1, and lined up from 20 mΩ to 160 mΩ as shown in Table 1. Although SC1 achieved much improved performances compared with IGBTs which is the conventional solution in 1200 V switches for industrial power systems, SC1 was targeted at general purpose, compromised parameters, not specified. Some designers would want more specified product for their own system.

onsemi Gen 2 1200 V SiC MOSFETs is divided into two core technologies, one is T−design and another is S−design. T−design is targeted at traction inverters requiring the lower Rds(on) and the better short circuit capability rather than faster switching speed. S−design is optimized on the high switching performance, so designed to have lower $Q_{G(TOT)}$ and higher di/dt and dv/dt, resulting in lower switching losses. M3S products is lined up 13/22/30/40/70 mΩ for discrete packages of TO247−3L/4L and D2PAK−7L. The benefits of silicon carbide material against silicon were described in the previous application note about Gen 1 1200 V SiC MOSFETs [1], it will be skipped in this note, in which will present the key characteristics of M3S by compared with SC1.

Table 1. 1200 V SiC MOSFETs IN DISCRETE PACKAGES (‘T’ for Industrial−grade, ‘V’ for Auto−qualified, AEC−Q101)

	TO247−3	TO247−4	D2PAK−7L
@ V_{GS} = 20 V	1200 V Gen 1 SC1 discrete products		
20 mΩ	NT(V)HL020N120SC1	NT(V)H4L020N120SC1	NT(V)BG020N120SC1
40 mΩ	NT(V)HL040N120SC1	NT(V)H4L040N120SC1	NT(V)BG040N120SC1
80 mΩ	NT(V)HL080N120SC1	NT(V)H4L080N120SC1	NT(V)BG080N120SC1
160 mΩ	NT(V)HL160N120SC1	NT(V)H4L160N120SC1	NT(V)BG160N120SC1
@ V_{GS} = 18 V	1200 V Gen 2 M3S discrete products		
13 mΩ		NTH4L013N120M3S	NTBG013N120M3S
22 mΩ	NTHL022N120M3S	NT(V)H4L022N120M3S	NT(V)BG022N120M3S
30 mΩ	NTHL030N120M3S	NT(V)H4L030N120M3S	NT(V)BG030N120M3S
40 mΩ	NTHL040N120M3S	NT(V)H4L040N120M3S	NT(V)BG040N120M3S
70 mΩ	NTHL070N120M3S	NT(V)H4L070N120M3S	NT(V)BG070N120M3S

© Semiconductor Components Industries, LLC, 2022

KEY CHARACTERISTICS OF M3S (GEN 2) AGAINST SC1 (GEN 1)

This section describes the key characteristics of Gen 2 (NTH4L022N120M3S, 1200 V / 22 mΩ, TO247−4L) compared with Gen 1 (NTH4L020N120SC1, 1200 V / 20 mΩ, TO247−4L). The evaluation was performed under the same test bench with a golden sample having median values in parameters at the same time.

$R_{DS(ON)}$, Temperature Coefficient

The on−resistance, $R_{DS(ON)}$ is a critical parameter in system's performance. The lower $R_{DS(ON)}$ returns the lower conduction loss. And its temperature coefficient is also important because devices are heated after starting the operation, so the actual conduction loss in system is referred to $R_{DS(ON)}$ at high temperature.

The MOSFET $R_{DS(ON)}$ is mainly made up of three components: channel resistance, JFET region resistance and drift region resistance. Channel resistance has a negative temperature coefficient (NTC) and others have a positive temperature coefficient (PTC). The overall temperature coefficient characteristics of $R_{DS(ON)}$ is decided and dominated by the composition of those resistances.

In Figure 1, the $R_{DS(ON)}$ of NTH4L020N120SC1 is increased by 31% at 150°C from at RT (Room Temperature around 25°C), while NTH4L022N120M3S shows 74% increase at the given conditions. This result indicates SC1 is highly dominated by channel resistance at the condition. The less increase at high temperature provides the lower conduction loss as load goes heavy in system. Regarding only the conduction loss, SC1 could be better than M3S. However, because applications operating at high switching frequency have relatively lower proportion of conduction than switching in losses, it would be not a big advantage in the applications. And the fact that it is highly dominated by channel resistance means that SC1 requires the higher positive gate bias (V_{GS}) to be turned on fully than Gen 2, which demands more efforts in drive circuitry design. Thus, M3S will be more suitable for the fast switching applications as intended.

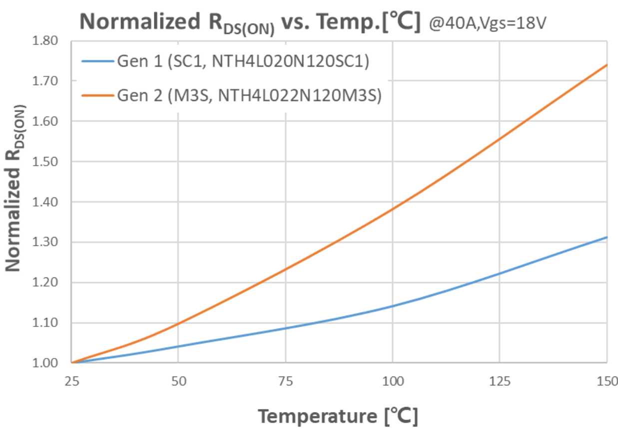


Figure 1. Normalized $R_{DS(ON)}$ vs. Temperature

$V_{GS(TH)}$, Temperature Dependency

The threshold voltage, $V_{GS(TH)}$ is the minimum gate bias that enables the formation of the channel between the source and the drain. It has a negative temperature coefficient. Basically, the design with the lower $V_{GS(TH)}$ gives the lower R_{SP} in the same technology, but there are obstacles to lower down $V_{GS(TH)}$. The lower $V_{GS(TH)}$ in operation provides bad noise immunity against unwanted parasitic turn−on by dv/dt−induced current spike through miller capacitor, and partial turn−on by di/dt−induced voltage spike across common source inductances, and oscillations resonated between parasitic inductors and capacitors. Those make the design of circuit and PCB layout difficult.

In Figure 2, M3S shows the same trend in $V_{GS(TH)}$ temperature dependency with SC1, and the slightly higher $V_{GS(TH)}$ at high temperature in actual measurement with a golden sample, though those have the same typical $V_{GS(TH)}$ as 2.72 V and 2.70 V respectively for the datasheet, which says M3S achieved the better performance in R_{SP} even with the similar level of $V_{GS(TH)}$. The 0.2 V higher $V_{GS(TH)}$ of NTH4L022N120M3S in the minimum value for the datasheet, 2.04 V vs. 1.8 V, will provide the less risky against noise.

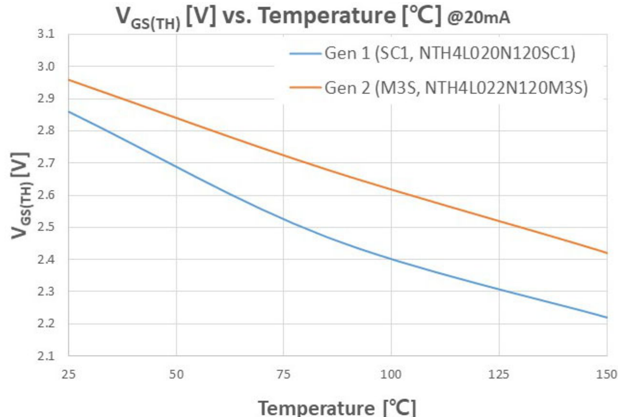


Figure 2. Threshold Voltage vs. Temperature

$V_{GS(OP)}$, Recommended Operating Gate Voltage

The recommended operating gate driving voltage is decided by considering the performance − such as $R_{DS(ON)}$, switching losses (E_{ON}, E_{OFF}), body diode's forward voltage drop (V_F) and its reverse recovery loss (E_{REC}) − and the reliability, especially about gate oxide quality issue.

Like Table 2, M3S is recommended −3 V as a negative gate bias supply voltage and 18 V as a positive gate bias, while −5 V / 20 V for SC1. The reason why SC1 needs higher voltage is less controllable to the channel than M3S. The higher $V_{GS(OP)}$ also requires the higher maximum rating in V_{GS} to have enough design margin, resulting in thicker gate oxide thickness which decreases the channel mobility and transconductance, slow down the switching speed.

This $V_{GS(OP)}$ is recommended value, not the only available value to use. It can be selected by requirements of

each system within the maximum V_{GS}. The proper $V_{GS(OP)}$ selection will be guided in the section 'How to Choose the Proper $V_{GS(OP)}$'.

Table 2. GATE−TO−SOURCE VOLTAGE FOR 1200 V SiC MOSFET

1200 V SiC MOSFET	Gen 1 (SC1)	Gen 2 (M3S)
Maximum V_{GS}	−15 V / +25 V	−10 V / +22 V
Recommended $V_{GS(OP)}$	−5 V / +20 V	−3 V / +18 V

$Q_{G(TOT)}$, Total Gate Charge

It is the amount of charge required during MOSFET turn−on or turn−off transient. The charge is current multiplied by time (Q=I*t). It means the higher $Q_{G(TOT)}$ requires the higher gate drive current within the same time or the longer time with the same gate current for the gate driving, which will demand the higher driving capability from the gate drive circuitry.

NTH4L022N120M3S has 135 nC at the given condition and 44% reduced FOM (Figure of Merit) factor in $R_{DS(ON)}*Q_{G(TOT)}$ than NTH4L020N120SC1, meaning it needs only 56% of the gate charge for switching in the same $R_{DS(ON)}$ device. Thanks to it, it can reduce down the burden of driving the gate by demanding the less capability of sinking and sourcing current from gate drivers, and also provides the ease for parallel operations.

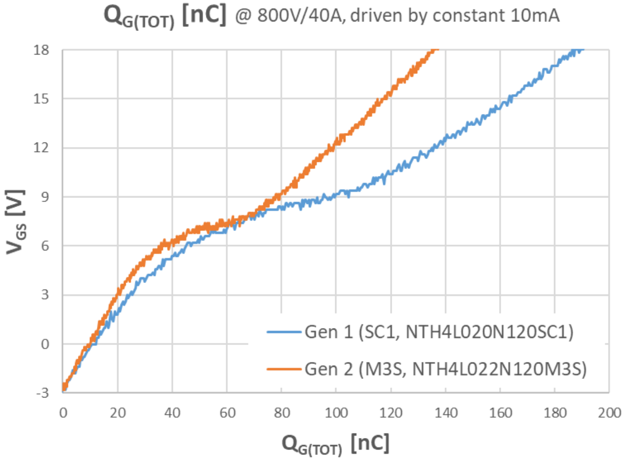


Figure 3. Total Gate Charge

E_{OSS}, Stored Energy in C_{OSS}

MOSFET have inevitable parasitic capacitances between nodes – C_{GS} between Gate and Source, C_{GD} between Gate and Drain, C_{DS} between Drain and Source. The capacitors should be charged and discharged during the transient period, which limits the voltage slope, dv/dt. The bigger output capacitance ($C_{OSS}=C_{GD}+C_{DS}$) requires the longer time and bigger energy for charging and discharging. The stored energy in C_{OSS} after charged is dissipated through MOSFET's channel or other parasitic resistance if not recycled back to other storage components when discharged again in hard switching applications. The loss of E_{OSS} is included into device's switching loss and this capacitive loss looks not so big compared with the switching loss at high current, but it looks not so small at low current like the case of light−load in system. Because the E_{OSS} is dependent on the Drain−Source Voltage, not current, it becomes a critical loss for the efficiency at light load. And the bigger E_{OSS} also makes the design difficult in soft switching applications by limiting the selection of magnetizing inductance.

Figure 4 shows that M3S has the much lower E_{OSS}. In Figure of Merit of $R_{DS(ON)}*E_{OSS}$, M3S shows 44% reduced than SC1, so it will provide the higher efficiency at the light load in the system and the ease for the transformer and inductor design.

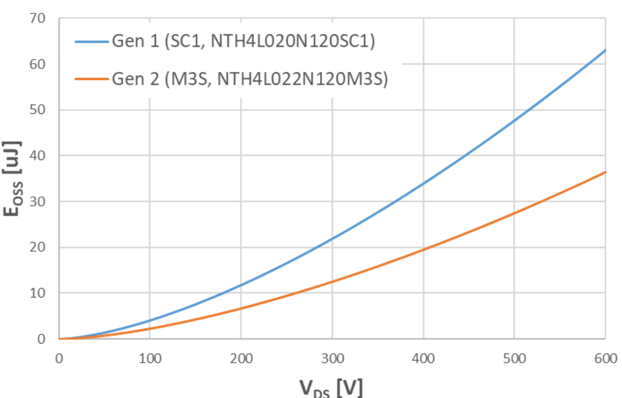


Figure 4. E_{OSS}, Stored Energy in C_{OSS}

Inductive Hard Switching Characteristics with External SiC SBD

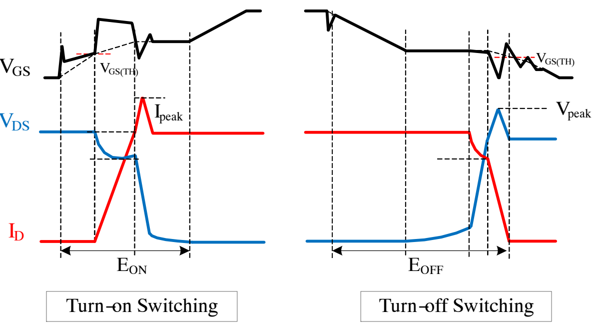
The Turn−on and off switching losses (E_{ON}, E_{OFF}) are very critical parameters in system efficiency. The applications, especially for high switching frequency topologies, require the lower switching loss to achieve the high efficiency than conduction loss. The better switching performance can make switching frequency increase, helping to reduce down the size of energy storage components such as inductors, transformers and capacitors, resulting in smaller volume of the system.

The switching losses can be measured in double−pulse testing circuit. The basic switching waveform is depicted in Figure 5 (a). The switching period for losses is defined as: from 10% of gate increase to V_{DS} = 0 V for E_{ON}, from 90% of gate decrease to I_D = 0 A for E_{OFF}. The switching conditions are that V_{DS} = 800 V, V_{GS} = −3 V / 18 V, R_G = 4.7 Ω, 25°C. The freewheeling diode is used as SiC SBD (Schottky Barrier Diode), part name is FFSH30120A which has no reverse recovery charge impacted on E_{ON}, has only capacitive loss affected to E_{ON}. The product package is TO247−4L, providing Kelvin source connection, which removes the impact of common source parasitic inductance in the gate driving loop. The gate drive IC is used with 14 A sinking and sourcing current capability, selected sufficiently

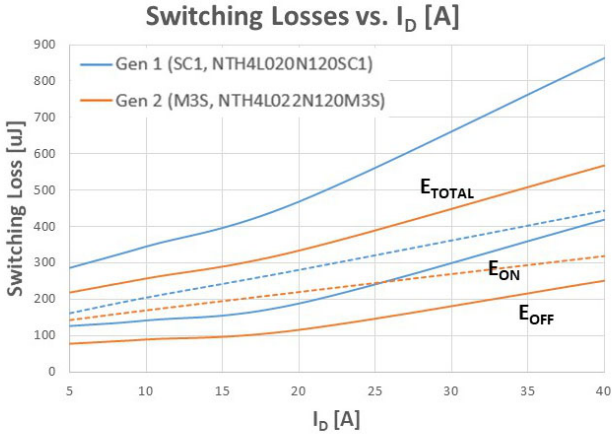
large, so the switching is not to be limited by the gate driving. The parasitic loop inductance of the double−pulse testing circuit is measured as 30 nH from DC−Link (+) to Ground.

Figure 5 (b) shows NTH4L022N120M3S achieved much improved switching performance at the given conditions, 40% lower in E_{OFF}, and 20−30% lower in E_{ON}, 34% lower in the total switching loss than NTH4L020N120SC1. In the applications with high switching frequency, it will cancel the disadvantage of the higher $R_{DS(ON)}$ temperature coefficient, explained in the section '$R_{DS(ON)}$ Temperature Coefficient'. M3S is optimized on such applications.

Because the capacitances are not independent on temperature and SiC SBD has only capacitive loss, there's no significant increase in switching losses as temperature increases, but few percent could be increased by measurement error and heated third part components like external resistors and drive ICs.



(a) Theoretical inductive switching waveform



(b) Inductive switching losses by drain current @ V_{DS} = 800 V, V_{GS} = −3 V / 18 V, R_G = 4.7 Ω, 25°C, L_σ = 30 nH

Figure 5. Inductive Switching Losses

Body Diode's Characteristics

onsemi SiC MOSFET also has an intrinsic bipolar body diode with pn junction like silicon MOSFET. The forward voltage of SiC MOSFET is relatively higher than Silicon MOSFET's because of the higher built−in voltage of pn junction by wide bandgap characteristics of the material. In general, a IGBT die has an additional standalone diode inside packages, called as co−packed or anti−parallel, because IGBT is unidirectional device unless it is RC (Reverse Conducting) IGBT technology. Thus, IGBT has more options on the selection of the co−packed diode, such as Low V_F diode, Fast recovery diode or SiC SBD. The diode whatever body or co−packed is required for reverse voltage bypass from opposite DC input connection or for ZVS in soft switching applications or as freewheeling diode in hard switching in bridge−type topologies that requires the faster reverse recovery for the better system efficiency.

Figure 6 shows the forward voltage characteristics by the drain current with the recommended negative bias of −3 V, called as third quadrant characteristics. Compared with silicon PIN diode around 1.5~3 V and SiC SBD around 1.5 V, it has relatively higher V_F of 3.8 V for NTH4L020N120SC1 and 4.5V for NTH4L022N120M3S at 40 A and 25°C. For the case that diode's conduction loss is critical, SR (Synchronous Rectifier) mode operation with a positive gate bias voltage like 18 V is required as the most effective way to reduce down the conduction loss, in which the voltage drop follow $R_{DS(ON)}$ by conducting the current reversely from Source to Drain through the channel. Otherwise it would require additional extra diode for the purpose.

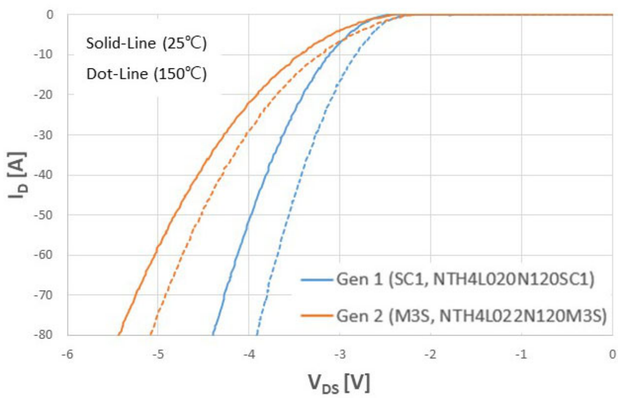


Figure 6. Body Diode Forward Voltage

Unlike the majority carrier device like the silicon carbide Schottky Barrier Diode that has no reverse recovery charge, the body diode of SiC MOSFET has the reverse recovery charge (Q_{RR}) by the minority carrier injection in the structure of PIN diode, the injected minority carrier into lightly doped drift region requires the time to remove them, called as reverse recovery time (t_{RR}). During the removal of the charge, the diode dissipates the loss, called as the reverse recovery loss (E_{REC}). And it increases as temperature increases due to the more injected minority carriers and the longer recombination lifetime. Figure 7 shows that NTH4L022N120M3S has much faster recovery time and lower recovery charge than NTH4L020N120SC1, around 40~50% improved. Therefore, M3S will provide the better performance in the bridge topologies in which body diode

should commutate with active switch, by the superior reverse recovery characteristics even with the higher V_F, especially for high frequency applications.

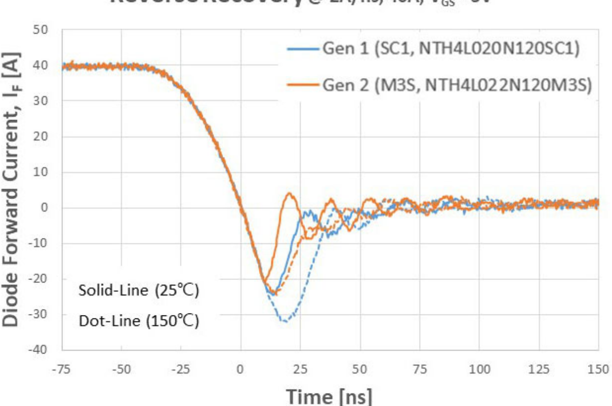


Figure 7. Reverse Recovery of the Body Diode

Turn−on Switching Performance with Self Body Diode, $E_{ON(BD)}$

In the bridge topologies, the body−diode is commutated with the active switch. During the reverse recovery time, the bridge goes into short circuited and causing shoot−through current, I_{peak} like in Figure 5 (b), which makes E_{ON} larger. The higher Q_{RR} and longer t_{RR} cause the higher I_{peak}, resulting in the higher E_{ON} in the bridge topology.

Figure 8 is the result of turn−on switching loss ($E_{ON(BD)}$) with self body diode at the given conditions under the same double−pulse test bench. NTH4L022N120M3S has the lower $E_{ON(BD)}$ by 45% than NTH4L020N120SC1. And this is the value increased by 30% than with SiC SBD, which means the impact of Q_{RR} on E_{ON} loss.

From those results of V_F, Q_{RR} and $E_{ON(BD)}$, it could say that M3S's body diode is designed for targeting at high−frequency applications and provides more advantages as switching frequency increases.

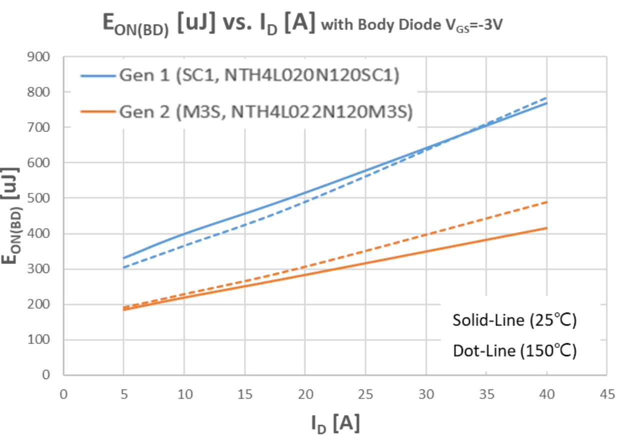


Figure 8. Turn−on Switching Loss with Body Diode @ V_{DD} = 800 V, V_{GS} = −3 / 18 V, R_G = 4.7, L_σ = 30 nH

DESIGN CONSIDERATIONS AND TIPS WITH GEN 2 1200 V M3S PRODUCTS

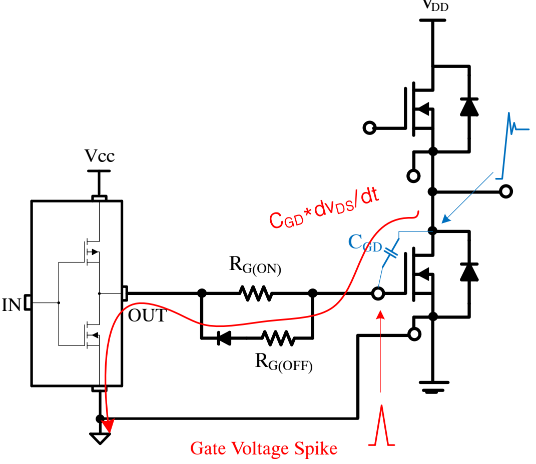
Parasitic Turn−on Concern

As described in section '$V_{GS(TH)}$, Temperature Dependency', because the threshold voltage of NTH4L022N120M3S (Gen 2) has NTC, it has the lowest value at the maximum junction temperature of $T_{J(MAX)}$ = 175°C. Even the typical $V_{GS(TH)}$ is 2.72 V in the datasheet, it could reach down to 1.5 V at the worst case of considering process variation of 25% for corner sample and the temperature coefficient. It means it can be turned on by noises over 1.5 V. It is potentially dangerous and demands the effort to suppress the noises, and it makes the design difficult and complicated.

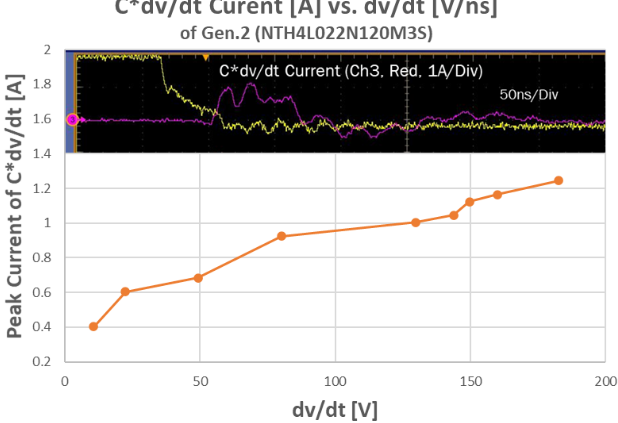
Even with the successful suppression, it can be turned on by so−called parasitic turn−on effect due to miller capacitor in bridge application [2] as depicted in Figure 9 (a). When the upper switch is turned on, it makes a voltage change dV_{CE}/dt across the lower switch. The current flows through the parasitic Miller capacitor, C_{GD}, and external resistors into Ground. This current can be expressed as $C_{GD}*dV_{CE}/dt$ approximately, which creates the voltage drop across the resistors in the path. If the voltage exceeds the threshold voltage, a parasitic turn−on occurs even after turned off.

The waveform in red of Figure 9 (b) shows the current measured through the path. The peak value of the current is directly proportional to the dv/dt and causes peak voltage across resistors. It means this current will limit the selection of the external gate resistances ($R_{G(ON)}$ and $R_{G(OFF)}$). Figure 9 (c) is the value of the peak voltage spike, calculated by the current multiplied by total external $R_{G(EXT)}$ in the path. The higher $R_{G(EXT)}$ causes the higher voltage spike, so exposed on the risk of the unwanted turn−on. If the $V_{GS(TH)}$ is 2.72 V and no use of negative bias, then $R_{G(EXT)}$ = 4.7 Ω will be limited to use by the high possibility of parasitic turn on, while $R_{G(EXT)}$ = 2 Ω will be no problem in all dv/dt range to avoid the case of exceeding the $V_{GS(TH)}$. In actual, $R_{G(EXT)}$ increase can reduce down the dv/dt, but it should be counted on how much decrease in dv/dt and how much increase in voltage peak by the $R_{G(EXT)}$ increase, so this will always give the difficulty to select proper resistors in bridge applications.

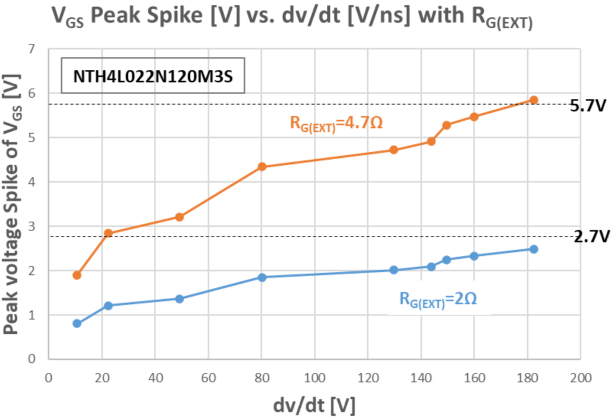
There are four mitigation solutions suggested in [2]. The first is to separate gate resistor for turn−on and turn−off to vary resistors, the second is to add capacitor between gate and source to shunt the Miller current, the third is to use a negative gate bias voltage to increase threshold voltage, the last is to use additional transistor for active miller clamping. The most effective and simple way to avoid this issue is to use negative supply voltage. In the Figure 9 (c), if −3 V is applied, the actual threshold voltage becomes 5.72 V, so it can be more flexible to select the gate resistors.



(a) Parasitic turn−on mechanism



(b) Measured miller current vs. dv/dt



(c) Peak voltage of V_{GS} spike vs. dv/dt

Figure 9. Parasitic Turn−on Phenomenon

How to Choose the Proper $V_{GS(OP)}$

Unlike silicon MOSFET which uses 10 V commonly as gate driving voltage and IGBT that commonly by 15 V, SiC MOSFETs are recommended by different $V_{GS(OP)}$ conditions by makers or by each product. It may mean the technology is not mature yet and still have many challenges to overcome such as defects at SiC/SiO2 interface, poor channel mobility, gate oxide quality and $V_{GS(TH)}$ stability issue.

As positive gate bias increases, on−resistance ($R_{DS(ON)}$) decreases and turn−on switching loss (E_{ON}) with external SiC SBD decreases, but no big change in turn−off switching loss (E_{OFF}) as shown in Figure 10 (a) and (b). But it could require more effort on gate driving circuit design and it causes the higher gate driving loss. The increased voltage and inevitable voltage spike will be more stressful on gate oxide. It is well known that the higher positive bias stress can result in more drift in $V_{GS(TH)}$, which will cause the degradation in electrical performances such as $R_{DS(ON)}$ and E_{ON}/E_{OFF}.

As negative gate bias increases to negative, the turn−off switching loss (E_{OFF}) decreases, while no change in the turn−on switching loss (E_{ON}) as shown in Figure 10 (c). In body diode's performance, the forward voltage (V_F) increases like in Figure 10 (d), which is due to the unstable channel closing at $V_{GS} = 0$ V and channel current reduction when the negative bias is increased. The reverse recovery characteristics becomes poorer a little, but not critical. In the same way, it also makes more stress on gate oxide, so it could cause more drift in $V_{GS(TH)}$ and also high supply voltage could lay a burden on gate drive circuitry design.

Based on those trends, it's recommended −3 / 18 V for Gen 2 1200 V M3S products generally, as explained in the section '$V_{GS(OP)}$, Recommended Operating Gate Voltage', which is suggested by considering optimization between performance and reliability. But it can be chosen different voltages for optimizing on each application and its operating condition. For examples, 0 V driving will be good choice if designer want the lower V_F of body diode and can accept E_{OFF} increase. 15 V driving will be good option if it can't meet EMI regulation and have enough margin in efficiency and thermal performance for the system to be sacrificed.

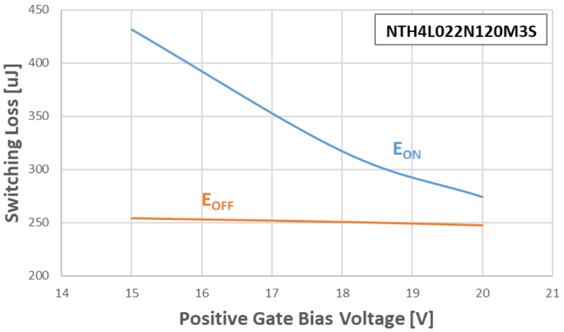
$R_{DS(ON)}$ [mΩ] vs. V_{GS} [V] @ 40A, 25°C

NTH4L022N120M3S

(a) $R_{DS(ON)}$ according to positive gate bias

Switching Loss by Positive Gate Bias Voltage

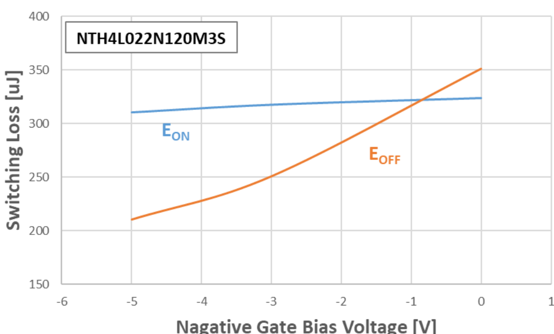
@ 800V/40A, R_G=4.7Ω, Lσ=30nH, w/SiC-SBD, w/-3V



(b) Switching Losses according to positive gate bias

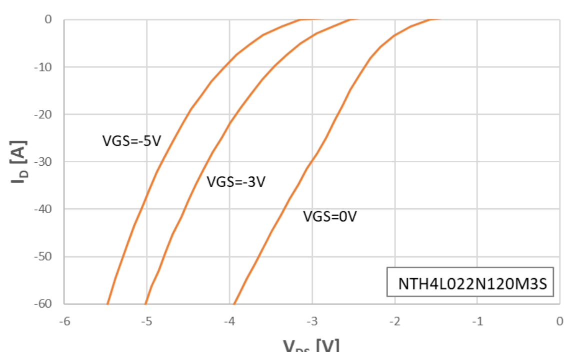
Switching Loss by Nagative Gate Bias Voltage

@ 800V/40A, R_G=4.7Ω, Lσ=30nH, w/SiC-SBD, w/18V



(c) Switching Losses according to negative gate bias

Body Diode Forward Votage [V] by V_{GS} @25°C



(d) Forward voltage according to negative gate bias

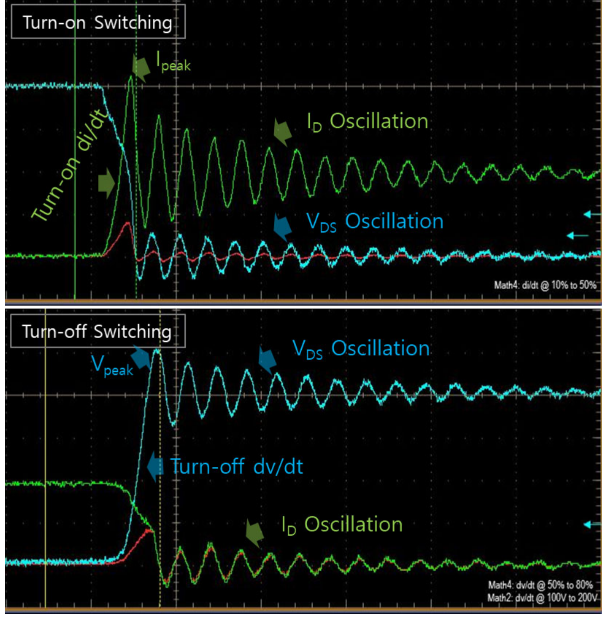
Figure 10. Performances According to V_{GS}

To Optimize Proper $R_{G(EXT)}$ Considering EMI (Electromagnetic Interference)

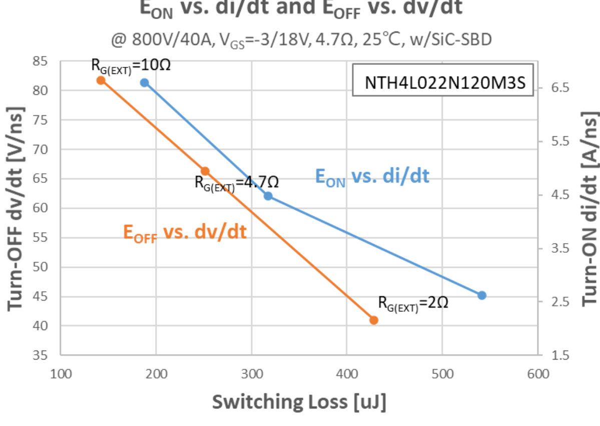
In switching performance, the smaller $R_{G(EXT)}$ returns the lower switching losses. But the strong drive to the gate causes the higher di/dt and dv/dt during the transition and which causes the sharp spikes in voltage and current by the parasitic inductances and capacitances in the board and packages, and also high frequency L/C resonated oscillations between them. The designer should find out the proper $R_{G(EXT)}$ which provides the best performance with the regulations for EMI satisfied.

Figure 11(a) describes the key sources of EMI disturbance in general switching waveforms. All those EMI sources are related to the di/dt and dv/dt. The high di/dt causes voltage spike across parasitic inductances by L*di/dt and the high dv/dt causes current spike in parasitic capacitances by C*di/dt. And both can trigger L/C resonated oscillation over tens or hundreds of MHz that directly impacts on EMI result.

Figure 11(b) says E_{ON} is dominated by turn−on di/dt under the same reverse recovery conditions and E_{OFF} is dominated by turn−off dv/dt. They are definitely in trade−off relationship between switching performance and EMI. If $V_{GS(OP)}$ is fixed, it can be controlled by $R_{G(EXT)}$, so need to optimize the $R_{G(EXT)}$. For example, if the PCB layout is not good, having high parasitic components, so can't pass the EMI regulation under the given di/dt and dv/dt in the try, and also if no chance to modify the PCB layout anymore to minimize parasitic components, it should decrease di/dt and dv/dt by increasing $R_{G(EXT)}$. then it will pass the EMI regulation, but pay system efficiency loss as a fee.



(a) EMI sources in switching



(b) di/dt and dv/dt by $R_{G(EXT)}$

Figure 11. EMI Consideration

CONCLUSION

This application note presented the key characteristics of **onsemi** 2nd generation 1200 V M3S SiC MOSFETs by compared with Gen 1 (SC1). Through section 'Key Characteristics of M3S (Gen 2) against SC1 (Gen 1)', it showed M3S has achieved the great improvement, that summarized in Table 3. Figure 12 shows the actual performance on the system, the efficiency measured on 5 kW Boost converter with 40 kHz switching frequency. The result definitely shows the better performance of M3S than SC1, especially at the light−load, in which range the switching performance dominate, so says Gen 2 (M3S) is the more suitable product for high switching frequency applications. Lastly it provided useful design tips to use M3S efficiently in section 'Design Considerations and Tips with Gen 2 1200 V M3S Products'.

Table 3. KEY PERFORMANCE COMPARISON SUMMARY TABLE, all measured under the same test bench at the conditions with one golden typical sample (V_{GS} = −3 / 18 V, $R_{G(EXT)}$ = 4.7 Ω, V_{DS} = 800 V, I_D = 40 A, L_{σ} = 30 nH, 14 A sinking/sourcing driver, 25°C, di/dt_{RR} = 2 A/ns)

	NTH4L020N120SC1	NTH4L022N120M3S
Gen.	1200 V Gen.1	1200 V Gen.2 S−design
$R_{DS(ON)}$	22 mΩ	22 mΩ
$Q_{G(TOT)}$	135 nC	191 nC
E_{OSS}	98 μJ	57 μJ
E_{OFF}	420 μJ	251 μJ
E_{ON}	444 μJ	317 μJ
$E_{ON(BD)}$	769 μJ	415 μJ
V_F	3.8 V	4.5 V
Q_{RR}	347 nC	188 nC

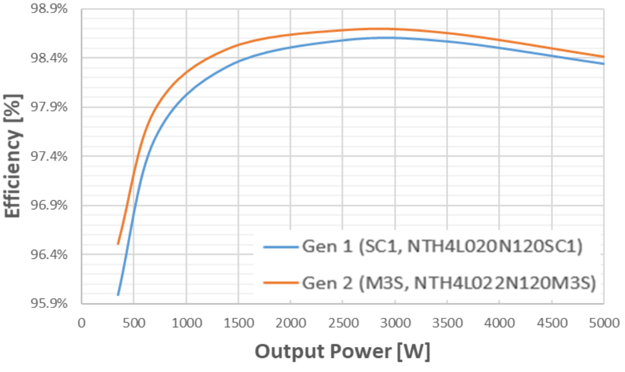


Figure 12. Measured Efficiency on 5 kW Boost Converter

References

[1] **onsemi** application note, AND90103/D, "ON Semiconductor Gen 1 1200V SiC MOSFETs & Modules: Characteristics and Driving Recommendations"

[2] Avago Technologies' white paper, "Mitigation methods for parasitic turn−on effect due to miller capacitor"

onsemi, onsemi, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊