



Meeting Challenging Efficiency Standards with Bridgeless Totem Pole Power Factor Correction

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The input bridge rectifier found in almost all AC–DC power supplies contributes losses that present a challenge in achieving the highest possible efficiency figures. However, removing the traditional diode bridge, PFC FET and boost diode in favor of a bridgeless totem pole PFC arrangement enhances efficiency through the use of active switches. The control of the new topology is more complex, often necessitating a microcontroller and associated code which presents a barrier to adoption for design teams where time is limited. The NCP1680 mixed signal PFC controller from **onsemi** is discussed in the article as it provides a code–less solution for totem–pole PFC.

Much of the world’s electrical energy is supplied to the AC–DC power supplies that are found in almost all mains–powered equipment and devices meaning that their efficiency has a huge impact on the operating costs, as well as contributing significantly to emissions.

While efficiency is a relatively simple concept – the ratio of useful output power to input power – the input power can be significantly affected by the input power factor which increases as the line current and line voltage move out–of–phase. The product of input power and power factor is the apparent power and, using this to calculate true efficiency, can result in a significant reduction in overall efficiency figures. Disturbances and inefficiencies so created can propagate back through the utility network.

However, using power factor correction (PFC) techniques, the situation can be addressed. The concept is sufficiently important that it is now a regulatory requirement. From a technical perspective, to improve power factor, EMC standards such as IEC 61000–3–2 limit the power in line harmonics that exist as a result of distorted line current.

Also, in the past, efficiency was mainly considered at its peak value, which masked poor performance, especially when system operated at low power levels. To address this, new schemes such as the 80+ certification program requires 80% efficiency at 20%, 50% and 100% of full load. The most stringent version of the 80+ standard is the ‘80+ Titanium standard’, which specifies at least 90% efficiency at 10% load and 94% efficiency at full load.

Meeting the Requirements of the ‘80+ Titanium Standard’

Most commonly, PFC uses a boost converter to derive a DC level higher than the mains voltage peak from rectified mains. This DC level, typically 395 V for a power supply designed for 90 to 264 VAC input, is then regulated using an isolated DC–DC conversion stage to produce

the required DC output voltage for the PSU. A valuable by-product of this is that the line current follows the line voltage waveform giving (in theory at least), unity power factor.

The approach above is effective and PFC can be designed to operate in continuous, discontinuous or critical conduction modes (CCM, DCM, CrM), which are largely defined by whether energy in the boost inductor fully exhausted during each cycle – or not. Normally, there is 2% loss within the DC-DC stage and 1% in the line rectification and PFC stage, although this is much closer to 2% during operation at low line. With close to 4% losses at low line, there is a significant challenge in meeting the strictest 80+ Titanium standard level that requires up to 96% efficiency at 230VAC input at 50% load – a specification commonly used in servers.

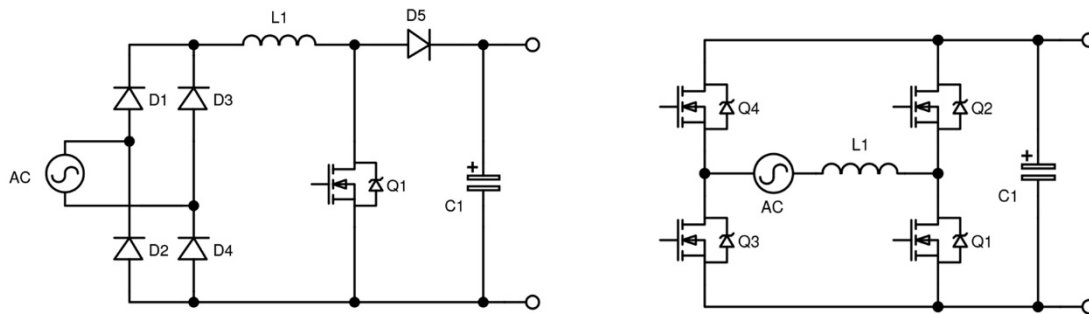


Figure 1. Typical PFC Circuits: Conventional boost (left) and Bridgeless Totem Pole (right)

To address this, a more efficient technique, known as bridgeless ‘Totem Pole PFC’ (TPPFC) has been garnering interests. In this method, active switches replace the AC line bridge rectifier diodes and adsorb the roles performed by the boost transistor and boost diode in conventional boost PFC. In this new topology, Q1 and Q2 in the fast leg of the totem pole, exchange roles, depending on mains polarity. In this configuration, just a pair of line rectifier diodes are used. Often, these are not diodes but synchronous rectifiers as shown (Q3 and Q4), further improving efficiency.

With lossless switches, a perfect inductor and no diode volt drops, TPPFC circuit efficiency becomes very close to 100%. However, in the real world MOSFETs exhibit conduction and switching losses. Although ultra-low on-resistance devices can be used – even in parallel – to minimize conduction losses, the result is generally an increase in high-frequency switching losses. As with almost all designs, there is a trade-off to be made.

Much of the switching / dynamic losses are due to the reverse recovery of the MOSFET that operates as the boost synchronous rectifier. The losses occur when the integral body diode conducts in the switching ‘dead’ time, as well as from the charging and discharging of the switch output capacitance that occurs every cycle – and therefore increases in proportion to frequency. As a result, silicon MOSFETs, even ‘Superjunction’ types are unsuitable for use in bridgeless totem pole PFC when operating in CCM. Consequently, wide bandgap (WBG) devices like

silicon carbide (SiC) and gallium nitride (GaN) are now the switch technology to use by default for this topology.

CCM is the better approach for higher power as the peak switch and inductor currents can be configured to be small, thereby reducing RMS values which keeps conduction and inductor core losses low. However, CCM is a ‘hard’ switching mode, so reverse recovery and output capacitance combine to cause relatively high dynamic losses.

During low power operation, DCM exhibits low turn-on losses, as the boost diode current is approximately zero, so there is negligible charge to recover. However, peak and RMS currents can be very significant causing high ohmic and core losses, making DCM unsuitable for high power operation.

CrM – A Balanced Approach

As neither CCM or DCM present an ideal solution, many designers use critical conduction mode (CrM) which is suitable for up to a few hundred watts (or more in an interleaved arrangement). CrM manages the switching frequency to operate on the border between DCM and CCM in response to changes in line voltage or load current. This benefits from low turn-on losses and, as the peak current is limited to double the average current, the core and conduction losses remain acceptable.

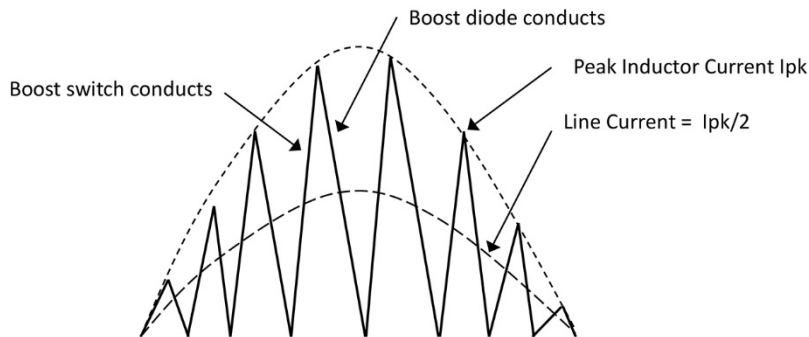


Figure 2. PFC Boost Inductor Current Waveform, Critical Conduction Mode

CrM is a hard-switching topology which means that any forward recovery of the boost diode causes an output voltage overshoot as well as in incurring some losses. Also, at light load, CrM runs at very high frequencies which degrades the efficiency through increased switching losses. The relationship is defined by:

$$f_{SW}(t) = \frac{V_{in,rms}^2}{2 \cdot L \cdot P_{in,avg}} \cdot \left(1 - \frac{v_{in}(t)}{V_{out}} \right) \quad (\text{eq. 1})$$

Looking at the equation, one would presume a simple inverse relationship between the switching frequency and input power, so a load shift from 20% to 100% (a five-fold change) should produce a similar five-fold change in frequency if efficiency remains constant. In

practice, higher frequency reduces the efficiency, so the factors interact. The relationship between frequency and line voltage is somewhat more complex, giving more than a 2:1 frequency over the line voltage span – and peaking at mid-voltage.

Addressing Light Load Losses by Restricting Frequency Range

At light load, the losses can represent a 10% drop in efficiency, which makes meeting modern efficiency standards such as 80+ very challenging. However, if designers incorporate a frequency clamp or ‘fold-back’ arrangement, the circuit is forced into DCM operation which improves light load efficiency.

Generally, silicon MOSFETs are used for the synchronous rectification of the AC line and Wide Bandgap (WBG) switches are incorporated into the totem pole’s high frequency ‘leg’. While the solution works well, control can be a challenge as there are four active devices to be driven as well as the need to detect zero current in the PFC inductor and regulating the output voltage.

Adding to this is the need for circuit protection including overcurrent and output overvoltage. A common approach is to utilize a microcontroller (MCU) where the complex algorithms can be implemented and executed through interfacing to the switches and in-circuit sensors. However, this is not a low-cost solution and it requires coding which can be challenging and time-consuming for some power supply designers.

An Integrated Solution for Totem-Pole PFC

onsemi offer an integrated and coding-free solution in their NCP1680 which is the industry’s first mixed-signal controller dedicated to CrM TTPFC. The SOIC-16 packaged device includes a novel low-loss, simple resistive current sensing arrangement and tried-and-tested PFC control algorithms, thereby delivering a low-risk and high-performance solution that is also cost-effective. The NCP1680 features constant on-time CrM and ‘valley switching’ during frequency foldback at light loads to enhance efficiency by switching at a voltage minimum. The digital voltage control loop is compensated internally to simplify system design while optimizing performance throughout the load range. Current limiting operates on a cycle-by-cycle basis for protection and no expensive Hall-effect sensor is required. Figure 3 shows a simplified TTPFC stage based upon the innovative NCP1680.

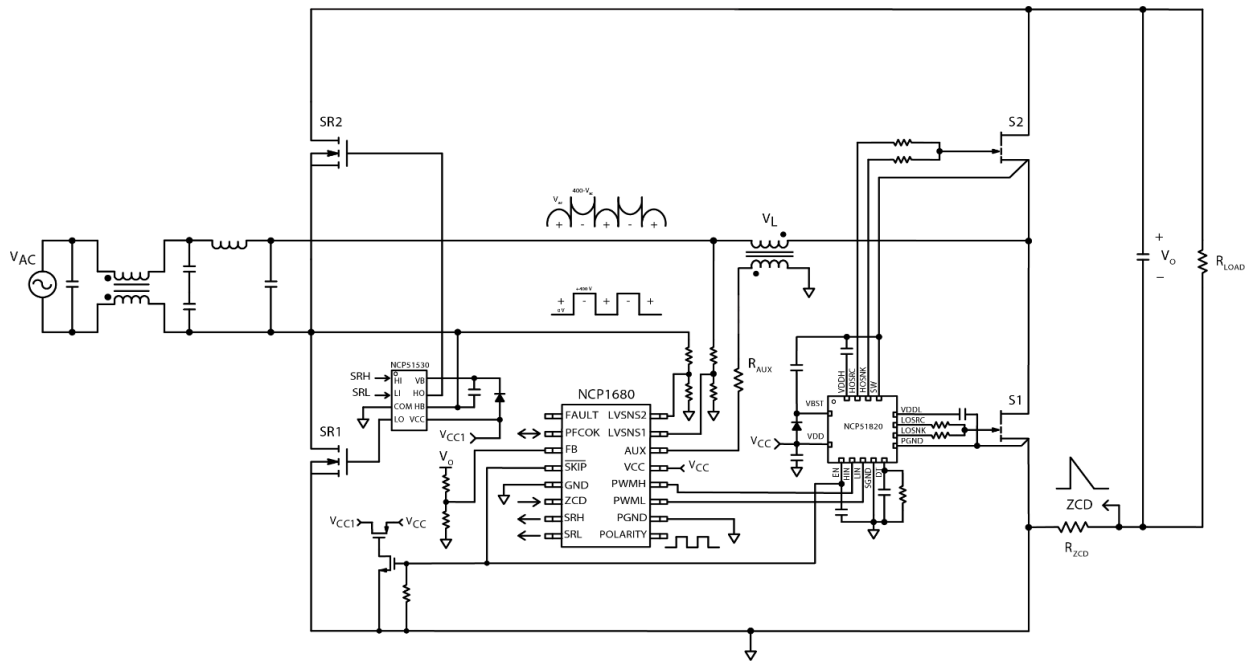


Figure 3. Simplified Typical TPPFC Application Diagram using NCP1680

To simplify design even further, **onsemi** has developed an evaluation board for the NCP1680 based with the fast leg's switches based upon GaN HEMT and Si-MOSFETs performing slow leg's AC line synchronous rectification.

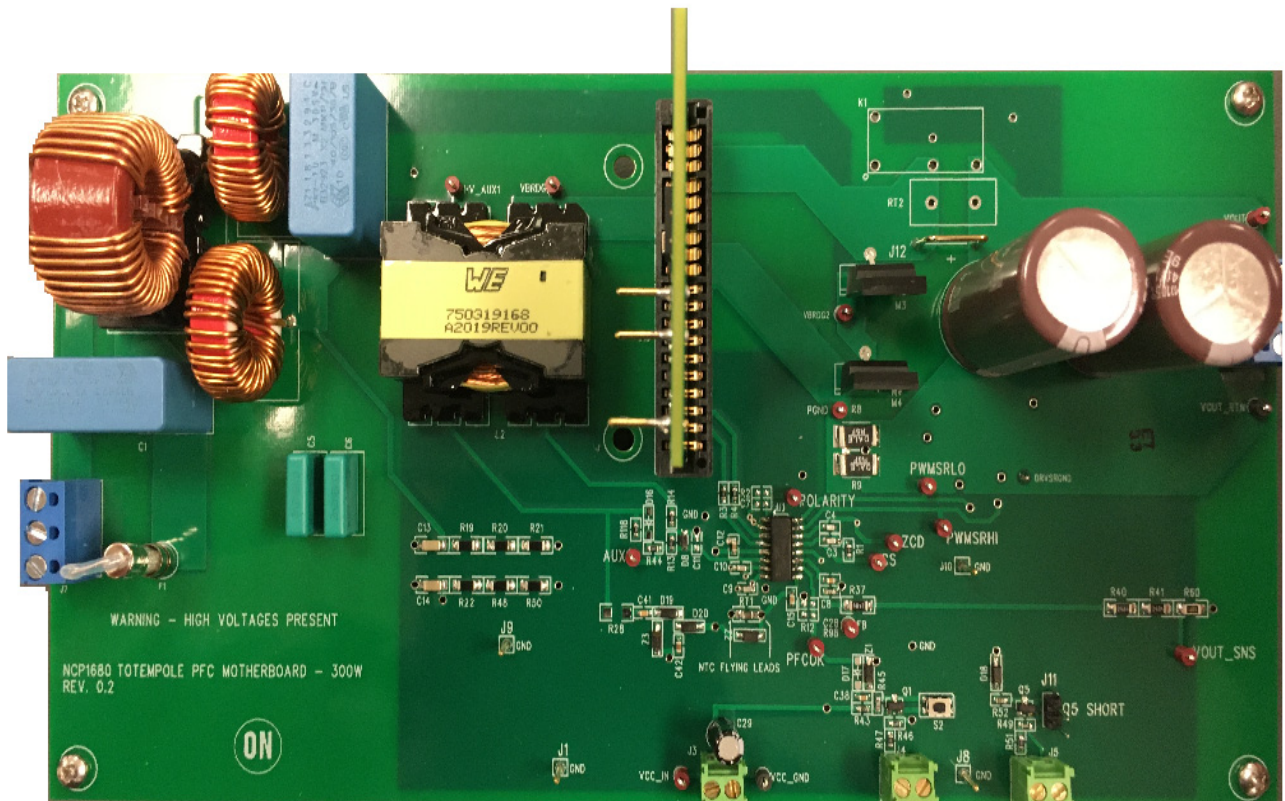


Figure 4. onsemi NCP1680 Evaluation Board

The evaluation board delivers up to 300 W of power at 395 VDC PFC output voltage from a universal input (90–265 VAC line) efficiency at full load peaking around 99% and an efficiency figure of 98% across the line range, at loads as low as 20% (Figure 5).

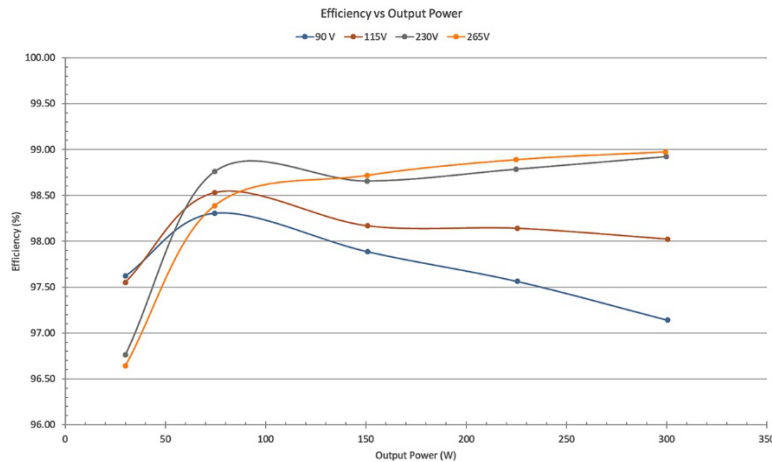


Figure 5. Efficiency Plots of the onsemi NCP1680 Evaluation Board

As WBG semiconductors and a cost-effective mixed signal, CrM controller are available from **onsemi** along with design support tools, the TPPFC approach is a preferred solution for high efficiency PFC to several hundred watts while ensuring compliance with the 80+ Titanium efficiency standard and other environmentally-based requirements for standby power consumption and no-load losses.

Higher efficiency is a requirement in every application so the improvements that can be garnered from CrM-based active PFC bring benefits (including reduced operating costs) to users. Technology from **onsemi**, including WBG semiconductors, advanced PFC controllers and design support tools dramatically simplify the task of designing for higher efficiency, ensuring these solutions can be brought to market more quickly.

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