TLE986x/TLE987x Bridge Driver Application Note

About this document

Scope and purpose

The TLE986x/TLE987x Bridge Driver Application Note gives information about the TLE986x/TLE987x Bridge Driver beyond the contents of the user manual and the datasheet. It covers dependencies between the involved modules and explains effects which occur at application level by exemplary simulation and measurement results.

Intended audience

All TLE986x/TLE987x Bridge Driver users.

Note: This information is provided to help implement our devices only. It should not be construed as a warranty of a certain functionality, condition or quality of the device.

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1 Introduction and Overview

Infineon has combined its wealth of experience in motor control drivers for automotive applications with all the benefits of an industry-standard core. The unique result, our 3rd Generation Embedded Power IC based on ARM® Cortex®-M cores, addresses a wide range of smart 3-phase brushless DC motor control applications like, fuel pumps, HVAC fans, engine cooling fans, electrical water pumps.

The TLE987x family offers scalability in terms of flash memory sizes and MCU system clock frequency supporting a wide range of motor control algorithms, either sensor-based or sensor-less. It uses the same MCU and peripherals as the TLE986x family, 2-phase driver, enabling design synergies between DC and BLDC motor control applications.

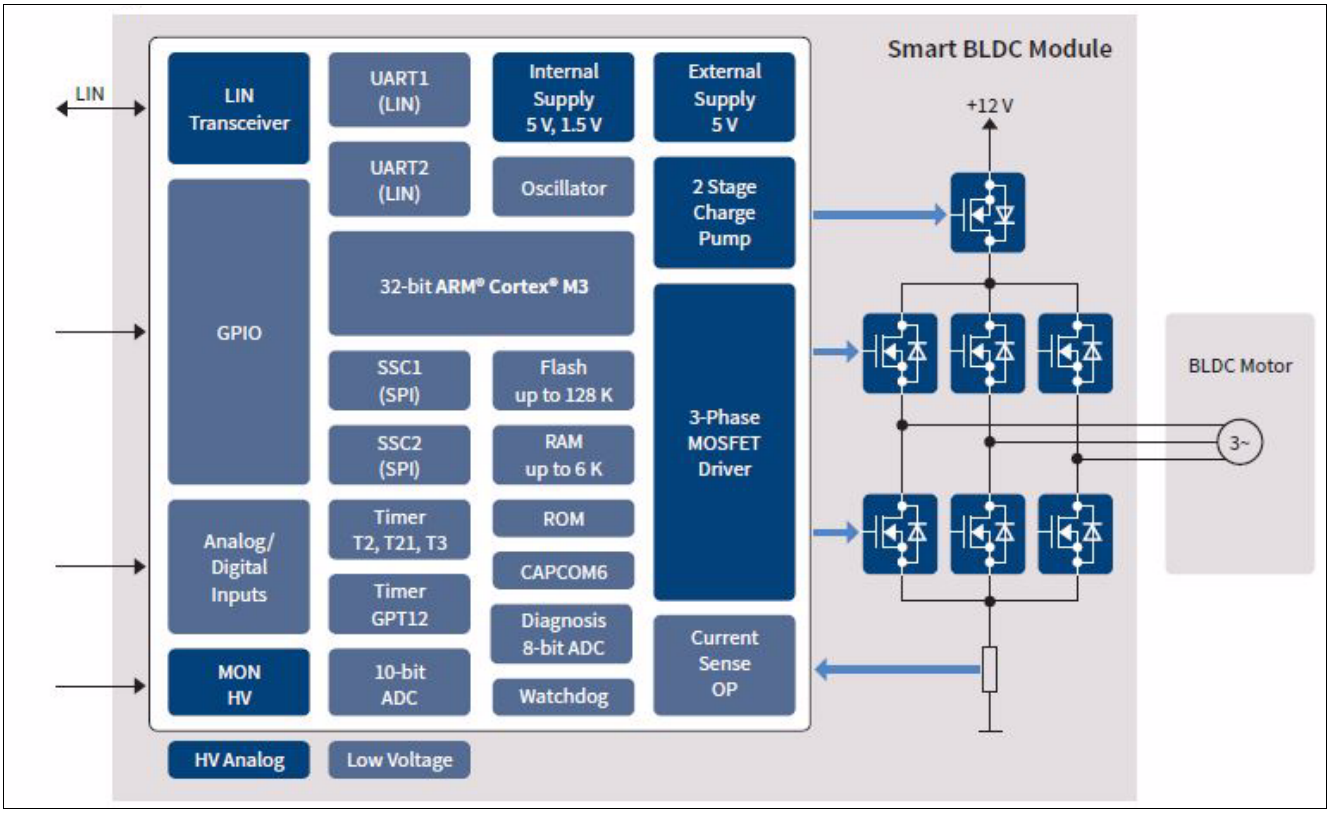

Figure 1 TLE987x Block Diagram

The topics covered in this application note are shown in **Figure 2**.

The bridge driver contains several submodules and interacts with different modules of the chip. Starting with the power supply of the bridge driver, **Chapter 2** explains the functionality of the charge pump. The most important module outside the bridge driver is the capture compare unit (CCU6). The interaction and PWM generation is explained in **Chapter 3**.

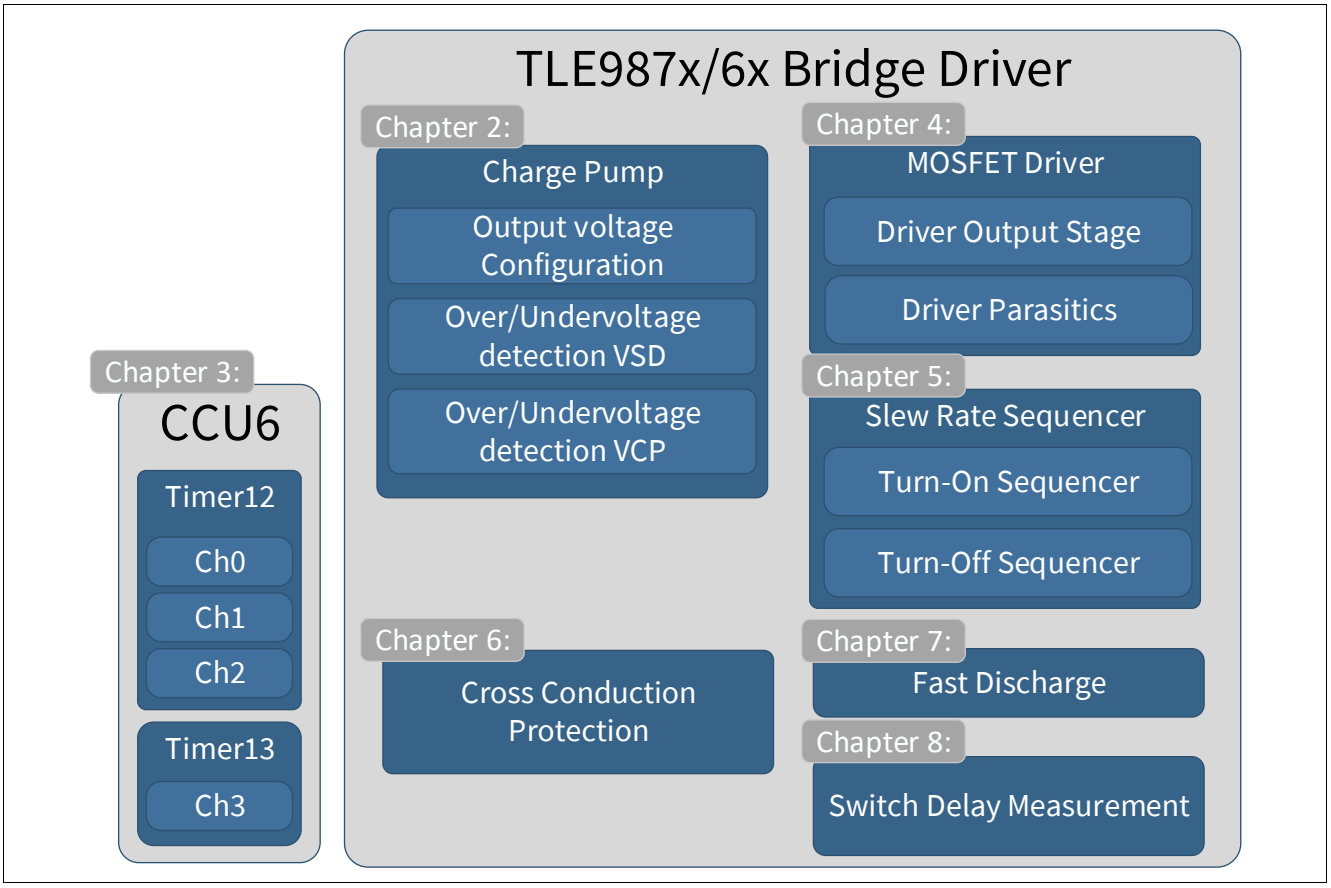

Figure 2 Application Note Content Overview

Chapter 4 explains the bridge driver behavior and the MOSFET-bridge parasitics, that have to be considered in the circuit. The bridge driver sequencer functionality is able to adjust the current sources to modulate the switching behavior of the connected MOSFET. The Slew Rate Sequencer is explained in **Chapter 5**.

2 Charge Pump

The driver is supplied by a 2 stage charge pump. The charge pump enables a duty cycle range from 0 - 100%.

The regulated output voltage is typically VSD + 14 V. The VSD-pin is the supply pin for the charge pump. **Figure 3** shows how the charge pump supplies the driver stage. The VCP pin is the output voltage of the charge pump. An additional external capacitor stabilizes the VCP voltage to VSD.

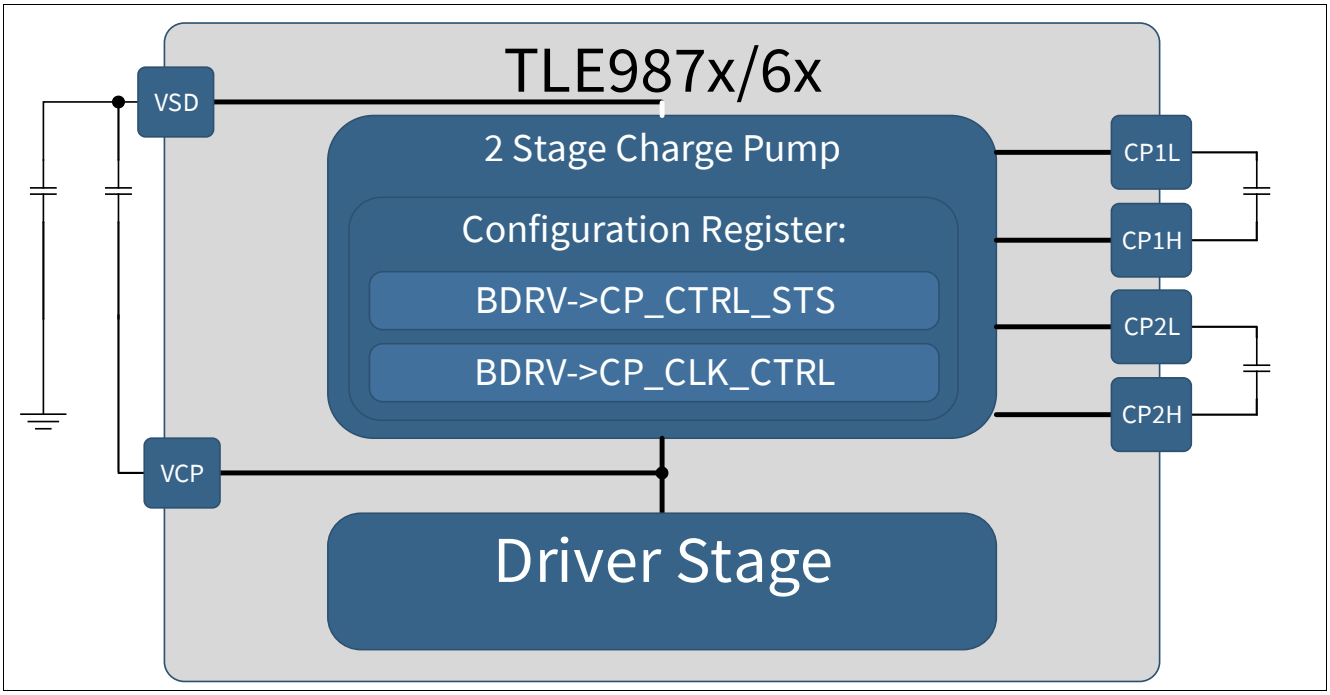

Figure 3 Charge Pump Block Diagram

The functions described in following chapters can be configured in the two charge pump registers:

- CP_CTRL_STS (Charge Pump Control and Status Register)
- CP_CLK_CTRL (Charge Pump Clock Control Register)

2.1 Output voltage configuration

The output voltage of the charge pump can be configured to 14 V or 9 V related to VSD. This function can be used under high VSD voltage conditions. The default configuration for the charge pump output voltage is 14 V. To protect the VCP from exceeding the electrical parameter for overvoltage, the output voltage can be changed to 9 V.

2.2 Over/Undervoltage Detection VSD

Over/undervoltage detection of VSD is a feature to avoid damage to the charge pump, caused by overvoltage or undervoltage. The voltage levels are configurable and can be disabled or enabled separately.

The following bits are part of the register CP_CTRL_STS:

- DRVx_VSDLO_DIS (lower voltage threshold disable)
- DRVx_VSDUP_DIS (upper voltage threshold disable)
- VSD_LOTH_STS (lower voltage threshold status)
- VSD_UPTH_STS (upper voltage threshold status)

2.3 Over/Undervoltage Detection VCP

Over/undervoltage detection of VCP is a safety feature to avoid damage to the charge pump and the bridge driver, caused by overvoltage or undervoltage. The voltage levels are configurable and can be disabled or enabled separately.

The following bits are part of the register CP_CTRL_STS:

- DRVx_VCPLO_DIS (lower voltage threshold disable)
- DRVx_VCPUP_DIS (upper voltage threshold disable)
- VCP_LOTH1_STS (lower voltage threshold status)
- VCP_LOTH2_STS (second threshold, depends on VCP_LOWTH2)
- VCP_LOWTH2 (configuration of discrete threshold level)
- VCP_UPTH_STS (upper voltage threshold status)

The VCP_LOWTH2 register can be configured in discrete values.

Table 1 Charge Pump output voltage lower Threshold for VCP_LOWTH2

Binary Value	Voltage Level
000B	7.325 V
001B	7.654 V
010B	7.982 V
011B	8.309 V
100B	8.638 V
101B	8.966 V
110B	9.293 V
111B	9.620 V

3 Capture Compare Unit (CCU6)

The CCU6 module is described in the user manual in detail.

This chapter will give a brief introduction and explains the connection between the CCU6 and the bridge driver.

The CCU6 is a high-resolution 16-bit capture and compare unit with application specific modes, mainly for AC drive control. Special operating modes support the control of brushless DC-motors using hall sensors or Back-EMF detection. Furthermore, block commutation and control mechanisms for multi-phase machines are supported.

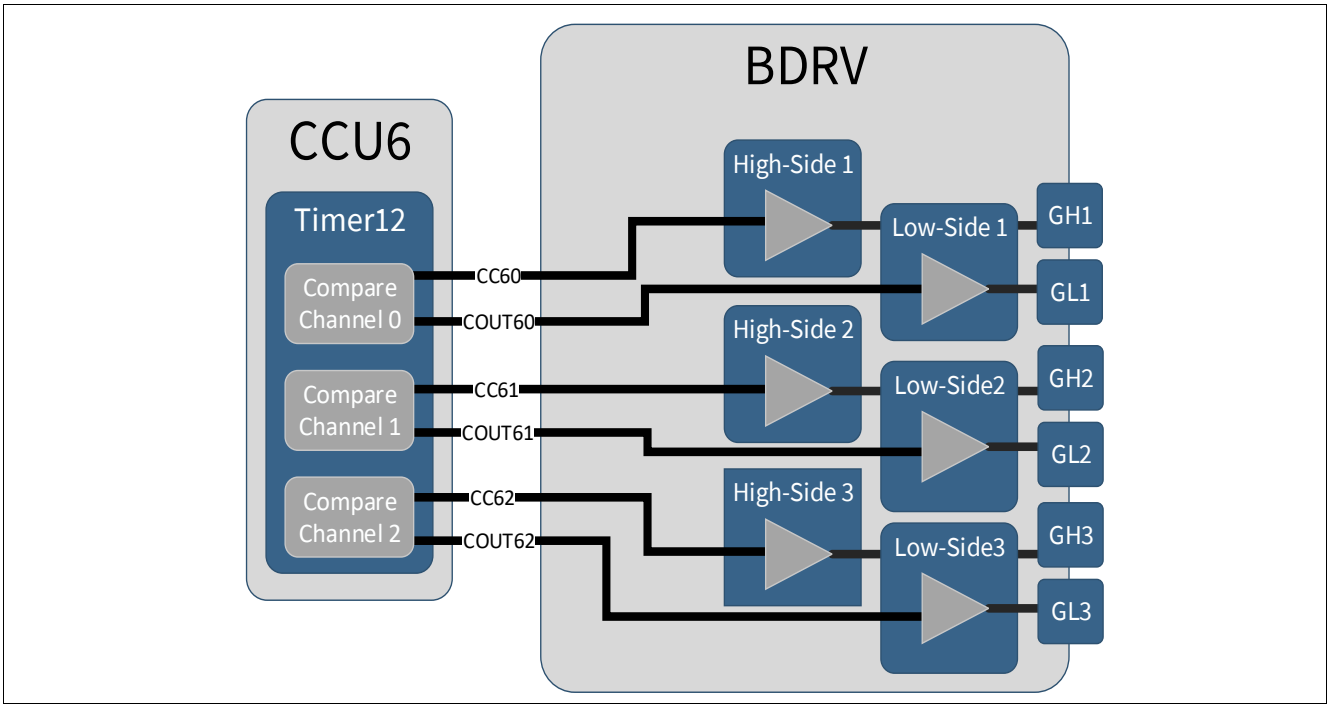

Figure 4 CCU6 Timer12 Connection to BDRV

Figure 4 gives an overview of the Timer12 connections to the driver stage. In addition **Table 2** shows the connection relations. This table is also given in the user manual.

Table 2 Driver Control by CCU6

Driver dedicated to external FET	Corresponding CCU6 channel
LS1	COUT60
LS2	COUT61
LS3	COUT62
HS1	CC60
HS2	CC61
HS3	CC62

4 Gate Driver Behavior considering Circuit Parasitics

This chapter describes some details of the gate driver which help explaining the gate driver behavior.

4.1 Gate Driver Output Stage

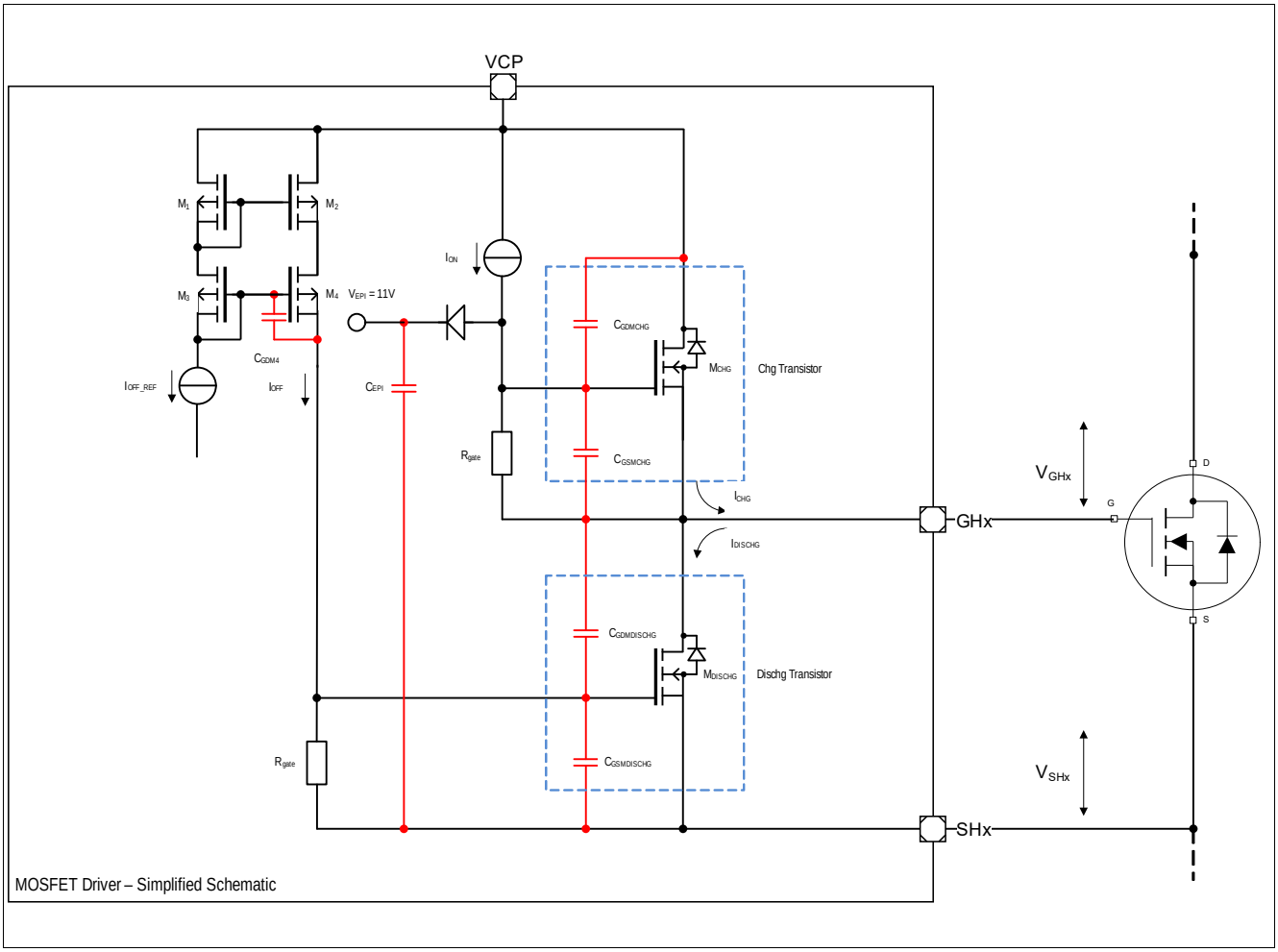

Figure 5 Simplified Schematic of the Gate Driver Output Stage

Figure 5 shows a simplified schematic of the gate driver output stage connected to an external MOSFET. Both the gate charge current and the gate discharge current are generated by an n-channel MOSFET. The V_{gs} of these two currents are generated by bias current from the charge pump voltage V_{cp} through their respective gate to source resistor. The red components are parasitic capacitors.

4.2 Gate Driver Parasitics and their influence

The gate drivers for both high-side and low-side MOSFETs are identical. The only difference is the connection to the external circuitry: the voltage at the SHx pin of the low-side gate driver is quite stable and near to ground potential (source of the external low-side MOSFET) and the voltage at the GHx pin of the high-side gate driver follows the pulse-width-modulated motor phase voltage at the source of the external high-side MOSFET.

In the second case (i.e. at the high-side MOSFETs), the parasitic capacitors shown in **Figure 5** influence the behavior of the output MOSFETs M_{CHG} and M_{DISCHG}:

- When charging the gate of the external MOSFET, the voltage at the SHx pin and the GHx pin rises. As a result, the parasitic capacitor C_{GDMCHG} has to be charged. This means that a portion of I_{ON} flows into C_{GDMCHG} resulting in a smaller voltage drop across the gate-to-source resistor of M_{CHG} and therefore a smaller gate

charge current I_{CHG} during the fast parts of the slope. This acts like a negative feedback limiting the slope speed.

- When discharging the gate of the external MOSFET, the voltage at the SHx pin falls. As a result, the parasitic capacitor *C*GDM4 pulls down the gate node of M4. The charge current flows additionally to I_{OFF} through the gate-to-source resistor leading to higher gate-to-source voltage at M_{DISCHG} and therefore a larger gate discharge current I_{DISCHG} during the fast parts of the slope. This acts like a positive feedback accelerating the slope speed.

Both effects depend on the speed of the voltage transient at the SHx pin, because the currents for charging C_{GDMCHG} and discharging C_{GDM4} are proportional to $\Delta V/\Delta t$ across their terminals ($I = C * \Delta V/\Delta t$). More details will be given in the following chapter.

5 Slew Rate Sequencer for MOSFET switching state control

The sequencer of TLE986x/TLE987x supports the control of the MOSFET switching phases, see **Figure 6**.

It contains the following subblocks:

- Turn-on sequencer with configuration options for all 4 switch-on phases
- Turn-off sequencer with configuration options of all 4 switch-off phases.
- Timer for measuring the MOSFET turn-on and turn-off delay for adaptive sequencer setting programming within the application software.

This chapter introduces the sequencer configuration. It will help the user find a suitable setting for his application.

5.1 Turn-On Sequencer Programming for Switch-On Phase

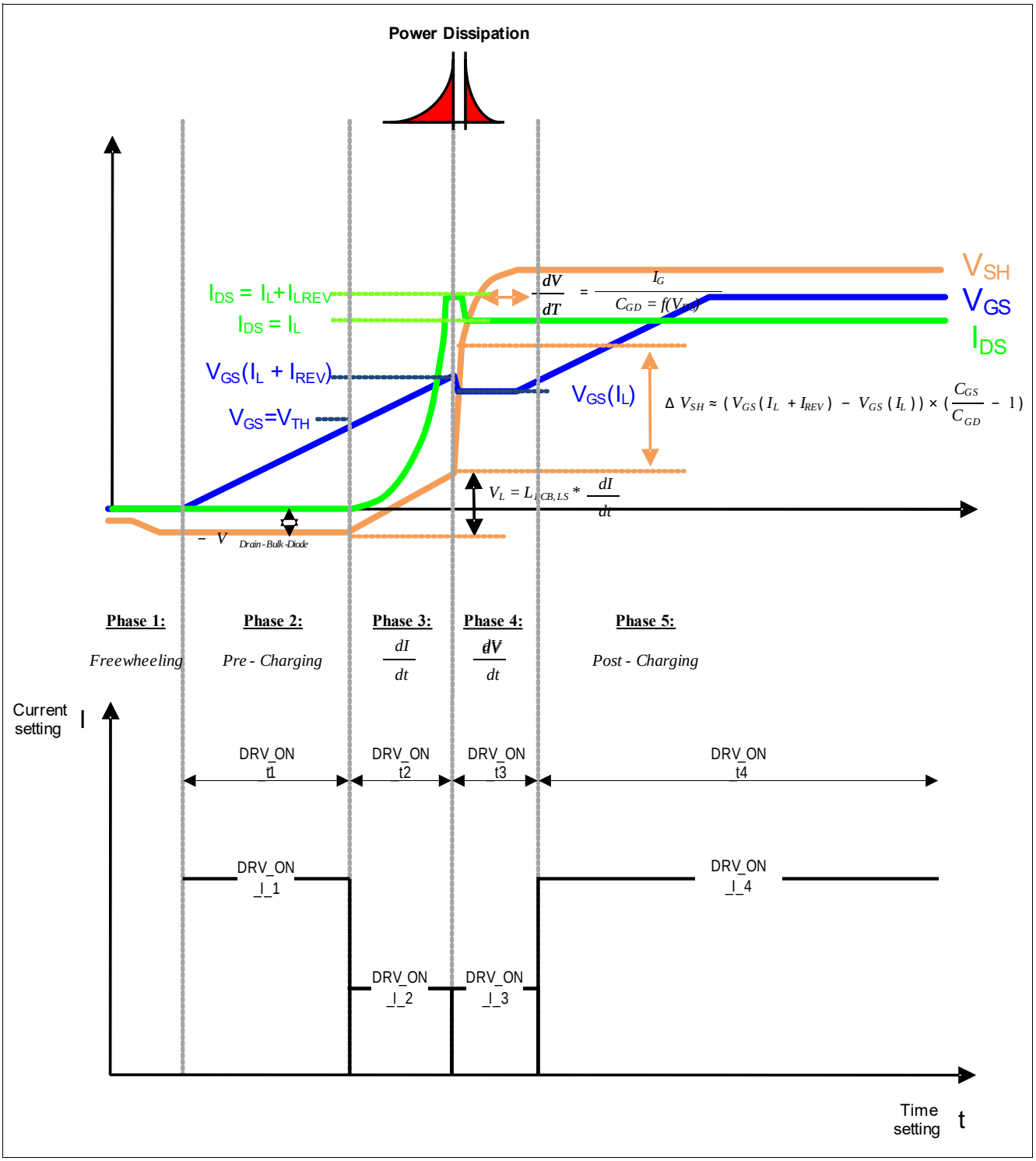

Figure 6 Fitting the Sequencer Phases to MOSFET Switching Phases for Turn On

Slew Rate Sequencer for MOSFET switching state control

Calculation of Time Settings for Phase 2 - Charge Process

In phase 2 of the switch-on process, the MOSFET gate is taken from 0V to the threshold voltage. During this process, the intrinsic gate source capacitance C_{GS} of the MOSFET is charged. The required time is calculated using the following formula:

(5.1)

$$t_1 = \frac{(C_{GS} + C_{GD}) * V_{thMOSFET}}{I_1}$$

where $V_{thMOSFET}$ is the datasheet value for the threshold voltage. Adding two external capacitances C_{GS_ext} and C_{GD_ext} will lead to the following formula:

(5.2)

$$t_1 = \frac{(C_{GS} + C_{GD} + C_{GS\_ext} + C_{GD\_ext}) * V_{thMOSFET}}{I_1}$$

For the gate-to-drain capacitance in the OFF state, the datasheet shows that the value is negligible compared to the gate-to-source capacitance. This provides the following formula:

(5.3)

$$t_1 = \frac{(C_{GS} + C_{GS\_ext} + C_{GD\_ext}) * V_{thMOSFET}}{I_1}$$

Note: The procedure for finding the right settings for the sequencer should always be based on predefined timing.
To meet this timing requirement, the charge current should be adapted accordingly.

Calculation of Time Settings for Phase 3 - Charge Process

In phase 3 of the switch-on-process, the MOSFET gate is taken from the threshold voltage up to the beginning of the Miller plateau voltage. During this process, the MOSFET intrinsic gate source capacitance C_{GS} is charged. Again, the C_{GD} can be neglected as the drain-to-source voltage is still constant. The required time is calculated by the following equation:

(5.4)

$$t_2 = \frac{C_{GS} * (V_{plateau} - V_{thMOSFET})}{I_2}$$

where $V_{plateau}$ is the datasheet value for the beginning of the Miller plateau. Adding two external capacitances C_{GS_ext} and C_{GD_ext} will lead to the following formula:

(5.5)

$$t_2 = \frac{(C_{GS} + C_{GS\_ext} + C_{GD\_ext}) * (V_{plateau} - V_{thMOSFET})}{I_2}$$

If the resulting time value t_2 for the third phase exceeds the maximum possible setting, the current value can be readjusted accordingly.

Calculation of Time Settings for Phase 4 - Charge Process

In phase 4 of the switch-on-process, the MOSFET gate is taken from the beginning to the end of the Miller plateau. During this phase, the charge of the MOSFET's intrinsic gate-to-source capacitance C_{GS} continues to increase. Additionally, the C_{GD} capacitance (which is heavily voltage-dependent) becomes significant. The required time is calculated as follows:

(5.6)

$$t_3 = \frac{C_{GS} * (V_{plateau\_end} - V_{plateau\_start}) + Q_{GD}}{I_3}$$

where $V_{plateau\_end}$ is the voltage at the end of the Miller plateau. Adding two external capacitances C_{GS_ext} and C_{GD_ext} will lead to the following formula (V_{DS_max} reflects the total voltage swing at the motor phase):

(5.7)

$$t_3 = \frac{((C_{GS} + C_{GS\_ext} + C_{GD\_ext}) * (V_{plateau\_end} - V_{plateau\_start})) + C_{GD\_ext} * V_{DS\_max} + Q_{GD}}{I_3}$$

If the resulting time value t_3 for the fourth phase exceeds the maximum possible setting, the current value can be readjusted accordingly.

Calculation of Time Settings for Phase 5 - Charge Process

In phase 5 of the switch-on-process, the MOSFET gate is charged completely. The time can be calculated with the help of the following equation:

(5.8)

$$t_4 = \frac{Q_G - (Q_{GS} + Q_{GD})}{I_4}$$

where Q_G is the datasheet value of the total gate charge, Q_{GS} is the gate-to-source charge and Q_{GD} is the gate-to-drain charge. Adding two external capacitances C_{GS_ext} and C_{GD_ext} will lead to the following formula:

(5.9)

$$t_4 = \frac{((C_{GS\_ext} + C_{GD\_ext}) * (V_{out\_driver} - V_{plateau\_start}) + (Q_G - (Q_{GS} + Q_{GD})))}{I_4}$$

If the resulting time value t_4 for the fifth phase exceeds the maximum possible setting, the current value can be readjusted accordingly.

5.2 Turn-Off Sequencer Programming for Switch-Off Phase

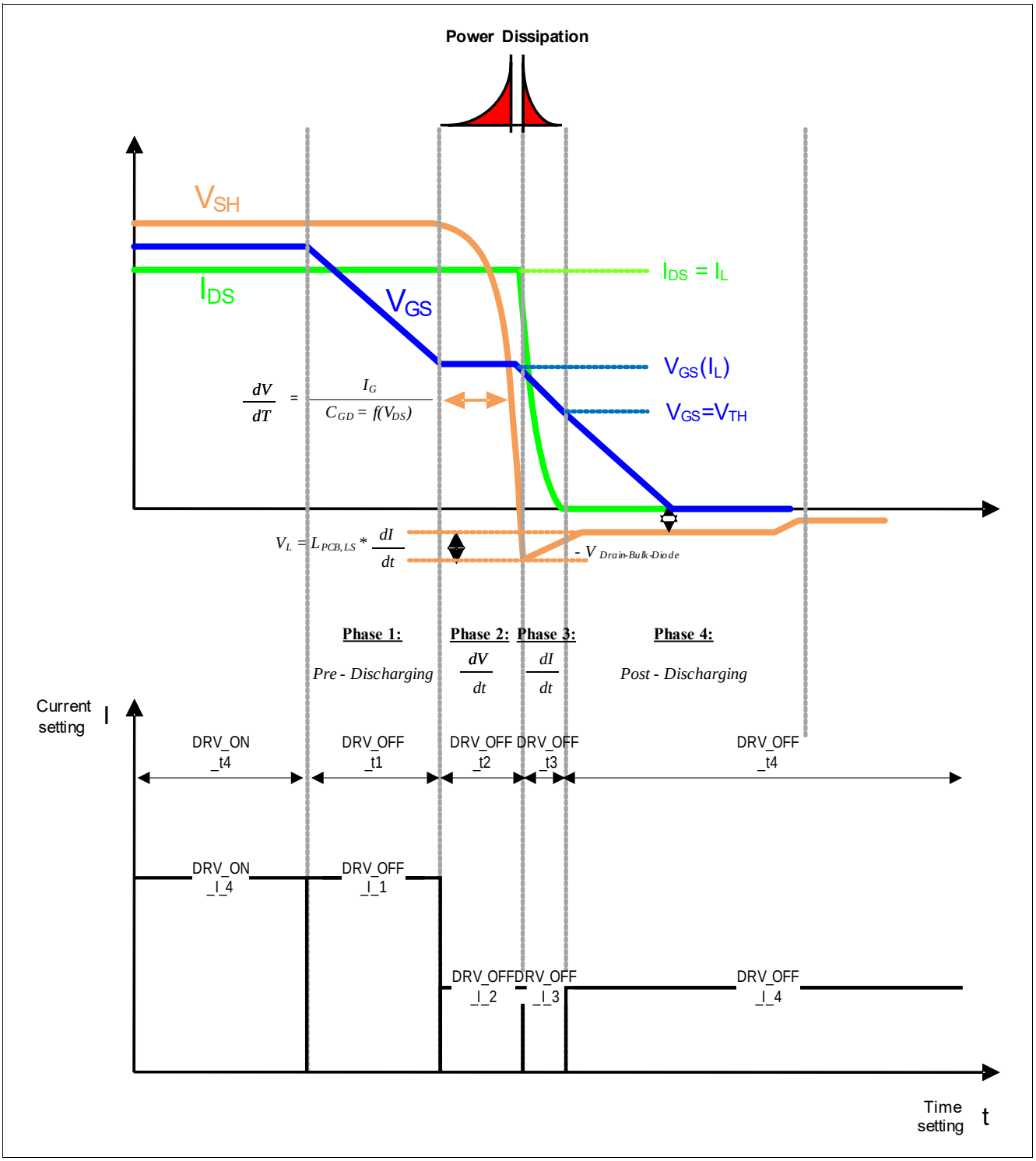

Figure 7 Fitting the Sequencer Phases to MOSFET Switching Phases for Turn Off

Slew Rate Sequencer for MOSFET switching state control

Calculation of Time Settings for Phase 1 - Discharge Process

In phase 1 of the switch-off process, the MOSFET gate is discharged from the max. output voltage provided by the driver down to the beginning of the plateau voltage. During this process, the MOSFET's intrinsic total gate charge Q_G is reduced. The time required is calculated by the equation:

(5.10)

$$t_1 = \frac{Q_G - (Q_{GS} + Q_{GD})}{I_1}$$

where Q_G is the value for the total gate charge, Q_{GS} is the gate-source charge and Q_{GD} is the gate-drain charge. All parameters can be found in the datasheet. Adding two external capacitances C_{GS_ext} and C_{GD_ext} will lead to the following formula:

(5.11)

$$t_1 = \frac{((C_{GS\_ext} + C_{GD\_ext}) * (V_{out\_driver} - V_{plateau\_start}) + (Q_G - (Q_{GS} + Q_{GD})))}{I_1}$$

Calculation of Time Settings for Phase 2 - Discharge Process

In phase 2 of the switch-off process, the MOSFET gate is taken down to the beginning of the Miller plateau voltage. During this phase, the MOSFET's intrinsic gate capacitance C_{GS} continues to be discharged. In addition, the charge of C_{GD} needs to be removed. The time required is calculated as follows:

(5.12)

$$t_2 = \frac{C_{GS} * (V_{plateau\_end} - V_{plateau\_start}) + Q_{GD}}{I_2}$$

where $V_{plateau\_end}$ and $V_{plateau\_start}$ are values taken from the datasheet. Adding two external capacitances C_{GS_ext} and C_{GD_ext} will lead to the following formula (V_{DS_max} reflects the total voltage swing at the motor phase):

(5.13)

$$t_2 = \frac{((C_{GS} + C_{GS\_ext} + C_{GD\_ext}) * (V_{plateau\_end} - V_{plateau\_start})) + C_{GD\_ext} * V_{DS\_max} + Q_{GD}}{I_2}$$

If the resulting time value t_2 for the second phase exceeds the maximum possible setting, the current value can be readjusted accordingly.

Calculation the Time Settings for Phase 3 - Discharge Process

In phase 3 of the switch-off process, the gate is discharged further from the start of the plateau voltage until it reaches the threshold voltage. During this process, the MOSFET's intrinsic gate-to-source capacitance C_{GS} continues to be discharged. The gate-to-drain capacitance C_{GD} can again be neglected as it is now at the minimum value.

(5.14)

$$t_3 = \frac{C_{GS} * (V_{plateau} - V_{thMOSFET})}{I_3}$$

where $V_{plateau}$ is the datasheet value of the beginning of the Miller plateau. Adding two external capacitances C_{GS_ext} and C_{GD_ext} will lead to the following formula:

(5.15)

$$t_3 = \frac{(C_{GS} + C_{GS\_ext} + C_{GD\_ext}) * (V_{plateau} - V_{thMOSFET})}{I_3}$$

If the resulting time value t_3 for the third phase exceeds the maximum possible setting, the current value can be readjusted accordingly.

Calculation of Time Settings for Phase 4 - Discharge Process

In phase 4 of the switch-on process, the MOSFET gate is discharged completely.

(5.16)

$$t_4 = \frac{(C_{GS} + C_{GD}) * V_{thMOSFET}}{I_4}$$

where $V_{thMOSFET}$ is the datasheet value of the threshold voltage. Adding two external capacitances C_{GS_ext} and C_{GD_ext} will lead to the following formula:

(5.17)

$$t_4 = \frac{(C_{GS} + C_{GD} + C_{GS\_ext} + C_{GD\_ext}) * V_{thMOSFET}}{I_4}$$

If the resulting time value t_4 for the fourth phase exceeds the maximum possible setting, the current value can be readjusted accordingly.

5.3 Sequencer Settings Example

This section describes how to get proper slew rate sequencer settings for the Infineon MOSFET IPD90N04S4-03 as an example. As external capacitors, C_{GS} = 10 nF and C_{GD} = 1 nF are used.

5.3.1 Target Slope Timing and Assumptions

The starting point for proper slew rate sequencer settings is the definition of the slope timing. In this example, the target switching time from the pre-charging or pre-discharging phases until the end of the slope is 600 ns.

The first three sequencer phase durations for charging the MOSFET gate are set to:

- Pre-Charging Phase: DRV_ON_t1 = 200 ns
- $\Delta I/\Delta t$ Phase: DRV_ON_t2 = 200 ns
- $\Delta V/\Delta t$ Phase: DRV_ON_t3 = 200 ns

The first three sequencer phase durations for discharging the MOSFET gate are set to:

- Pre-Discharging Phase: DRV_OFF_t1 = 400 ns
- $\Delta V/\Delta t$ Phase: DRV_OFF_t2 = 200 ns
- $\Delta I/\Delta t$ Phase: DRV_OFF_t3 = 200 ns

Notes

1. *Since the post-charging and post-discharging phases do no more contribute to the slope they are not considered here and therefore the 4th sequencer phases are set to the same values (current value and duration value) than the first ones.*
2. *The asymmetry between pre-charging a MOSFET from V_{GS} = 0 V to the miller plateau and pre-discharging a MOSFET from V_{GS} = $V_{GS(max)}$ to the miller plateau is reflected by setting the pre-discharging phase duration to the double value than the pre-charging phase duration to get similar gate charging/discharging current values.*

5.3.2 Calculating the Current Set Point Values

Based on the above mentioned assumptions a starting set of current set point values for the sequencer can be calculated:

- DRV_ON_I1 = 226 mA[1)]
- DRV_ON_I2 = 145 mA[2)]
- DRV_ON_I3 = 35 mA[3)]
- DRV_ON_I4 = DRV_ON_I1
- DRV_OFF_I1 = 234mA[4)]
- DRV_OFF_I2 = DRV_ON_I2
- DRV_OFF_I3 = DRV_ON_I3
- DRV_OFF_I4 = DRV_OFF_I1

1) See **Equation (5.11)**. $C_{GS} + C_{GD}$ = 4.05 nF (see C_{iss} in MOSFET datasheet), $V_{thMOSFET}$ = 3 V (see $V_{GS(th)}$ in MOSFET datasheet).

2) See **Equation (5.13)**. C_{GS} = 2.63 nF (C_{GS} estimated from C_{iss} in MOSFET datasheet: $C_{GS} = C_{iss}$ – 35%), $V_{thMOSFET}$ = 3 V (see $V_{GS(th)}$ in MOSFET datasheet), $V_{plateau}$ = 5.8 V (see $V_{plateau}$ in MOSFET datasheet).

3) See **Equation (5.15)**. Q_{GD} = 7 nC (see Q_{GD} in MOSFET datasheet), V_{DS_max} = 13 V (i.e., the voltage swing at the motor phase). Simplification of (4.7) by setting $V_{plateau\_end} = V_{plateau\_start}$ removes the capacitance-dependant terms.

4) See **Equation (5.17)**. V_{out_driver} = 12.5 V (typical gate driver output voltage), $V_{plateau\_start}$ = 5.8 V (see $V_{plateau}$ in MOSFET datasheet), Q_G = 51 nC, Q_{GS} = 24 nC, Q_{GD} = 7 nC (see corresponding parameters in MOSFET datasheet).

5.3.3 Bridge Driver Sequencer Register Settings

The next step is to define the bridge driver control register contents to enable the slew rate sequencer and to map the calculated current set point values from **Chapter 5.3.2** to values available in the bridge driver registers.

CTRL3

In the CTRL3 register the slew rate sequencer can be enabled and the correct gate current range of the gate driver can be set:

- Bit 15, “OFF_SEQ_EN”: set to 1 (enable turn-off slew rate sequencer)
- Bit 14, “IDISCHARGEDIV2_N”: set to 1 (full range up to 300mA is available for gate discharge currents)[1)]
- Bit 7, “ON_SEQ_EN”: set to 1 (enable turn-on slew rate sequencer)
- Bit 6, “ICHARGEDIV2_N”: set to 1 (full range up to 300 mA is available for gate charge currents)[2)]

Note: The descriptions of the bit fields “ICHARGE_TRIM” and “IDISCHARGE_TRIM” of the register “CTRL3” show all available full-range charge/discharge current settings (for half range the given current values must be divided by 2). These values are also the values for the current set point bit fields of the sequencer registers.

ON_SEQ_CTRL

In the ON_SEQ_CTRL register all 4 phases of the turn-on slew rate sequencer can be programmed. It consists of 4 current set point values and the corresponding 4 phase duration values.

The duration bit fields (“DRV_ON_t*”) are 3 bits wide and provide the following 8 duration values:

- 0_H: 50 ns
- 1_H: 100 ns
- 2_H: 150 ns
- 3_H: 200 ns
- 4_H: 250 ns
- 5_H: 300 ns
- 6_H: 350 ns
- 7_H: 400 ns

In the current example all turn-on sequencer duration bit fields (“DRV_ON_t*”) are set to 200ns, i.e. 3_H.

The calculated current set point values must be mapped to the available current set point values of the gate drivers which are described in the bit field “ICHARGE_TRIM” of the “CTRL3” register. If the exact value is not available the next smaller one is selected:

- DRV_ON_I1 = 226 mA: The next smaller available set point value is 218.40 mA (10101_B=15_H=21_D)
- DRV_ON_I2 = 145 mA: The next smaller available set point value is 140.30 mA (01101_B=$0D_H$=13_D)
- DRV_ON_I3 = 100 mA: The next smaller available set point value is 98 mA (01001_B=09_H=9_D)
- DRV_ON_I4 = DRV_ON_I1: 10101_B=15_H=21_D

As a result, the value of the ON_SEQ_CTRL register for this example is: $AB6B4BAB_H$.

1) The maximum calculated discharge current is 234 mA. Full current range must be enabled because the maximum current at half range is 150 mA.

2) The maximum calculated charge current is 226 mA. Full current range must be enabled because the maximum current at half range is 150 mA.

Slew Rate Sequencer for MOSFET switching state control

OFF_SEQ_CTRL

In the OFF_SEQ_CTRL register all 4 phases of the turn-off slew rate sequencer can be programmed. It consists of 4 current set point values and the corresponding 4 phase duration values.

The duration bit fields (“DRV_OFF_t*”) are 3 bits wide and provide the following 8 duration values:

- 0_H: 50 ns
- 1_H: 100 ns
- 2_H: 150 ns
- 3_H: 200 ns
- 4_H: 250 ns
- 5_H: 300 ns
- 6_H: 350 ns
- 7_H: 400 ns

In the current example the first turn-off sequencer duration bit field (“DRV_OFF_t1”) is set to 400 ns, i.e. 7_H, and the remaining duration bit fields (“DRV_OFF_t*”) are set to 200 ns, i.e. 3_H.

The calculated current set point values must be mapped to the available current set point values of the gate drivers which are described in the bit field “IDISCHARGE_TRIM” of the “CTRL3” register. If the exact value is not available the next smaller one is selected:

- DRV_OFF_I1 = 234 mA: The next smaller available set point value is 227.40 mA (10110_B=16_H=22_D)
- DRV_OFF_I2 = 145 mA: The next smaller available set point value is 140.30 mA (01101_B=$0D_H$=13_D)
- DRV_OFF_I3 = 100 mA: The next smaller available set point value is 98 mA (01001_B=09_H=9_D)
- DRV_OFF_I4 = DRV_ON_I1: 10110_B=16_H=22_D

As a result, the value of the OFF_SEQ_CTRL register for this example is: $B76B4BB3_H$.

5.3.4 Slew Rate Measurements

This section shows the measurement results of the calculated values from the previous sections.

Turn-On Slew Rate Sequencer Measurement

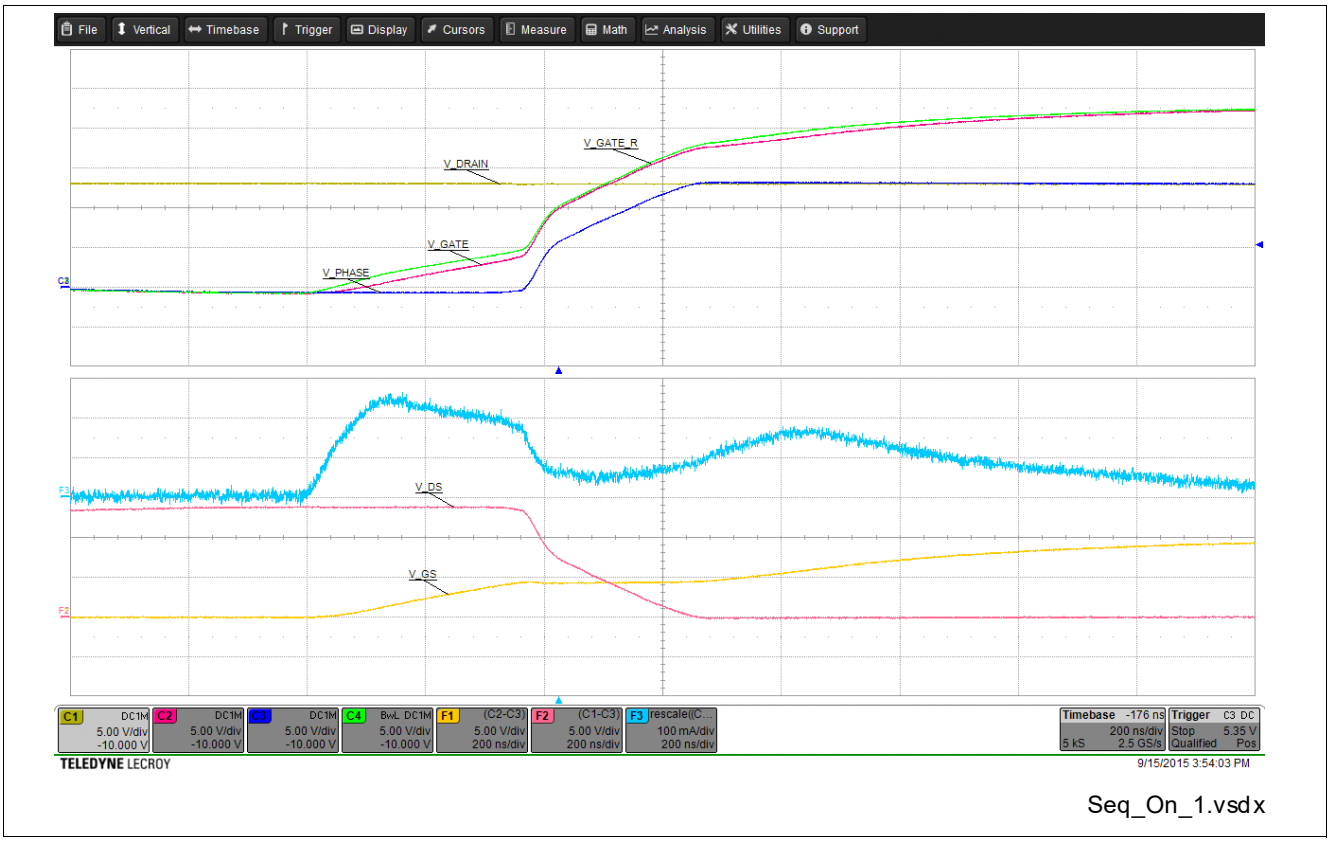

Figure 8 Turn-On Slew Rate Sequencer

Figure 8 shows the measurement results of the turn-on slew rate sequencer settings as defined in **Chapter 5.3.3** (**ON_SEQ_CTRL**).

The signals shown in the scope plot are:

- Channel C1 (yellow): drain voltage of the high-side MOSFET
- Channel C2 (red): gate voltage of the high-side MOSFET
- Channel C3 (blue): source voltage of the high-side MOSFET
- Channel C4 (green): gate voltage of the high-side MOSFET before a 4.7 Ω gate resistor for gate current measurement
- Channel F1 (orange): calculated gate-to-source voltage of the high-side MOSFET
- Channel F2 (purple): calculated drain-to-source voltage of the high-side MOSFET
- Channel F3 (cyan): calculated gate current through the 4.7 Ω gate resistor

These settings serve as a good starting point for further optimization. The total switch-on time is a little bit longer than the target value of 600 ns because the actually programmed current set point values are lower than the calculated ones. Additionally, the limited gate driver dynamic behavior leads to too high gate charging current values during the $\Delta I/\Delta t$ phase and at the beginning of the $\Delta V/\Delta t$ phase which results in a faster voltage transient at the beginning of the slope.

Turn-Off Slew Rate Sequencer Measurement

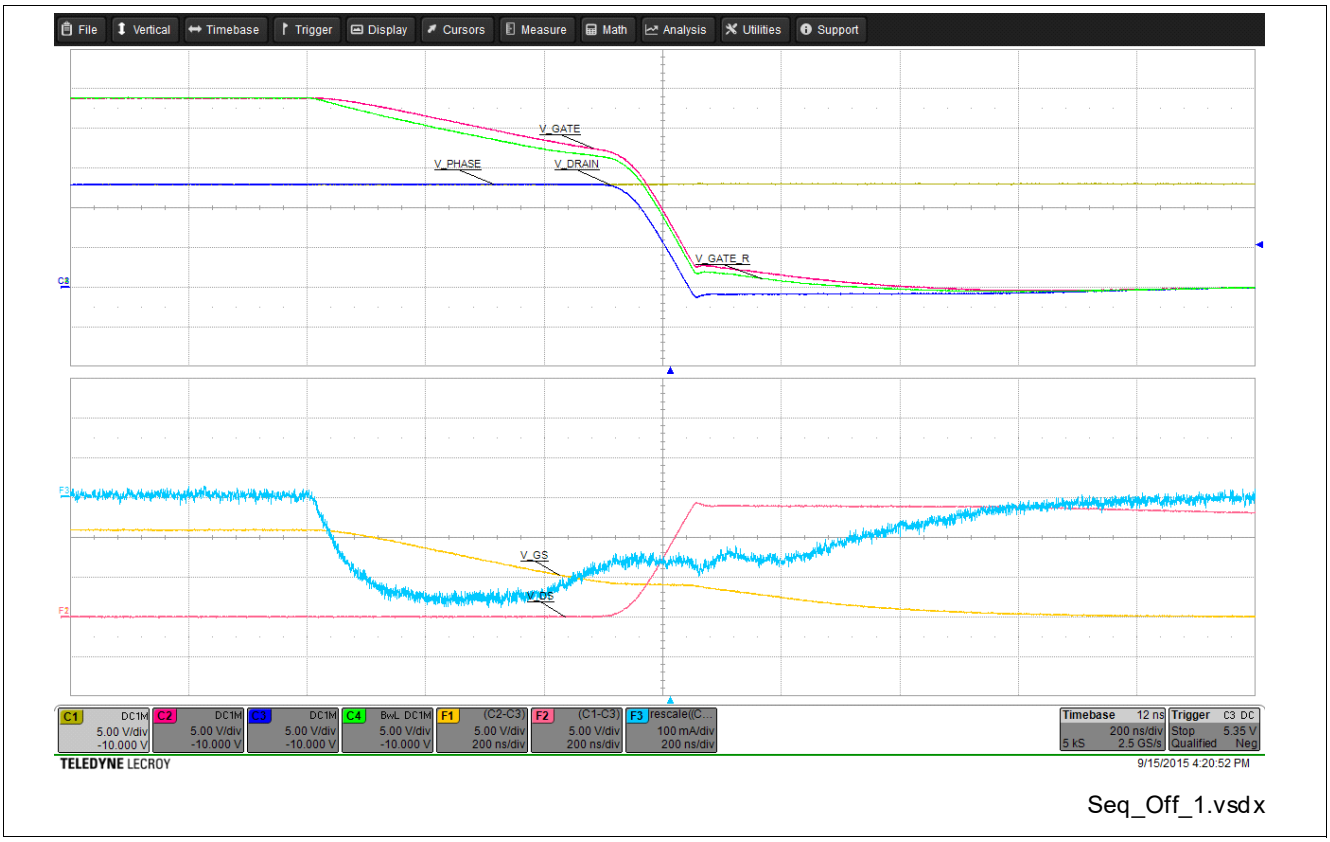

Figure 9 Turn-Off Slew Rate Sequencer

Figure 9 shows the measurement results of the Turn-Off Slew Rate Sequencer settings as defined in **Chapter 5.3.3** (**OFF_SEQ_CTRL**).

The signals shown in the scope plot are:

- Channel C1 (yellow): drain voltage of the high-side MOSFET
- Channel C2 (red): gate voltage of the high-side MOSFET
- Channel C3 (blue): source voltage of the high-side MOSFET
- Channel C4 (green): gate voltage of the high-side MOSFET before a 4.7 Ω gate resistor for gate current measurement
- Channel F1 (orange): calculated gate-to-source voltage of the high-side MOSFET
- Channel F2 (purple): calculated drain-to-source voltage of the high-side MOSFET
- Channel F3 (cyan): calculated gate current through the 4.7 Ω gate resistor

These settings serve as a good starting point for further optimization. The total switch-off time is a little bit longer than the target value of 600 ns because the actually programmed current set point values are lower than the calculated ones.

5.3.5 Iterative Optimization

The measurement results of **Chapter 5.3.4** show that the calculated values of **Chapter 5.3.2** give already reasonable results. Further optimization is needed for the turn-on edge. One possibility, which will be demonstrated here, is to decrease the total current level by a certain percentage while the timing remains unchanged. This will lead to a longer delay time and a slower slope but helps the gate driver to settle closer to the target current values.

Slew Rate Sequencer for MOSFET switching state control

As an example, the current values will be decreased by 20% (correction factor of 0.8):

- DRV_ON_I1 = 226mA * 0.8 = 180.8 mA: The next smaller available set point value is 180.30 mA (10001_B=11_H=17_D)
- DRV_ON_I2 = 145 mA * 0.8 = 116mA: The next smaller available set point value is 108.50 mA (01010_B=$0A_H$=10_D)
- DRV_ON_I3 = 100 mA * 0.8 = 80 mA: The next smaller available set point value is 76.20 mA (00111_B=07_H=7_D)

As a result, the value of the ON_SEQ_CTRL register for the first iteration is: $8B533B8B_H$.

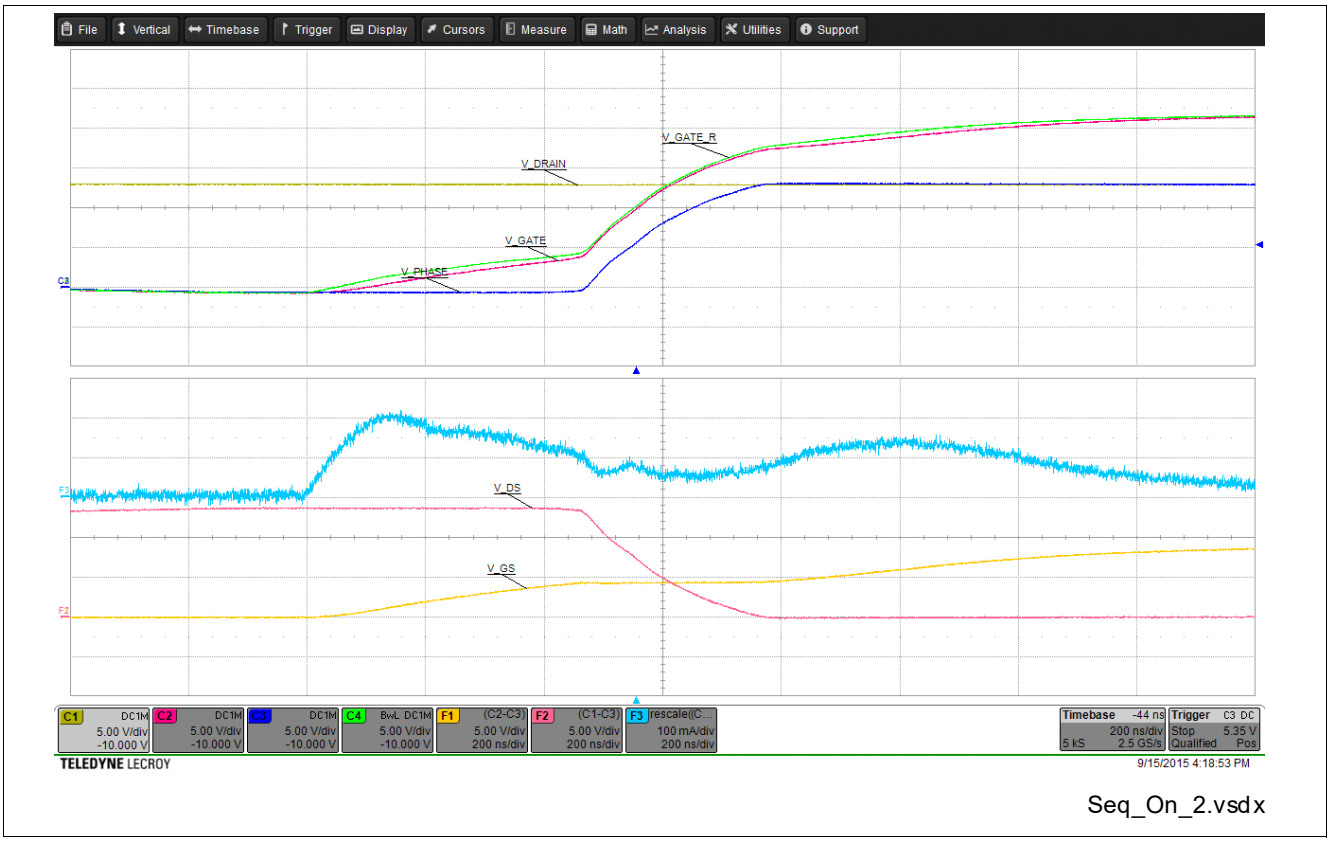

Figure 10 Turn-On Slew Rate Sequencer with optimized Settings

Figure 10 shows the measurement results with the optimized turn-on slew rate sequencer settings.

The signals shown in the scope plot are:

- Channel C1 (yellow): drain voltage of the high-side MOSFET
- Channel C2 (red): gate voltage of the high-side MOSFET
- Channel C3 (blue): source voltage of the high-side MOSFET
- Channel C4 (green): gate voltage of the high-side MOSFET before a 4.7 Ω gate resistor for gate current measurement
- Channel F1 (orange): calculated gate-to-source voltage of the high-side MOSFET
- Channel F2 (purple): calculated drain-to-source voltage of the high-side MOSFET
- Channel F3 (cyan): calculated gate current through the 4.7 Ω gate resistor

As expected, the switch-on delay time is longer and the slope slower, but its $\Delta V/\Delta t$ is now quite constant over time.

6 Cross-Conduction Protection

The driver circuit of the TLE986x/TLE987x includes a hardware cross-conduction protection logic. This protection mechanism is illustrated by the figures below, which include the following signals:

- LS_ON_CCU6: ON signal of MOSFET low side driver generated by on-chip PWM engine.
- HS_ON_CCU6: ON signal of MOSFET high side driver generated by on-chip PWM engine.
- Dead time counter: user programmable dead time counter.
- LS_ON_CCU6_masked: ON signal of MOSFET low side driver masked by the hardware cross-conduction protection.
- HS_FDISCHG: fast discharge signal of MOSFET high side driver.
- V_HS_GATE: gate voltage of MOSFET high side driver.
- V_LS_GATE: gate voltage of MOSFET low side driver.

6.1 Case 1: Cross-Conduction Protection in CCU6 is Too Short

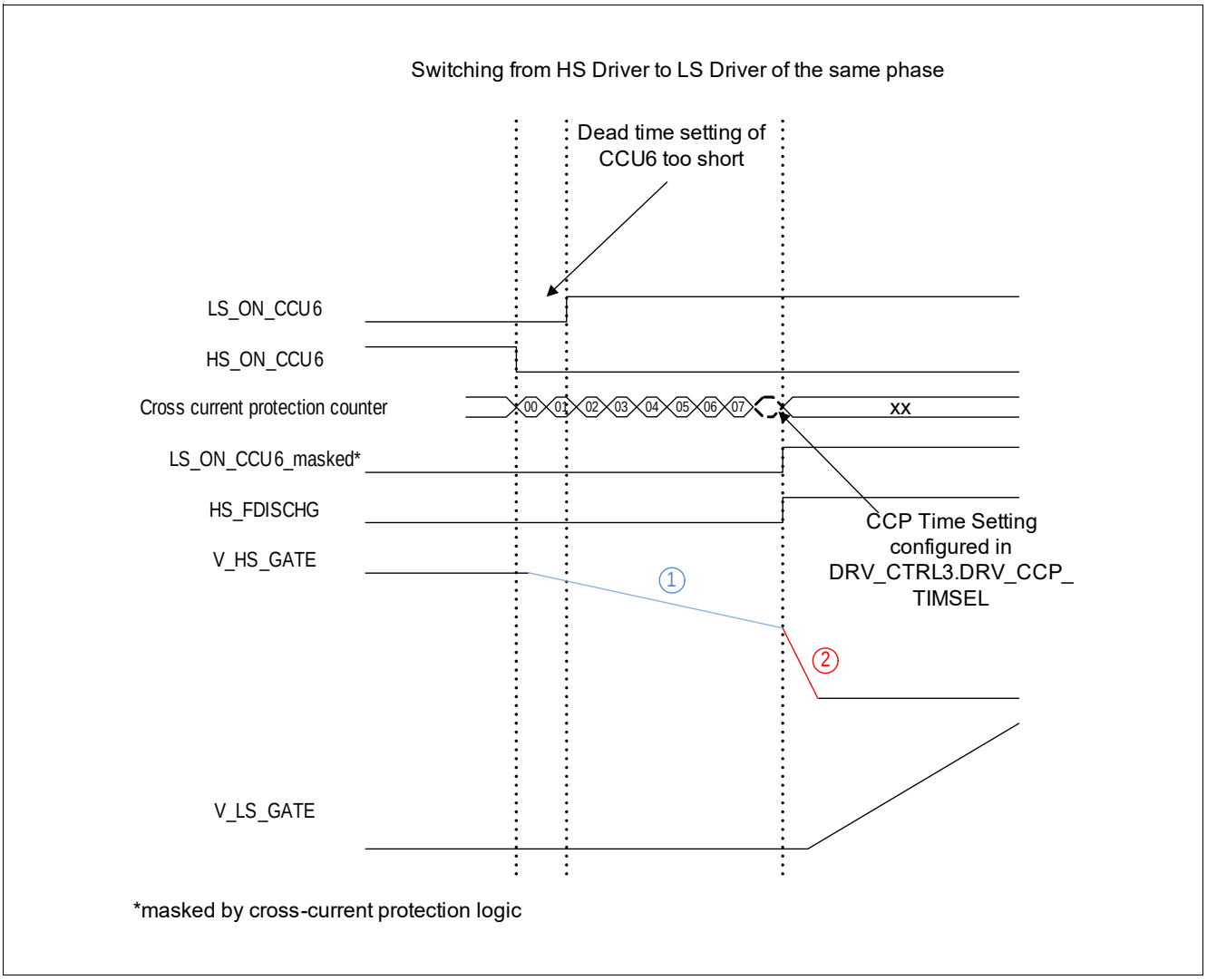

Figure 11 Cross-Conduction Protection Logic - Case1

The timing diagram shows the case where the MOSFET low side driver is switched on directly after switching off the MOSFET high side driver. In this case, the signal of the low side driver is delayed by the cross-conduction time. When this time has elapsed, the ON signal (LS_ON_CCU6_masked) is propagated to the driver module. In addition to the delay of the low side driver's ON signal, the high side driver's fast discharge feature is enabled to rapidly discharge the high side FET gate below its threshold. This avoids cross current in the inverter stage.

6.2 Case 2: Cross-Conduction Protection in CCU6 is properly set

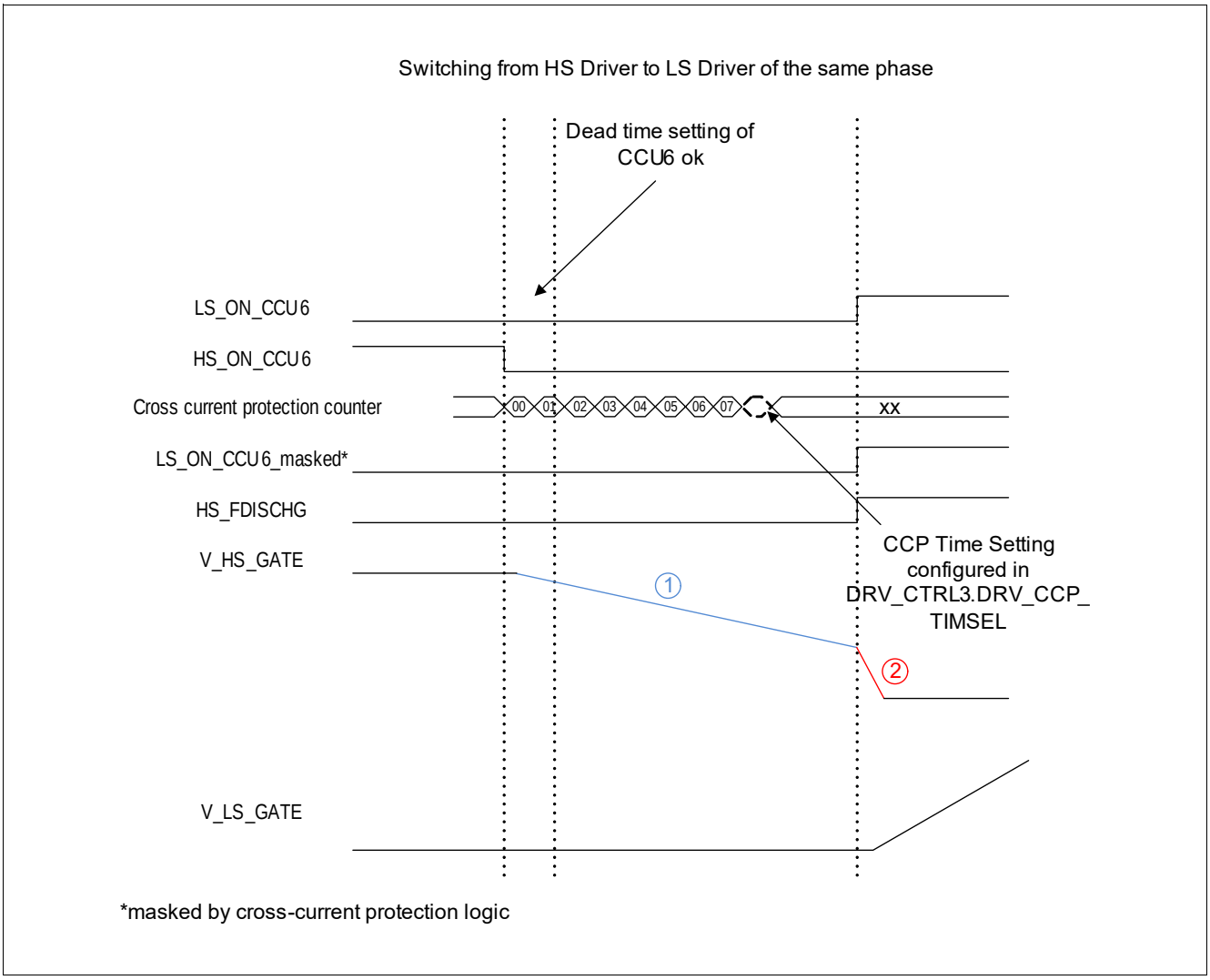

Figure 12 Cross-Conduction Protection Logic - Case2

The timing diagram shows the case where the MOSFET low side driver is switched on directly after switching off the MOSFET high side driver. In this case, the signal of the low side driver is delayed by the cross-conduction time. After the time has elapsed, the ON signal (LS_ON_CCU6_masked) is propagated to the driver module.

7 Fast Discharge Functionality

The hard-wired cross-conduction protection uses the fast discharge feature to ensure a short turn-off time for the conducting MOSFET of the active inverter stage. The implementation of the fast discharge feature is shown below:

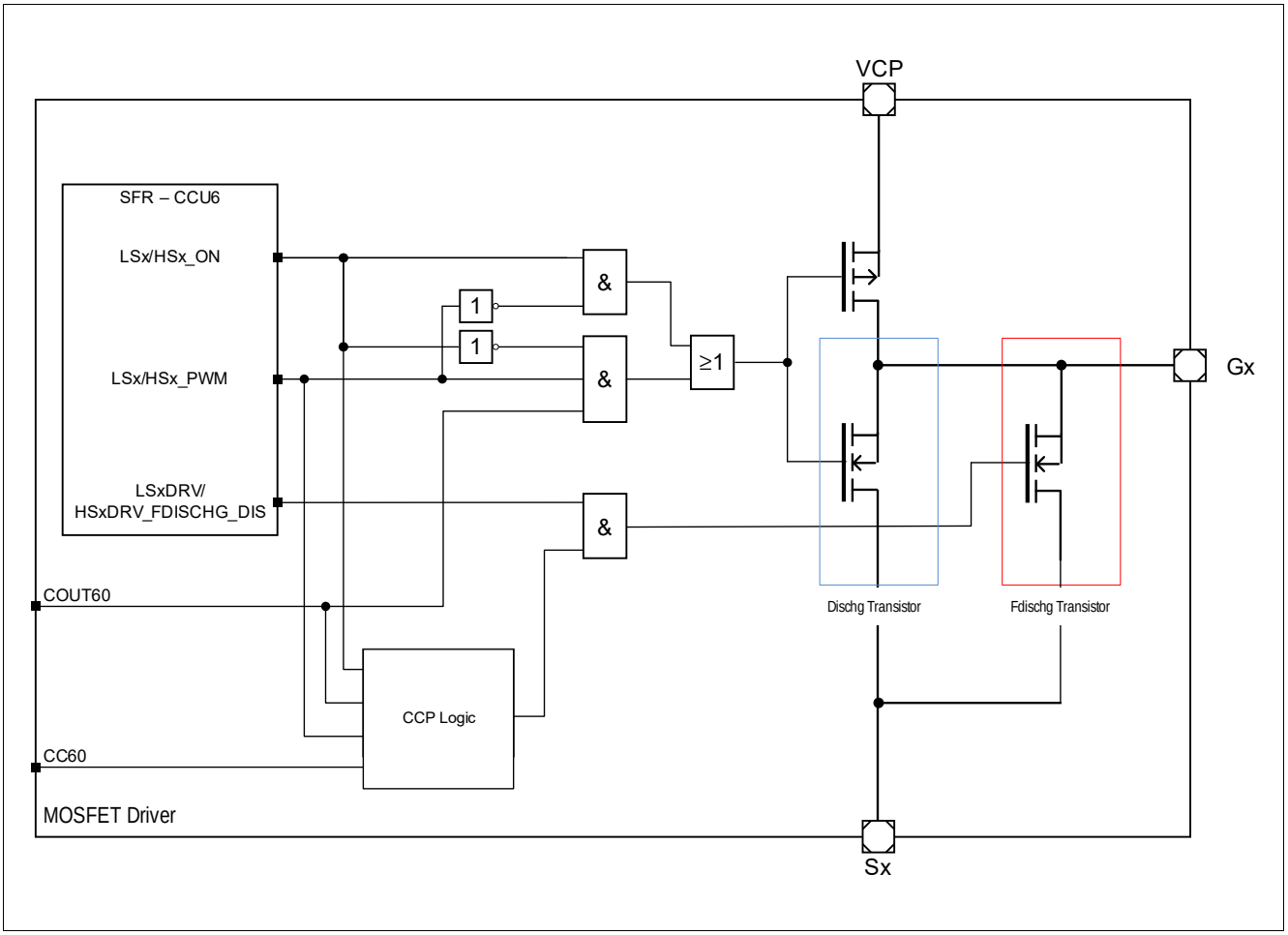

Figure 13 Implementation of Fast Discharge Feature

After the cross-conduction protection phase, the parallel transistor starts to increase the discharge current. This effect can be seen on the discharge slope (**Figure 14**), which accelerates in the second phase.

Fast Discharge Functionality

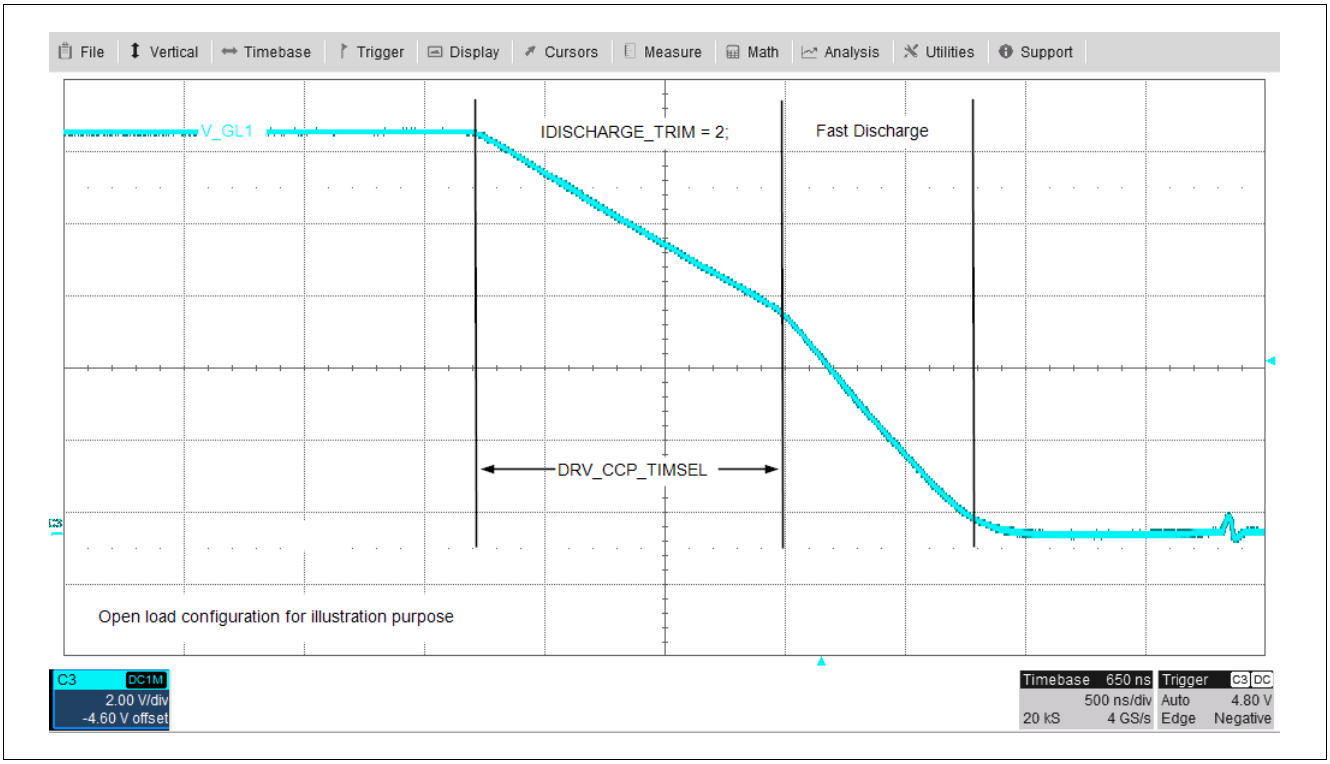

Figure 14 Discharge Slope

8 Switch-On / Off Delay Time Measurement

The TLE987x/TLE986x provides a hardware feature to measure the switch-on/switch-off delay of the system consisting of:

- Driver
- External MOSFET
- External components needed for driver and MOSFET operation

According to the value measured, the sequencer setting can be adapted to keep the desired switching time. The figure below shows the working principle of this delay measurement for the switch-on case.

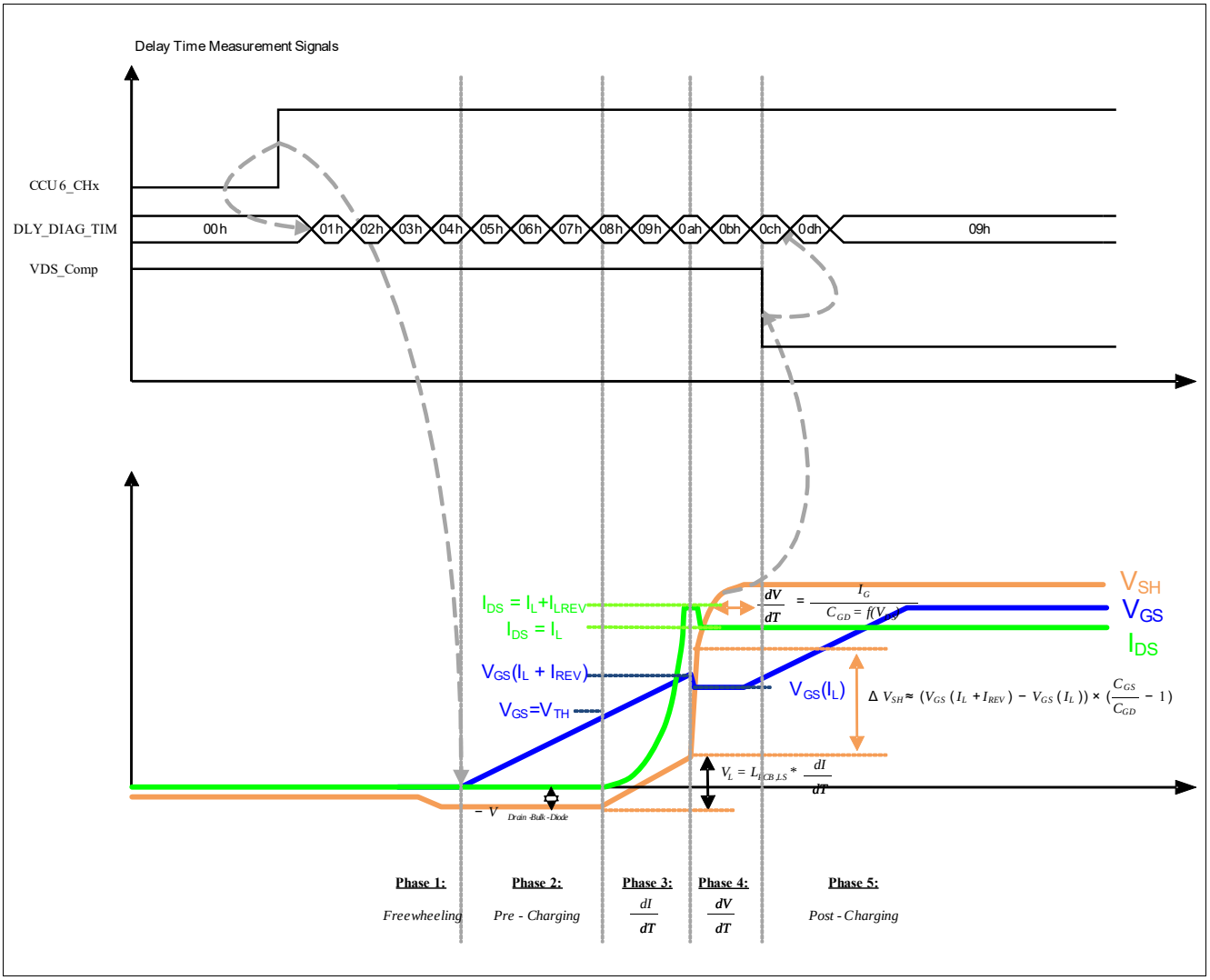

Figure 15 Principle of Delay Time Measurement in TLE986x/TLE987x

- CCU6_CHx is the control signal provided by the CCU6 to control the driver. The driver is switched on by CCU6_CHx (signal changes from low to high).
- DLY_DIAG_TIM is the delay timer used for the delay measurement. It is started by the rising edge of the CCU6 signal CCU6_CHx and stopped by the falling edge of the drain source comparator.
- VDS_Comp is the output of the drain source comparator indicating the end of the measurement to the timer.

The switch-off case looks like this:

Switch-On / Off Delay Time Measurement

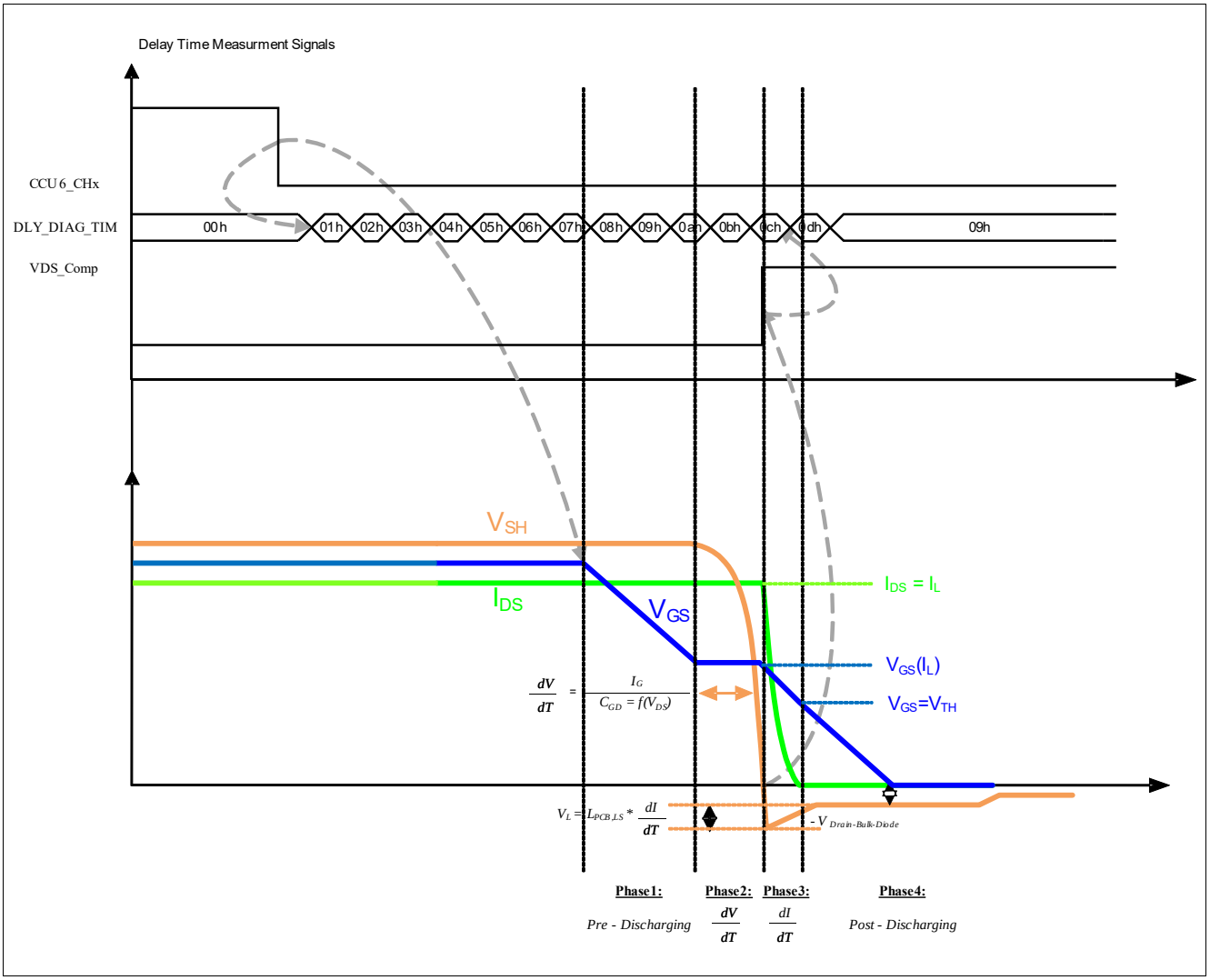

Figure 16 Principle of Delay Time Measurement in TLE986x/TLE987x

- CCU6_CHx is the control signal provided by the CCU6 to control the driver. The driver is switched off by CCU6_CHx (signal changes from high to low).
- DLY_DIAG_TIM is the delay timer used for the delay measurement. It is started by the falling edge of the CCU6 signal CCU6_CHx and stopped by the rising edge of the drain source comparator.
- VDS_Comp is the output of the drain source comparator indicating the end of the measurement to the timer.

9 Revision History

Revision	Date	Changes
1.0	2018-12-13	Initial creation.

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