Zynq-7000 All Programmable SoCs
Product Tables and Product Selection Guide

ZYNQ

XILINX
ALL PROGRAMMABLE™

Zynq®-7000 All Programmable SoCs

		Low-End Portfolio			Mid-Range Devices			
	Device Name	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™						
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor						
	Maximum Frequency	866MHz			Up to 1GHz(1)			
	L1 Cache	32KB Instruction, 32KB Data per processor						
	L2 Cache	512KB						
	On-Chip Memory	256KB						
	External Memory Support(2)	DDR3, DDR3L, DDR2, LPDDR2						
	External Static Memory Support(2)	2x Quad-SPI, NAND, NOR						
	DMA Channels	8 (4 dedicated to Programmable Logic)						
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
	Peripherals w/ built-in DMA(2)	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO						
	Security(3)	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot						
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts						
Programmable Logic	7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Kintex®-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA
	Logic Cells (Approximate ASIC Gates(4))	28K (~430K)	74K (~1.1M)	85K (~1.3M)	125K (~1.9M)	275K (~4.1M)	350K (~5.2M)	444K (~6.6M)
	Look-Up Tables (LUTs)	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM (# 36Kb Blocks)	2.1Mb (60)	3.3Mb (95)	4.9Mb (140)	9.3Mb (265)	17.6Mb (500)	19.1Mb (545)	26.5Mb (755)
	Programmable DSP Slices (18x25 MACCs)	80	160	220	400	900	900	2,020
	Peak DSP Performance (Symmetric FIR)	100 GMACs	200 GMACS	276 GMACs	593 GMACs	1,334 GMACs	1,334 GMACs	2,622 GMACs
	PCI Express® (Root Complex or Endpoint)	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC(2)	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs						
	Security(3)	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration						

1. 1 GHz processor frequency is available only for -3 speed grades for devices in flip-chip packages. Please see the data sheet for more details.
2. Z-7010 in CLG225 has restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to the Technical Reference Manual for more details.
3. Security block is shared by the Processing System and the Programmable Logic.
4. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.

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HR I/O, PS I/O, and Transceivers (GTP or GTX)

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	Part Number	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Unique Footprint	PCB Footprint Dimensions (mm) [1]	HR I/O, PS I/O[2], GTP Transceivers			HR I/O, HP I/O, PS I/O[2], GTX Transceivers			
CLG225	13x13	54[3], 86, 0						
CLG400	17x17	100, 128, 0		128, 128, 0				
CLG484	19x19			200, 128, 0				
CLG485[4]	19x19		150, 128, 4					
SBG485 / SBV485[4]	19x19				50[3], 100, 128, 4			
FBG484 / FBV484	23x23				100, 63, 128, 4			
FBG676 / FBV676[1]	27x27				100, 150, 128, 4	100, 150, 128, 8	100, 150, 128, 8	
FFG676 / FFV676[1]	27x27				100, 150, 128, 4	100, 150, 128, 8	100, 150, 128, 8	
FFG900 / FFV900	31x31					212, 150, 128, 16	212, 150, 128, 16	212, 150, 128, 16
FFG1156 / FFV1156	35x35							250, 150, 128, 16

1. Devices in the same package are footprint compatible. FBG676 / FBV676 and FFG676 / FFV676 are also footprint compatible.
2. PS I/O count does not include dedicated DDR calibration pins.
3. Static memory interface combined with the usage of many peripherals could require more than 50 I/Os. In that case, the designer can use the Programmable Logic SelectIO interface.
4. CLG485 and SBG485 / SBV485 are pin-to-pin compatible. See product data sheets and user guides for more details.
   See DS190, *Zynq-7000 All Programmable SoC Overview* for package details.

Zynq®-7000 AP SoC Ordering Information

XC	7	Z	###	-1	FF	V	###	C
Xilinx Commercial	Series	Zynq	Value Index	Speed Grade -1: Slowest -L1: Low Power -2: Mid -L2: Low Power -3: Fastest	CL: Wire-bond Molded w/ 0.8mm Ball Pitch SB: Flip-chip Lidless w/ 0.8mm Ball Pitch FF: Flip-chip Lidded w/ 1.0mm Ball Pitch FB: Flip-chip Lidless w/ 1.0mm Ball Pitch	V: RoHS 6/6 G (CLG) = RoHS 6/6 G (SBG, FBG, FFG) = RoHS 6/6 with exemption 15	Package Pin Count	Temperature Grade (C, E, I)

C = Commercial (Tj = 0°C to +85°C)
E = Extended (Tj = 0°C to +100°C)
I = Industrial (Tj = –40°C to +100°C)

Refer to DS190, Zynq-7000 All Programmable SoC Overview for additional information.