



life.augmented

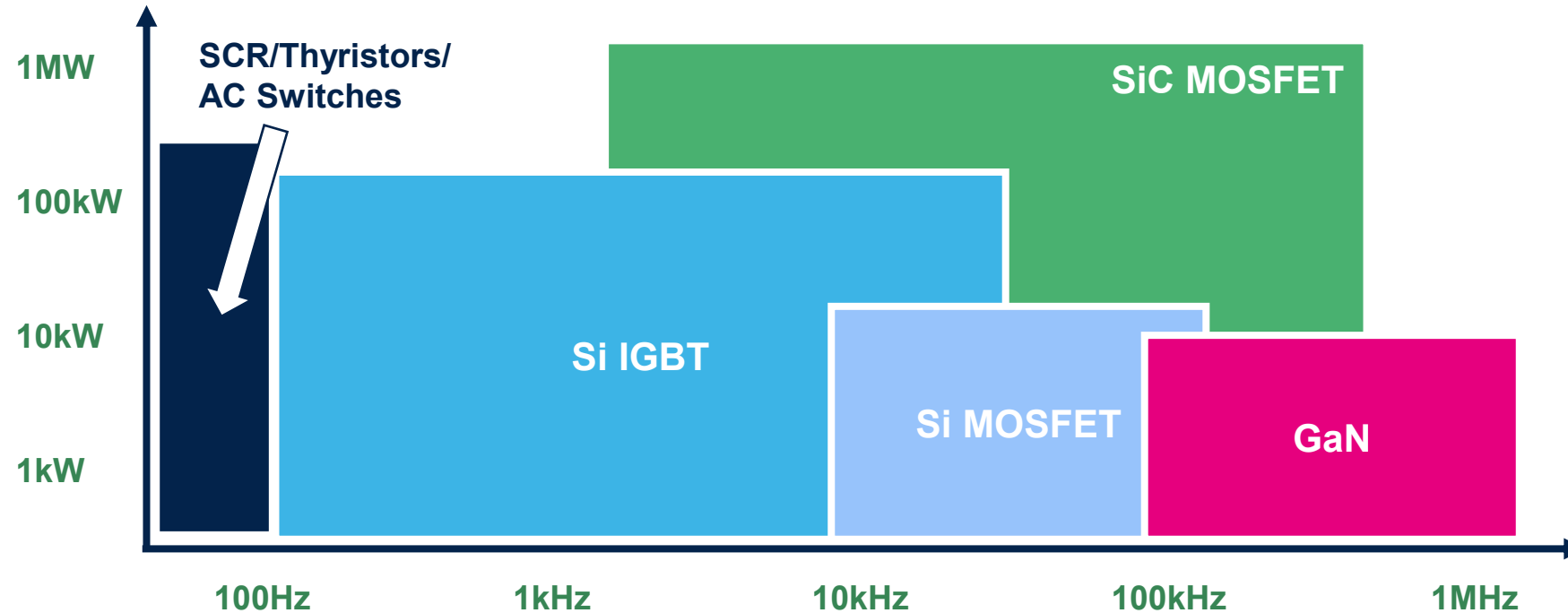
# SiC - Highlighting the newest generations and optimized packages

Salvatore La Mantia  
STMicroelectronics

AVNET Silica Tech Day Breda  
December 11th, 2025 - Breda



# Silicon and wide-bandgap power technology positioning

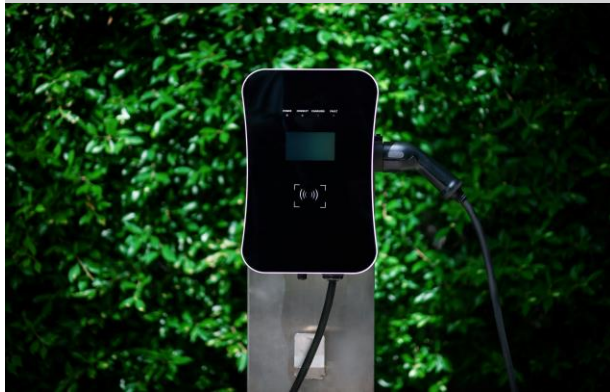


Our „all you can eat“ menu!

# Power & Discrete in industrial

Allowing more compact systems and reducing total cost of ownership

## Charging stations



Faster charging

## Datacenters, UPS, AI servers



Higher power density

## Renewable energy, BESS



Smaller and lighter systems

## Industrial drives



Lower total cost of ownership

SiC MOSFET

Silicon MOSFET

IGBT

Discrete & Filter

Power modules  
& IPM

Power GaN

# Investing in vertically integrated SiC manufacturing

## Leading market position

### In volume production with SiC devices since 2007

- More than 500 million devices shipped to automotive and industrial customers
- Qualification of 200 mm wafer fabrication in 2023
- A vertical integration strategy

#### Substrate



#### Front-end



#### Back-end



## Future expansions

### Catania

ST silicon carbide Campus  
World's first fully integrated  
silicon carbide facility



Production to start in **2026** and **full build-out in 2033**

### Chongqing

ST and Sanan Joint Venture for SiC  
device manufacturing in China



Production to start in **Q4 2025** and **full buildout in 2028**

# STPOWER SiC MOSFET

## Latest Technology families overview

The best high voltage and high frequency switch for high density applications



### Gen3

**650V, 750V, 900V, 1200V**

Extensive product range, available in multiple industry standard packages: suitable for high frequency applications & AG qualified

### Gen4\*

**750V, 1200V**

Extremely low RDS(on). Up to -15% RDS(on) x area improvement vs Gen3. Complementing Gen3 in the low ohmic range

### SiC VHV

**1700V / >2kV\*\***

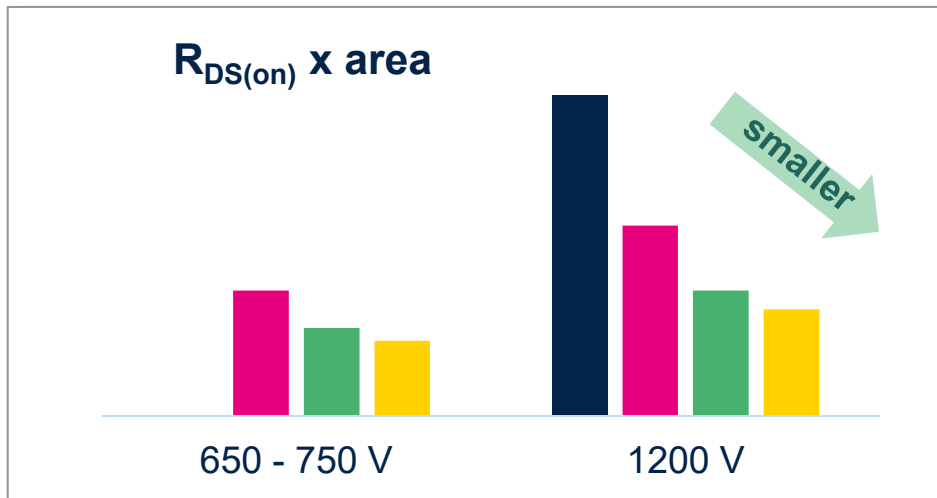
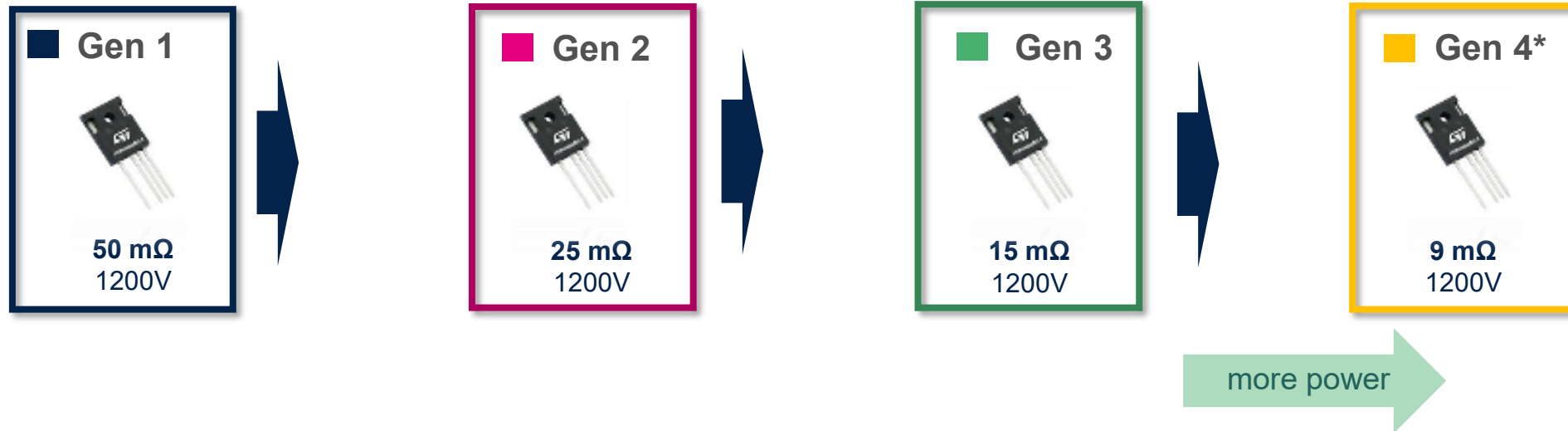
**Very High Voltage SiC** extend the advantages of SiC technology to Higher voltage ranges

\* First discrete product release by 2026

\*\* >2kV in roadmap 27/28

# SiC MOSFET Advances in Technology

## Figure of Merits

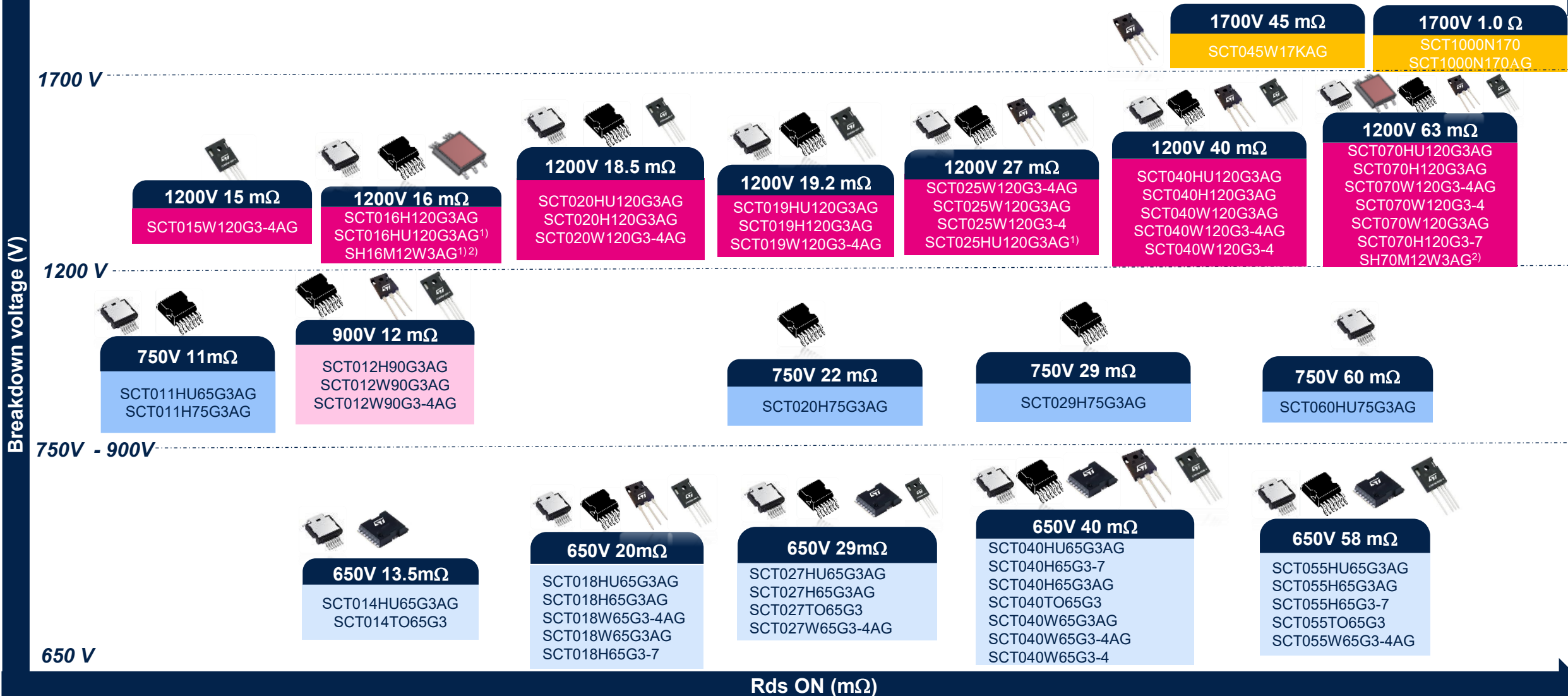


### improvement in MOSFET generations

- **Lower  $R_{on} \times \text{Area}$**  → lower  $R_{on}$  for a given chip size (or smaller chip size for a given  $R_{on}$ ), higher current capability, lower conduction Losses → means higher power achievable with the same form factor
- **Lower  $R_{on} \times Q_g$**  → lower switching losses, higher frequency (reduced board)

# SiC MOSFETs - Product Portfolio

All P/N in Mass Production

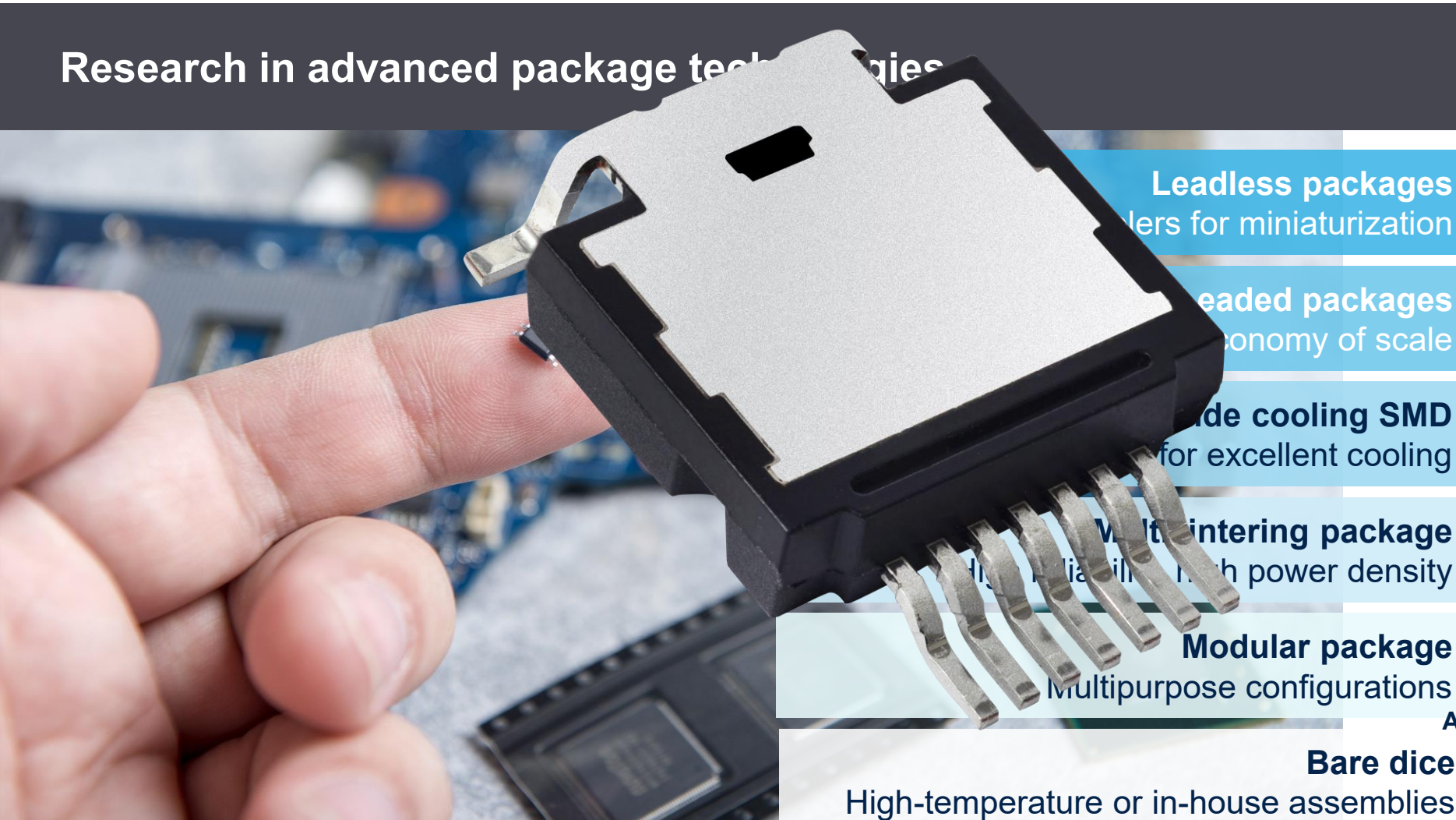


<sup>1)</sup> MP planned during 2026  
<sup>2)</sup> Half Bridge SiC MOS. MP 2026



# Advanced packaging

## Research in advanced package technologies



**Leadless packages**  
enables for miniaturization

**Leadless packages**  
economy of scale

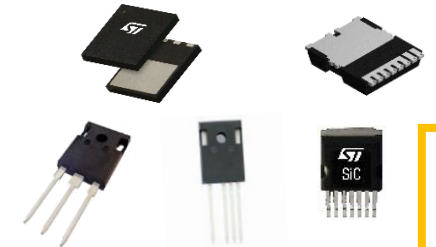
**Wide cooling SMD**  
for excellent cooling

**Multi-lead interlocking package**  
high reliability, high power density

**Modular package**  
Multipurpose configurations

**Bare dice**  
High-temperature or in-house assemblies

PowerFLAT 8x8 HV TO-LL



Q3'26

HiP247 HiP247-4 H2PAK-7



TO247-4 HC



HU3PAK\*



HU3PAK HC

TOLT



Q2'26



STPAK\*



Q4'26

ACEPACK\* SMIT

ACEPACK\* 1, 2 & 3



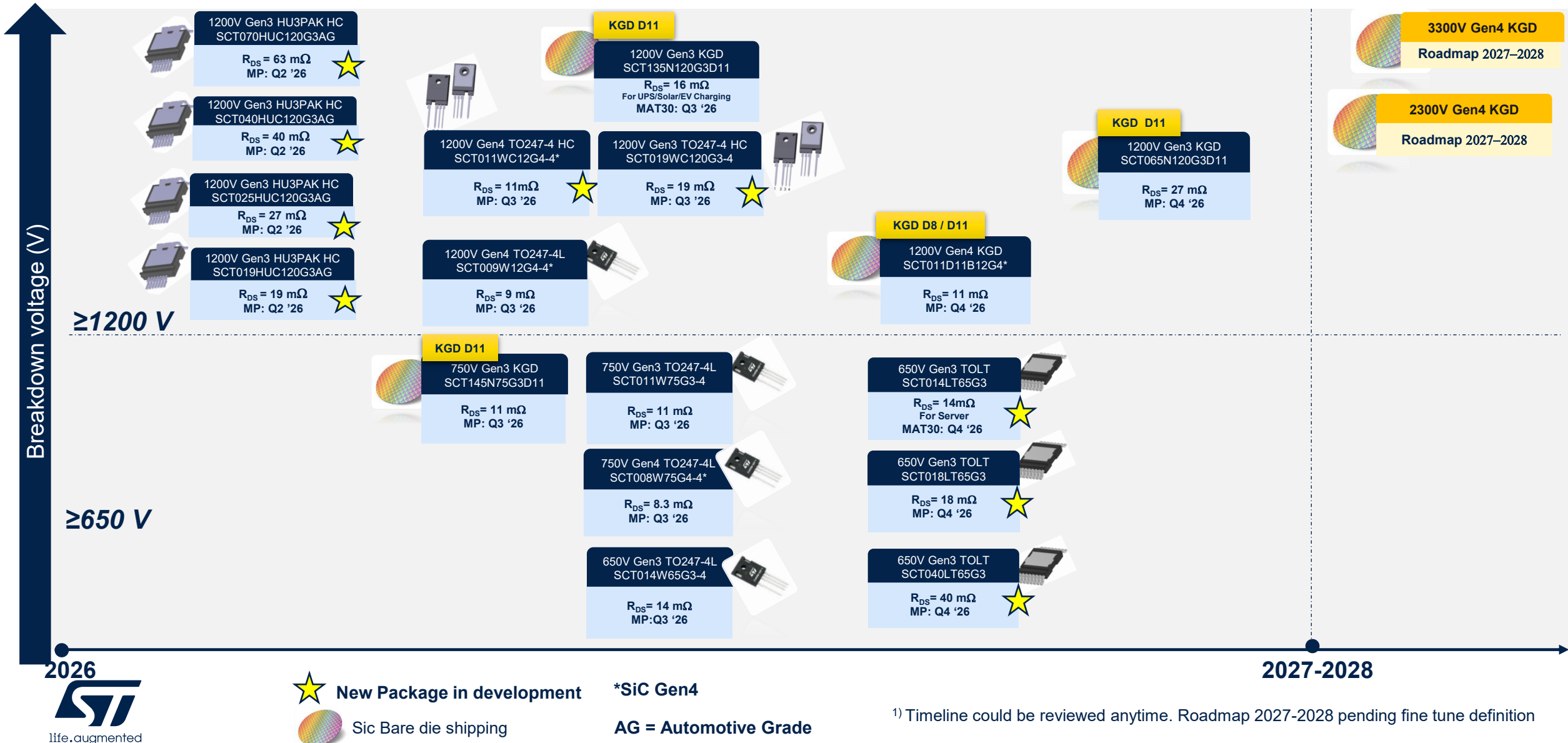
roadmap

Tested dice in T&R Wafer on Sticky foil



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# Industrial SiC MOSFET and Module roadmap product plan<sup>1)</sup>



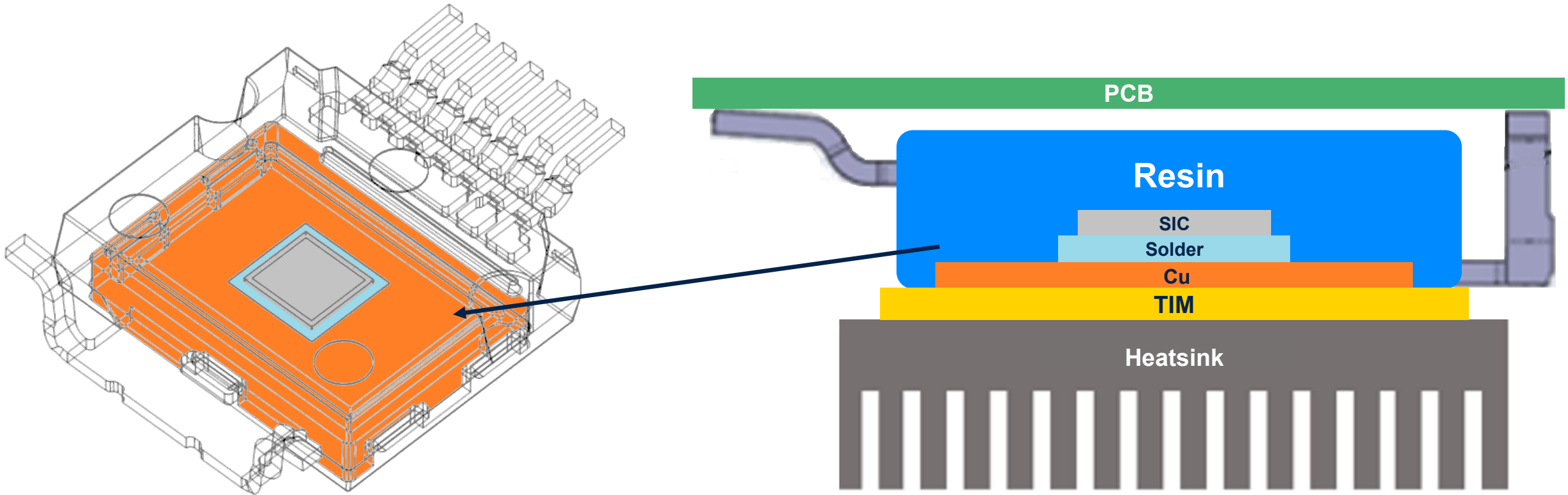


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# Top-Side-Cooled package HU3PAK

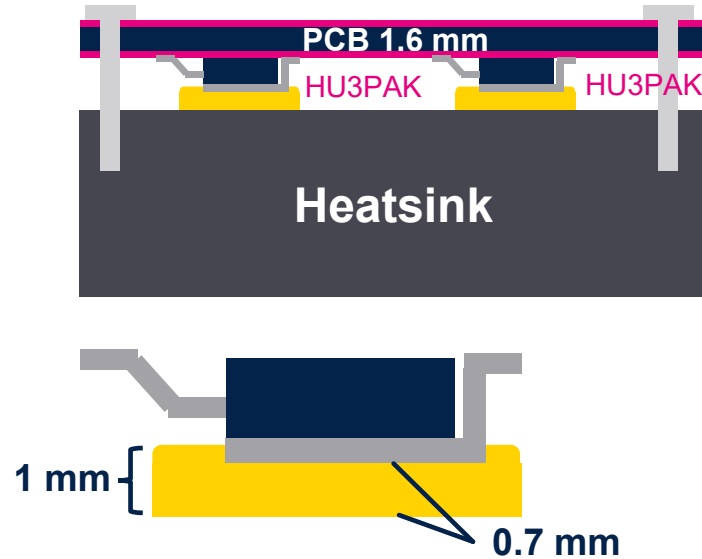


# Top-Side-Cooling HU3PAK Application Structure



**Top-Side-Cooling enables to  
dissipate heat directly to  
heatsink (through thin TIM layer)**

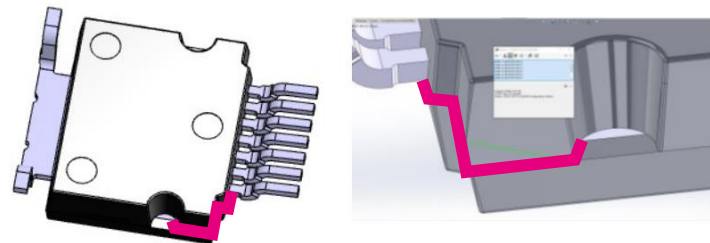
## Gap-Filler solution



- Designed to **fill space** between package and heatsink
- **Electrically isolated**
- Could be **Solid** (pads) or **Liquid** (one or two compound)



## Creepage is calculated on side



### Pads = Solid Gap-Filler

Adhesive soft pads could be compressed up to ~70% and still maintain isolation

### Liquid Gap-Filler

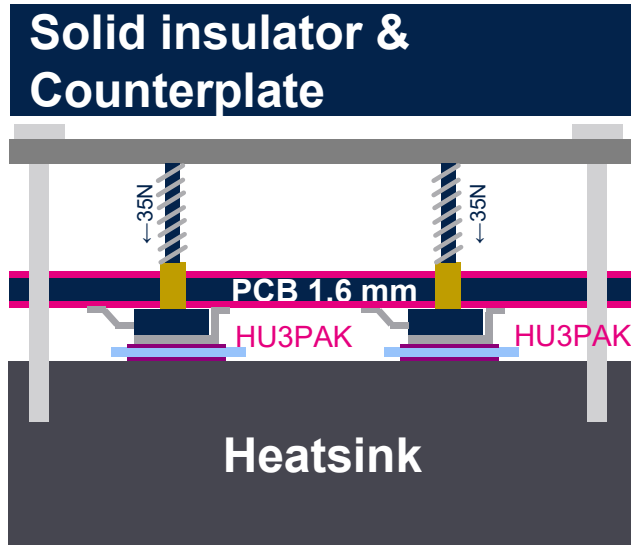
Usually two-compound mixture is easy to dispense. Could be either curing or non-curing

- **Curing**

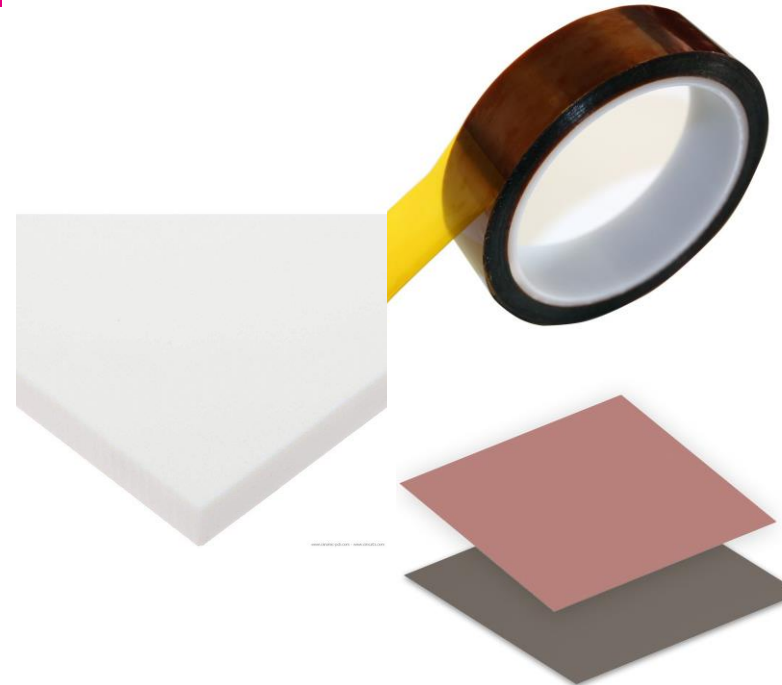
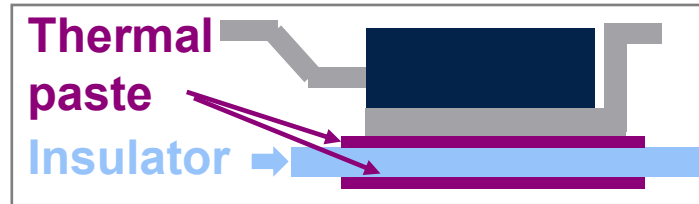
Hardens after dispense, acts as a glue keeping the packages in position

- **Non-curing**

One-part compound that allows further compression: behaves well under vibrations

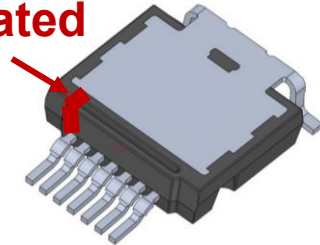


- **Counterplate** presses the package to the heatsink
- All **gaps** and tolerances are **covered** by the pressing force



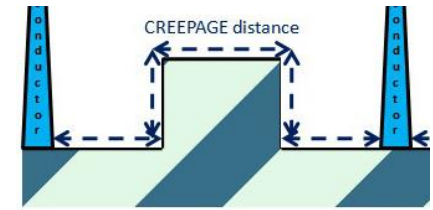
## Thermal paste

- Necessary for good thermal transfer, fills only surface
- Can suffer of **pump-out** effect
- Have **no guaranteed isolation**  
→ **creepage is calculated across the groove!**

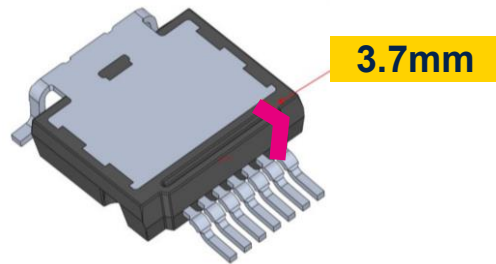
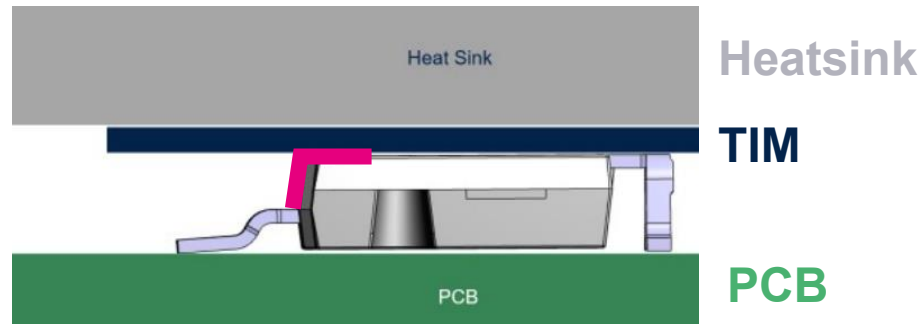


## Solid insulators

- **Electrical isolation**
- Can be hard (*ceramics*) or soft (Kapton / polyamide)

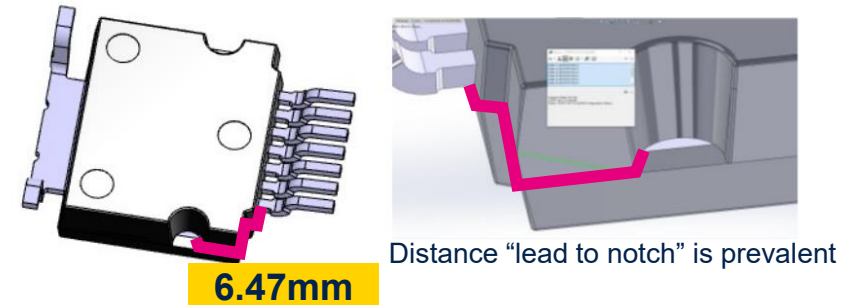
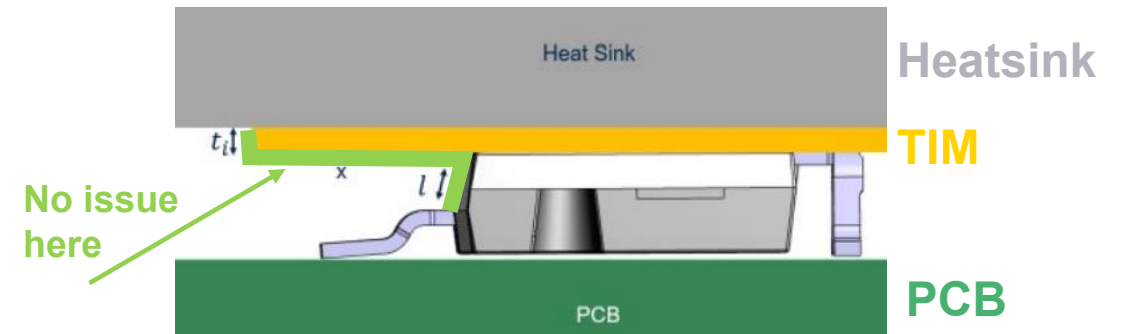


## Option 1: TIM - Solid Isolator Foil



Pollution degree	Material group	Max rms voltage
1	I & II	1070 V
2	II	515 V

## Option 2: TIM - Gap Filler



Pollution degree	Material group	Max rms voltage
1	I & II	1750 V
2	II	910 V

# Results of best TIM material measurements for HU3PAK

1) 0.32 K/W Gap-Filler pad – 0.7mm thickness



2) 0.33 K/W Liquid Gap-Filler – 0.7mm thickness



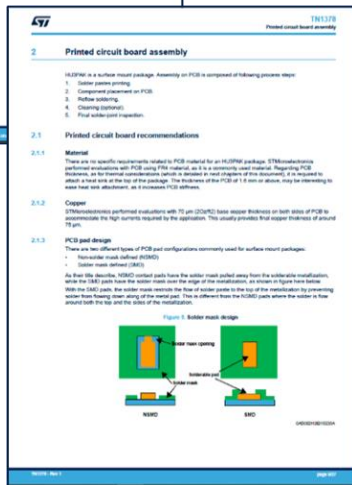
3) 0.35 K/W Al<sub>2</sub>O<sub>3</sub> ceramics + Thermal paste + Counterplate –  
1.0mm thickness





# Top-Side-Cooling - HU3PAK mounting instructions & thermal management ←TN1378

Title	Type	Icon
<a href="#">TN1378: HU3PAK package mounting and thermal behavior</a>	Technical Note	<a href="#">PDF</a>

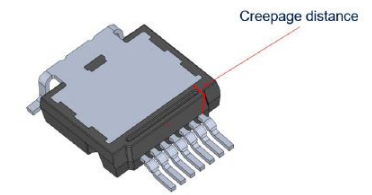
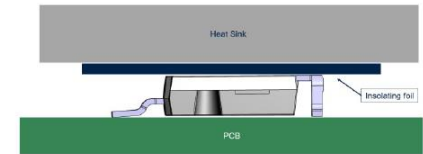


Top side cooling can best be mounted with soft gap filler or liquid gap filler for optimal performances

Gap filler comes with different thermal conductivity that play an important role on Rth and thermal management

Many thermal compounds are available on the market that may provide good results:

Figure 17. Creepage distance in HU3PAK on uncemented insulating foil

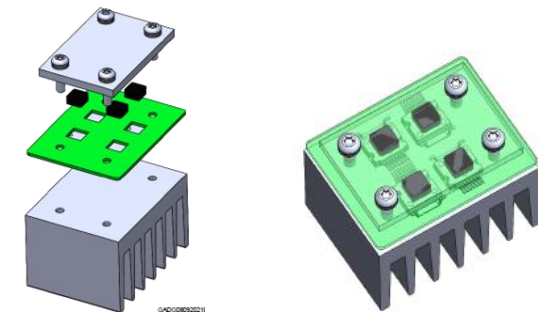


GAD0021120211341

Depending on the pollution degree and the material group of the resin, the maximum rms voltage that can be withstood by the package is defined in the table below:

Table 4. Maximum rms voltage capability with a creepage distance of 3.7 mm

Pollution degree	Material group	Max rms voltage
1	I and II	1070 V
2	II	515 V



Example of heat sink assembly with counter plate



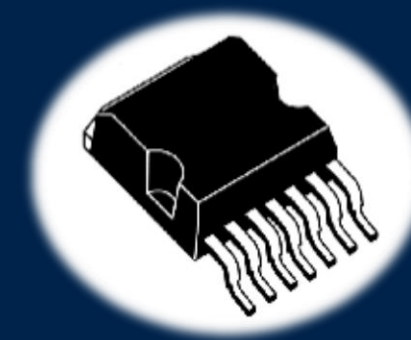
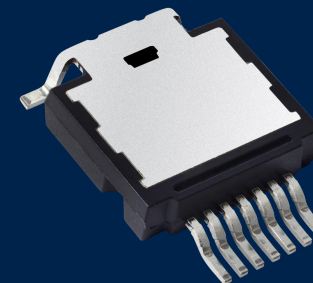
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**Top-Side-Cooling HU3PAK**

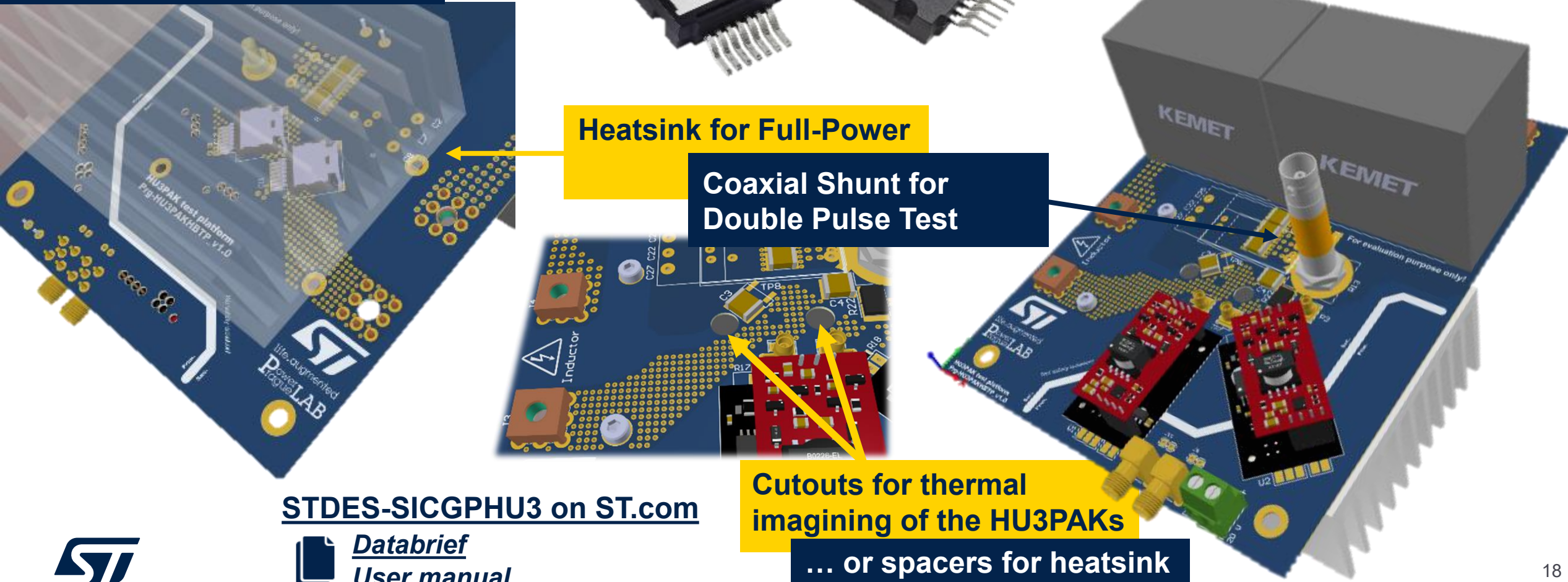
VS

**Bottom-Side-Cooling H2PAK-7**

*Study Case*



## Overview of platform used for testing



[STDES-SICGPHU3 on ST.com](https://www.st.com)



[Databrief](#)  
[User manual](#)



- Features**
- Gate Driver based on **STGAP3SXS**
  - **10A** driving capability
  - Active Miller Clamp
  - Isolation
  - Universal output connection

- Status LEDs
  - Secondary OK
  - Primary OK
  - Desaturation

**STL8N6F7**  
Miller Clamp MOSFET

Isolation barrier

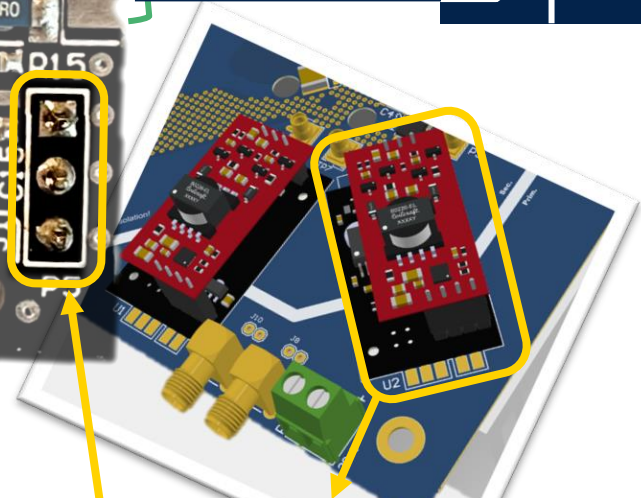
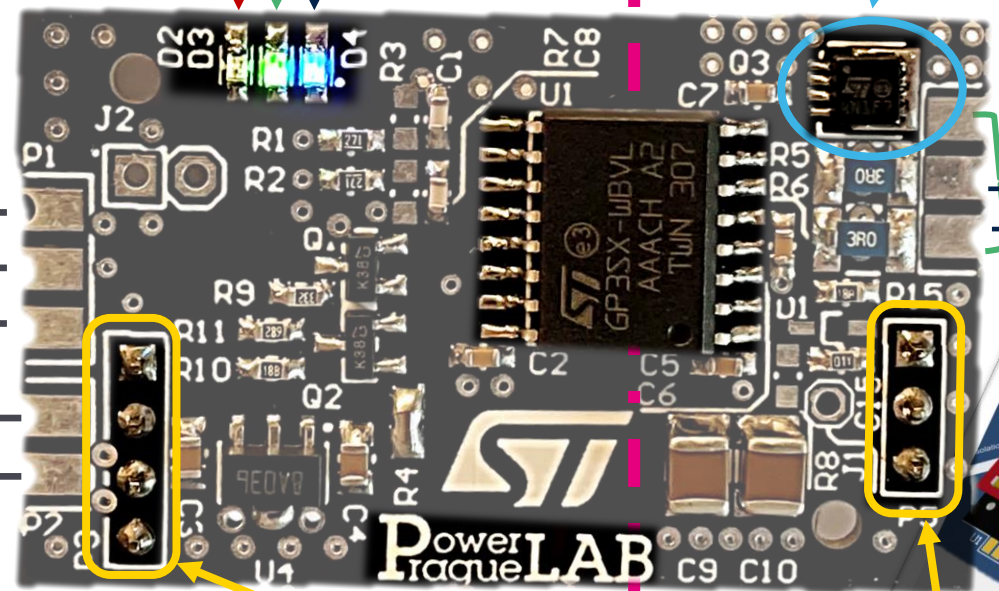
Kelvin Source

Gate signal



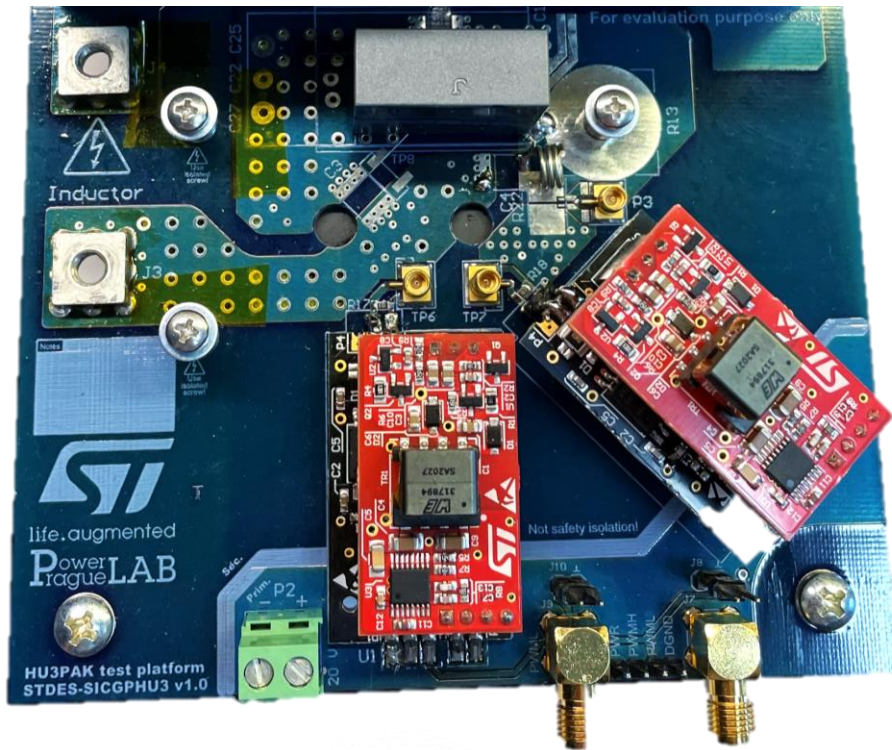
**24V Supply (20-26V)**

- GND
- IN+
- IN-
- VCC
- GND



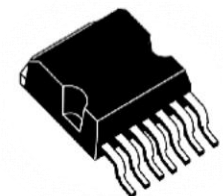
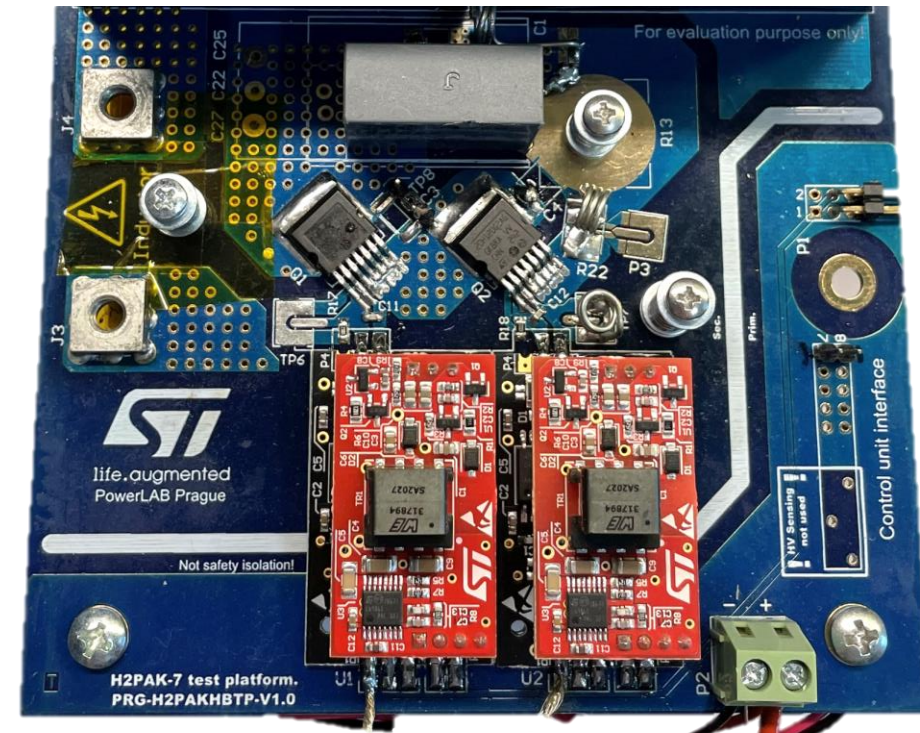
**Headers for isolated DC/DC**

## HU3PAK test board



Thermal testing:  
Power dissipation on body diodes

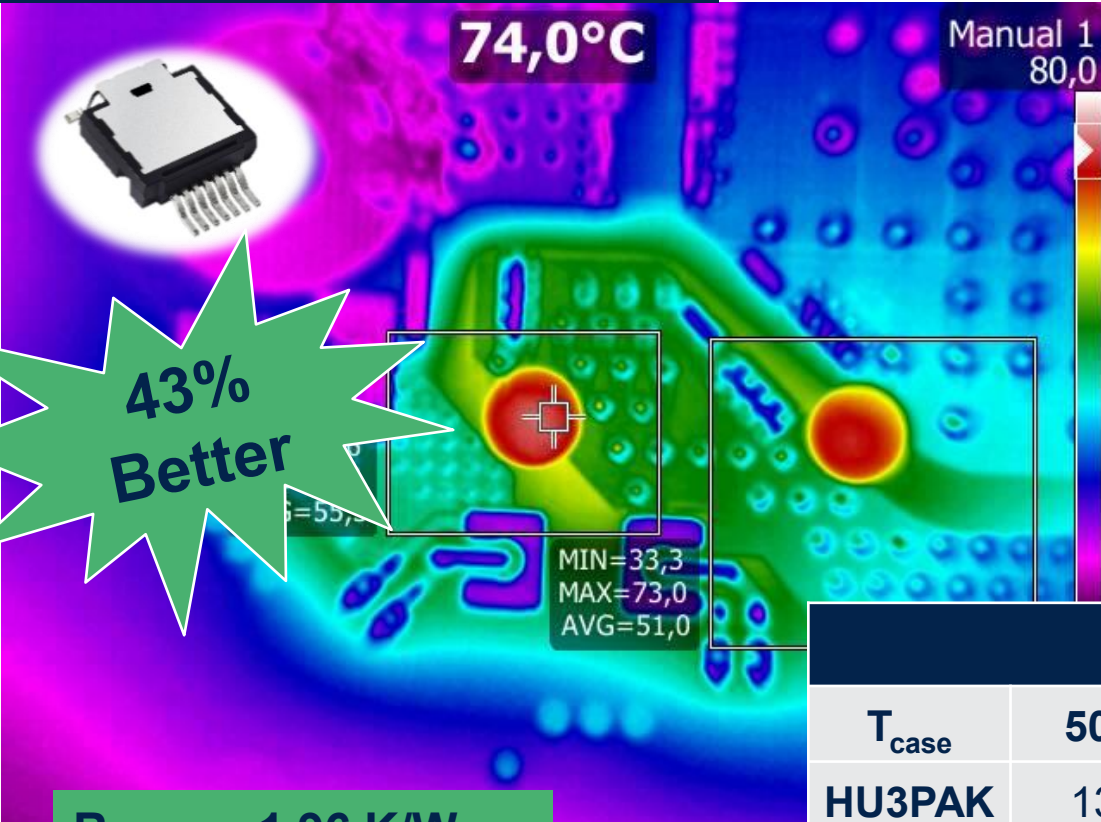
## H2PAK-7 test board



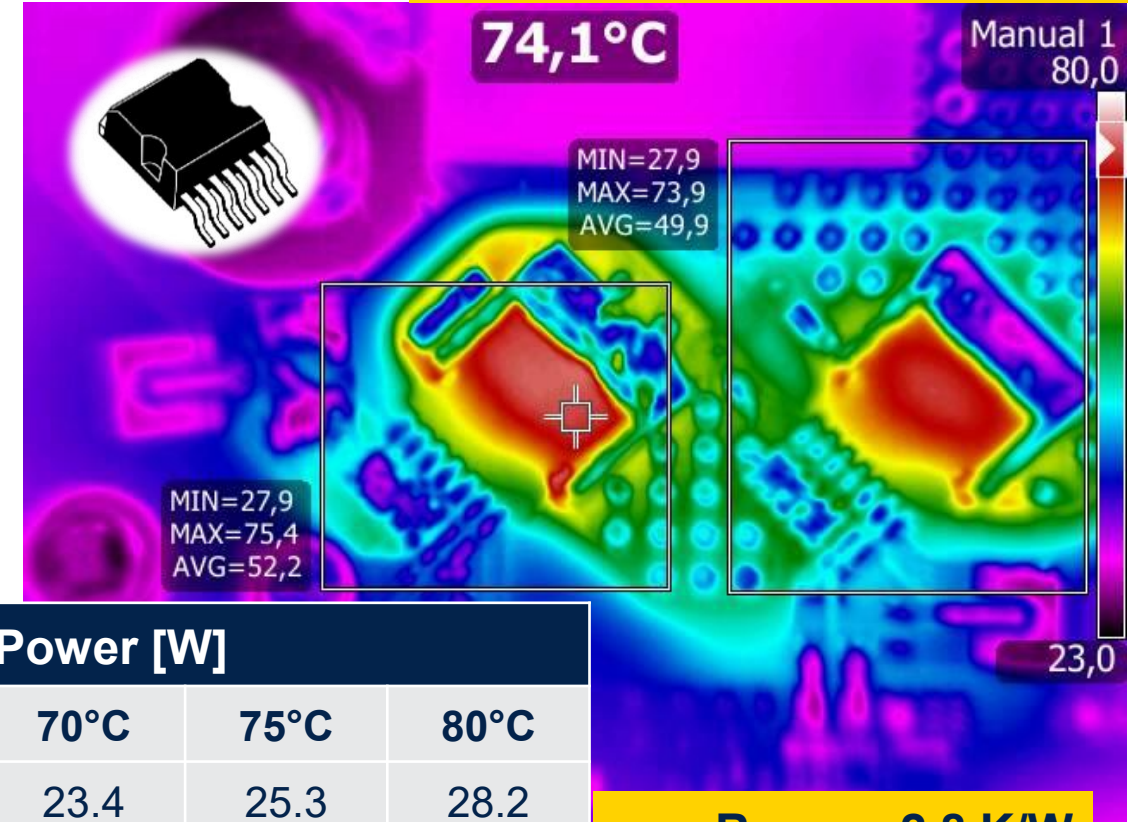


# Power dissipation results

**HU3PAK test board**



**H2PAK test board**



$R_{th-total} \sim 1.96 \text{ K/W}$

$R_{th-total} \sim 2.8 \text{ K/W}$

Dissipated Power [W]					
$T_{case}$	50°C	60°C	70°C	75°C	80°C
HU3PAK	13.1	18.4	23.4	25.3	28.2
H2PAK	9.0	12.6	16.3	18.1	19.9

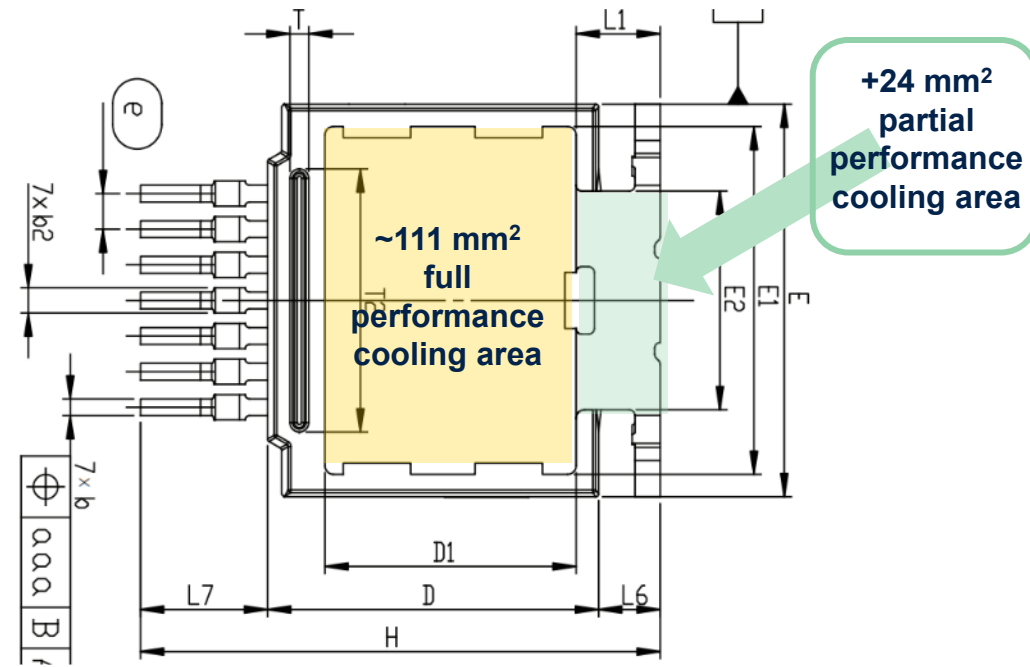
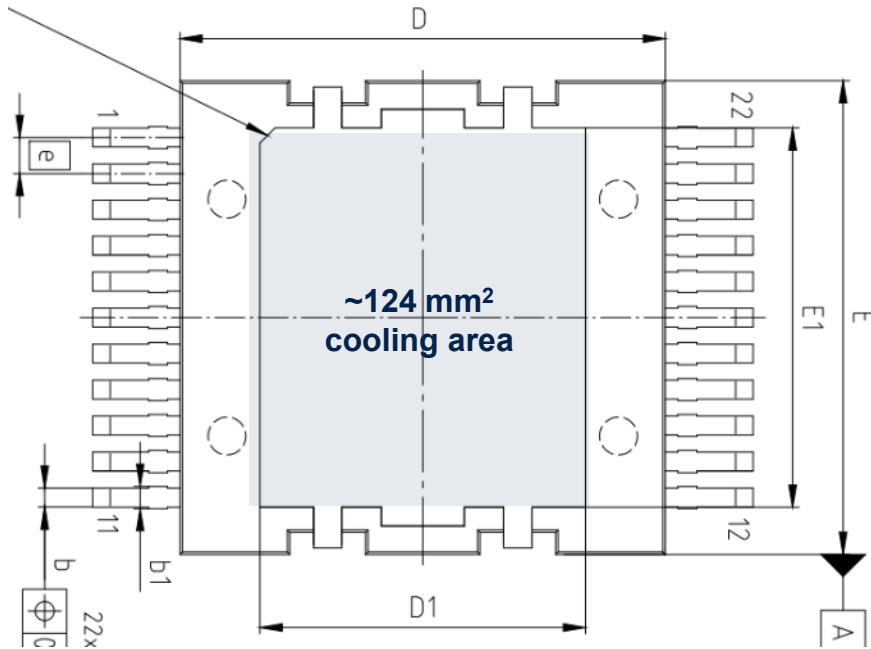
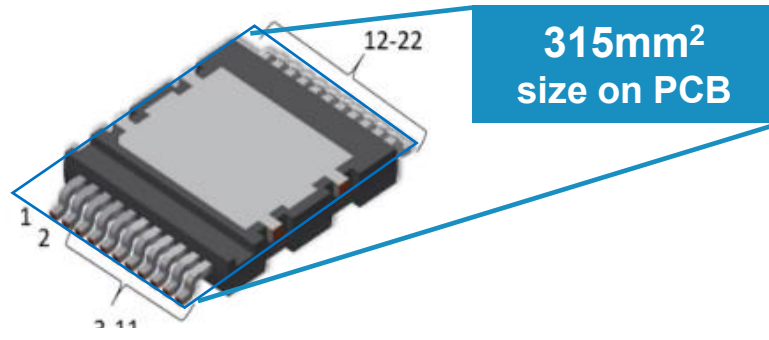
$T_{amb} = 24.5^\circ\text{C}$



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# Different versions and aspects of Top-Side-Cooling HU3PAK vs QDPAK

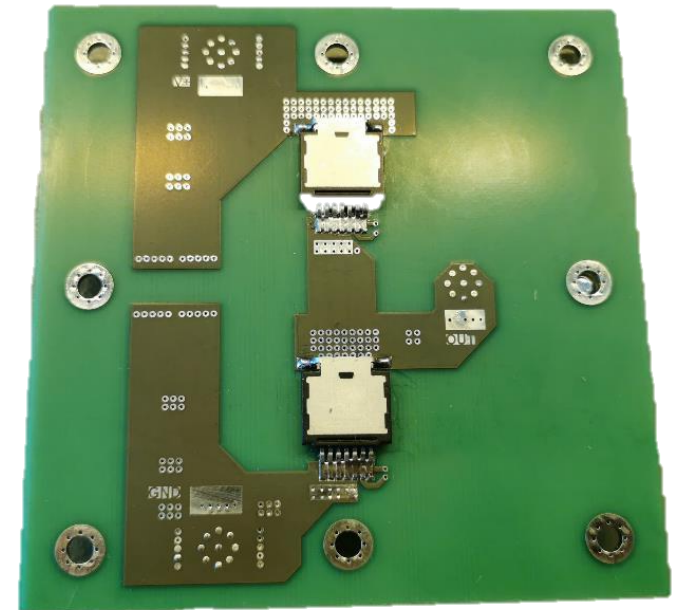
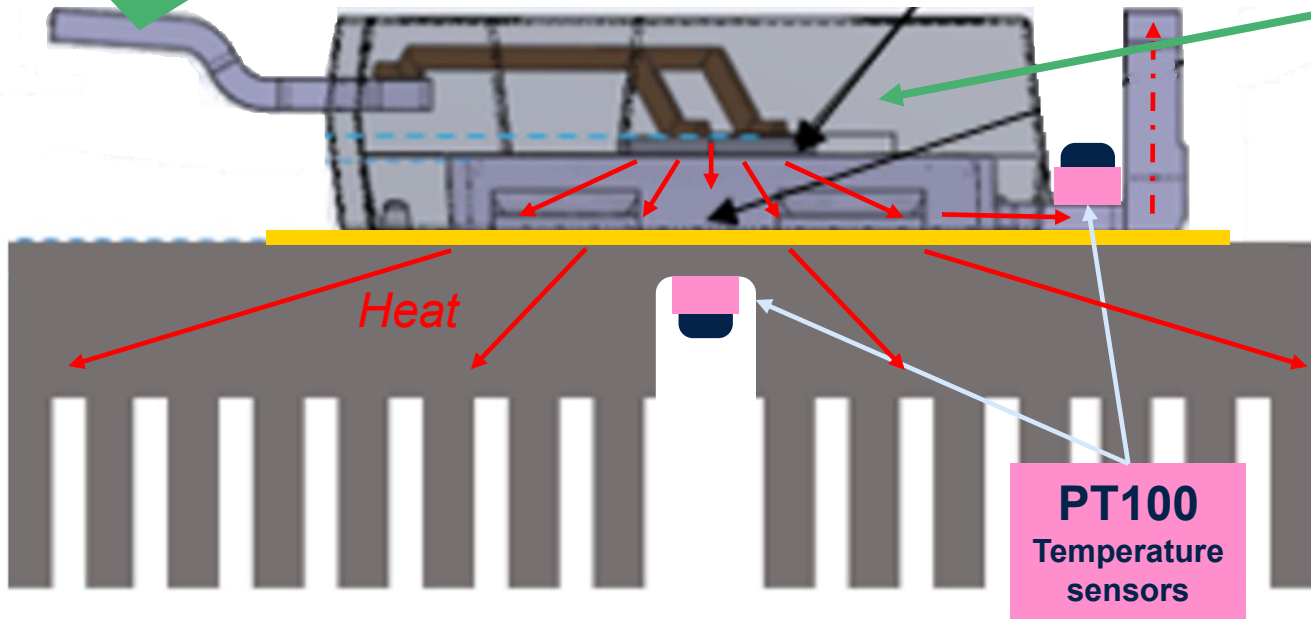
# Top Side Cooling Cooling pad size and PCB size



**Conclusion:**  
Cooling area matters – power dissipation per area is better for HU3PAK

## $R_{th}$ Case-to-Heatsink

Lab measurement



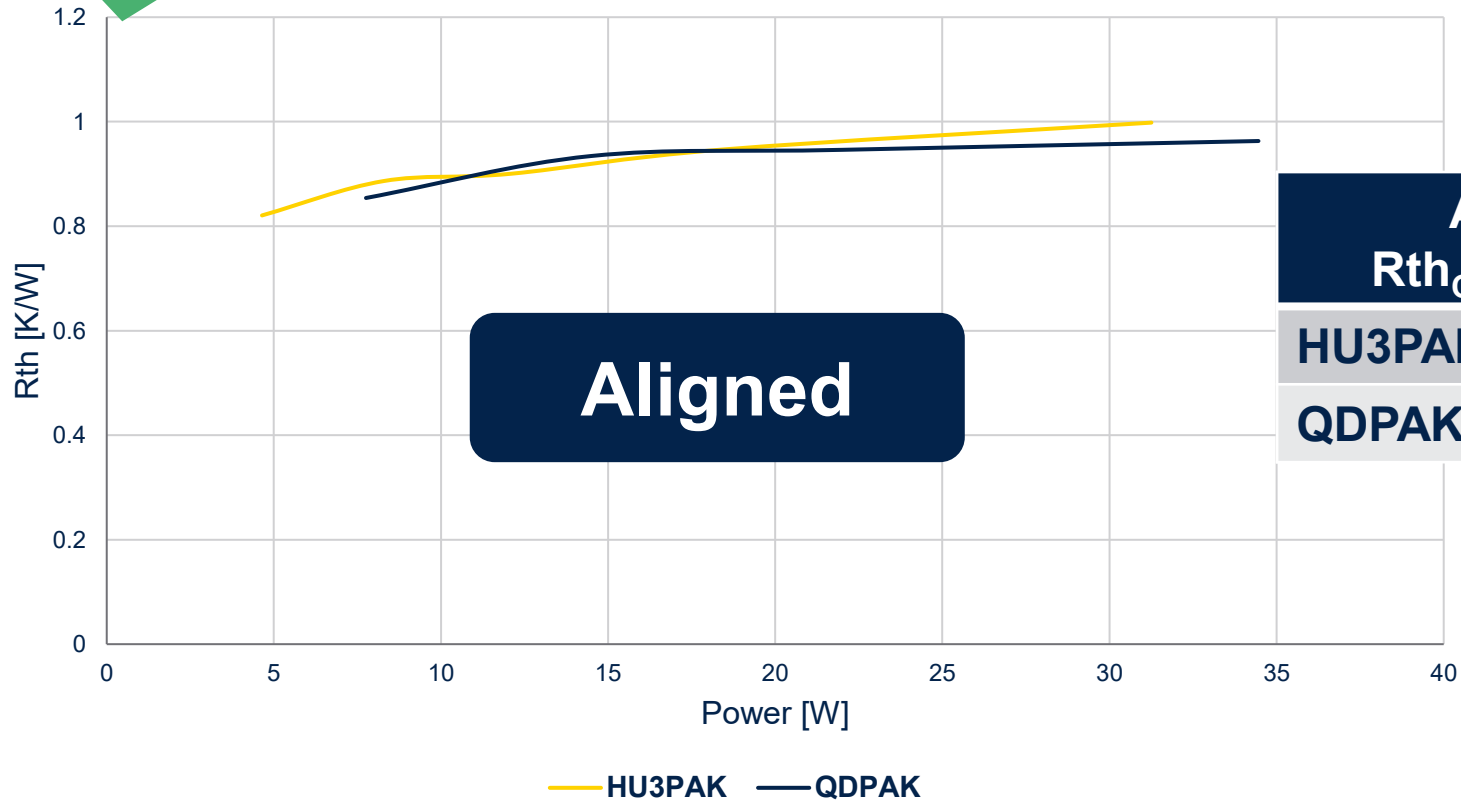
$$R_{th} = \frac{\Delta T}{Q} [K/W]$$

## $R_{th}$ Case-to-Heatsink

Lab measurement

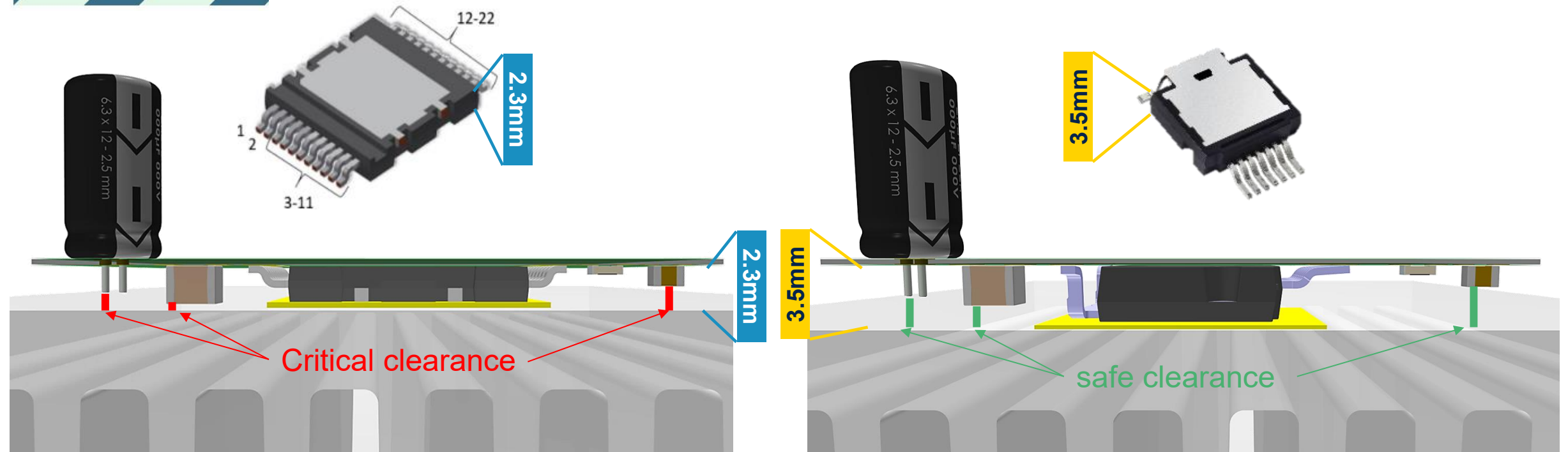
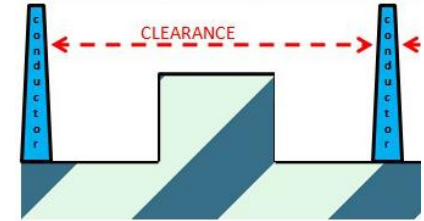
Cooling capability of smaller **HU3PAK** is same as bigger QDPAK

Rth Measurement



	Average $R_{th}$ Case-to-Heatsink	Size mm2	Cooling mm2
HU3PAK	0.91 K/W	260	111+24
QDPAK	0.92 K/W	315	124

## Top Side Cooling Clearance - *Package thickness*



Conclusion:  
Some applications benefit from low thickness. Some require higher thickness

### *Top Side Cooling Package: HU3PAK, not a Package Option but a System Solution*

#### 1 Improved Thermal Performances

- ✓ *Avoiding thermal conduction through PCB*
- ✓ *Optimizing heatsink form factor and efficiency*



Top View (Heatsink Side)

#### 2 Higher Efficiency enabler

- ✓ *A better  $T_j$  management permits to rise up system efficiency*

#### 3 Suitable for All Technological Platforms

- ✓ *Full Product Ecosystem with Silicon and SiC main power devices for all the topologies of the Power Converter from input diode bridge till the most common output stages*

#### 4 BOM Cost Reduction

- ✓ *Adopting a planar and simple heatsink*
- ✓ *Using a simple FR-4 PCB instead of an expensive IMS one*

# Power Switch Parallelization

Why we talk about parallelization?



# SiC MOSFET - packaging solutions for industrial

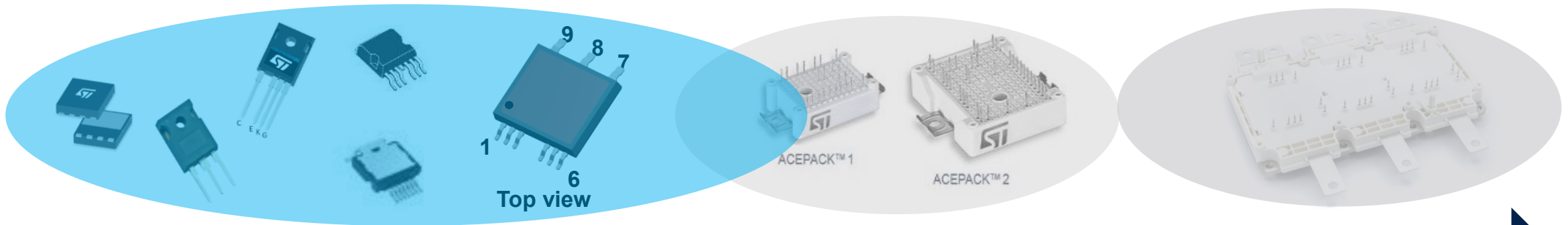
## Power range positioning

Industry standard discrete packages combine performance, design flexibility, pin-out compatibility

SiC discretes

Baseplate-less modules

Baseplate modules



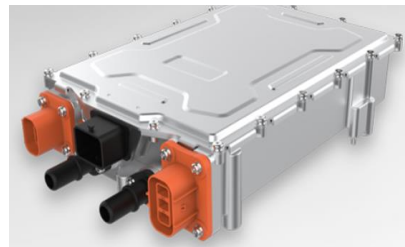
50kW

100kW

300kW



SMPS and UPS



On-board charger  
(Automotive or industrial)



EV charging  
(uni or bi-directional)



Storage systems

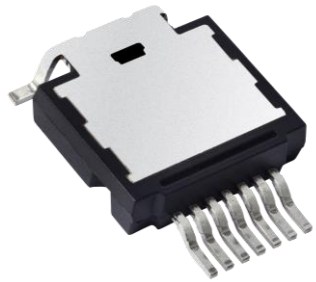


Solar

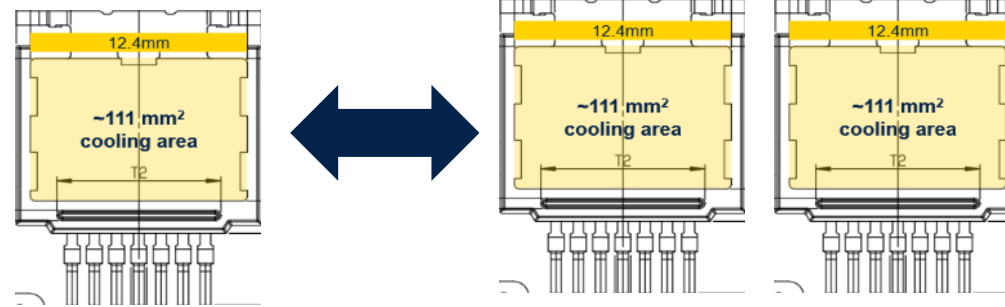


# Benefits of parallelization

## 1. Thermal



HU3PAK

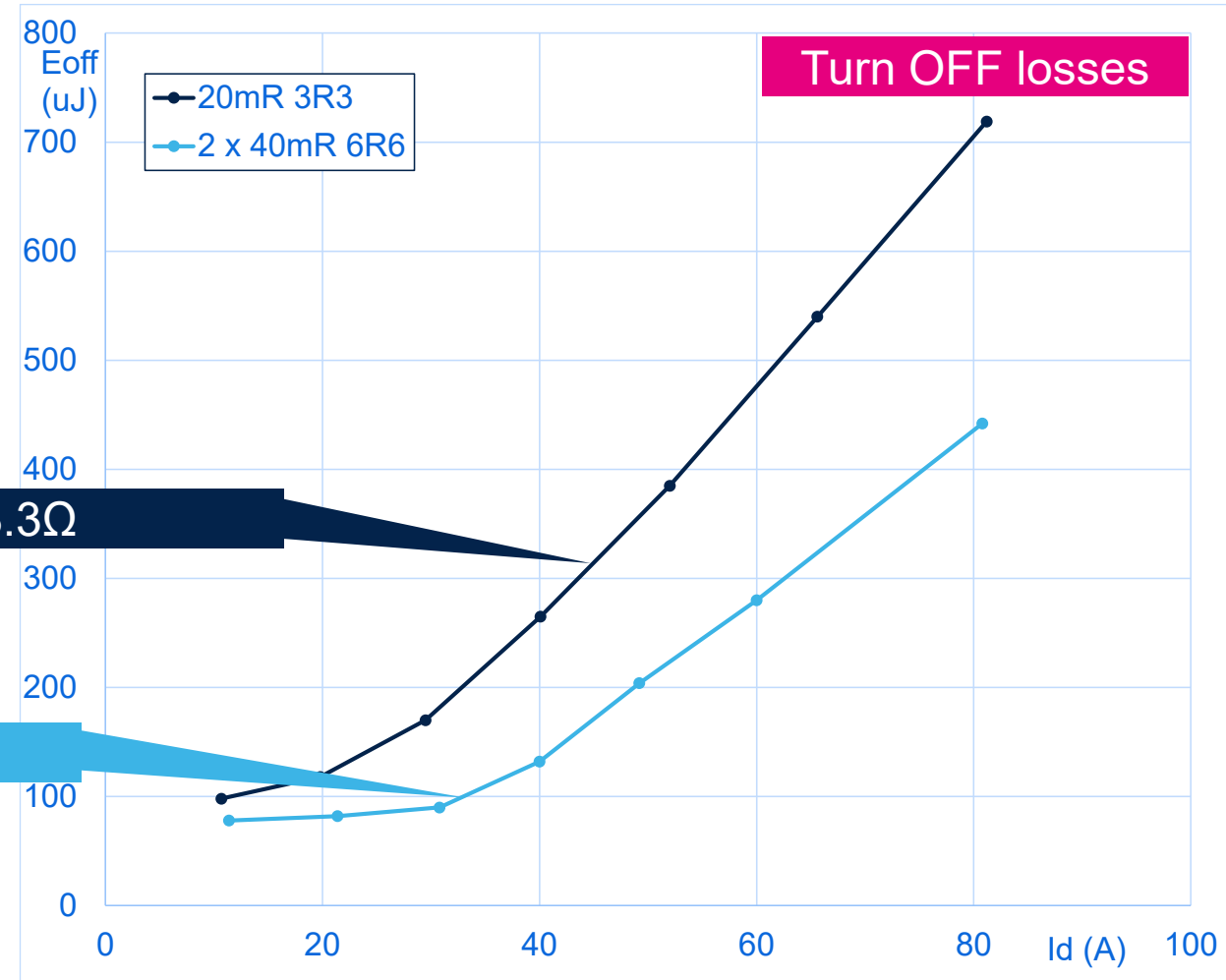
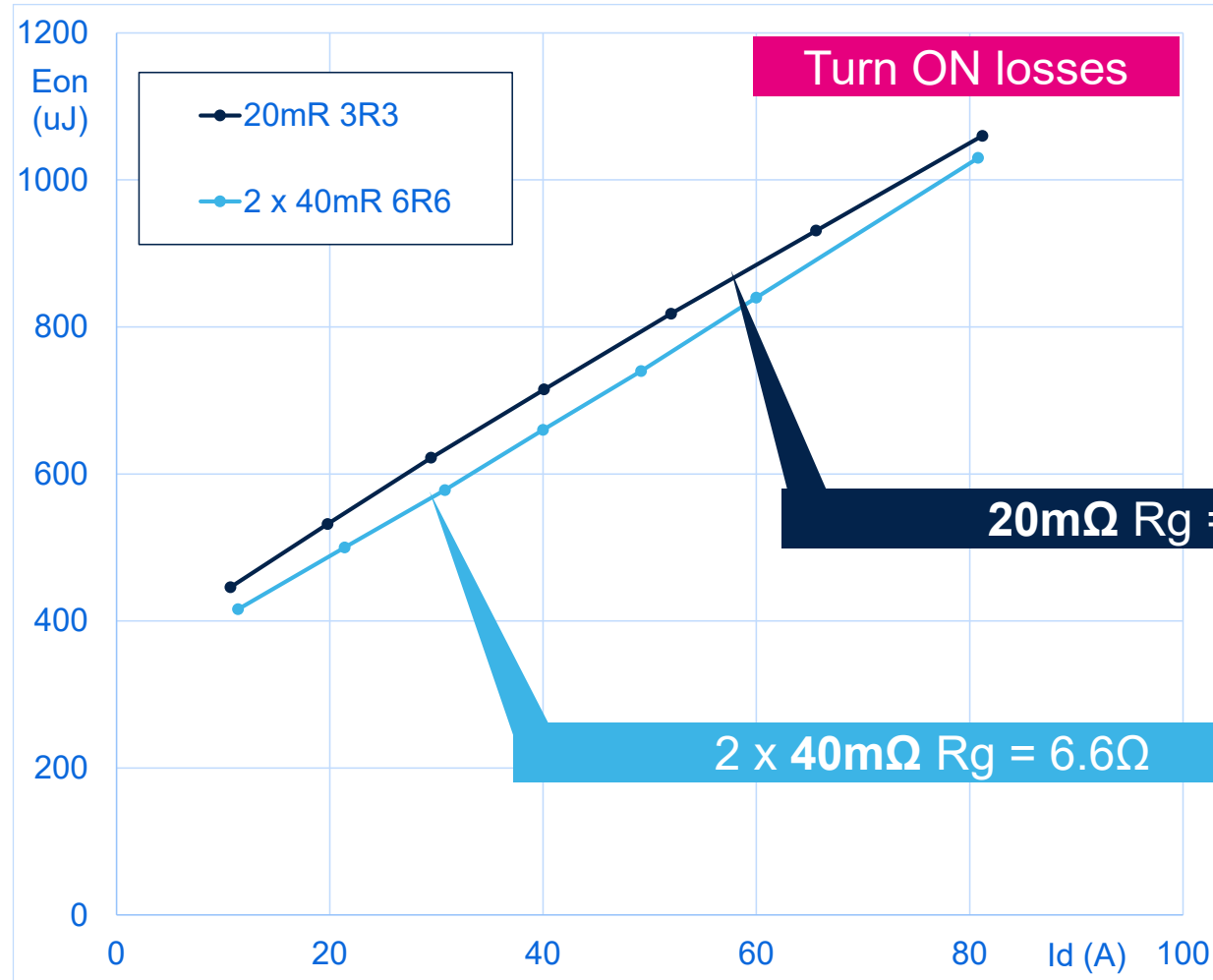


Devices	Total Rdson (Configuration)	Equivalent Thermal resistance J-case	Equivalent Thermal resistance case-heatsink*	Equivalent Total thermal resistance Junction-heatsink	$\Delta T_j$ for each 100 W Power Losses
SCT019HU120G3AG	9.6 m $\Omega$ (2 x 19.2m $\Omega$ in //)	0.15°C/W (2 x 0.3 in //)	0.3°C/W (2 x 0.6 in //)	0.45°C/W (2 device in //)	45°C
SCT025HU120G3AG	13.5 m $\Omega$ (2 x 27m $\Omega$ in //)	0.2°C/W (2 x 0.4 in //)	0.3°C/W (2 x 0.6 in //)	0.5°C/W (2 device in //)	50°C
SCT040HU120G3AG	20 m $\Omega$ (2 x 40m $\Omega$ in //)	0.25°C/W (2 x 0.5 in //)	0.3°C/W (2 x 0.6 in //)	0.55°C/W (2 device in //)	55°C
9.6 m $\Omega$ 1200V (simulated)	9.6 m $\Omega$ 1 x device in HU3PAK	0.2°C/W	0.6°C/W	0.8°C/W (one device)	80°C

Two devices in parallel provides significantly better thermal behavior than a single switch

# Benefits of parallelization

## 2. Switching losses



Comparing 2 devices in parallel and single device with comparable  $R_{DSon}$   
2 devices will generate lower switching losses



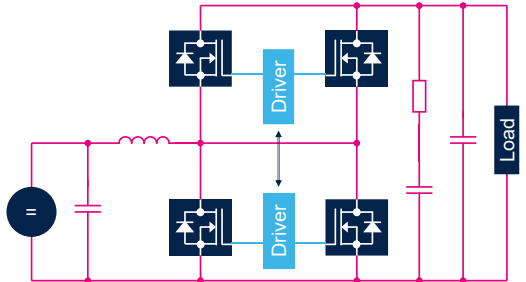
**SCT019HU120G3AG**  
**1200V/19.2mΩ**



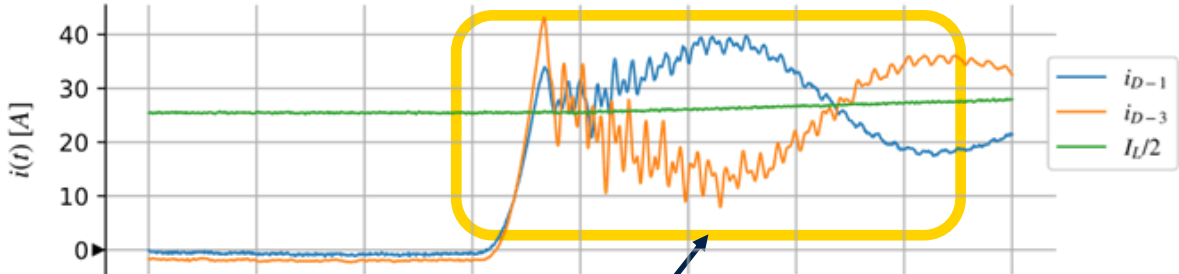
# Layout impact – tests with HU3PAK

## Comparison on signal level

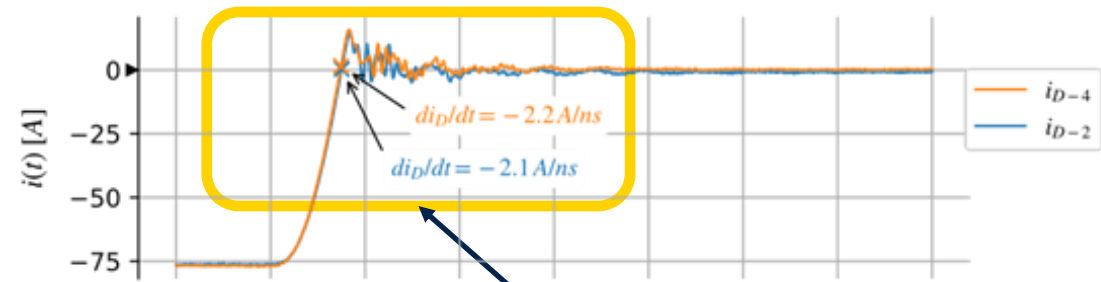
Tur ON – current waveform  
 Non ideal layout (2 layer)



Tur ON – current waveform  
 Very good layout (4 layer)



Blue –  $I_D$  through MOSFET 1  
 Orange –  $I_D$  through MOSFET2  
 Significant unbalance and oscillation amplified by non ideal layout



Blue –  $I_D$  through MOSFET 1  
 Orange –  $I_D$  through MOSFET2  
 Thanks good layout the currents are in similar tracks.





# **SiC MOSFET in HU3PAK - Case study**

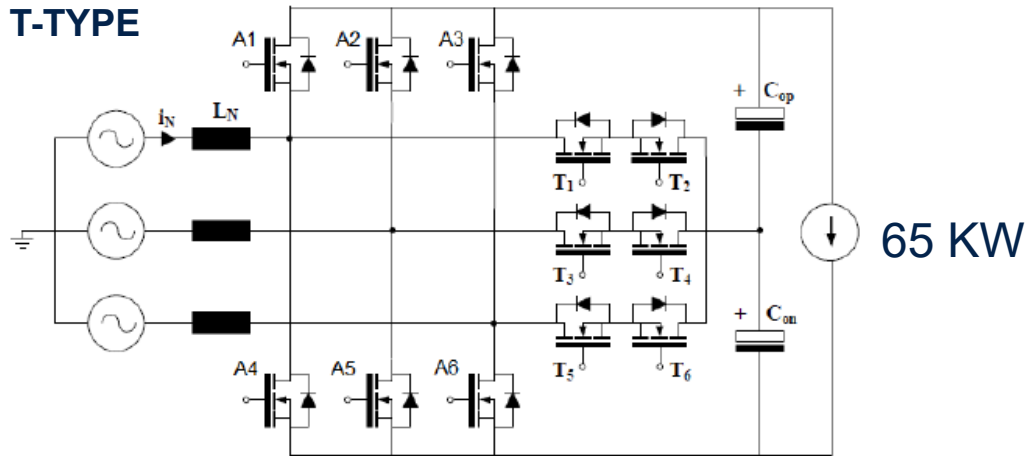
**PFC stage T-Type 3L topology**

# SCT019HU120G3AG in HU3PAK

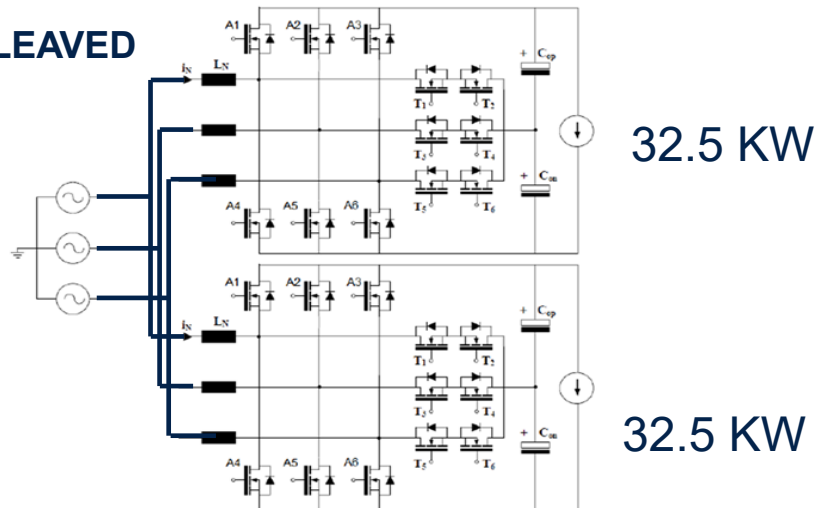
## SiC Gen3 1200V/19.2mΩ

### PFC Topologies in evaluation

#### T-TYPE



#### T-TYPE INTERLEAVED



### The main testing conditions are

- $V_{in} = 400V_{ac}$
- $V_{out} = 900V$
- $T_{hs} = 80^{\circ}C$
- $R_{th\_C-H} = 0.5^{\circ}C/W$
- $R_{th\_J-C} = 0.3^{\circ}C/W$
- $R_{g,on} = R_{g,off} = 3.3\Omega / 2\Omega$
- $f_{sw} = 40kHz$
- $P_{out} = 32.5kW / 65kW$
- $f_{sine} = 50Hz$

Order code	$V_{DS}$	$R_{DS(on)}$ typ.	$I_D$
SCT019HU120G3AG	1200 V	19.2 mΩ	90 A



Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	0.30	$^{\circ}C/W$
$R_{thJA}$	Thermal resistance, junction-to-ambient	50	$^{\circ}C/W$

- Simulations have been done considering a three-phase input voltage of  $400V_{ac}$ , with  $V_{out} 900V$  and two values of output power (32.5kW and 65kW) for 3L T-type PFC
- The cooling system consists of a heatsink with a fixed temperature of  $80^{\circ}C$  and a value of  $0.5^{\circ}C/W$  for  $R_{th\_C-H}$  for each device
- The switching frequency is 40kHz

$$R_{g,on\_dev} = R_{g,off\_dev} = 3.3\Omega$$

$$R_{th\_c-f\_dev} = 0.5^{\circ}\text{C/W}$$

$$T_{hs} = 80^{\circ}\text{C}$$



# SCT019HU120G3AG in HU3PAK

## SiC Gen3 1200V/19.2mΩ in 3L T-Type PFC

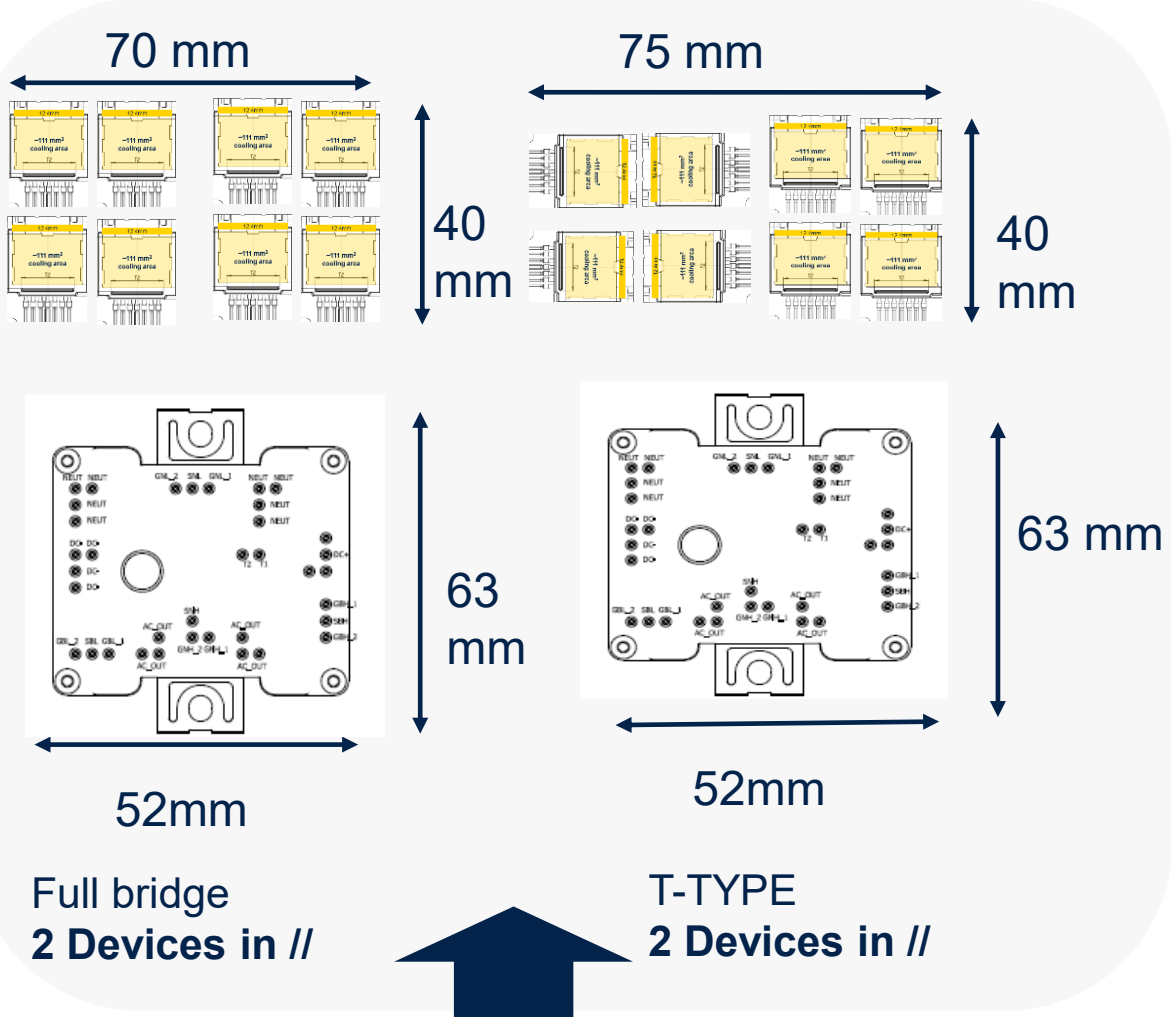
$P_{out}$ [kW]	n° devices x switch	$f_{sw}$ [kHz]	$V_{out}$ [V]	Device	$T_{j\_peak}$ [°C]	$T_{j\_avg}$ [°C]	$P_{cond}$ [W]	$P_{sw}$ [W]	$P_{tot\_dev}$ [W]	$P_{tot\_app}$ [W]	$\eta$ [%]
32.5	1	40	900	V	113	100.59	23.61	2.13	25.74	364.26	98.94%
/	/			H	112.08	107.97	28.14	6.83	34.97	/	
65	2									728.52	

- Power losses per each device are the same if doubling both the power and the number of devices. What changes are just the total power losses of the application.
- Resulting thermal resistance is very good using 2 devices in parallel for switch or interleaved solution (that is equivalent to 2 devices in parallel)
- With reference to 2x devices for each switch the resulting overall  $R_{th_{J-H}}$  for each device is **0.4°C/W** (considering the contribution of Device  $R_{th_{J-C}}$  0.3°C/W and  $R_{th_{C-H}}$  0.5 °C/W)
- Total amount of **24 SiC MOSFET in HU3PAK devices** fit with **65KW PFC 3L T-Type** Topology representing a **cost saving** solution vs any alternative package option with performances comparable to an equivalent Power Module with ALN

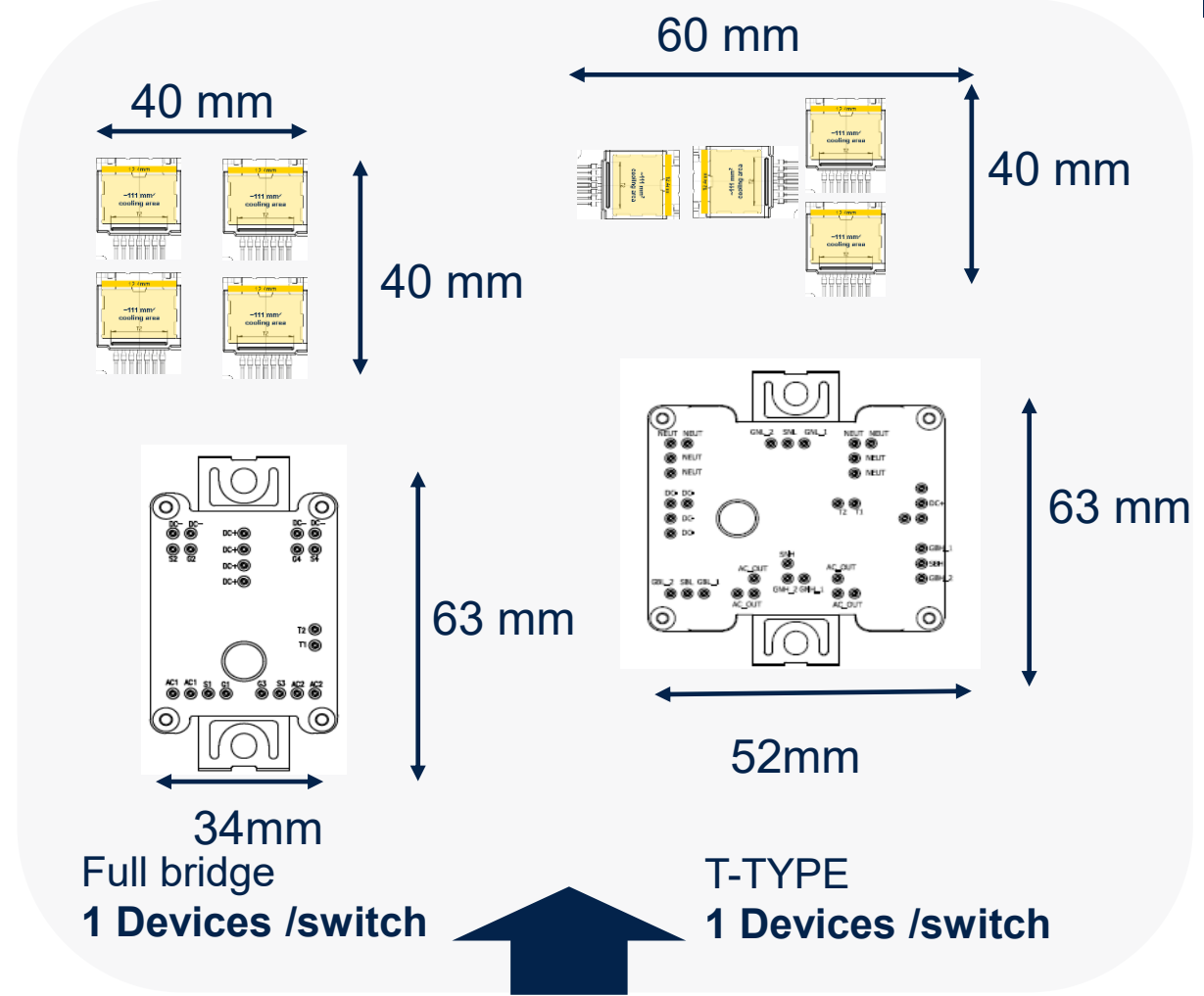
# SiC HU3PAK vs Power Module

## PCB Area layout examples

Discretes enable great flexibility vs design optimization



Parallel MOSFETs - Optimized for thermal resistance



Optimized for number of devices reduction (or interleaved solution)



# SiC paralleling - conclusions

- **Parallelization** allows to achieve **higher power transfer** thanks to:
  - Reduction of thermal resistance to heatsink allowing to reduce device temperature
  - Reduction of switching power losses (turn OFF)
- **Parallelization** allows **using discretes** for application typically covered by **power modules**
- The **good layout** (reduction of commutation loop) helps to reduce any current unbalance



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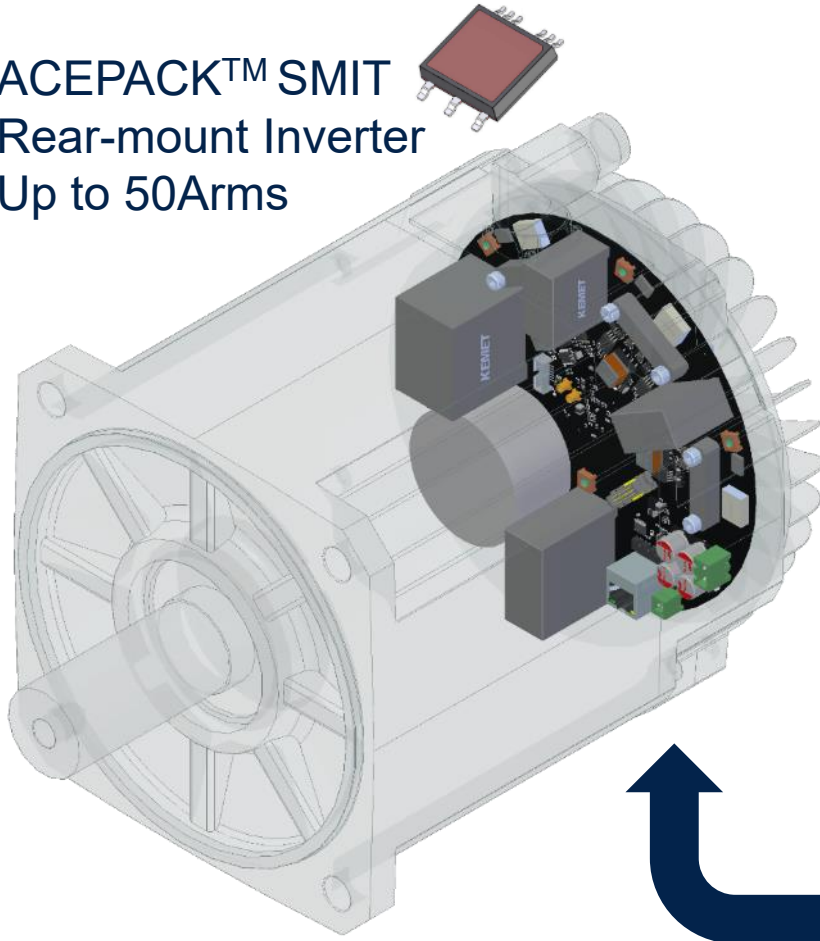
## **SiC MOSFET in Motor Control – study case**

**Infield servo drive**



# Infield Servo Drive Board Variants

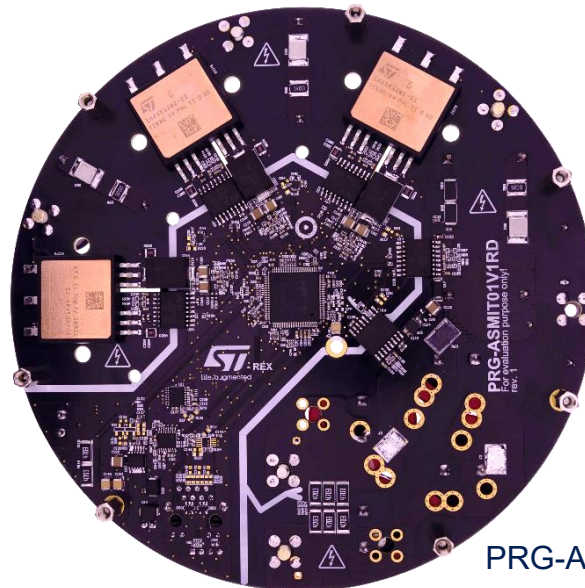
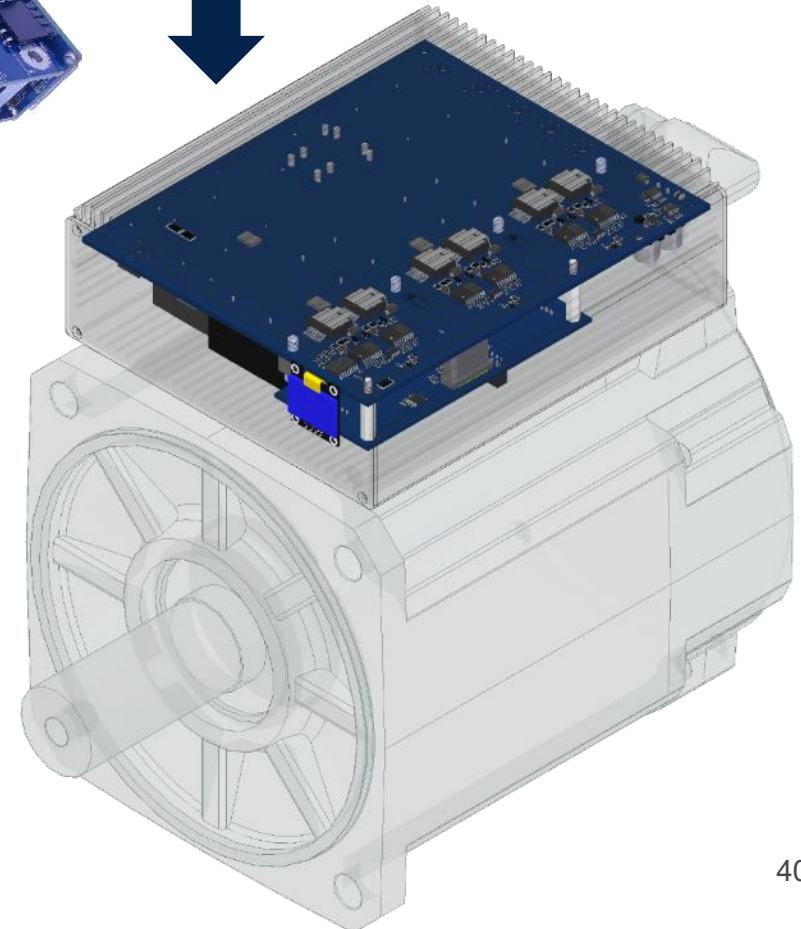
ACEPACK™ SMIT  
Rear-mount Inverter  
Up to 50Arms



PRG-HU3PK01V1



HU3PAK+STGAP3  
Top-mount Inverter  
(Near-mount)  
Up to 75Arms



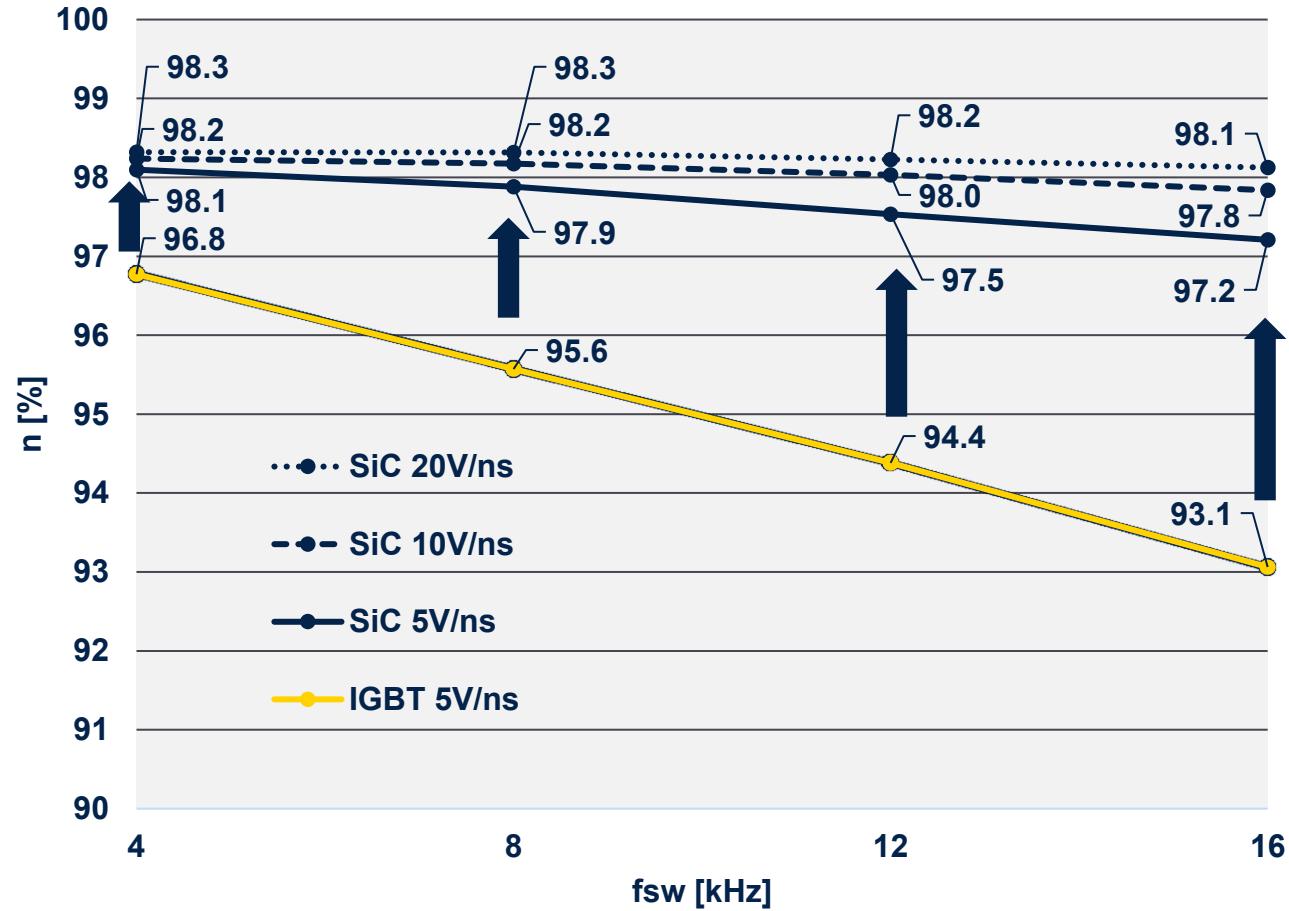
PRG-ASMIT01V1RD



# Inverter Efficiency

## 1200V/50A IGBT M series vs 1200V/40mΩ SiC Gen3

efficiency [%] @ fsw [kHz], 3.3kW output, 600VDC, f<sub>mot</sub>=50Hz,  
I<sub>mot</sub>=14.1Arms, Th=80°C, w/o residual discharge



SiC MOSFETs efficiency  
at same dV/dt

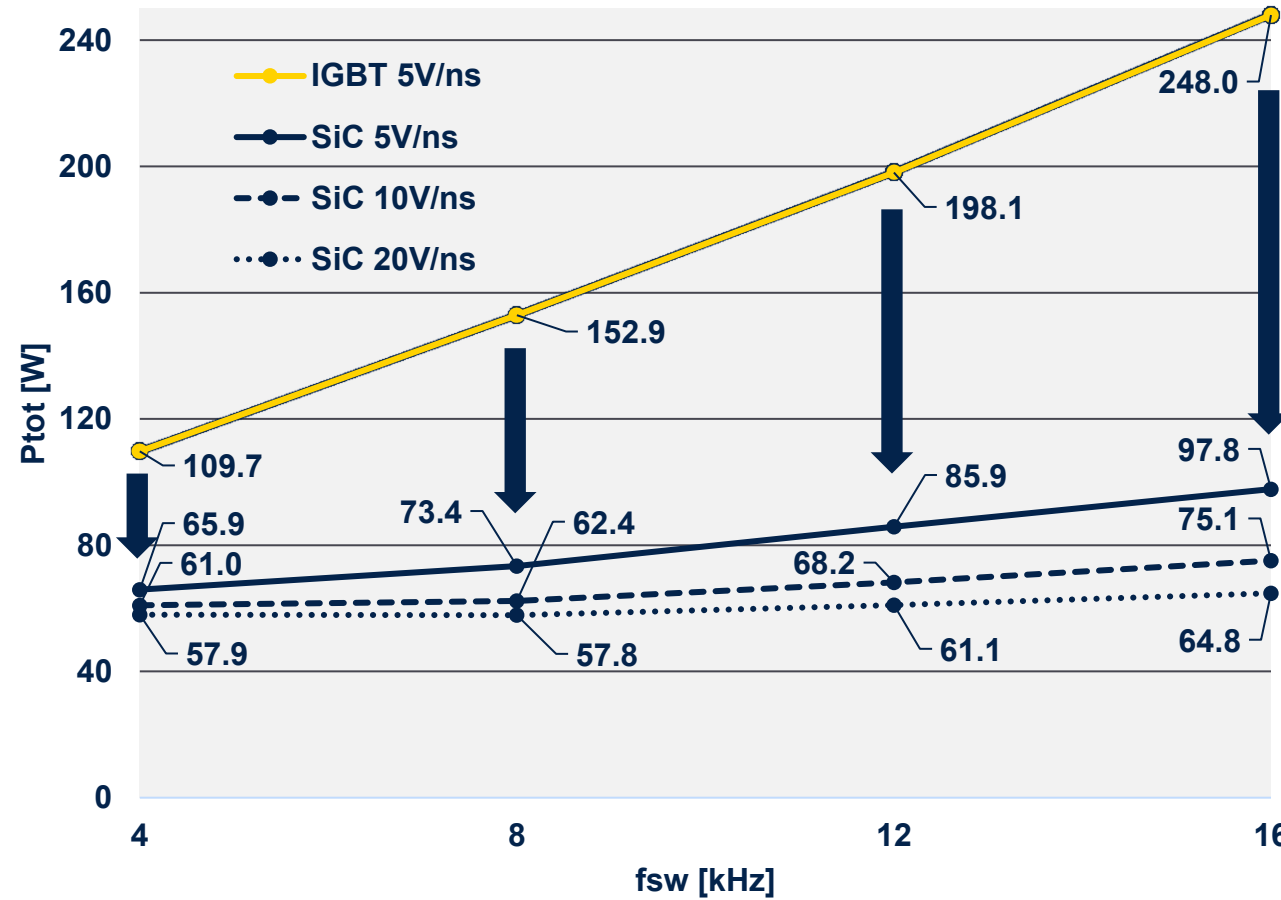
- +1.3% at 4kHz
- +2.3% at 8kHz
- +3.1% at 12kHz
- +4.1% at 16kHz



# Inverter Power Losses

## 1200V/50A IGBT M series vs 1200V/40mΩ SiC Gen3

power losses [W] @ fsw [kHz], 3.3kW output, 600VDC, fmot=50Hz, Imot=14.1Arms, Th=80°C, w/o residual discharge



SiC MOSFETs power losses at same dV/dt

- 1.7x lower at 4kHz
- 2.1x lower at 8kHz
- 2.3x lower at 12kHz
- 2.5x lower at 16kHz

Opportunity:

reduce frame size ↓

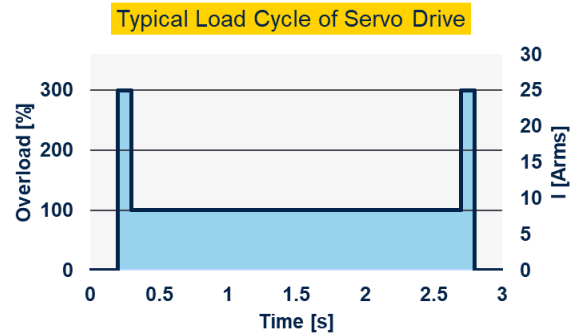
increase power density ↑



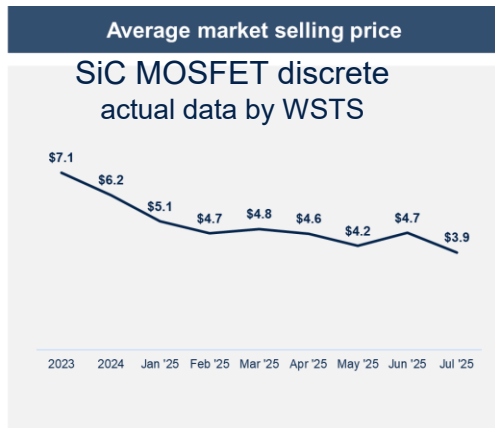
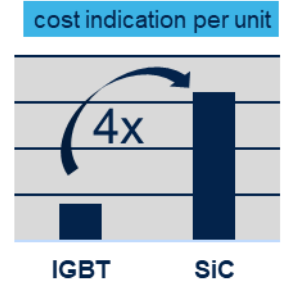
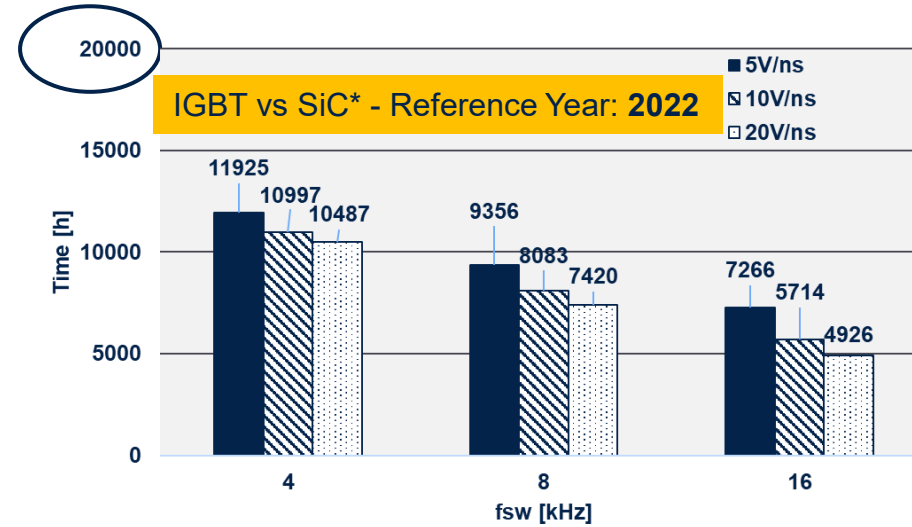
# SiC in Motor Control

## When SiC technology makes sense

### Typical Inverter lifetime (hours)



SiC worth-it-time 0.25€/kWh (source Eurostat 10/2022)



IGBT vs SiC\* - Reference Year: 2025

SiC technology makes sense anytime!



\*Source: WSTS Semiconductor Industry blue book, December 2023, December 2024, Jul '25



# Takeaways



Silicon carbide is key in **power conversion efficiency**

**Demand for SiC is growing quickly** due to its extensive use either in Automotive and Industrial fast-growing applications

Continued development of the **technology** combined with **package innovation** to improve power density and deliver **optimized cost** solutions

**ST leadership** in SiC MOSFET to support the growth today



# Our technology starts with You



Find out more at [www.st.com](http://www.st.com)

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