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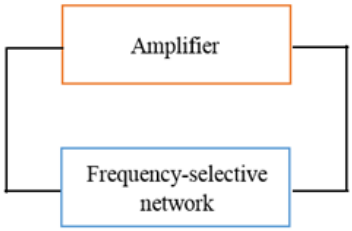
APPLICATION NOTE

# Benefit of Measuring Crystal In-Circuit

## Basic Oscillator Structure

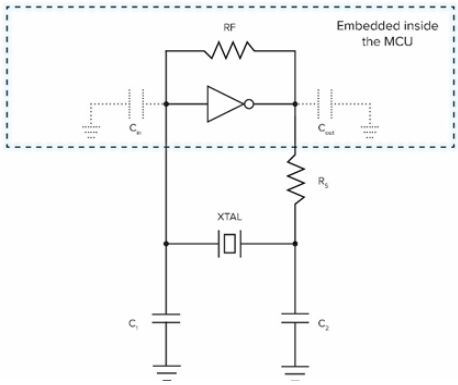
The basic structure of an oscillator comprises of two elements – an amplifier and a frequency-selective network.




There are two ways to clock a system: use a fully integrated crystal oscillator, or mate the crystal directly with the on-chip oscillator. Using an XO tends to increase power consumption and system costs. By mating a quartz crystal with the embedded Pierce oscillator circuit inside the MCU, system power consumption and costs are reduced.

The majority of embedded oscillator circuits use the Pierce oscillator, a configuration which comprises of a simple inverter amplifier as the inverting gain element within the loop.

In most cases, the amplifier unit is internal to the MCU and the frequency-selective network is external to the MCU. The key component in the external network is the quartz crystal. Associated loop capacitors and a series (current limiting) resistor (Rs) are also used.




Quartz Crystals used in this approach are coined as Parallel Plated Crystals, with standard values such as 10pF, 12pF, 18pF, etc. This implies that the final oscillation frequency will be within the tolerance of the standalone quartz crystal when the closed-loop effective capacitance is exactly equal to the quartz plating capacitance.

As a feedback system, the oscillator demands extensive analysis along with a thorough understanding of circuit board and layout parasitics to optimize the loop and ensure operation over all conditions. Designers often optimize the crystal oscillator performance via trial and error, which saves time analyzing and modeling the components and circuit board. Tight time-to-market and scheduling constraints have led to more trial and error rather than bottoms up analysis. The result is non-optimal coupling between the crystal and the Pierce oscillator.

Optimal coupling guarantees the crystal is neither over-driven nor under driven. Overdriving the crystal, especially in today's low power varieties can lead to stress fractures and overall reliability concerns during operation. Under driving may lead to failure on startup or an eventual decay of the oscillation. Additionally, there are frequency accuracy concerns. MCUs with Pierce oscillators that offer configurable transconductance, can also optimize for lowest power consumption. Without careful analysis and verification, design by trial and error can lead to any of these concerns.

Growing technology trends including green energy initiatives and the explosive growth of IoT centric solutions, are driving the need to accurately define the frequency-selective network in order to achieve the best possible accuracy in frequency domain, while ensuring robust oscillator loop performance.

Measuring in-circuit crystal performance eliminates the problem by converting the unknowns into well knowns. Characterizing the complete frequency-selective network including board parasitics minimizes uncertainty and maximizes confidence in long term system reliability.

The frequency-selective network includes the following passive components selected and optimized by the designer:

1. Quartz Crystal
2. Loop Capacitor, C1
3. Loop Capacitor, C2
4. Current Limiting Resistor, RS (if applicable)

There are three key oscillator performance parameters dictating the values of the passive components.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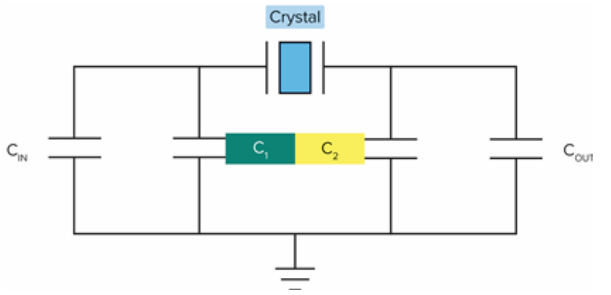
These parameters include frequency accuracy of the oscillator loop, drive level seen by the crystal, and the closed-loop Gain Margin of the oscillator.

Frequency Accuracy of the Oscillation Loop

The frequency at which the oscillator loop is oscillating should be as close as possible to the specified carrier frequency of the crystal. Deviating too far from the system's boundary condition in frequency domain may result in system fault or failure.

To achieve desired frequency accuracy, the crystal must see in-circuit capacitance equivalent to the plating capacitance set when the crystal was manufactured, such as 10pF, 12pF, 18pF, etc.




Wherein, Cin and Cout are the amplifier's input/output junction capacitances, respectively, the effective closed-loop capacitance (Ceff) seen by the crystal can be defined as:

$$\text{ceff} = \left\{\frac{(Cin + C1)(C2 + Cout)}{(Cin + C1 + C2 + Cout)}\right\} + C(board\ strays)$$

The challenge lies in the fact that most MCU datasheets do not clearly outline the expected values for Cin and Cout; even though they play a critical role in the final oscillation frequency.

The current limiting resistor is rarely engaged, since most MCU embedded oscillator loops do not present excessive drive to the crystal.

Drive Level seen by the Crystal

The drive level seen by the crystal can be approximated as:

DL=ESR × IQ^2

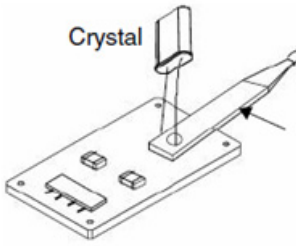
Where;

ESR = equivalent series resistance of the crystal
IQ = current flowing the crystal in RMS

It is important to note that driving a quartz crystal with a much higher drive may lead to quartz blank heating, excitation of unwanted modes or spurs, frequency shift, aging, etc. In the case of unwanted modes and spurs, the end result would most likely be degradation of phase noise and jitter at the oscillator output.

Adding the current limiting resistor is the simplest way to reduce unwanted effects. Together, the resistor and the reactive impedance of the oscillator loop capacitor on the output side of the amplifier, create a voltage divider. This phenomenon scales the signal level going through the crystal.

To determine the drive level (DL) in the crystal, the RMS current (IQ) through the crystal must be measured using a current probe.




The current probe is connected to an oscilloscope and the Vp-p signal is measured. Then, using the following relationship, DL can be estimated.

$$IQ = \frac{IQ(Vp-p)}{2\sqrt{2}}$$

$$DL = ESR \times IQ^2$$

For proper oscillator loop operation, it is imperative that DL does not exceed the maximum specified value by the Quartz Crystal manufacturer, typically 100µW. Exceeding this value on a consistent basis may cause accelerated aging, frequency drift, EMI issues due to excitation of unwanted tones, modes or spurs, etc.

Gain Margin of the Oscillator Loop

The Gain Margin (GM), also referred to as the Safety Factor (SF) of the oscillator circuit quantifies the oscillator's ability to start up and sustain oscillations under all operating conditions and associated variations in critical parameters such as ESR, amplifier transconductance, temperature, bias, etc.

GM can be quantified as:

$$\text{GM} = \frac{Amplifier\ transconductance\ (gm)}{\{4 \times ESR \times (2\pi F)^2 \times (C0 + CL)^2\}}$$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Physical conditions which could affect the safety factor of the oscillator circuit include part-to-part and lot-to-lot variations of crystal ESR in mass production and variation in the oscillator amplifier's transconductance, particularly over the extended operating temperature range.

The presence of an AGC circuit embedded inside the oscillator loop of the MCU significantly limits the ability to manipulate the drive level through the crystal by altering the plating load of the crystal and/or the external loop capacitors.

To quantify the true closed-loop gain margin, a variable resistor needs to be placed in series with the crystal and adjusted until the oscillations seize. Then, the value of this resistance is divided by the ESR of the crystal to arrive at the closed-loop gain margin. The oscillation margin, or Safety Factor (SF), industry adopted target is as follows:

| Safety Factor (SF) | Design Capability |
|---|---|
| SF < 1.50 | In-sufficient |
| 1.50 < SF < 2.0 | Risky |
| 2.00 < SF < 3.00 | Marginal |
| 3.00 < SF < 5.00 | Safe (acceptable) |
| SF > 5.00 | Desired |

## Conclusion

Although the implementation of a commodity crystal in a typical timing requirement seems trivial at first glance, specific provisions need to be taken to ensure a robust design that accounts for real world variation of key performance parameters for both the quartz crystal and the embedded oscillator loop.

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