600 V CoolMOS™ PFD7

SJ MOSFET for high power density adapters and motor drives

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About this document

Scope and purpose

This document describes Infineon's latest high voltage (HV) superjunction (SJ) MOSFET technology with integrated fast body diode for consumer applications. This new product family broadens the CoolMOS™ 7 series, addressing ultra-high-power density chargers, travel adapters and low-power motor drives. The 600 V CoolMOS™ PFD7 offers all the efficiency benefits enabled by fast switching and low conduction losses combined with a reduced oscillation tendency, providing ease of use. In order to prevent failures during the assembly phase the 600 V CoolMOS™ PFD7 features an ESD robustness greater than 2 kV (HBM) for $R_{DS(on)}$ greater than or equal to 280 mΩ. The ultra-low reverse recovery charge (Q_{rr}) at the same time boosts efficiency in motor drive applications and improves reliability in high-density adapters based on half-bridge configuration (e.g. Active Clamp Flyback), where hard commutation on a conducting body diode may occur under abnormal conditions.

This application note will describe the technical benefits of the 600 V CoolMOS™ PFD7 compared to the 600 V CoolMOS™ P7 and 600 V CoolMOS™ CE based on characterization data and application measurements.

In the last section of the document design guidelines will be provided to ensure a trouble-free design-in process for both targeted applications.

Intended audience

This document is intended for SMPS design engineers.

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1 Introduction

This application note describes the characteristics of the 600 V CoolMOS™ PFD7, the newest HV SJ MOSFET technology from Infineon for the consumer market, featuring a substantial efficiency increase in the targeted applications combined with ease of use. This consists of high ESD robustness, low oscillation tendency and excellent body diode robustness against destruction due to hard commutation.

The 600 V CoolMOS™ PFD7 offers all the known benefits of the 600 V CoolMOS™ P7, and in addition a best-in-class fast body diode and a switching behavior specifically optimized for resonant topologies (ZVS Flyback, Active Clamp Flyback, LLC).

1.1 Target applications

The 600 V CoolMOS™ PFD7 is the latest product in the CoolMOS™ 7 series, tailored for:

- High-density chargers/adapters (more than 30 W)
- Low-power drives (less than 300 W)

1.1.1 High power density chargers/adapters

The increasing market adoption of fast charging and USB-PD standards compels designers to significantly improve the power density of travel adapters. In a completely enclosed adapter, any size reduction through high switching frequency or package innovation must go hand in hand with efficiency improvements to maintain low component and adapter case temperatures. Figure 1 shows the relationship between power density and the minimum efficiency required to keep the adapter case temperature below 70°C for a 65 W adapter. It is evident that, to increase the power density above 20 W/in^3, the converter efficiency must be above 92.5 percent. Typically, for chargers and adapters with universal input range (90 V_{ac}-264 V_{ac}) the most critical operating point to meet the minimum efficiency requirement is at:

- Maximum continuous output power
- Minimum input voltage (typically 90 V_{ac})

The reason for this is that at this operating point the conduction losses reach the maximum, resulting in a poorer overall efficiency compared to high input-line conditions.

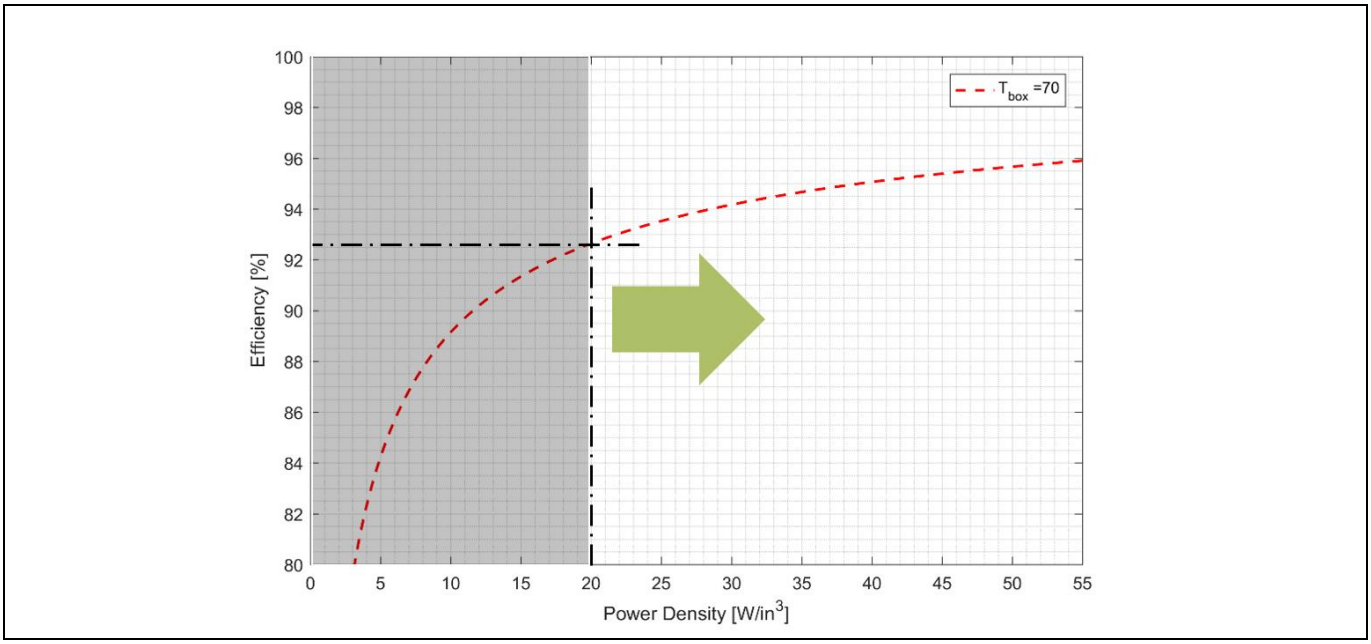


Figure 1 Efficiency required for an adapter case temperature equal to 70°C (P_{out} = 65 W)

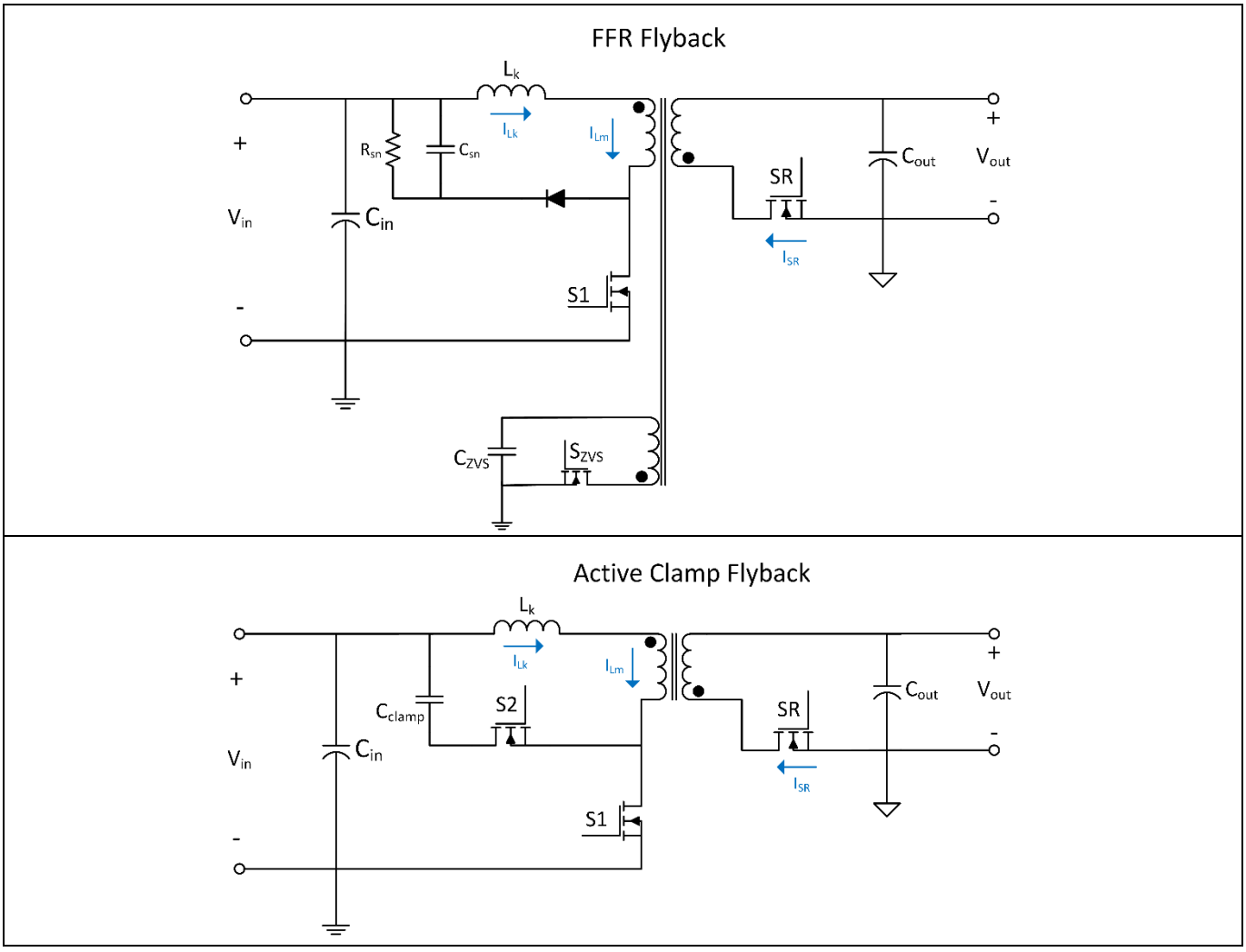
The single-switch QR Flyback has been widely adopted in power adapter applications: it is operated in Discontinuous Conduction Mode (DCM), achieving Zero Voltage Switching (ZVS) at low-line and partial hard switching at high-line. However, the hard-switching operation occurring at high-line together with the lack of recovery of the transformer leakage energy limits the maximum switching frequency at which the adapter can be operated.

In order to overcome these limitations designers are moving toward topologies embedding the following features:

- Soft-switching (ZVS) operation, regardless of the input-line voltage and loading conditions
- Recovery of the transformer leakage energy

Well-known examples of topologies satisfiying one or both requirements above are the Forced Frequency Resonant Flyback (FFR), the Active Clamp Flyback (ACF) and the Resonant Hybrid Flyback (RHF) (see Figure 2). In all these cases soft-switching operation enables the elimination of turn-on losses and moving to relatively high switching frequencies (typically more than 120 kHz). At this point the remaining main loss mechanisms affecting the MOSFET are turn-off losses, conduction losses and the so-called "C_{oss} hysteresis losses", which will be described in 2.2.6. With the new 600 V CoolMOS™ PFD7 Infineon is addressing all these loss mechanisms at once, reducing the switching losses (turn-off and C_{oss} hysteresis losses) and enabling low $R_{DS(on)}$ in packages with reduced mechanical dimensions.

The new 600 V CoolMOS™ PFD7 is Infineon's optimized solution to achieve high power density at an affordable cost.



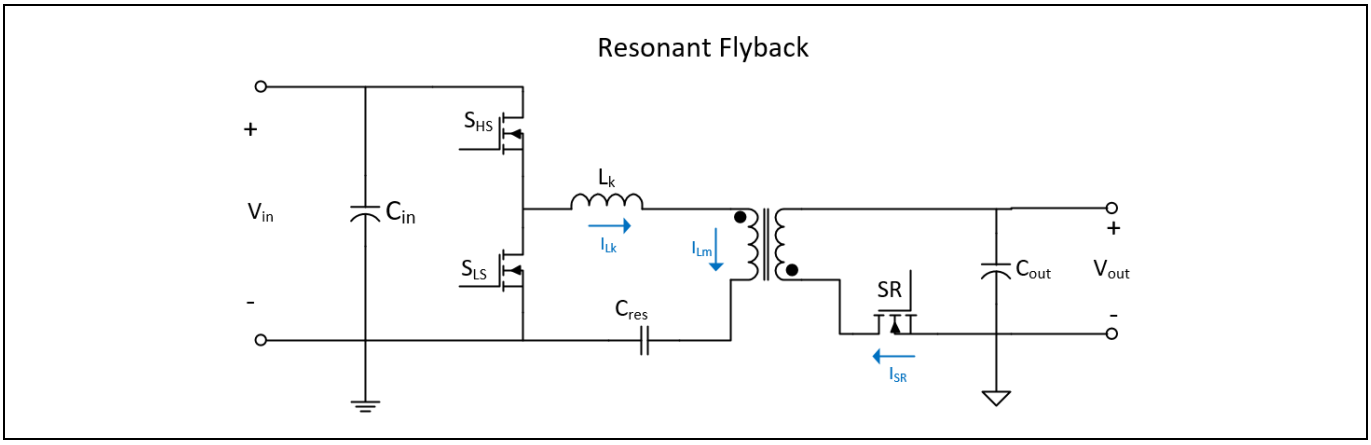


Figure 2 Simplified schematics of most common topologies used for high-density adapters

All the topologies mentioned above exploit the same principle to ensure soft-switching throughout the entire load range and input voltage conditions. This principle consists of energizing the magnetizing inductance of the transformer with a small amount of negative current, which enables discharge of the output capacitance of the low-side switch, thus enabling ZVS. Detailed descriptions of FFR and RHF are available in [1] and [2] respectively, while ACF operation will be covered in this document.

1.1.1.1 Active Clamp Flyback Operation

As previously mentioned, ACF is one of the most attractive topologies for high-density adapter applications because it enables soft-switching operation and the recovery of the transformer leakage energy. The two most common control schemes used with this topology are the so-called Non-Complementary Control (NCC) and Complementary Control (CC). Since the latter is the most adopted, it will be explained in detail below.

The typical waveforms of the ACF operated with CC are shown in Figure 3.

Phase 1 ($t_0 \rightarrow t_1$)

During this phase the switch S1 is on while switches S2 and SR are kept off. A positive voltage V_{in} is applied to the primary side of the transformer, forcing the same current through leakage and magnetizing inductance. No current is flowing through the secondary side since the SR is kept off and its body diode is blocking a voltage equal to $V_{out} + V_{in}/n$ where n is the transformer turns ratio.

The expression of the primary-side current is as follows:

$$I_{Lm}(t) = I_{Lk}(t) = I_{Lm}(t_0) + \frac{V_{in}}{L_m + L_k}(t - t_0)$$

Phase 2 ($t_1 \rightarrow t_2$)

During this phase all the switches are off, the magnetizing current is still positive and it discharges the parasitic capacitance of the switch S2, thus enabling ZVS operation for the latter.

Phase 3 ($t_2 \rightarrow t_3$)

At the beginning of this phase S2 is turned on with ZVS while all the other switches are kept off. As soon as the primary-side voltage reaches a value slightly higher than the reflected voltage nV_{out} the body diode of the SR starts to conduct current and a resonance between the leakage inductance L_k and the clamp capacitor C_{clamp} occurs. The resonant frequency of the oscillation is as follows:

$$f_{res} = \frac{1}{2\pi\sqrt{L_k C_{clamp}}}$$

At the same time the magnetizing inductance is discharging with a current equal to:

$$I_{Lm}(t) = I_{Lm}(t_2) - \frac{nV_{out}}{L_m}(t - t_2)$$

The current flowing through the secondary-side SR is equal to the difference between the magnetizing current I_{Lm} and the leakage current I_{Lk}:

$$I_{SR}(t) = n(I_{Lm}(t) - I_{Lk}(t))$$

When $I_{Lk}(t) = I_{Lm}(t)$ the secondary-side current is equal to zero and the SR can be turned off with ZCS. In order to ensure simultaneous ZVS and ZCS operation the leakage current I_{Lk} must intersect the magnetizing current I_{Lm} when the latter is negative enough to be able to completely discharge the parasitic capacitance seen at the drain node of the primary-side switch S1. Optimum operation is achieved when the intersection happens at the minimum negative value of magnetizing current needed to discharge the parasitic capacitance seen at the drain node of the primary-side switch S1.

Phase 4 ($t_3 \rightarrow t_4$)

During this phase all the switches are off, and the magnetizing current is still negative thus it discharges the parasitic capacitance seen at the drain node of the primary-side switch S1, enabling the lossless ZVS turn-on of the latter in the next phase. Once the parasitic capacitance seen at the drain node of the primary-side switch S1 has been completely discharged, a new switching cycle can begin with the ZVS turn-on of S1.

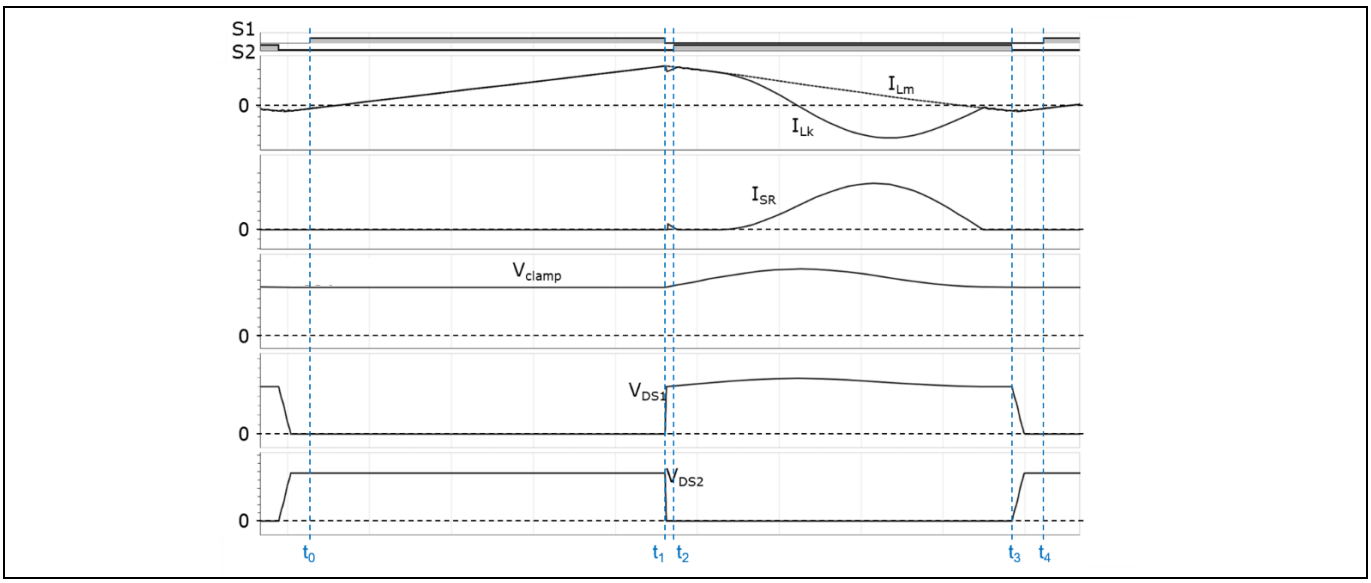


Figure 3 typical waveforms

1.1.2 Low-power motor drives

Motors are a key part of many appliances. So far, the traditional approach has been based on (on/off) control with no speed control techniques. This leads to a much higher power consumption. On the other hand, inverterization is the technique commonly used today, where an inverter converts power from DC to AC. This means that the end application not only runs in a quieter and smoother manner, but also that the average power consumption is reduced in comparison to the traditional on/off control.

Infineon aims to make the world an easier and greener place by delivering highly energy-efficient semiconductor solutions with best performance. In application note [3] we focus on developing a complete system design to help customers reduce time-to-market. Infineon offers a range of products dedicated to motor applications such as iMOTION™ controllers, CoolMOS™ discrete SJ MOSFETs and EiceDRIVER™ gate driver ICs. This covers complete solutions including applications for Brushless DC (BLDC) fans, refrigerators, pumps and low-power appliances.

Constant cost pressure and increased consumer expectations have driven design engineers to seek minimal hardware solutions that extract maximum performance from motors used in consumer goods. Space Vector Modulation (SVM) techniques can be applied for AC induction motors, permanent magnet synchronous motors and BLDC motor types, while the SVM provides more efficient use of the bus voltage than the conventional modulation, at the price of a higher number of commutations per switching cycle. Therefore, methods with the maximum number of commutations like the symmetrical SVM method have the highest switching losses.

Another important contribution to switching losses is related to the switching speed dv/dt. High-speed switching transitions of the MOSFET drain-source voltage dv/dt during PWM operation in motor drive inverters cause displacement currents through the parasitic capacitance of the motor to the Protective Earth (PE). These currents flow predominantly through the bearings, leading to accelerated aging of the latter. This is a well-known failure mechanism, which depends on the switching frequency of the inverter and on the switching speed of the inverter's MOSFET.

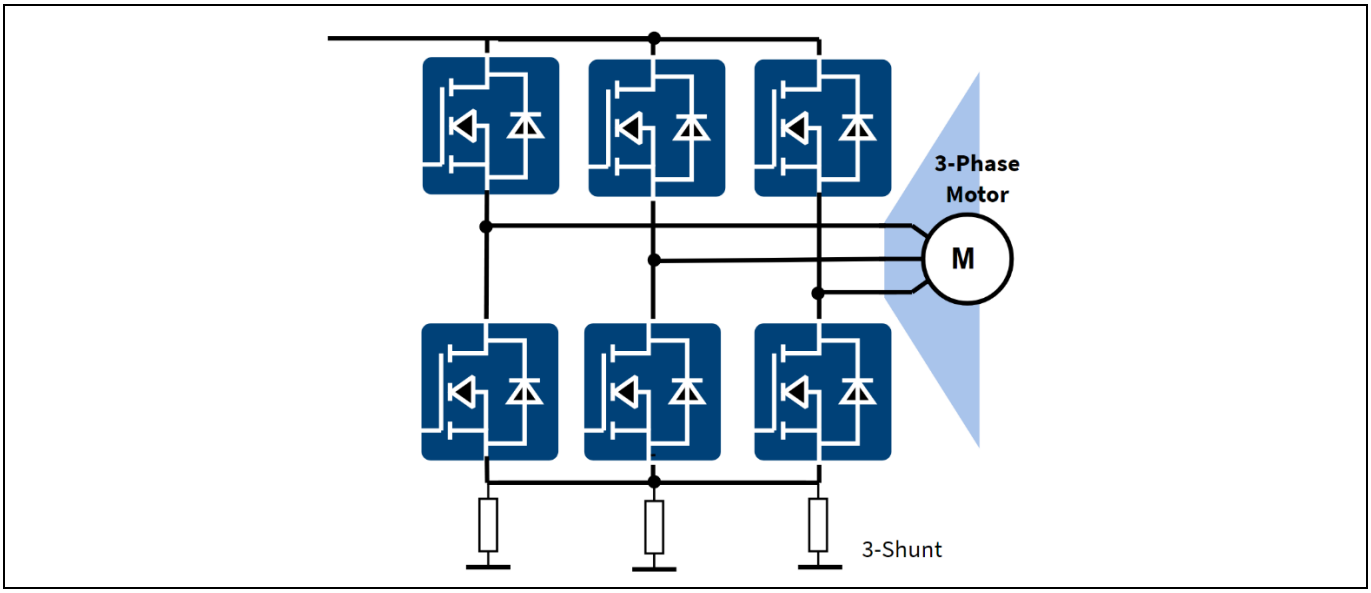


Figure 4 Typical three-phase power inverter

The slower the turn-on and turn-off, the less current flows through the bearings; however, unfortunately, slow switching is always correlated with increased switching losses. A typical three-phase power inverter, shown in Figure 4, is commonly used in IGBTs mainly because of the good performance offered by the co-packaged diode. In contrast, SJ MOSFETs suffer from a high reverse-recovery charge Q_{rr} when operated in diode mode. Consequently, especially at light load conditions, the switching losses become dominant. In order to enable very low switching losses for SJ transistors it is necessary to use transistors with very low Q_{rr} such as the new 600 V CoolMOS™ PFD7.

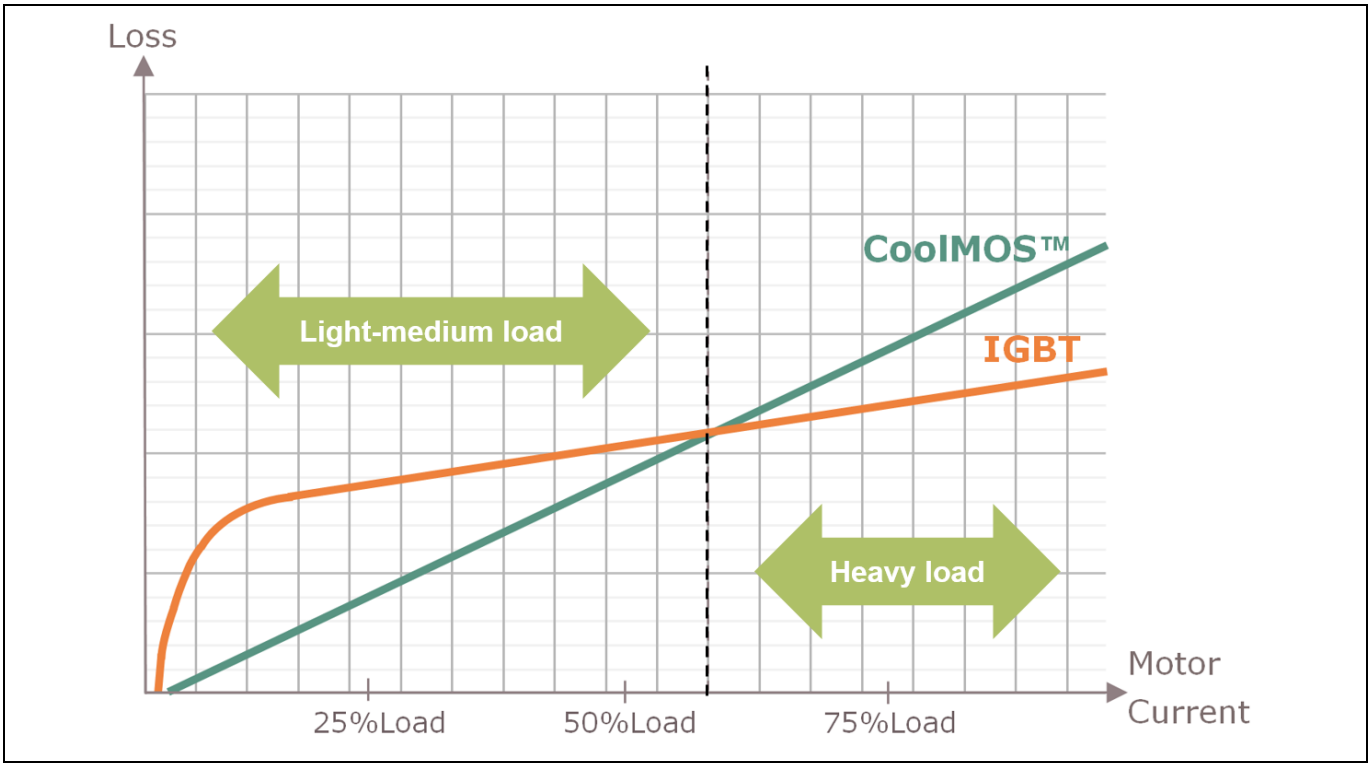


Figure 5 Conduction loss comparison between CoolMOS™ and IGBT with the same current rating

When conducting, the unipolar MOSFET acts like a resistor. In contrast, a bipolar IGBT device behaves like a resistor in series with a diode. Figure 5 illustrates the conduction losses of a MOSFET and of an IGBT having a similar current rating: while the MOSFET exhibits a linear increase of the conduction loss with the motor current determined by the on-state resistance $R_{DS(on)}$ value, the IGBT exhibits a non-linear behavior due to the almost constant collector-emitter V_{CE} voltage drop. This intrinsic difference in the on-state behavior leads to different performances at different load points: MOSFETs show lower losses than IGBTs at medium and light loads thanks to the lower conduction losses at low current, while the situation is the opposite at heavy load.

Now, considering the overall device losses for both switch types, MOSFET and IGBT, conduction losses are the dominating factor at heavy load. At medium and light loads, instead, the contribution of conduction losses is drastically reduced for the MOSFET, while it remains significant for the IGBT. As a result, the MOSFET enables higher efficiency at medium and light loads compared to the IGBT.

2 Technology parameter comparison of 600 V CoolMOS™ CE, P7 and PFD7

2.1 Technology description

The fundamental prerequisite for selecting the optimal MOSFET for the desired application is to clearly understand how it differs from previous technologies. This section will clarify which electrical parameters of the 600 V CoolMOS ™ PFD7 are key for the targeted applications. Specifically, the 600 V CoolMOS™ PFD7 replaces the 600 V CoolMOS™ P7 in charger/adapter applications targeting the highest power densities, while it replaces the 650 V CoolMOS™ CE in motor drive applications, providing higher performance at lower cost.

Table 1 compares datasheet values between the 600 V CoolMOS™ CE, 600 V CoolMOS™ P7 and 600 V CoolMOS™ PFD7. It is important to note that values of the electrical parameters provided in the datasheet are often specified at different test conditions by different vendors, thus preventing a fair comparison. In order to overcome this limitation in the following document a comparison of the key electrical parameters based on characterization data will be provided.

Table 1 Comparison based on datasheet values between CoolMOS™ CE, P7 and PFD7 in the 360 mΩ $R_{DS(on)}$ class

Specification	Unit	Symbol	CE 380 mΩ	P7 360 mΩ	PFD7 360 mΩ
Drain-source breakdown voltage	V	$V_{(BR)DSS}$	600	600	600
Max. on-state resistance at 25°C	mΩ	$R_{DS(on)}$	380	360	360
ID current rating at 25°C	A	$I_{D,cont}$	15	9	10
ID pulse rating	A	$I_{D,pulse}$	30	26	24
Typical gate-to-source charge	nC	Q_{gs}	4	3	3
Typical gate-to-drain charge	nC	Q_{gd}	16	4	4.4
Typical gate charge total	nC	Q_g	32	13	12.7
Typical C_{iss}	pF	C_{iss}	700	555	534
Typical C_{oss} at V_{DS} = 400 V	pF	C_{oss}	46	10	12
Typical energy stored in the output capacitance at V_{DS} = 400 V	µJ	E_{oss}	2.8	1.6	1.6
Typical effective output capacitance, energy related	pF	$C_{o(er)}$	30	20	20
Typical effective output capacitance time related	pF	$C_{o(tr)}$	136	214	187
MOSFET dv/dt ruggedness	V/ns	dv/dt	50	80	120
Reverse diode dv/dt	V/ns	dv/dt	15	50	70
Maximum diode commutation speed	A/µs	dI_F/dt	500	900	1300
Reverse recovery charge (typical)	µC	Q_{rr}	3.3	0.74	0.14
Peak reverse recovery current (typical)	A	I_{rrm}	21	11	4.1
Reverse recovery time (typical)	ns	t_{rr}	290	145	60

2.2 Technology comparison between CoolMOS™ PFD7, P7 and competitors

In this section the key electrical parameters of the 600 V CoolMOS™ PFD7 will be compared to those of the 600 V CoolMOS™ P7 and of two competitor devices based on characterization data.

Furthermore the parameters that make the 600 V CoolMOS™ PFD7 the best choice for high-density charger and adapter applications will be explained.

A brief description of which PFD7 parameters are important for motor drive applications will be provided in Figure 19, while a detailed description is provided in application note [3].

2.2.1 Gate charge

The total gate charge Q_g of the 600 V CoolMOS™ PFD7 is at the same level as in the 600 V CoolMOS™ P7, which makes it more than 50 percent lower than the one of the best competitors, the SiHF30N60E from Vishay. A low total gate charge value improves the light load efficiency, helping the designer meet the ultra-low standby consumption levels typically required in adapter/charger applications.

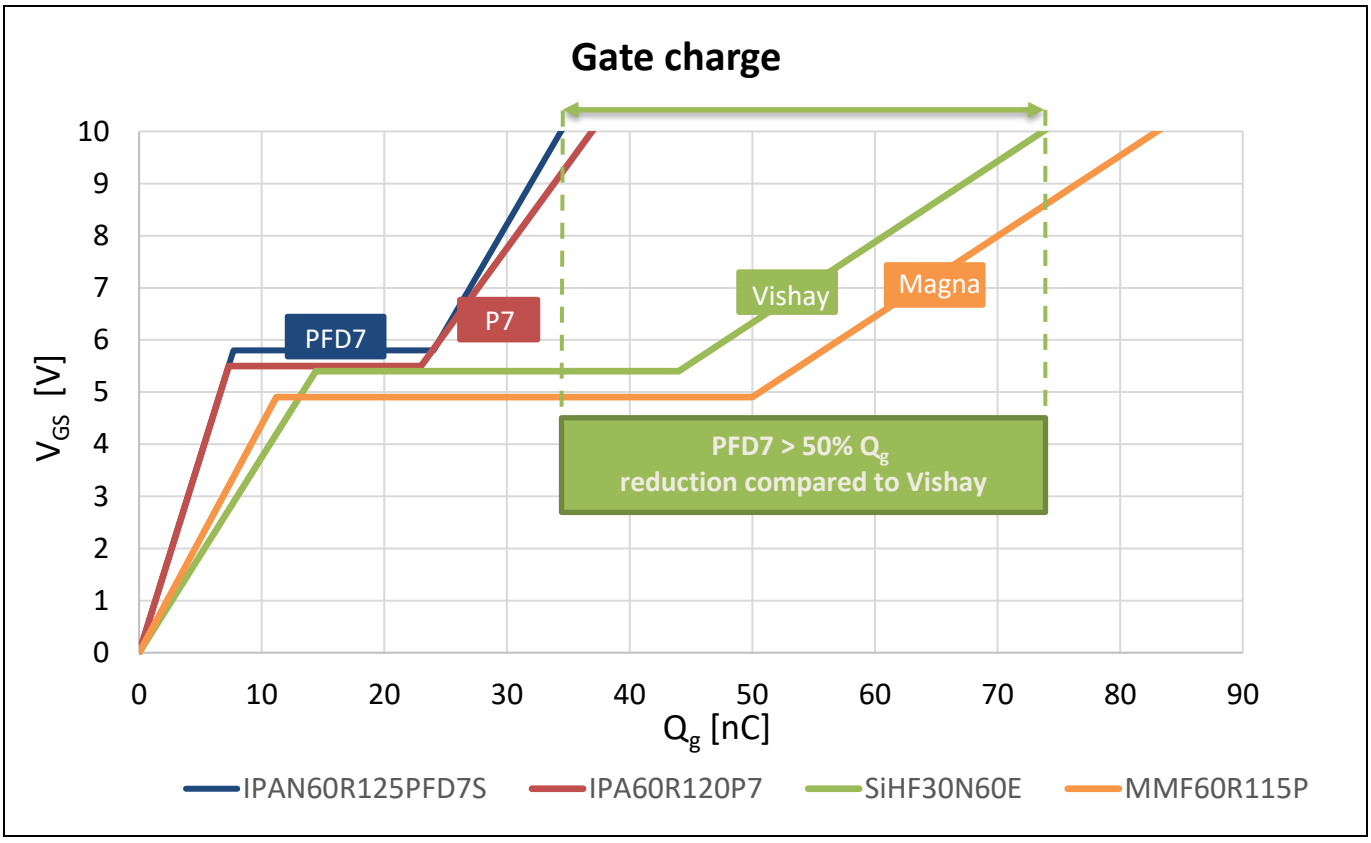


Figure 6 Gate charge comparison between CoolMOS™ PFD7, P7 and competitors

2.2.2 Energy and charge stored in the output capacitance (E_{oss} and Q_{oss})

The E_{oss} represents the energy stored in the output capacitance of the MOSFET. Figure 7 clearly shows that E_{oss} of the CoolMOS™ PFD7, which is virtually overlapping with that of the P7, from 45 V onward is much lower than the values offered by the competitors. It is evident that at high drain-source voltages the CoolMOS™ PFD7 and P7 offer up to 60 percent (at 400 V) lower E_{oss}. However, since high-density charger and adapter applications operate under soft-switching conditions, meaning that the drain-source voltage of the device is brought down close to 0 V prior to turning on the device, the important points to look at in the graph below are the bends in the E_{oss} curves.

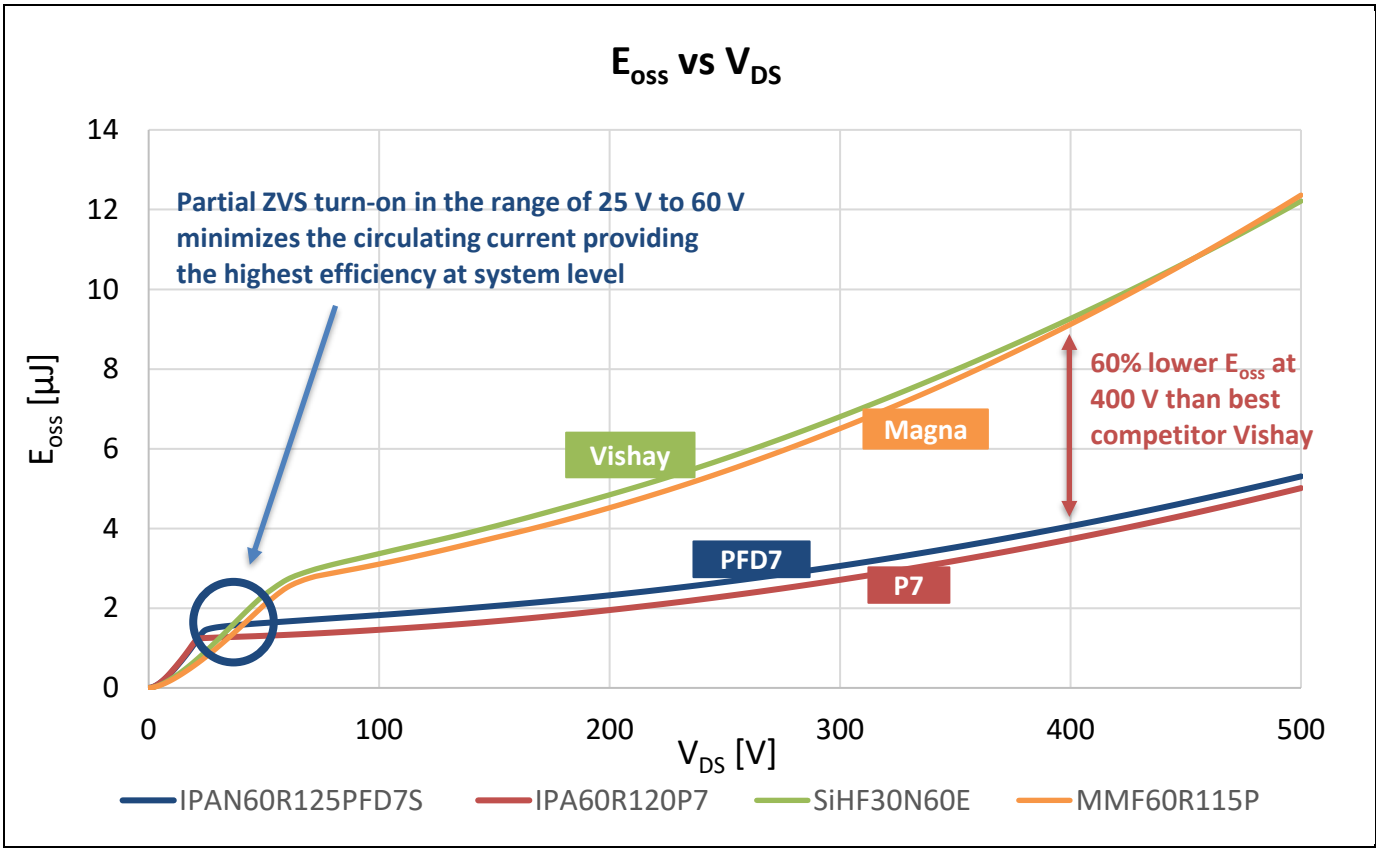


Figure 7 E_{oss} comparison between CoolMOS™ PFD7, P7 and competitors in the 120 mΩ class

The importance of the bend in the E_{oss} curve can be understood by looking at the Q_{oss} graph shown in Figure 8: the bend in the Q_{oss} curve of the CoolMOS™ PFD7 and P7 happens to be at about 25 V, aligned with the one in the E_{oss}. This bend is of interest because it represents the point where the output capacitance of the MOSFET transitions from being extremely low to being extremely high. This means that the amount of electric charge which needs to be removed to reduce the V_{DS} from 400 V to 25 V is much lower than the one from 25 V to 0 V.

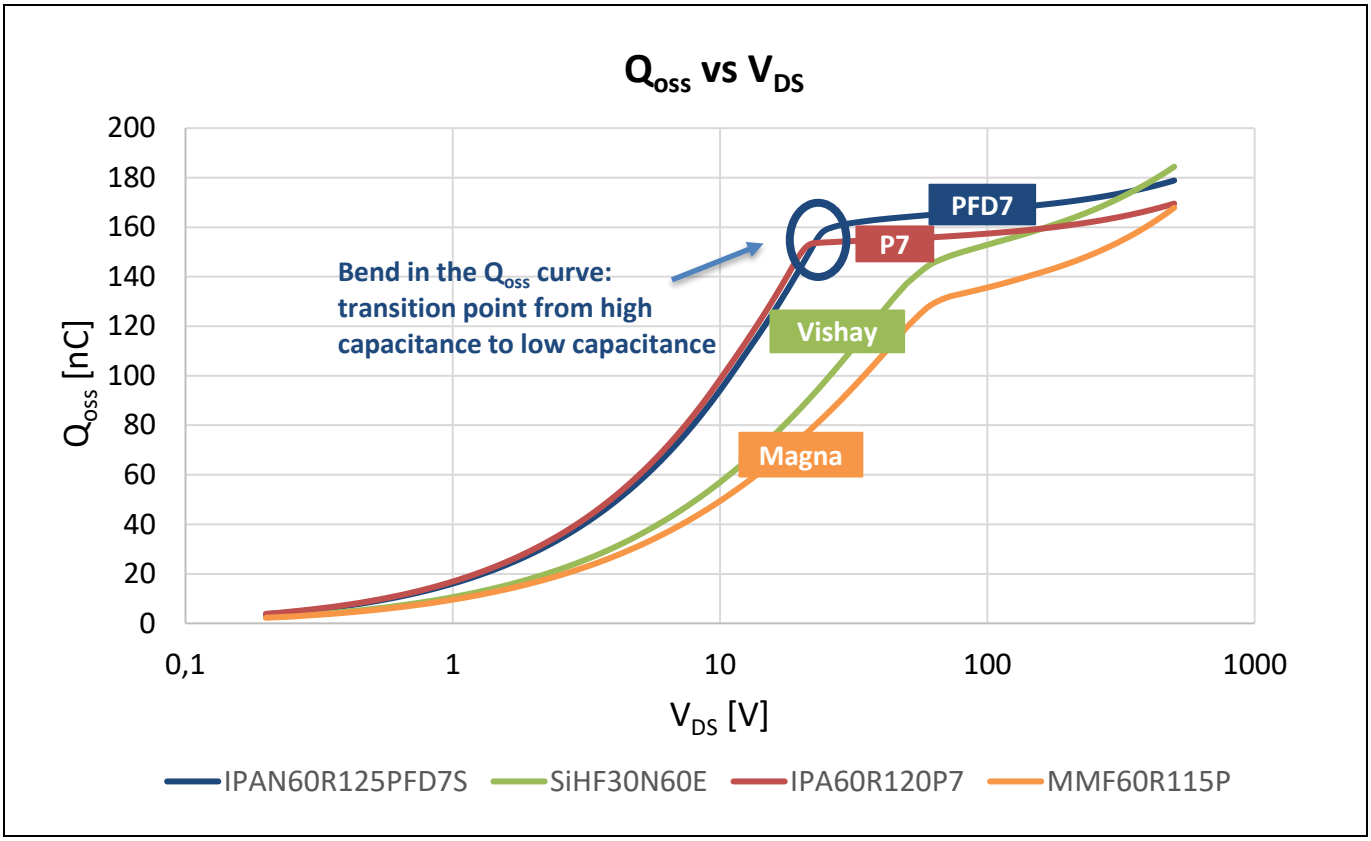


Figure 8 **Q_{oss} comparison between CoolMOS™ PFD7, P7 and competitors**

For instance, let's consider the following example design, based on the FFR Flyback concept described in [1]:

Table 2 **Specifications and parameters of adapter design considered based on FFR Flyback concept**

Specification	Symbol	Value
Nominal output power	$P_{out,n}$	65 W
Input voltage range	$V_{in,ac}$	90 V_{rms} to 264 V_{rms}
Output voltage	V_{out}	20 V
Magnetizing inductance	L_m	110 mH
Transformer turns ratio	n	5
Primary-side MOSFET	–	IPAN60R125PFD7S

The method which will be used in this document to calculate the amount of current required for partial and full ZVS is explained in [4].

Let's calculate the amount of negative current required to achieve partial and full ZVS for the 125 mΩ CoolMOS™ PFD7 under the assumption of operating at the nominal high line voltage of 230 V_{rms}.

In this case the maximum voltage blocked by the MOSFET is equal to:

$$V_{DS,max} = V_{in,HL,nom} + n \cdot V_{out} = \sqrt{2} \cdot 230\ V + 5 \cdot 20\ V = 426\ V$$

Now it is possible to compute the amount of charge that needs to be removed from the output capacitance of the MOSFET in order to achieve partial and full ZVS respectively:

$$Partial\ ZVS\ (25\ V) \rightarrow Q_{oss}(426\ V) - Q_{oss}(25\ V) = 177\ nC - 159\ nC = 18\ nC$$

$$Full\ ZVS\ (0\ V) \rightarrow Q_{oss}(426\ V) - Q_{oss}(0\ V) = 177\ nC - 0\ nC = 177nC$$

It is worth to mention that in order to discharge the C_{oss} from 426 V to 25 V is enough to remove only 10% of the Q_{oss}(426 V).

Knowing the amount of charge to be removed, it is possible to calculate the amount of negative current required to reach the desired ZVS level rearranging the following equation:

$$E_{oss}(V_{Coss,in}) + \frac{1}{2} \cdot L_m \cdot I_{Lm,neg}^2 = E_{oss}(V_{Coss,fin}) + \Delta Q_{oss} \cdot V_{in,HL,nom}$$

Therefore we have that:

$$Full\ ZVS \rightarrow\ 4.4\ \mu J + \frac{1}{2} \cdot 110\ \mu H \cdot I_{Lm,neg}^2 = 0\ \mu J + 177\ nC \cdot 325\ V$$

$$Partial\ ZVS \rightarrow\ 4.4\ \mu J + \frac{1}{2} \cdot 110\ \mu H \cdot I_{Lm,neg}^2 = 1.46\ \mu J + 18\ nC \cdot 325\ V$$

Solving by $I_{Lm,neg}$ we obtain:

$$Full\ ZVS\ (25\ V) \rightarrow I_{Lm,neg} =\ 983\ mA$$

$$Partial\ ZVS\ (0\ V) \rightarrow I_{Lm,neg} = 230\ mA$$

Opting for partial ZVS instead of full ZVS the amount of negative magnetizing current required is less than one fourth. This helps reducing not only the RMS current flowing through the primary side switch but also the RMS current flowing through the transformer and through the synchronous rectifier (SR), leading to an efficiency benefit at system level.

Now, keeping the same amount of negative current calculated for the partial ZVS of PFD7 ($I_{Lm,neg}$=230 mA), a simulation has been run to evaluate at which voltage and subsequent E_{oss} the part MMF60R115P from the competitor Magna is turned on. The simulation results are shown in Figure 9: it can be seen that, using the same amount of negative magnetizing current current $I_{Lm,neg}$ for both parts, the PFD7 V_{DS} valley is, as expected 25 V, while for the competitor part it is 80 V.

As shown in Table 3, this results in an E_{oss} 200% higher for the competitor device compared to PFD7, leading to higher switching losses.

Furthermore Figure 9 shows also that the competitor device requires longer time to reach the V_{DS} valley (190 ns vs. 120 ns) forcing the designer to extend the dead time setting.

Table 3 Comparison of turn-on V_{DS} and of E_{oss} dissipated at turn-on between IPAN60R125PFD7S and competitor device MMF60R115P in partial ZVS conditions ($I_{mag,neg}$ = 263 mA)

Part number	Turn-on drain-source voltage	E_{oss} dissipated at turn-on
IPAN60R125PFD7S (Infineon PFD7)	25 V	1.46 µJ
MMF60R115P (Magna)	80 V	2.9 µJ

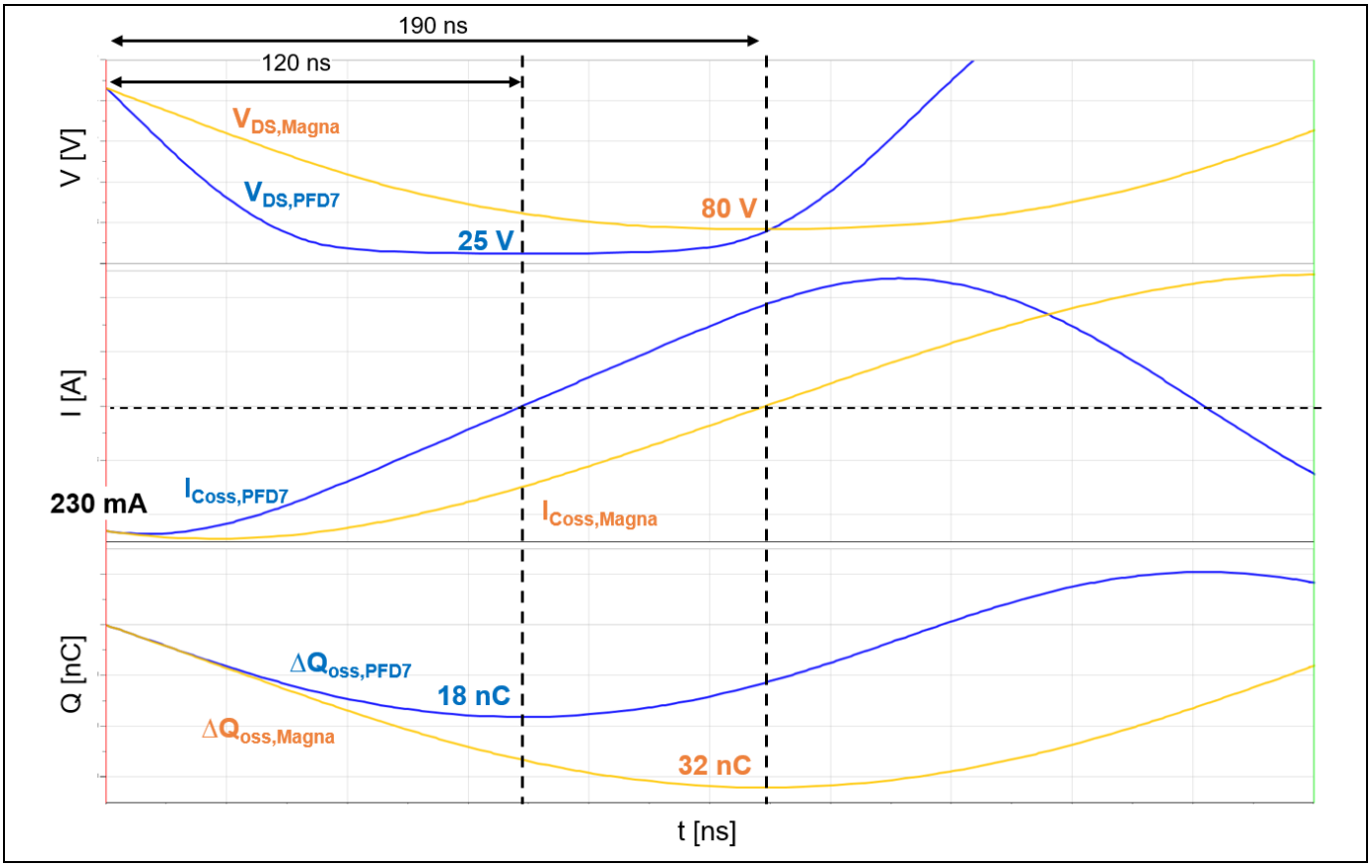


Figure 9 **Simultation results of V_{DS} transitions of IPAN60R125PFD7S and MMF60R115P assuming a negative magnetizing current $I_{Lm,neg}$ = 230 mA**

2.2.3 Reverse recovery charge (Q_{rr})

The 600 V CoolMOS™ PFD7 features a best-in-class fast body diode with ultra-low reverse recovery charge (Q_{rr}). Figure 10 shows that the PFD7 body diode has a Q_{rr} that is 82 percent lower than the CoolMOS™ P7.

The tremendous Q_{rr} reduction greatly improves the reliability of the final application, making it rugged against hard commutation on the conducting body diode, thus drastically reducing the risk of field failure.

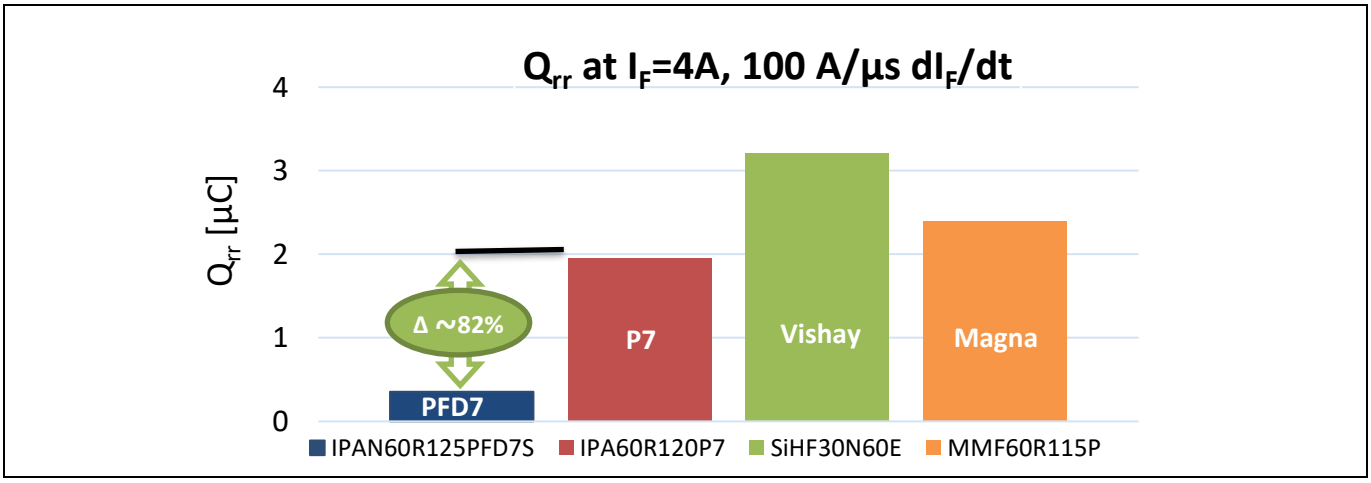


Figure 10 **Reverse recovery charge comparison between PFD7, P7 and two competitor parts in the 120 mΩ $R_{DS(on)}$ class**

In principle, all half-bridge-based topologies are susceptible to hard commutation on the conducting body diode; however, when using SJ MOSFETs, this is avoided by selecting the proper modulation scheme. This is the reason (together with the need for ZVS) why high-density adapters based on the half-bridge topology are typically operated in Critical Conduction Mode (CrCM). In the ACF, for instance, as explained in 1.1.1.1, during normal operation, the low-side MOSFET is turned on only after the magnetizing current has become negative. This ensures that the body diode of the high-side MOSFET is not conducting when the low-side is turned on, avoiding the risk of hard commutation. Under abnormal conditions such start-up and output short-circuit, however, the converter may transiently operate in Continuous Conduction Mode (CCM), causing hard commutation on the conducting body diode of the high-side MOSFET (Figure 11). Differently from all the other MOSFETs shown in Figure 10, CoolMOS™ PFD7, thanks to its extremely low Q_{rr}, is rugged against hard commutation, making the risk of field failure minimal.

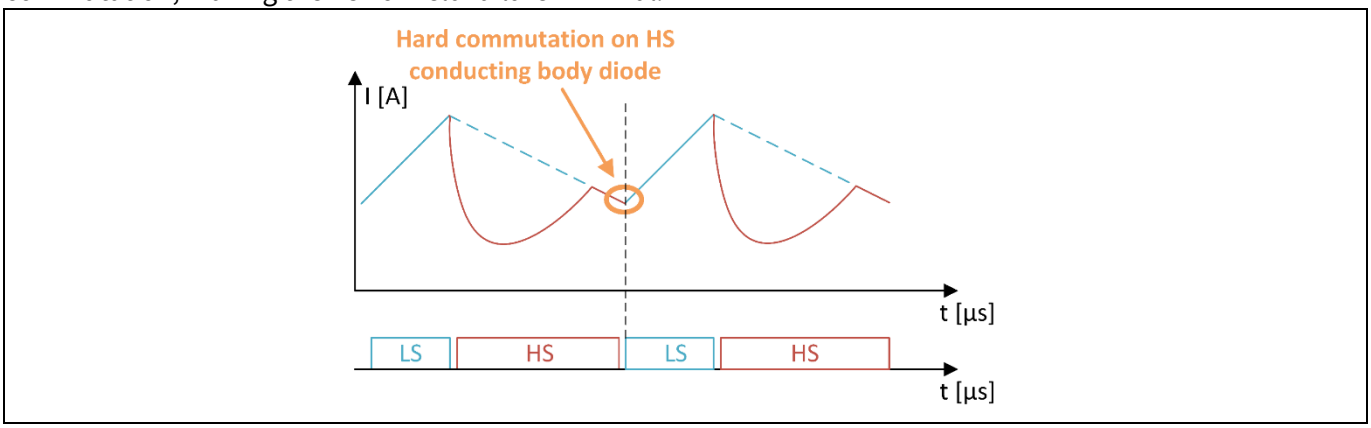


Figure 11 **Example of hard commutation on the high-side body diode in an ACF. Blue full line: LS MOSFET current, red full line: HS MOSFET current, blue line: magnetizing current during demagnetization phase.**

2.2.4 Turn-off losses (E_{off})

The E_{off} represents the losses dissipated by a MOSFET during a hard turn-off event (turn-off commutation with non-zero current). The 600 V CoolMOS™ PFD7 shows a turn-off energy similar to P7 and ~38 percent lower than the best competitor, Vishay.

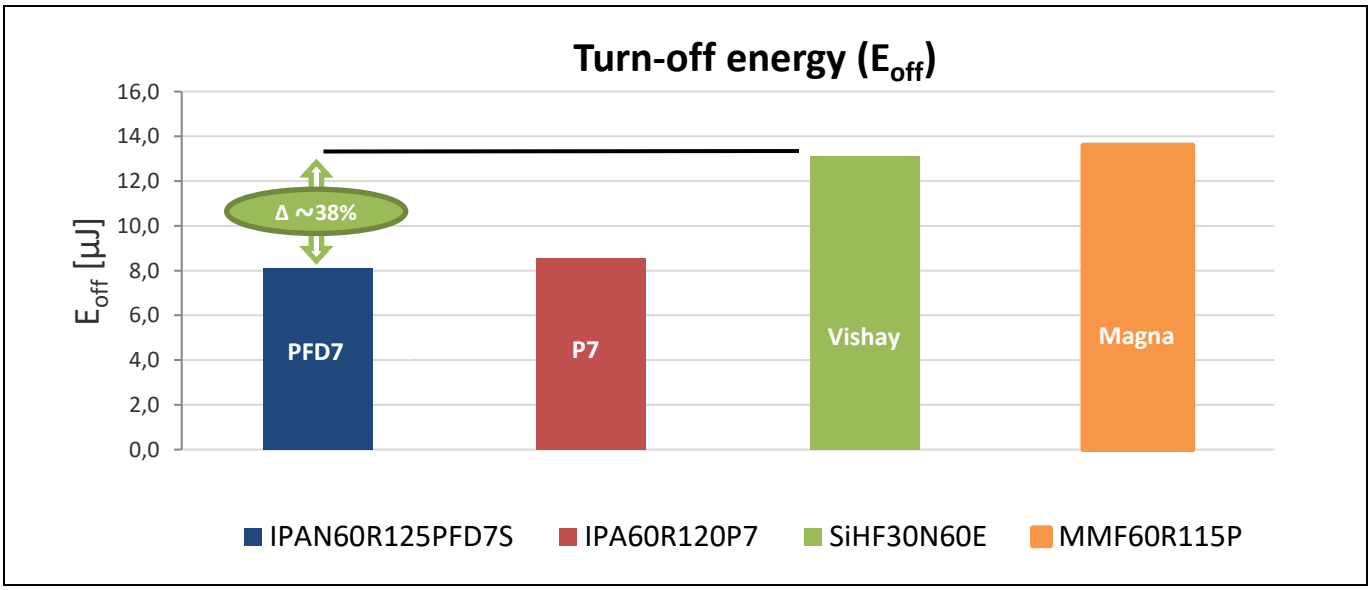


Figure 12 **E_{off} comparison between PFD7, P7 and competitors in the 120 mΩ $R_{DS(on)}$ class. $R_{g,off,ext}$ = 1.8 Ω, I_d = 4 A.**

2.2.5 $R_{DS(on)}$ temperature dependency

The $R_{DS(on)}$ typical and maximum values specified at 25°C in the datasheet may be misleading, since in most of the applications MOSFETs are operated at much higher temperatures. Figure 13 shows that the 600 V CoolMOS™ PFD7 features a lower $R_{DS(on)}$ increase with the junction temperature T_j, resulting in a 5 percent lower $R_{DS(on)}$ value at 80°C with respect to the best competitor, thus improving the efficiency in the mid and full-load range.

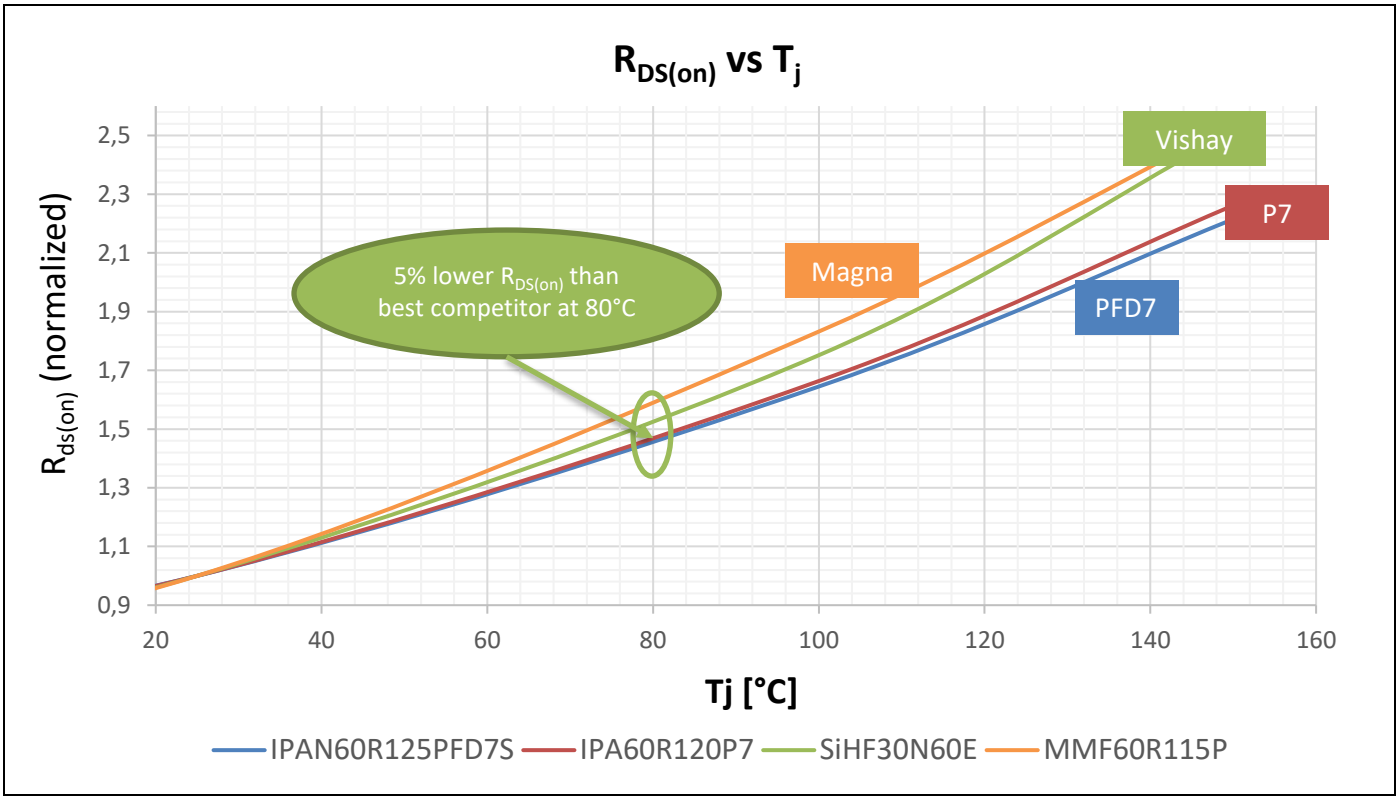


Figure 13 Normalized $R_{DS(on)}$ vs junction temperature T_j for PFD7, P7 and competitors

2.2.6 C_{oss} hysteresis losses ($E_{oss,hys}$)

As already explained in 1.1.1, in order to operate efficiently at the relatively high switching frequencies typically utilized in high-density adapters, soft-switching techniques are a must. Soft-switching techniques enable operation of the device in ZVS, meaning that the MOSFET is turned on only after its drain-source voltage has reached 0 V (or a value close to 0 V). This strategy eliminates the turn-on losses of the device, which are typically the largest contribution to the overall switching losses. Unfortunately, all HV SJ MOSFETs suffer from an additional type of losses due to the “non-lossless” behavior of the output capacitance. This means that when the MOSFET output capacitance (C_{oss}) is charged and subsequently discharged some energy is lost, so even when operating in ZVS conditions, the entire energy stored in the output capacitance (E_{oss}) is not recovered. This phenomenon is related to the hysteretic behavior of the C_{oss}, which can be observed performing a C_{oss} charge/discharge cycle with a large signal measurement, as shown in Figure 14. This is the reason why these losses are commonly known as C_{oss} hysteresis losses, in short $E_{oss,hys}$.

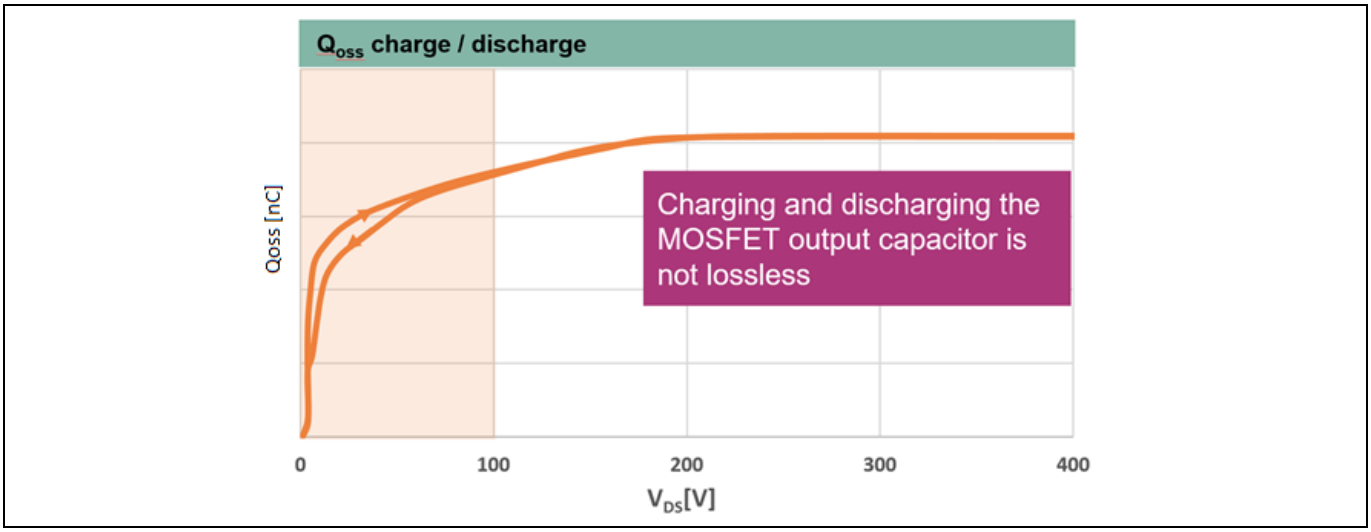


Figure 14 Q_{oss} charge/discharge cycle of a SJ MOSFET

The power dissipation originated by the loss mechanism depends on:

- **Technology:** For the same chip size, thus $R_{DS(on)}$, different technologies show different $E_{oss,hys}$, as for instance CoolMOS™ PFD7 and CoolMOS™ P7.
- **Breakdown voltage:** For the same technology $E_{oss,hys}$ increases with the voltage class, meaning that typically a 650 V device shows higher $E_{oss,hys}$ than a 600 V device based on the same technology.
- **Switching frequency f_{sw}:** Since the charge and discharge cycle of the C_{oss} happens one time per switching cycle, the power dissipation orginated by this loss mechanism is proportional to the switching frequency (f_{sw}).
- **$R_{DS(on)}$ class:** Affecting the C_{oss} of the device, this loss is also dependent on the chip size, meaning that, for the same technology, MOSFETs with lower $R_{DS(on)}$ will show higher $E_{oss,hys}$ losses.

The 600 V CoolMOS™ PFD7 features 41 percent less C_{oss} hysteresis losses with respect to P7, offering a significant efficiency improvement in soft-switching applications.

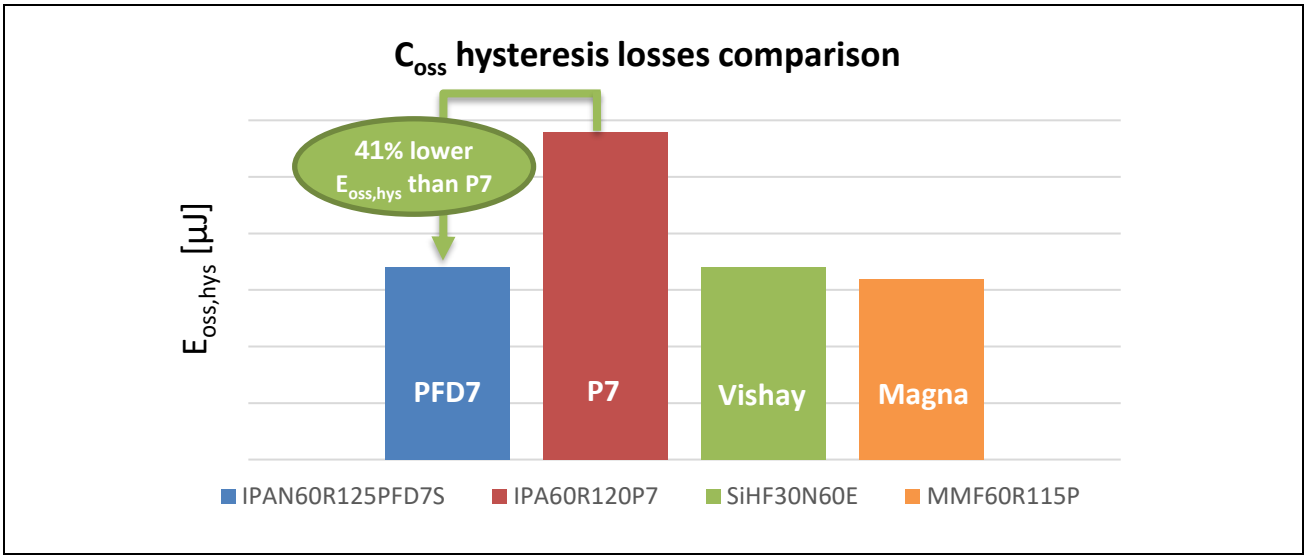


Figure 15 C_{oss} hysteresis losses comparison between PFD7, P7 and two competitor devices in the 120 mΩ $R_{DS(on)}$ class

Figure 16 shows the impact of the different loss mechanisms to the overall losses of the high-side and low-side MOSFET in a 65 W adapter based on the ACF topology at low-line, full load. The ZVS has been optimized to reduce the overall system losses, turning on the LS MOSFET at 25 V, while the high-side operates in full ZVS. It can be observed that, when using the CoolMOS™ P7, the C_{oss} hysteresis losses account for 44 percent of the total MOSFET loss (high-side + low-side) at low-line which, as already mentioned, is the most critical operating point for adapters from the thermal standpoint. By replacing the CoolMOS™ P7 with the PFD7 the overall device losses are reduced by 22 percent.

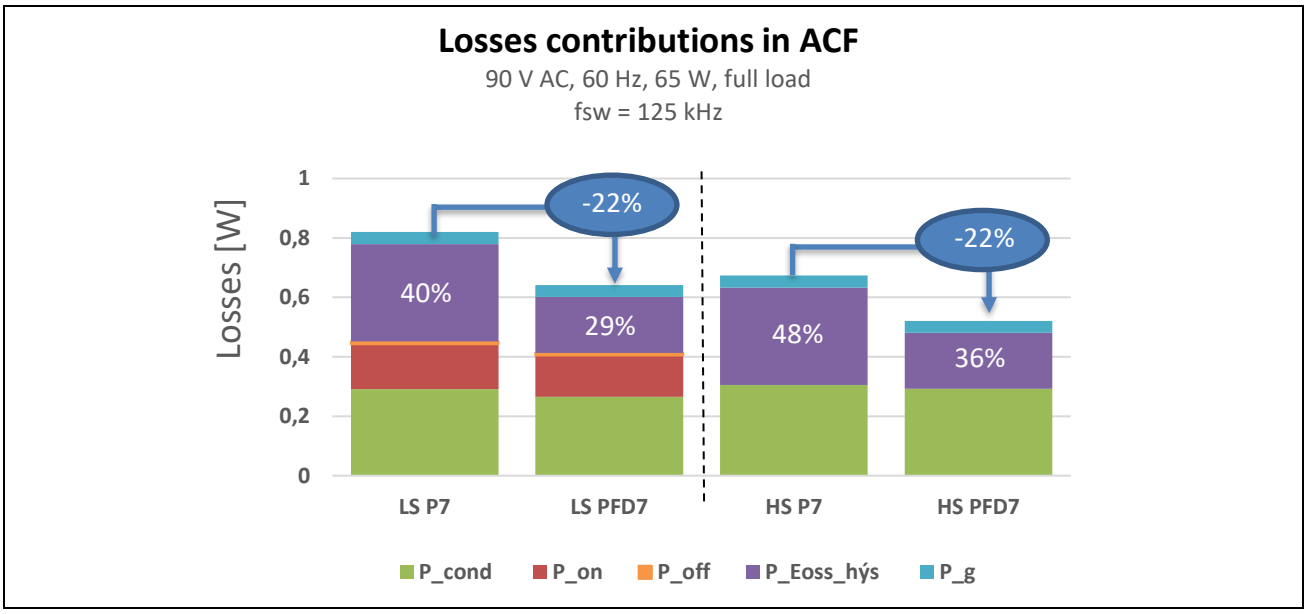


Figure 16 **Comparison of different loss contributions to the overall MOSFET losses between IPAN60R120P7 and IPAN60R125PFD7S in an ACF. Abbreviations: conduction losses (P_{cond}), turn-on losses (P_{on}), turn-off losses (P_{off}), C_{oss} hysteresis losses ($E_{oss,hys}$) and driving losses (P_g).**

3 Application measurements

3.1 65 W high-density adapter

Figure 17 shows a comparison of the relative efficiency measurements in an ACF board of the CoolMOS™ PFD7, P7 and two competitors at low-line, full-load. The average operating switching frequency of the board is around 155 kHz at low-line. Replacing the CoolMOS™ P7 with the PFD7 provides a significant efficiency advantage of 0.34 percent at low-line (90 V_{ac}), which is typically the condition defining the maximum achievable power density, due to thermal limitations.

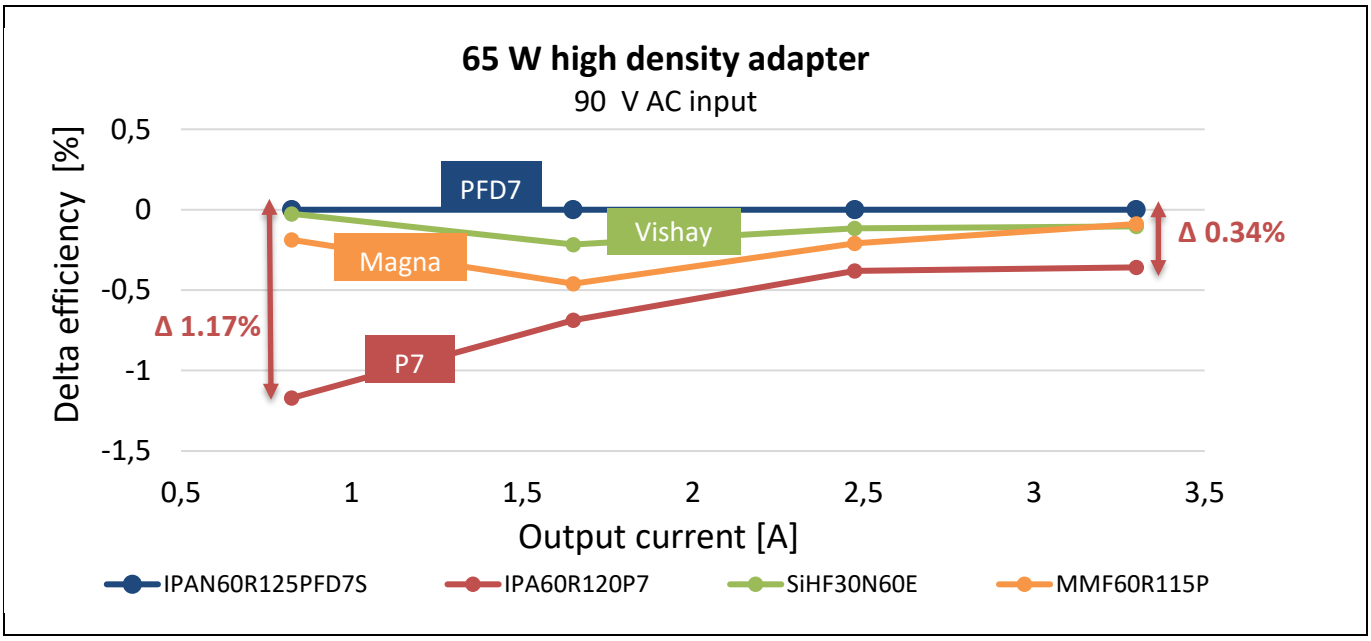


Figure 17 Relative efficiency comparison PFD7, P7 and two competitor parts in the 120 mΩ $R_{DS(on)}$ class at low-line (90 V_{ac}, 60 Hz)

As a result, replacing the CoolMOS™ P7 with the PFD7 enables reduction of the MOSFET temperature by 5°C (Figure 18), reducing the risk of a hotspot on the adapter case. It can be observed that the competitor parts exhibit lower case temperature despite providing a full-load efficiency slightly lower than CoolMOS™ PFD7. This is due to the fact that both competitor parts have a significantly bigger chip size resulting in a lower thermal resistance.

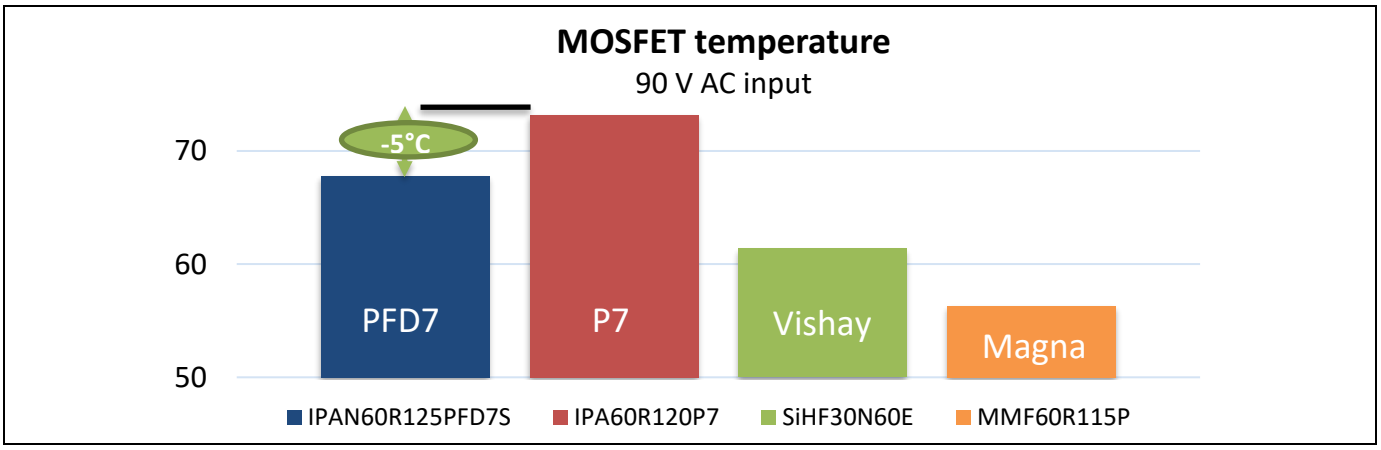


Figure 18 MOSFET case temperature comparison between PFD7, P7 and competitor parts in the 120 mΩ $R_{DS(on)}$ class at low-line (90 Vac, 60 Hz)

Figure 19 shows the power density limits enabled by the CoolMOS™ PFD7 and P7, assuming a maximum adapter case temperature of 70°C. Thanks to the improved efficiency, PFD7 pushes the maximum power density limit above 20 W/in^3, increasing it by 1.8 W/in^3 compared to P7.

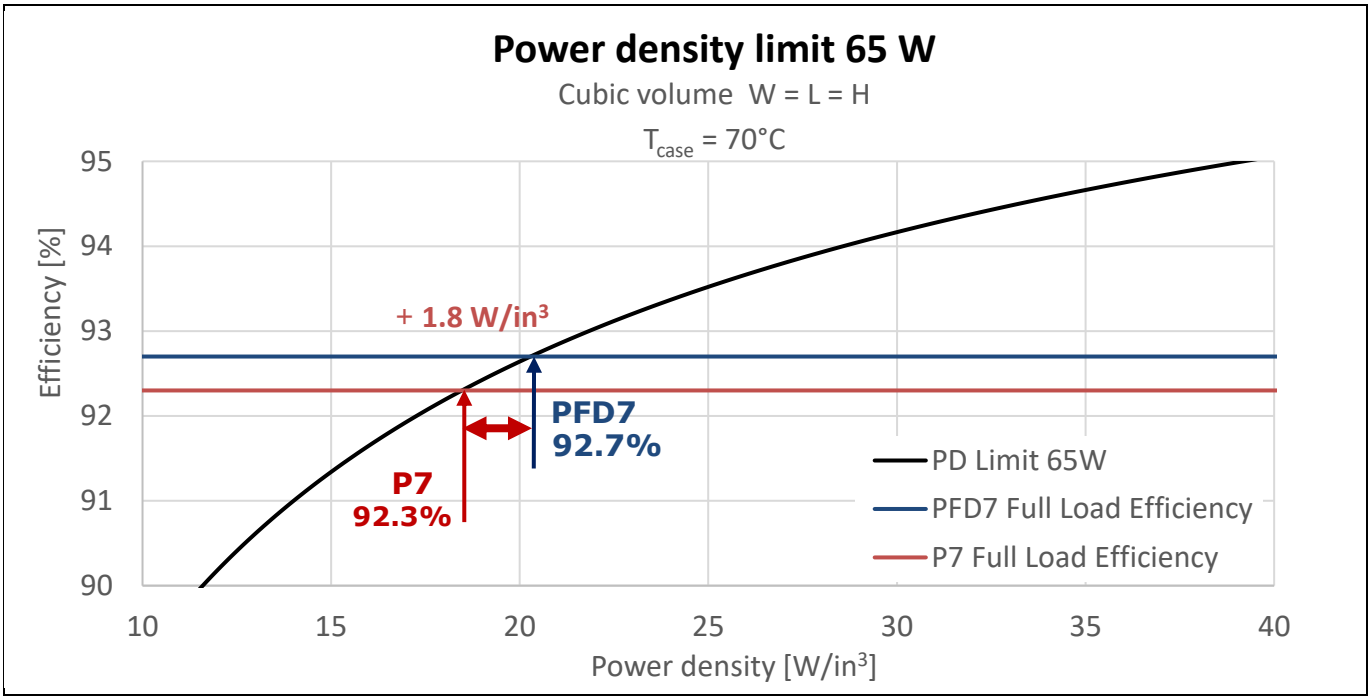


Figure 19 Maximum achieveable power density enabled by CoolMOS™ IPAN60R125PFD7S and IPA60R120P7

3.2 100 W motor drive application board

Figure 20 shows the tremendous efficiency benefit provided by the 600 V CoolMOS™ PFD7 in comparison to CE in a 100 W motor drive application board. The PFD7 enables higher efficiency over the entire load range reaching up to 2 percent improvement at full load.

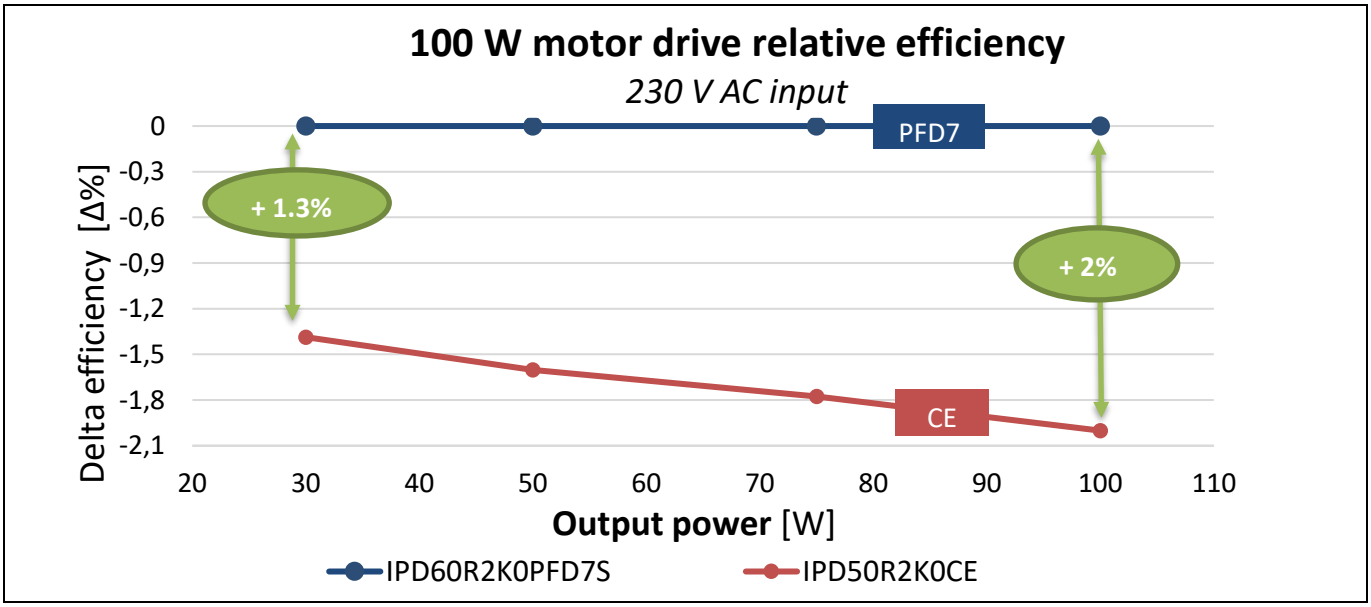


Figure 20 Relative efficiency comparison between CoolMOS™ PFD7 and CE in a 100 W motor drive application board in the 2 Ω $R_{DS(on)}$ class

As a result, using the PFD7 means the case temperature is 18.2°C lower than with CE, as shown in Figure 21.

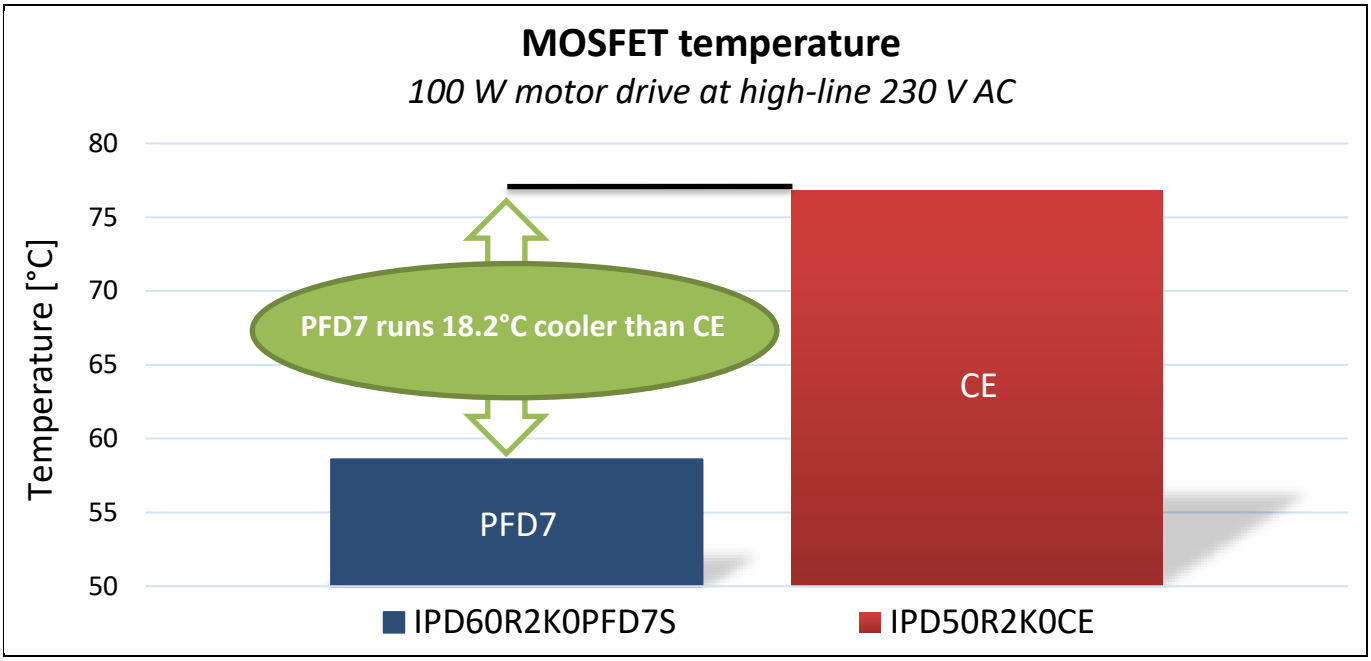


Figure 21 Comparison of the low-side MOSFET case temperature between CoolMOS™ PFD7 and CE

The technology parameters that enable such an outstanding efficiency improvement are as follows:

- Reduced turn-on losses thanks to 86 percent lower Q_{rr} and 35 percent lower E_{oss} compared to CoolMOS™ CE
- Reduced turn-off losses
- Lower $R_{DS(on)}$ increase with junction temperature T_j

For further details please refer to application note [3].

4 Design guidelines

In the following sections we will give some guidelines on how to use the CoolMOS™ PFD7 in the best way to enable optimized performance.

4.1 Minimum external gate resistor ($R_{g,ext}$)

In a well-designed power supply we recommend using an external resistor in the range of 5 to 10 Ω for turn-on and 0 Ω for turn-off. By implementing this $R_{g,ext}$ value a very good efficiency level has been achieved in combination with very smooth switching waveforms, showing limited spikes on the gate. This efficiency driven $R_{g,ext}$ selection is enabled by the implementation of an integrated gate resistance $R_{g,int}$ and the inherent robustness of the CoolMOS™ PFD7. However, the selection of external gate resistance $R_{g,ext}$ is always a function of the PCB parasitics, which may generate unexpected voltage or current peaks on the MOSFET caused by the induced voltage (L_{stray} *di/dt) and current signals ($C_{parasitics}$ *dv/dt). To prevent such peaks, a reduction of the parasitic components or an increased $R_{g,ext}$ selection is recommended.

5 Portfolio overview

As shown in Figure 22, Infineon's 600 V CoolMOS™ PFD7 portfolio includes a wide $R_{DS(on)}$ span ranging from 125 mΩ to 2 Ω. Special focus has been given to SMD packages in order to help designers achieve the highest power density with best-in-class $R_{DS(on)}$ in both ThinPAK 5x6 and SOT-223 packages.

CoolMOS™ PFD7 600V – portfolio overview

$R_{DS(ON)}$ [mΩ]	 TO-220FP_NL PG-TO220-3-319	 IPAK SL PG-TO251-3-346	 DPAK PG-TO252-3-344	 SOT-223 PG-SOT223-3-1	 ThinPak 5x6 PG-TDSON-8-52
2000			IPD60R2K0PFD7S	IPN60R2K0PFD7S	
1500			IPD60R1K5PFD7S	IPN60R1K5PFD7S	IPLK60R1K5PFD7
1000		IPS60R1K0PFD7S	IPD60R1K0PFD7S	IPN60R1K0PFD7S	IPLK60R1K0PFD7
600		IPS60R600PFD7S	IPD60R600PFD7S	IPN60R600PFD7S	IPLK60R600PFD7
360	IPAN60R360PFD7S	IPS60R360PFD7S	IPD60R360PFD7S	IPN60R360PFD7S	IPLK60R360PFD7
280	IPAN60R280PFD7S	IPS60R280PFD7S	IPD60R280PFD7S		
210	IPAN60R210PFD7S	IPS60R210PFD7S	IPD60R210PFD7S		
125	IPAN60R125PFD7S				

Figure 22 600 V CoolMOS™ PFD7 portfolio

As shown above in the portfolio overview, the 600 V CoolMOS™ PFD7 is available in both SOT-223 and ThinPak 5x6 packages. The advantages provided by these packages are two-fold: their reduced mechanical dimensions save PCB area, enabling higher power density and reducing PCB cost.

5.1.1 SOT-223

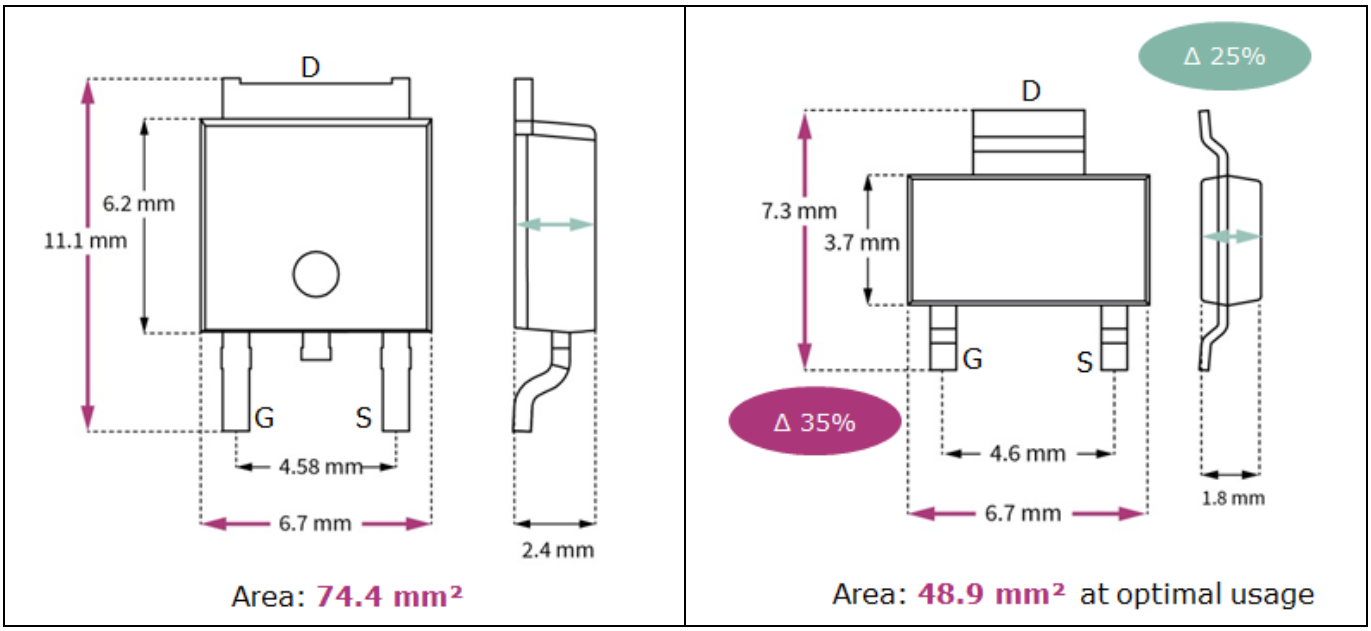


Figure 23 Package comparison of DPAK (74.4 mm² PCB area) and SOT-223 (48.9 mm²)

The 600 V CoolMOS™ PFD7 is available in SOT-223 for $R_{DS(on)}$ starting from 360 mΩ.

A SOT-223 package can be a direct pin-to-pin replacement for a DPAK package with the outer dimensions and lead spacing shown in Figure 23.

This cost-effective package offers direct pin-to-pin compatibility to DPAK without suffering any large thermal limitations when using the DPAK footprint for SOT-223. It features the smallest geometry per $R_{DS(on)}$ (drain-source on-state resistance) and reduces the overall Bill of Materials (BOM) cost of an application as much as possible.

It is important to keep in mind that the temperature and the maximum power dissipation allowed by this package are influenced by the ambient temperature, PCB temperature and PCB copper area.

For a comprehensive description of the SOT-223 package please refer to application note [6].

5.1.2 ThinPAK 5x6

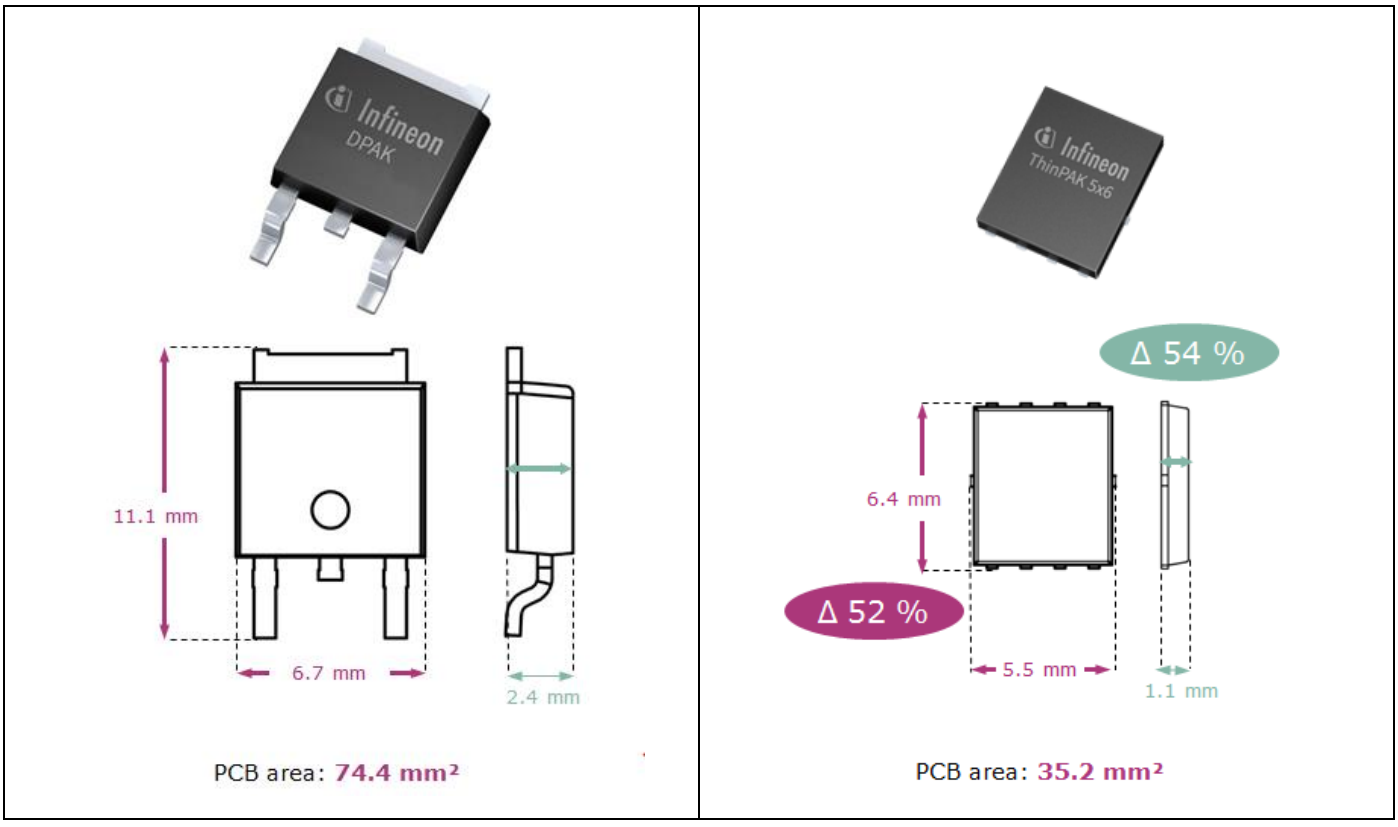


Figure 24 Package comparison of DPAK (74.4 mm² PCB area) and ThinPAK 5x6 (35.2 mm²)

The 600 V CoolMOS™ PFD7 is available in ThinPAK 5x6 for $R_{DS(on)}$ starting from 360 mΩ.

During the development phase of a power supply the design engineer must take into account three important aspects:

- Power density
- Signal integrity
- Manufacturability

The ThinPAK 5x6 addresses all the points above, offering:

- **Reduced mechanical dimensions:** In Figure 24 it can be seen that the overall mechanical dimensions of the ThinPAK 5x6 package offer an improvement when compared to the DPAK package. The PCB area usage is reduced by 52 percent and the overall height of the package is reduced by 54 percent, or to only 1.1 mm. This package height is particularly favourable, because the typical lead trimming height required on the bottom side of a PCB when using a standard low-cost configuration with through-hole components on the top and SMD components on the bottom is between 1 mm and 1.5 mm.
- **Reduced package parasitics in combination with a Kelvin source connection:** The ThinPAK 5x6 features reduced package parasitics combined with a Kelvin source connection enabling cleaner and faster switching waveforms, which improve the full-load efficiency.
- **Improved manufacturing flexibility:** The ThinPAK 5x6 has exposed leads, which makes it compatible with wave-soldering exposure and additionally allows for Automated Optical Inspection (AOI) to ensure that the pads of the device have been soldered correctly. This helps to reduce fallout in mass production.

It is important to keep in mind that the temperature and the maximum power dissipation allowed by this package are influenced by the ambient temperature, PCB temperature and PCB copper area.

For a comprehensive description of the ThinPAK 5x6 package please refer to application note [7].

6 Conclusions

This document described Infineon's latest HV SJ 600 V CoolMOS™ PFD7 MOSFET technology, with the following key features:

1. **Best-in-class performance for target markets**
   - Significant reduction of C_{oss} hysteresis losses (-41 percent compared to P7)
   - Reduced recovery charge Q_{rr} (-96 percent compared to CE)
   - Enables high power density
2. **"Ease-of-use" and state-of-the-art**
   - Very low ringing tenedency
   - Best-in-class body diode enables increased performance and reliability
   - Smooth switching waveforms
   - Excellent ESD robustness greater than 2 kV (HBM) for $R_{DS(on)}$ greater than or equal to 280 mΩ
3. **Best-in-class from a commercial standpoint**
   - Best-in-class price–performance ratio
   - 25 parts in five packages
   - Increased $R_{DS(on)}$ coverage from 125 mΩ to 2 Ω
   - Focus on new SMD packages (ThinPAK 5x6, SOT-223)
   - Available in industrial and standard grade packages
   - Suitable for high-density chargers/adapters and low-power motor drives

Furthermore, efficiency improvement with respect to P7 and CE has been demonstrated through measurements in target applications.

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Document version	Date of release	Description of changes

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