

## R9A02G011

ASSP (USB Power Delivery Controller)

R19DS0088EJ0130

Rev.1.30

Jan. 29, 2019

## 1. OVERVIEW

The R9A02G011 is a USB Power Delivery Controller that is based on the Universal Serial Bus (USB) Power Delivery Specification Revision 3.0 and USB Type-C™ Cable and Connector Specification Revision 1.3. The R9A02G011 performs negotiation for more current and/or higher voltages over the USB cable (VBUS) than are defined in the USB2.0, USB3.0 or BC1.2 specifications, and controls circuitry to select local power source or power sink. The R9A02G011 uses a 300kbps BMC modulated signal through the CC wire in the USB Type-C™ cable. It comes in a small 32-pin QFN package and integrates several commonly required external components, making it ideally suited for applications with limited PCB space. In addition, the R9A02G011 incorporates Renesas' low-power technologies.

### 1.1 Features

- Compliant with USB Power Delivery Specification Revision 3.0 and USB Type-C™ Cable and Connector Specification Revision 1.3.
  - Certified by USB Implementers Forum: TID= 1061007 (Silicon), 1020074 (E-marker)
  - Supports Programmable Power Supply
  - Supports IEC63002
  - Supports up to 260 bytes data transfer
  - Supports all USB Type-C™ Connection State Diagrams for USB Type-C™ port control
- Compliant with USB Power Delivery Specification Revision 2.0
  - Certified by USB Implementers Forum: TID=1000004 (Silicon), 1020073 (E-marker)
  - Supports alternate mode and electronically marked cables
  - Supports Dual Role operation and Role Swap protocol
  - Supports Dead Battery operation
- Single Power Supply with wide voltage range from 3.0 to 5.5V
- Integrated CC-PHY and CC-logic
- On-chip Flash ROM
- On-chip Oscillator
- On-chip Power-On-Reset (POR) circuit
- Small Footprint
  - Small and low pin count package with simple pin assignment for PCB layout
  - Integration of many peripheral components
- Supports SMBus Master and Slave interfaces
- Suitable for Energy Star and EuP specifications for low-power PC peripheral systems.

### 1.2 Applications

AC Adapter, Power outlet, USB PD Hub, PC, Tablet, Smartphone, Docking Station, PC Peripheral Device (Monitor, Printer, Router, External HDD), Consumer Electronics (DTV, STB, Home Gateway), etc.

### 1.3 Ordering Information

| Part Number      | Package               | Remark            |
|------------------|-----------------------|-------------------|
| R9A02G011GNP#AC0 | 32-pin QFN (5 × 5 mm) | Lead-free product |

### 1.4 Block Diagram

Figure 1-1. R9A02G011 Block Diagram

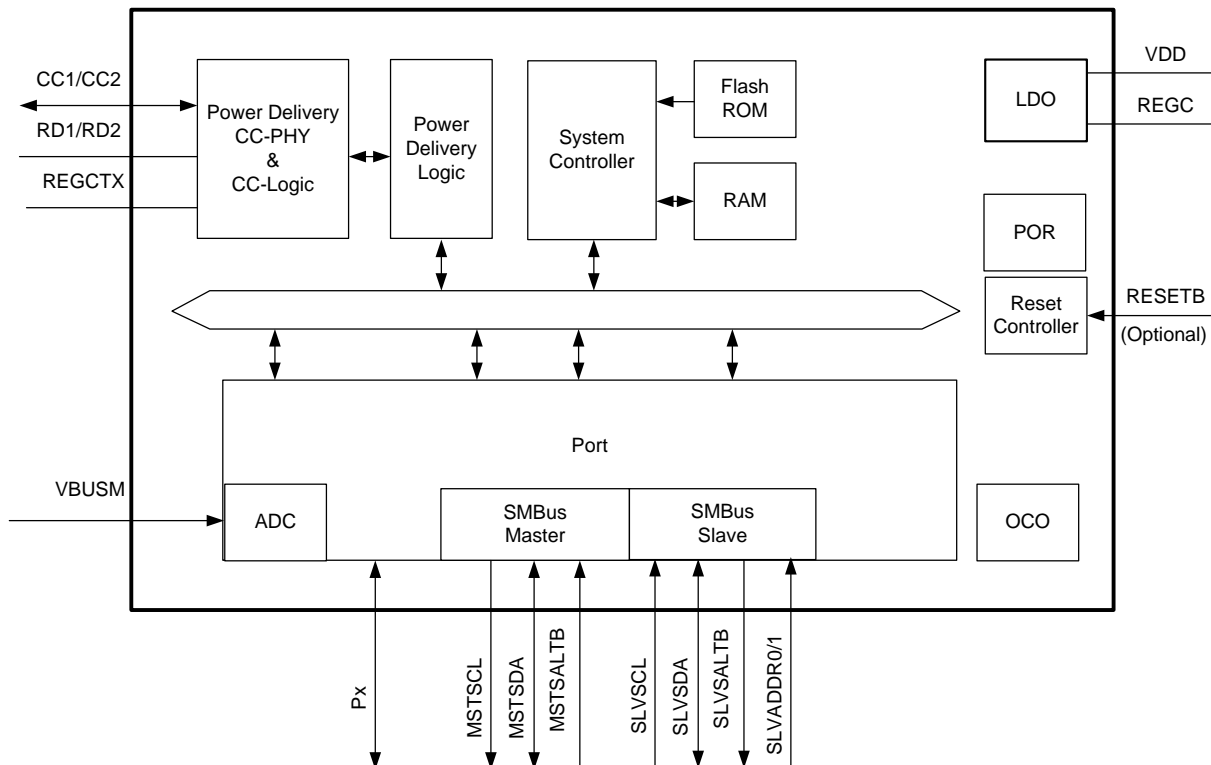


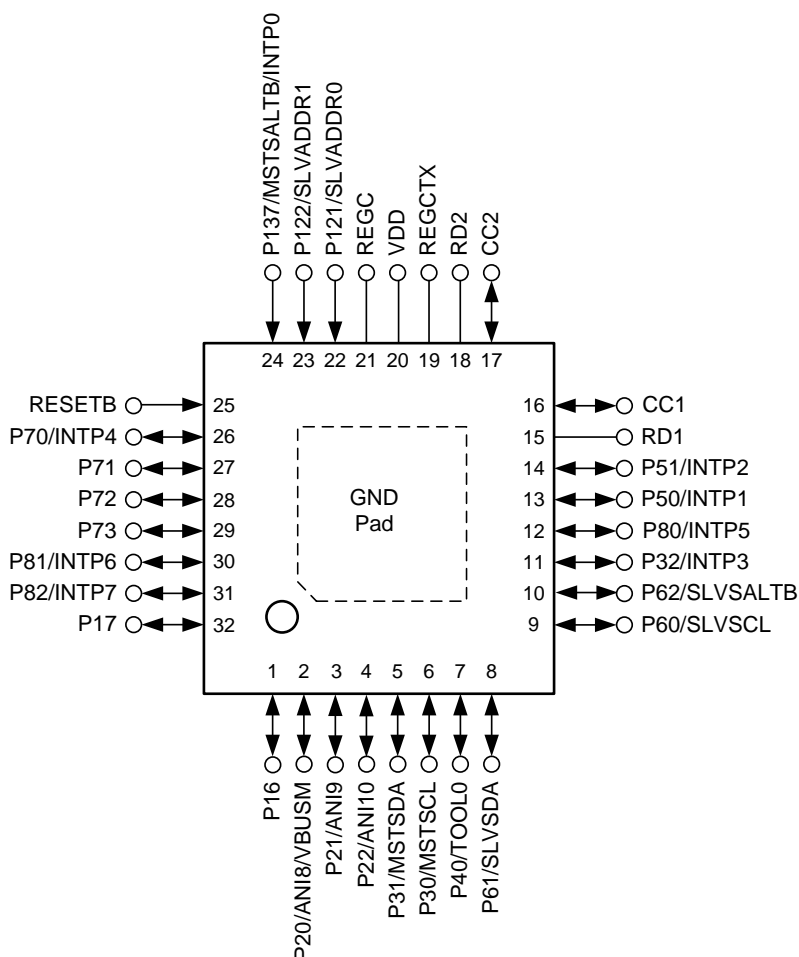
Table 1-1. Terminology

| Block Name                    | Description                                       |
|-------------------------------|---|
| Power Delivery CC-PHY & Logic | CC-PHY (Tx/Rx), CC-logic, and LDO used for CC-PHY |
| Power Delivery Logic          | Power Delivery logic controller                   |
| System Controller             | System CPU core (RL78)                            |
| Flash ROM                     | Internal Flash ROM                                |
| RAM                           | Internal SRAM                                     |
| SMBus Slave                   | Interface signals to external SMBus Master.       |
| SMBus Master                  | Interface signals to external SMBus Slave.        |
| Port                          | Controls Port I/O signals                         |
| OCO                           | On-Chip Oscillator                                |
| POR                           | Internal Power-On-Reset circuit                   |
| Reset Controller              | External reset signal (Optional)                  |
| ADC                           | AD Converter                                      |
| LDO                           | Low Drop Out regulator integrated in this IC      |

### 1.5 Pin Configuration

- 32-pin QFN (5 × 5 mm)

Figure 1-2. Pin Configuration of R9A02G011 32-pin QFN (Top View)



## 2. PIN FUNCTION

This section describes each pin's function.

### 2.1 Power supply

| Pin Name | Pin No. | I/O Type | Function  |
|----------|---------|----------|---|
| VDD      | 20      | Power    | Power supply (from 3.0V to 5.5V)  |
| REGCTX   | 19      | Power    | Regulator capacitance for CC-PHY. Connecting regulator output stabilization capacitance for internal operation. |
| REGC     | 21      | Power    | Regulator capacitance. Connecting regulator output stabilization capacitance for internal operation.            |
| GND      | Die Pad | -        | Ground  |

### 2.2 System Interface Pins

| Pin Name | Pin No. | I/O Type | Function                    |
|----------|---------|----------|-----------------------------|
| RESETB   | 25      | IN       | Chip Reset Input (L active) |

### 2.3 USB PD and Type-C™ Port Pins

| Pin Name | Pin No. | I/O Type | Function  |
|----------|---------|----------|---|
| RD1      | 15      | I/O      | Rd resistor 1, Analog pin from CC-PHY.          |
| CC1      | 16      | I/O      | Configuration Channel 1, Analog pin from CC-PHY |
| CC2      | 17      | I/O      | Configuration Channel 2, Analog pin from CC-PHY |
| RD2      | 18      | I/O      | Rd resistor 2, Analog pin from CC-PHY           |

### 2.4 I/O Port Pins

| Pin Name | Pin No. | I/O Type | During reset | After reset | Function                |
|----------|---------|----------|--------------|-------------|-------------------------|
| P16      | 1       | I/O      | Input        | Input       | Port 1, 2 bit I/O port. |
| P17      | 32      | I/O      | Input        | Input       | Port 1, 2 bit I/O port. |

| Pin Name | Pin No. | I/O Type | During reset | After reset      | Function  |
|----------|---------|----------|--------------|------------------|---|
| P20      | 2       | I/O      | Input        | Input            | Port 2, 3 bit I/O port.<br>It is also configurable as VBUSM or ANI8         |
| P21      | 3       | I/O      | Input        | Input            | Port 2, 3 bit I/O port.<br>It is also configurable as ANI9                  |
| P22      | 4       | I/O      | Input        | Input            | Port 2, 3 bit I/O port.<br>It is also configurable as ANI10                 |
| P30      | 6       | I/O      | Input        | Input            | Port 3, 3 bit I/O port.<br>It is also configurable as MSTSCL.               |
| P31      | 5       | I/O      | Input        | Input            | Port 3, 3 bit I/O port.<br>It is also configurable as MSTSDA                |
| P32      | 11      | I/O      | Input        | Input            | Port 3, 3 bit I/O port.<br>It is also configurable as INTP3                 |
| P40      | 7       | I/O      | Input        | Input<br>Pull-up | Port 4, 1 bit I/O port.<br>It is also configurable as TOOL0                 |
| P50      | 13      | I/O      | Input        | Input            | Port 5, 2 bit I/O port.<br>It is also configurable as INTP1                 |
| P51      | 14      | I/O      | Input        | Input            | Port 5, 2 bit I/O port.<br>It is also configurable as INTP2                 |
| P60      | 9       | I/O      | Input        | Input            | Port 6, 3 bit I/O port.<br>It is also configurable as SLVSCL                |
| P61      | 8       | I/O      | Input        | Input            | Port 6, 3 bit I/O port.<br>It is also configurable as SLVSDA                |
| P62      | 10      | I/O      | Input        | Input            | Port 6, 3 bit I/O port.<br>It is also configurable as SLVSALTB              |
| P70      | 26      | I/O      | Input        | Input            | Port 7, 4 bit I/O port.<br>It is also configurable as INTP4                 |
| P71      | 27      | I/O      | Input        | Input            | Port 7, 4 bit I/O port.   |
| P72      | 28      | I/O      | Input        | Input            | Port 7, 4 bit I/O port.   |
| P73      | 29      | I/O      | Input        | Input            | Port 7, 4 bit I/O port.   |
| P80      | 12      | I/O      | Input        | Input            | Port 8, 3 bit I/O port.<br>It is also configurable as INTP5                 |
| P81      | 30      | I/O      | Input        | Input            | Port 8, 3 bit I/O port.<br>It is also configurable as INTP6                 |
| P82      | 31      | I/O      | Input        | Input            | Port 8, 3 bit I/O port.<br>It is also configurable as INTP7                 |
| P121     | 22      | IN       | Input        | Input            | Port 12, 2 bit Input port.<br>It is also configurable as SLVADDR0           |
| P122     | 23      | IN       | Input        | Input            | Port 12, 2 bit Input port.<br>It is also configurable as SLVADDR1           |
| P137     | 24      | IN       | Input        | Input            | Port 13, 1 bit Input port.<br>It is also configurable as MSTSALTB or INTP0. |

## 2.5 Alternate Functions on I/O Port Pins

I/O ports support the following alternate functions.

| Function Name  | I/O    | Function   |
|----------------|--------|--|
| ANI8 to ANI10  | Input  | Analog Input   |
| MSTSCL         | I/O    | SMBus master clock input/output (open-drain) <sup>Note 1</sup>   |
| MSTSDA         | I/O    | SMBus master data input/output (open-drain) <sup>Note 1</sup>  |
| MSTSALTB       | Input  | SMBus master alert input <sup>Note 1</sup>   |
| SLVSCL         | I/O    | SMBus slave clock input/output (open-drain) <sup>Note 2</sup>  |
| SLVSDA         | I/O    | SMBus slave data input/output (open-drain) <sup>Note 2</sup>   |
| SLVSALTB       | Output | SMBus slave alert output (open-drain)  |
| SLVADDR0       | input  | SMBus slave address bit [1] <sup>Note 2</sup>  |
| SLVADDR1       | input  | SMBus slave address bit [2] <sup>Note 2</sup>  |
| VBUSM          | Input  | VBUS voltage monitor input.<br>The pin assignment is fixed to this function.   |
| INTP0 to INTP7 | Input  | Interrupt detection input. The valid edge (rising edge, falling edge, or rising and falling edges) can be specified. |
| TOOL0          | I/O    | Data input/output for flash programming tool.<br>The pin assignment is fixed to this function.                       |

**Note 1.** The pin assignment is fixed to this function when SMBus Master is enabled.

**Note 2.** The pin assignment is fixed to this function when SMBus Slave is enabled.

## 3. ELECTRICAL SPECIFICATIONS

This chapter describes the following electrical specifications.

### 3.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings (1/2)

| Parameter              | Symbols       | Conditions  | Ratings  | Unit |
|------------------------|---------------|---|--|------|
| Supply voltage         | $V_{DD}$      |   | -0.5 to +6.5   | V    |
|                        | $V_{SS}$      |   | -0.5 to +0.3   | V    |
| REGC pin input voltage | $V_{IREGC}$   | REGC  | -0.3 to +2.8<br>and -0.3 to $V_{DD} + 0.3$ <sup>Note 1</sup> | V    |
|                        | $V_{IREGCTX}$ | REGCTX  | -0.3 to +2.8   | V    |
| Input voltage          | $V_i$         | P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82, P121, P122, P137, RESETB | -0.3 to $V_{DD} + 0.3$ <sup>Note 2</sup>                     | V    |
| Output voltage         | $V_o$         | P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82                           | -0.3 to $V_{DD} + 0.3$ <sup>Note 2</sup>                     | V    |
| Analog input voltage   | $V_{AI1}$     | ANI8 to ANI10   | -0.3 to $V_{DD} + 0.3$ <sup>Note 2</sup>                     | V    |
|                        | $V_{AI2}$     | CC1, CC2, RD1, RD2  | -0.5 to +6.5   | V    |

**Notes 1.** Connect the REGC pin to  $V_{SS}$  via a capacitor (0.47 to 1  $\mu$ F). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.**  $V_{SS}$  : Reference voltage

**Absolute Maximum Ratings (2/2)**

| Parameter                     | Symbols   | Conditions                       |  | Ratings     | Unit |
|-------------------------------|-----------|----------------------------------|--|-------------|------|
| Output current, high          | $I_{OH1}$ | Per pin                          | P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to 73, P80 to P82 | -40         | mA   |
|                               |           | Total of all pins                |  | -170        | mA   |
| Output current, low           | $I_{OL1}$ | Per pin                          | P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to 73, P80 to P82 | 40          | mA   |
|                               |           | Total of all pins                |  | 170         | mA   |
| Operating ambient temperature | $T_A$     | In normal operation mode         |  | -40 to +105 | °C   |
|                               |           | In flash memory programming mode |  |             |      |
| Storage temperature           | $T_{stg}$ |                                  |  | -65 to +150 | °C   |

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



## 3.2 Oscillator Characteristics

### 3.2.1 On-chip oscillator characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Oscillators  | Parameters | Conditions                            |  | MIN. | TYP. | MAX. | Unit |
|--|------------|---------------------------------------|--|------|------|------|------|
| High-speed on-chip oscillator clock frequency<br>Notes 1 | $f_{IH}$   |                                       |  |      | 24   |      | MHz  |
| High-speed on-chip oscillator clock frequency accuracy   |            | $-20$ to $+85\text{ }^\circ\text{C}$  | $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | -1   |      | +1   | %    |
|  |            | $-40$ to $-20\text{ }^\circ\text{C}$  | $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | -1.5 |      | +1.5 | %    |
|  |            | $+85$ to $+105\text{ }^\circ\text{C}$ | $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | -2   |      | +2   | %    |

**Notes 1.** This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

### 3.3 DC Characteristics

#### 3.3.1 Pin characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ) (1/3)

| Items               | Symbol    | Conditions   | MIN.   | TYP. | MAX.         | Unit     |   |
|---------------------|-----------|--|--|------|--------------|----------|---|
| Input voltage, high | $V_{IH1}$ | P16, P17, P20 to P22, P30 to P32, P50, P51, P60 to P62, P70 to P73, P80 to P82 | TTL input buffer<br>$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.2  |              | $V_{DD}$ | V |
|                     |           |  | TTL input buffer<br>$3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$    | 2.0  |              | $V_{DD}$ | V |
|                     |           |  | TTL input buffer<br>$3.0\text{ V} \leq V_{DD} < 3.3\text{ V}$    | 1.5  |              | $V_{DD}$ | V |
|                     | $V_{IH2}$ | P40, P121, P122, P137, RESETB  | $0.8 V_{DD}$   |      | $V_{DD}$     | V        |   |
| Input voltage, low  | $V_{IL1}$ | P16, P17, P20 to P22, P30 to P32, P50, P51, P60 to P62, P70 to P73, P80 to P82 | TTL input buffer<br>$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0    |              | 0.8      | V |
|                     |           |  | TTL input buffer<br>$3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$    | 0    |              | 0.5      | V |
|                     |           |  | TTL input buffer<br>$3.0\text{ V} \leq V_{DD} < 3.3\text{ V}$    | 0    |              | 0.32     | V |
|                     | $V_{IL2}$ | P40, P121, P122, P137, RESETB  | 0  |      | $0.2 V_{DD}$ | V        |   |

**Caution** The maximum value of all pins is  $V_{DD}$ , even in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**(T<sub>A</sub> = -40 to +105°C, 3.0 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V) (2/3)**

| Items                | Symbol           | Conditions  | MIN.   | TYP.                  | MAX. | Unit |
|----------------------|------------------|---|--|-----------------------|------|------|
| Output voltage, high | V <sub>OH1</sub> | P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82 | 3.0 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>I <sub>OH1</sub> = -1.5 mA | V <sub>DD</sub> - 0.5 |      | V    |
| Output voltage, low  | V <sub>OL1</sub> | P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82 | 3.0 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>I <sub>OL1</sub> = 1.5 mA  |                       | 0.4  | V    |

**Caution** All pins do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**(T<sub>A</sub> = -40 to +105°C, 3.0 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V) (3/3)**

| Items                       | Symbol            | Conditions  | MIN.   | TYP. | MAX. | Unit |    |
|-----------------------------|-------------------|---|--|------|------|------|----|
| Input leakage current, high | I <sub>LH1</sub>  | P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82, P137, RESETB | V <sub>I</sub> = V <sub>DD</sub>                 |      | 1    | μA   |    |
|                             | I <sub>LH2</sub>  | P121, P122  | V <sub>I</sub> = V <sub>DD</sub> , In input port |      | 1    | μA   |    |
| Input leakage current, low  | I <sub>LIL1</sub> | P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82, P137, RESETB | V <sub>I</sub> = V <sub>SS</sub>                 |      | -1   | μA   |    |
|                             | I <sub>LIL2</sub> | P121, P122  | V <sub>I</sub> = V <sub>SS</sub> , In input port |      | -1   | μA   |    |
| On-chip pull-up resistance  | R <sub>U</sub>    | P16, P17, P20 to P22, P30 to P32, P40, P50, P51, P60 to P62, P70 to P73, P80 to P82               | V <sub>I</sub> = V <sub>SS</sub> , In input port | 10   | 20   | 100  | kΩ |

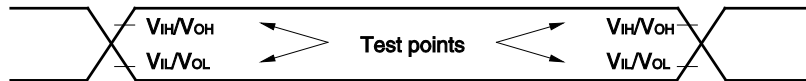
**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### 3.4 AC Characteristics

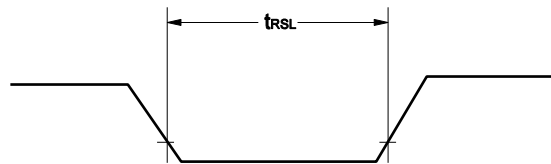
( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Items                  | Symbol | Conditions | MIN. | TYP. | MAX. | Unit          |
|------------------------|--------|------------|------|------|------|---------------|
| RESETB low-level width | trSL   |            | 10   |      |      | $\mu\text{s}$ |

#### AC Timing Test Points



#### RESETB Input Timing



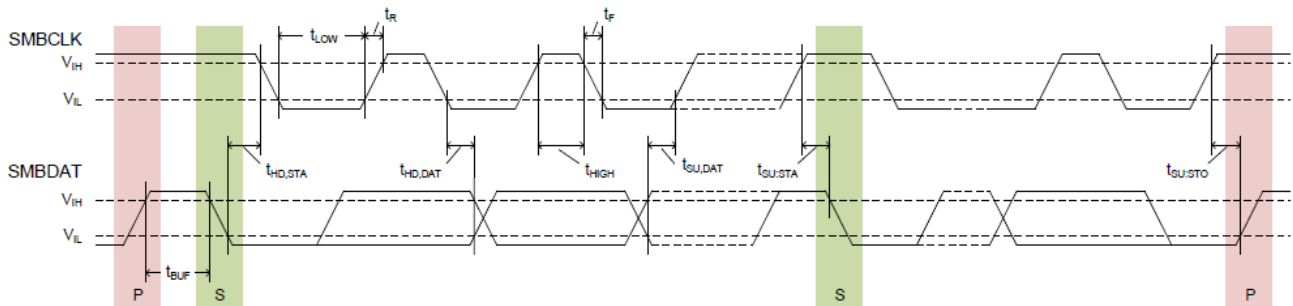
### 3.5 Peripheral Functions Characteristics

#### 3.5.1 SMBus Interface

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter  | Symbol         | Condition | 100 kHz Class |      | 400 kHz Class |     | 1 MHz Class |      | Units         |
|--|----------------|-----------|---------------|------|---------------|-----|-------------|------|---------------|
|  |                |           | MIN           | MAX  | MIN           | MAX | MIN         | MAX  |               |
| SMBus operating frequency  | $F_{SMB}$      |           | 10            | 100  | 10            | 400 | 10          | 1000 | kHz           |
| Bus free time between stop and start condition   | $T_{BUF}$      |           | 4.7           |      | 1.3           |     | 0.5         |      | $\mu\text{s}$ |
| Hold time after (Repeated) start condition. After this period, the first clock is generated. | $T_{HD:STA}$   |           | 4.0           |      | 0.6           |     | 0.26        |      | $\mu\text{s}$ |
| Repeated start condition setup time  | $T_{SU:STA}$   |           | 4.7           |      | 0.6           |     | 0.26        |      | $\mu\text{s}$ |
| Stop condition setup time  | $T_{SU:STO}$   |           | 4.0           |      | 0.6           |     | 0.26        |      | $\mu\text{s}$ |
| Data hold time   | $T_{HD:DAT}$   |           | 0             |      | 0             |     | 0           |      | ns            |
| Data setup time  | $T_{SU:DAT}$   |           | 250           |      | 100           |     | 50          |      | ns            |
| Clock low period   | $T_{LOW}$      |           | 4.7           |      | 1.3           |     | 0.5         |      | $\mu\text{s}$ |
| Clock high period  | $T_{HIGH}$     |           | 4.0           | 50   | 0.6           | 50  | 0.26        | 50   | $\mu\text{s}$ |
| Cumulative clock low extend time (slave device)  | $T_{LOW:SEXT}$ |           |               | 25   |               | 25  |             | 25   | ms            |
| Cumulative clock low extend time (master device)   | $T_{LOW:MEXT}$ |           |               | 10   |               | 10  |             | 10   | ms            |
| Clock/Data fall time   | $T_F$          |           |               | 300  |               | 300 |             | 120  | ns            |
| Clock/Data rise time   | $T_R$          |           |               | 1000 |               | 300 |             | 120  | ns            |
| Noise spike suppression time   | $T_{spike}$    |           |               |      | 0             | 50  | 0           | 50   | ns            |
| Operational time after power-on reset  | $T_{POR}$      |           |               | 500  |               | 500 |             | 500  | ms            |

Figure 3-1. SMBus Signal Timing



### 3.6 Analog Characteristics

#### 3.6.1 A/D converter characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , Reference voltage (+) =  $V_{DD}$ , Reference voltage (-) =  $V_{SS}$ )

| Parameter                           | Symbol    | Conditions        |  | MIN. | TYP. | MAX.      | Unit |
|-------------------------------------|-----------|-------------------|--|------|------|-----------|------|
| Resolution                          | RES       |                   |  | 8    |      | 10        | bit  |
| Overall error <sup>Notes 1, 2</sup> | AINL      | 10-bit resolution | $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |      | 1.2  | $\pm 7.0$ | LSB  |
| Analog input voltage                | $V_{AIN}$ | ANI8 to ANI10     |  | 0    |      | $V_{DD}$  | V    |

**Notes** 1. Excludes quantization error ( $\pm 1/2$  LSB).

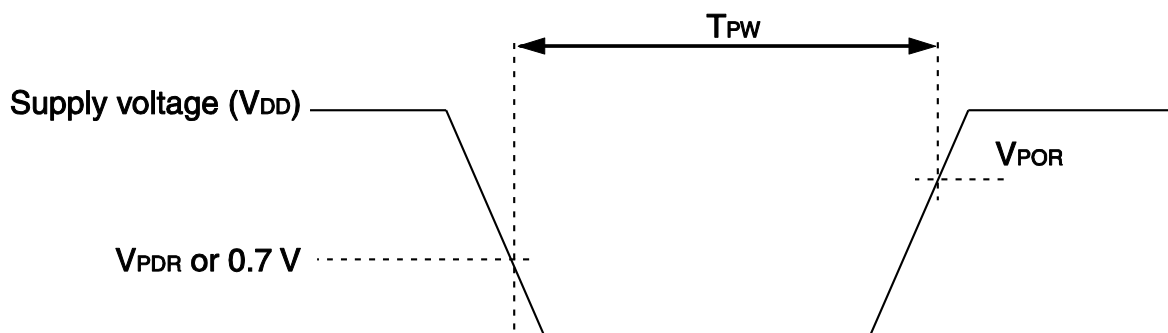
2. This value is indicated as a ratio (%FSR) to the full-scale value.

#### 3.6.2 POR circuit characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter           | Symbol    | Conditions             | MIN. | TYP. | MAX. | Unit          |
|---------------------|-----------|------------------------|------|------|------|---------------|
| Detection voltage   | $V_{POR}$ | Power supply rise time | 1.43 | 1.51 | 1.59 | V             |
|                     | $V_{PDR}$ | Power supply fall time | 1.42 | 1.50 | 1.58 | V             |
| Minimum pulse width | $T_{PW}$  |                        | 300  |      |      | $\mu\text{s}$ |

**Note** Minimum time required for a POR reset when  $V_{DD}$  exceeds below  $V_{PDR}$ . This is also the minimum time required for a POR reset from when  $V_{DD}$  exceeds below 0.7 V to when  $V_{DD}$  exceeds  $V_{POR}$  while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



#### 3.6.3 Power supply voltage rising slope characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                         | Symbol    | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|-----------|------------|------|------|------|------|
| Power supply voltage rising slope | $S_{VDD}$ |            |      |      | 54   | V/ms |

**Caution** Make sure to keep the internal reset state by the LVD circuit or an external reset until  $V_{DD}$  reaches the operating voltage range.

## 3.6.4 CC-PHY characteristics

| Parameter                    | Symbol   | Conditions | MIN. | TYP. | MAX. | Unit          |
|------------------------------|----------|------------|------|------|------|---------------|
| CC Current Source (Default)  | I80u     |            | 64   | 80   | 96   | $\mu\text{A}$ |
| CC Current Source (1.5A)     | I180u    |            | 166  | 180  | 194  | $\mu\text{A}$ |
| CC Current Source (3A)       | I330u    |            | 304  | 330  | 356  | $\mu\text{A}$ |
| Transmitter Output Impedance | zDriver  |            | 33   |      | 75   | $\Omega$      |
| Transmitter Rise Time        | tRISE_TX |            | 300  |      |      | ns            |
| Transmitter Fall Time        | tFALL_TX |            | 300  |      |      | ns            |
| Receiver Input Impedance     | zBMCRX   |            | 1    |      |      | M $\Omega$    |



### 3.7 Flash Memory Programming Characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                                    | Symbol     | Conditions                                   |                                  | MIN.  | TYP. | MAX. | Unit  |
|--|------------|--|----------------------------------|-------|------|------|-------|
| System clock frequency                       | $f_{CLK}$  | $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ |                                  | 1     |      | 24   | MHz   |
| Number of code flash rewrites<br>Notes 1,2,3 | $C_{erwr}$ | Retained for 20 years                        | $T_A = 85^\circ\text{C}$ Notes 4 | 1,000 |      |      | Times |

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
  2. When using flash memory programmer and Renesas Electronics self-programming library.
  3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
  4. This temperature is the average value at which data are retained.

### 3.8 Pin Capacitance

| Parameter                        | Symbol    | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------------------|-----------|------------|------|------|------|------|
| System Interface Pin capacitance | $C_{SYS}$ |            |      |      | 5    | pF   |
| I/O Port Pin capacitance         | $C_{IO}$  |            |      |      | 5    | pF   |

### 3.9 Power Consumption

( $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                         | Conditions  | TYP.                 | Unit          |    |
|-----------------------------------|---|----------------------|---------------|----|
| Operating current as Source role  | Sink attached.  | No PD Communication. | 3.2           | mA |
|                                   |   | PD Communication.    | 4.1           | mA |
| Operating current as Sink role    | Source attached.  | No PD Communication. | 2.7           | mA |
|                                   |   | PD Communication.    | 3.6           | mA |
| Supply current in sleep mode      | Unplugged. SMBus, WAKEUP/INTP and CC enabled for wakeup. Source role. | 205                  | $\mu\text{A}$ |    |
| Supply current in deep sleep mode | Unplugged. SMBus and WAKEUP/INTP enabled for wakeup.                  | 2.8                  | $\mu\text{A}$ |    |

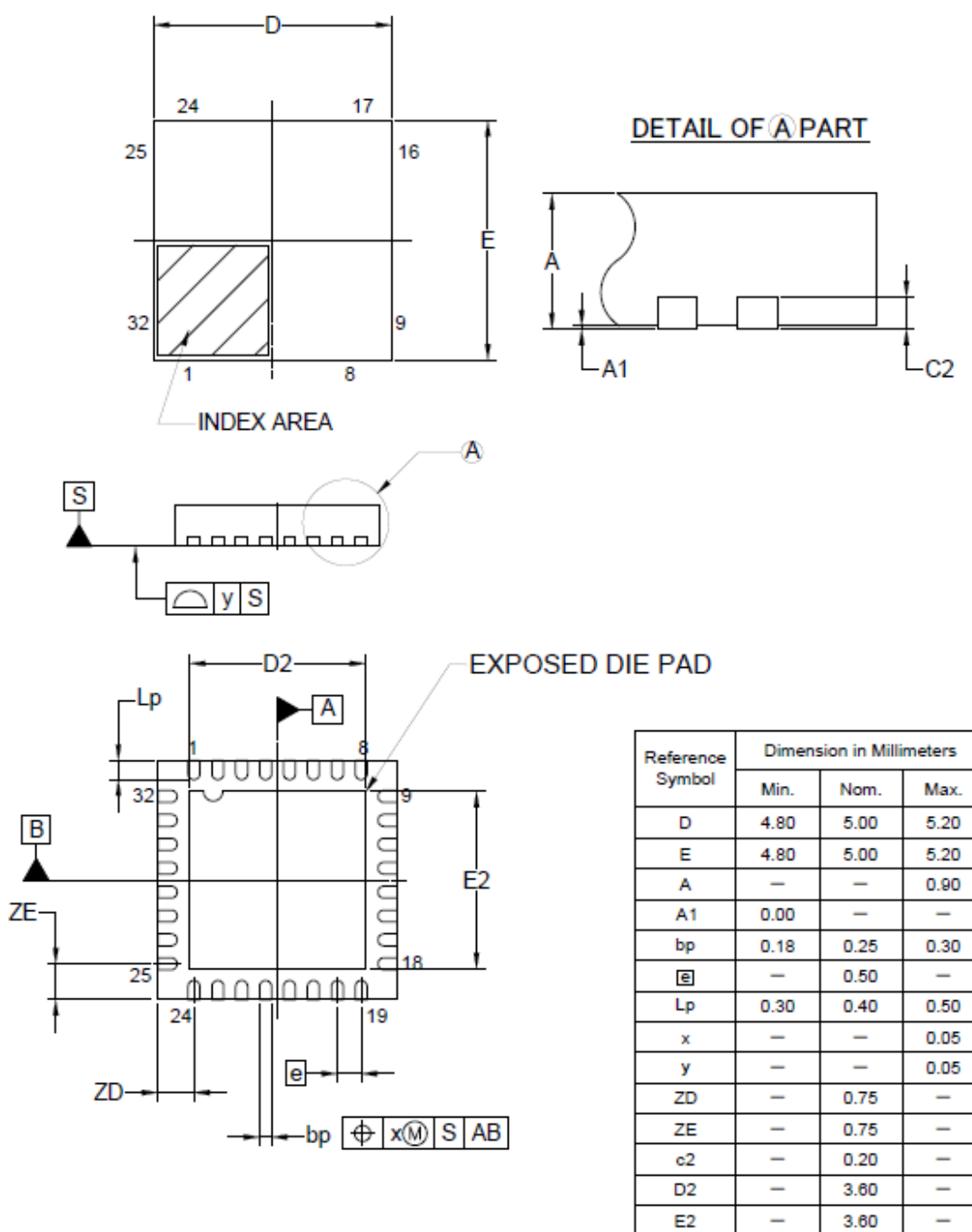
( $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter                         | Conditions  | TYP.                 | Unit          |    |
|-----------------------------------|---|----------------------|---------------|----|
| Operating current as Source role  | Sink attached.  | No PD Communication. | 3.9           | mA |
|                                   |   | PD Communication.    | 4.8           | mA |
| Operating current as Sink role    | Source attached.  | No PD Communication. | 3.4           | mA |
|                                   |   | PD Communication.    | 4.3           | mA |
| Supply current in sleep mode      | Unplugged. SMBus, WAKEUP/INTP and CC enabled for wakeup. Source role. | 230                  | $\mu\text{A}$ |    |
| Supply current in deep sleep mode | Unplugged. SMBus and WAKEUP/INTP enabled for wakeup.                  | 3.2                  | $\mu\text{A}$ |    |

### 4. PACKAGE DRAWINGS

32-PIN QFN (5 x 5 mm)

|                    |              |               |               |
|--------------------|--------------|---------------|---------------|
| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
| P-HVQFN32-5x5-0.50 | PVQN0032KG-A | T32K8-50-BAP  | 0.07          |



|                  |                      |
|------------------|----------------------|
| Revision History | R9A02G011 Data Sheet |
|------------------|----------------------|

| Rev. | Date          | Description |   |
|------|---------------|-------------|---|
|      |               | Page        | Summary                                     |
| 1.0  | Nov. 25, 2016 | -           | First Edition issued                        |
| 1.01 | Feb. 17, 2017 | 3           | Updated Figure 1-2                          |
|      |               | 5           | Updated section 2.4                         |
|      |               | 6           | Updated section 2.5                         |
| 1.02 | Oct. 24, 2017 | 1           | Updated section 1, section 1.1              |
|      |               | -           | Corrected writing errors                    |
| 1.10 | Jan. 29, 2018 | 1           | Updated section 1, section 1.1, section 1.3 |
|      |               | 3           | Updated section 1.5                         |
|      |               | 15          | Updated section 3.6.2                       |
|      |               | 18          | Updated section 3.9                         |
|      |               | 19          | Updated section 4                           |
| 1.20 | Mar. 27, 2018 | 1           | Updated section 1.1                         |
| 1.30 | Jan. 29, 2019 | 4-6         | Updated section 2.4, section 2.6            |

SuperFlash(R) is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan.

NOTE) This product uses SuperFlash(R) technology licensed from Silicon Storage Technology, inc.

|   |
|---|
| All trademarks and registered trademarks are the property of their respective owners. |
|---|

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
  2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
  3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
  4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
  5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.  
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.  
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.  
Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
  6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
  7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
  8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
  9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
  10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
  11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
  12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
- (Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.  
(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)



### SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

**Renesas Electronics Corporation**  
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

**Renesas Electronics America Inc.**  
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.  
Tel: +1-408-432-8888, Fax: +1-408-434-5351

**Renesas Electronics Canada Limited**  
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3  
Tel: +1-905-237-2004

**Renesas Electronics Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-651-700

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**  
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2265-6688, Fax: +852 2886-9022

**Renesas Electronics Taiwan Co., Ltd.**  
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan  
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**  
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

**Renesas Electronics Malaysia Sdn.Bhd.**  
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics India Pvt. Ltd.**  
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India  
Tel: +91-80-67208700, Fax: +91-80-67208777

**Renesas Electronics Korea Co., Ltd.**  
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5338