TLE987x/6x
Hardware design guideline

Application note

About this document

Scope and purpose

The MOTIX™ MCUs integrate on a single die a 32-bit microcontroller, non-volatile flash memory, analog and mixed-signal peripherals, communication interfaces along with the driving stages needed for either relay, half-bridge or full-bridge DC and BLDC motor applications. The MOTIX™ MCU is an industry standard microcontroller processor (32-bit Arm®* Cortex®-M core) in leading-edge automotive qualified technology (130 nm smart power process).

The TLE987x/6x family addresses a wide range of smart 3-phase (TLE987x) and 2-phase (TLE986x) brushless DC motor control applications, like engine cooling fans, auxiliary pumps and fans, sunroof, window lift.

This application note provides the reader with detailed descriptions about hardware design guidelines for the external components when using the TLE987x/6x devices.

Intended audience

This application note is addressed to embedded hardware and software developers using the TLE987x/6x devices to design ECUs (electronic control units) for BLDC/PMSM motor control applications.

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1 TLE987x/6x family

The TLE987x/6x is a single-chip 3-phase/2-phase motor driver that integrates the industry standard Arm® Cortex®-M3 core, enabling the implementation of advanced motor control algorithms such as field-oriented control.

It includes six (TLE987x) or four (TLE986x) fully integrated NFET drivers optimized to drive a 3-phase or 2-phase motor via external power NFETs, programmable current sources along with slope control for optimized EMC behavior and an integrated charge pump enabling low-voltage operation. Its peripheral set includes a current sense amplifier, a successive approximation ADC optionally synchronized with the capture and compare unit for PWM control, and 16-bit timers. A LIN transceiver to enable communication with the device and several general-purpose I/O units are also integrated. It includes an on-chip linear voltage regulator to supply external loads.

Unlike the other members of the TLE987x family, the TLE9879-2QXA40 incorporates two 14-bit sigma-delta ADCs, which provide a reliable interface for an external GMR/TMR sensor.

1.1 TLE987x/6x block diagram

Figure 1 shows the block diagram of the TLE987x. The TLE986x differs from the TLE987x since it integrates two bridge drivers, instead of three.

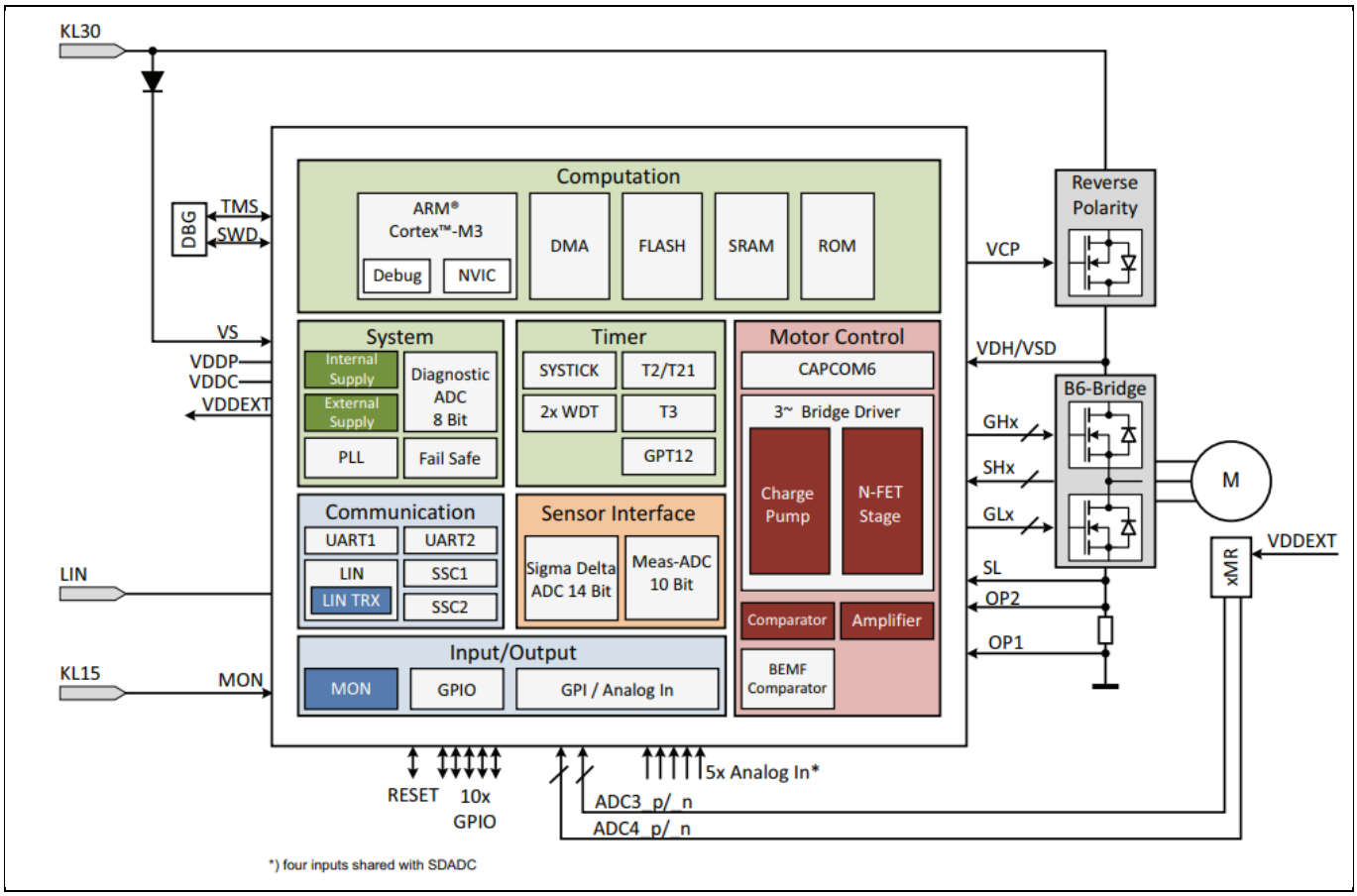


Figure 1 Block diagram of the TLE987x

In the variants with the sigma-delta ADCs, the XTAL1 and XTAL2 pins for the external oscillator are not available.

1.2 TLE987x/6x family comparison

Table 1 and Table 2 list the variants available in the TLE987x/6x product family. The versions with the sigma-delta ADCs are named using the scheme TLE987x-2Qx.

Table 1 TLE987x product family variants

Product	Package	Flash	RAM	Max. operating frequency	Interfaces	T_j max.
TLE9871QXA20	VQFN-48	36 kByte	3 kByte	24 MHz	PWM	150°C
TLE9873QXW40	VQFN-48	48 kByte	3 kByte	40 MHz	PWM + LIN	175°C
TLE9877QXA20	VQFN-48	64 kByte	6 kByte	24 MHz	PWM + LIN	150°C
TLE9877QXA40	VQFN-48	64 kByte	6 kByte	40 MHz	PWM + LIN	150°C
TLE9877QXW40	VQFN-48	64 kByte	6 kByte	40 MHz	PWM + LIN	175°C
TLE9877QTW40	TQFP-48	64 kByte	6 kByte	40 MHz	PWM + LIN	175°C
TLE9879QXA20	VQFN-48	128 kByte	6 kByte	24 MHz	PWM + LIN	150°C
TLE9879-2QXA40	VQFN-48	128 kByte	6 kByte	40 MHz	PWM + LIN	150°C
TLE9879QXA40	VQFN-48	128 kByte	6 kByte	40 MHz	PWM + LIN	150°C
TLE9879QXW40	VQFN-48	128 kByte	6 kByte	40 MHz	PWM + LIN	175°C
TLE9879QTW40	TQFP-48	128 kByte	6 kByte	40 MHz	PWM + LIN	175°C
TLE9872-2QXA40	VQFN-48	256 kByte	8 kByte	40 MHz	PWM + LIN	150°C
TLE9872QXA40	VQFN-48	256 kByte	8 kByte	40 MHz	PWM + LIN	150°C
TLE9872QTW40	TQFP-48	256 kByte	8 kByte	40 MHz	PWM + LIN	175°C

Table 2 TLE986x product family variants

Product	Package	Flash	RAM	Max. operating frequency	Interfaces	T_j max.
TLE9861QXA20	VQFN-48	36 kByte	3 kByte	24 MHz	PWM	150°C
TLE9867QXA40	VQFN-48	64 kByte	6 kByte	40 MHz	PWM + LIN	150°C
TLE9867QXA20	VQFN-48	64 kByte	6 kByte	24 MHz	PWM + LIN	150°C
TLE9867QXW20	VQFN-48	64 kByte	6 kByte	24 MHz	PWM + LIN	175°C
TLE9868QXB20	VQFN-48	128 kByte	4 kByte	20 MHz	PWM + LIN	150°C
TLE9869QXA20	VQFN-48	128 kByte	6 kByte	24 MHz	PWM + LIN	150°C
TLE9862QXA40	VQFN-48	256 kByte	8 kByte	40 MHz	PWM + LIN	150°C

1.3 Application information

Figure 2 and Figure 3 show the TLE987x in an electric-drive application setup controlling a BLDC motor. This is a very simplified example of an application circuit and bill of materials. The function must be verified in the actual application. The TLE986x differs from the TLE987x since it has two bridge drivers, instead of three.

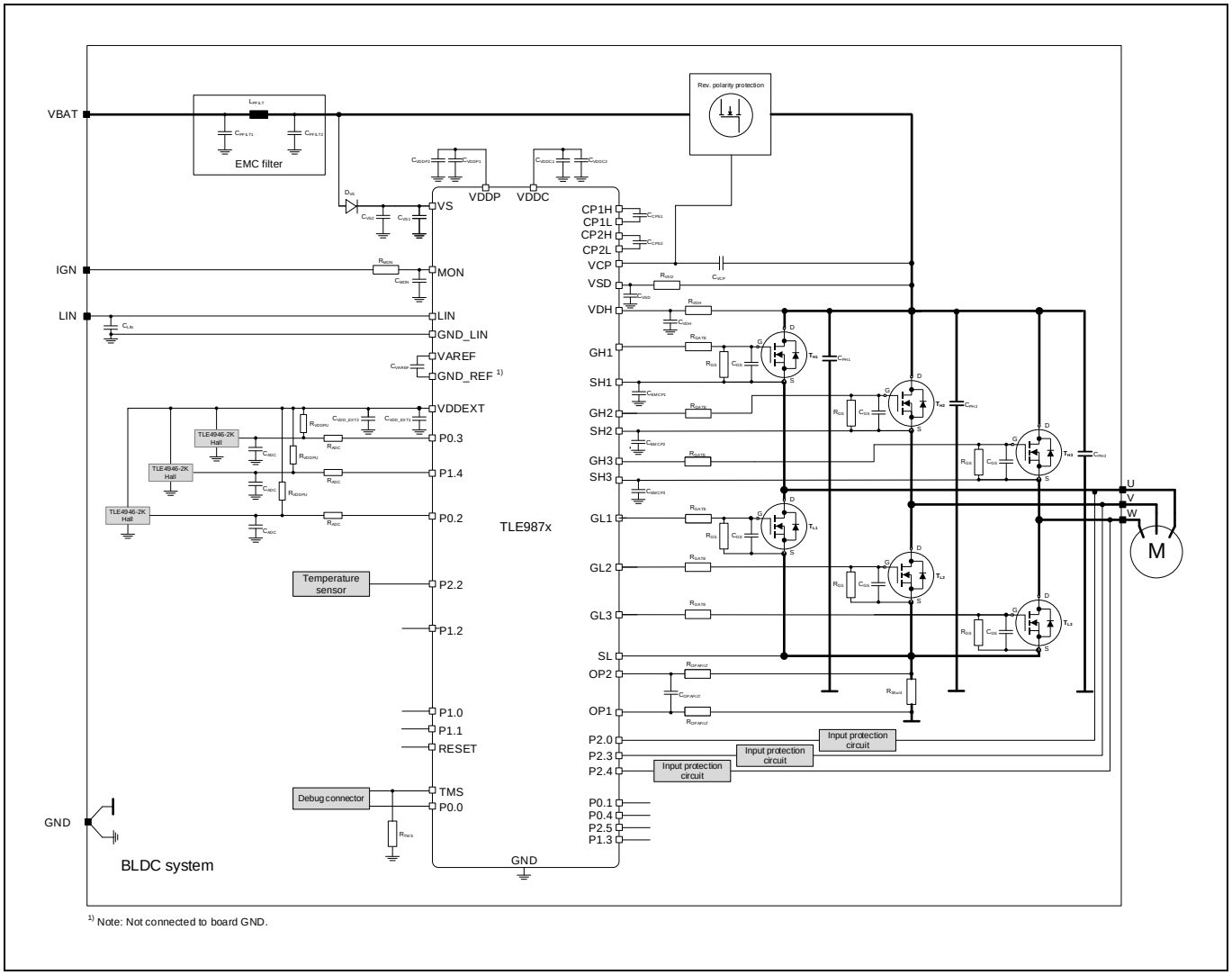
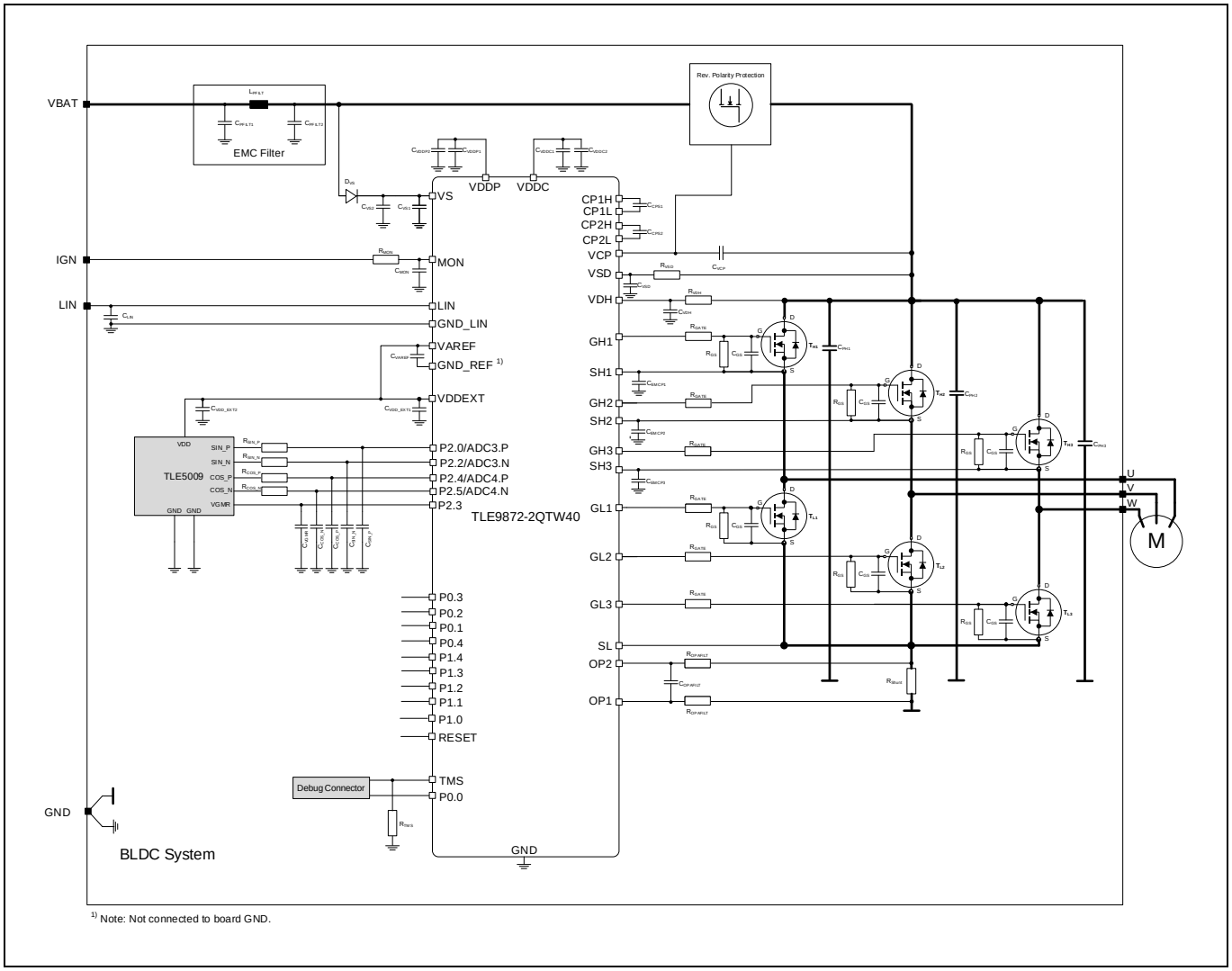


Figure 2 Application schematic example for TLE987x



1) Note: Not connected to board GND.

Figure 3 Application schematic example for TLE987x-2QX

Table 3 External components (BOM)

Symbol	Function	Component (typical)
C_{VS1}	Filter capacitor at VS pin (TLE987x supply)	≥ 100 nF
C_{VS2}	Bulk capacitor at VS pin (TLE987x supply)	> 2.2 µF
C_{VDDP}	Output capacitor at VDDP pin (voltage regulator)	470 nF + 100 nF
C_{VDD_EXT}	Output capacitor at VDD_EXT pin (voltage regulator)	100 nF
C_{VDDC}	Output capacitor at VDDC pin (voltage regulator)	470 nF + 100 nF
C_{VAREF}	Filter capacitor at VAREF pin (analog reference)	100 nF
C_{LIN}	Filter capacitor at LIN pin	220 pF
C_{VSD}	Filter capacitor at VSD pin (charge pump supply)	1 µF
C_{CPS1}	Charge pump capacitor (first stage flying capacitor)	220 nF
C_{CPS2}	Charge pump capacitor (second stage flying capacitor)	220 nF
C_{VCP}	Charge pump capacitor (output bulk capacitor)	470 nF
C_{MON}	Filter capacitor at MON pin (high-voltage monitor input)	10 nF
C_{VDH}	Filter capacitor at VDH pin (drain high-side MOSFET driver)	3.3 nF

Symbol	Function	Component (typical)
C_{PH1}	Bulk capacitor at drain high-side FET (phase U)	220 µF
C_{PH2}	Bulk capacitor at drain high-side FET (phase V)	220 µF
C_{PH3}	Bulk capacitor at drain high-side FET (phase W)	220 µF
$C_{OPAFILT}$	Filter capacitor at OP1 and OP2 pins (CSA inputs)	Application related
C_{EMCP1}	Filter capacitor at SH1 pin (source high-side FET 1)	1 nF
C_{EMCP2}	Filter capacitor at SH2 pin (source high-side FET 2)	1 nF
C_{EMCP3}	Filter capacitor at SH3 pin (source high-side FET 2)	1 nF
C_{PFILT1} , C_{PFILT2}	Filter capacitors of the input π-filter	Application related
D_{VS}	Reverse-polarity protection diode	Application related
L_{PFILT}	Filter inductor of the input π-filter	Application related
R_{MON}	Filter resistor at MON pin	3.9 kΩ
R_{VSD}	Filter resistor at VSD pin	2 Ω
R_{VDH}	Filter resistor at VDH pin	1 kΩ
R_{GATE}	FET gate resistor	2 Ω
$R_{OPAFILT}$	Filter resistor at OP1 and OP2 pins (CSA inputs)	Application related
R_{Shunt}	Shunt resistor	Application related
R_{GS}	FET gate-source resistor	Application related
C_{GS}	FET gate-source resistor	Application related
R_{VDDPU}	Pull-up resistor for Hall sensor	Application related
R_{ADC}	Filter resistor at ADC1 input	Application related
C_{ADC}	Filter capacitor at ADC1 input	Application related
R_{TMS}	Pull-down resistor at TMS pin (test mode select)	Optional
R_{SIN_P} / R_{SIN_N}	Filter resistors at ADC3 input pins (sigma-delta version)	10 kΩ
R_{COS_P} / R_{COS_N}	Filter resistors at ADC4 input pins (sigma-delta version)	10 kΩ
C_{SIN_P} / C_{SIN_N}	Filter capacitors at ADC3 input pins (sigma-delta version)	68 nF
C_{COS_P} / C_{COS_N}	Filter capacitors at ADC4 input pins (sigma-delta version)	68 nF
C_{VGMR}	Filter capacitor at GPIO input pin (GMR bridge voltage)	4.7 nF

2 Power supply generation unit (PGU)

The power management unit (PMU) is responsible for generating all required voltage supplies for the embedded MCU (VDDC, VDDP) as well as for the external supply (VDDEXT).

2.1 Block diagram

Figure 4 shows the structure of the PMU, where the power supply generation unit (PGU) includes the voltage regulators for the pad supply (VDDP), the core supply (VDDC) and the voltage regulator to supply external circuits (VDDEXT).

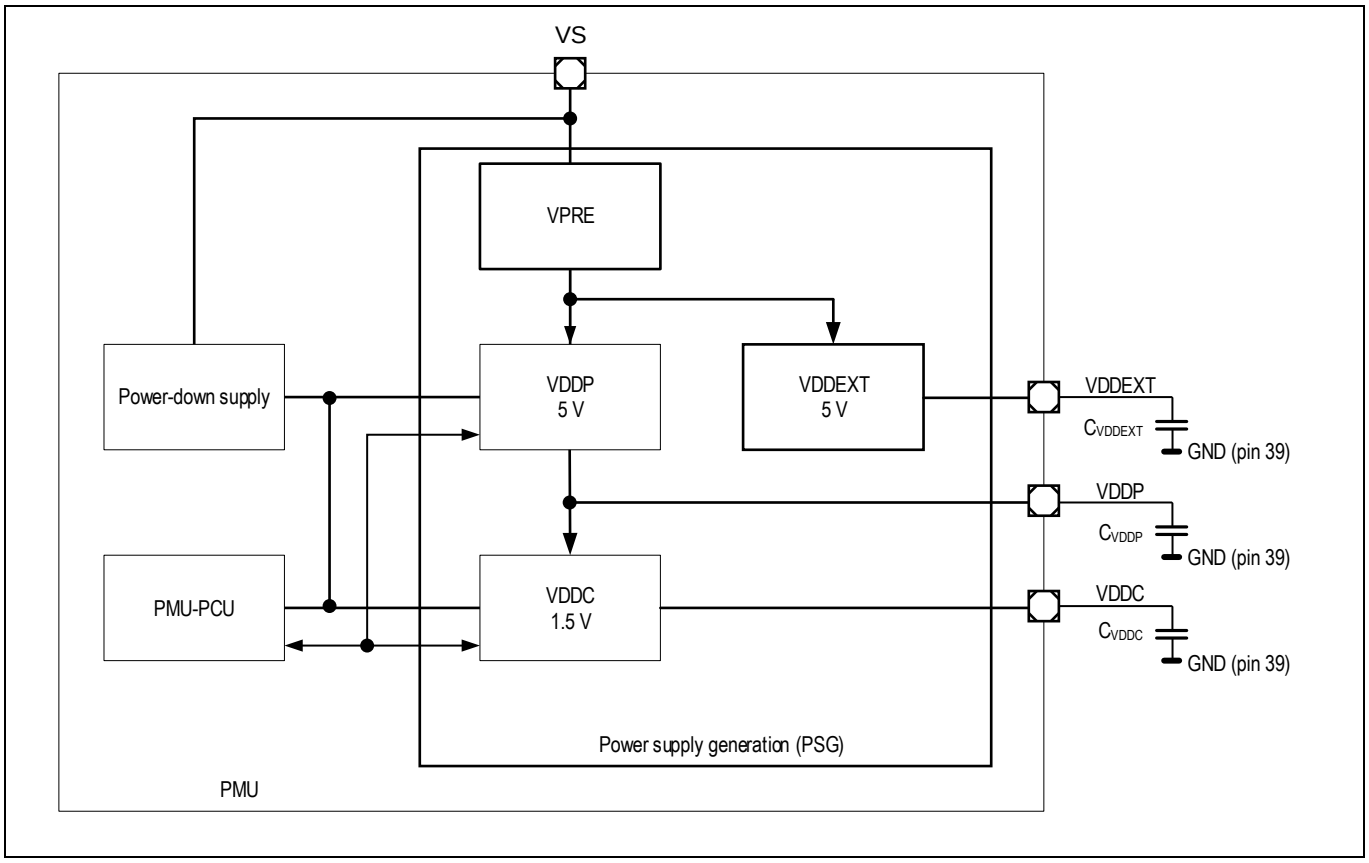


Figure 4 Power supply generation block diagram

The submodules of the PMU are:

- **Power-down supply:** independent analog supply voltage generation for power control unit logic, for the VDDP regulator and for the VDDC regulator
- **VPRE:** analog supply voltage pre-regulator. This regulator reduces the power dissipation for the following regulator stages
- **VDDP:** 5-V digital voltage regulator used for internal modules and all GPIOs
- **VDDC:** 1.5-V digital voltage regulator used for internal microcontroller modules and core logic
- **VDDEXT:** 5-V digital voltage regulator used for external circuits
- **PMU-PCU:** power control unit responsible for supervising and controlling the 5-V regulator and the 1.5-V regulator

2.2 Input voltage, VS pre-regulator VPRE, and reference voltage VAREF

The VS input is the supply voltage of the VPRE pre-regulator and the power-down supply. VS is derived from the battery voltage (VBAT), and, if necessary, it must be protected against reverse battery connections using a diode (D_{VS}) in series to VBAT. The Infineon application note "Reverse Polarity Protection for Embedded Power ICs" provides a detailed description of the complete circuit for reverse battery protection.

The C_{VS1} and C_{VS2} capacitors, placed before the VS pin, respectively act as a filter and a bulk capacitor for the TLE987x/6x power supply.

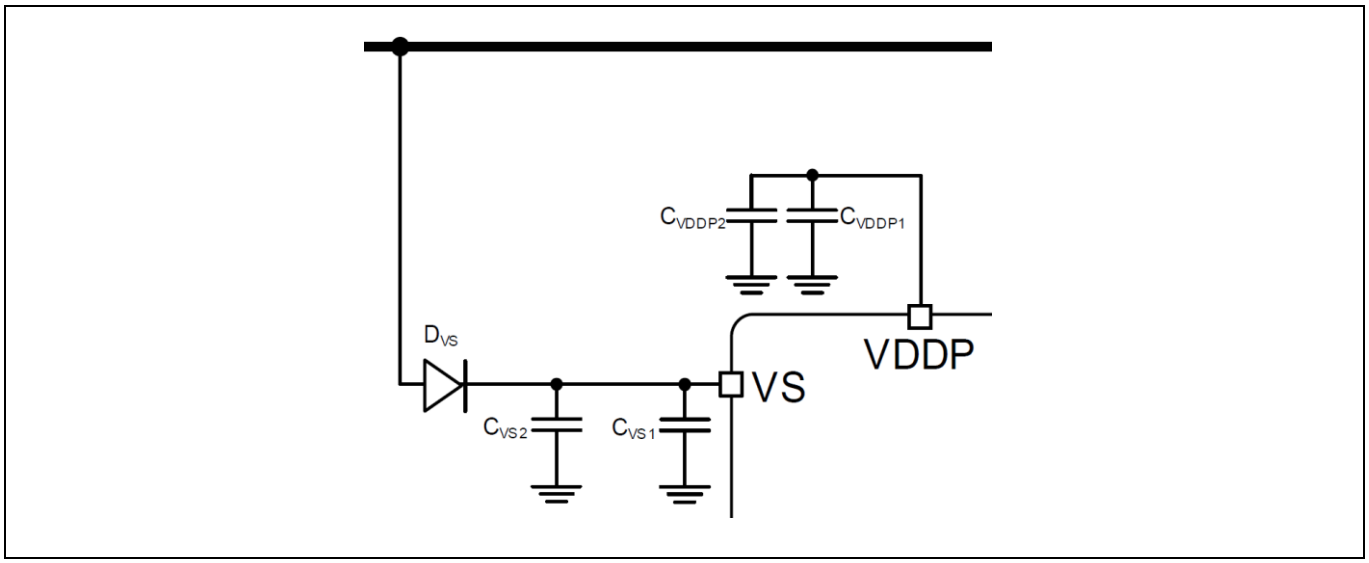


Figure 5 Components before VS pin

If data should be saved in the flash memory at power down, the selection of C_{VS2} should be done in order to ensure that operations modifying the content of the flash are never interrupted (for example, in case of power loss). Assuming that at power loss detection all the peripherals are disabled, the power is still consumed by the MCU and flash erase and write operations. The size of C_{VS2} can be calculated using the equation:

$$C_{VS2} \geq \frac{I \times t}{\Delta V}$$

Where:

- I is the current consumption at power down
- t is the time for which the MCU should stay active after power loss
- ΔV is the difference between the voltage at the time when the loss of power is detected and the reset voltage of the MCU

As reported in the TLE987x/6x product datasheets, the supply voltage in Active mode with reduced functionality (full MCU and flash operation) has a minimum value of 3 V. For example, assuming 10 mA as the current consumption during power down, 20 ms as the time needed to save the flash content, and 3 V as ΔV, then C_{VS2} must be at least 67 µF.

Table 4 shows the recommended components to connect before the VS pin.

Table 4 Component selection for VS pin

Symbol	Function	Recommended component
D_{VS}	Diode for reverse battery protection	**PN or Schottky diode** Voltage and current ratings defined according to the application
C_{VS1}	Filter capacitor	Ceramic capacitor **Min. value 100 nF type: X7R** Voltage rating and dielectric type defined according to the application
C_{VS2}	Bulk capacitor	Electrolytic or ceramic capacitor **Min. value 2.2 µF type: X7R** Value, voltage rating, and temperature defined according to the application

The voltage pre-regulator VPRE generates an internal voltage of about 7 V from the VS input. The output voltage of VPRE is used as input for the internal voltage regulators, and it is not accessible externally.

The I_{PRE} current is shared between the VDDP and VDDEXT voltage regulators. The table summarizes the maximum currents allowed for each voltage regulator.

Linear regulator	Maximum current
VPRE	I_{PRE} = 110 mA $I_{PRE} = I_{DDP} + I_{DDEXT}$
VDDP	I_{DDP} = 90 mA I_{DDEXT} = 20 mA
VDDEXT	I_{DDEXT} = 40 mA I_{DDP} = 70 mA
VDDC	I_{DDC} = 40 mA

The voltage VAREF is derived from VPRE and it can be used as 5 V reference voltage for the internal AD converters. The value of the capacitor C_{VAREF} is in the range of 100 nF up to 1 µF.

2.3 VDDP voltage regulator 5.0 V

This 5-V voltage regulator provides the pad supply for the parallel port pins and other 5-V analog functions (for example, the LIN transceiver).

Notes

1. *The output capacitor C_{VDDP} is necessary for the stability of the output voltage.*
2. *The values of the C_{VDDP} capacitors are specified in the table below.*
3. *One single ceramic capacitor can be used, as long as the value is within the recommended range.*
4. *The C_{VDDP} capacitor should be placed as close as possible to the VDDP pin in the layout.*
5. *For EMC reasons, a ferrite bead can be placed between the VDDP pin and the C_{VDDP} capacitor.*

Table 5 Capacitor selection for VDDP

Symbol	Function	Recommended component
C_{VDDP}	Output capacitor at VDDP	Ceramic capacitor **Min. value: 470 nF + 1 µF (1.47 µF) type: X7R** **Max. value: 2.2 µF + 2.2 µF (4.4 µF) type: X7R** Voltage rating: 10 V or higher Size and dielectric type defined according to the application

2.4 VDDC voltage regulator 1.5 V

This 1.5-V voltage regulator provides the power supply for the microcontroller core, the digital peripherals, and other internal analog 1.5-V functions (for example, ADC2).

Notes

1. *The output capacitor C_{VDDC} is necessary for the stability of the output voltage.*
2. *The values of the C_{VDDC} capacitors are specified in the table below.*
3. *One single ceramic capacitor can be used, as long as the value is within the recommended range.*
4. *The C_{VDDC} capacitor should be placed as close as possible to the VDDC pin in the layout.*
5. *It is NOT possible to place a ferrite bead between the VDDC pin and the C_{VDDC} capacitor.*
6. *For EMI reasons the ground of the VDDC and the ground of the TLE987x/6x can be separated by placing a ferrite bead between the two ground points.*

Table 6 Capacitor selection for VDDC

Symbol	Function	Recommended Component
C_{VDDC}	Output capacitor at VDDC	Ceramic capacitor **Min. value: 100 nF + 330 nF (430 nF) type: X7R** **Max. value: 1 µF + 1 µF (2 µF) type: X7R** Voltage rating: 4 V or higher Size and dielectric type defined according to the application

2.5 VDDEXT voltage regulator 5.0 V

This 5-V voltage regulator supplies power to external circuits. It can be used, for example, to supply an external sensor, LEDs, or potentiometers. VDDEXT can be used as the reference for SDADC (ADC3/4), if available in the product variant.

Notes

1. *The output capacitor C_{VDDEXT} is necessary for the stability of the output voltage.*
2. *The values of the C_{VDDEXT} capacitors are specified in the table below.*
3. *One single ceramic capacitor can be used, as long as the value is within the recommended limits.*
4. *The C_{VDDEXT} capacitor should be placed as close as possible to the VDDEXT pin in the layout.*
5. *In case VDDEXT is not used and disabled, the output capacitor C_{VDDEXT} is not needed. The pin VDDEXT can be left open.*

Table 7 Capacitor selection for VDDEXT

Symbol	Function	Recommended component
C_{VDDEXT}	Output capacitor at VDDEXT	Ceramic capacitor **Min. value: 100 nF + 1 µF (1.1 µF) type: X7R** **Max. value: 2.2 µF + 2.2 µF (4.4 µF) type: X7R** Voltage rating: 10 V or higher Dielectric type defined according to the application

3 Clock generation unit (CGU)

The clock generation unit (CGU) enables a flexible clock generation. The frequency can be modified to optimize performance-to-power-consumption ratio. The system clock f_{SYS} can be generated from one of the following sources:

- Phase-locked loop (PLL) output f_{PLL}
- External clock from external crystal oscillator f_{OSC}
- External clock from external clock input f_{OSC}
- Low-precision clock f_{LP_CLK}

3.1 Block diagram

The CGU consists of a high-precision oscillator circuit (OSC_HP), a PLL module with an internal oscillator (OSC_PLL), and a configurable clock control unit (CCU). The CGU can convert a low-frequency input or external clock signal to a high-frequency internal clock.

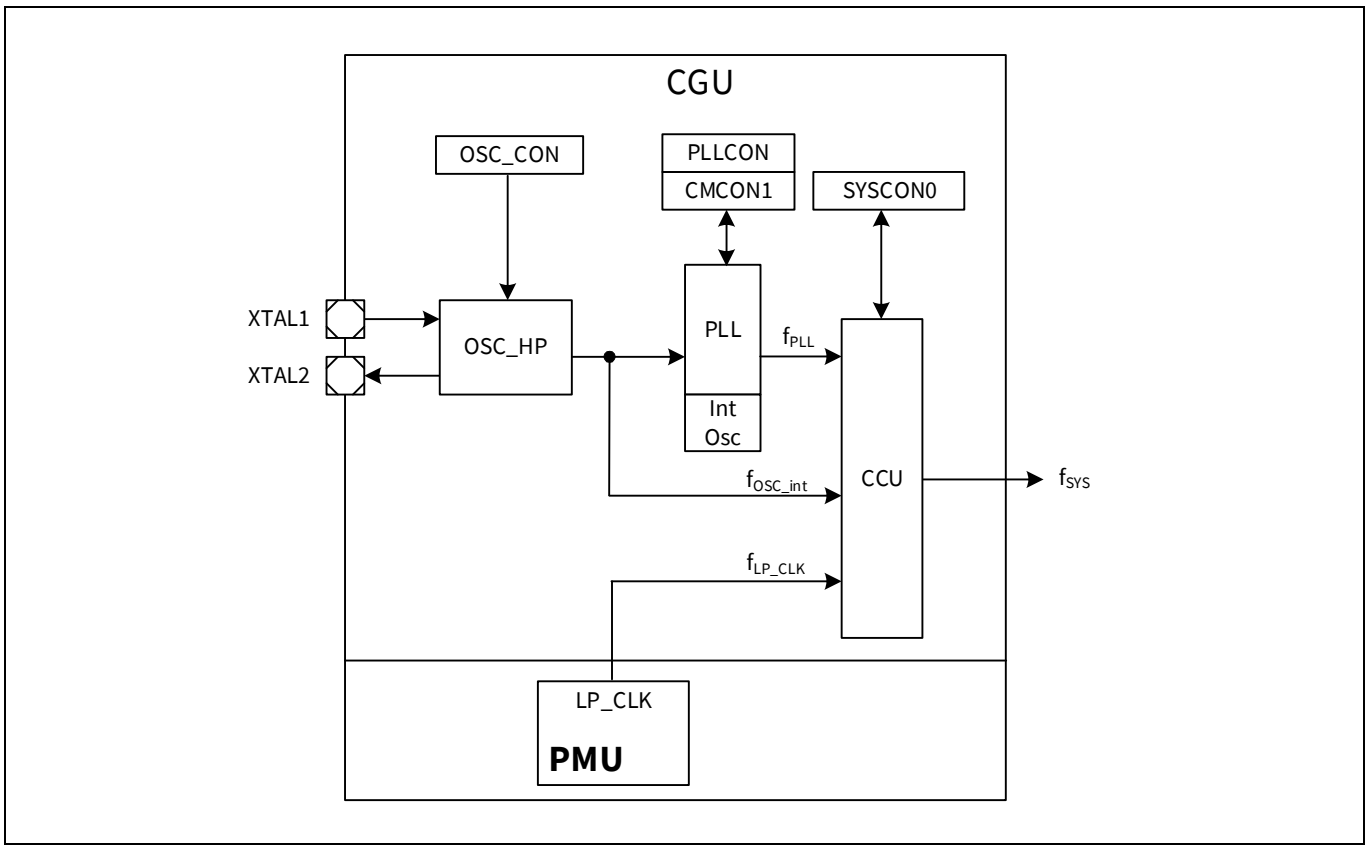


Figure 6 CGU block diagram

The submodules of the CGU are:

- **High-precision oscillator circuit:** designed to work with either an external crystal oscillator or an external stable clock source. It consists of an inverting amplifier with XTAL1 as the input and XTAL2 as the output.

- **Phase-locked loop (PLL) module:** generates the clock f_{PLL} in different modes:
  - Prescaler mode (VCO Bypass mode)
  - Normal mode
  - Free-running mode

  The reference frequency f_R can be selected to be taken either from the internal oscillator f_{INT} or from an external clock source f_{OSC_INT}.
  The PLL uses up to three dividers to manipulate the reference frequency in a configurable way. Each of the three dividers can be bypassed corresponding to the PLL operating mode.

- **Clock control unit (CCU):** enables the selection of the source for f_{SYS}

3.2 External Input Clock mode

The External Input Clock mode is used to directly supply the device with an externally generated clock signal in the range from 4 MHz to 16 MHz. In this mode, the high-precision oscillator circuit is bypassed and the external clock signal is directly fed into the PLL module. The input frequency has to be 4 MHz or higher, if the prescaler mode is used.

The external clock input has to be connected to XTAL1, while XTAL2 is left open (not connected). The negative terminal of the external clock input has to be connected to the analog GND (pin 39).

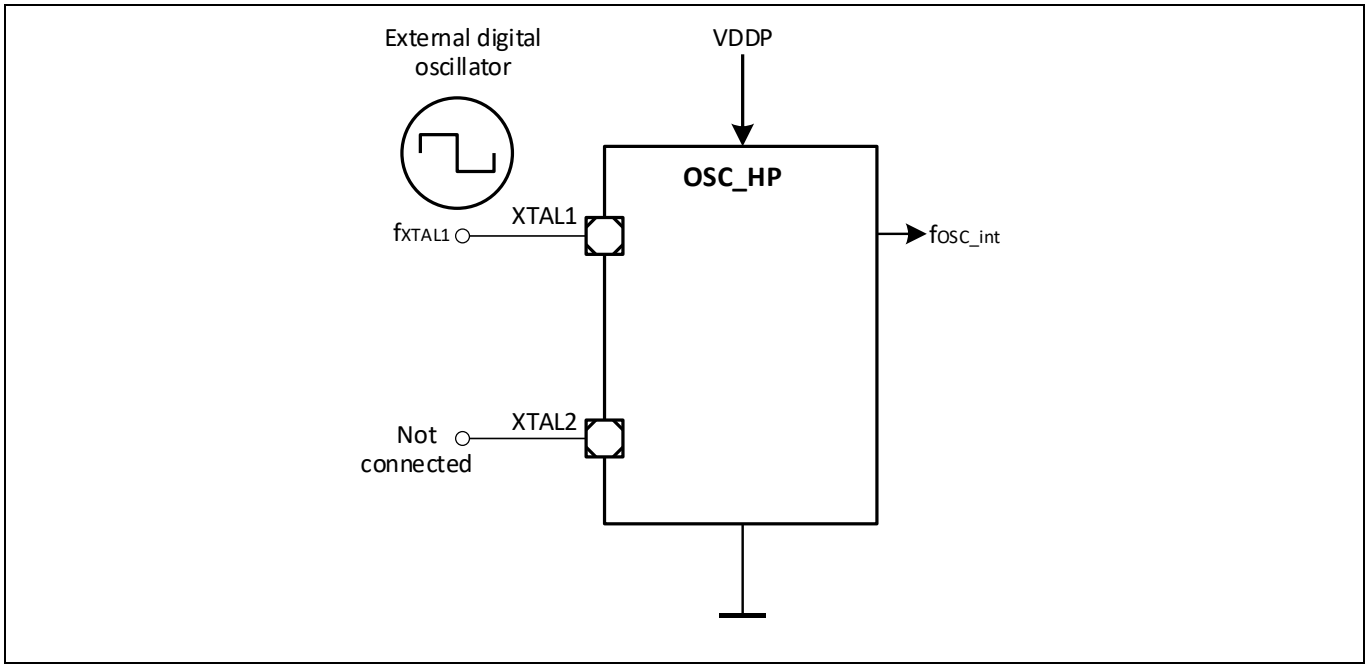


Figure 7 External Input Clock mode

3.3 External Crystal mode

The External Crystal mode is used to supply the device with an external crystal within in the range from 4 MHz to 16 MHz. An external oscillator circuity has to be placed, consisting of two load capacitors connected to XTAL1/GND and XTAL2/GND and an optional serial damping resistor at XTAL2. The GND pin is in this case the analog GND (pin 39).

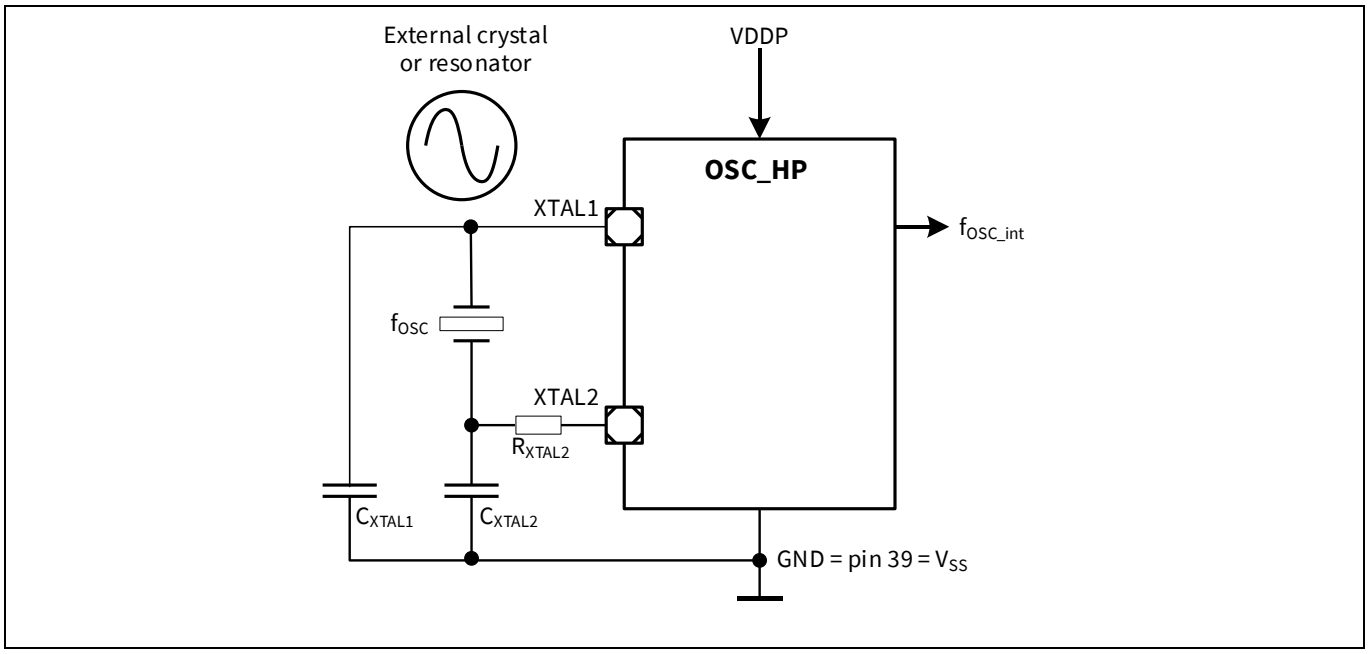


Figure 8 External Crystal mode

The values and the corresponding operating ranges depend on the chosen crystal and have to be determined and optimized in cooperation with the crystal vendor, using the negative resistance method, which is the most common test for start-up and oscillation reliability of the oscillator. This method is about the insertion of a test resistor in series with the quartz crystal and the monitoring of the drive current. Typically, this test does not result in one set of circuitry values which is the ‘right one’, but it indicates a recommended range. Depending on further system requirements such as XTAL1 amplitude specification or oscillator frequency, the final circuitry values of the oscillator are then selected.

More information about the test method can be found in the Infineon application note “Crystal Oscillator Basics AP56002”.

Symbol	Function	Recommended component
C_{XTAL1}, C_{XTAL2}	Load capacitors for external crystal oscillator forming an LC tank circuit which determines the oscillator frequency	≥ 10 V ceramic capacitor X7R/X8R (low ESR, 0805 package)
R_{XTAL2}	Serial damping resistor	0-280 Ω

The oscillator can operate for a specified set of crystals with known ESR and parasitic capacitances C_{IO} and C_O up to a specific value.

Choosing different crystals requires detailed consideration of parasitics, external circuitry, frequency range, and quality of the intended crystal. Its proper operation has to be verified by testing.

Table 8 Recommendation for oscillator load capacitors

f_{osc}	4 MHz	8 MHz	12 MHz	16 MHz
ESR_{typ} / Ω	120	90	80	70
C_{IO} / pF	3.5	3.5	3.5	3.5
C_O / pF	3	3	3	3
$C_{XTAL1} = C_{XTAL2}$ / pF	33	18	12	12

3.3.1 Ceramic resonator

Some applications do not require highest clock accuracy, especially for lower temperatures it might not be necessary to use a quartz crystal and a ceramic resonator can be used instead. These integrated resonator circuits don't need additional load capacitors and damping resistors and can be directly connected to XTAL1/2.

3.4 Layout recommendations

Figure 9 shows a layout example for an SMD quartz crystal to be used with the TLE987x/6x.

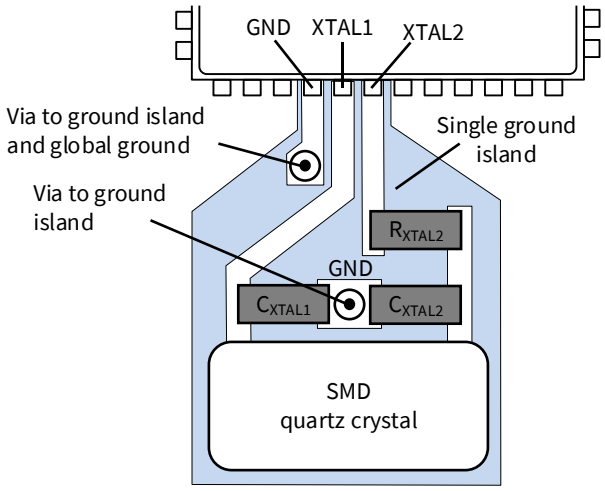


Figure 9 CGU layout recommendation

4 General purpose inputs outputs (GPIO)

The TLE987x/6x has two bidirectional ports (P0, P1) and one analog port (P2). Each pin (*n* = 0-7) of each port (*x* = 0-2) can individually be configured as an input or output by setting the respective P*n* bitfield in the P*x*_DIR register. If configured as an output, the pin state can be set to high or low by setting the respective P*n* bitfield in the P*x*_DATA register. Additionally, the pin state can be set to tristate or high impedance with weak pull-up/pull-down termination by activating the internal pull-up or pull-down devices.

This allows the following output characteristics:

- Push/pull
- Open drain (OD) with internal pull-up device
- OD with external pull-up

And the following input characteristics:

- Tristate
- High-impedance (HI) with weak pull-up termination
- HI with weak pull-down termination

4.1 Pull-up and pull-down devices and pin state

The internal pull-up and pull-down devices can be active to determine the pin state (logical high or low), if no external source or sink tries to determine the pin state. If the pin voltage is changed by an external source or sink, a keep or force current will flow from the pull-up or pull-down device, trying to keep or force the pulled state. This is called a weak termination, since the maximal current to keep the pull-up or pull-down state the devices can provide is relatively low. The currents that will flow for a specific deviation from the target voltage state are specified in the electrical characteristics of the parallel ports. These values differ between P0/P1 and P2.

4.2 Software settings and hardware considerations

A specific GPIO can only be used as an input or an output at the same time. When using the internal pull-up or pull-down devices, no external pull-up or pull-down shall be used.

Table 9 GPIO configuration settings

State	Px_DIR.Pn	Px_DATA.Pn	Px_OD.Py	Px_PUDSEL.Py	Px_PUDEN.Py	External HW
Push (optional pull-up device)	1	1	0	1	optional: 1	–
Pull (optional pull-down device)	1	0	0	0	optional: 1	–
OD with internal pull-up device	1	0	1	1	1	–
OD with external pull-up	1	0	1	0	0	10 kR
Tristate	0	Read for pin state	NA	0	0	–
HI with weak pull-up termination	0	Read for pin state	NA	1	1	–
HI with weak pull-down termination	0	Read for pin state	NA	0	1	–

4.3 Serial resistor for high-speed signals

When using an alternative function of a GPIO, different hardware measures might be needed for optimized performance and robustness. When, for example, operating logic-level communication interface at the devices, a serial resistor (R_{IO}) might be necessary to suppress ringing of the signals caused by the LC-circuit formed by the port-capacitance of the GPIOs (C_{IO}), and the capacitance (C_{TRACE}), and inductance (L_{TRACE}) of the PCB traces.

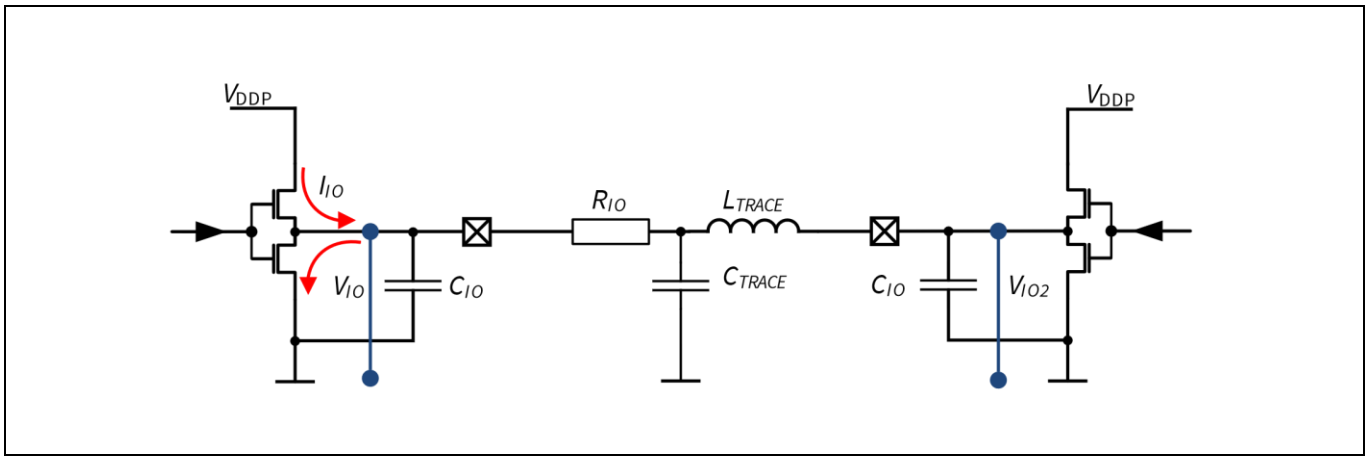


Figure 10 GPIO serial resistor

V_{IO} is the signal generated by the sending GPIO and V_{IO2} the signal seen by the receiving GPIO. Each GPIO has a pin capacitance (P_5.1.19).

The trace capacitance and inductance depend on the traces' width (W), length (L), thickness (T), PCB layer thickness (H) (all dimensions in meter), the PCB's dielectric constant ε_R, and vacuum permittivity ε_0. The used formula is only valid for surface traces with an adjacent power or ground plane.

$$C_{Trace} = \varepsilon_R \times \varepsilon_0 \times \frac{W \times L}{H} \; [F]$$

$$L_{Trace} = 0.2 \times ln\left(\frac{8 \times H}{W} + \frac{W}{4 \times H}\right) \times L \; [nH]$$

The trace capacitance and inductance are calculated for a standard trace width of 0.2 mm and thickness of 0.04 mm and a PCB layer thickness of 1.6 mm. V_{IO} is 5 V and rises and falls within 1 ns. V_{IO} and V_{IO2} are plotted for different trace lengths and serial resistor dimensions in Figure 11.

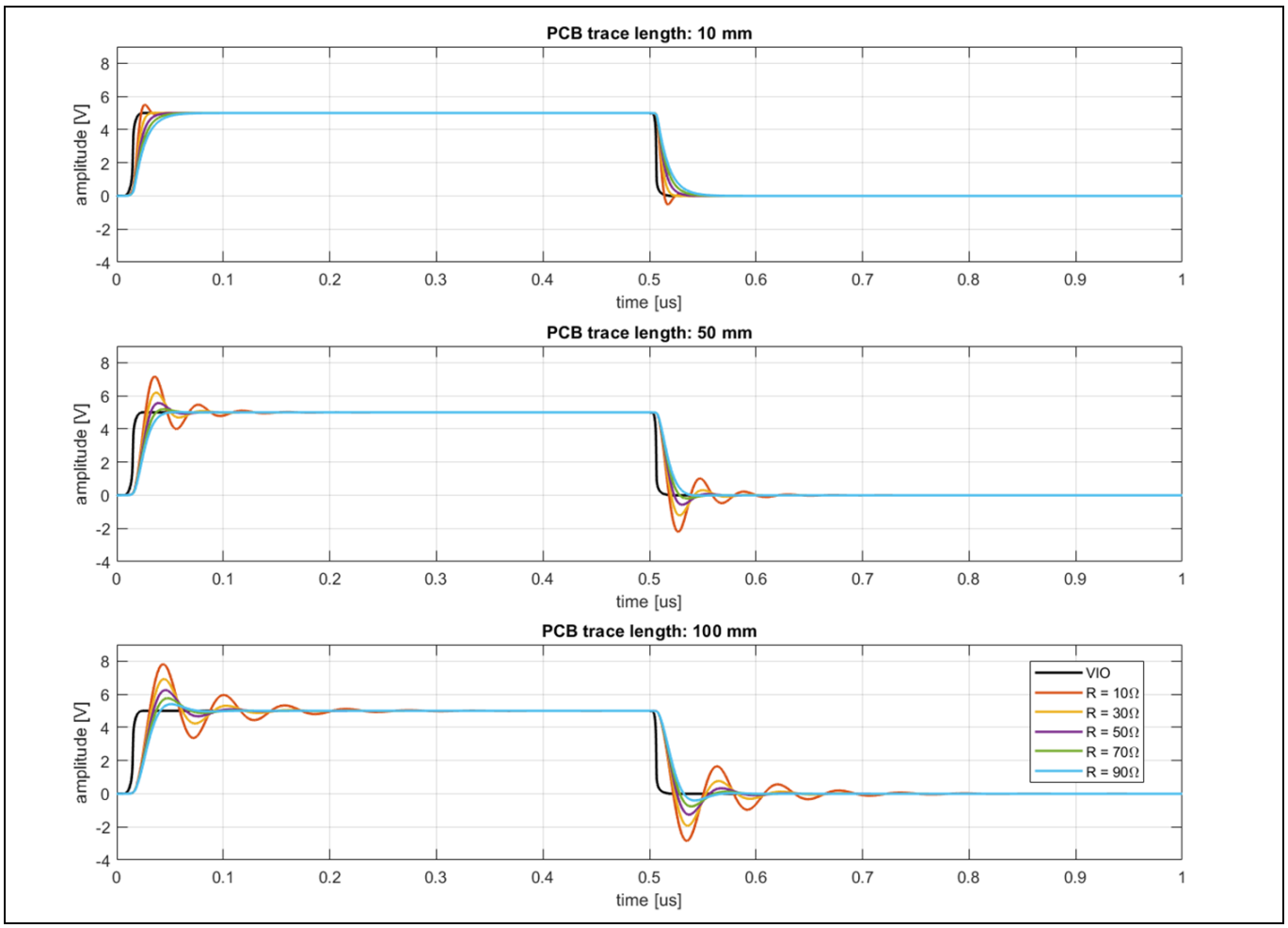


Figure 11 GPIO ringing

For traces with a length of 100 mm, a 90 Ω resistor suppresses ringing efficiently. If production spread and temperature dependency are considered, 220 Ω are sufficient for most applications.

Table 10 Resistor selection for GPIOs

Symbol	Function	Recommended component
RPU	Pull-up for external pin termination	10 kΩ
RIO	Serial resistor for high accuracy high-speed communication	**Min:** value 220 Ω Has to be assessed if needed in the application

5 LIN transceiver

The LIN module is a transceiver for the local interconnect network (LIN) compliant to the LIN2.2 standard, backward compatible to LIN1.3, LIN2.0 and LIN2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single-wire, bidirectional bus, which is typically used for in-vehicle networks, using data rates between 2.4 kBaud and 20 kBaud. Additionally, data rates up to 115.2 kBaud are supported.

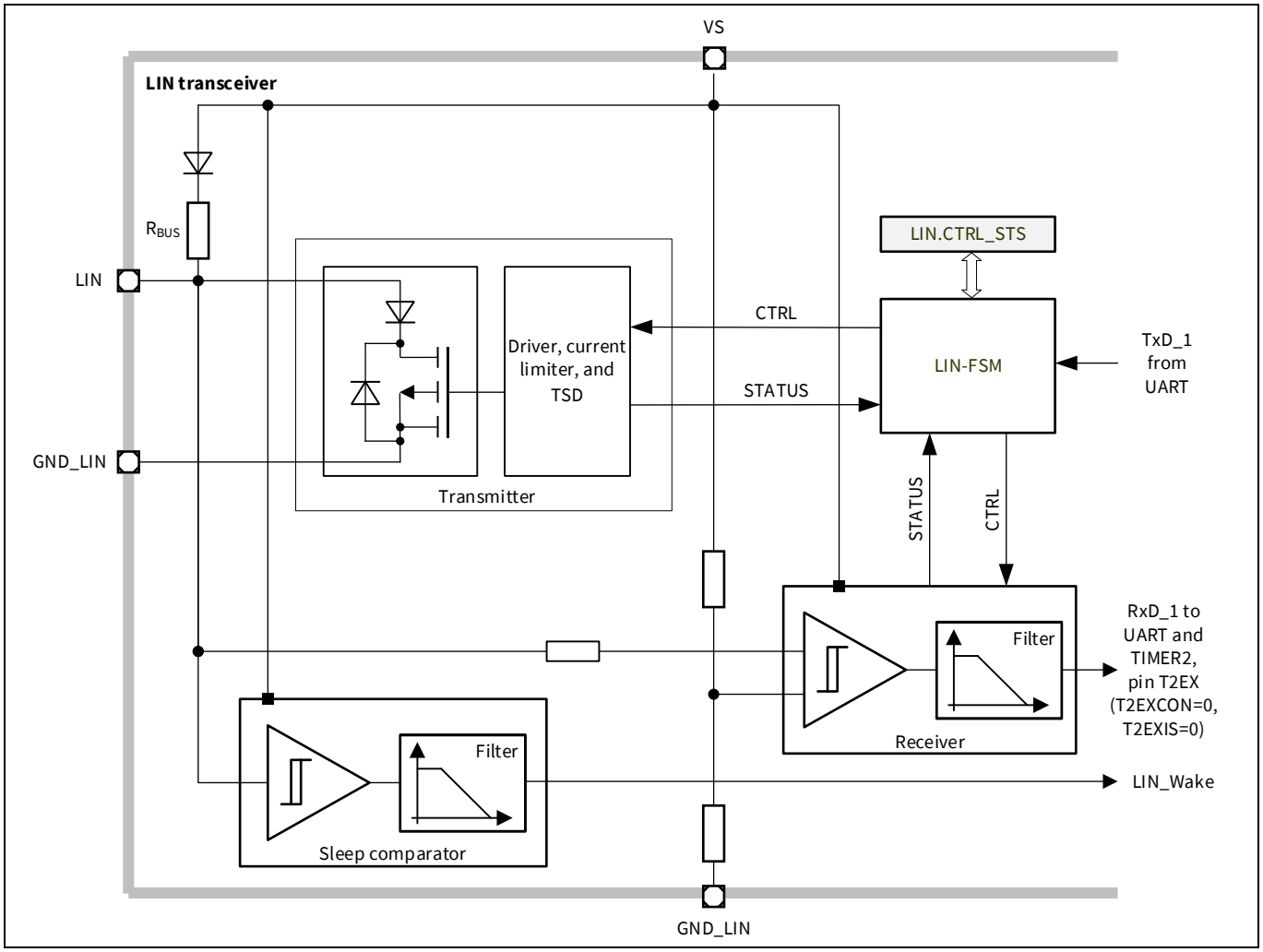


Figure 12 LIN transceiver block diagram

It is recommended to put a 220 pF capacitor between the LIN and the GND_LIN pins. This complies with the LIN specification 2.2. The GND_LIN pin has to be connected to a global ground net outside of the chip.

In order to avoid interferences with the SoC's core voltage, it is recommended to connect GND_LIN to the same ground net of the power MOSFETs – called power GND. It is strongly advised not to wire GND_LIN to a connector which leaves the PCB. The global ECU ground level shall be used as a reference for the LIN connection. To reduce digital ground bounce transmitted via LIN, GND_LIN should not be connected directly to the GND of the TLE987x/6x. It is better to have a slight decoupling by using few millimeters of trace. The LIN transceiver can be used also with PWM control. In this case, a pull-up resistor between the LIN input and the battery input voltage should be placed. The value of the pull-up resistor is ≥ 1 kΩ. In case additional filtering is needed because of EMC issues, common mode chokes before the LIN pin are not recommended. A ferrite bead placed at GND_LIN is preferred.

6 High-voltage monitor input

This module monitors external voltage to detect levels above or below a specified threshold, or it can be used in Low Power mode to detect a wake-up event at the high-voltage MON pin.

6.1 Block diagram

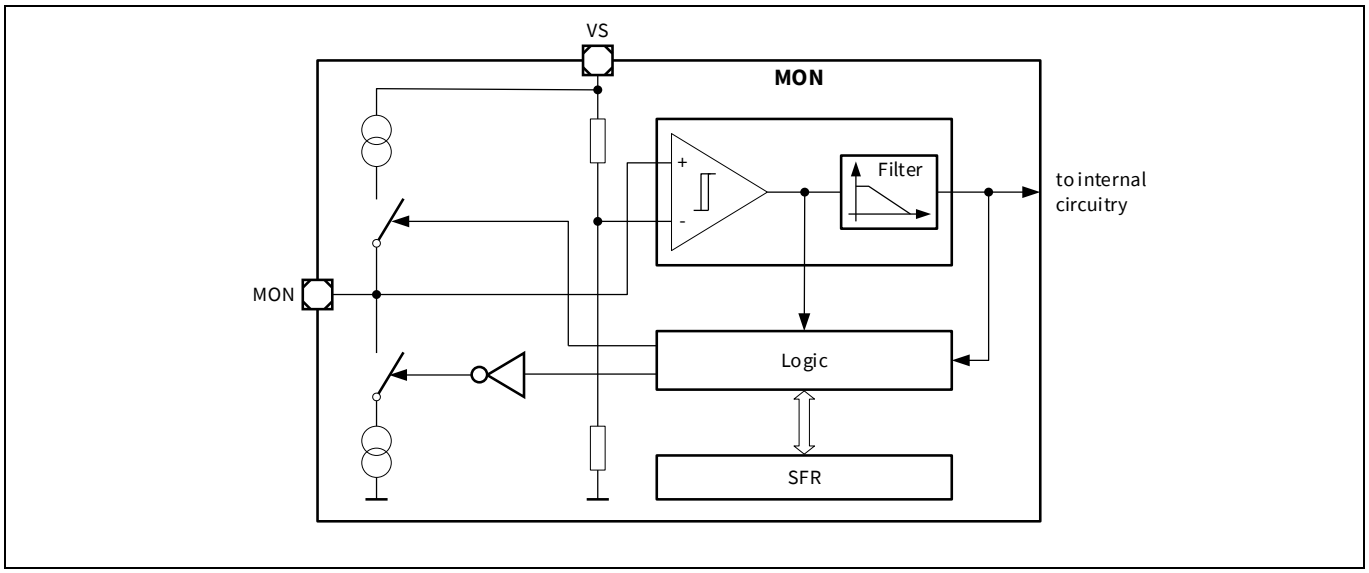


Figure 13 Monitor input block diagram

6.2 Application hints

The functional description of the high-voltage monitor input is included in chapter 26 of the TLE987x and TLE986x user manual.

A dedicated R-C filter (R_{MON} and C_{MON}) must be placed before the MON pin, in order to protect it against reverse polarity connection and voltage transients (ISO pulses), which could violate the absolute maximum ratings of the MON pin. In fact, in a typical use-case the MON pin could be directly connected to the car battery in order to sense the supply voltage, especially during power-down. Having no diode placed in series, the MON pin of the TLE987x would be not protected against reverse polarity connection.

The table below shows the recommended R_{MON} and C_{MON} values. The GND to be used for C_{MON} is the analog or digital GND. Since the R-C time constant affects the voltage slope on the MON pin, the R_{MON} and C_{MON} values should be selected according to the application requirements. Due to potential high peak power during transient tests, the recommended package for R_{MON} is 1206 SMD.

Table 11 Component selection for the MON pin

Symbol	Function	Recommended component
R_{MON}	Filter resistor	**Min. value 1 kΩ** R_{MON} value and size selected according the application, package 1206 SMD recommended
C_{MON}	Filter capacitor	Ceramic capacitor **Min. value 10 nF, typical voltage rating 50 V** C_{MON} value, voltage rating, size, and dielectric type selected according to the application

7 Analog to digital converters (ADC1)

The TLE987x/6x has two successive approximation ADCs with 10-bit (ADC1) or respectively 8-bit (ADC2) resolution to monitor external and internal signals.

7.1 Software settings and hardware considerations

The two ADCs are connected to different signals and have different digital post-processing units, sample and hold capacitors and attenuator voltage divider networks.

7.2 Signals ADC1

The ADC1's 8 input channels are used by the analog low-voltage port P2, the internal current sense amplifier and the VDH pin. The connected signals are shown in the following table.

Table 12 ADC1 channels

Channel	Signal	Pin
0	P2.0	29
1	CSA	Internal
2	P2.2	30
3	P2.3	35
4	P2.4	32
5	P2.5	31
6	VDH	Internal
7	NC	NA

7.3 ADC1 measuring principle

The channel input voltages are divided with a capacitive voltage divider down to the reference voltage level. This voltage divider consists of the internal sample and hold capacitor array. The reference voltage for ADC1 is the bandgap voltage (PMU-VBG). For all ADC1 channels, but channel 6 (VDH), this measurement principle results in a small current consumption (~10 µA), caused by internal switching currents. VDH has an additional resistive voltage divider, since VDH is a high-voltage pin.

7.4 ADC1 external components design

The external components used for VDH and the CSA are already described in chapter 9 and 11. For the remaining low-voltage inputs, an external anti-aliasing low-pass filter can be used. This filter limits the ADC channel input frequency to half the sampling frequency to fulfill the Nyquist criterion to prevent aliasing of the input signal. Figure 14 shows the block diagram of ADC1 and the external filter components.

The ADC consists of a multiplexer to switch the channel that should be measured during the actual sequence onto the ADC module. The ADC module consists of the resistance of the analog input path (R_{AIN}), the switched capacitance of the analog input path (C_{AINS}), two switches (S_1 and S_2) to decouple the ADC from the multiplexer inputs to charge the capacitor array (cap array) and the actual sample and hold ADC core (ADC_{CORE}).

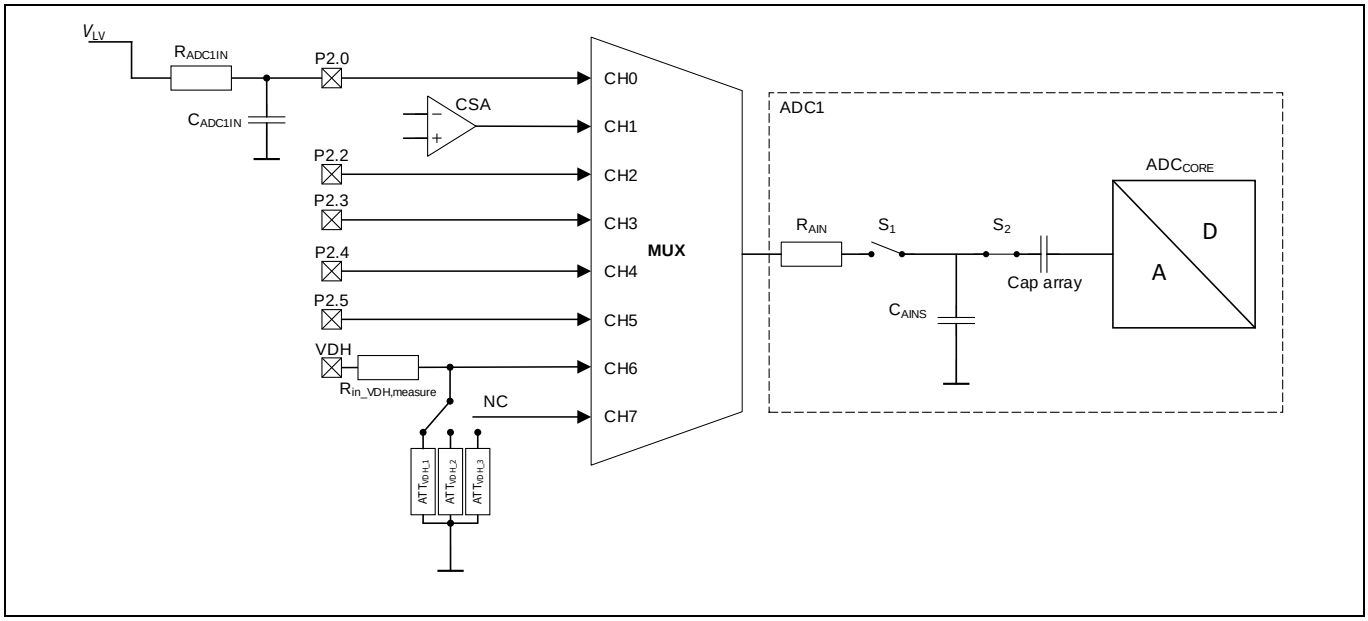


Figure 14 ADC1 block diagram and external components

7.4.1 Anti-aliasing filter design

The anti-aliasing filter has to be sized to the lowest expected sampling frequency. In the TLE987x the analog clock f_{ADCI} is used to sample the ADC. The cut-off frequency of the external low-pass filter is given with:

$$\frac{f_{ADCI}}{2} = \frac{1}{2\pi \times \sqrt{\tau_{ADC1IN} \times \tau_{IN}}}$$

With:

- $\tau_{IN} = R_{AIN} \times C_{AINS}$
- $\tau_{ADC1IN} = R_{ADC1IN} \times C_{ADC1IN}$

Resulting in a desired time constant for the external anti-aliasing filter of:

$$\tau_{ADC1IN} = \frac{1}{(f_{ADCI}\ x\ \pi)^2 \times \tau_{IN}}$$

With:

- f_{ADCI}(min) = 5 MHz and f_{ADCI}(max) = 24 MHz (P_9.2.4)
- R_{AIN} = 2 kΩ (P_9.2.16)
- C_{AINS} = 4 pF (P_9.2.15)
- Resulting in:
  - τ_{ADC1IN}(5 MHz) = 507 ns
  - τ_{ADC1IN}(24 MHz) = 22 ns

Table 13 Component selection for ADC1

Symbol	Function	Recommended component
RADC1IN	Resistor for anti-aliasing low-pass filter	Min. value 1 Ω (f_{ADCI} = 5 MHz) Max. value 2 Ω (f_{ADCI} = 24 MHz)
CADC1IN	Capacitor for anti-aliasing low-pass filter	Min. value 10 nF (f_{ADCI} = 24 MHz) Max. value 470 nF (f_{ADCI} = 5 MHz)

8 Sigma-delta analog digital converters (ADC3/4)

The TLE987x-2QX variants of the TLE987x have two integrated sigma-delta analog to digital converters (SDADC) with 14-bit resolution to monitor signals with highest accuracy requirements.

8.1 Software settings and hardware considerations

The SDADCs can be used to build a sensor interface for an external AMR/GMR sensor. The connected signals are:

Table 14 SDADC signals

Signal	Pin
ADC3.P	29
ADC3.N	30
ADC4.P	31
ADC4.N	32

8.2 ADC3/4 measuring principle

The differential input channels are divided via a fixed capacitive stage down to the reference voltage level. The switched-capacitor integrators of the second-order sigma-delta demodulator run at a fixed frequency of 20 MHz. The integrator output is connected to a quantizer which toggles as soon as the integrator output reaches the SDADC reference voltage and resets the integrator via a feedback digital to analog converter. The modulated bit stream is then filtered by a third-order comb filter with an oversampling rate of up to 2048.

8.3 ADC3/4 external components design

An external filter circuit can be used for several purposes. The main applications would be to improve the SDADC performance by decreasing the signal noise and to protect the device from HF noise, which may couple into the sensor interface.

The filter has to be dimensioned by the user for a specific target sensor. A suitable sensor would be the XENSIV™ TLE5009 E2000 analog GMR angle sensor. The sensor interface is shown in the following figure.

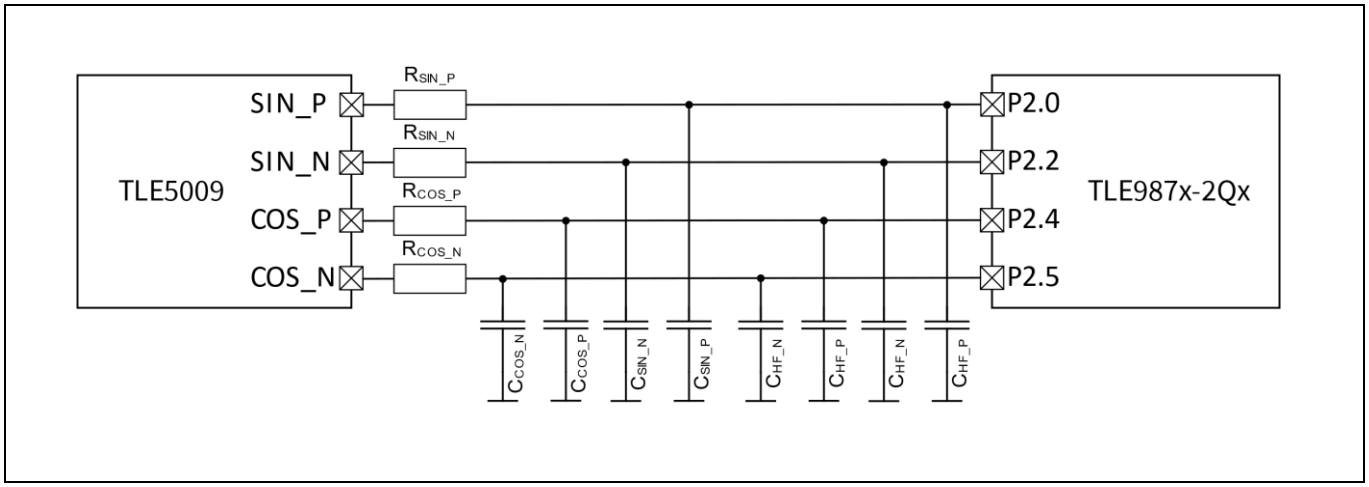


Figure 15 SDADC sensor interface

To improve the accuracy of the sensor interface, the cut-off frequency (f_C) for -3 dB attenuation has to be decreased. This will decrease the RMS output noise (V_{Noise}) of the SDADC for the maximal signal amplitude ($A_{X/Ydiff}$).

The original resolution of sensor is given with $A_{X/Ydiff}$ = 2.8 V and $V_{Noise}(f_C)$ = 3 mV

$$n = log_2 \times \left(\frac{A_{XYdiff}}{V_{Noise}(f_C)}\right) bit = log_2 \times \left(\frac{2.8\ V}{3\ mV}\right) bit \approx 10\ bit$$

The cut-off frequency of the SDADC can be changed with an external RC-filter to match the maximum input frequency of the SDADC (P_10.1.8), gaining resolution in the sensor while sacrificing bandwidth. Since the sensors RMS noise is pink-noise the spectral noise density is constant for different cut-off frequencies can be calculated with the formula below. With f_{new} = 2 × P_10.1.8 = 2 kHz the new RMS noise results in:

$$V_{Noise(f_{new})} = V_{Noise}(f_C) \times \sqrt{\frac{f_{new}}{f_c}} = 3\ mV \times \sqrt{\frac{2\ kHz}{30\ kHz}} = 775\ \mu V$$

Improving the resolution by 2 bits.

$$n = log_2 \times \left(\frac{A_{XYdiff}}{V_{Noise}(f_{new})}\right) bit = log_2 \times \left(\frac{3.7\ V}{775\ \mu V}\right) bit \approx 12\ bit$$

The time constant τ for the desired RC-filter is therefore given with:

$$\tau = R_{SINCOS} \times C_{SINCOS} = \frac{1}{2 \times \pi \times f_{new}} = \frac{1}{2 \times \pi \times 2\ kHz} = 80\ \mu s$$

With a dynamic input impedance (P_10.1.15) Z_{IN} = 250 kΩ and the maximum gain error G_{ERR} = 0.5% R_{SINCOS} is given with:

$$R_{SINCOS}(\max) = Z_{IN} \times G_{ERR} = 250\ k\Omega \times 0.5\% = 1.25\ k\Omega \approx 1\ k\Omega$$

Resulting in a C_{SINCOS} of:

$$C_{SINCOS} = \frac{\tau}{R_{SINCOS}} = \frac{80\ \mu s}{1\ k\Omega} = 80\ nF \approx 100\ nF$$

To protect the SDADC against HF coupling noise between 200 MHz and 500 MHz, the C_{HF} capacitors have be selected accordingly.

If R_{SINCOS} can be placed close to the TLE987x-2QX, the capacitor can be calculated with:

$$C_{HF} = \frac{1}{R_{SINCOS} \times 2\pi \times 500\ MHz} = \frac{1}{1\ k\Omega \times 2\pi \times 500\ MHz} = 3\ pF$$

If R_{SINCOS} cannot be placed close to the TLE987x-2QX or no RC-filter is used, the recommended value for C_{HF} is 470 pF.

Table 15 Component selection for SDADC

Symbol	Function	Recommended component
R_{SINCOS}	Resistor for resolution low-pass filter	1 kΩ
C_{SINCOS}	Capacitor for resolution low-pass filter	Ceramic capacitor **Min. value has to be calculated as described above** Voltage rating and dielectric type defined according to the application
C_{HF}	HF decoupling capacitor	Ceramic capacitor **Min. value 2 pF type: X7R** **Min. value 470 pF type: X7R** Voltage rating and dielectric type defined according to the application

9 Bridge driver (excluding charge pump)

The bridge driver is intended to drive external normal-level MOSFETs in bridge configuration. This chapter provides details about external components, which are needed depending on application requirements.

Detailed information about the bridge driver functioning and configuration is available in the Infineon application note “TLE986x/TLE987x Bridge Driver”.

9.1 Application diagram

The following application diagram shows the gate drivers for one half-bridge with the (partially optional) external components, which are described in this chapter.

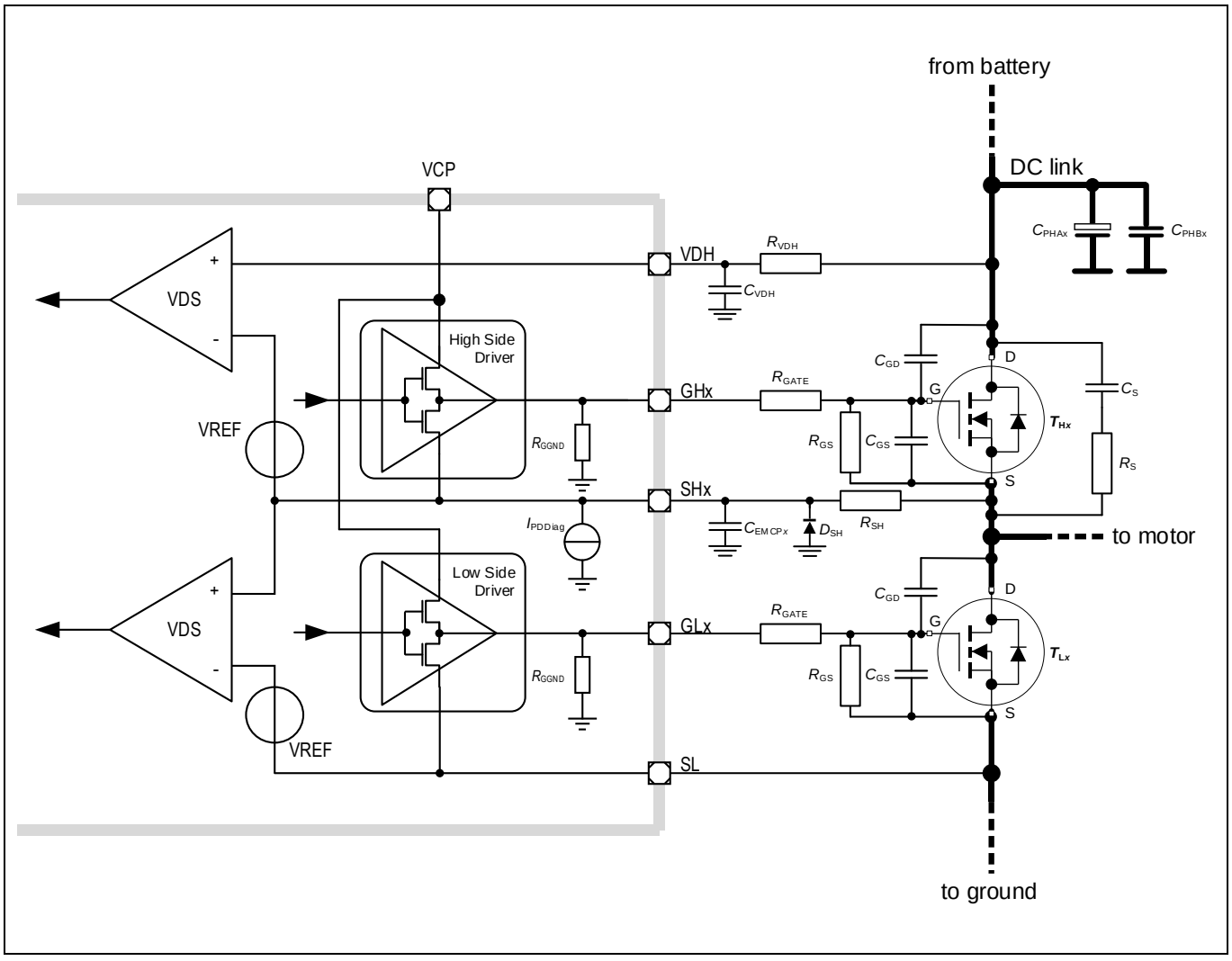


Figure 16 Gate drivers for one half-bridge with external components

9.2 External components

Component	Short description	Recommended value
R_{GATE}	**Gate resistor (optional):** suppresses potential oscillations between PCB line inductances and MOSFET capacitances	2 … 10 Ω
R_{GS}	**Gate-to-source resistor:** terminates the MOSFET gate	100 kΩ
C_{GS}	**Gate-to-source capacitor (optional):** linearizes the intrinsic MOSFET gate-to-source capacitor	Depends on MOSFET
C_{GD}	**Gate-to-drain capacitor (optional):** linearizes the intrinsic MOSFET gate-to-drain capacitor	
C_{PHAx}	**DC link capacitor A:** buffers DC link voltage	Depends on application requirements
C_{PHBx}	**DC link capacitor B:** suppresses double-digit MHz oscillations	
R_S, C_S	**Snubber (optional):** reduces voltage peaks and ringing at motor pin	
C_{EMCPx}	**EMC filter capacitor at the SHx pin:** suppresses fast transients at SHx	1 nF
R_{VDH}, C_{VDH}	**Low-pass filter at the VDH pin:** suppresses high-frequency components of DC link voltage	1 kΩ, 1 … 3.3 nF
D_{SH}	**Protection diode at the SHx pin (optional):** limits SHx undershoot voltages	–
R_{SH}	**Source resistor at the SHx pin (optional):** suppresses potential oscillations from motor phase to SHx pin and synchronizes the gate channel	2 … 10 Ω

Gate resistor

The optional gate resistor R_{GATE} suppresses potential oscillations between PCB line inductances and MOSFET capacitances, which build up an LC oscillator that can be stimulated by fast transients during MOSFET switching. The value of R_{GATE} depends on the PCB layout conditions, MOSFET parasitics, and switching speed, but should be as small as possible, preferably in the range from 2 Ω to 10 Ω.

Gate-to-source resistor

The gate-to-source resistor R_{GS} terminates the gate of the external MOSFET to its source. It should be placed as close as possible to the MOSFET to keep it turned off, for example, in the case of electromagnetic interference (EMI) or broken PCB lines. The recommended value is 100 kΩ.

Gate-to-source capacitor

The optional gate-to-source capacitor C_{GS} linearizes the intrinsic MOSFET gate-to-source capacitors and reduces the tolerance of the total gate-to-source capacitance seen by the gate driver. The value of C_{GS} should be large enough to dominate the intrinsic MOSFET gate-to-source capacitance C_{GS_int}.
The recommendation is: $C_{GS} \geq 2 \times C_{GS\_int}$.

Notes:

1. *The maximum gate charge Q_{tot_max} per MOSFET including the external gate capacitors must not exceed 100 nC for VQFN variants and 150 nC for TQFP variants.*
2. *C_{GS_int} is usually not directly given in MOSFET datasheets, but can be estimated from parameters like C_{iss} or Q_{gs}.*

Gate-to-drain capacitor

The optional gate-to-drain capacitor C_{GD} linearizes the intrinsic MOSFET gate-to-drain capacitor and reduces the tolerance of the total gate-to-drain capacitance seen by the gate driver. The placement of C_{GD} is recommended, if it is important for the application to have a well-controlled linear slew rate at the SHx pin: $\Delta V_{SHx} / \Delta t = I_{GATE} / C_{GD}$.

Notes:

1. *The maximum gate charge Q_{tot_max} per MOSFET including the external gate capacitors must not exceed 100 nC for VQFN variants and 150 nC for TQFP variants.*
2. *In order to avoid unintended switch-on of the MOSFET during fast transients, the following condition must be met: $C_{GD} / C_{GS} \leq 1 / 10$.*

DC link capacitors

The DC link capacitors C_{PHAx} and C_{PHBx} serve two purposes:

1. C_{PHAx} serves as a buffer capacitor
2. C_{PHBx} suppresses double-digit MHz oscillations on the DC link voltage

The total value of all DC link capacitors $C_{PH\_tot} = \sum (C_{PHAx} + C_{PHBx})$ depends on the acceptable DC link voltage ripple caused by PMW operation and on additional application-specific requirements, like having motors operating in generator mode or the need to buffer the motor energy in the case of an emergency shutdown of the MOSFETs.

Note: *C_{PH_tot} must be large enough to always keep all connected input pins (for example, VDH, VSD) within their absolute maximum ratings.*

As a starting point for the value of C_{PH_tot}, a rule of thumb is 230 µF per 10 A motor current. The bigger part of the capacitance is covered by electrolytic capacitors C_{PHAx} and the rest by ceramic capacitors C_{PHBx}. It is recommended to choose capacitors with low ESR and low self-inductance and place them close to their respective high-side MOSFETs, in order to minimize series resistances and inductances in the high-current path.

Snubber

The optional snubber R_S and C_S reduces voltage peaks and ringing at the motor pin, which can be caused by PCB parasitics like series inductances. The values for R_S and C_S depend on the half-bridge power ratings and on the parasitics of the selected MOSFET.

Starting values for R_S and C_S can be derived from the following constraints:

- $R_S \leq V_{DClink} / I_{motor}$ in order to keep the voltage across R_S always smaller than the DC link voltage
- $C_S \geq 2 \times C_{oss}$, where C_{oss} is the output capacitance of the MOSFET

Notes:

1. *For R_S a resistor with very low self-inductance should be chosen. The resistor power class can be derived from the maximum energy stored in C_S.*
2. *For C_S a capacitor with high peak-current capability should be chosen.*

EMC filter capacitor at the SHx pin

The EMC filter capacitor C_{EMCPx} at the SHx pin suppresses fast transients coming from the motor pin. The recommended value is 1 nF. This capacitor should be placed as close as possible to the SHx pin.

Low-pass filter at the VDH pin

The low-pass filter R_{VDH} and C_{VDH} at the VDH pin suppresses high-frequency components on the DC link voltage. The VDH input serves as the reference voltage of the high-side drain-source comparators and should be stable right after each MOSFET switching event. Therefore, a time constant in the range of a low single-digit µs value should be targeted, for example: R_{VDH} = 1 kΩ and C_{VDH} = 1 nF.

Note: *R_{VDH} performs an additional protection role by limiting the current out of the VDH pin in the case of a reverse-polarity event or other undershoots of the DC link voltage.*

Protection diode at the SHx pin

The optional protection diode at the SHx pin limits SHx undershoot voltages. This diode is only recommended if undershoots below the absolute maximum ratings may be expected due to unknown application conditions.

Source resistor at the SHx pin

The optional source resistor at the SHx pin serves two purposes:

- It suppresses the potential oscillations from the motor phase to SHx pin
- It synchronizes the gate channel with small RC filter (τ_{max} = 500 ns)

The recommended value for R_{SH} is in the range from 2 to 10 Ω.

10 Charge pump

The charge pump is intended to supply the bridge driver integrated in the TLE987x/6x, as well as the Back-EMF comparators. The purpose of this chapter is to provide a design method for the external capacitors, depending on the application requirements.

10.1 Application diagram

The following application diagram shows the charge pump and its external components, which are the flying capacitors CCPS1 / CCPS2 and the output capacitor CVCP. The input voltage of the charge pump is VSD, while the output voltage is VCP.

V_{DC} is the DC-link voltage after the MOSFET for reverse polarity protection. An RC network can be optionally placed between V_{DC} and VSD. C_{VSD} is acting as filter capacitor, while R_{VSD} limits the current flowing into VSD during voltage transients. The recommended values for C_{VSD} and R_{VSD} are 1 µF and 2 Ω.

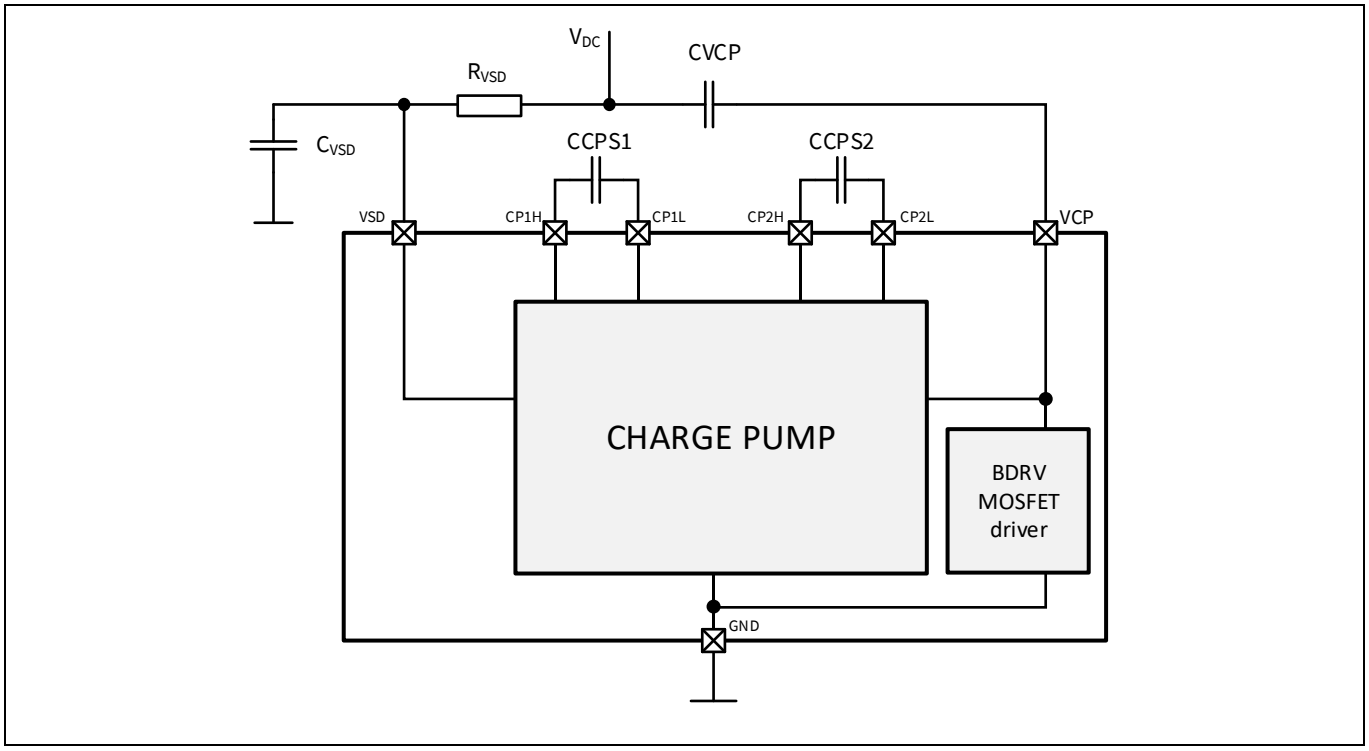


Figure 17 Charge pump application diagram

10.2 Charge pump: how it works

The voltage VCP is generated by a 2-stage charge pump, as a multiplying effect of the input voltage VSD using two flying capacitors CCPS1 and CCPS2: ideally, each stage of the charge pump can provide a voltage increase equal to the input voltage. The output capacitor CVCP acts as bulk for the voltage VCP. A detailed description of the behavior of an n-stage charge pump is available in the following literature:

- “On-Chip High-Voltage Generation in Integrated Circuits Using an Improved Multiplier Technique” by J.F. Dickson
- “Theoretical and Experimental Analysis of Dickson Charge Pump Output Resistance” by A. Cabrini, L. Gobbi, and G. Torelli

The switches of the charge pump are driven by an internal clock (CLK) with a frequency equal to f_{SW}, derived from the TLE987x/6x system clock. The following pattern applies (Figure 18):

- **Clock set to low:** the capacitor CCPS1 is charged by VSD, while the energy of CCPS2 is transferred to the output, boosting the voltage VCP of the capacitor CVCP. Considering V_{DROP1} as the voltage drop of the switches of the first stage and ignoring the load current, the average voltage VCPS1 can be expressed as:

$$VCPS2 = 3\,VSD - V_{DROP2} \quad ; \quad VCP = 3\,VSD - V_{DROP}$$

  Where: V_{DROP} as the is the total voltage drop of the switches of the charge pump.
- **Clock set to high:** the energy is transferred from CCPS1 to CCPS2, while the output voltage VCP is buffered by the bulk capacitor CVCP. Considering V_{DROP2} as the voltage drop of the switches of the first and second stage and ignoring the load current, the average voltages VCPS2 and VCP can be expressed as:

$$VCPS1 = 2\,VSD - V_{DROP1}$$

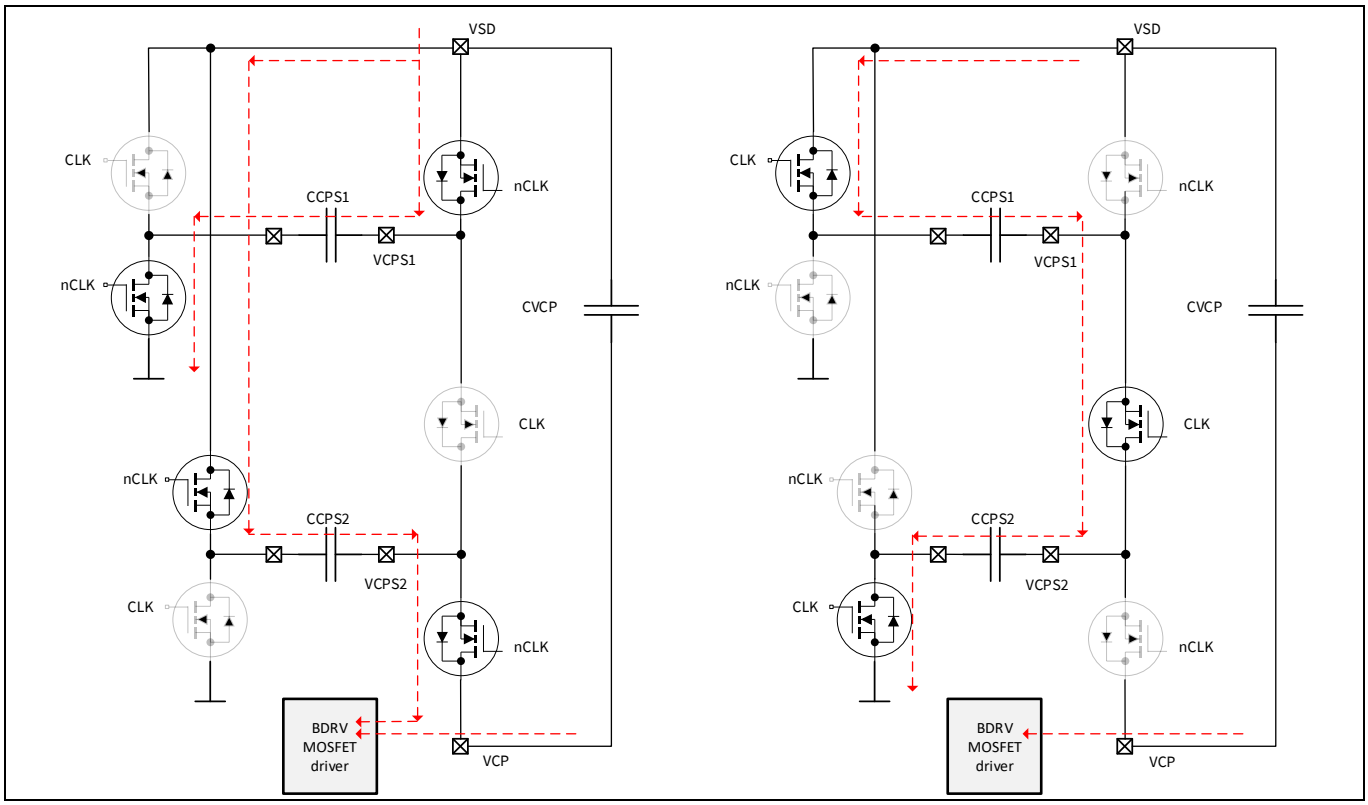


Figure 18 Basic scheme of the charge pump (left: clock set to low; right: clock set to high)

Including now the load current in the calculation, the output voltage VCP can be expressed as:

Equation 1:

$$VCP = 3\,VSD - V_{DROP} - R_{OUT\_AVG} \times ICP$$

Where:

- ICP is the average output current, as sum of the bias current of the bridge driver and the total current needed to drive the MOSFETs gates
- R_{OUT_AVG} is the average output resistance of the charge pump, which can be expressed as:

Equation 2:

$$R_{OUT\_AVG} \approx \frac{2}{f_{SW} \times CCPS} + \frac{3}{4 \times f_{SW} \times CVCP}$$

Where:

- f_{SW} is the switching frequency of the charge pump, and CCPS1 and CCPS2 are both equal to CCPS

Considering:

Equation 3:

$$V_{DROP} = ICP \times R_{EQ}$$

The Equation 1 can be re-arranged as follows:

Equation 4:

$$VCP = 3 \times VSD - ICP(R_{EQ} + R_{OUT\_AVG})$$

Where:

- R_{EQ} is an average resistance, which takes into account the total voltage drop V_{DROP} in respect to the output current. A value of R_{EQ} fitting to the charge pump implemented in the TLE987x is about 100 Ω.

Figure 19 shows the equivalent circuit as expressed by the Equation 4.

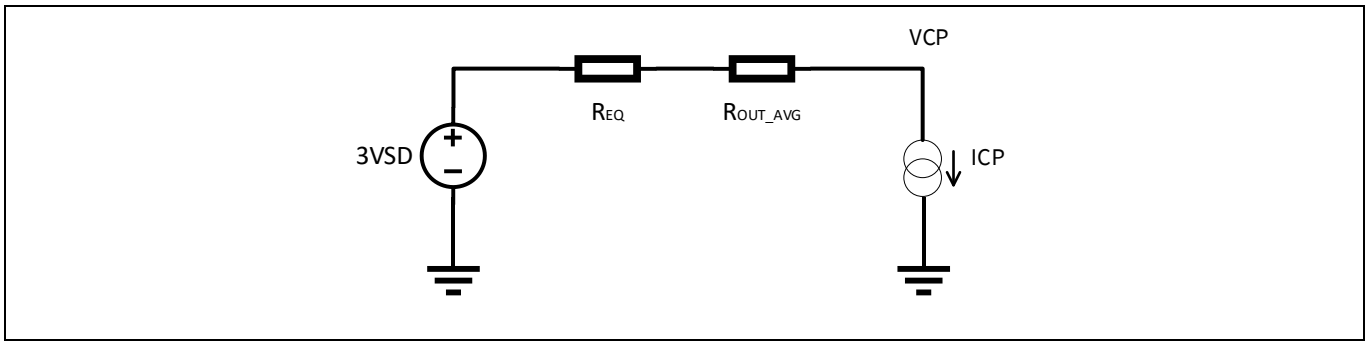


Figure 19 Charge pump equivalent circuit

Considering the wide range of the input voltage VSD, the charge pump of the TLE987x limits the output voltage VCP according to the following relations:

$$VCP - VSD \cong \begin{cases} 14\,V & if \;\; VCP - VSD \geq 14\,V \\ VCP - VSD & if \;\; VCP - VSD < 14\,V \end{cases}$$

Note: *Important to note is that the above equations are aiming to provide an equivalent model of the charge pump considering average values of the electrical parameters, not RMS (root medium square) values.*
For this reason, they should not be used straightforward to calculate the power dissipation of the charge pump itself.

10.2.1 ICP load current calculation

The load current ICP of the charge pump is the sum of the currents supplied to each gate, and the bias current of the bridge driver. In Figure 20 the gate charge and discharge current paths are shown. Referring to this figure, the following equations can be derived:

Equation 5:

$$ICP = N_G \times (ICP_M + I_{BIAS})$$

Equation 6:

$$ICP_M = N_M \times f_{PWM} \times Q_M$$

Equation 7:

$$Q_M = Q_{MOSFET} + CGS_{ext} \times VGS + CGD_{ext} \times VGD$$

Where:

- N_G is the number of half-bridge drivers active in one PWM switching period. This value depends on the PWM switching scheme and the control technique used in the application. Considering a 3-phase motor, N_G is equal to 1 with block commutation, while N_G is equal to 3 with FOC (field-oriented control)
- ICP_M is the current of each half-bridge gate driver
- I_{BIAS} is the bias current of each single half- bridge driver. A typical value for I_{BIAS} is about 2 mA
- N_M is the number of MOSFETs turned on in one PWM switching period. This value depends on the PWM switching scheme and the control technique used in the application. For block commutation and FOC N_M is equal to 2
- f_{PWM} is the PWM switching frequency
- Q_M is the total charge transferred to the high-side (HS) and/or low-side (LS) gate, including the charge of external capacitors
- Q_{MOSFET} is the gate charge of the HS (and/or LS) gate present at a certain VGS
- CGS_{ext} is the value of the external gate to source capacitance
- VGS is the gate to source voltage
- CGD_{ext} is the value of the external gate to drain capacitance
- VGD is the gate to drain voltage

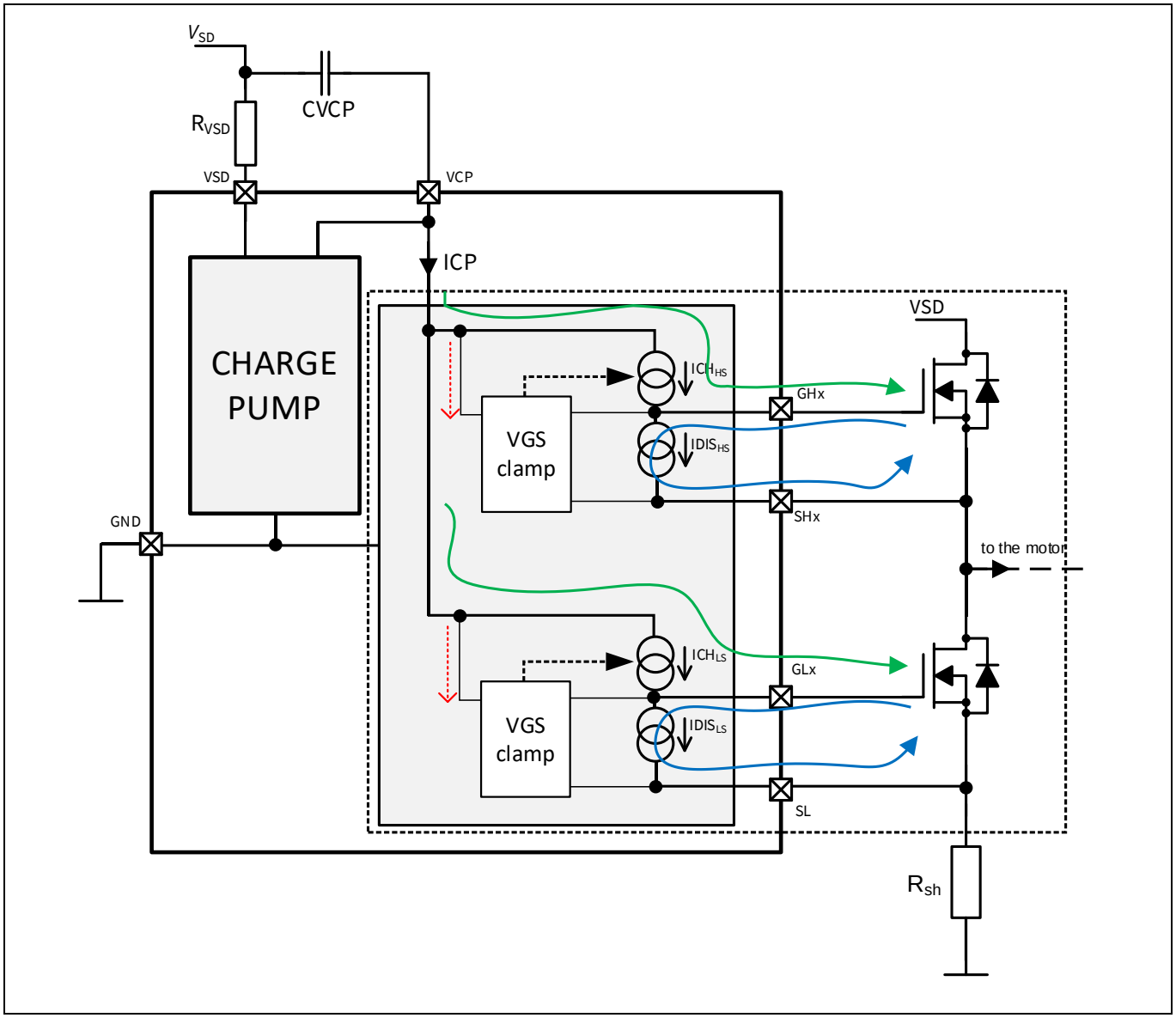


Figure 20 Schematic representation of the high-side and low-side MOSFET gate charge (green) and discharge (blue) currents paths (left). Bias current in red. Each gate driver block is repeated 3× in the TLE987x, while 2× in TLE986x

The gate charge Q_{MOSFET} can be determined from the characteristics of the MOSFET. A typical gate charge graph of an automotive Infineon MOSFET (IAUA120N04S5N014) is shown in the Figure 21.

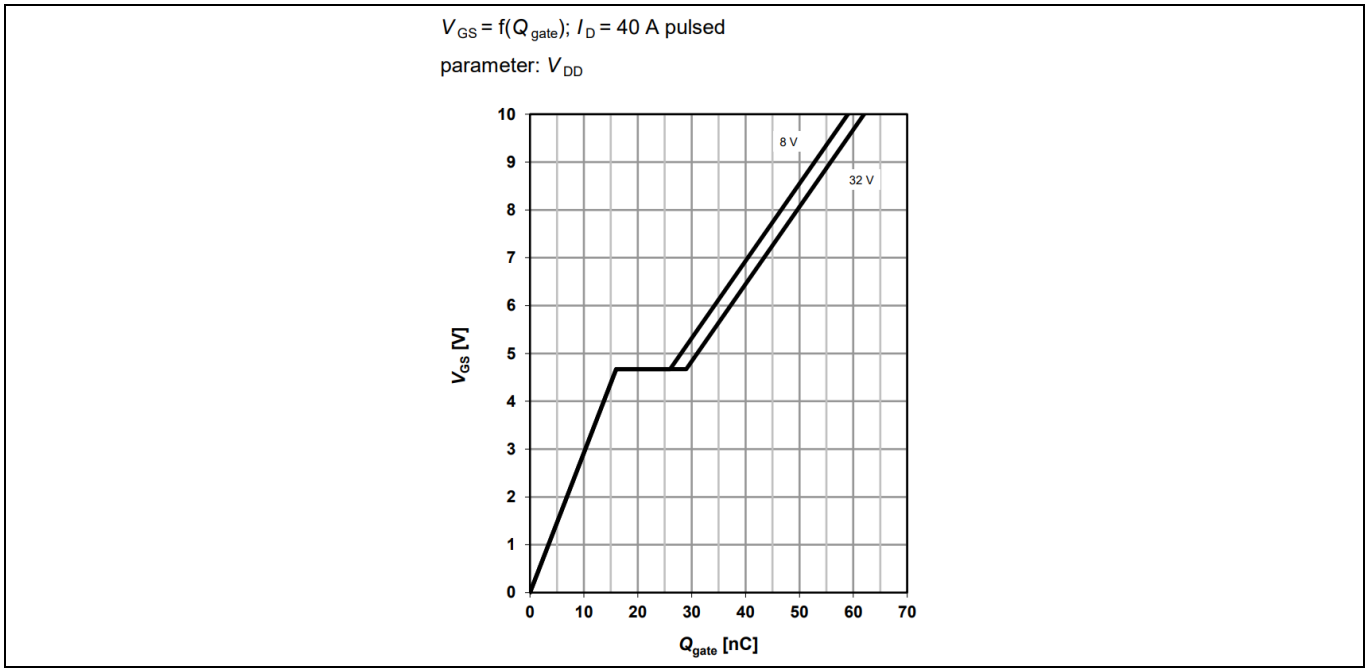


Figure 21 Gate charge of the IAUA120N04S5N014

In the bridge driver implementation of the TLE987x/6x, the HS and LS gate source voltages VGS are limited by an internal clamping. In Figure 22 a simplified schematic of the bridge driver is illustrated. It can be assumed that the MOSFETs ON-resistances and the current sensing resistor R_{sh} are in the order of magnitude of [mΩ]. As a consequence the following approximations can be made:

- When **HSx** is **ON** and **LSx** is **OFF** → VPHx ≅ VSD
- When **LSx** is **ON** and **HSx** is **OFF** → VPHx ≅ VSL ≅ GND

Taking this into account, the typical average VGS_{HS} (for the HS) and VGS_{LS} (for the LS) voltages can be estimated as:

Equation 8:

$$VGS_{HS} \cong \begin{cases} 12.5\,V & if\ VCP - VSD \geq 14\,V \\ VCP - VSD - 1.5\,V & if\ VCP - VSD < 14\,V \end{cases}$$

$$VGS_{LS} \cong \begin{cases} 12.5\,V & if\ VCP \geq 14\,V \\ VCP - 1.5\,V & if\ VCP < 14\,V \end{cases}$$

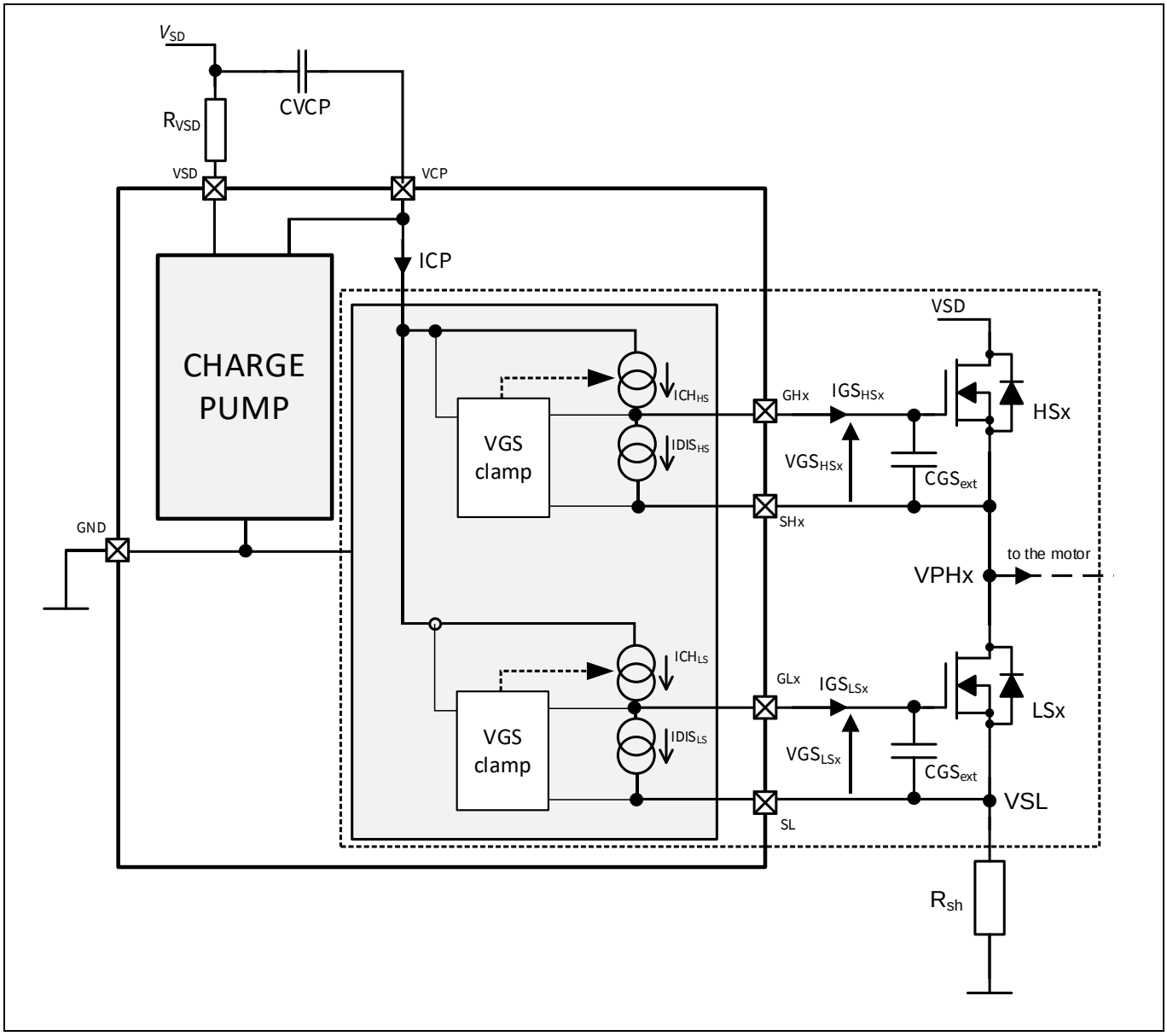


Figure 22 Simplified BDRV block diagram with highlight on gate-source voltage clamping. Each gate driver block is repeated 3× in the TLE987x, while 2× in the TLE986x

A calculation example is provided here below, where no capacitors are connected to the MOSFETs gates and FOC control with a 3-phase motor is used. For sake of simplicity, we can assume VGS to have the same value for HS and LS, as well as to be independent from ICP.

- Assumptions:

$$N_M = 2 \quad ; \quad f_{PWM} = 20\ kHz \quad ; \quad Q_{MOSFET} \cong 60\ nC \quad ; \quad VGS = 12.5\ V$$

- Considering VGS is equal to 12.5 V, the gate charge shall be consequently increased, since the 60 nC are estimated for VGS = 10 V:

$$Q_{MOSFET} \cong 60\ nC \times \frac{12.5\ V}{10\ V} = 75\ nC$$

- The current for each gate driver is equal to:

$$ICP_M = N_M \times f_{PWM} \times Q_{MOSFET} \cong 3\ mA$$

- The total ICP current is:

$$ICP = 3 \times (ICP_M + I_{BIAS}) \cong 15\ mA$$

Another calculation example is provided here below, where a capacitor is placed between gate and source, and no capacitor between gate and drain is connected. The control scheme is always FOC. For sake of simplicity, we can assume VGS and VGD to have the same value for HS and LS, as well as to be independent from ICP.

- Assumptions:

$$N_M = 2 \quad ; \quad f_{PWM} = 20\ kHz \quad ; \quad Q_{MOSFET} = 60\ nC$$
$$VGS = VGD = 12.5\ V \quad ; \quad CGS_{ext} = 1\ nF$$

- The charge for each gate is then:

$$Q_M = 60\ nC \times \frac{12.5\ V}{10\ V} + 12.5\ V \times 1\ nF \cong 88\ nC$$

- The current for each gate driver is equal to:

$$ICP_M = N_M \times f_{PWM} \times Q_M \cong 3.5\ mA$$

- The total ICP current is:

$$ICP = 3 \times (ICP_M + I_{BIAS}) \cong 16.5\ mA$$

10.3 Charge pump external capacitors design

The flying capacitors CCPS1 and CCPS2 boost the input voltage VSD to generate the output voltage VCP, while the output capacitor CVCP is acting as bulk capacitor. The selection of the values and type should consider the following requirements:

- **VCP voltage in steady state**: as shown in the Equation 1, the output voltage depends also on the value of the charge pump capacitors.
- **Voltage ripple**: the ripple of the flying capacitors can be expressed as:

Equation 9:

$$V_{ripple} = \frac{ICP}{f_{SW} \times C}$$

Where:

- C is the value of the capacitor

The voltage ripple of the output capacitor CVCP is equal to the one of the flying capacitors, but divided by 2.

- **Dynamic response**: the higher the value of the capacitors, the slower will be the start-up time and the response to load changes. In a typical TLE987x/6x application, this requirement is not critical
- **Losses due to ESR** (equivalent series resistance): the higher the value of the capacitors, the higher will be the ESR and so the losses. Using ceramic capacitors, the losses can be considered as not relevant in this application
- **DC bias voltage**: ceramic capacitors exhibit lower capacitance values, when the applied voltage increases. According to the point of load and the desired capacitance value, the voltage rating should be adequately selected. For a typical application, 50 V capacitors are recommended

A method to select the charge pump capacitors

1. Define the type of MOSFETs of the application
2. Define the switching frequency f_{PWM} of the bridge driver
3. Calculate the load current ICP, as described in the Equation 5
4. Calculate the preliminary values of CCPS and CVCP using the Equation 9. As a rule, we can consider a maximum ripple of 0.5 V for the flying capacitors CCPS and 0.25 V for CVCP. Moreover, at least 50% higher capacitance should be taken into account of the DC bias
5. Calculate R_{OUT_AVG} using the Equation 2
6. Calculate V_{DROP} using the Equation 4
7. Calculate VCP voltage using the Equation 4
8. Calculate the voltage VCP vs. VSD using the Equation 8, checking that the gates are driven with a sufficient voltage in the input voltage range VSD, as required by the application.

The recommended values are 220 nF for the flying capacitors (CCPS1 / CCPS2), and 470 nF for the output capacitor (CVCP). These values allow to have a VCP voltage sufficiently high within the nominal working conditions of the charge pump, as well as a low voltage ripple in the load current range.

10.3.1 Calculation example

A calculation example is provided here below.

1. Identify the MOSFETs, for example: IAUA120N04S5N014
2. Define the switching frequency:

$$f_{PWM} = 20\ kHz$$

3. Calculate ICP, considering VGS = 12.5 V, N_M = 2, and no external capacitors connected to the gates:

$$ICP \cong 15\ mA$$

4. Calculate preliminary values for CCPS and CVCP, considering a charge pump frequency of 250 kHz and a voltage ripple of 0.4 V and 0.2 V for CCPS and CVCP respectively:

$$CCPS = 150\ nF \rightarrow +50\% \rightarrow 220\ nF$$

$$CVCP = 300\ nF \rightarrow +50\% \rightarrow 470\ nF$$

5. Calculate R_{OUT_AVG}:

$$R_{OUT\_AVG} = 43\ \Omega$$

$$ICP \times R_{OUT_{AVG}} \cong 0.65\ V$$

6. Calculate the voltage drop:

$$V_{DROP} = ICP \times R_{EQ} \cong 1.5\ V$$

7. Calculate VCP versus VSD:

$$VCP - VSD \cong 2 \times VSD - 2.2\ V$$

8. Considering from 8 V to 18 V as VSD voltage range, calculate the voltages VCP vs VSD, VGS_{HS} and VGS_{LS}:

	VCP-VSD	**VGS_{HS}**	**VGS_{LS}**
VSD = 18 V	14 V	12.5 V	12.5 V
12 V	14 V	12.5 V	12.5 V
10 V	14 V	12.5 V	12.5 V
8 V	13.8 V	12.3 V	12.5 V

From the table, the minimum VGS voltage is equal to 12.3 V, so the MOSFETs can be correctly driven in every condition.

11 Current sense amplifier

The current sense amplifier (CSA) is an analog circuit capable of amplifying the differential input voltage by a programmable gain G.

Despite being actually a voltage amplifier, it is specifically designed for shunt current measurements. For this purpose, the pins OP2 and OP1 are connected to the terminals of a suitably designed shunt resistor, through which the current to be measured flows, and a filter network.

11.1 Block diagram

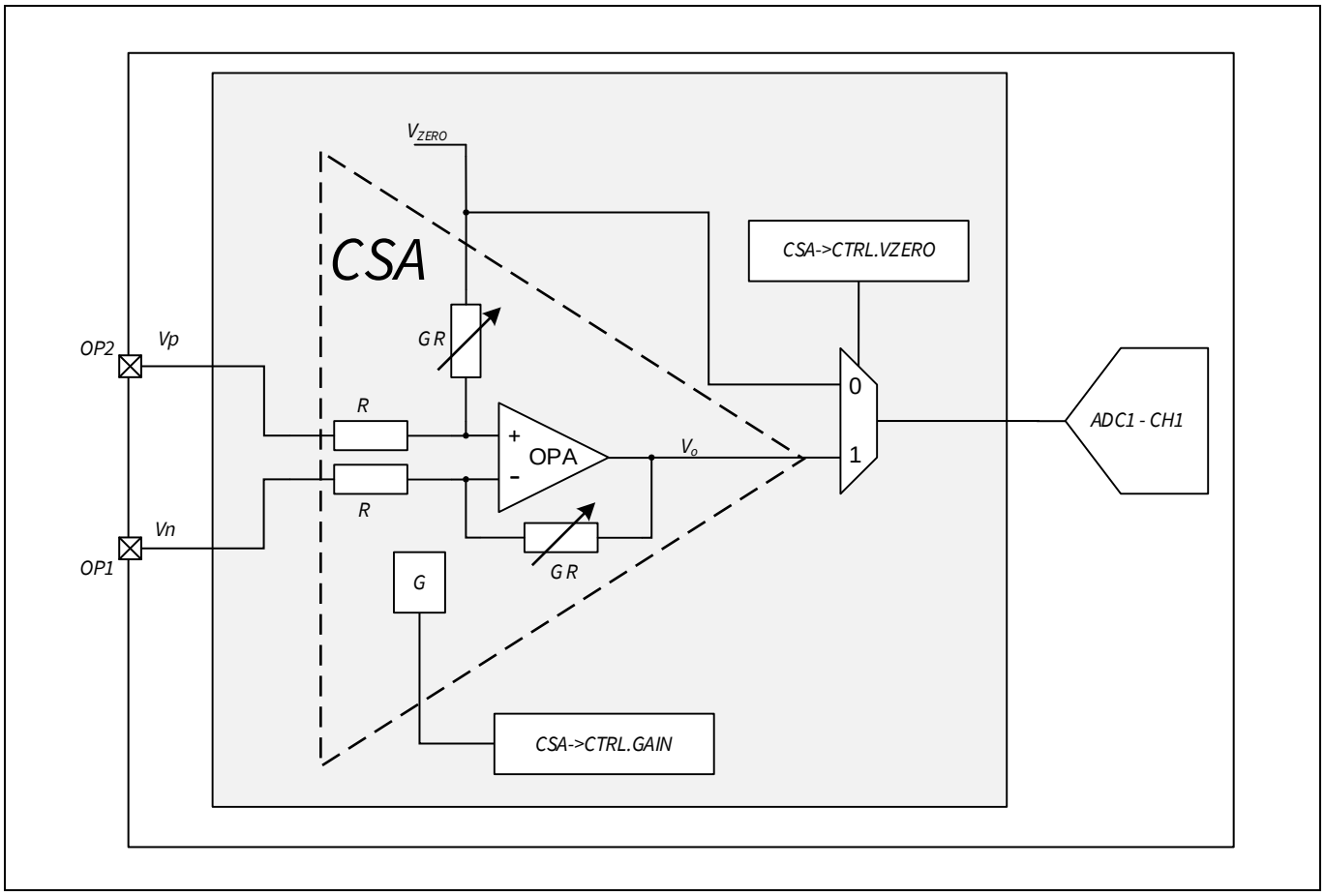


Figure 23 CSA block diagram and application schematic for shunt current measurement

11.2 Functional description

Figure 23 shows the block diagram of the CSA together with the registers and logic related to its setup.
The amplifier is built around an OPA configured as a differential amplifier with an output voltage offset.
The amplifier's output is permanently connected to the ADC1 channel 1, which means it is loaded by a fixed impedance. It is an integrated closed-loop amplifier and it can be used only as such. What follows will describe the entire CSA configuration and behavior.

11.3 DC characteristics

The **differential input voltage** is defined as:

$$V_{id} = OP2 - OP1 = V_p - V_n$$

The **ideal DC transfer characteristics** can be calculated as:

$$V_o = V_{ZERO} + G\ V_{id}$$

$$V_{ZERO} = 0.4\ VAREF$$

$$V_{id} = 0 \rightarrow V_o = V_{ZERO}$$

Where:

- V_{ZERO} is the **output voltage offset**
- VAREF is the reference voltage of ADC

If, for example, VAREF is generated by the internal reference voltage generator, its nominal value is 5 V. As a consequence V_{ZERO} = 2 V, which allows the ADC1 channel 1 to measure positive and negative values of V_{id}.

The **linear output voltage range** of the amplifier is (see P_13.1.4 of the datasheet):

$$min, \max\{V_o\} = V_{OUT} = V_{ZERO} \pm 1.5\ V$$

With the use of the internal VAREF generator, V_o can assume any value between 0.5 V and 3.5 V.

The V_o range limits the **differential linear input range**, which also depends on the gain setting according to (see P_13.1.1 of the datasheet):

$$min, \max\{V_{id}\} = V_{IX} = \pm 1.5\ V/G$$

Outside these ranges, the CSA characteristics are not linear and therefore undefined.

Because it is not an ideal circuit, the OPA exhibits **an input offset** V_{OS}. Because of this, the output voltage can be expressed by:

$$V_o = V_{ZERO} + G\ (V_{id} \pm V_{OS})$$

$$V_{id} = 0 \rightarrow V_o = V_{ZERO} \pm G\ V_{OS} = V_{ZERO} \pm V_{OOS}$$

This implies that the direct measurement of V_{ZERO} by means of CSA->CTRL.VZERO = 1 will differ from the value of V_o with V_{id} = 0 with CSA->CTRL.VZERO = 0. This difference equals to the **output offset** V_{OOS} (see parameter P_13.1.17). The measurements can be used to calculate this difference in the application software and to compensate the offset.

The **common mode input voltage** is defined as:

$$V_{icm} = \frac{OP2 + OP1}{2} = \frac{V_p + V_n}{2}$$

Considering also the contribution of V_{icm} and **the common mode rejection ratio** DC_CMRR (see parameter P_13.1.8 for grade 1 devices in conjunction with P_13.1.27 for grade 0 devices) the **DC characteristics** can be expressed as:

$$V_o = V_{ZERO} \pm V_{OOS} + G\ (V_{id} + V_{icm}/CMRR_{lin})$$

$$CMRR_{lin} = 10^{\frac{DC\_CMRR}{20}}$$

Figure 24 shows a graphical representation of the **differential DC characteristics** and the input/output range.

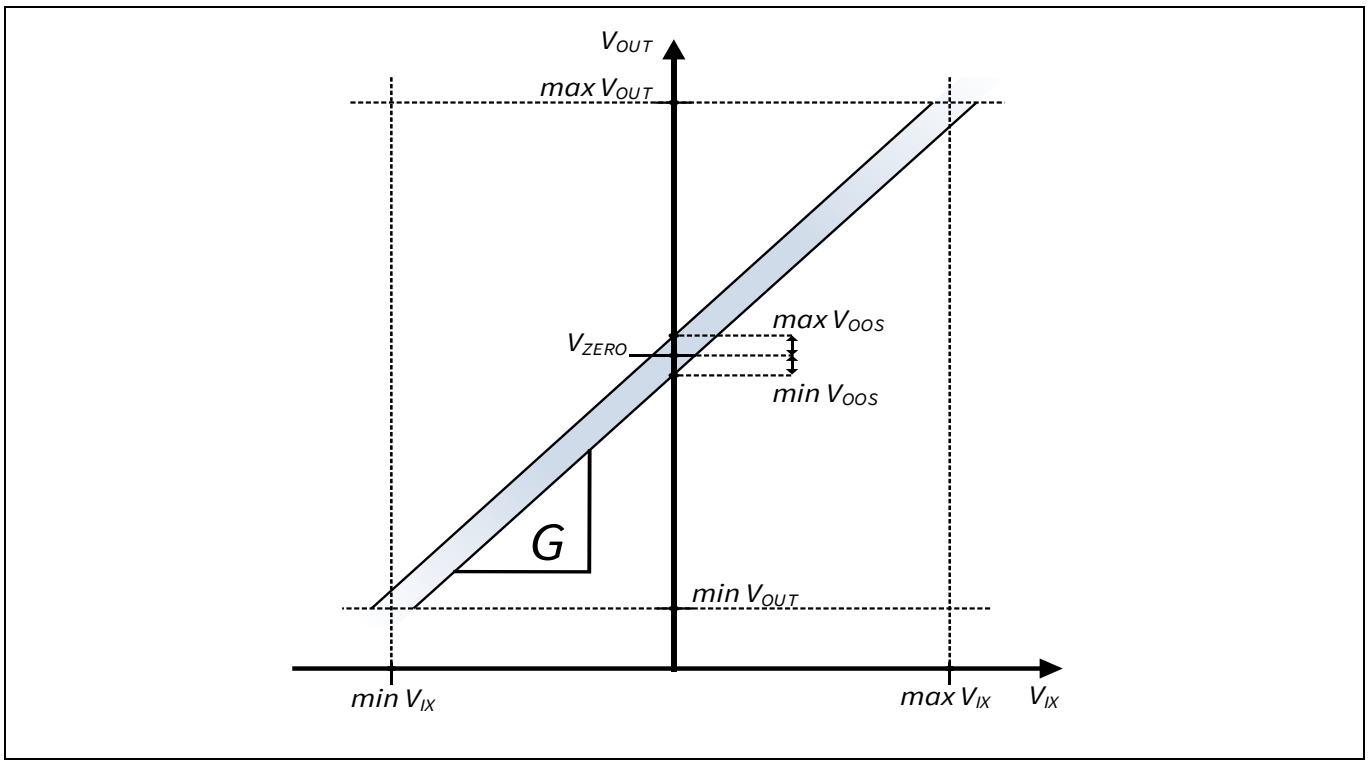


Figure 24 Differential DC characteristics

11.3.1 AC characteristics

The CSA can be modeled as a three-port network with two input ports and one output port, as shown in Figure 25. The two input ports represent OP2 and OP1, while the output port represents V_{OUT}. Voltages for all three ports are referred to the ground potential GND.

By considering the specific characteristics of the CSA, the three-port network can be expressed as:

Equation 10:

$$\begin{cases} v_o = A_d v_{id} + A_{cm} v_{icm} \\ v_p = Z_{pp} i_p + Z_{pn} i_n \\ v_n = Z_{np} i_p + Z_{nn} i_n \end{cases}$$

Where:

Equation 11:

$$\begin{cases} v_{id} = v_p - v_n \\ v_{icm} = \dfrac{v_p + v_n}{2} \end{cases}$$

The first equation in Equation 10 represents the output behavior, while the other two represent the input behavior of the CSA. The nominal value of the input impedances can be expressed as:

$$Z_{pp} = \left.\frac{v_p}{i_p}\right|_{i_n=0} = (G+1)R \quad Z_{pn} = \left.\frac{v_p}{i_n}\right|_{i_p=0} = 0$$

$$Z_{np} = \left.\frac{v_n}{i_p}\right|_{i_n=0} = G\,R \quad Z_{nn} = \left.\frac{v_n}{i_n}\right|_{i_p=0} = R$$

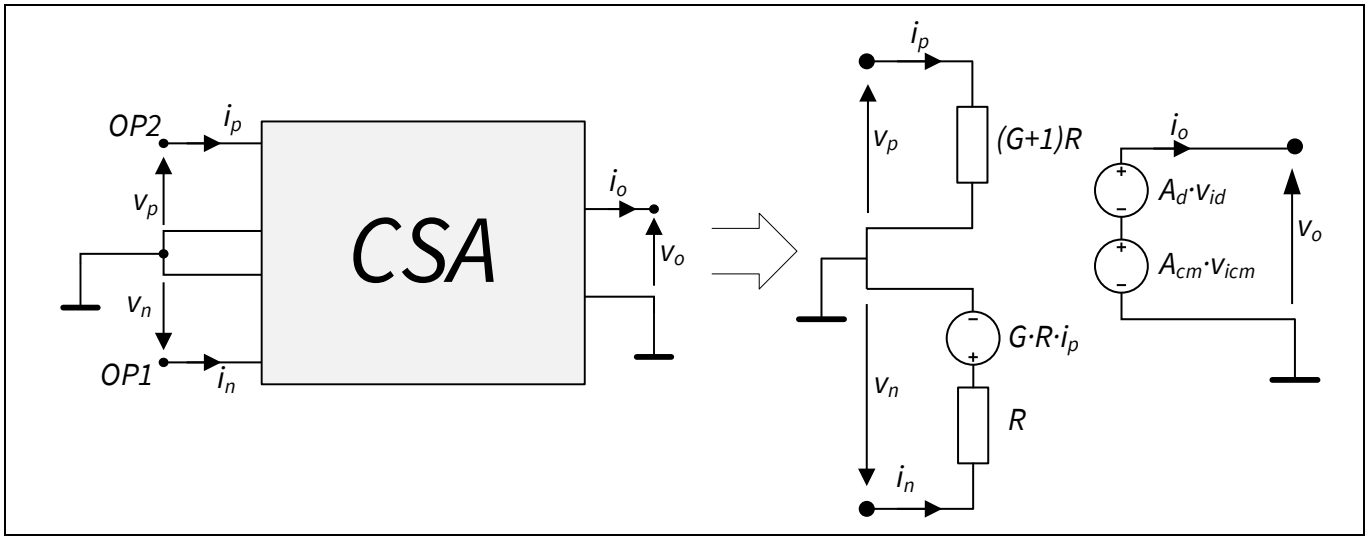


Figure 25 CSA AC simplified three-port model

Figure 25 shows a schematic representation of the input equations and its impedances. This representation together with the equations are necessary to design the external current-sensing and filtering network.

The resistors R have nominal values of 1.25 kΩ (see P_13.1.25 of the datasheet) and G changes according the programmed gain.

The closed-loop nature of the CSA ensures the user that the stability is guaranteed in any application condition. The **open-loop transfer function** of the CSA together with its **gain and phase margins** are designed and fixed for each G gain configuration. Therefore, only the **closed-loop** transfer functions are described here.

The **DC common mode gain** can be derived from the CMRR as:

$$A_{cm} = \frac{A_d}{CMRR}$$

The typical **AC differential gain transfer function** is shown in Figure 26 and defined as:

$$A_d(s) = \frac{v_o(s)}{v_{id}(s)}$$

A simplified analytical expression for each transfer function can be used in order to identify the typical frequency and time-domain parameters. A dominant-pole approximation of $A_d(s)$ is:

$$A_d(s) = \frac{v_o(s)}{v_{id}(s)} \approx \frac{G}{\left(\frac{s}{\omega_p} + 1\right)^4}$$

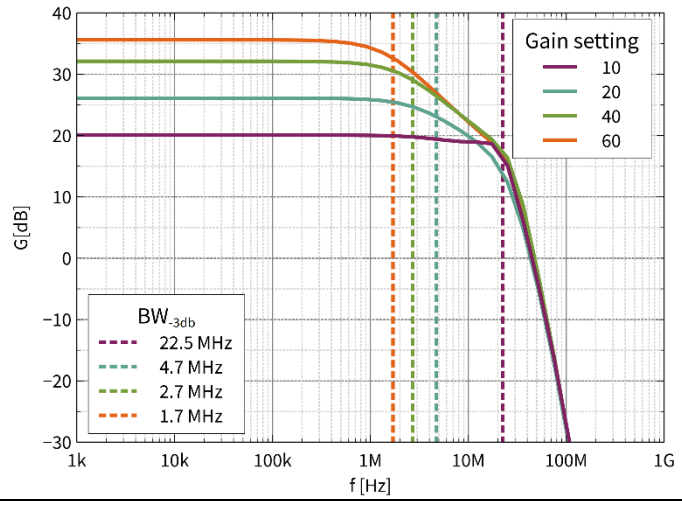


Figure 26 AC differential gain transfer function

The typical values of ω_p for each gain setting are shown in Table 16. Being a 4th-order transfer function, its step response in the time domain has a fairly complex analytical expression. However, the time constant τ_p and its relation to the settling time T_s can be defined as:

$$\tau_p = \frac{1}{\omega_p} \qquad T_s \approx 9\,\tau_p$$

The **settling time T_s** is defined as the time between the instant when the step is applied at V_{id} and the instant in which V_o remains confined within ±2% of its final value. Table 16 shows the values of the estimated typical T_s and τ_p for each gain setting.

Table 16 Typical values for gain settings

Gain [V/V]	10	20	40	60
ω_p [Mrad/s]	50	27	17	12
τ_p [ns]	20	37	57	84
Settling time [ns]	185	330	520	760

11.4 Application hints

The CSA is designed to measure the differential voltage across a shunt resistor through which the current to be measured flows. A typical circuit implementation of the sensing network is shown in Figure 27.

Because of the parasitic inductance introduced by the shunt resistor and the PCB traces, the signal across the shunt resistor presents spikes and ringings. This effect must be compensated by a filtering network as shown in Figure 27.

The following chapters describe a procedure for designing the shunt resistor and the filter network.

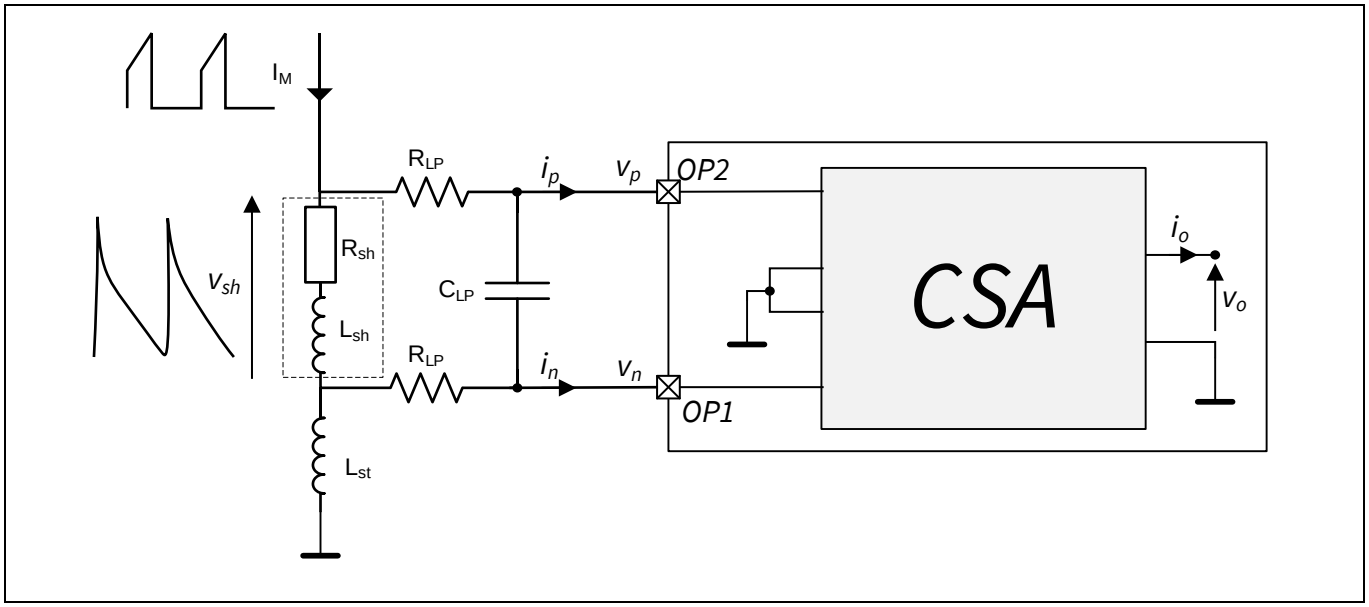


Figure 27 Typical circuit implementation

11.4.1 Shunt resistor selection

In a typical application, the input pins OP2 and OP1 are connected to an external shunt resistor so that:

$$V_{id} = R_{sh} I_M$$

$$V_o = V_{ZERO} + G\ R_{sh} I_M$$

Where:

- I_M is the current to measure
- R_{sh} is the nominal resistance of the shunt resistor

This equation represents the ideal DC behavior of the CSA, so it is only valid once all the dynamics of the system are eliminated. However, it is still a valid design equation for the choice of R_{sh} and G.

Indeed, because of the limited output voltage range of the CSA, one has to consider the behavior under maximum current:

$$V_o{}^{max} = V_{ZERO} + 1.5\ V > V_{ZERO} + G\ R_{sh} {I_M}^{max}$$

This leads to the **1st design equation**:

$$R_{sh} < {R_{sh}}^{max} = \frac{1.5\ V}{G\ {I_M}^{max}}$$

Note: This equation should be used so that R_{sh} is as close as possible to its maximum limit in order to take the greatest advantage of the V_o range.

Since the output voltage is eventually measured by the ADC1 channel 1, one has to consider the relation between the current resolution ΔI_M and the ADC1 resolution ΔV_o:

$$\Delta V_o = \frac{VAREF}{2^{10} - 1} < G\ R_{sh}\ {\Delta I_M}^{min}$$

Using the internal reference leads to $\Delta V_o \approx 4.5$ mV. From this condition, the **2nd design equation** derives:

$$R_{sh} > {R_{sh}}^{min} = \frac{\Delta V_o}{G\ {\Delta I_M}^{min}}$$

Note: This equation should be used so that R_{sh} is as far as possible to its minimum limit.

Another effect to consider is the power dissipation of the shunt resistor:

$$P_{D\,sh} = R_{sh}\ {I_{M\,RMS}}^2$$

In order to limit the power dissipation to a certain value P_{Dsh}^{max}, the **3rd design equation** should be applied:

$$R_{sh} < {R_{sh}}^{D} = \frac{{P_{D\,sh}}^{max}}{{I_{M\,RMS}}^2}$$

The following considerations are also relevant when selecting a shunt resistor:

1. The higher the gain, the lower the bandwidth, as seen in Figure 26
2. The values of commercial current sensing resistors are discrete and limited
3. More shunt resistors in parallel are possible to increase the total maximum power dissipation

Design example: Selecting a shunt resistor

- $I_M(t)$ is a square-wave current with:
  - $I_M^{max} = 10$ A
  - $I_M^{min} = 0$ A
  - Duty cycle = 80%
- VAREF = 5 V (internal)
- $\Delta I_M^{min} = 100$ mA
- $P_{Dsh}^{max} = 1$ W

To find the optimal shunt resistance, the best approach is to consider the three design equations for each gain setting G = {10, 20, 40, 60}:

1. From the 1st design equation:
$$R_{sh} < {R_{sh}}^{max} = \frac{1.5\ V}{G\ 10\ A} = \{15\ ;\ 7.5\ ;\ 3.75\ ;\ 2.5\}\ m\Omega$$
2. From the 2nd design equation:
$$R_{sh} > {R_{sh}}^{min} = \frac{4.5\ mV}{G\ 100\ mA} = \{4.5\ ;\ 2.25\ ;\ 1.225\ ;\ 0.75\}\ m\Omega$$
3. From the 3rd design equation:
$$R_{sh} < {R_{sh}}^{D} = \frac{1\ W}{80\ A^2} = 12.5\ m\Omega$$

Figure 28 shows a graphical representation of the design equations above. It shows that any gain setting can fit the case, given that R_{sh} falls in the selection area.

On the base of this analysis and consideration 1. and 2., a suboptimal choice for this use case would be a 7 mΩ resistor with a gain setting G = 20. This will lead to the following actual values:

$$V_o{}^{max} = 2 + 20 \times 7\ m\Omega \times 10A = 3.4\ V$$

$$\Delta I_M = \frac{4.5\ mV}{20 \times 7\ m\Omega} \approx 32.2\ mA$$

$$P_{D_{sh}} = 7\ m\Omega \times 80\ A^2 = 560\ mW$$

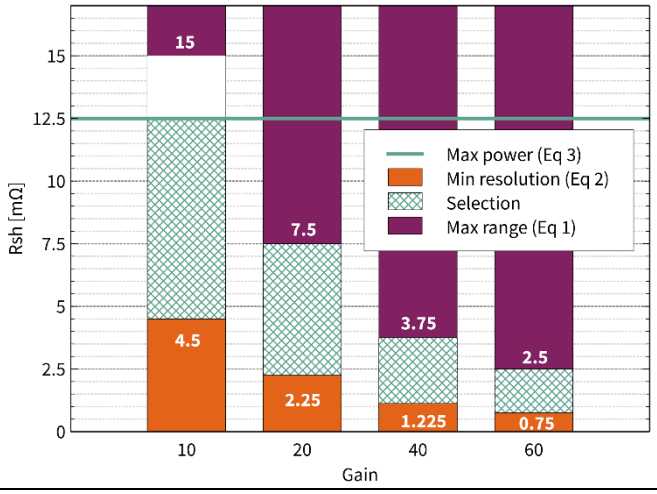


Figure 28 Graphical representation of the design example values

11.4.2 Filter network selection

The goal of the filter network design is to shape the dynamics of the CSA input voltage so that it is the best representation of the measured current. In practice, the design goal is to choose the values of the low-pass filter components R_{LP} and C_{LP} that damp the ringings caused by the parasitic inductance L_{sh}.

V_o as function of I_M needs to be expressed. This could be done in the time domain, but the AC analysis in the frequency domain can simplify the design procedure. The total CSA gain transfer function can be defined as:

$$H(s) = \frac{v_o(s)}{i_M(s)}$$

Further H(s) can be broken down as a function of the CSA differential and common mode gains from the input pins OP2 and OP1 to the input of the ADC1:

$$H(s) = \frac{v_o(s)}{i_M(s)} = \frac{A_d(s)\ v_{id}(s) + A_{cm}(s)\ v_{icm}(s)}{i_M(s)} \approx \frac{v_{id}(s)}{i_M(s)} A_d(s)$$

Note: The above simplification is possible because both common mode input signal and gain are negligible compared to the differential ones.

In the frequency domain, the goal mentioned above translates into obtaining a response as flat as possible, ideally a constant response across the whole frequency spectrum. As known, $A_d(s)$ has a flat gain, but within limited bandwidth (see Figure 26 and Table 16), so the effect of the shunt and filter network has to preserve this level of fidelity.

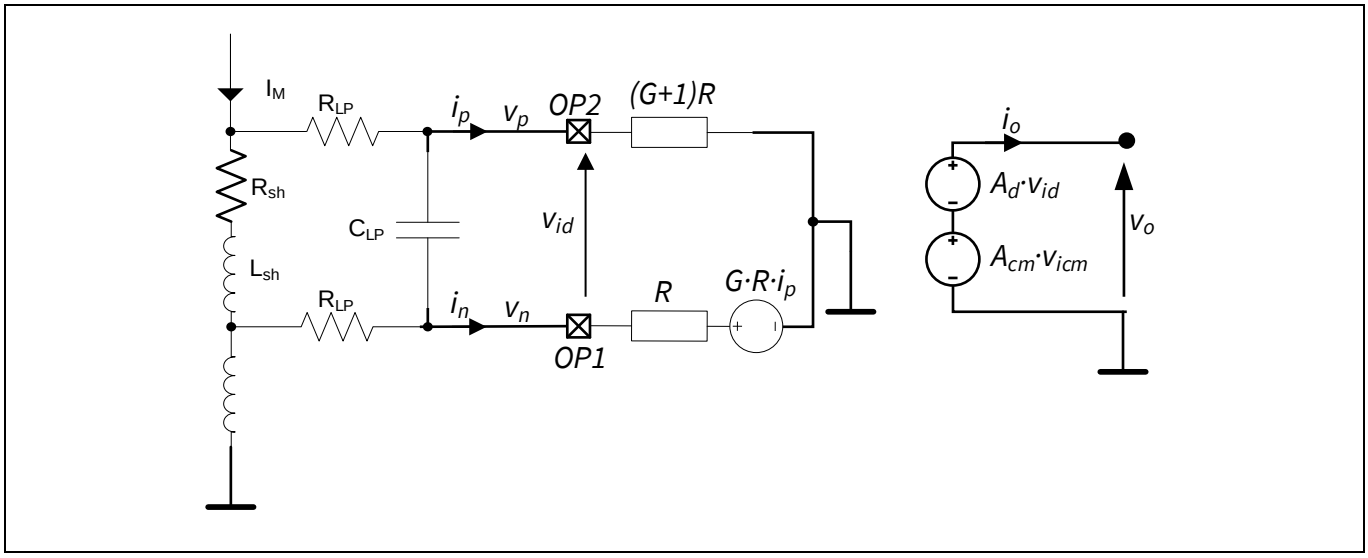


Figure 29 CSA input filter and graphical representation of the CSA impedances

In conclusion, the best dynamic performances obtainable (without introducing any additional reactive device) is the one of the CSA. This requires:

$$Z_T(s) = \frac{v_{id}(s)}{i_M(s)} = R_{sh}$$

This will be eventually the condition for calculating one of the design equations.

The analytical calculation of $Z_T(s)$ from the schematic in Figure 29 leads to:

$$Z_T(s) = \frac{v_{id}(s)}{i_M(s)} = R_{sh} \frac{F\left(1 + \frac{s\,L_{sh}}{R_{sh}}\right)}{s^2\,C_{LP}\,L_{sh}\,F + s\left(\frac{L_{sh}}{2\,R} + C_{LP}(R_{sh} + 2\,R_{LP})\right)F + 1}$$

$$F = \frac{2\,R}{2\,R + R_{sh} + 2\,R_{LP}}$$

For s = 0, which means in DC regime, the transimpedance can be expressed as:

$$Z_T(s)|_{s=0} = R_{sh}\,F$$

This means that the factor F introduces a DC error. This factor indeed represents the portion of the DC current I_M that flows through the low pass filter resistors R_{LP} and the input stage of the CSA (because of its non-infinite input resistance R).

This error can be minimized by considering that R_{sh} << R and by imposing the **1st design equation**:

$$R_{LP} < \frac{R}{p}$$

This condition leads to a DC gain error of:

$$ErrZ_T\% = \frac{R_{sh} - R_{sh}\,F}{R_{sh}}\% < \frac{1}{1+p}\%$$

For example, for p = 100 the error would be less than 1%. It is therefore good practice to choose a value of R_{LP} between 1 Ω and 15 Ω.

The following considerations can then be applied:

- If p = 100 then F ≈ 1
- $R_{sh} << R_{LP}$
- $L_{sh} / 2R \approx 0$

These assumptions will lead to a final simplified transfer function:

$$Z_T(s) = \frac{v_{id}(s)}{i_M(s)} \approx R_{sh} \frac{1 + \frac{s\,L_{sh}}{R_{sh}}}{s^2\,C_{LP}\,L_{sh} + s\,C_{LP}\,2\,R_{LP} + 1} = R_{sh} \frac{1 + \frac{s}{\omega_z}}{\frac{s^2}{{\omega_0}^2} + \frac{s}{Q\omega_0} + 1}$$

The parasitic inductance introduces a 2nd-order dynamics and a zero in the filter transfer function. The zero will boost the transfer function, increasing the high frequency content of the step response. The poles instead, depending on the filter values, could:

- Introduce a resonance ($Q > 1/\sqrt{2}$), which will result in a fast, but overshooting step response
- Split, one in low frequency and one at high frequency ($Q < 1/\sqrt{2}$) obtaining a slow, but smooth step response.

None of these effects is desirable because the goal is to obtain a flat response (at least within the bandwidth of the CSA). A third option would be to try to cancel the dynamic of the zero with one of the poles. Partial cancelation of the zero is indeed possible when:

$$C_{LP} = \frac{L_{sh}}{2\,R_{LP}\,R_{sh}}$$

This is the **2nd design equation**. The pole/zero cancellation is never perfect in practice, because of the uncertainty and variation of the passives values. So, this method gives the suboptimal value of C_{LP} that maximizes the bandwidth of the filter.

This design equation has to be considered as a starting point recommendation for the customer's design. The designer shall make use of the analytical tools shown in this chapter to choose the C_{LP} value considering the design's specifications.

In Figure 30 the effect of four different C_{LP} values on the normalized transfer functions and step responses can be observed:

$$\frac{H(s)}{G\,R_{sh}} \quad ; \quad \frac{Z_T(s)}{R_{sh}}$$

11.4.3 Conclusions

When all the design equations are used to select the current sensing and filter network, the transfer function from measured current to output of the CSA can be simplified as:

$$H^{opt}(s) = \frac{v_o(s)}{i_M(s)} = {Z_T}^{opt}(s)A_d(s) \approx \frac{R_{sh}}{1 + s\ C_{LP}\ 2\ R_{LP}} \ \frac{G}{\left(\frac{s}{\omega_p} + 1\right)^4}$$

This means that:

- The DC error introduced by the finite CSA input impedance R is minimized
- The 2nd-second order dynamics introduced by the sensing resistor parasitic inductance L_{sh} is tamed

The speed of the signal is mainly affected by the CSA bandwidth. As shown in Table 16, the typical settling time depends on the gain setting G. Figure 30 shows that the CSA bandwidth is capable to settle within 800 ns typically for the highest gain (lowest bandwidth) setup. In a motor control with 20 kHz PWM, 800 ns represents a duty cycle of 1.6%. So for applications where very high precision and fast response is needed by the current sensing, it is suggested to setup the CSA (and design the passives) for the lowest gain possible.

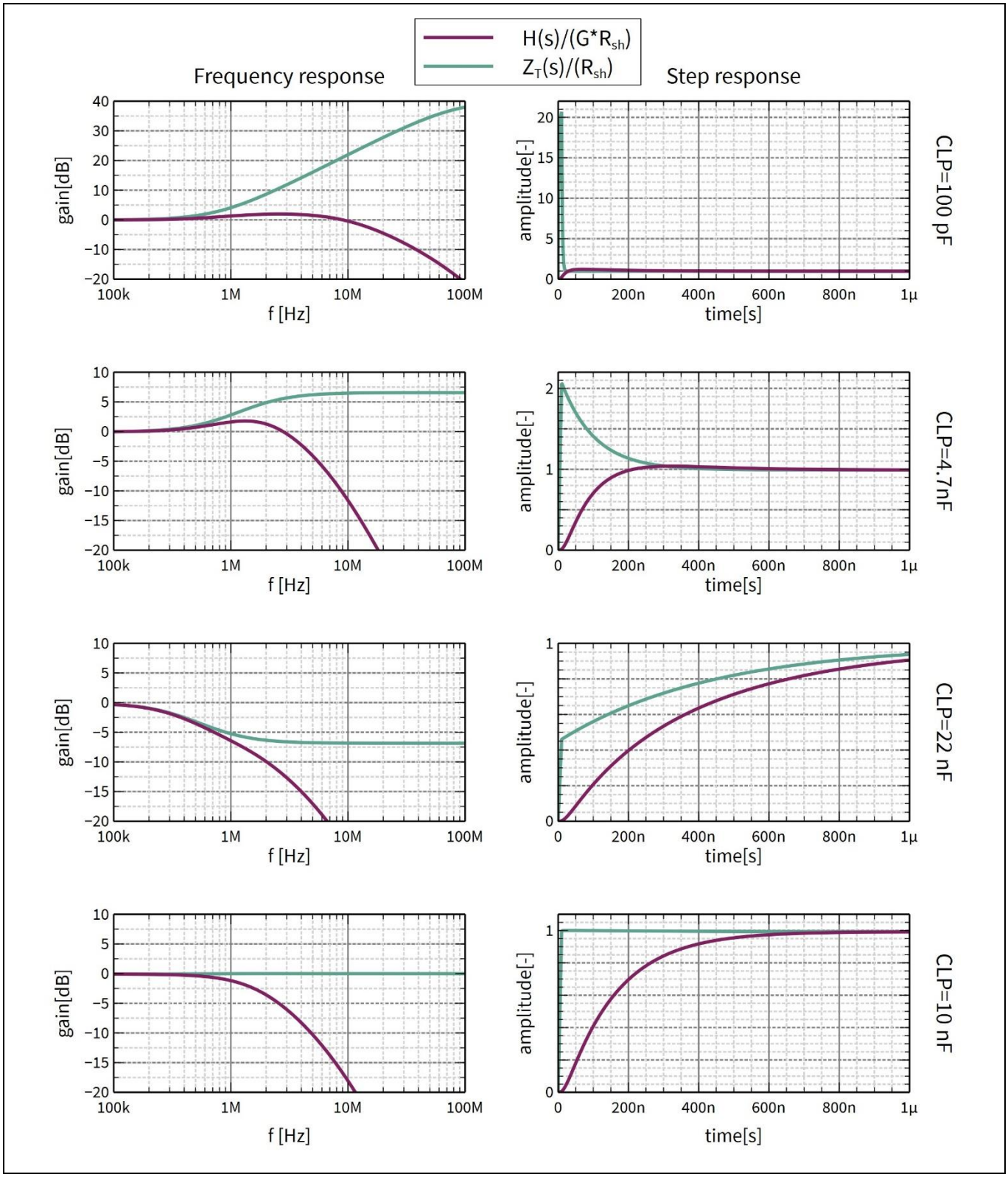


Figure 30 **Frequency and step response of the transfer functions $Z_T(s)$ and H(s) with different values of C_{LP} and the following values: L_{sh}=1 nH, R_{sh}=5 mΩ, R_{LP}=10 Ω, G = 60. The last value, 10 nF, is the suboptimal value that satisfies the 2nd design equation**

12 Sensor interfaces

The TLE987x/6x family offers the option to interface different sensors and communication interfaces to the device. Depending on the application requirements, one or more of these interfaces can be used by configuring the corresponding functionality in the relevant device registers. This chapter presents some example interfaces with relevant pins of the chip which can be used for these interfaces.

12.1 Implementing different interface connections to TLE987x/6x

Using different ports and their alternate select functions, multiple interfaces can be implemented including TMR sensor (TLE987x-2QX only), Hall sensor, SPI, and UART. Figure 31 and Figure 32 each show two possible configurations depending on the application requirement. External components which might be needed for some of the interfaces have not been included, as they depend on the sensors which are used. In case some interface is not needed, the relevant ports can be used as per application requirement.

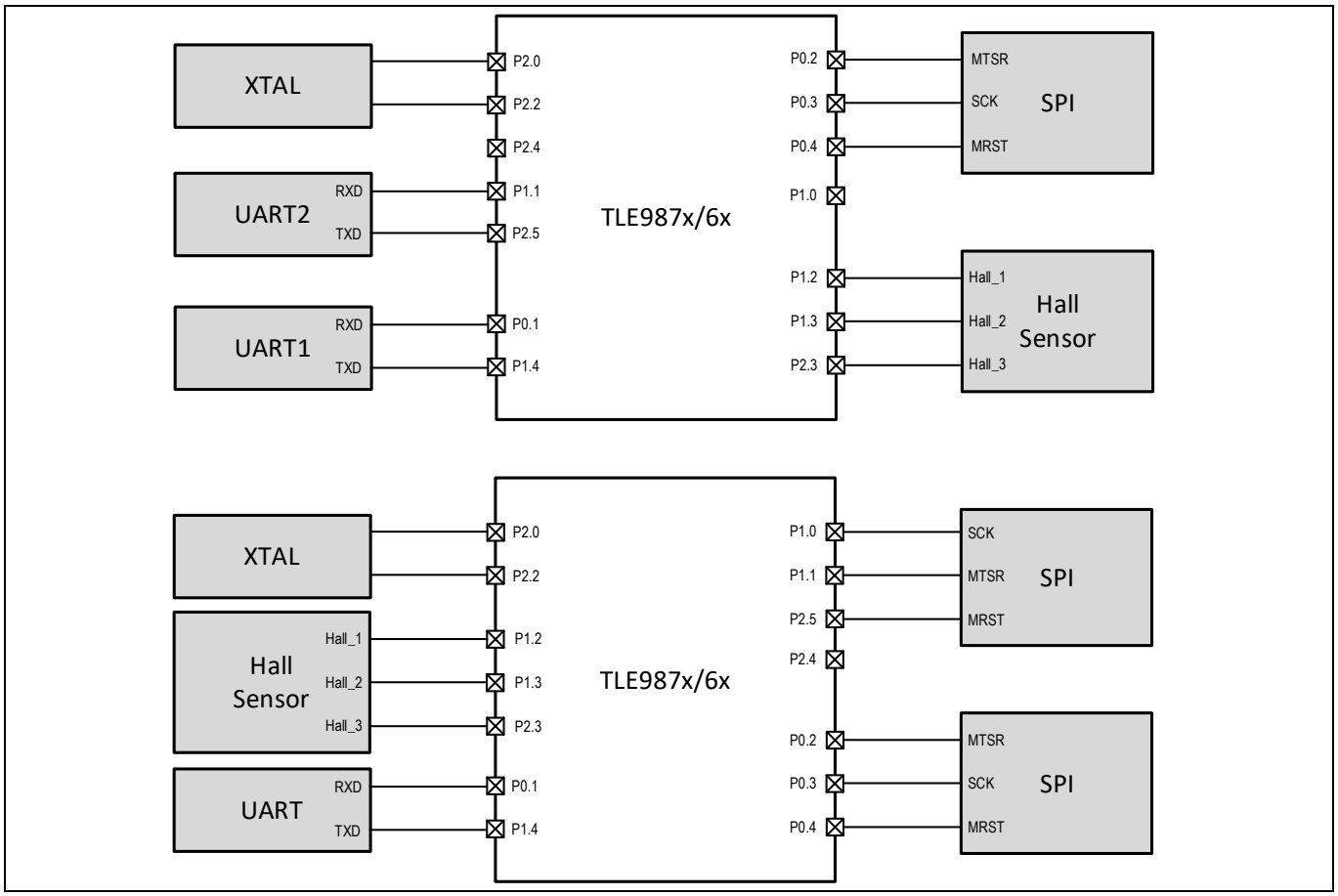


Figure 31 Example interfaces for TLE987x/6x

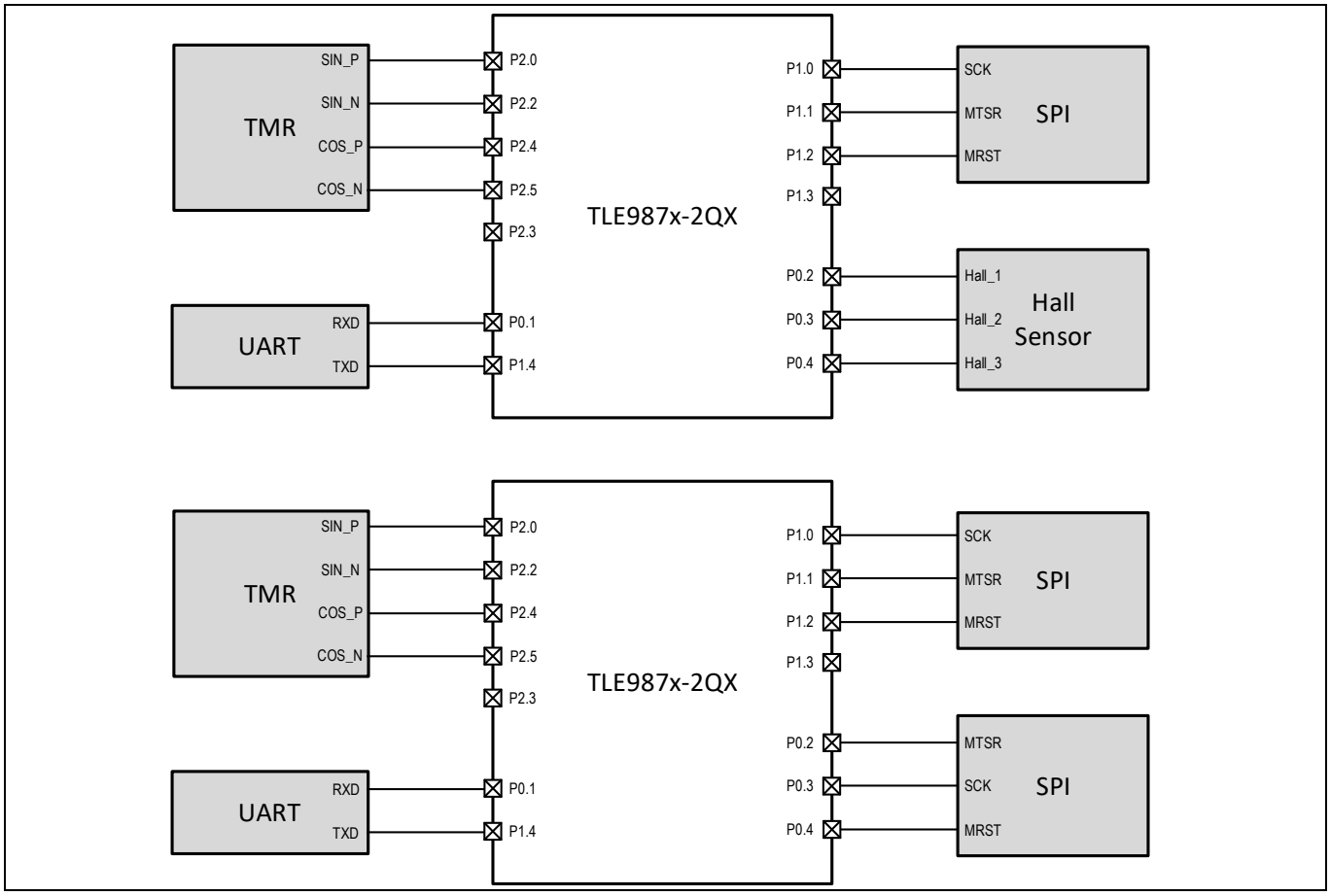


Figure 32 Example interfaces for TLE987x-2QX

13 SWD (serial wire debug) interface circuitry

The serial wire debug interface (SWD) is used to download code to the MOTIX™ MCU or to debug the chip. This chapter explains how to implement the circuitry around the chip to achieve a successful SWD connection.

13.1 Description of the SWD interface

The SWD interface provides a debug port for severely pin-limited packages, and as such may be used for small package microcontrollers but also complex ASICs where limiting the pin count is critical and can be a critical factor for the device cost.

As SWD interface, the TLE987x/6x uses the pins TMS (data) and P0.0 (clock). In the evaluation boards, the signals are routed through a 5×2 pin header (SWD connector). The following implementation explains the connection between embedded power IC and SWD interface.

13.2 Implementing an SWD interface connection to TLE987x/6x

The SWD interface can be directly connected to chips of the TLE987x/6x family. Figure 33 shows the interconnections between the device and SWD connector.

External pull-up or pull-down resistors are not needed because internal pull-down resistors are present.

The GND for the SWD connector is the digital GND of the TLE987x/6x (pin 19).

A ceramic capacitor from the RESET pin to GND can be placed in order to improve immunity from transients. The recommended value of the capacitor is 1 nF. If this capacitor is used, a blanking time of 31 µs in the reset blind time register (CNF_RST_TFB) has to be configured.

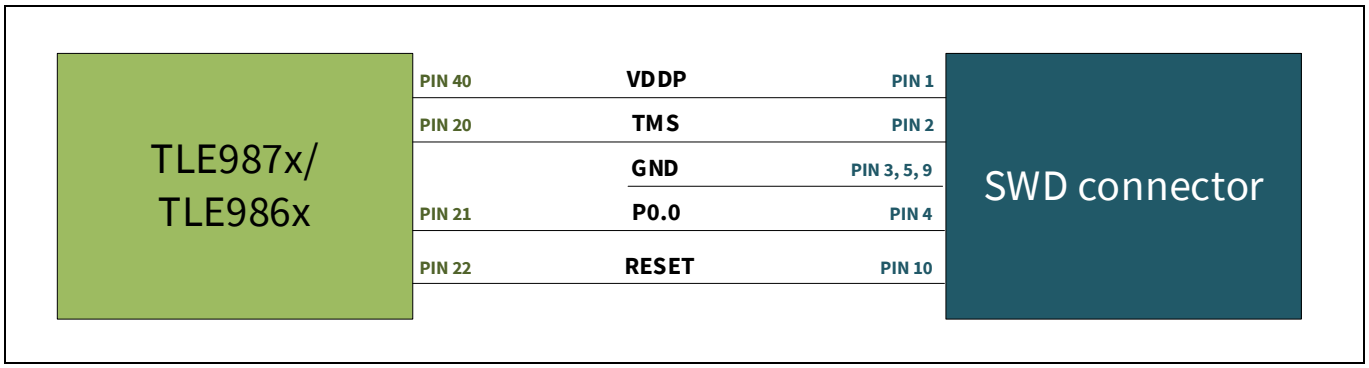


Figure 33 SWD connection to the TLE987x/6x device

On the SWD interface of the TLE9879 EvalKit and TLE9869 EvalKit, pin 9 is used to deactivate the onboard debugging circuit. In a typical implementation, this pin is used as GND. The pinout is shown in Figure 34.

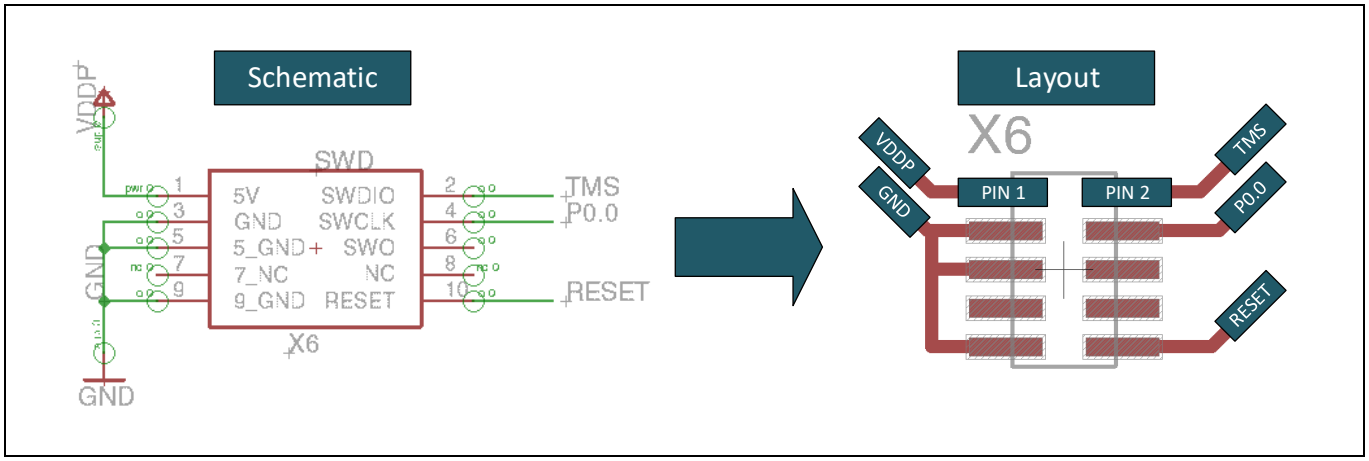


Figure 34 SWD interface implementation for an application

14 Unused pins

Table 17 shows the recommendations for the TLE987x/6x pins, in case they are not used in the application. The GND digital pins are pin 19 and pin 28, while the GND analog is pin 39.

Table 17 Connecting unused pins

Type	Pin number	Recommendation 1 (if unused)	Recommendation 2 (if unused)
CP1L, CP2H, CP2L, CP1H	1, 3, 4, 48	Open	–
VCP	2	Open	–
GH3, GH2, GH1, GL3, GL2, GL1	5, 7, 9, 11, 12, 13	Open	–
SH2, SH1, SL, SH3	6, 8, 10, 46	GND	–
MON	14	GND analog/digital	Open + configured internal PU/PD
GPIO	15, 16, 17, 18, 21, 23, 24, 25, 26, 27, 31, 32, 35	GND analog/digital	External PU/PD or Open + configured internal PU/PD
TMS	20	Open	–
RESET	22	Open	–
P2.0 / XTAL1	29	GND analog/digital	–
P2.2 / XTAL2	30	Open	–
VAREF	34	Open (VAREF disabled)	–
CSA	36, 37	Open (CSA disabled)	–
VDH	44	GND	–
VDDEXT	45	Open (VDDEXT disabled)	–
VSD	47	GND	Connect to VS for monitoring purpose
LIN	48	Open	–

15 Layout guidelines

In this chapter general recommendations are provided regarding PCB layout, as well as some specific hints for microcontrollers and MOSFET bridge drivers.

15.1 General PCB recommendations

Electromagnetic interference (EMI) is mainly radiated by the PCB and the connected cables. In fact, cables are very efficient antennas, especially for common-mode currents. Loops on the PCB are regarded as good emitting antennas. Loops inside an IC are considered to be small compared to the external loops on PCB and cabling. Therefore, EMI from the IC can be neglected in most cases. Below there are some considerations for an EMI-aware system/PCB design:

- Signal lines from outside need to be filtered
- Buffer capacitor for supply pins
- Decoupling ceramic capacitors ≤ 100 nF
- Filter and decoupling devices close to disturbance source
- Low-impedance ground plane
- Place filter and storage coils away from sensitive parts
- Pi-filter design with decoupled input/output side, by orthogonally placed components
- PCB format which allows short routing traces
- Multiple vias for filter capacitor GND connections
- GND plane close to component side
- Separate power from control signals
- Fast signals with short connection traces away from PCB border
- Shielding of critical lines by parallel GND lines

15.1.1 Placement of the connectors

Having connectors on both sides of the PCB might cause high emissions. A good PCB design should place all connectors on the same side.

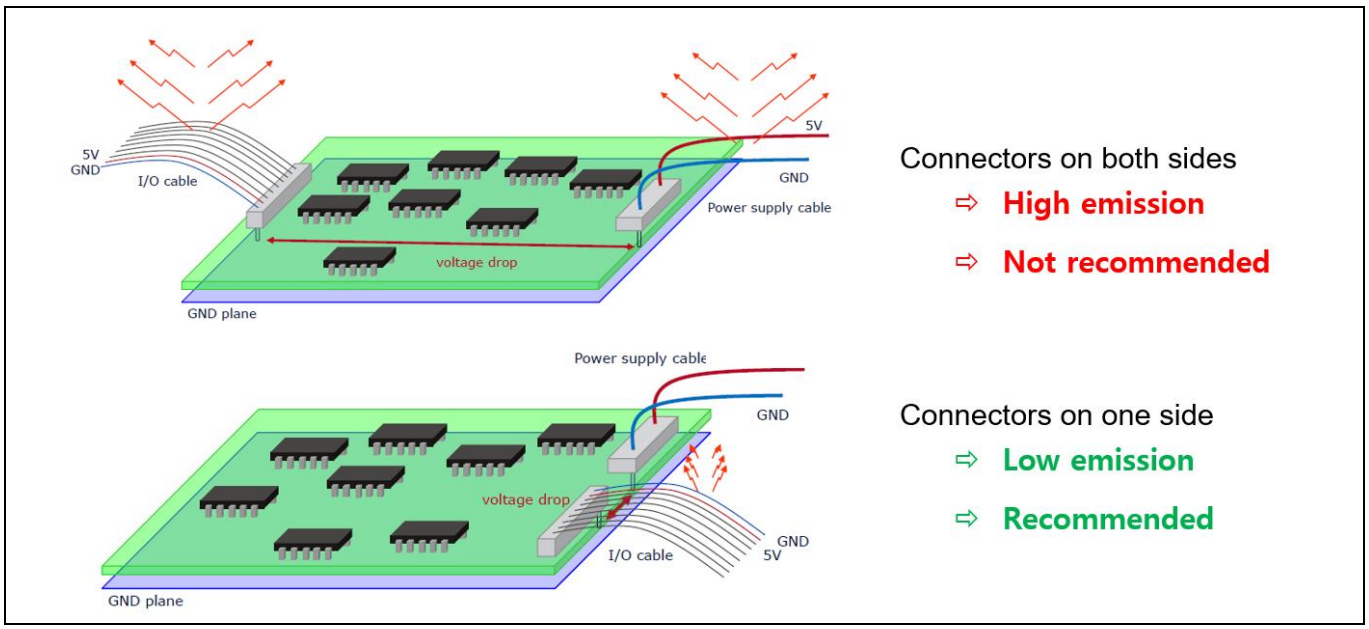


Figure 35 Placement of the connectors

15.1.2 Floor-planning the PCB

For the placement of components, the following rules should be considered:

- All components from one group should be located together (power, digital, analog, supply, and so on)
- Connectors should all be placed on the same side
- Susceptible parts should be placed away from noisy parts (power, digital, analog)
- Parts that generate noise should be close to a connector
- Route all traces to the components in each zone as if this zone had its own ground plane

For simplicity and clarity reasons, number the components in each zone in the same way (for example, analog = 100, digital = 200, power = 300, and so on).

15.1.3 Routing the power supply traces

Wiring loops on the PCB should be as small as possible.

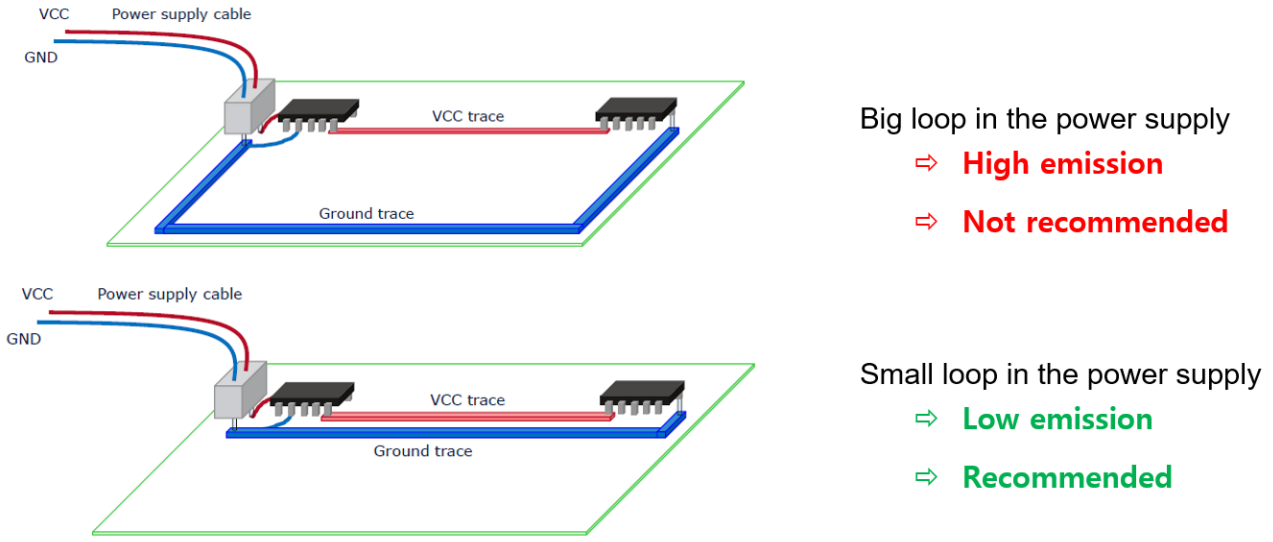
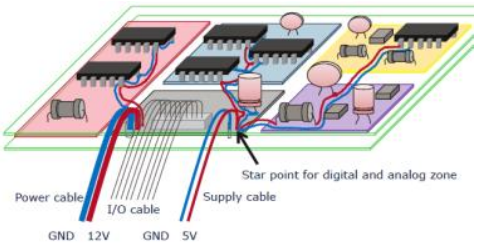
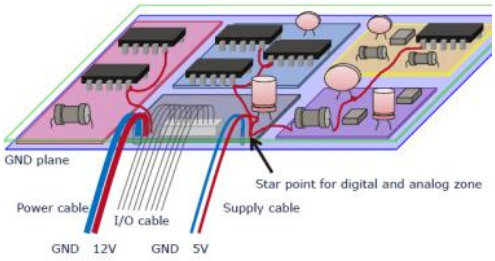
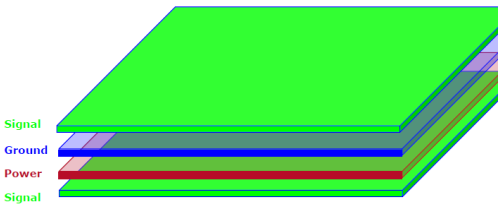
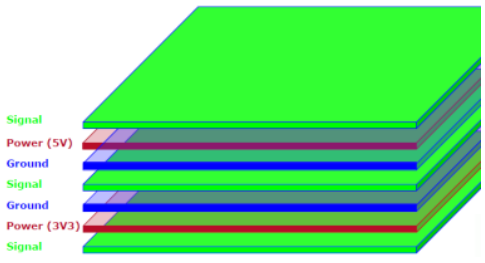


Figure 36 Routing the power supply traces

15.1.4 Number of PCB layers

Table 18 Rules for different PCB types

Two-layer PCB (no ground plane)		• Keep the loop areas that are formed by ground and power supply traces as small as possible • Route power supply traces always together (parallel, next to each other) starting from one central start point and spreading into each individual zone • Do not mix the supplies of different zones • Fill free areas with ground
Two-layer PCB (solid ground plane)		• Use a solid ground plane • Components of one zone should be supplied by only one supply from a central star point • Do not mix the supplies of different zones • Supply traces cannot have loops; use a tree structure instead
Multilayer configuration (4 layers)		• Keep ground and power supply layers next to each other. This provides a good decoupling capacitor for free • Avoid slots in ground and power supply planes (for example, by routing signal traces within these planes, vias in a row, through-hole connectors)
Multilayer configuration (> 4 layers)		• Route critical signals (for example, high-frequency signals, susceptible signals) in an inner signal layer that is embedded between two ground layers • Give each power supply domain (for example, 5 V, 3.3 V) a separate power and ground plane

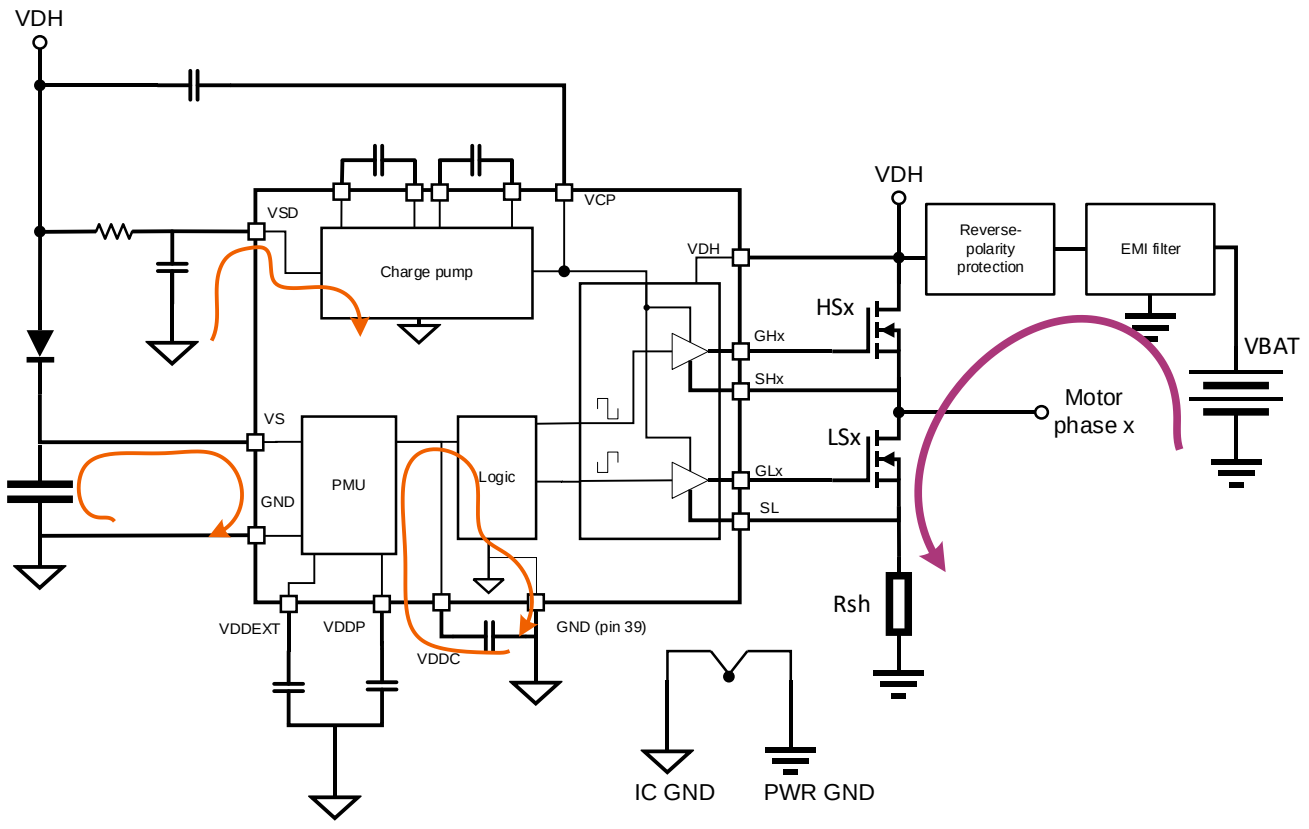
15.2 Specific PCB design rules for microcontroller with bridge drivers

Some general recommendations are:

- Separate the IC supply (VS and VSD) from VDH, that is, separate voltage sense line from power stage
- For minimal power dissipation, the recommended package for serial resistor at MON is SMD1206
- Placeholder for RC snubber circuit for all bridge MOSFETs should be considered for damping of circuit resonances during switching (if needed)
- For better filter performance and longer life, low-ESR electrolytic capacitors, rated for higher ripple current, should be used
- When a shunt resistor is used, the maximum acceptable capacitance between VDH and SL is 30 µF. Higher values would affect the current sensing too much
- The input capacitor, flying capacitors and tank capacitor should have short traces to reduce radiated emission and voltage drop across the trace inductances
- The DC-link capacitors should be placed close to the power stage in order to get stray inductance as low as possible

15.2.1 GND concept

Ground planes should be placed to separate the power MOSFETs' switching currents and the IC operating currents as much as possible. Figure 37 shows these currents and the symbols used for their return paths.



PWM switching currents in purple, IC supplies current in orange

Figure 37 GND concept and main current paths

This solution has two beneficial effects:

- The three main GND pins (19, 28, 39) are not influenced by the PWM currents. Voltage differences in the internal ground connections of the analog and digital circuitry in the IC will be limited
- High-frequency current interactions with the battery ground terminal will be limited

A practical example is shown in Figure 38. The connection between the PWR GND (mid-top) and IC GND (mid-bottom) planes consists of a slim trace and a via. This connection ensures the IC's current supply, while rejecting high-frequency currents that could loop from the IC to the battery. Consider these guidelines for the GND pin routing:

- Pin 39 should have the most solid connection to the IC GND plane. In the layout example this is accomplished by taking advantage of the exposed pad solid connection through multiple vias. When this is not feasible, connect the VDDC capacitor's GND pin to IC GND with as many vias as possible
- Pin 19 and 28 can have a weaker connection to IC GND

To minimize the stray inductance, the loop “input cap – bridge MOSFET – shunt resistor” should be as small as possible

A typical conducted EMI spectrum of an application that follows these rules is shown in Figure 39. This measurement has been performed on the layout example with the motor-running functions turned off to highlight the spectral contribution of the AC currents generated by the IC.

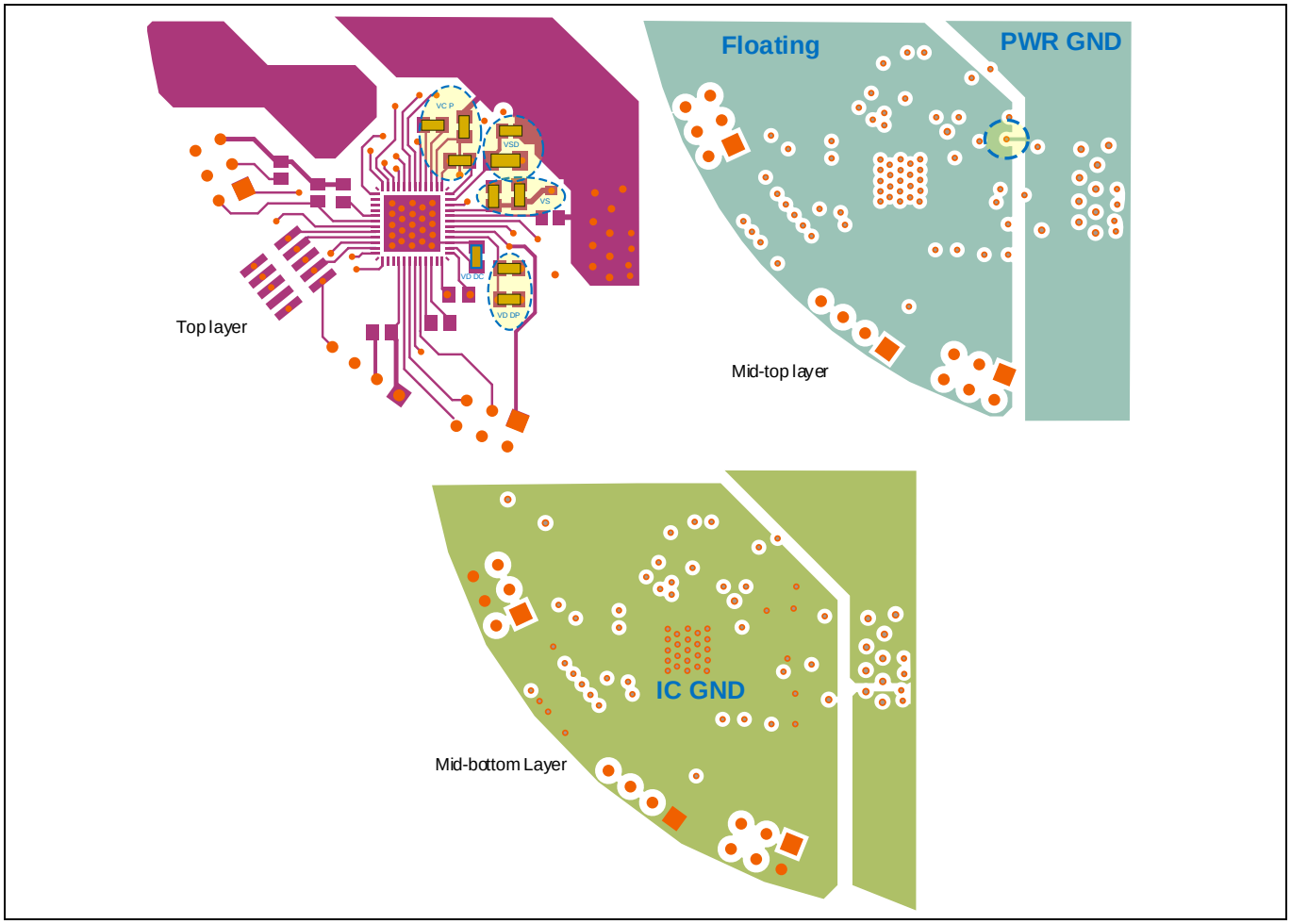


Figure 38 Example PCB layers

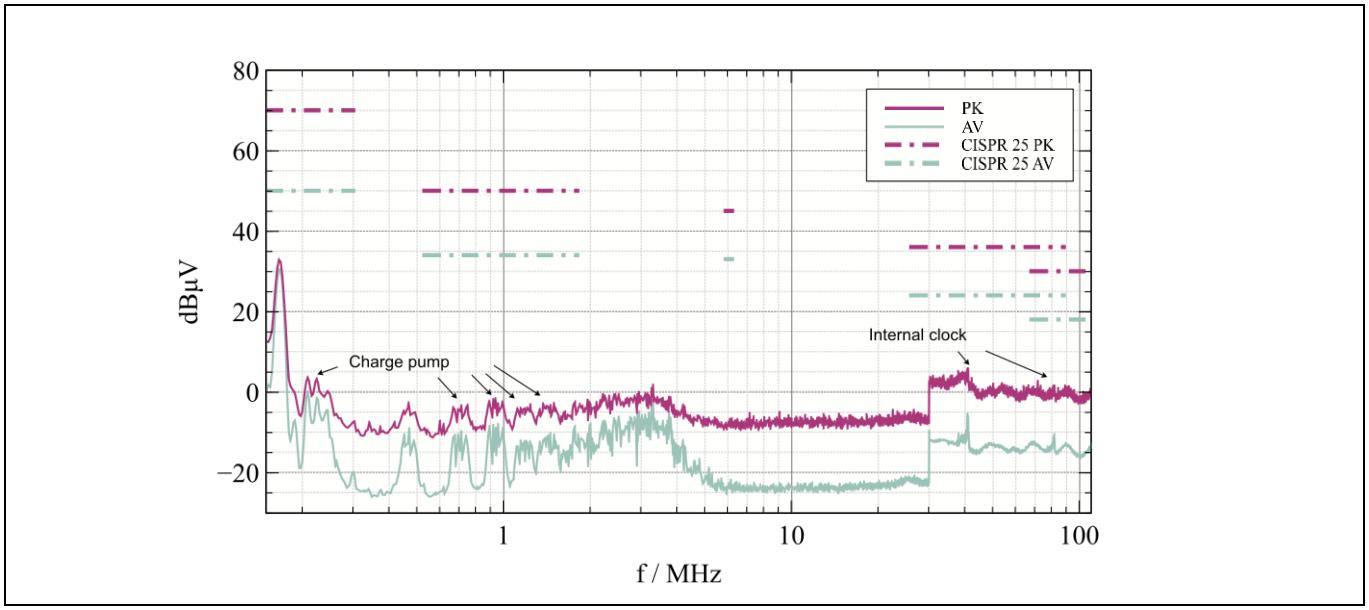


Figure 39 Conducted EMI measurement spectrum related to the layout example

15.2.2 Layout recommendation for 3-phase motor bridge

Figure 40 shows the commutation circuit of one bridge leg. This bridge leg can be a part of a 2-phase or 3-phase bridge.

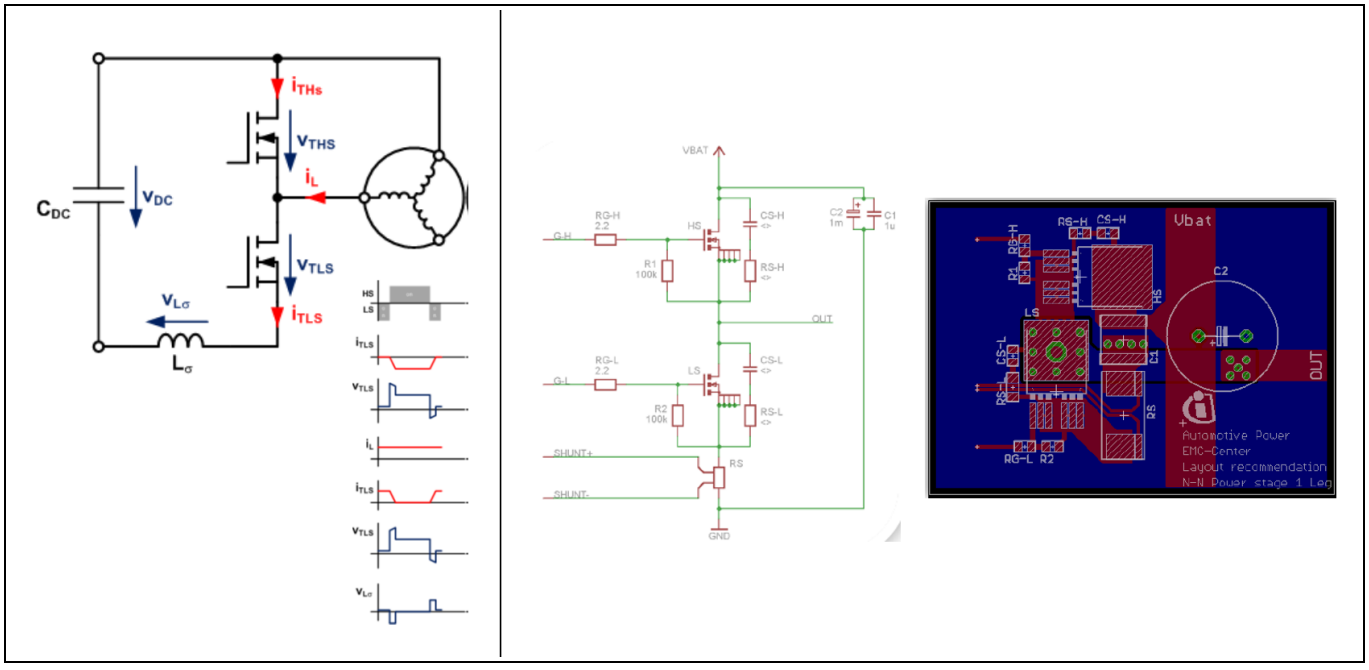


Figure 40 Layout – one bridge leg with two N-MOSFETs (as part of a 2-phase or 3-phase motor bridge)

During a transition from the low-side to the high-side, the current is commutating from LS switch to HS switch. The ideal commutation circuit is a loop consisting of CDC, THS and TLS. The inductive part of the real circuit is considered in the stray inductance L_σ. Overvoltages are induced over L_σ during the switching. These overvoltages are coupled directly to OUT and VS and will also cause radiated emission. The size of the commutation circuit has to be as small as possible.

Figure 40 shows an example for a low-impedance layout of one motor bridge leg.
The capacitors C2, CS-H and CS-L are placed as close as possible to the device pins.
Figure 41 shows a recommendation for the commutation circuit of a 3-phase motor bridge.

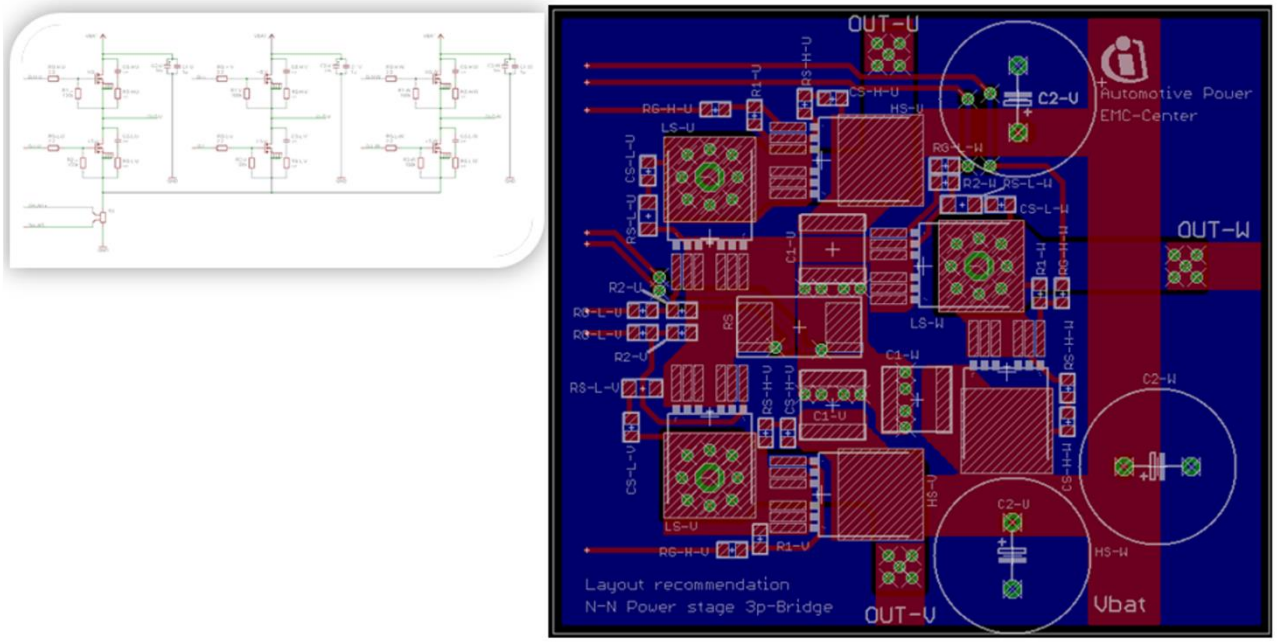


Figure 41 Layout recommendation – 3-phase motor bridge

15.2.3 Layout recommendation for a current sense shunt

The layout affects the current sensing of the shunt. A low-inductive shunt is no guarantee for a low-noise measurement signal. The quality of the signal depends on the layout with trace parasitics:

- Use a four-wire sense approach with symmetric sense lines
- Avoid inductive coupling into the sense wires
- Take care of capacitive currents on the leads in presence of high ΔV/Δt (common mode noise)

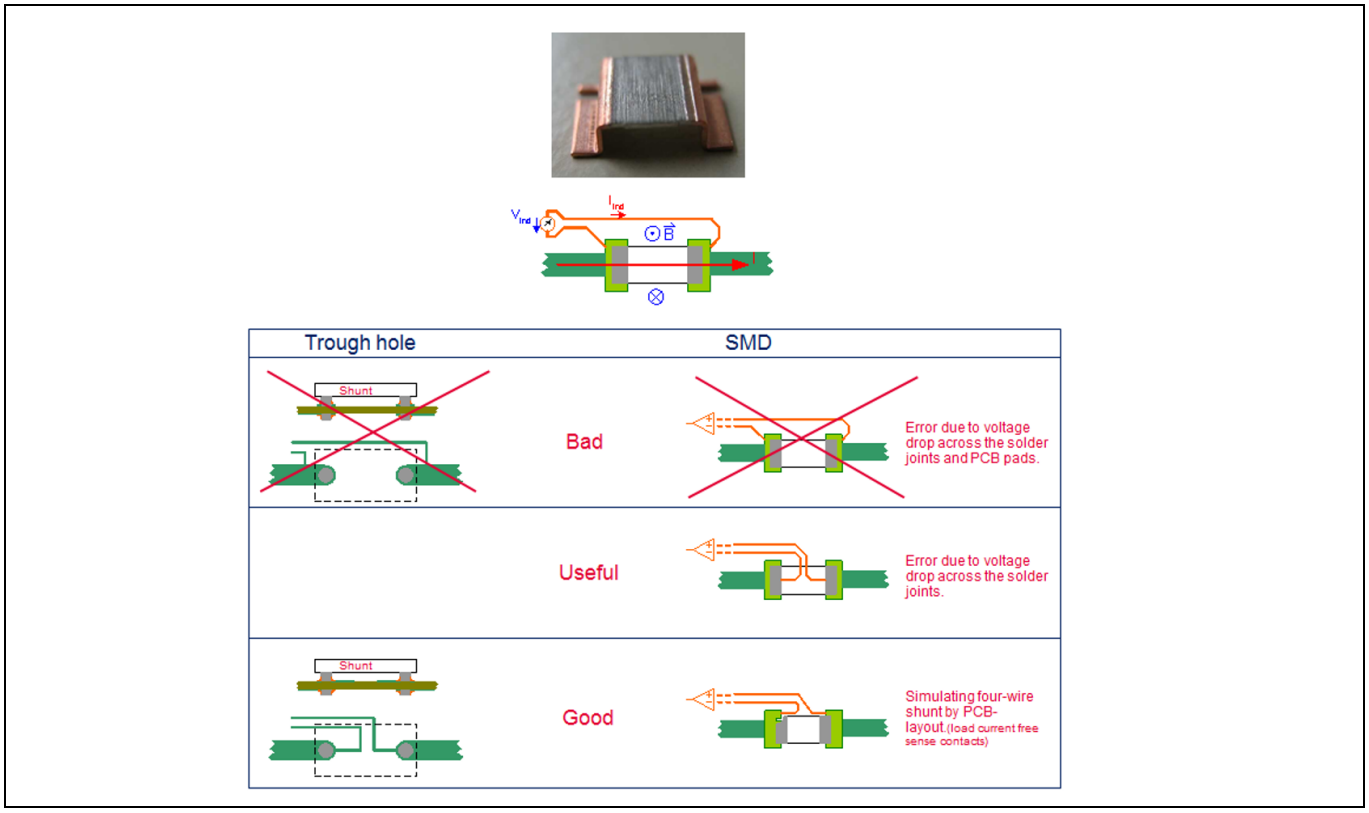


Figure 42 Layout recommendation – current sense shunt
No magnetic current sensing, pseudo-four-wire technique

Revision history

Document revision	Date	Description of changes
1.1	2022-04-01	General: • Renamed “Embedded Power IC” to “MOTIX™ MCU” • Added “type: X7R” to the component selections • Editorial changes
		Chapter “3 Clock generation unit (CGU)” • Added chapter “Ceramic resonator”
		Chapter “9 Bridge driver” • Added “Source resistor at the SHx pin” as an external component
		Chapter “10 Charge pump” • Updated “Charge pump application diagram” • Switched equations in chapter “Charge pump: how it works” • Changed voltage ripple time in chapter “Calculation example”
		Chapter 11 “Current sense amplifiers” • Changed L_{sh} = 1 µH to L_{sh} = 1 nH
		Chapter “14 Unused pins” • Updated table “Connection of unused pins”
		Chapter “15 Layout guidelines” • Renamed headings, moved chapter “Added considerations for an EMI-aware system/PBC design” • Removed chapter “Input filter”, figure “Ground concept and bypass capacitors, and chapter “Bypass capacitors”
		Added chapter “4 General purpose inputs outputs (GPIO)” Added chapter “7 Analog to digital converters (ADC1)” Added chapter “8 Sigma-delta analog digital converters (ADC3/4)” Added chapter “12 Sensor interfaces”
1.0	2020-10-30	Initial creation

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