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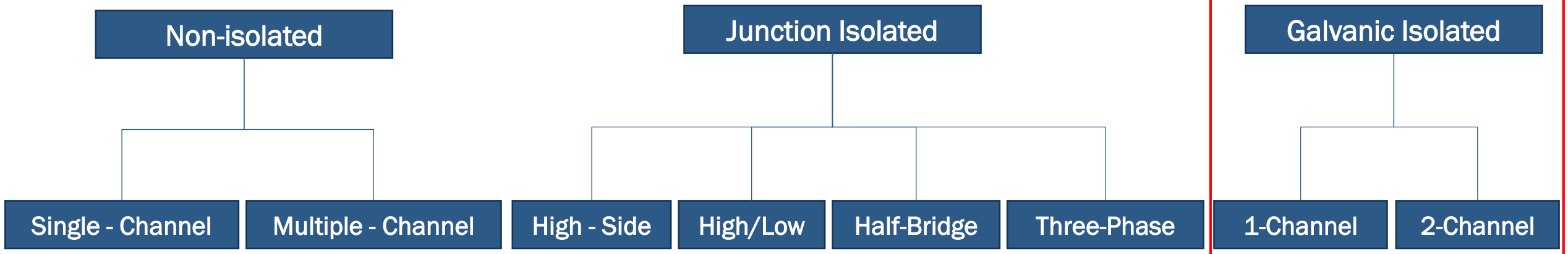
High Performance Isolated Drivers

PCS August - 2020

Public Information

Gate Driver Category Definition



Non-isolated		Junction Isolated				Galvanic Isolated	
• Single or multiple channel • Cheapest, simple solution for many applications where only a low-side driver is needed		• High Side, High/Low and Half Bridge • Floating HV well • From LV to 1200V breakdown voltage				• Normally needed in very high power/high voltage systems. • Three options: Optical, Inductive, Capacitive	
Applications							
• Automotive • Industrial Systems • Consumer Devices		• Appliances • Consumer Devices & Power Tools • Auxiliary Automotive & Motors Drives • Offline Power				• Automotive traction inverters • Industrial Drive • Server Rack Power • Solar and Energy Storage	
Products							
FAN3111 FAN3100 FAN3181 FAN312x	FAN321x FAN322x	FAN73611	FAN8811 FAN7392 NCP51530 NCP5183	FAN7382 FAN73833 FAN73912 NCP5106B	FAN7382 FAN73833 FAN73912 NCP5106B	NCP5115x NCP5175x	NCP5156x

Isolated Drivers Part Release Plan

OPN	Description	Package	AEC	Datasheet	Sample Date	RTM	Collaterals (AN/DB)
NCP51561BxDW	2-Ch Isolated Driver MOS (4/8A)	SOIC-16WB	No	Now	Now	Q4-2020	Now
NCP51561DxDW	2-Ch Isolated Driver SIC (4/8A)	SOIC-16WB	No	Now	Now	Q4-2020	Now
NCP51560BxDW	2-Ch Isolated Driver MOS (2/4A)	SOIC-16WB	No	Now	On Demand	TBC	Q3 2020
NCP51563BxDW	2-Ch Iso Driver MOS High Creepage (4/8A)	SOIC-14WB	No	Prelim July-2020	Q4-2020	Q1-2021	October 2020
NCV51561BxDW	NCP51561 MOS for Automotive	SOIC-16WB	Yes	Prelim July-2020	Q3 2020	Q1-2021	October 2020
NCV51561CxDW	NCP51561 SIC for Automotive	SOIC-16WB	Yes	Prelim July-2020	Q3 2020	Q1-2021	October 2020
NCP51566BxDW	High Perf 2-Ch Isolated Driver MOS (4/8A)	SOIC-16WB	No	Prelim July-2020	Q1-2021	Q2-2021	Q1-2021
NCP51567CxDW	High Perf 2-Ch Isolated Driver SIC (4/8A)	SOIC-14WB	No	Prelim Aug-2020	Q1-2021	Q2-2021	Q1-2021
NCP51752xDW	1-Ch Iso SiC Driver with int. Neg CP	SOIC-14WB	No	Now	Q2-2021	Q4-2021	Q1-2021
NCV51752xDW	NCP51752 for Automotive	SOIC-14WB	Yes	Prelim July-2020	Q2-2021	Q1-2022	Q1 2021
NCP51157xDW	High Perf 1-Ch Isolated Driver MOS (4/8 A)	SOIC-8WB	No	Prelim Aug -2020	Q1-2021	Q2-2021	Q1 2021
NCV51157xDW	High Perf 1-Ch Isolated Driver MOS (4/8 A)	SOIC-8WB	Yes	Prelim Aug-2020	Q2-2021	Q3-2021	Q2 2021
NCP51152xD	High Perf 1-Ch Isolated Driver MOS (4/8 A)	SOIC-8	No	Prelim Aug -2020	Q2-2021	Q3-2021	Q1 2021
NCV51152xD	High Perf 1-Ch Isolated Driver MOS (4/8 A)	SOIC-8	Yes	Prelim Aug-2020	Q2-2021	Q3-2021	Q2 2021
NCV51567CxDW	NCP51567 for Automotive	SOIC-14WB	Yes	Prelim Sept -2020	Q1-2021	Q3-2021	Q1 2021
NCP51755xDW	Full feature 1-Ch Iso SiC Driver (I2C/Neg CP/TS)	SOIC-20WB	No	Now	TBC	TBC	N/A
NCV51755xDW	NCP51755 for Automotive	SOIC-20WB	Yes	Prelim Sept-2020	TBC	TBC	N/A
NCV51568BxMN	High Perf 2-Ch Isolated Driver MOS (4/8A)	QFN16 5*5	No	Prelim Q4-2020	TBC	TBC	N/A

Public Information

Isolated Drivers Selection Guide

OPN	Features									Target Applications								
										Automotive				Industrial 4.0				
	No. of channels	Isolation	Primary use	Differential Input	Split output	DESAT w/ FLT	Miller Clamp	Neg Charge Pump	I2C	Traction	PTC	OBC	HV DC-DC	UPS	Solar	Motor Control	Telecom	Server
NCP51561BxDW	2	5 kV	MOS	✓											✓	✓		✓
NCP51561DxDW	2	5 kV	SiC	✓										✓		✓		
NCP51560BxDW	2	5 kV	MOS	✓												✓		✓
NCP51563BxDW	2	5 kV	MOS	✓										✓	✓	✓		
NCV51561BxDW	2	5 kV	MOS	✓								✓	✓					
NCV51561DxDW	2	5 kV	SiC	✓						✓	✓	✓	✓					
NCP/NCV51566BxDW	2	5 kV	MOS	✓								✓	✓		✓		✓	✓
NCP51567CxDW	2	5 kV	SiC	✓										✓	✓	✓		✓
NCP51752xDW	1	5 kV	SiC	✓	✓			✓						✓	✓	✓	✓	✓
NCV51752xDW	1	5 kV	SiC	✓	✓			✓		✓		✓	✓					
NCP51157xDW	1	5 kV	MOS	✓	Y/N									✓	✓	✓	✓	✓
NCV51157xDW	1	5 kV	MOS	✓	Y/N					✓	✓	✓						✓
NCP51152xD	1	3.7 kV	MOS	✓	Y/N									✓	✓	✓	✓	✓
NCV51152xD	1	3.7 kV	MOS	✓	Y/N					✓	✓	✓						✓
NCV51567CxDW	2	5 kV	SiC	✓	✓					✓	✓	✓	✓	✓	✓	✓		
NCP51755xDW	1	5 kV	SiC	✓	✓	✓	✓	✓	✓					✓	✓	✓		
NCV51755xDW	1	5 kV	SiC	✓	✓	✓	✓	✓	✓	✓		✓	✓					
NCV51568BMN	2	2 kV	MOS	✓													✓	✓

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NCP/NCV51561 – 5 kV Isolated High Speed Dual MOS/SiC Drivers

Value Proposition

The NCP5156x are isolated dual-channel gate driver with up to 4-A/8-A source and sink peak current. It is designed for fast switching to drive power MOSFETs power switches. The NCP5156x offers short and matched propagation delays. Internal functional isolation between the two secondary-side drivers allows a working voltage of up to ~1,200 VDC. The NCP5156x offers other important protection functions such as independent under-voltage lockout for each drivers and disable function.

Unique Features

- Input side isolated from output drivers by 5-kVRMS isolation barrier
- **40ns Prop Delay & 15ns Delay Match**
- **>= 150 V/ns dV/dt Immunity**
- Typical Source/Sink Current Capability
  - NCP51560 : 2-A/4-A
  - NCP51561 : 4-A/8-A

Benefits

- Give reliable operation and safety
- Efficient switching
- High Robustness
- Driver to accommodate diff MOS load

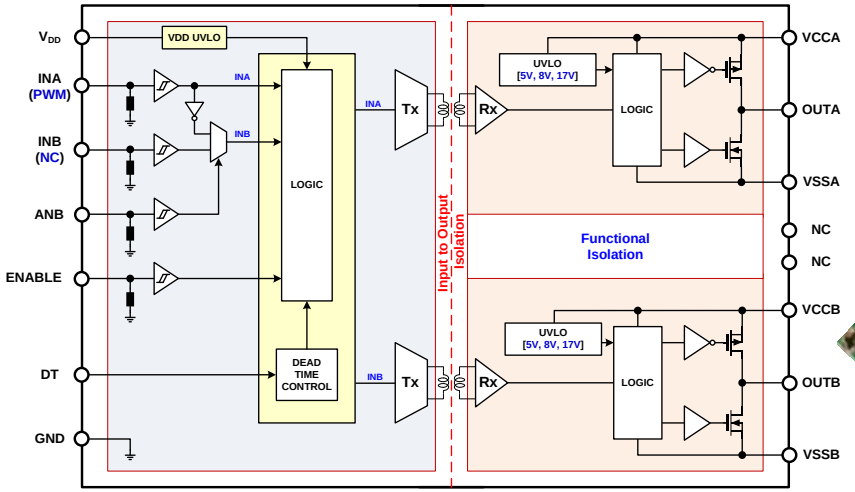
Other Features

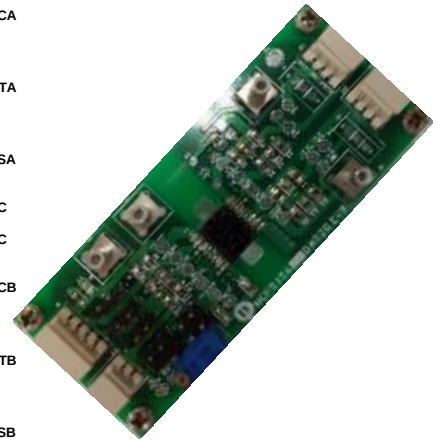
- Matched Propagation Delays : Max. 15 ns
- User Programmable Input Logic
  - Single or Dual-input modes via ANB
  - DISABLE or ENABLE mode
- User Programmable Dead-Time Control
- Different UVLO options: 5-V,8-V & 17-V

Market & Applications

- Isolated Converters in Offline AC-to-DC Power Supplies
- Motor Drive and DC-to-AC Solar Inverters
- HEV and EV On-Board chargers

Typical Application Schematic





Sampling now

Package Information

- SOIC-WB16
- OPN : NCV51561yzDWR2G
- y: UVLO level
- z: Enable/Disable

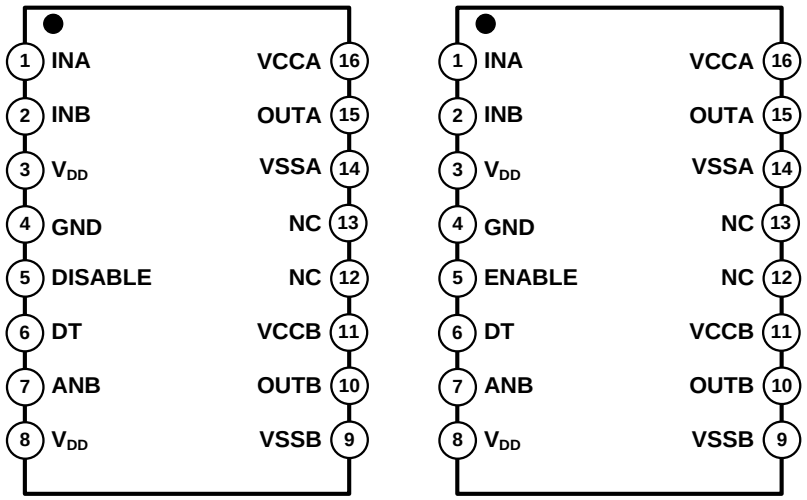
Public Information

NCP5156x – Product Family Information

OPN	Description	Package	Driving Current [A]		UVLO	ENABLE / DISABLE
			Source	Sink		
NCP51560AADWR2G	Low current dual isolated MOSFET driver	SOIC-16 WB	2	4	5 V	ENABLE
NCP51560ABDWR2G					5 V	DISABLE
NCP51560BADWR2G					8 V	ENABLE
NCP51560BBDWR2G					8 V	DISABLE
NCP51560CADWR2G					13 V	ENABLE
NCP51560CBDWR2G					13 V	DISABLE
NCP51560DADWR2G					17 V	ENABLE
NCP51560DBDWR2G					17 V	DISABLE
NCP51561AADWR2G	High current dual isolated MOSFET driver	SOIC-16 WB	4	8	5 V	ENABLE
NCP51561ABDWR2G					5 V	DISABLE
NCP51561BADWR2G					8 V	ENABLE
NCP51561BBDWR2G					8 V	DISABLE
NCP51561CADWR2G					13 V	ENABLE
NCP51561CBDWR2G					13 V	DISABLE
NCP51561DADWR2G					17 V	ENABLE
NCP51561DBDWR2G					17 V	DISABLE

OPN's	UVLO	EN/DIS	PACKAGE	SAMPLE
NCP51561AADWR2G	5 V	ENABLE	SOIC-16 WB	On demand
NCP51561BADWR2G	8 V	ENABLE	SOIC-16 WB	Now
NCP51561DADWR2G	17 V	ENABLE	SOIC-16 WB	Now
NCP51561ABDWR2G	5 V	DISABLE	SOIC-16 WB	On demand
NCP51561BBDWR2G	8 V	DISABLE	SOIC-16 WB	On demand
NCP51561DBDWR2G	17 V	DISABLE	SOIC-16 WB	On demand

NCP51561 – Pin Configuration



16 SOIC-WB

Pin No.	Pin Name	Description
1	INA	Logic Input for Channel A with internal pull-down resistor to GND
2	INB	Logic Input for Channel B with internal pull-down resistor to GND.
3, 8	V_{DD}	Input-side Supply Voltage. It is recommended to place a bypass capacitor from VDD to GND.
4	GND	Ground Input-side. (all signals on input-side are referenced to this pin)
5	DISABLE (ENABLE)	Logic Input High Disables Both Output Channels. Internal pull-down resistor (Option (ENABLE): Logic Input High Enables Both Output Channels. Internal pull-up resistor)
6	DT	Input for programmable Dead-Time It provides the operating three kind of mode according to the DT pin voltage as below. **Mode-A**: Cross-conduction both channel outputs is not allowed even though dead-time is less than maximum 20 ns when the DT pin is floating (Open). **Mode-B**: Dead-time is adjusting according to an external resistance (R_{DT}). t_{DT} (in ns) =10 ×R_{DT} (in kΩ) Recommended dead-time resistor (R_{DT}) values are between 1 kW and 500 kW. **MODE-C**: Cross-conduction both channel outputs is allowed when the DT pin pulled to VDD.
7	ANB	Logic Input for changing the input signal configuration with internal pull-down resistor to GND. The OUTA and OUTB as complementary outputs from one PWM input signal on the INA pin regardless the INB signal when the ANB pin is high. The INB pin should be pulled down to GND (recommended) or floating (not recommended) when the ANB pin is high. The ANB pin should be kept low when the OUTA and OUTB are controlled individually by INA and INB pins. (along with DISABLE and DT pins).
9	VSSB	Ground for Channel B
10	OUTB	Output for Channel B
11	VCCB	Supply Voltage for Output Channel B. It is recommended to place a bypass capacitor from VCCB to VSSB.
12, 13	NC	No Connection; Keep pin floating
14	VSSA	Ground for Channel A
15	OUTA	Output of Channel A
16	VCCA	Supply Voltage for Output Channel A. It is recommended to place a bypass capacitor from VCCA to VSSA.

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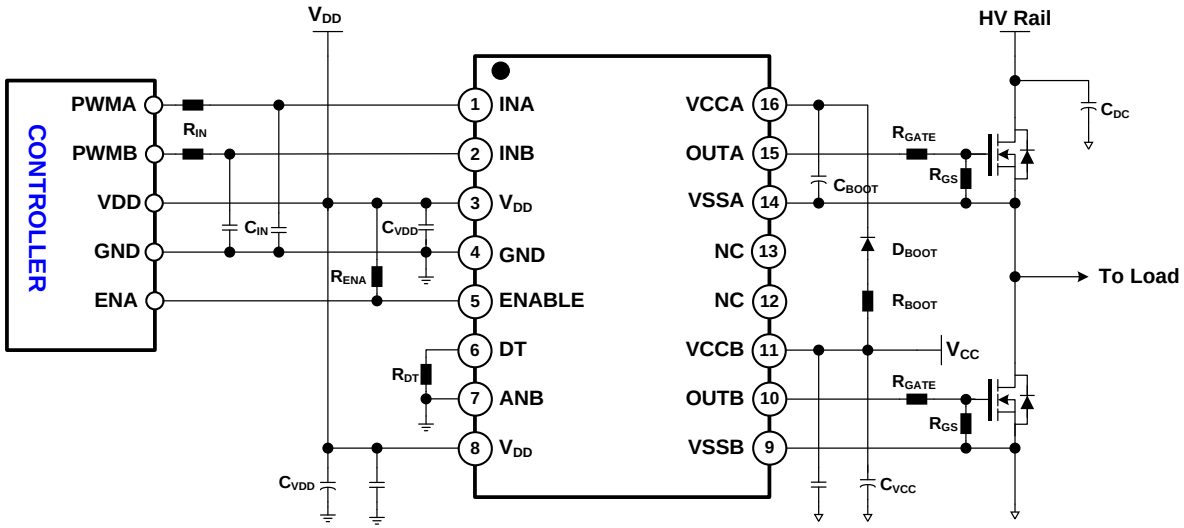
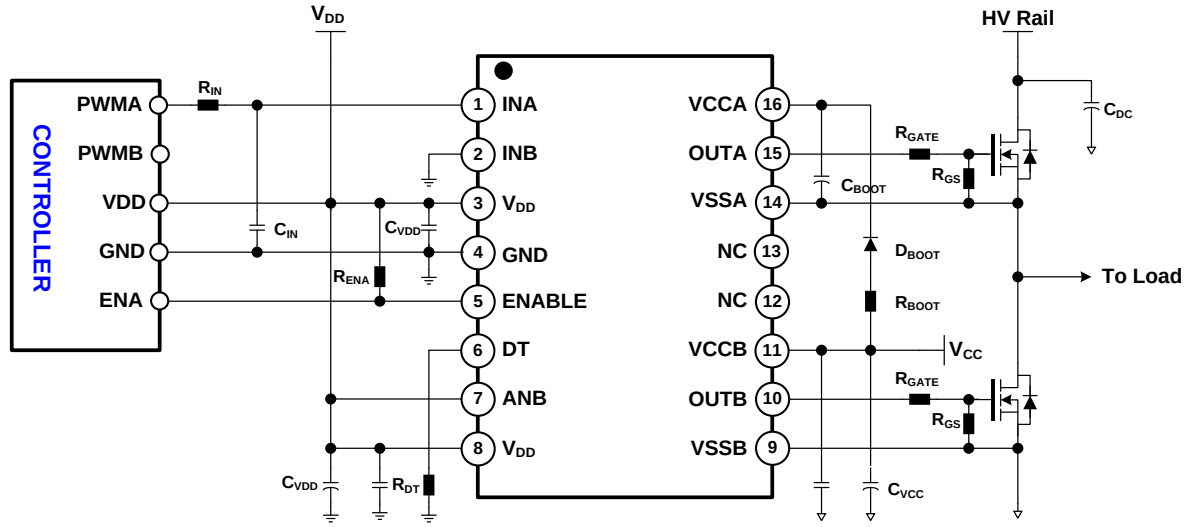
NCP51561 – Typical Application Schematic

- **Case A : Dual Input Mode (ANB=GND)**



(A) High and Low Side MOSFET Gate Drive

- **Case B : Single Input Mode (ANB=VDD)**



(B) High and Low Side MOSFET Gate Drive with PWM Controller

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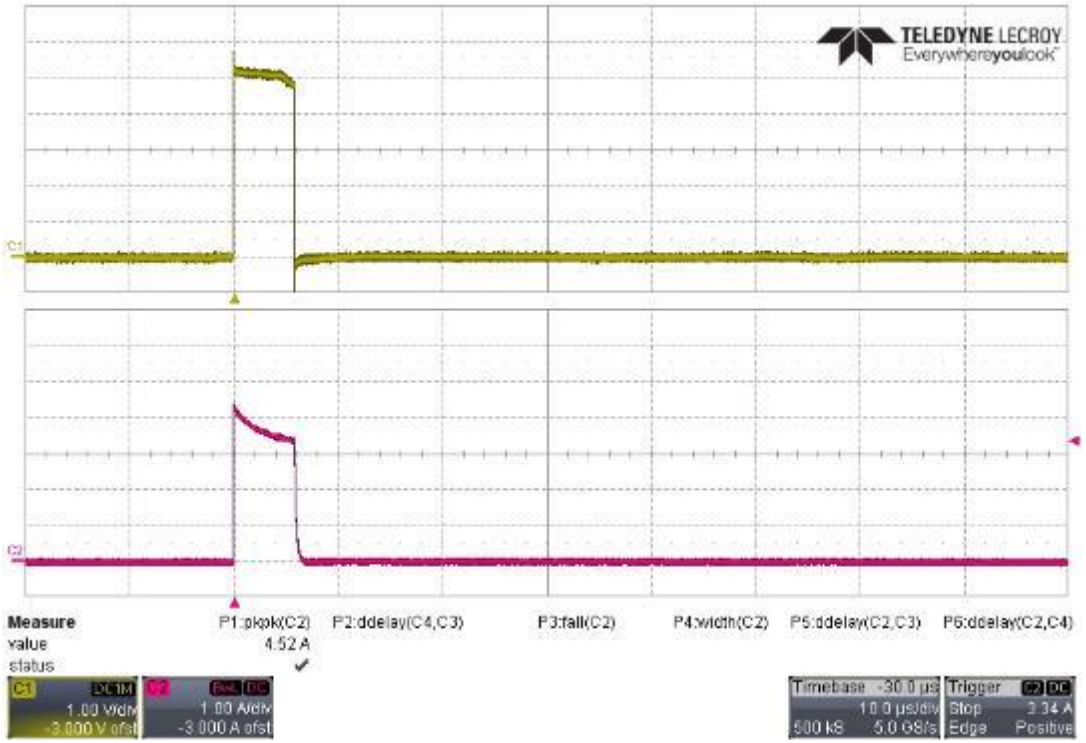
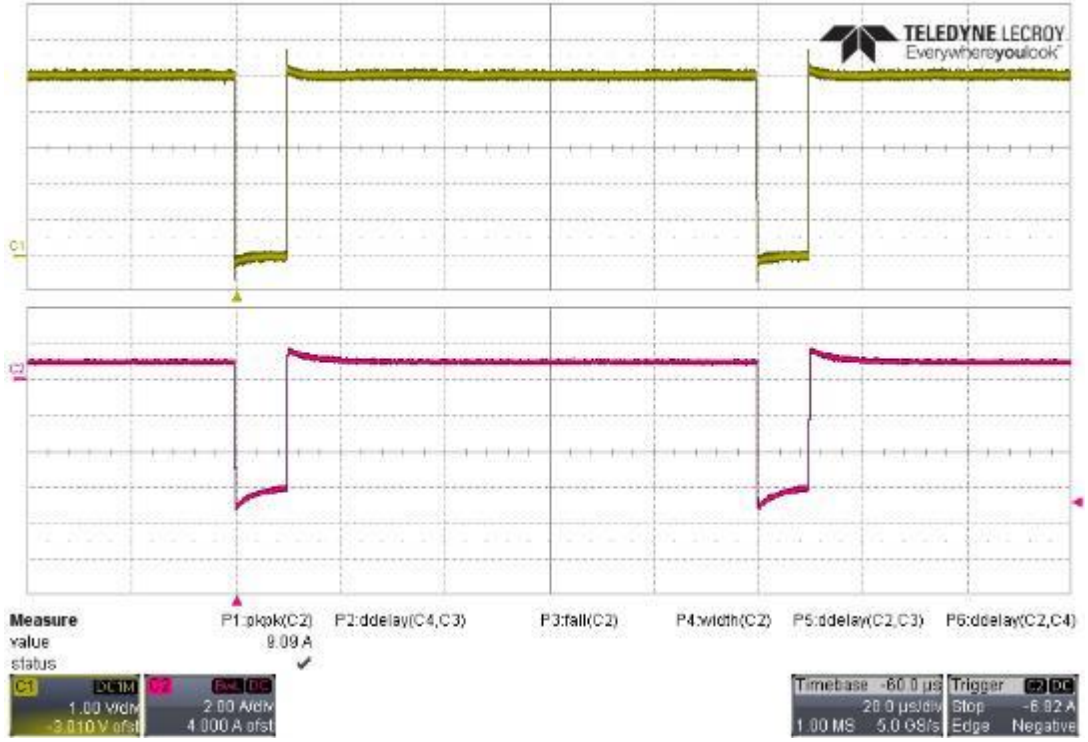
NCP51561 – OUTPUT Source/Sink Current

Peak Source: 4.5 A



Source Peak Current @ VCC=12V

Peak Sink: 9.1 A



Sink Peak Current @ VCC=12V

CH1: IN, CH2: OUT Current

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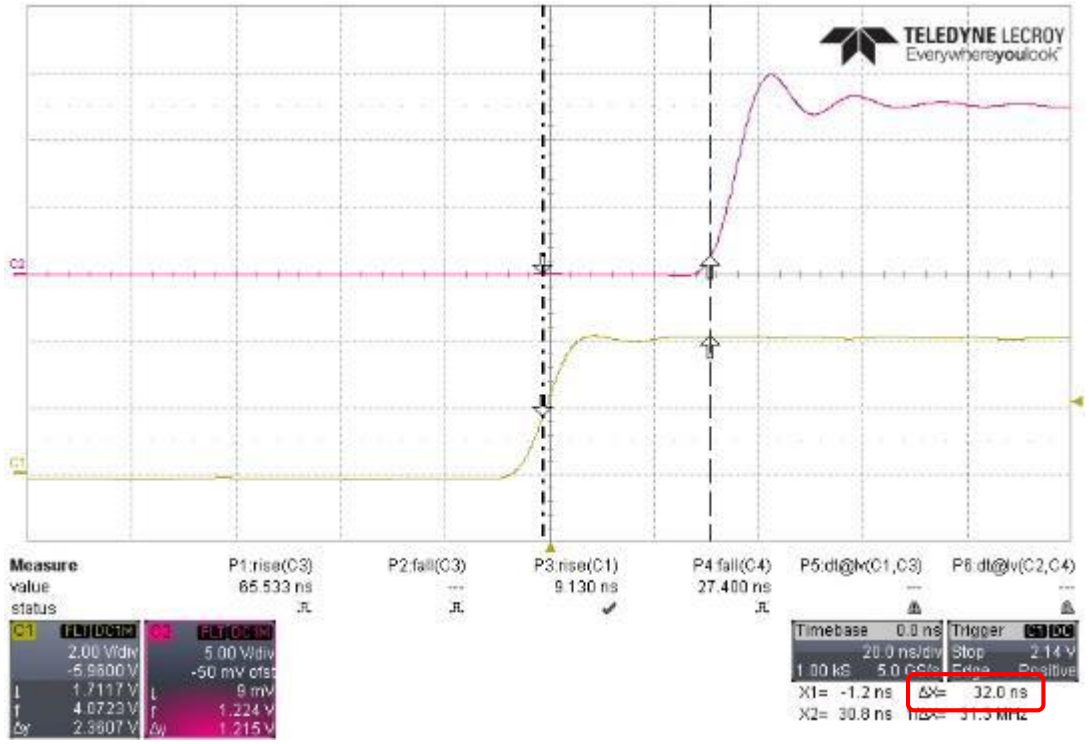
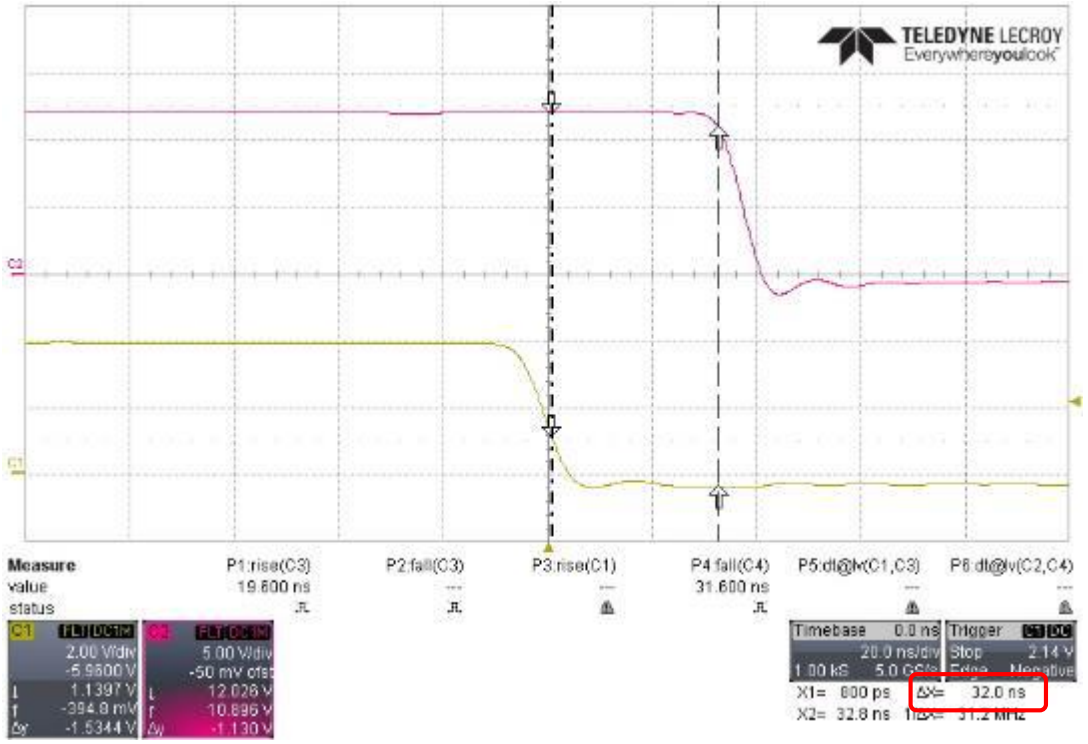
NCP51561 – Fast Propagation Delay Time

- **Propagation Delay Time**
  a. Test Conditions : VDD= 5 V, VCCA=12V, and Cload = 0nF
  b. Test Results : Ton = 32 ns, and Toff = 32 ns

CH1: INA, and CH2: OUTA



Turn-on Delay Time



Turn-off Delay Time

Public Information

Summary of Propagation Delay

- Measurement Results

Item	NCP51561	Compet 1	Compet 2	Compet 3
Turn-on propagation delay [ns]	32.5	23.6	23.8	42.0
Turn-off propagation delay [ns]	32.4	21.8	21.0	44.2
Delay matching [ns]	0.1	1.8	2.8	2.2

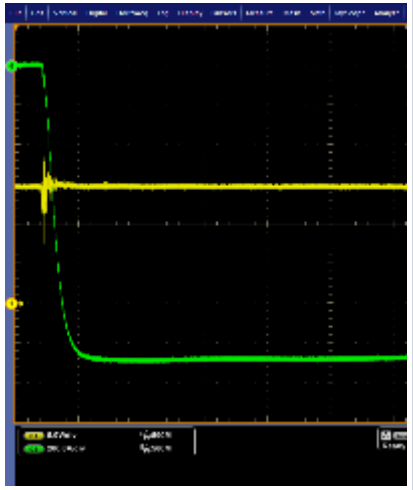
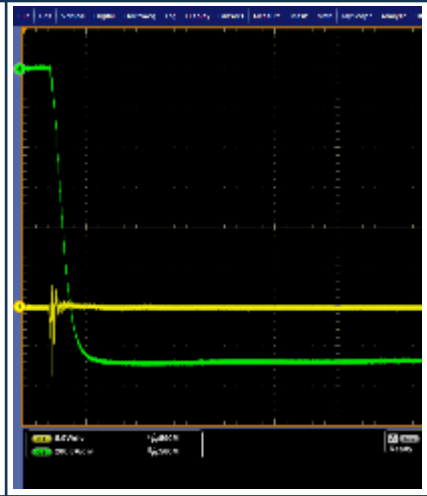
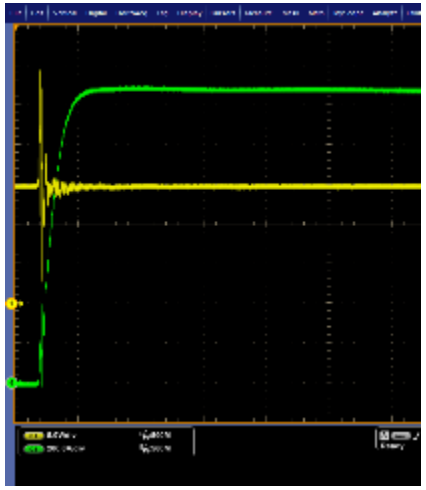
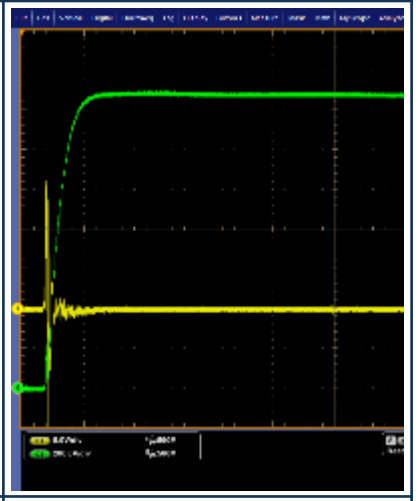
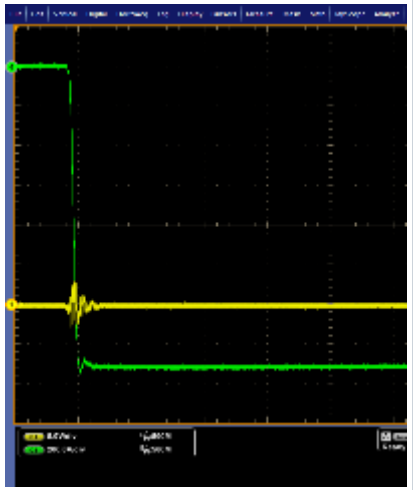
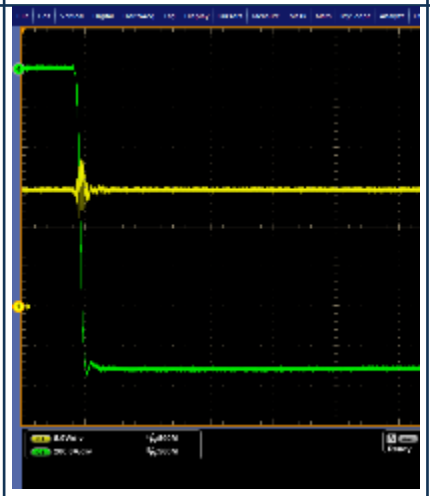
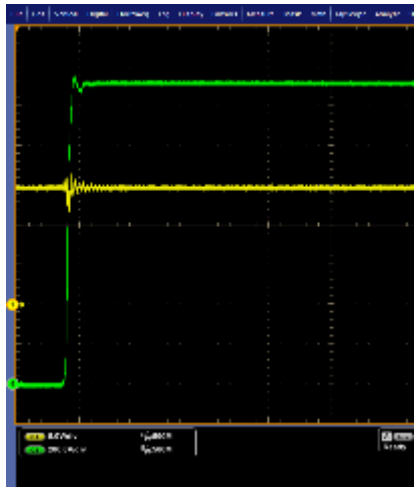
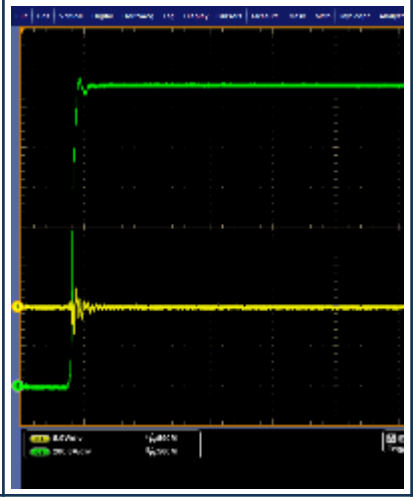
- Specification in Datasheet

Item	NCP51561			Compet 1			Compet 2			Compet 3		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	max	Min	Typ	Max
Turn-on propagation [ns]	25	35	45	14	19	30		30	45	31	37	44
Turn-off propagation [ns]	25	35	45	14	19	30		30	45	31	37	44
Delay matching [ns]	-15		15			5						3

Note : NCP51561 Prelim DS stage as of now

Public Information

NCP51561 – CMTI Performance

dV/dt	Falling pulse (Secondary Rising)		Rising pulse (Secondary Falling)	
	INA=INB=5V	INA=INB=0V	INA=INB=5V	INA=INB=0V
15V/ns Slope OUT [5V/div] GND-VSS [200V/div] Time [200ns/div]				
125V/ns Slope OUT [5V/div] GND-VSS [200V/div] Time [100ns/div]				

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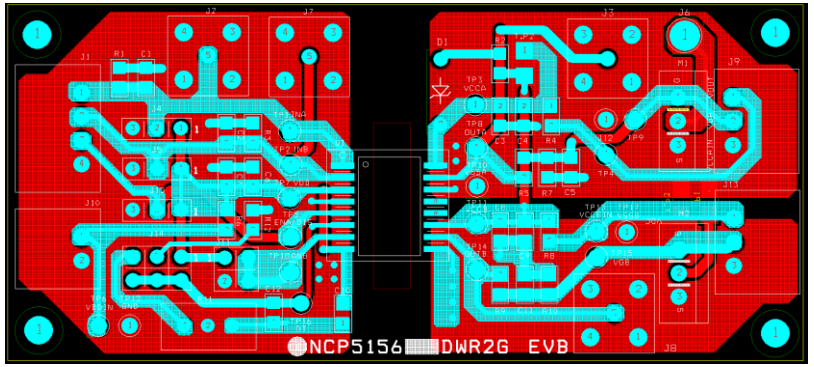
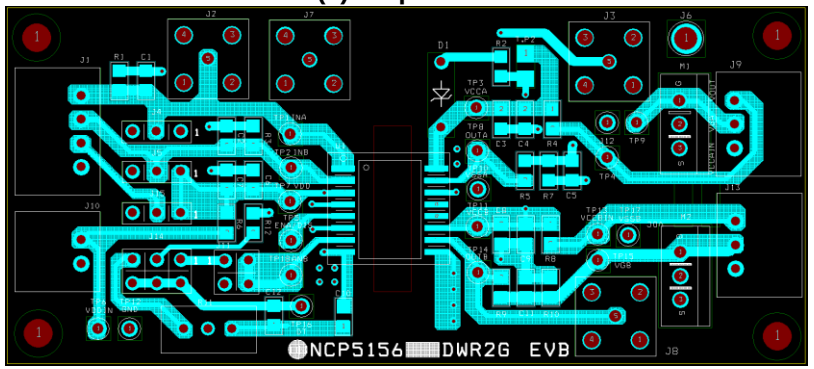
NCP51561 – Printed Circuit Board

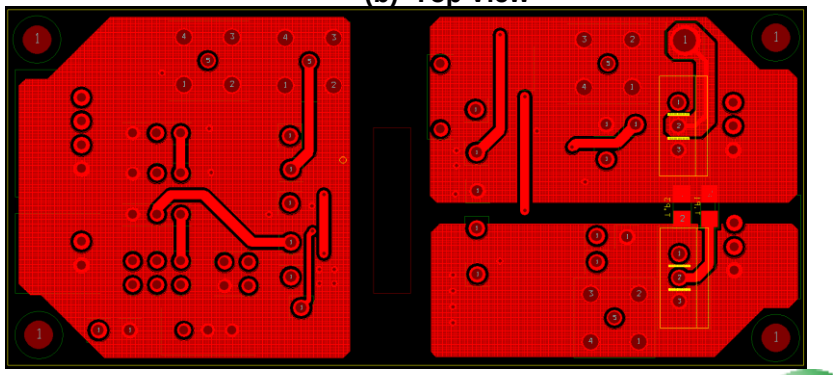
Picture of EVB



(a) Top & Bottom View



(b) Top View



(c) Bottom View

Public Information

NCP/NCV5156x Competitive Landscape

Device		NCP51560	NCP51561	NCD57252	UCC21520	UCC21521	2EDS8165	2EDS8265	Si823x	Si827x	ADuM3223	Unit
Company		ON			TI		IFX		Silicon Lab		ADI	
Absolute Max. Voltage	VDD	5.5	5.5	22	20	20	3.7(1)	3.7(1)	6	6	7	V
	VCC	33	33	36	30	30	22	22	25	25	20	
UVLO Threshold	VDD	2.8	2.8	max. 3	2.7	2.7	2.85	2.85	2.3	2.2		V
		2.7	2.7	min. 2.4	2.5	2.5	2.7	2.7	2.22	2.1		
	VCC	8.7	8.7	13	8.7	8.5	8	8	8.6	8.3	6.9	
		8.2	8.2	12	8.2	8	7	7	8.1	7.8	6.2	
Input Logic Threshold	V_{INH}	1.4/1.7/2.0	1.4/1.7/2.0	1.8/ /	1.8	1.8	2	2	2	2	0.7 * V_{DD}	V
	V_{INL}	0.8/1.1/1.4	0.8/1.1/1.4	/ /1.5	1	1	1.2	1.2	0.8	0.8	0.3 * V_{DD}	
INA,INB, DIS Voltage	V_{IN}	V_{DD} + 0.3	V_{DD} + 0.3	V_{DD} + 0.3	V_{DD} + 0.3	V_{DD} + 0.3	Max. 17	Max. 17			V_{DD}+0.5	V
	Transient(7)	Min -5	Min -5	Min -5	Min -5	Min -5	Min -5	Min -5				
Driving Current	Source	2	4	8	4	4	1	4		1.8	4	A
	Sink	4	8	8	6	6	2	8		4	4	
Turn-on propagation delay		30/40/55	30/40/55	40/ 60 / 90	14 / 19 / 30	/ 19 / 30	31 / 37 /44	31 / 37 /44	/ 30 / 45	20/30/60	35/43/54	ns
Turn-off propagation delay		30/40/55	30/40/55	40/ 60 / 90	14 / 19 / 30	/ 19 / 30	31 / 37 /44	31 / 37 /44	/ 30 / 45	20/30/60	35/43/54	ns
Propagation Delay matching		Max. 15	Max. 15	Max. 20	Max. 5	Max. 5	Max. 3	Max. 3	Max. 5.6	Max. 8	Max. 12	ns
Pulse Width Distortion (T_{PM})		Max. 15	Max. 15	Max. 20	Max. 5	Max. 5						ns
Dead-Time	Min. DT	10	10	20					0.4	0.4		ns
	DT(8)	160/200/240	160/200/240	160/200/240	160/200/240	160/200/240	/ 115 /	/ 115 /	730/900/1170	150/210/260		ns
		R_{DT}= 200kΩ	R_{DT}= 200kΩ	R_{DT}= 200kΩ	R_{DT}= 20kΩ	R_{DT}= 20kΩ	R_{DT}= 62kΩ	R_{DT}= 62kΩ	R_{DT}= 100kΩ	R_{DT}= 100kΩ		
Minimum Input Pulse Width		Max. 30	Max. 30	Max. 30	Max. 20	Max. 20	Typ. 18	Typ. 18				ns
Common mode Transient		Min. 100	Min. 100	Min. 100	Min. 100	Min. 100	Min. 150	Min. 150	Min. 20	Min. 150	Max. 100	V/ns
Device Start-up Time									Max. 40	Typ. 16		us
ESD	HBM(9)	2000			±4000		2000					V
	CDM(9)	500			±1500		500					

Note

1. With SLDO inactive (NC or connected to VDD
2. Input signal (INA, INB, DISABLE) pins transient for 50 ns
3. Dead-time Setting
   - -. NCP5176x : t_{DT}=10 ×R_{DT} where R_{DT} is kΩ and t_{DT} is ns. (Same as TI product)
   - -. UCC2152x : t_{DT}= 10 ×R_{DT} where R_{DT} is kΩ and t_{DT} is ns
   - -. 2EDS8165: R_{DT} = (t_{DT} − 3) / 1.8 where R_{DT} is kΩ and t_{DT} is ns
   - -. Si823x : DT = 10 ×R_{DT}
   - -. Si827x : DT = 2.02 ×R_{DT} + 7.77 (for 10 ~ 200 ns version)
   - -. ADuM3223: No dead-time control function
7. ESD Human Body Model tested per ANSI/ESDA/JEDEC JS-001-2012

ESD Charged Device Model tested per JESD22-C101.

NCP/NCV51563 – Isolated Dual MOS/SiC Drivers with 3.3mm creepage

Value Proposition

The NCP5156x are isolated dual-channel gate driver with up to 4-A/8-A source and sink peak current. It is designed for fast switching to drive power MOSFETs power switches. The NCP5156x offers short and matched propagation delays. Internal functional isolation between the two secondary-side drivers allows a working voltage of up to ~1,200 VDC. The NCP5156x offers other important protection functions such as independent under-voltage lockout for each drivers and disable function.

Unique Features

- Input side isolated from output drivers by 5-kVRMS isolation barrier
- **Increased Channel-to-Channel Spacing**
- **40ns Prop Delay & 15ns Delay Match**
- >= 100 V/ns dV/dt Immunity
- Typical Source/Sink Current Capability of 4-A/8-A

Benefits

- Give reliable operation and safety
- **3.3 mm for higher functional isolation**
- Efficient switching
- High Robustness
- Strong Driver to optimize losses

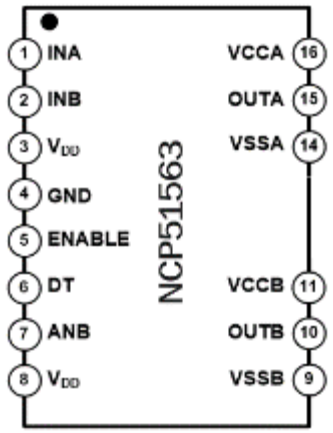
Other Features

- Matched Propagation Delays : Max. 15 ns
- User Programmable Input Logic
  - Single or Dual-input modes via ANB
  - DISABLE or ENABLE mode
- User Programmable Dead-Time Control
- Different UVLO options: 5-V,8-V & 17-V

Market & Applications

- Isolated Converters in Offline AC-to-DC Power Supplies
- Motor Drive and DC-to-AC Solar Inverters
- HEV and EV On-Board chargers

Typical Application Schematic



Higher creepage distance between channel offers better immunity in polluted environments

Sampling Q4-20
P2P with UCC21530

Package Information

- **SOIC-WB14 with high DTI**
- OPN : NCP51563BzDWR2G
  - y: UVLO level
  - z: Enable/Disable

Public Information

NCP51566 – 5 kV Isolated High Performance Dual MOS/SiC Drivers

Value Proposition

The NCP51566 is isolated dual-channel gate driver with up to 4-A/8-A source and sink peak current. It is designed for fast switching to drive power MOSFETs power switches. The NCP51566 offers short and matched propagation delays. Internal functional isolation between the two secondary-side drivers allows a working voltage of up to ~1,200 VDC. The NCP51566 offers other important protection functions such as independent under-voltage lockout for each drivers and enable function.

Unique Features

- Input side isolated from output drivers by 5-kVRMS isolation barrier
- **Max. 45 ns Prop Delay & 5 ns Delay Match**
- **>= 200 V/ns dV/dt Immunity**
- **< 5 ns part-to- part Skew**

Benefits

- Give reliable operation and safety
- Efficient switching
-
- High Robustness
- Easier design

Other Features

- Typical Source/Sink Current Capability up to 4-A/8-A
- Programmable Input Logic
- Single or Dual-input modes via ANB
- ENABLE mode
- User Programmable Dead-Time Control
- Different UVLO options: 5-V,8-V & 17-V

Market & Applications

- Isolated Converters in Offline AC-to-DC Power Supplies
- Motor Drive and DC-to-AC Solar Inverters
- HEV and EV On-Board chargers

Typical Application Schematic

Parameters	Symbol	NCP51566			NCP51561		
		Min	Typ	Max	Min	Typ	Max
Power Supply Voltage – Input side	V_{DD}	3		5	3		5
Power Supply Voltage – Driver side	V_{CC}	9.5		30	9.5		30
Logic Input Voltage at pins INA, INB, ANB and DISABLE	V_{IN}	GND		18	GND		18
Common Mode Transient Immunity	CMTI	150		200	100		120
Turn-On Propagation Delay from INx to OUTx	t_{PDON}	25	35	45	30	40	55
Turn-Off Propagation Delay from INx to OUTx	t_{PDOFF}	25	35	45	30	40	55
Pulse Width Distortion ($t_{PDON} – t_{PDOFF}$)	t_{PWD}			5			15
Mismatching between Channels	t_{DM}			5			15
Turn-On Rise Time	t_R		7			7	
Turn-Off Fall Time	t_F		5			5	
Enable to OUTx Delay	$T_{EABLE,OUT}$		60			60	
Minimum Pulse Width Filtering Time	t_{PW}	10		30	10		30

Sampling Q1-21

Package Information

- SOIC-WB16 with high DTI
- OPN : NCV5156yzDWR2G
- y: UVLO level
- z: Enable/Disable

Public Information

NCP51157 – 5 kV Isolated High Performance MOS/SiC Drivers

Value Proposition

The NCP51157 is isolated 1-channel gate driver with up to 4-A/8-A source and sink peak current. It is designed for very fast switching to drive power MOSFETs power switches. The NCP51157 offers **short and matched propagation delays**. Internal functional isolation between the two secondary-side drivers allows a working voltage of up to ~1,200 VDC. It offers other important protection functions such as under-voltage lockout for each drivers and enable function.

Unique Features

- Input side isolated from output drivers by 5-kVRMS isolation barrier
- **Max. 45 ns Prop Delay & 5 ns Delay Match**
- **>= 200 V/ns dV/dt Immunity**
- **< 5 ns part-to- part Skew**
- Vdd up to 20V

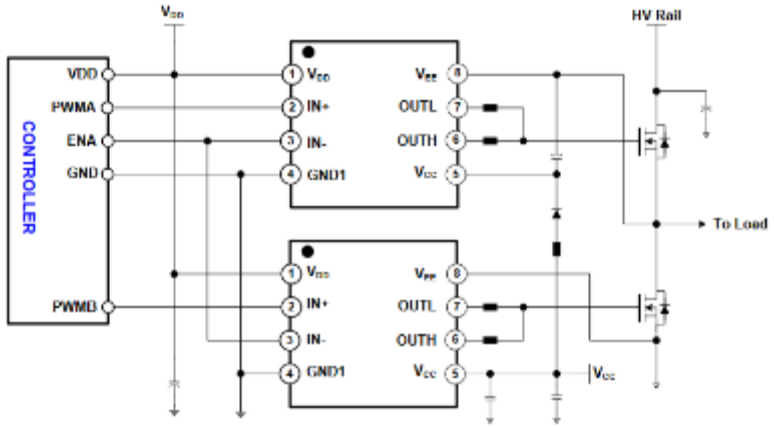
Benefits

- Give reliable operation and safety
- Efficient switching
- High Robustness
- Easier design
- Can work with both Analog and Digital Controllers

Other Features

- Typical Source/Sink Current Capability up to 4-A/8-A
- Programmable Input Logic
- Split Outputs for easier control
- Enable/IN+
- Different UVLO options: 5-V,8-V & 17-V

Typical Application Schematic



Sampling Q1-21

Market & Applications

- Isolated Converters in Offline AC-to-DC Power Supplies
- Motor Drive and DC-to-AC Solar Inverters
- HEV and EV On-Board chargers

Package Information

- SOIC-8 WB with high DTI
- OPN : NCV51157xDWR2G
- x: UVLO level

Public Information

NCP51157 Competitive Landscape (1)

Paramter		Symbol	ON NCP5115x			TI UCC5350SB			Unit
			Min	Typ	Max	Min	Typ	Max	
ABSOLUTE MAXIMUM RATINGS									
Power Supply Voltage – Input side	VDD to GND	V_{DD}	-0.3		5.5	-0.3		18	V
Power Supply Voltage – Driver side	VCC – VEE	V_{CC}	-0.3		33	-0.3		30	V
Driver Output Voltage (OUT-VEE)			V_{EE} - 0.3		V_{CC}+0.3	V_{EE}-0.3		V_{CC}+0.3	V
	Transient for 200ns		V_{EE} - 2		V_{CC}+0.3				V
Input Signal Voltages (IN+, and IN-)			GND - 0.3		20	GND - 5		V_{DD}+0.3	V
	Transient for 50ns		GND - 5		20				V
RECOMMENDED OPERATING CONDITIONS									
Power Supply Voltage – Input side		V_{DD}	3		5	3		15	V
Power Supply Voltage – Driver side		V_{CC}	9.5		30	9.5		33	V
Logic Input Voltage at pins IN+, and IN-		V_{IN}	GND		18				V
Common Mode Transient Immunity		CMTI	150		200 (TBC)	100	120		kV/us
ELECTRICAL SPECIFICATIONS									
PRIMARY POWER SUPPLY SECTION (VDD)									
VDD Quiescent Current	V_{IN+}= Low, V_{IN-} = Low	I_{QVDD}		710	900		1670	2400	uA
	V_{IN+}=High, V_{IN-} =Low			9.5					mA
V_{DD} Operating Current	f_{IN}=500 kHz, C_{LOAD} = 100 pF	I_{VDD}		6	8				mA
VDD Supply Under-Voltage Positive-Going Threshold		V_{DDUV+}	2.7	2.8	2.9		2.60	2.8	V
VDD Supply Under-Voltage Negative-Going Threshold		V_{DDUV-}	2.6	2.7	2.8	2.4	2.5		V
VDD Supply Under-Voltage Lockout Hysteresis		V_{DDHYS}		0.1			0.1		V
SECONDARY POWER SUPPLY SECTION									
V_{CC} Quiescent Current	VINA= VINB = 0 V, per ch	I_{QVCC}		300			1100	1800	uA
	VINA= VINB =5 V, per ch			360					uA
V_{CC} Operating Current	fIN=500 kHz, current per ch, C_{LOAD} = 100 pF	I_{VCC}		2.2			2		mA

NCP51157 Competitive Landscape (2)

Paramter		Symbol	ON			TI			Unit
			NCP5115x			UCC5350SB			
			Min	Typ	Max	Min	Typ	Max	
VCC UVLO THRESHOLD (8-V UVLO Version)									
VCC Supply Under-Voltage Positive-Going		V_{CCUV+}	8.3	8.7	9.2		8.7	9.4	V
VCC Supply Under-Voltage Negative-Going		V_{CCUV+}	7.8	8.2	8.7	7.3	8		V
Under-Voltage Lockout Hysteresis		V_{CCHYS}		0.5			0.7		V
LOGIC INPUT SECTION (IN+, and IN-)									
High Level Input Voltage		V_{INH}	1.4	1.7	2.0		0.55*VDD	0.7*VDD	V
Low Level Input Voltage		V_{INL}	0.8	1.1	1.4	0.3*VDD	0.45*VDD		V
Input Logic Hysteresis		V_{INHYS}		0.6			0.1*VDD		V
Negative Transient referenced to GND	For 50 ns pulse	V_{INA}, V_{INB}	-5						V
High Level Logic Input Bias Current	IN+ = VDD	I_{IN+}	20	25	33		40	240	uA
Low Level Logic Input Bias Current	IN- = GND	I_{IN-}	-33	-25	-20	-240	-40		uA
	IN- = GND - 5 V					-310	-80		uA
GATE DRIVE SECTION for 4-A/8-A									
OUTA and OUTB Source Peak Current	V_{IN+}= High, V_{IN-} = Low, PW ≤ 5 us	I_{OUT+}		4		5	10		A
OUTA and OUTB Sink Peak Current	V_{IN+}= Low, V_{IN-} = High, PW ≤ 5 us	I_{OUT-}		8		5	10		A
DYNAMIC ELECTRICAL CHARACTERISTICS									
Turn-On Propagation Delay from INx to OUTx	0 V <-> 5 V, 1V/ns Slew Rate	t_{PDON}		35	TBD		65	100	ns
Turn-Off Propagation Delay from INx to OUTx	C_{LOAD}=1.8 nF	t_{PDOFF}		35	TBD		65	100	ns
Pulse Width Distortion (t_{PDON} – t_{PDOFF})		t_{PWD}			5			20	ns
Mismatching between Channels	INA=INB , f_{IN} = 100 kHz	t_{DM}			TBD			25	ns
Turn-On Rise Time	CLOAD=1 nF	t_R		10			10	25	ns
Turn-Off Fall Time	10% to 90%/90% to 10%	t_F		10			10	22	ns
Minimum Pulse Width Filtering Time	C_{LOAD}=0 nF,	t_{PW}	10		30			20	ns

NCP51152 – 3.7 kV Isolated High Performance MOS/SiC Drivers

Value Proposition

The NCP51152 is isolated 1-channel gate driver with up to 4-A/8-A source and sink peak current. It is designed for very fast switching to drive power MOSFETs power switches. The NCP51152 offers **short and matched propagation delays**. Internal functional isolation between the two secondary-side drivers allows a working voltage of up to ~1,200 VDC. It offers other important protection functions such as under-voltage lockout for each drivers and enable function.

Unique Features

- Input side isolated from output drivers by 3.7-kVRMS isolation barrier
- **Max. 45 ns Prop Delay & 5 ns Delay Match**
- **>= 200 V/ns dV/dt Immunity**
- **< 5 ns part-to- part Skew**
- Vdd up to 20V

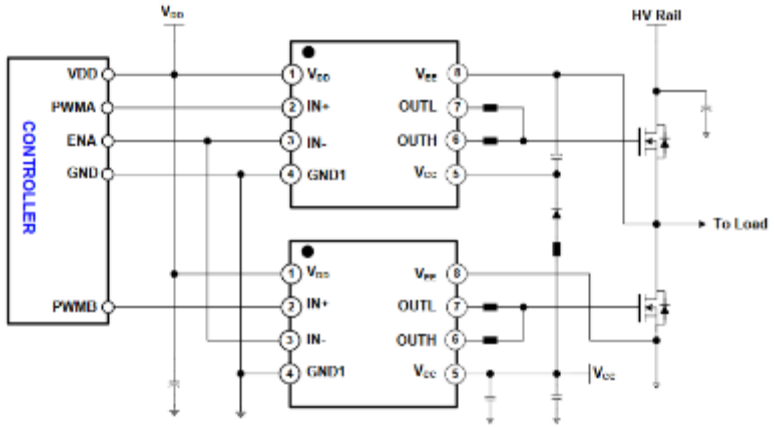
Benefits

- Give reliable operation and safety
- Efficient switching
- High Robustness
- Easier design
- Can work with both Analog and Digital Controllers

Other Features

- Typical Source/Sink Current Capability up to 4-A/8-A
- Programmable Input Logic
- Split Outputs for easier control
- Enable/IN+
- Different UVLO options: 5-V,8-V & 17-V

Typical Application Schematic



Sampling Q1-21

Market & Applications

- Isolated Converters in Offline AC-to-DC Power Supplies
- Motor Drive and DC-to-AC Solar Inverters
- HEV and EV On-Board chargers

Package Information

- SOIC-8 NB for space saving
- OPN : NCV51152xDR2G
- x: UVLO level

Public Information

NCP/NCV51752 – Isolated Gate Driver with Internal Chg Pump

Value Proposition

The NCP/V51752 driver is designed to primarily drive SiC MOSFET transistors. For the lowest possible conduction losses, the driver is capable to deliver the maximum allowable gate voltage to the SiC MOSFET device. For improved reliability, dV/dt immunity and even faster turnoff, the NCP/NCV51752 can utilize its on-board charge pump to generate a user selectable negative voltage rail.

Unique Features

- Input side isolated from output drivers by 5-kVRMS isolation barrier
- **On-board regulated negative charge pump (options for -3V,-4V,-5V)**
- Vdd up to 20V

Benefits

- Give reliable operation and safety
- **Simplified BOM and no need for extra isolated DC/DC**
- Can work with both Analog and Digital Controllers

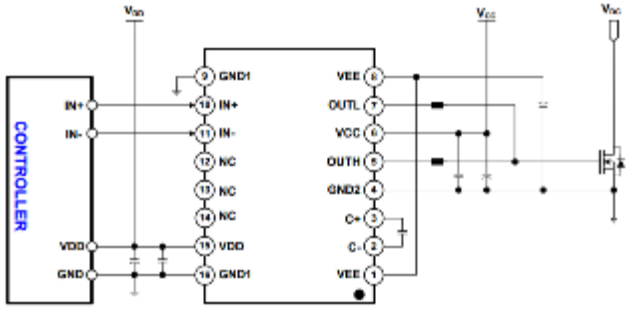
Other Features

- High peak output current 4A/-8A
- Split sink/source outputs for easier dV/dt control
- Extended positive voltage rating for efficient SiC MOSFET operation during the conduction period
- Different UVLO options: 5-V,8-V,13-V & 17-V
- With or Without Dead-Time

Market & Applications

- Industrial Inverters, Motor drives
- High Performance PFC, AC/DC & DC/DC Converters
- HEV and EV Traction inverters

Typical Application Schematic



Sampling Q2-21

Package Information

- SOIC-16 WB
- OPN : NCP51752xDWR2G
  NCV51752xDWR2G

Public Information

NCP/NCV51755 – Isolated Full Features SiC MOSFET Gate Driver

Value Proposition

The NCP/V51755 driver is designed to primarily drive SiC MOSFET transistors. For the lowest possible conduction losses, the driver is capable to deliver the maximum allowable gate voltage to the SiC MOSFET device. For improved reliability, dV/dt immunity and even faster turnoff, the NCV51755 can utilize its on-board charge pump to generate a user selectable negative voltage rail.

Unique Features

- Input side isolated from output drivers by 5-kVRMS isolation barrier
- On-board regulated negative charge pump
- I2C to program driver parameters & Bi-directional communication
- Active Clamp

Benefits

- Give reliable operation and safety
- Simplified BOM and no need for extra DC/DC
- UVLO/DESAT/DRIVE/TSD, ...
- Fault reporting from driver to µCtrl
- For single ended/low freq SiC & IGBT

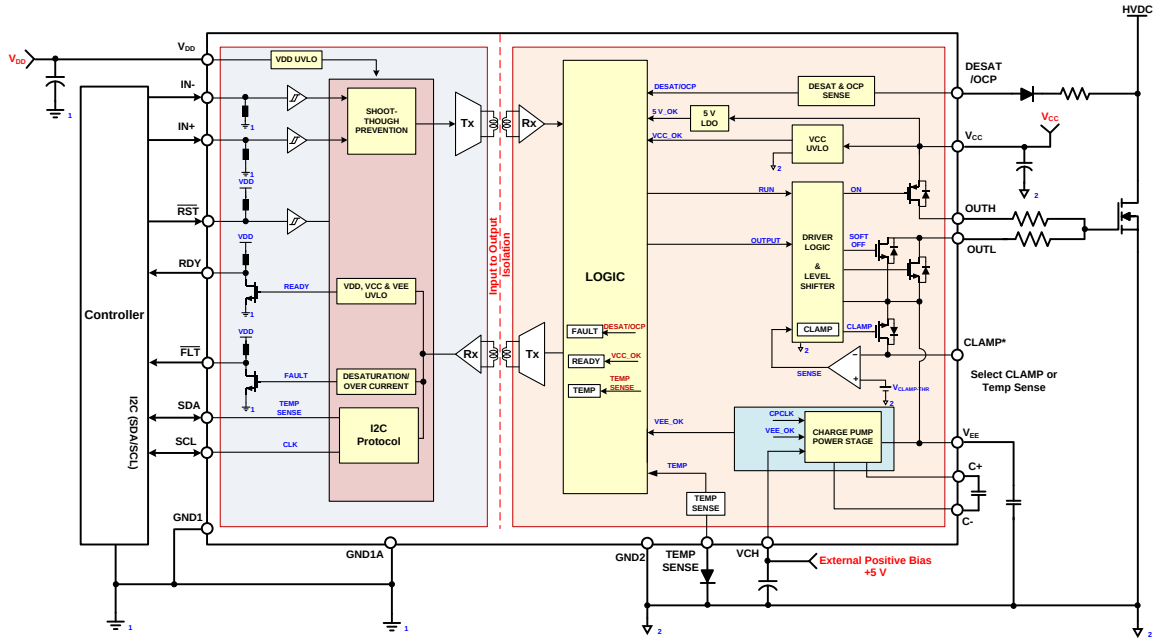
Other Features

- High peak output current - 6A
- Split sink/source outputs for easier dV/dt control
- Extended positive voltage rating for efficient SiC MOSFET operation during the conduction period
- Thermal shutdown function and Temp Sense via NTC
- DESAT detection for short circuit protection

Market & Applications

- Industrial Inverters, Motor drives
- High Performance PFC, AC/DC & DC/DC Converters
- HEV and EV Traction inverters

Typical Application Schematic



Package Information

- SOIC-20 WB
- OPN : NCP51755DWR2G
  NCV51755DWR2G

Planning

Public Information

Isolated Gate Drivers Value Proposition

Performance:

- 30% faster propagation delay and CMTI up to 150V/ns
- New GI structure with CMTI up to 200V/ns and tighter spec in 2021
- Integrated Negative Charge Pump & Fast fault detection

Reliability & Robustness:

- DESAT, Adj UVLO, TSD, Neg. Ch. Pump, I2C , FLT, Enable
- Embedded Vstress and IPT
- Low pulse-width distortion, Low part-part variation in delay times

Cost/Convenience:

- Simplified BOM due to high integration
- Elimination of buffers for most applications
- Dedicated features for each power switch type

Confidential

Thank you – Stay Tuned

PCS Gate Driver Product Line Managers

Marc Barboni (marc.barboni@onsemi.com)
Steve Yoo (steve.yoo@onsemi.com) for Asia region

Appendix D

Public Information

Galvanic Isolated Techniques

Optical	Transformer	Capacitor	RF
ADVANTAGES: • Mature Technology (Oldest) • Have improved over decades • Have decreased LED aging over time • Physical Barrier utilizing Dielectric Material • Used by Top Companies like ON Semi, Avago and others • No Turn ON/OFF spurries oscillations	**ADVANTAGES:** • No LED to wear out • Used by many suppliers • Consistent propagation delay vs. temperature • Lowest current consumption • Generally higher CMR than optical isolators • Lower part-to-part skew than optical	**ADVANTAGES:** • Physical barrier utilizing dielectric insulating material • No LED to wear out • Total immunity to magnetic fields • Used by Texas Instruments & SiLabs	**ADVANTAGES:** • Requires less input power than optoisolator technologies • Lower propagation delay than optoisolators • Total immunity to magnetic fields • No LED to wear out
DISADVANTAGES • Relatively Large Drive Current for Primary LED side • Unable to implement 'Exclusive OR' shoot through feature • Relatively large variation in propagation delay with temperature chan	**DISADVANTAGES** • Some sensitivity to magnetic fields • Possible oscillations going into Saturation and Desaturation modes	**DISADVANTAGES** • Higher current consumption than transformer isolation	**DISADVANTAGES** • Higher current consumption than magnetic isolation • Carrier frequency limits pulse position accuracy
ON Drivers & Signal Isolation	ON Drivers	ON Signal Isolation	

Isolation Technology Comparison

Attribute		OptoCoupler	On-chip Magnetic	On-chip Capacitive	Off-chip Capacitive
Isolation		Epoxy/gel	SiO_2 or equivalent	SiO_2 or equivalent	Ceramic Substrate
Signal coupling		Light (LED +diode)	Magnetic field	Electric field	Electric field
Speed		Slow	Fast	Fast	Fast
Distance Through Insulation (DTI)		>0.5 mm	~20 microns	~20 microns	>0.38 mm and >0.5 mm option
CMTI		~25 kV/us	High CM impedance, trade-off between spacing and CMTI	Low CM impedance, trade-off between current and CMTI	100 V/ns minimum
EMI EMC	Susceptibility	Non-issue – too slow	Design techniques	Signal level dependent	CMTI, SNR
	Radiation	Non-issue (light transmission)	Design techniques	Signal level dependent	Adjustable carrier Differential signaling
Temperature		Up to 110°C	Wide range (150 °C)	Wide range (150 °C)	Wide range (150 °C)
Standards		UL1577, IEC60747-5-5, C-UL, CQC etc	UL1577, VDE0884-11	UL1577, VDE0884-11	UL1577 (c… prote… VD… 84-…