Application note No. 1: building the hardware

Imaging solutions project objectives

This is the first of three application notes for creating imaging solutions using the 96Boards onsemi Dual Camera Mezzanine and Ultra96V2.

In this project, we demonstrate how to build the hardware design by using the 96Boards onsemi Dual Camera Mezzanine with the Avnet Ultra96V2 board.

The expected outcome of this project is a Xilinx Shell Archive (XSA) for use in the development of higher-level applications running in PetaLinux. This project will also explain the major elements of the hardware design in the Vivado® Design Suite to ensure later concepts and procedures are understood. We recommend the project outlined in this application note be created on a Xilinx-supported 64-Bit Linux operating system. The two subsequent application notes require creation and use of embedded Linux.

Getting started: requirements

The following hardware is required to follow this series of application notes:

- Ultra96V2
- Ultra96V2 power supply
- 96Boards onsemi Dual Camera Mezzanine
- SD card

To implement this series of application notes, you will need the following Xilinx software installed:

- Vitis 2020.1, including Vivado 2020.1
- PetaLinux 2020.1
- Git
- Terminal application

You'll need a few licenses for this implementation. Bitstreams for the Xilinx ZU3EG device can be generated license-free as part of the Xilinx Vivado webPACK. However, some of the IP used within this design requires an additional license. This license is provided with the Ultra96V2 and is marked "OEM Zynq ZU3 Ultra96 Vivado Design Edition with SDSoC Voucher Pack." Redeem this license and install it on the machine you're using to implement the project. Once it is installed, you can use the license manager (see Figure 1) to see the licensed IP, including the on-screen display.

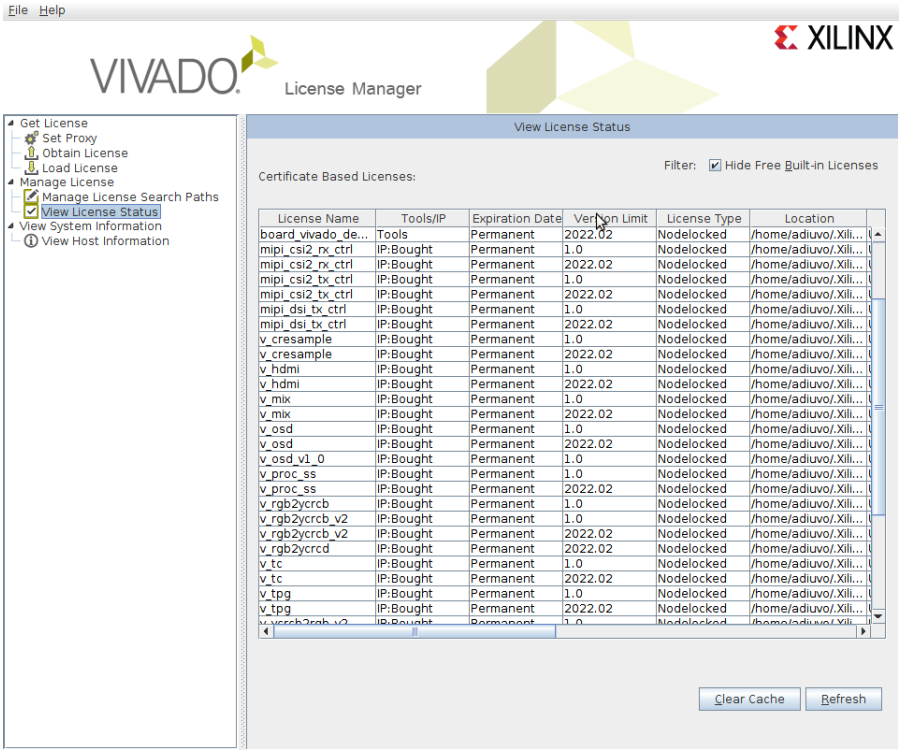


Figure 1. Check that the correct license is installed using the license manager.

Introduction to image sensor flexibility

The 96Boards onsemi Dual Camera Mezzanine provides support for two imaging sensors and is designed to be flexible, allowing support for a range of image sensors of varying color spaces and resolutions. To support a flexible integration, both image sensors are connected to an image co-processor (Image Signal Processor or ISP) on the 96Boards onsemi Dual Camera Mezzanine (see Figure 2). The ISP merges the images into one and outputs a mobile industry processor interface (MIPI) stream to the Ultra96 board, where the image is recovered and processed by the Xilinx ZU3EG MPSoC.

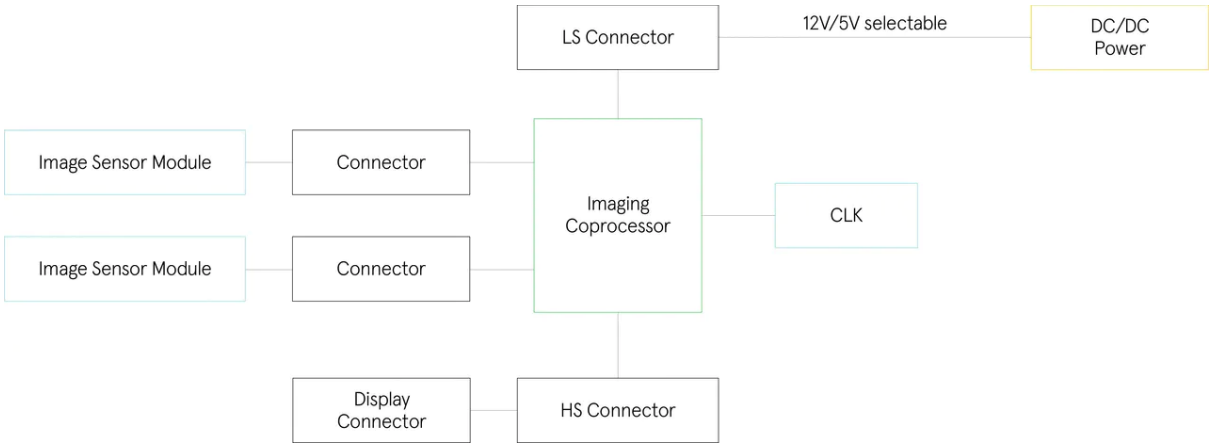


Figure 2. 96Boards onsemi Dual Camera Mezzanine architecture

MIPI is a high-bandwidth, point-to-point protocol used to transfer image sensor or display information over several differential serial lanes. Like most protocols, it works on the OSI model with different layers of implementation. The lowest level of the MIPI protocol is the DPHY, which defines the number of lanes, clocking and the transition between differential (scalable low voltage swing, or SLVS) and single-ended signalling (LVCMOS).

This combination of high-speed differential and low-speed, single-ended signalling enables the high-bandwidth transfer of the image/display data using a higher-level protocol such as CSI-2 or DSI. The low-speed communication enables the low-level protocol information to be communicated at lower power. Each MIPI DPHY link may have between one and four high-speed serial links operating at up to 2.5 Gbps or 10 Gbps across all four lanes. Data transfer over these lanes occurs at double the data rate and is synchronous to the clock lane.

The 96Boards onsemi Dual Camera Mezzanine comes with two CAV10-000A image sensors as standard. These offer a 1-megapixel resolution (1280 pixels by 800 lines) and output a grayscale image. To support high-speed operations the sensors offer a global shutter, which prevents artifacts that might appear in the image if a rolling shutter was used to capture high-speed images (see Figures 3 and 4).

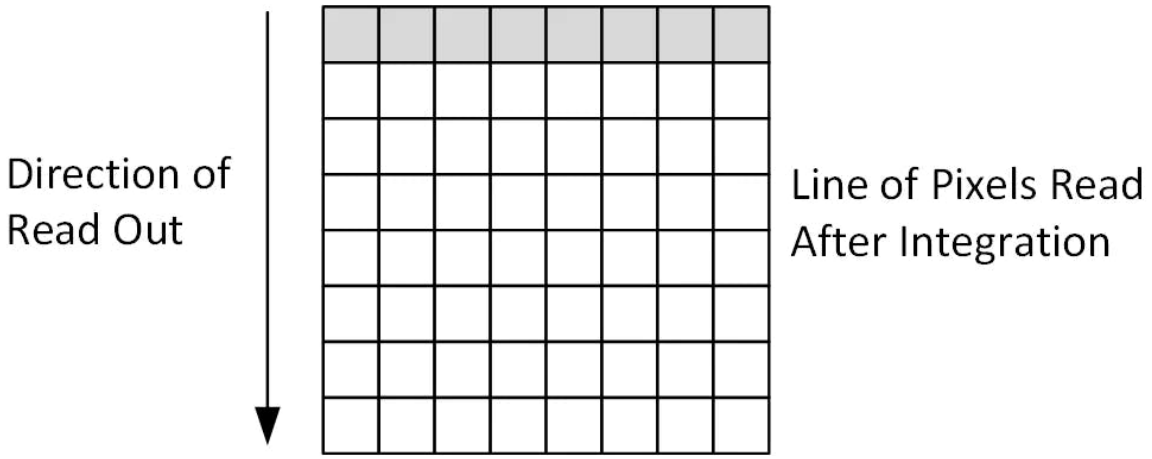


Figure 3. Rolling shutter line by line read out

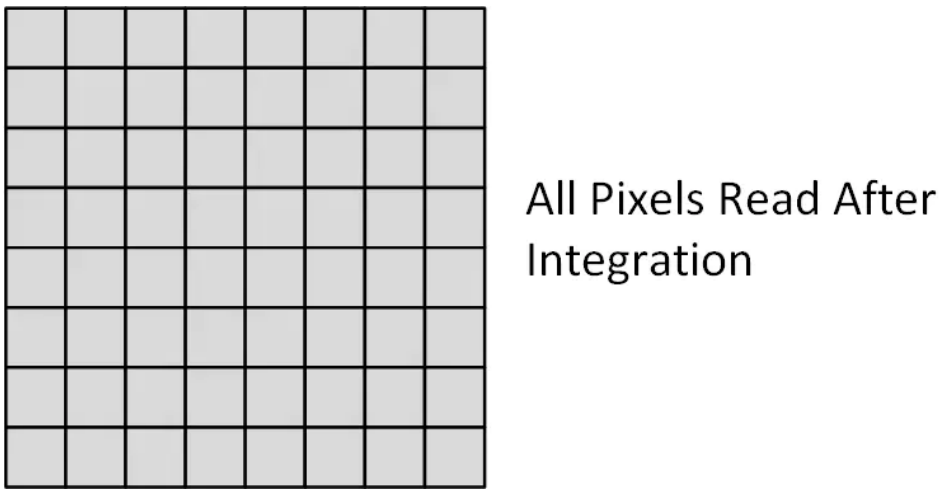


Figure 4. Global shutter accesses all pixels at once

Grayscale imaging is popular for many industrial applications. In fact, one of the first operations in many image-processing systems is to convert the image from color to grayscale. For example, see this edge detection application where the first stage is converted to grayscale. Grayscale provides luminance information on the image, which is one of the most important factors in finding visual features. Elements such as brightness, contrast, edges, shape, contours, texture, perspective and shadow can be identified without the need for a color image.

Assembling Ultra96V2 and 96Boards onsemi Dual Camera Mezzanine

1. Ensure that the Ultra96V2 is powered off and the power supply is disconnected (see Figure 5).

Figure 2. Ultra96V2 and 96Boards onsemi Dual Camera Mezzanine board ready for assembly

2. Gently align the 96Boards onsemi Dual Camera Mezzanine board. Carefully align the high-speed and low-speed connector and press the two boards together.

Figure 3. Aligning the high-speed and low-speed connectors

3. Once both boards are mated, connect the power supply to the Ultra96V2 such that it is ready to power up when required (see Figure 7).

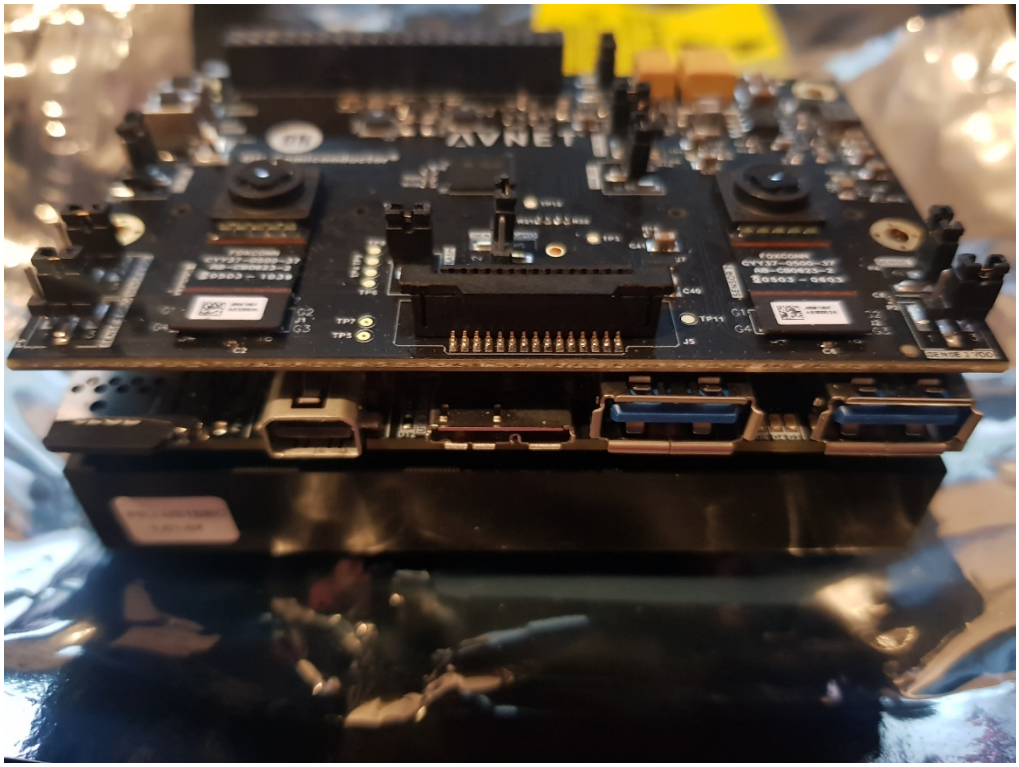


Figure 4. Assembled system ready for testing

Hardware project creation

1. Create a directory for the 96Boards onsemi Dual Camera Mezzanine. In Linux, use the command *mkdir -p <directory name>* once the directory is created cd into it (see Figure 8).

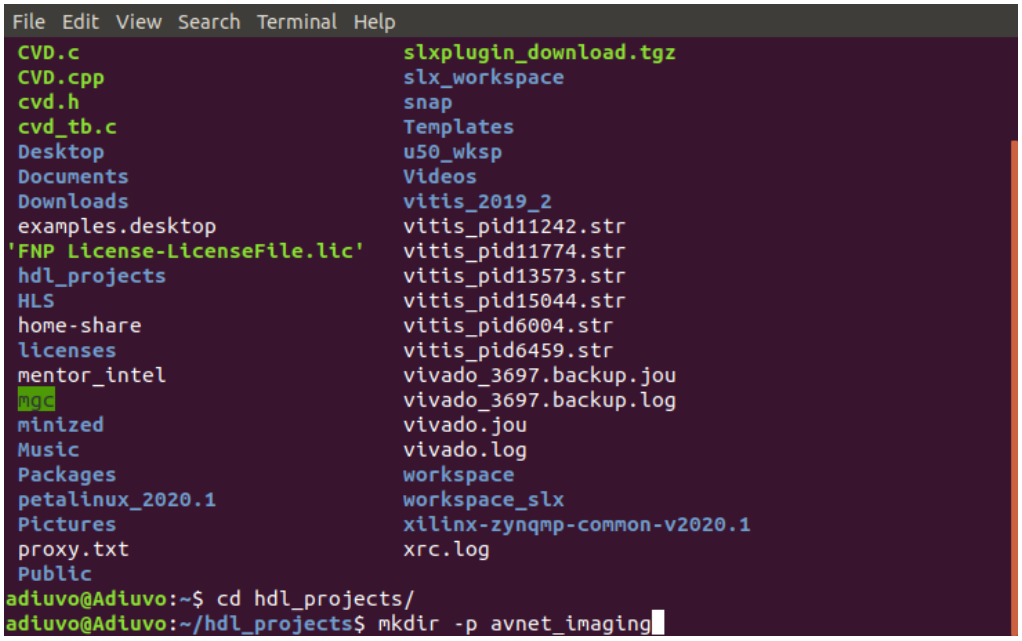


Figure 8. Creating the new directory

2. The next step is to clone the Avnet bdf repository (see Figure 9). From the command line inside the directory you just created, enter the command *git clone https://github.com/Avnet/bdf.git*

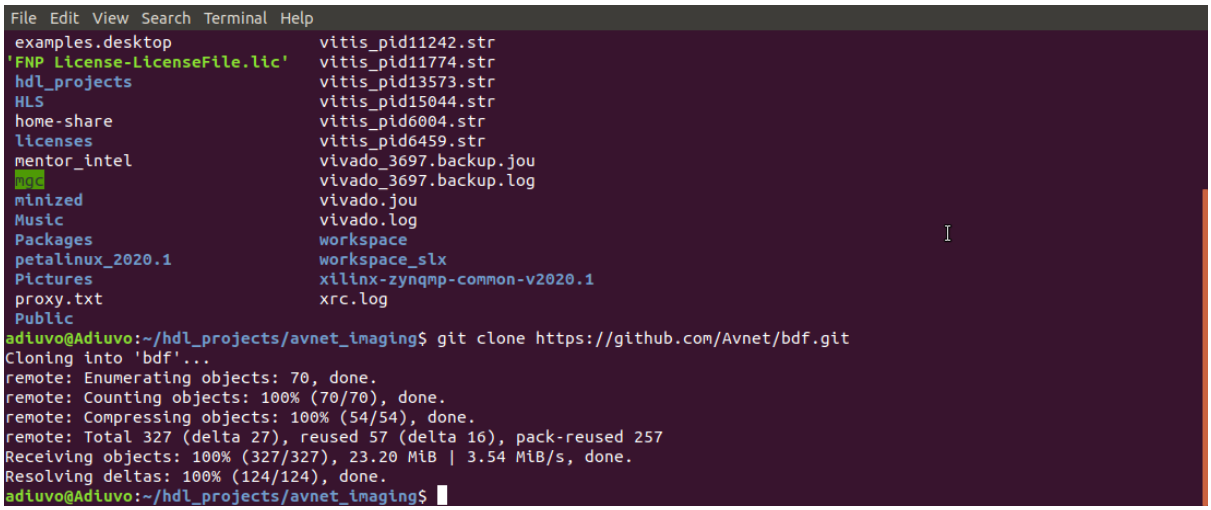


Figure 9. Cloning the Avnet bdf repository

3. The final repository to clone for this application note is the HDL repository (see Figure 10). Use the command git clone https://github.com/Avnet/hdl.git

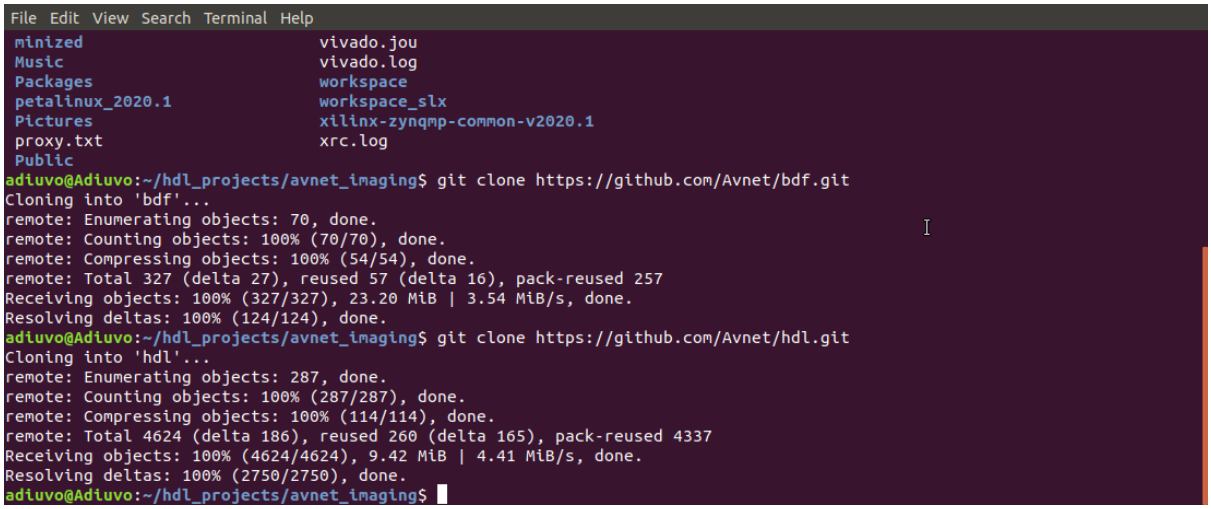


Figure 10. Cloning the Avnet HDL repository

4. With the repositories cloned, the next step is to ensure we check out the correct branch from the master. For the bdf repository, we want to work from the master branch. To do this, we cd into the newly cloned bf folder and execute the command *git checkout master* (see Figure 11).

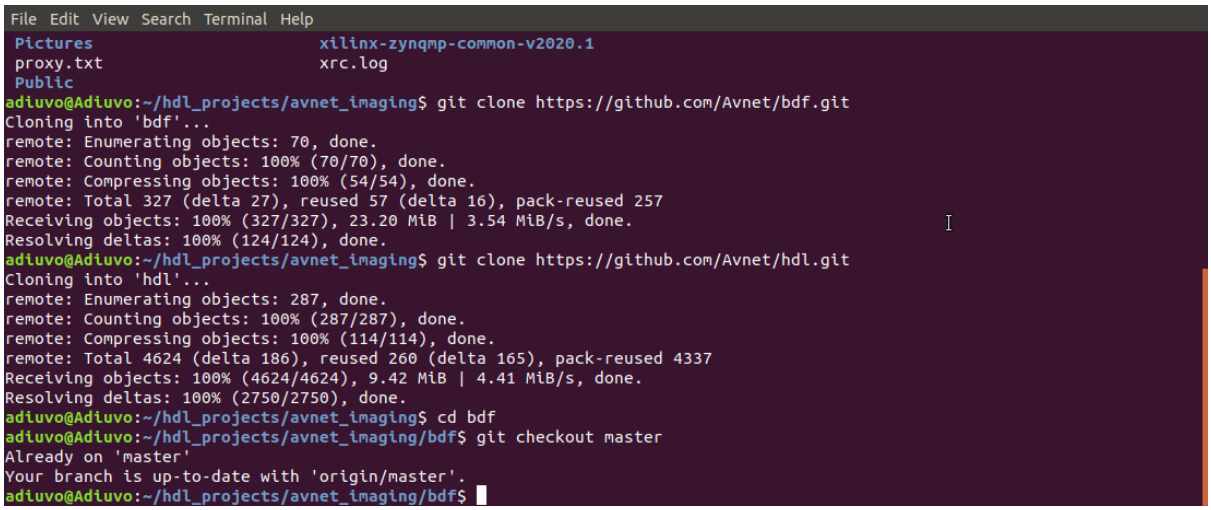


Figure 11. Checking out the bdf master branch

5. For the HDL branch, we want to check out the 2020.1 branch. Use the command *git checkout 2020.1* again from within the HDL folder (see Figure 12).

```
File  Edit  View  Search  Terminal  Help
remote: Enumerating objects: 70, done.
remote: Counting objects: 100% (70/70), done.
remote: Compressing objects: 100% (54/54), done.
remote: Total 327 (delta 27), reused 57 (delta 16), pack-reused 257
Receiving objects: 100% (327/327), 23.20 MiB | 3.54 MiB/s, done.
Resolving deltas: 100% (124/124), done.
adiuvo@Adiuvo:~/hdl_projects/avnet_imaging$ git clone https://github.com/Avnet/hdl.git
Cloning into 'hdl'...
remote: Enumerating objects: 287, done.
remote: Counting objects: 100% (287/287), done.
remote: Compressing objects: 100% (114/114), done.
remote: Total 4624 (delta 186), reused 260 (delta 165), pack-reused 4337
Receiving objects: 100% (4624/4624), 9.42 MiB | 4.41 MiB/s, done.
Resolving deltas: 100% (2750/2750), done.
adiuvo@Adiuvo:~/hdl_projects/avnet_imaging$ cd bdf
adiuvo@Adiuvo:~/hdl_projects/avnet_imaging/bdf$ git checkout master
Already on 'master'
Your branch is up-to-date with 'origin/master'.
adiuvo@Adiuvo:~/hdl_projects/avnet_imaging/bdf$ cd ..
adiuvo@Adiuvo:~/hdl_projects/avnet_imaging$ cd hdl/
adiuvo@Adiuvo:~/hdl_projects/avnet_imaging/hdl$ git checkout 2020.1
Branch '2020.1' set up to track remote branch '2020.1' from 'origin'.
Switched to a new branch '2020.1'
adiuvo@Adiuvo:~/hdl_projects/avnet_imaging/hdl$
```

Figure 12. Checking out the 2020.1 branch of the HDL repository

6. With the repositories cloned and the correct branches checked out, the project can be created by using the project build script (see Figure 13). From within the HDL folder, CD into scripts and execute the command *Vivado -mode batch -source ./make_ultra96v2_dualcam.tcl*

```
File  Edit  View  Search  Terminal  Help
adiuvo@Adiuvo:~/hdl_projects/avnet_imaging/hdl$ cd Scripts/
adiuvo@Adiuvo:~/hdl_projects/avnet_imaging/hdl/Scripts$ vivado -mode batch -source ./make_ultra96v2_dualcam.tcl

****** Vivado v2020.1 (64-bit)
  **** SW Build 2902540 on Wed May 27 19:54:35 MDT 2020
  **** IP Build 2902112 on Wed May 27 22:43:36 MDT 2020
    ** Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.

source ./make_ultra96v2_dualcam.tcl
# set argv [list board=ULTRA96V2 project=ultra96v2_dualcam sdk=no close_project=no version_override=yes dev_arch=zynqmp]
# set argc [llength $argv]
# source ./make.tcl -notrace

*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
*-                                                                          -*
*-        Welcome to the Avnet Project Builder                              -*
*-                                                                          -*
*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*
*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*

BDF path set to /home/adiuvo/hdl_projects/avnet_imaging/bdf
```

Figure 13. Building the project using the project script

7. Following this command, the script will create the Vivado project, synthesize the design and implement the design for the Zynq ZU3EG device used on the Ultra96V2. This may take some time, depending upon the capabilities of the build machine. A typical build time may take about an hour.

Understanding the hardware project

With the project created, we can now explore the design that was created in Vivado (see Figure 14). To do this, we need to launch the Vivado GUI and open the project just created.

1. In the terminal window, enter the command *Vivado* and this will launch the Vivado GUI.

2. In the Vivado GUI, open the project ultra96V2_2020_1 under the Ultra96v2_dualcam directory in the HDL/Projects directory

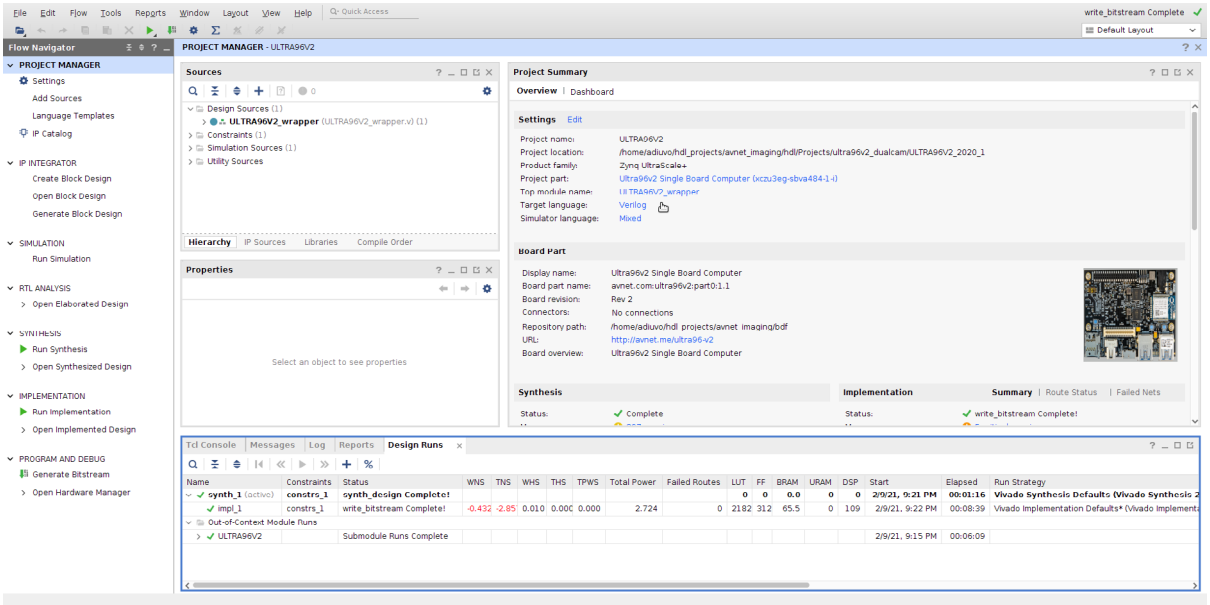


Figure 14. Project open in Vivado

3. Open the block diagram (see Figure 15) to observe the design that has been implemented in the project and float the block diagram so that it is in its own window.

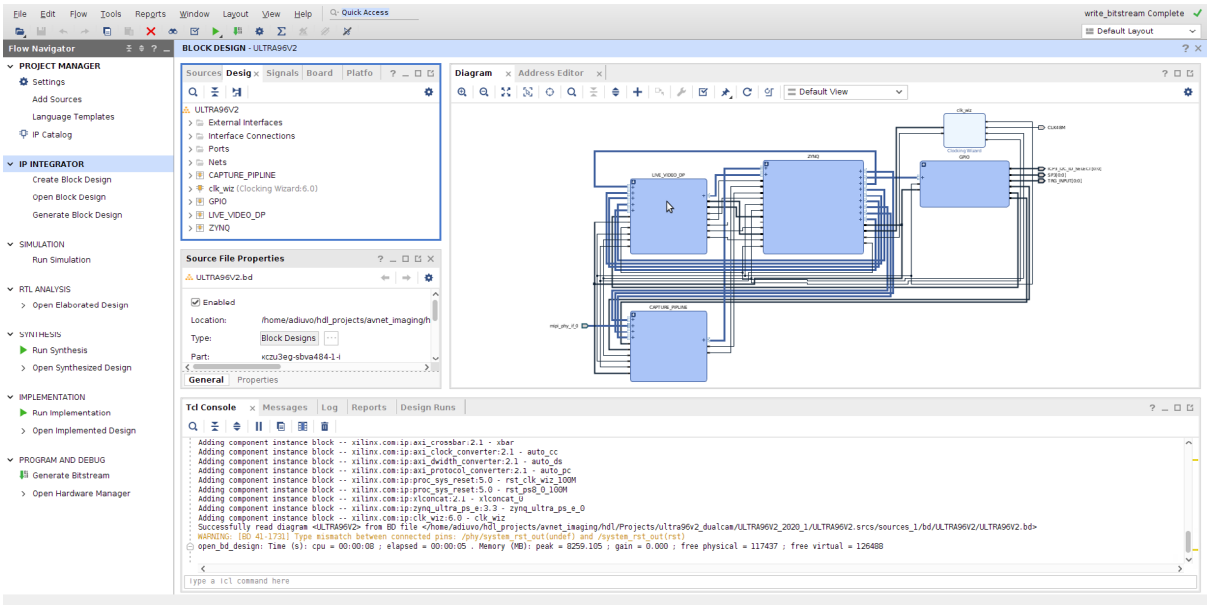


Figure 15. Block diagram opened in Vivado

4. Note how there are four hierarchical elements in the block design (see Figure 16). These blocks contain the Zynq MPSoC processing system, the capture pipeline, live video display port and the GPIO needed in the system.

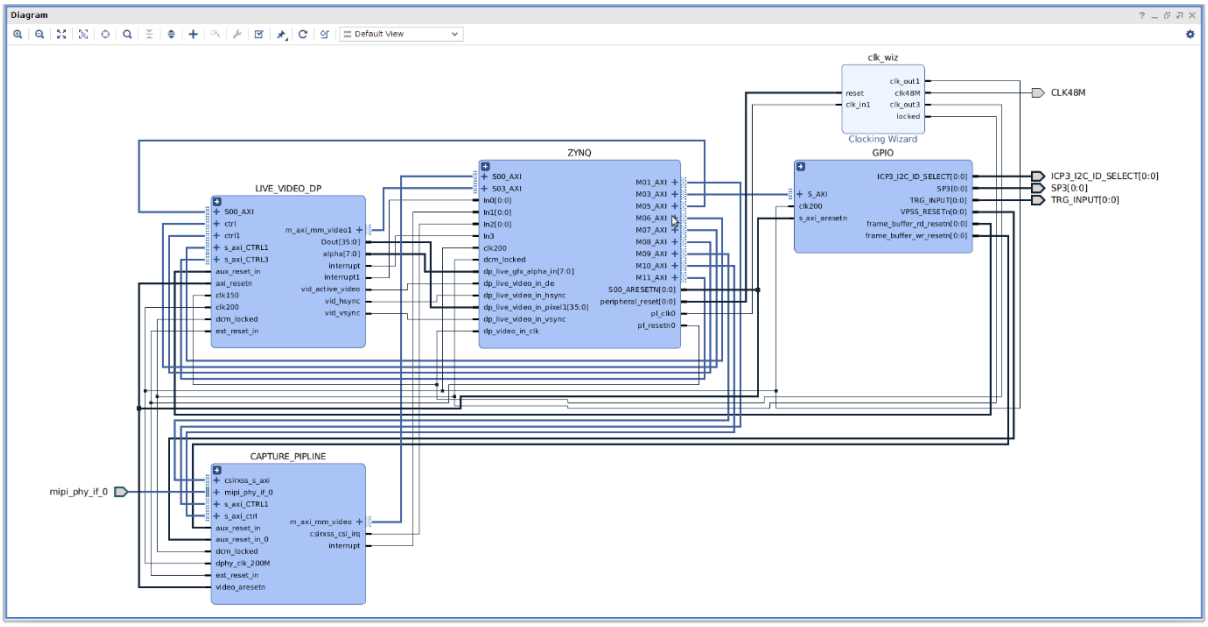


Figure 16. Block diagram of the image processing system

5. The clocking architecture (see Figure 17) of the design is critical and a multi-clock design is implemented with the 200MHz and 150MHz being used as references for the MIPI interface and the AXI Stream video processing network. The 48MHz clock is provided externally to the ISP.

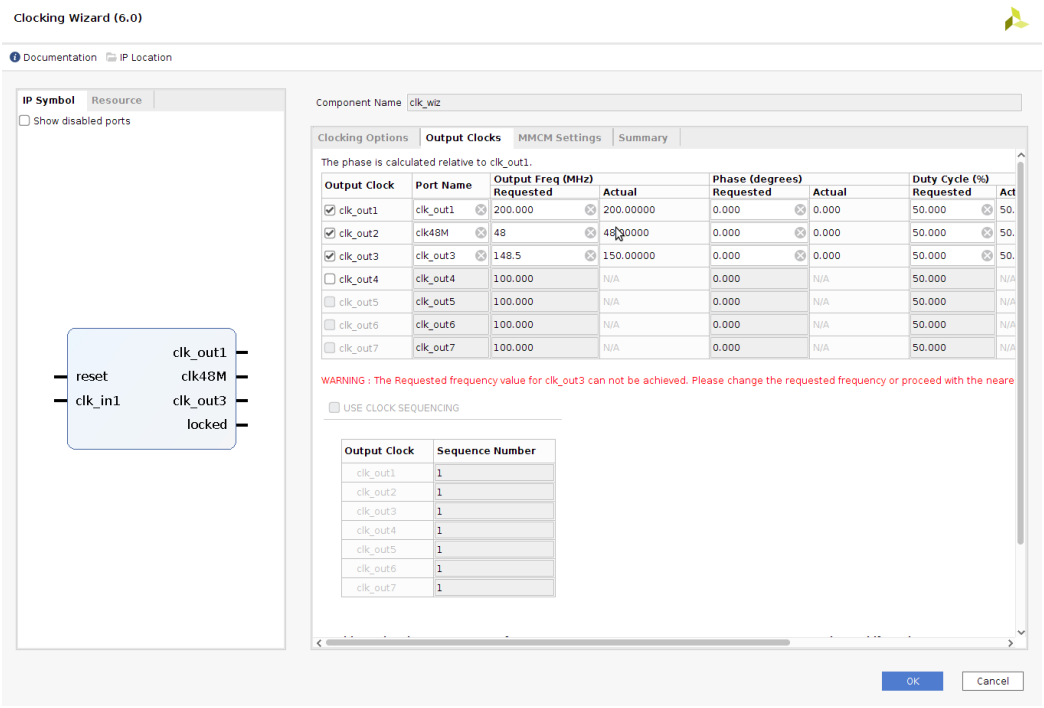


Figure 17. Clocking architecture

6. Double click on the capture pipeline (see Figure 18). This block contains the MIPI input IP, the video processing subsystem and the frame write buffer. This enables the image frames to be stored and accessed by the Zynq PS DDR.

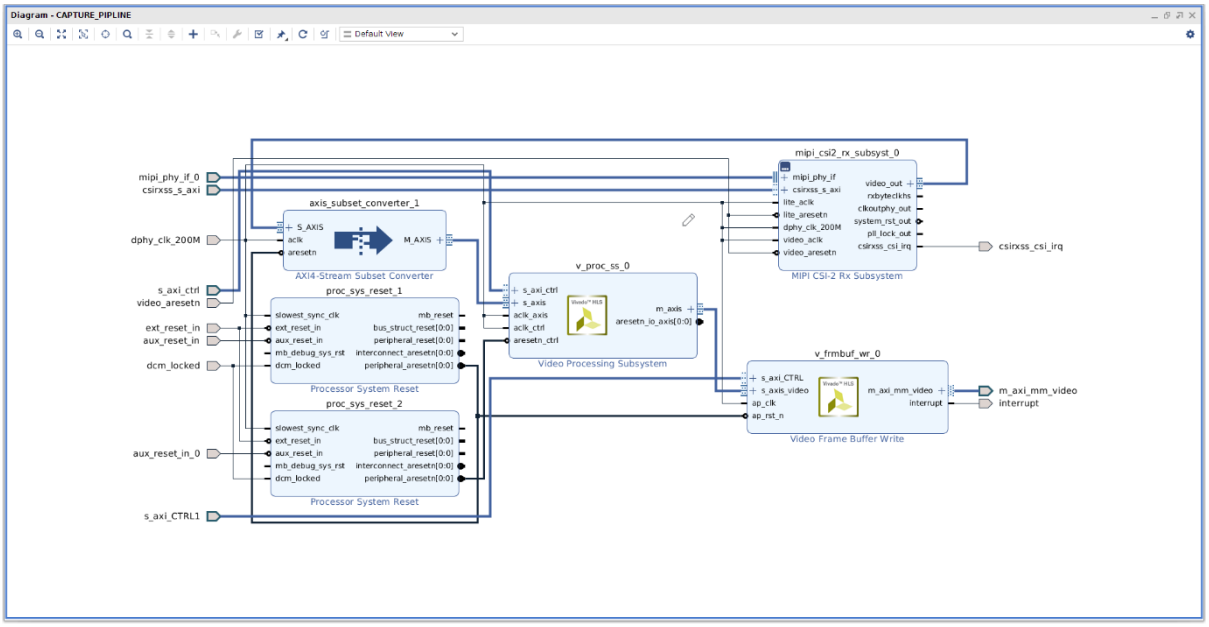


Figure 18. Capture pipeline

7. Examine the configuration of the MIPI IP core and add in 896 Mbps for the line rate (see Figure 19).

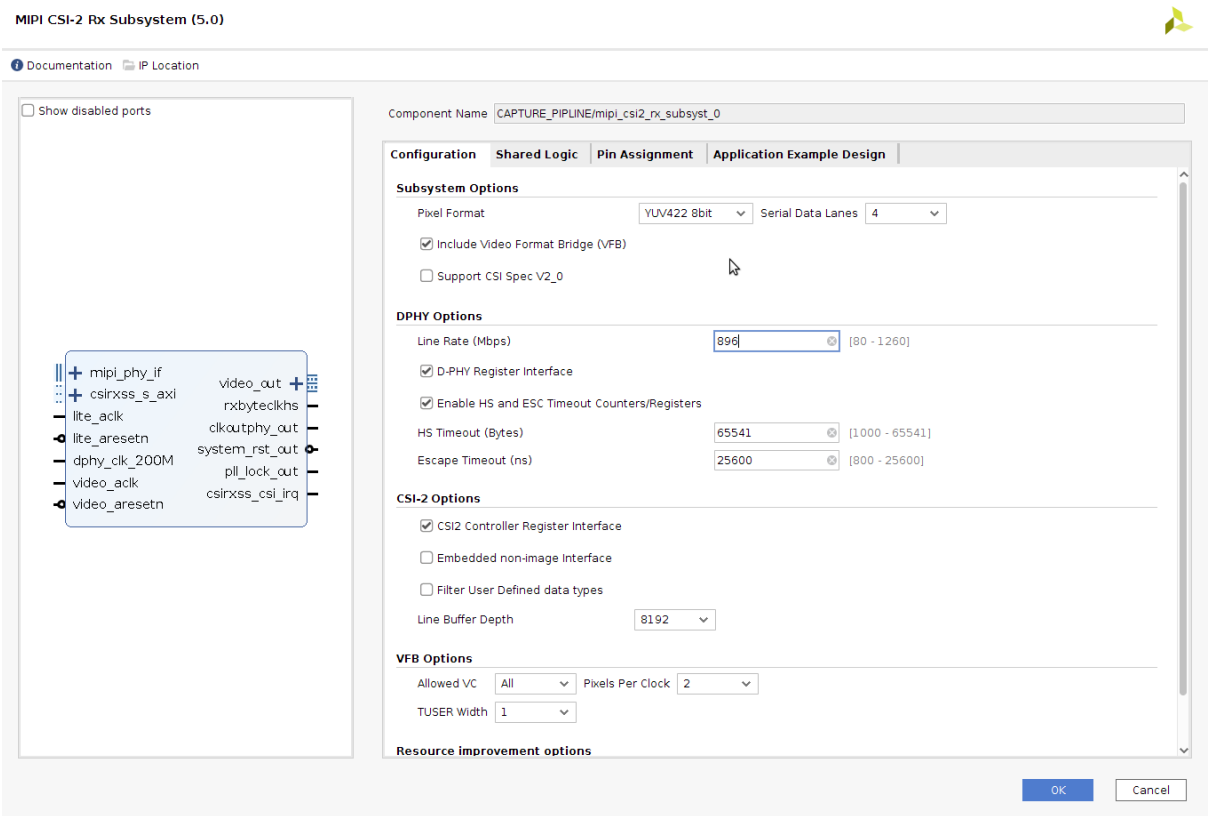


Figure 19. MIPI IP configuration

8. Examine the Live Video Display Port (DP) block (see Figure 20). The output video path is through the live video DP output provided by the Zynq ZU3EG. To access this, the frame is read out of the processing system DDR memory and converted from an AXI Stream into a parallel video (pixel, HSync, VSync). This parallel video is timed by the video timing controller.

To demonstrate the capabilities of the image processing in programmable logic, a test pattern generator is also used along with the on-screen display IP block.

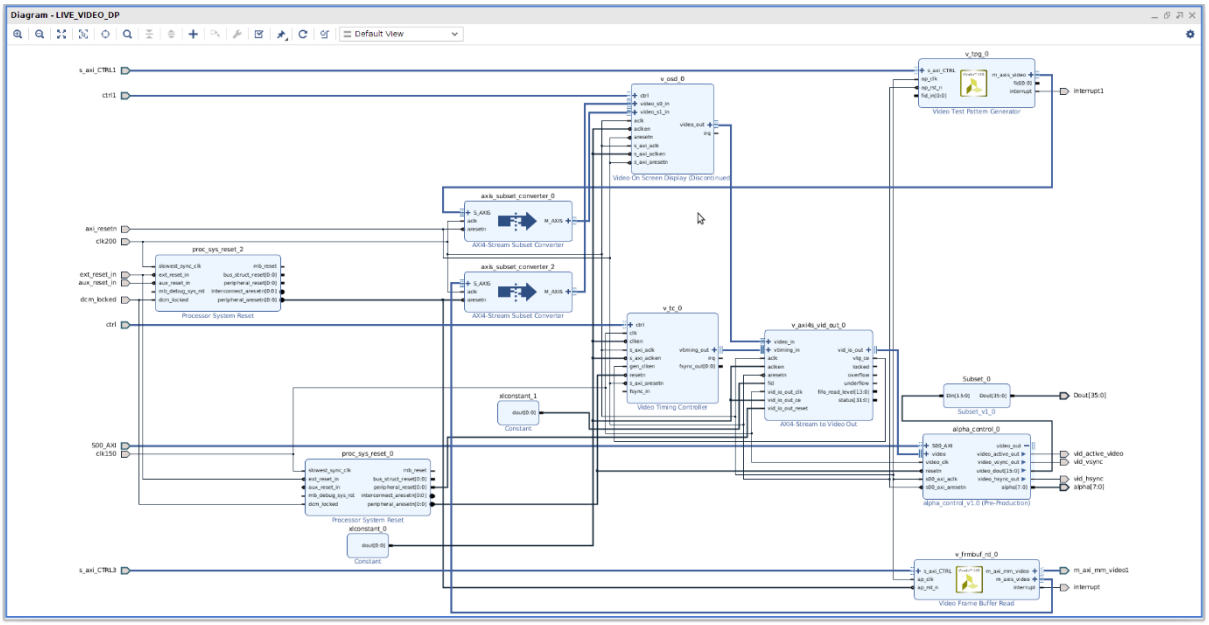


Figure 20. Live video DP block

9. Examine the Zynq block (see Figure 21). This element contains the configuration of processing system in the ZU3EG MPSoC.

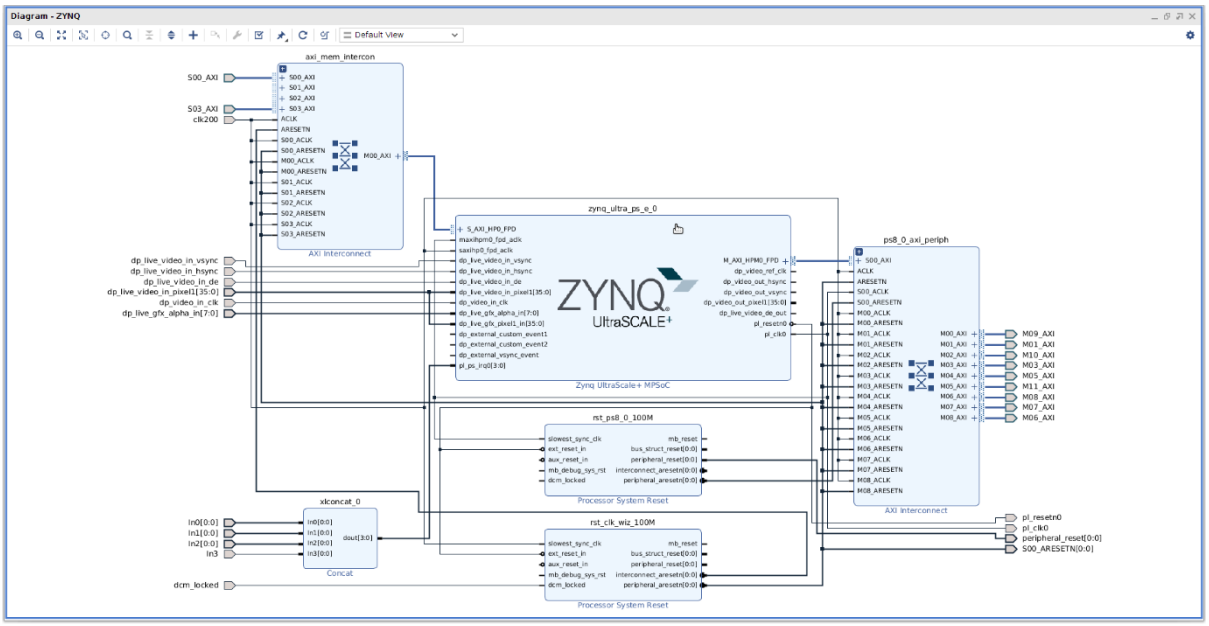
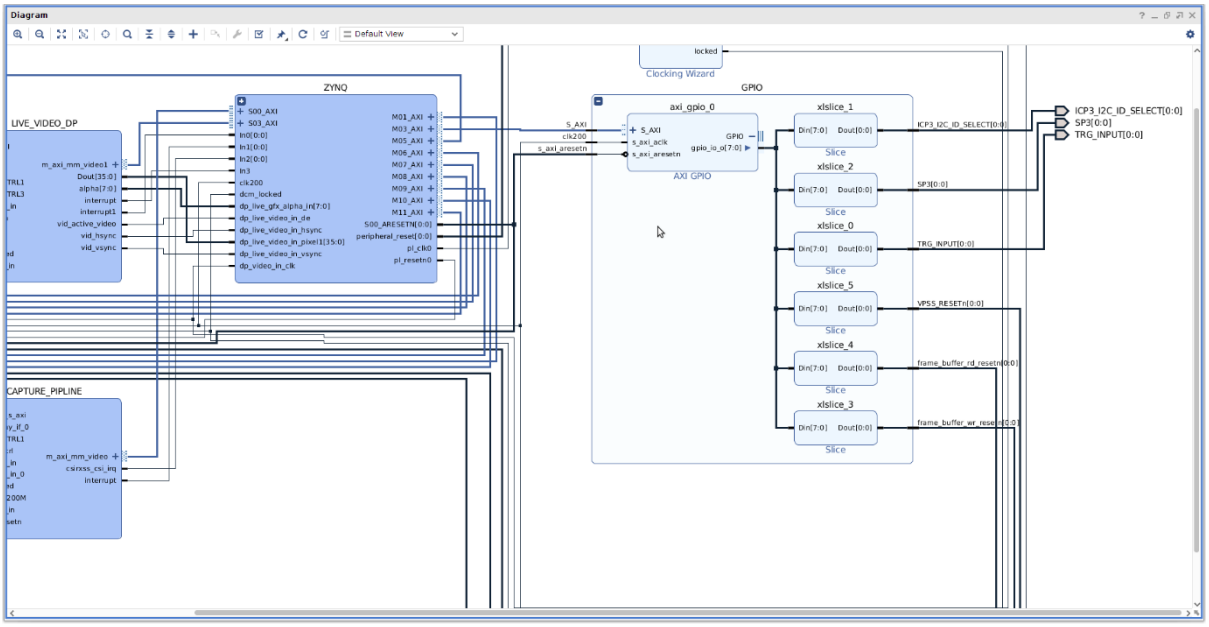
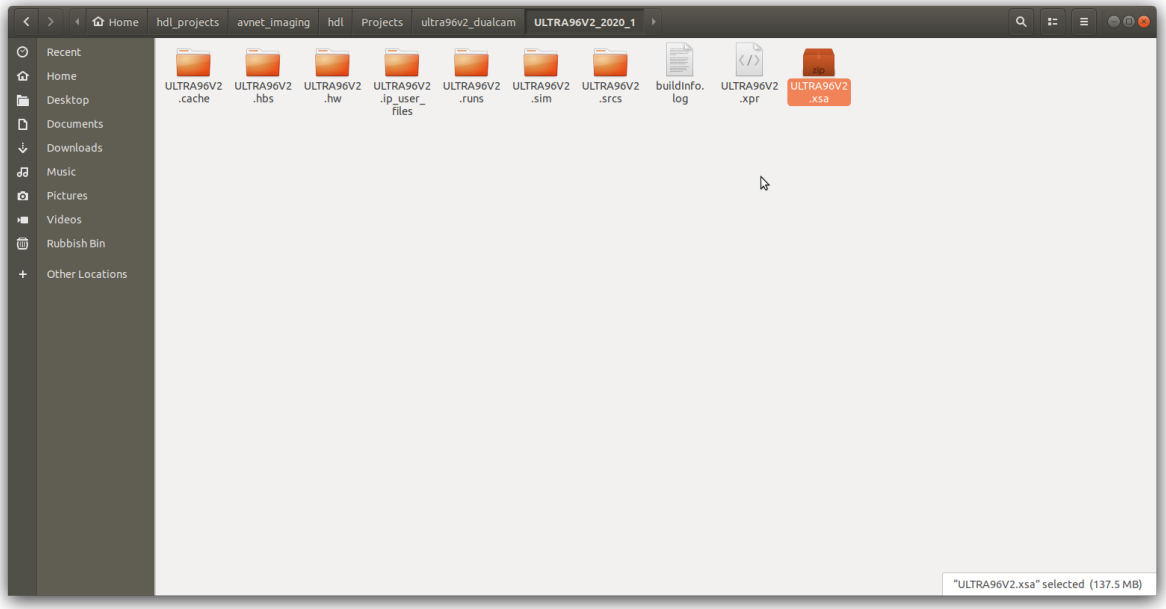


Figure 21. The processing system block

10. Examine the GPIO block. This block slices a GPIO bus to provide individual reset and GPIO as required by the design.



11. Close Vivado. Open a file browser and examine the project directory. There is a file named ULTRA96V2.xsa and this is the Xilinx Shell Archive that we will be using in the next application note to customize the PetaLinux operating system for the design created in Vivado.



Conclusion

This project shows how you can quickly and easily create the hardware design for a complex imaging system using Xilinx IP and Avnet ready-to-go build scripts, which enable you to hit the ground running in your application development.

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