User's Manual

RZ/G3S Group

Overview for User's Manual: Hardware

Renesas Microprocessor
RZ Family / RZ/G Series

arm

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

1. Overview

1.1 Introduction

This LSI is a single-chip microprocessor that includes a single Arm® Cortex®-A55 core, which operates at speeds of up to 1.1GHz and two Cortex®-M33 250MHz cores. One Cortex®-M33 has FPU function. This LSI includes a 32-Kbyte L1 instruction cache, a 32-Kbyte L1 data cache, and a 256-Kbyte L3 cache. The following are the features of this LSI.

- RZ/G3S
  - 1.1 GHz Arm® Cortex®-A55 MPCore
  - Two 250 MHz Arm® Cortex®-M33 cores (One Cortex®-M33 has FPU function)
  - Memory controller for DDR4-1600 / LPDDR4-1600 with 16 bits
  - Octa-Flash/Octa-RAM interface
  - USB2.0 host / function interface
  - Gigabit Ethernet interface
  - SD/MMC host interface
  - CAN interface
  - Sound interface
  - On The Fly Decryption / Encryption
  - Tamper Detection
  - PCI Express Gen 2.0 interface (option)

NOTE

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1.2 List of Specifications

1.2.1 CPU Core

Item	Description
System CPU Cortex-A55	• Arm Cortex-A55 Single Core 1.1 GHz • L1 I-cache: 32 Kbytes (Parity) / D-cache : 32 Kbytes (ECC) • L2 cache: Not included • L3 cache: 256 Kbytes (ECC) • NEON™ / FPU supported • Cryptographic Extension supported • Arm® v8.2-A architecture
System CPU Cortex-M33	• Arm Cortex-M33 Processor 250 MHz × 2 cores • Security Extension supported • Floating Extension supported*1 • Arm® v8-M architecture
Boot	• Bootable CPU: Cortex-A55, Cortex-M33*4 • Boot device: Boot Mode 0: Booting from eSD Boot Mode 1: Booting from eMMC Boot Mode 2: Booting from a serial flash memory (Single / Quad /Octal)*3 Boot Mode 3: Booting from SCIF download • Boot device voltage: 1.8 V*2, 3.3 V
Debug Interface	• Arm® CoreSight™ architecture • JTAG / SWD interface supported • ETF 16 Kbytes for program flow trace (each cluster) • JTAG Disable supported

Note 1. One core supports Floating Extension

Note 2. 1.8 V is supported in booting from eMMC and serial flash memory.

Note 3. A serial flash memory (Octal) is supported when Boot device voltage is 1.8 V.

Note 4. Cortex-M33 booting is supported from a serial flash memory and SCIF download.

1.2.2 CPU Peripheral

Item	Description
Clock Pulse Generator (CPG)	• Generates the clocks from external clock (EXCLK 24 MHz). Maximum Arm Cortex-A55 clock: 1.1 GHz Maximum Arm Cortex-M33 clock: 250 MHz Maximum DDR clock: 800 MHz (DDR4-1600 / LPDDR4-1600) Maximum AXI-bus clock: 200 MHz Maximum APB-bus clock: 100 MHz • SSC (Spread Spectrum Clock) supported
Direct Memory Access Controller (DMAC)	• 2 modules, 16 channels per module • Transfer request: On-chip peripheral request / auto request (software trigger) • A specific DMA transfer interval can be specified to adjust the bus occupancy. • LINK mode (DMA transfer under descriptor control) supported • Transfer information can be automatically reloaded
Interrupt Controller	• Arm® CoreLink™ Generic Interrupt Controller (GIC-600) for Arm Cortex-A55 • Nested Vectored Interrupt Controller (NVIC) for Arm Cortex-M33 • External Interrupt pins (NMI, IRQ7 to IRQ0, TINT31-0) • On-chip peripheral Interrupts: Priority level set for each module
Message Handling Unit (MHU)	• Message handling function between Arm Cortex-A55 and Arm Cortex-M33 • Assert interrupt to inform message and response from/to Arm Cortex-A55, Cortex-M33
General-purpose I/O (GPIO)	• General-purpose I/O ports
Thermal Sensor Unit (TSU)	• 1 channel

1.2.3 Internal Memory

Item	Description
On-chip RAM	• RAM of 1 Mbytes (ECC)

1.2.4 External Memory Interface

Item	Description
External Bus Controller for DDR4 / LPDDR4 SDRAM (DDR)	• Support DDR4-1600 / LPDDR4-1600 • Bus Width: 16-bit • In line ECC supported (Support error detection interrupt) • Memory Size: Up to 4 Gbytes (DDR4), 1 Gbytes (LPDDR4) • Auto Refresh / Self Refresh supported • On-The-Fly Decryption / Encryption supported
eXpanded Serial Peripheral Interface (xSPI)	• 1 channel • Up to 2 serial flash memories can be connected • Connectable with 2 Quad-SPI flash memories • Connectable with 2 Octal-SPI flash memories • Connectable with 2 Octal-RAMs • External address space read mode (built-in read cache) • SPI operation mode • Maximum Clock Frequency: 66 MHz (Single-SPI / Quad-SPI, SDR, 1.8 V / 3.3 V), 133 MHz (Octal-SPI / OctaFlash / OctaRAM, DDR, 1.8 V) • On-The-Fly Decryption / Encryption supported
Octa Memory Controller	• Macronix Serial Multi I/O (MXSMIO®) Octa Peripheral Interface (OPI) for high-end consumer applications is supported. • One each of an OctaFlash device and an OctaRAM device compliant with the OPI specifications are connectable. • A chip select signal is assigned to each memory device (OM_CS0#: OctaFlash; OM_CS1#: OctaRAM). • Supported device interfaces SPI: Serial peripheral interface (OctaFlash, SPI mode) SOPI: Single Octa I/O (8 bits) (OctaFlash, single data rate) DOPI: Double Octa I/O (8 bits) (OctaFlash and OctaRAM, double data rate) • On-The-Fly Decryption / Encryption supported
SD Card Host Interface / Multimedia Card Interface (SD/MMC)	• 3 channels • Channel 0 supports SDHI / e-MMC (boot supported) • Channel 1 and 2 support SDHI (Channel 1: Dedicated pin, Channel 2: Multiplexed pin, 3.3 V only) • SD memory I/O card interface (1-bit/4-bit SD bus) • SD, SDHC and SDXC SD memory card access supported • Compliant with SD 3.0 • Default, high-speed, UHS-I/SDR50, SDR104 transfer modes supported • Error check function: CRC7 (Command/response), CRC16 (Data) • Card detection function, write protect supported • MMC interface (1-bit/4-bit/8-bit MMC bus) • e-MMC device access supported • Compliant with eMMC 4.51 • High-speed, HS200 transfer modes supported (SD clock (SD_CLK) frequency: Up to 125 MHz)

1.2.5 Sound Interface

Item	Description
Serial Sound Interface (SSI)	• 4 channels bidirectional serial transfer • 2 external clock sources available • Full Duplex communication • Support of I2S / Monaural / TDM audio formats • Support of master and slave functions • Generation of programmable word clock and bit clock • Multi-channel formats • Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support of 32-stage FIFO for transmission and reception • Support of LR-clock continue function in which the LR-clock signal is not stopped
Pulse Density Modulated (PDM) Interface	• 3 channels • Capable of filtering 1-bit digital input data PDM_DATn (n = 0,..,2) and converting them into 20-bit or 16-bit digital data. • Support of stereo microphone (L/R sampling by rising/falling clock edge). • Support of sound activity detector. • Support of programmable filters: 4th order sinc filter, high-pass filter (for suppression of DC bias), correction filter (for sinc passband distortion), half-band decimation filter (for aliasing distortion). • Internal buffer: Capable of storing voice data during low power mode
SPDIF	• Supports the IEC 60958 standard (stereo and consumer use modes only). • Supports sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz. • Supports audio word sizes of 16 to 24 bits per sample. • Biphase mark encoding. • Double buffered data. • Parity encoded serial data. • Simultaneous transmit and receive • Receiver autodetects IEC 61937 compressed mode data
Sampling Rate Converter (SRC)	• 1 channel • Data format: 16-bit (stereo / monaural) • Sampling Rate Input: Selectable from 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz Output: Selectable from 8 kHz*, 16 kHz*, 32 kHz, 44.1 kHz, 48 kHz (*: can select in 44.1 kHz input mode) • SNR: More than or equal to 80 dB

1.2.6 Storage and Network

Item	Description
USB2.0 Host / Function (USB)	• 2 channels (ch0: Host-Function ch1: Host only) • Compliance with USB2.0 • Supports On-The-Go (OTG) Function • Supports Battery Charging Function • Internal dedicated DMA
Gigabit Ethernet Interface (GbE)	• 2 channels • Supports transfer at 1000 Mbps and 100 Mbps, 10 Mbps • Supports filtering of Ethernet frames • Supports interface conforming to IEEE802.3 PHY RGMII (Reduced Gigabit Media Independent Interface) • Supports interface conforming to IEEE802.3 PHY MII (Media Independent Interface)
Controller Area Network Interface (CAN)	• 2 channels • CAN-FD ISO 11898-1 (CD2015) compliant • Up to 1 Mbps for arbitration phase and up to 8 Mbps for data phase • Message buffer – Up to 64 × 2-channel receive message buffer: Shared among all channels – 16 transmit message buffers per channel
PCI Express Gen2 (option)	• PCI Express Base Specification 4.0 compliant • PCI Express Gen1(2.5[GT/s])/Gen2(5.0[GT/s]) • Root Complex, Type1 Configuration Register • Lane implementation ×1 • Support Polarity inversion • Maximum data payload of 256 bytes, Maximum read request size 512 bytes • Not support for Virtual channels (support VC0 only) • Number of outstanding 1-8 • Dynamic control of speed/width up/down configuration • Not support for Clock Power Management (not support P1.CPM, P2.CPM) • Power Management (ASPM L1-Substate Support (Support Power Down Sequence only)) • Error handling/logging (AER Support) • Replay FIFO with ECC • Internal Memory without Parity • Number of Support Functions 1

1.2.7 Timer

Item	Description
Multi-function Timer Pulse Unit 3 (MTU3a)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Module clock frequency: 100 MHz • Maximum 28 lines of pulse inputs/outputs and 3 lines of pulse inputs • 14 types of count clocks selectable • Input capture function • 39 outputs compare and input capture registers • Counter clear operation (Simultaneous counter clearing by Compare match or Input capture is available) • Simultaneous writing to multiple timer counters (TCNT) • Synchronous input/output of each register due to synchronous operation of the counter • Buffered operation • Cascade-connected operation • 43 types of interrupt sources • Automatic transfer of register data • Pulse output modes Toggle, PWM, complementary PWM, and reset-synchronized PWM modes • Synchronization of multiple counters • Phase counting mode – 16-bit mode (channel 1 and 2) – 32-bit mode (channel 1 and 2) • Counter function of dead time compensation • Digital filter functions for the input capture and external count clock pin
Port Output Enable 3 (POE3)	• Control of the high-impedance state of the MTU3a waveform output pins • Activation with four input pins • Activation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Activation by register write • Additional programming of output control target pins is possible.
General PWM Timer (GPT)	• 32 bits × 8 channels • Counting up or down (sawtooth wave), counting up and down (triangular wave) selectable for all channels • Independent selectable for each channel • 2 input/output pins per channel • 2 output compare / input capture registers per channel • For the 2 output compare / input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Generation of dead times in PWM operation • Synchronous start / stop / clear of counters on arbitrary channels • Starting, stopping, and clearing up/down counters in response to a maximum of eight events • Starting, stopping, and clearing up/down counters in response to input level comparison • Starting, stopping, and clearing up/down counters in response to a maximum of four external triggers • Output pin invalidation functions due to dead time error or detection of short circuit between output pins • Digital filter functions for the input capture and external trigger pins
Port Output Enable for GPT (POEG)	• Output prohibition control of the GPT waveform output pin • Activation with up to four input pins • Activation by dead time error detection or output short detection • Activation by register write

Item	Description
Watchdog Timer (WDT)	• 3 channels • A counter overflow can reset the LSI • CPU parity error can reset the LSI
General Timer (GTM)	• 32 bits × 8 channels • Two operating modes – Interval timer mode – Free-running comparison mode
RTC	• Clock sources: 32 kHz clock (RTXIN) • Count mode: Calendar count mode / binary count mode • Interrupt sources: Alarm interrupt, periodic interrupt and carry interrupt • Time capture function

1.2.8 Peripheral Module

Item	Description
I2C Bus Interface (I2C)	• 4 channels (ch0,1 = Dedicated pin, ch2,3 = Multiplexed pin) • Master mode and slave mode supported • Support for 7-bit and 10-bit slave address formats • Support for multi-master operation • Timeout detection
I3C Bus Interface (I3C)	• 1 channel • Master (Main Master/Secondary Master) mode and Slave mode selectable • SDR (I3C Single Data Rate) Mode – Private Message – Broadcast Message (Common Command Code) – Direct Message (Common Command Code) • Legacy I2C Message – Fast-mode (Fm): Up to 400 kbit/s – Fast-mode Plus (Fm+): Up to 1 Mbit/s • Slave Interrupt Request • Master Ship Request (Secondary Master only) • Support for 7-bit slave address formats • Synchronous Timing Control – Sync Mode: Synchronous Basic Mode • Asynchronous Timing Control – Async Mode 0: Asynchronous Basic Mode – Async Mode 1: Asynchronous Advanced Mode • Error Detection
Serial Communication Interface with FIFO (SCIFA)	• 6 channels • Clock synchronous mode or asynchronous mode selectable • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud rate generator • Separate 16-byte FIFO registers for transmission and reception • Modem control function (channel 0, 1 and 2 in asynchronous mode)
Serial Communication Interface (SCIg)	• 2 channels • Clock synchronous mode, asynchronous mode, or smart card interface mode is selectable • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud rate generator • LSB first / MSB first selectable • Modem control function • Encoding and decoding of IrDA communications waveforms in accord with version 1.0 of the IrDA standard (on channel 0)
Renesas Serial Peripheral Interface (RSPI)	• 5 channels • SPI operation • Master mode and slave mode supported • Programmable bit length, clock polarity, clock phase can be selected • Consecutive transfers • LSB first / MSB first selectable

1.2.9 Security

Item	Description
Renesas Security IP (RSIP-E01B) [option]	• Security algorism – Common key encryption: AES (compliant with NIST FIPS PUB 197) – Non-common key encryption: RSA, ECC • Other features – TRNG (true-random number generator) – Hash value generation: SHA-1, SHA-224, SHA-256 – Support of Unique ID
One Time Programmable memory (OTP)	• A nonvolatile memory that can be written only once • Security setting, authentication setting are possible • Support one time read function (128 bytes)
Battery Backup Function	• Realtime clock • Backup register • Tamper detection

1.2.10 Analog

Item	Description
A/D Converter (ADC)	• 8 channels • Resolution: 12-bit • Input Range: 0 V to 1.8 V • Conversion Time: 1.0 µs • Operation Mode: Select mode / scan mode • Conversion Mode: Single mode / repeat mode • Condition for A/D conversion start – Software trigger – Asynchronous trigger: External trigger supported – Synchronous trigger: MTU and PWM timer

1.2.11 Others

Item	Description
Boundary Scan	• Boundary scan based on IEEE 1149.1 via JTAG interface is supported. Note that some module pins are not available on this boundary scan.

1.2.12 Power Supply Voltage

Item	Description
Power supply voltage	• VBATT_VDD: 1.65 to 1.95 V • VDD, PLL16_AVDD, PLL23_AVDD, PLL4_AVDD: 0.905 to 0.99 V • PVDD33: 3.0 to 3.6 V • PVDD18, ADC_AVDD18, OTP_AVDD18: 1.65 to 1.95 V • JTAG_PVDD: 1.65 to 1.95 V • XSPI_PVDD: 1.65 to 1.95 V / 3.0 to 3.6 V • I3C_PVDD: 1.1 to 1.3 V / 1.65 to 1.95 V • VDD_ISO, PCIE_VDD09: 0.905 to 0.99 V • SDn_PVDD (n = 0, 1): 1.65 to 1.95 V / 3.0 to 3.6 V • PVDD182533_n (n = 0, 1): 1.65 to 1.95 V / 2.3 to 2.7 V / 3.0 to 3.6 V • USB_VDD33: 3.0 to 3.6 V • USB_AVDD18, USB_VDD18, PCIE_VDD18: 1.65 to 1.95 V • DDR_VAA: 1.65 to 1.95 V • DDR_VDDQ: 1.06 to 1.17 V(LPDDR4) / 1.14 to 1.26 V (DDR4)

1.2.13 Temperature Range

Item	Description
Temperature range	• T_a: −40°C to +85°C*1 • T_j: −40°C to +125°C

Note 1. If wider temp is required than this range, use case has to be investigated.

1.2.14 Quality Level

Item	Description
Quality level	• Industrial usage, etc.

1.2.15 Package

Item	Description
Package	• PBGA, 13-mm square, 0.5mm pitch (w/o PCIe) • PBGA, 14-mm square, 0.5mm pitch (w/ PCIe)

1.3 Product Lineup

Table 1.1 Product Lineup

Group	Package	Part Number	CPU	Security	PCIe
RZ/G3S	14 mm BGA	R9A08G045S37GBG	1× Cortex-A55, 2× Cortex-M33	Available	Available
		R9A08G045S17GBG	1× Cortex-A55, 1× Cortex-M33		
		R9A08G045S33GBG	1× Cortex-A55, 2× Cortex-M33	Not supported	
		R9A08G045S13GBG	1× Cortex-A55, 1× Cortex-M33		
	13 mm BGA	R9A08G045S35GBG	1× Cortex-A55, 2× Cortex-M33	Available	Not supported
		R9A08G045S15GBG	1× Cortex-A55, 1× Cortex-M33		
		R9A08G045S31GBG	1× Cortex-A55, 2× Cortex-M33	Not supported	
		R9A08G045S11GBG	1× Cortex-A55, 1× Cortex-M33		

1.4 Pin

This section describes the pins of this LSI.

1.4.1 Pin Assignment

Refer to another excel file for the “pin function list” about pin assignment of this LSI.

1.4.2 External Pins

Refer to another excel file for the “pin function list” about information of external pins of this LSI.

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