Low Power = Battery Life?
Low Power = System Saving!

Author: Martin Kellermann,
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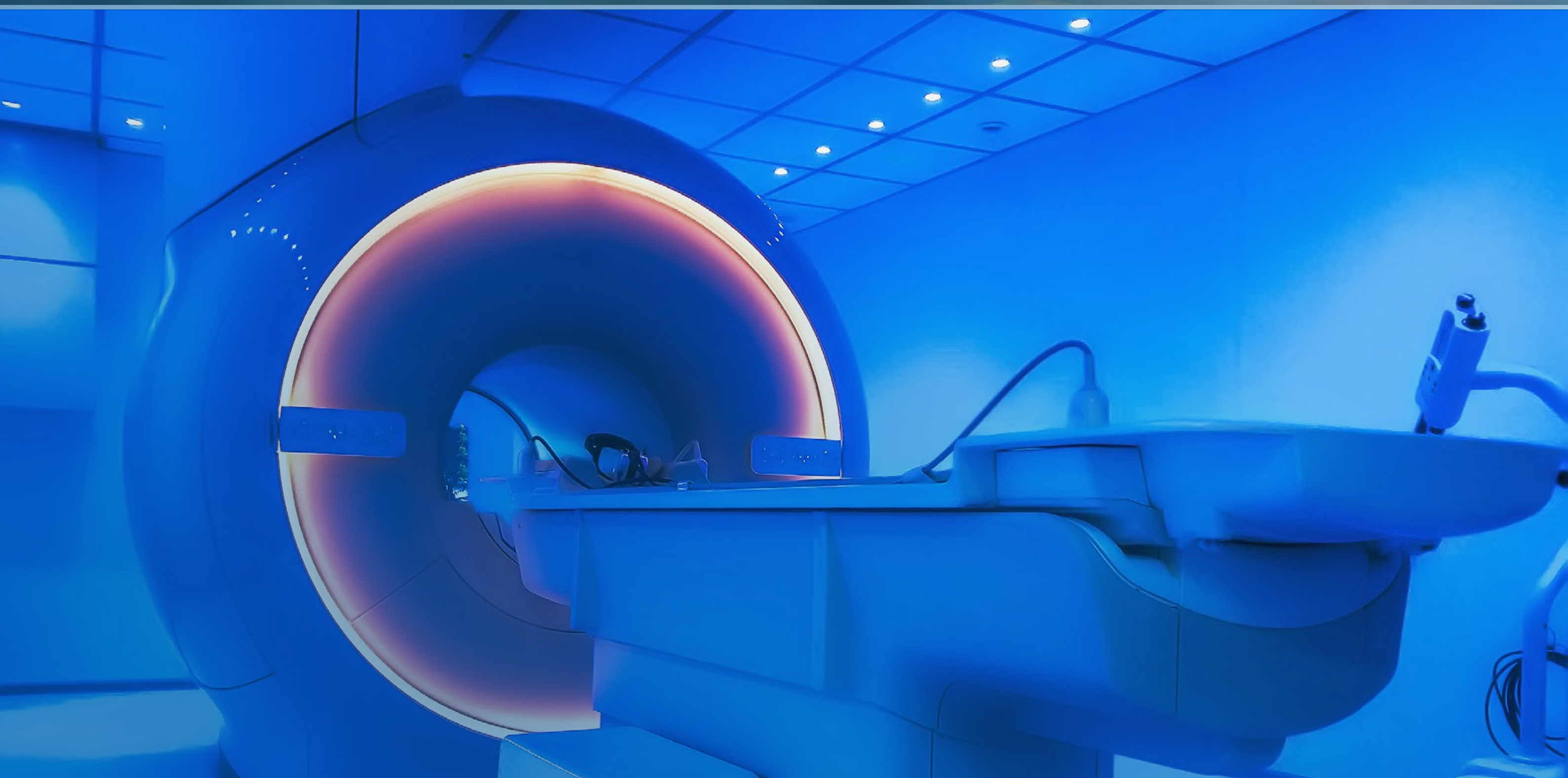

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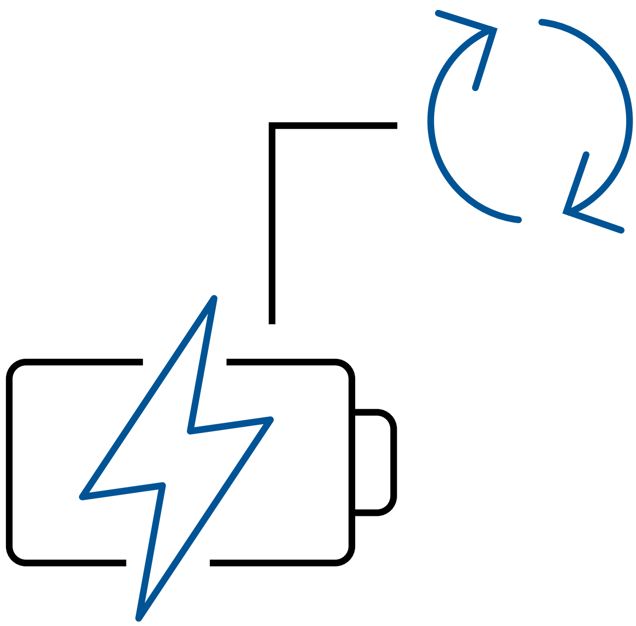
Power Consumption matters in all electronic systems, even if not immediately obviously. The total cost of ownership can be significantly reduced by using electronic devices with low power consumption.

Introduction

Have you ever been asked if your application should run on a component with lower power consumption? Either by someone in management or from a semiconductor vendor? Maybe you thought "my application is not battery powered" or you have other components in your application that are of much higher power consumption anyway and hence "low power" is not very relevant to you.

I invite you to think about that topic again from the perspective of total cost of ownership. You have very good chance of benefitting from lower power consumption in unexpected ways. We'll present how and discuss how high-power consuming non battery powered systems using a low power component like a PolarFire® Field Programmable Gate Array (FPGA) or PolarFire SoC could be beneficial and possibly reduce risk and save money.



Why Power Consumption Matters in all Systems

One common topic has emerged over the last years: the need for computational performance at a small power envelope. A part of this development is the move of FPGAs from glue logic into the center of the system. These computationally-efficient hardware architectures, with their inherent flexibility, allow users to tailor a hardware solutions to their requirements.
This flexibility can serve a wide range of applications, including automotive (production, not just prototyping), industrial, medical, networking, aviation, and Aerospace and defense, to name a few. Some example applications include motor control for electric drives, very-precisely-synchronized injection control on combustion engines, intelligent sensors like LiDAR or 4D RADAR and diagnostic medical equipment ranging from handheld ultrasound to large Magnetic Resonance Tomography (MRT) or X-ray.

The rise of available performance was driven by Moore's law; however, this also came at the cost of more energy in the digital circuits being directly converted into heat. Let us come back to the initial point of "my application is not battery-powered and hence power-consumption is not very relevant" in the light of computational operations driving up the temperature of the components:
If an electronic component has higher power consumption for a given task of operation, then it will also generate more heat. With that, more cooling could be required.

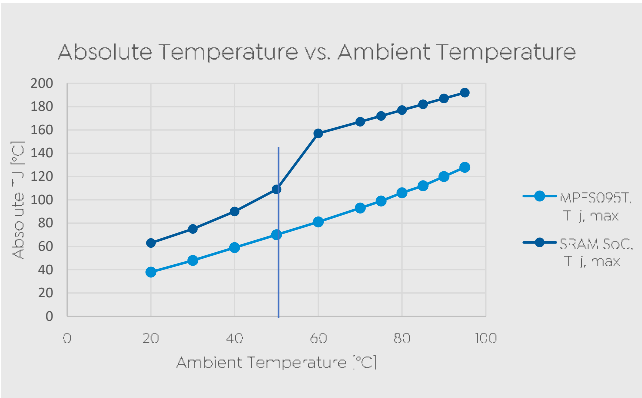
What are your options for cooling? Heat-sinks, fans, even water-cooling? What do all these have in common?

They are additional components requiring additional effort in design and production and possibly add sources of potential failure. Fans, as an example, are notorious for failing. By choosing architectures and devices with a strong focus on low power and subsequent lower cooling needs you can potentially reduce your system cost and system effort. A simplified and reduced cooling system can decrease the physical size of the equipment, lower the material cost and allow you to build in smaller form factors, if desired. The system cost saved by simplifying a cooling system can be significant. Microchip estimates bill of material (BOM) cost savings as high as $1.50/Watt.

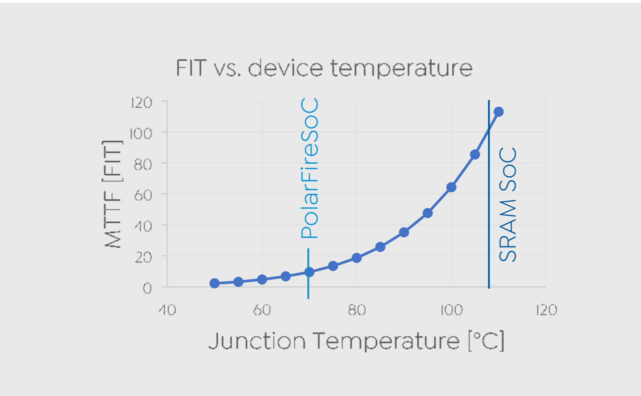
In a situation where an FPGA is sitting next to a separate power-hungry device in the system, where tens of Watts or even more are converted into heat and a large cooling system is likely required anyways, will the system design still benefit from lower power devices? Absolutely, yes!
Take a given cooling system that is designed for the high amount of heat generated by the other components. In this case, the FPGA is often simply cooled as a side component. In this example it is seen as "good enough" for the FPGA to stay within its specified temperature range. However, an FPGA with a lower self-heating can still be beneficial in the following ways:

- Its placement on the board may be easier as no major effort would be required for keeping it near the cooling system and within its temperature range
- By operating at a lower temperature, the FPGAs aging can also be reduced. The lower the temperature of the FPGA, the slower it ages and with that the mean time to failure (MTTF) is increased.

Is the MTTF and the accompanying FIT-rate (failure in time) really such a big deal? A common rule of thumb in the electronics industry is that a reduction of 10°C halves the FIT-rate of a semiconductor device. Not a big deal, you say? Let's put some numbers behind this.
Microchip implemented the same design on a Microchip PolarFire SoC and a competitive SRAM-based FPGA SoC. On both devices, a thermal sweep was performed using the vendor-specific power estimation tools with identical Theta Junction Ambient of 8.2°C/W and the resulting junction temperature of the devices recorded as follows:



At an ambient temperature of 50°C the junction temperature of the PolarFire SoC was 70°C. The SRAM-based SoC ended up at 109°C, already beyond the industrial temperature grade which we will ignore for a moment.
What effect does that temperature difference of nearly 40°C have for the likelihood of device-failure?
Using the Arrhenius High Temperature Over Lifetime (HTOL) [1] model with the assumption of equal test hours for both devices shows this (for simplicity we are plotting the FIT-rate versus junction-temperature):
PolarFire SoC has an MTTF of around 10 FIT. The SRAM-based SoC has around 107 FIT, a significant difference.



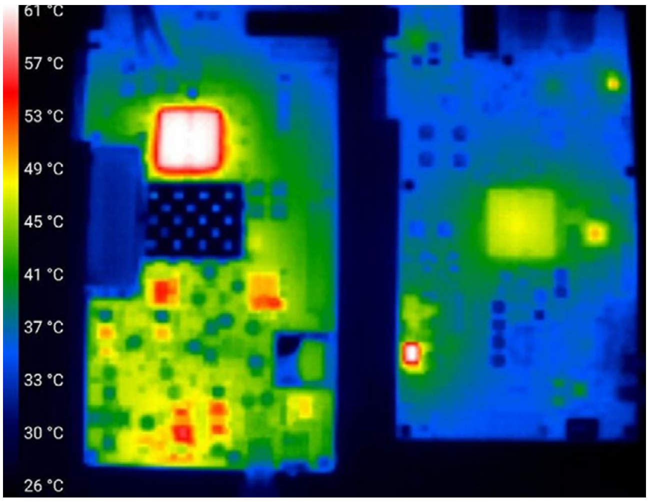
What does this mean?

First, 1 FIT is one failure in 10^9 hours, so one failure in approximately 114.000 years. 10 FIT is 10 failures in 10^9 hours so 10 failures in 114.000 years. With one device you would probably not really care. However, statistics apply here; more fielded devices will shorten the time until you can expect to see a failure. The following table shows how volume is affecting the number of failures one can expect in such a situation based on 10 FIT for PolarFire SoC and 107 FIT for the other SRAM-based SoC:

Result: keep the temperature of your components down to keep the number of field-failures down.

Speaking of field-failures: In the case of where you are building a design involving functional safety, failure rate is of even greater importance in your interactions with the notified bodies such as exida, TÜV or SGS-TÜV. Showing lower FIT rates of your system and its main electronic components, as an FPGA typically is, can ease the process of safety certification. For those of you wondering if the message of significantly lower power consumption of Microchip's FPGAs is true: yes, it is.

Microchip implemented several designs on both an MPF300-EVAL-KIT with a PolarFire MPF300T as the FPGA and a similarly-equipped board from another vendor. These test designs were loaded onto the boards and clocks, logic, on-chip RAM and transceivers were exercised in the same manner in both cases. After the temperatures had settled, a thermal camera was used to take a simultaneous reading of both boards and their main component as shown in the following image:



	PolarFire SoC			other SoC		
Fielded Devices	**Time be-tween failures [h]**	**Time be-tween failures [d]**	**Failures / year**	**Time be-tween failures [h**	**Time be-tween failures [d]**	**Failures / year**
10000	10000	416.7	0.9	935	39	9
100000	1000	42	9	93	4	91
1000000	100	4	91	9	0.4	913

The side-by-side comparison of the MPF300-EVAL-KIT (right) and the other vendor board (left) clearly shows the thermal advantage of the Microchip PolarFire FPGA. At room temperature of approximately 30°C the PolarFire device stayed around 45°C without any heat sink. The other device, with its passive heat sink, reached 60°C.

Conclusion

Paying attention to lower power consumption, even for systems that are not battery operated, can have significant impact on the “Big Three” things that developers typically care about.

All in all, Microchip FPGAs and SoCs are ideal candidates to build your low-power system and meet the “Big Three” needs of your projects. And, as shown, low power consumption is far more than battery life.

Details on the power comparison between various FPGAs are to be published in a separate article. Stay tuned!

Reduce risk

By choosing a Microchip FPGA or SoC you can simplify the system design by removing fans or complicated and expensive heat sinks. This can ease the development and reduce the risk in the project.

Save money

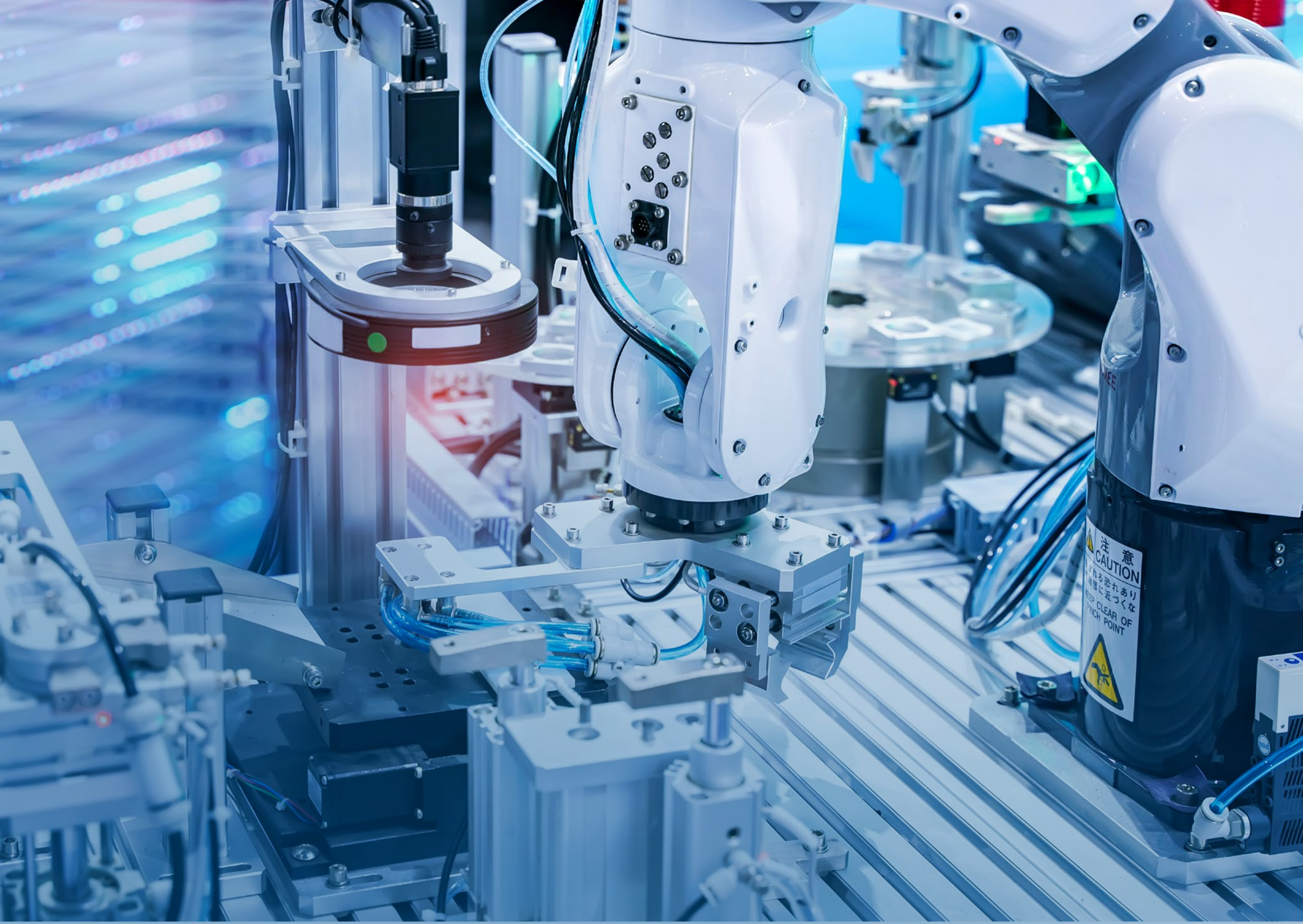
With a simpler system you typically have less components, and with that, less development time and shorter test time. This can be a strong money saver for you as a developer! Significant money can also be saved on fewer repairs or customer returns due to more reliable equipment in the field.

Make money

If you are working on a given power budget, you can also turn things around and add more features into your system as “features per Watt”. More features in the system can also mean more features that your customers may want and can lead to more revenue for you.

References

[1] https://www.microsemi.com/document-portal/doc_view/124041-calculating-reliability-using-fit-mttf-arrhenius-htol-model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CAUTION


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