Totem Pole PFC Layout Considerations

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Abstract

PCB layout plays an important role in power conversion. Magnetics and capacitors are typically switched on and off at a high frequency resulting in voltages and currents that are discontinuous and have sharp edges popularly referred to as high dv/dt and di/dt edges in the literature. Any parasitic inductance and capacitance in the PCB layout can cause noise being injected into various nodes due to these sharp edges prevalent in a power converter. These issues are particularly exacerbated in topologies that utilize Wide Bandgap (WBG) devices such as GaN and SiC. WBG devices, typically, have lower capacitances and switch at a faster rater further increasing the dv/dt and di/dt of various edges.

The goal of this whitepaper is to identify layout challenges within a totem pole power factor converter (TPFC) and illustrate a way to overcome some of those challenges. Since TPFC is typically paired up with WBG devices such as GaN, this whitepaper will pay particular attention to its idiosyncrasies. Further, TPFC operating both in Critical Conduction Mode (CrM) and Continuous Conduction Mode (CCM) are discussed encompassing both NCP1680 and NCP1681 product families.

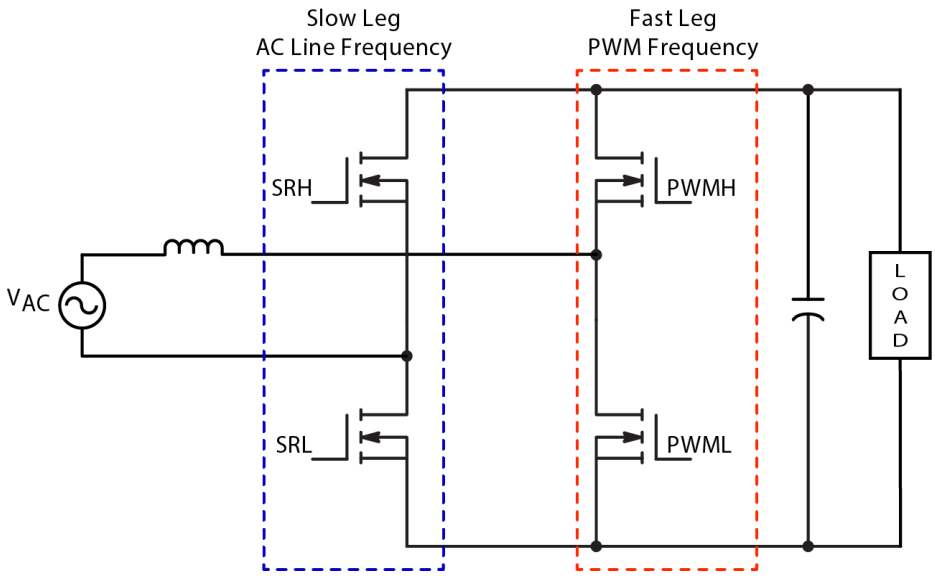

Figure 1. Simplified Totem Pole PFC Topology

Introduction

The Totem Pole PFC (TPFC) circuit is shown in Figure 1. The topology consists of two half−bridge configurations; one half bridge, commonly referred to as the “Fast Leg” switches at the PWM frequency and the other, commonly referred to as the “Slow Leg” switches at the AC line frequency. The fast leg switches perform the role of the switch and the diode in a classical boost PFC, that is, these switches function to regulate the output voltage and shape the input current to provide high power factor and low harmonic distortion. The slow leg switches perform the role of the diode bridge in a classical boost PFC. Active switches with low ON resistance are utilized instead of diodes, resulting in improved efficiency. Also, as will be described in the discussion below, the TPFC operates with only one slow leg and one fast leg device in the conduction path, whereas the conventional boost PFC operates with two bridge diodes and one active switch or boost diode in the conduction path. Fewer devices in the conduction path and active switches replacing bridge diodes allow the TPFC topology to achieve higher system efficiency and power density than the classical boost PFC.

Typical Application Schematics

Before delving into the details of the layout, it is important to look at the typical application schematic of TPFC operating in CrM (NCP1680 and CCM (NCP1681). NCP1680 employs constant on−time control with valley synchronized frequency foldback and therefore needs a simple current sensing scheme for current limit and zero current detection at turn−off the synchronous or (1−D) FET. Please refer to the datasheet for detailed operation.

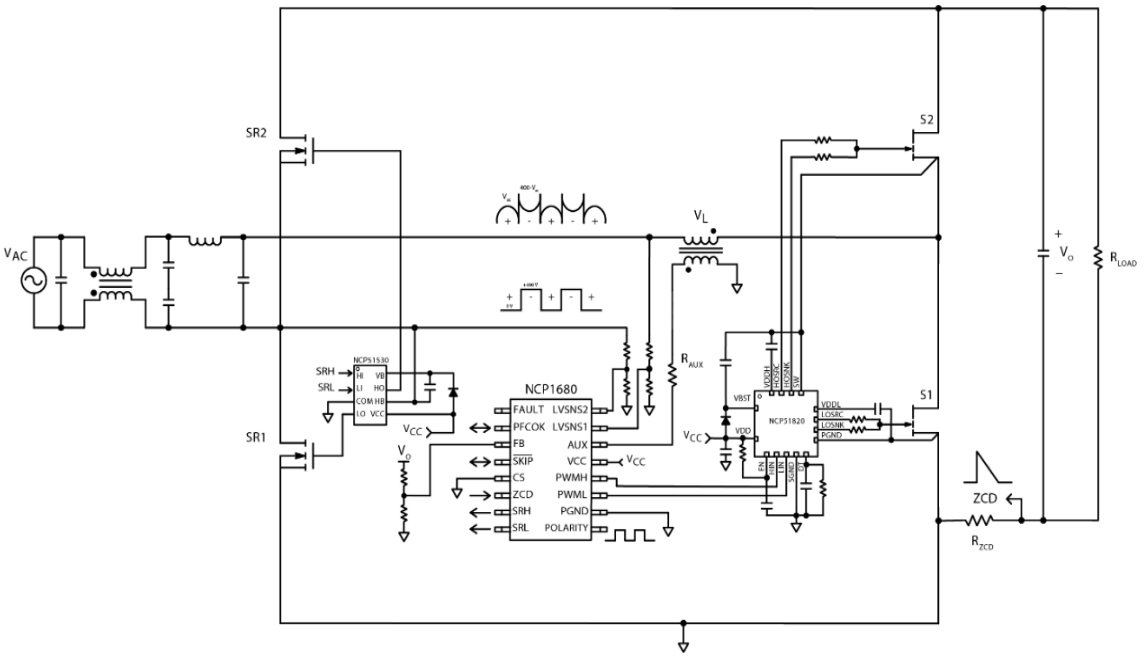

Figure 2. NCP1680 Typical Application Schematic

NCP1681 is suitable for high power converters from 300 W to 2.5+ kW. NCP1681 needs both inductor upslope and downslope information to implement average current mode control and hence employs current transformers in the high frequency leg as shown in Figure 3.

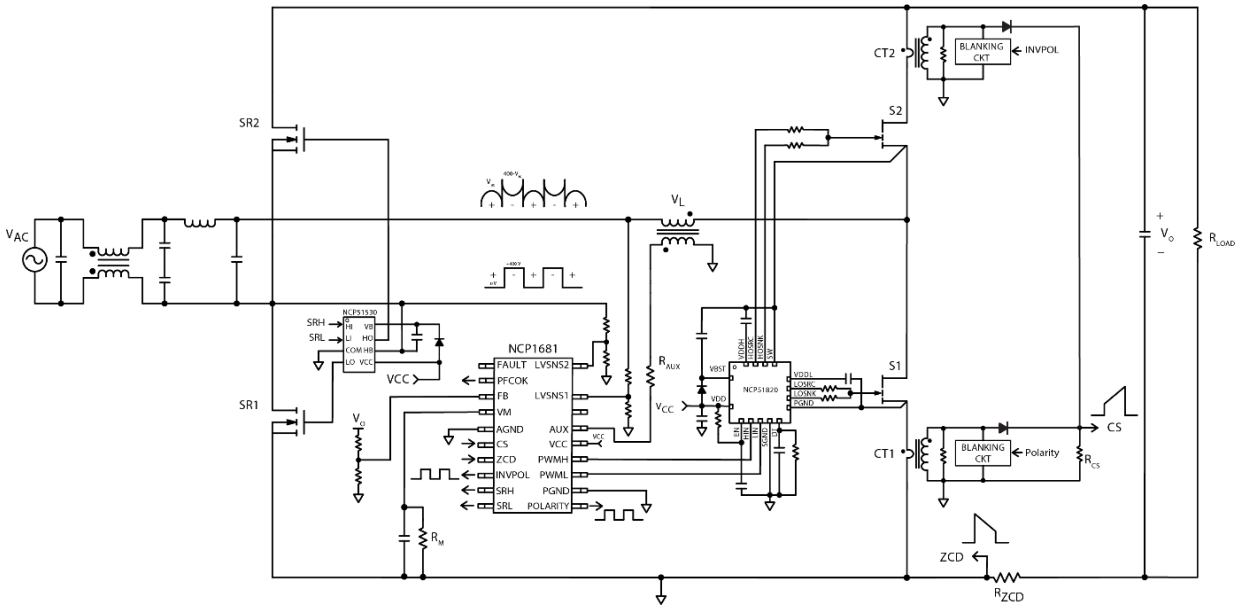

Figure 3. NCP1681 Typical Application Schematic

Part Placement

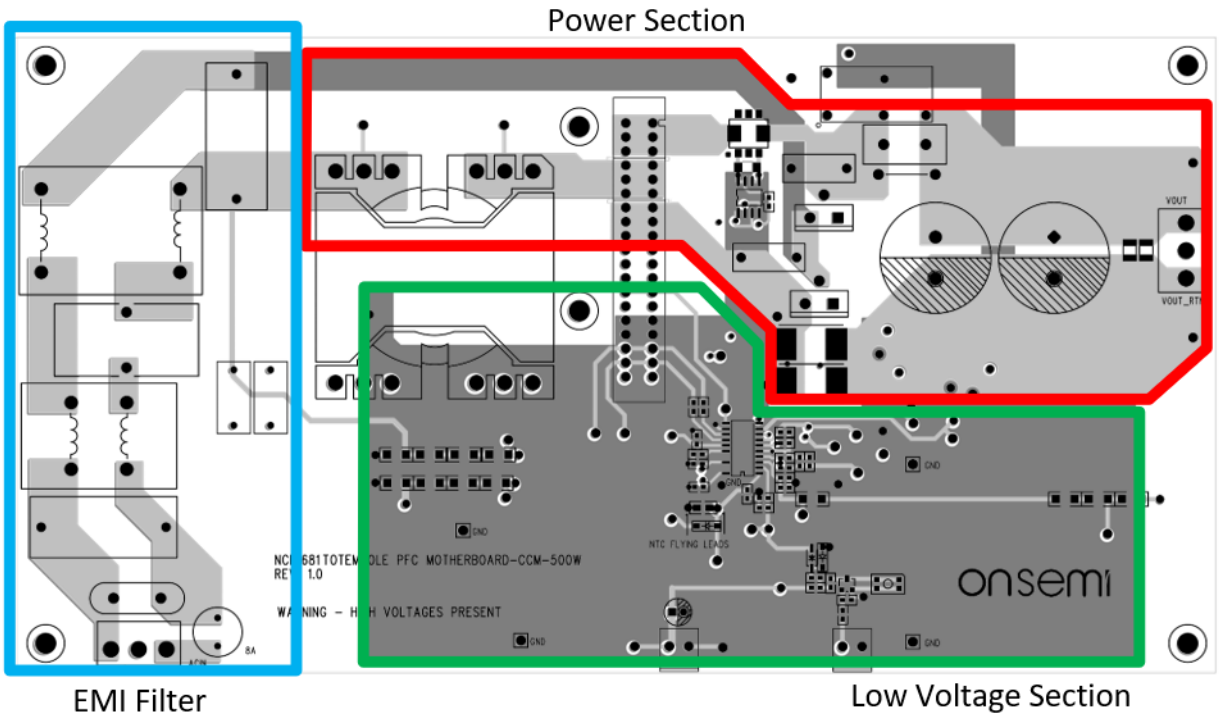

Figure 4. NCP1681 Motherboard Circuit Breakdown

The NCP1680/81 board can be separated into three sections: EMI filter, power train and low−voltage section. Each section has specific placement and routing needs.

1. Power Train

Power train encompasses all the components that process the power i.e., slow leg switches and its driver, inductor, and output capacitors. High frequency switches are part of the power train but are implemented in a daughter card so that various switch technologies and combinations can be tested easily.

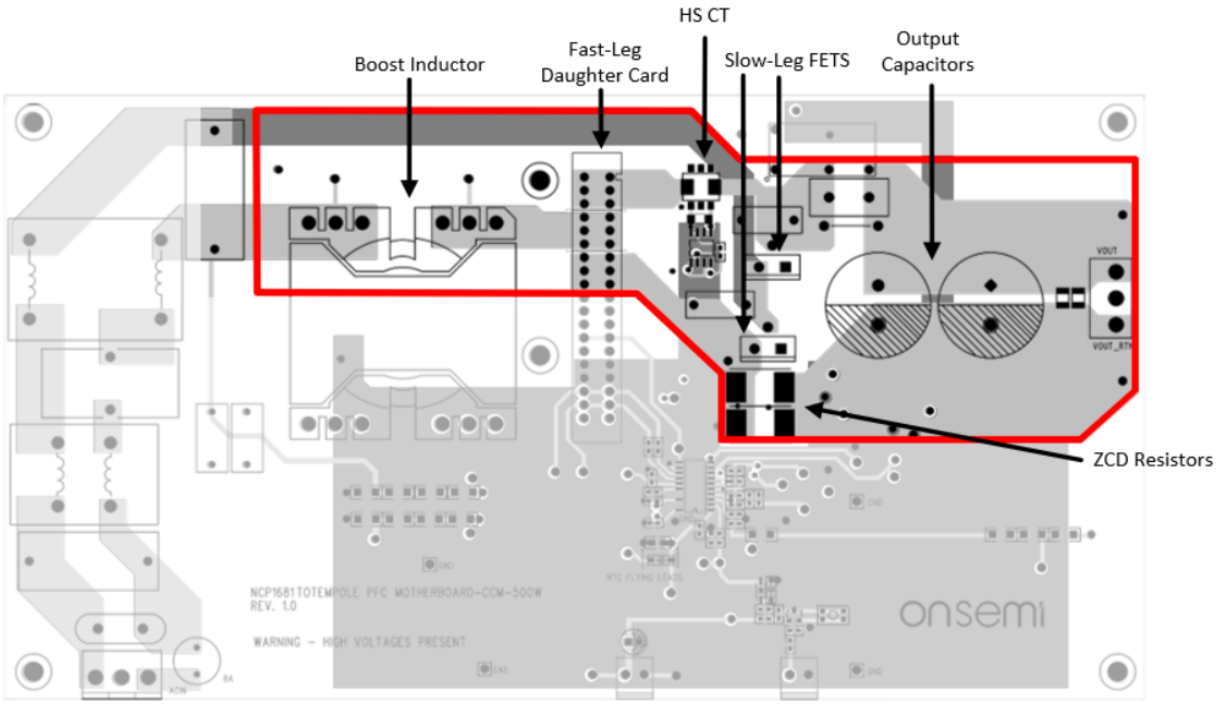

Figure 5. NCP1681 Motherboard Power Section

- Components in the power train should be kept close to each other to help contain the switching noise and are placed to avoid creating power loops that would affect noise sensitive low−voltage signals.
- Avoid placing FETs on a different layer or under of the inductor. This is not good for thermal management. Ensure that there are plenty of vias and copper around high power dissipating components.
- The ZCD resistors are part of both the power train and the low−voltage section, and need to be placed in the power loop, yet still be close enough to the controller to keep the ZCD signal short.
- The Fast−Leg daughter card contains the Fast−Leg switches and the isolated gate driver. The Fast−Leg circuit is separated on a daughtercard to allow for heatsinking specific to the needs of the switches used in the Fast−Leg daughtercard. Another benefit of using a separate daughter card is to test out multiple Fast−Leg switches (MOSFET, GaN, SiC) by swapping out

the daughtercard. As the highest dv/dt and di/dt is present in the Fast−Leg circuit, the daughtercard should be placed close to the boost inductor and the PFC output. The PWMH and PWML traces coming from the NCP1680/81 controller should also be as short and direct as possible, and being high speed, are susceptible to noise interference.

2. Low−Voltage Section

Low voltage section includes components that are used to program certain function in the IC such as the components for the Vm pin, input voltage, output voltage divider resistors and the PWM controller itself.

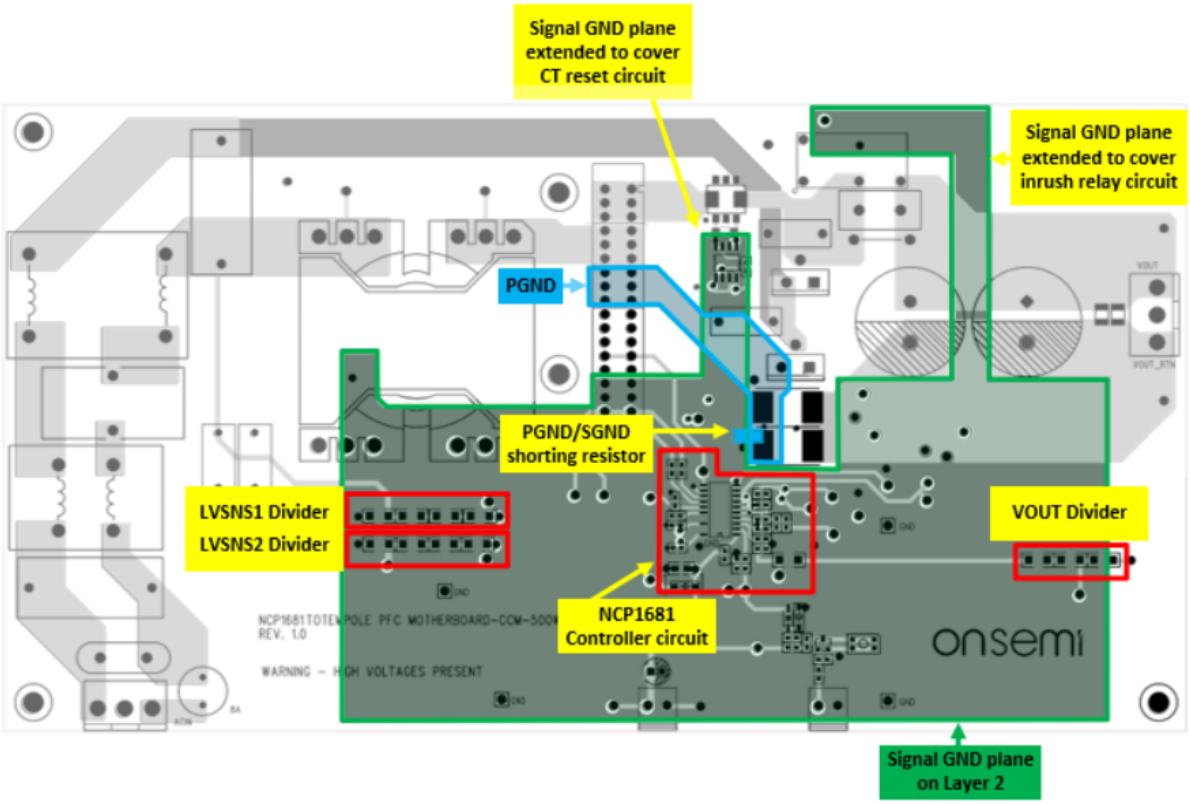

Figure 6. NCP1681 Motherboard Low Voltage Section

- If possible, keep all low−voltage signal components away from power section.
- All low−voltage signal components should be placed above a Signal GND plane to minimize switching noise spikes from affecting the low−voltage circuits.
- The controller needs to be placed above the signal ground plane, yet also be placed close to the ZCD resistors to keep the ZCD path as short as possible.
- Place all bypass capacitors close to the controller to reduce switching noise spikes from entering the IC.
- The 0 Ω PGND/SGND shorting resistor should be placed close to the ZCD resistors and the controller, as this is the return path for the ZCD signal and must be kept short. See ZCD signal routing section for more information.

- As the slow leg is switching at 60 Hz (line frequency), component placement isn't as critical as fast−leg and signal components. Make sure that Vcc and Boot capacitors are placed as close to the IC as possible, and the gate drive trace is not very long.

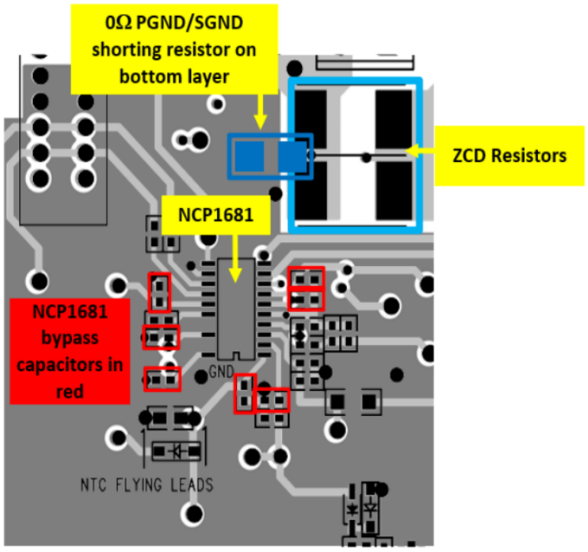

Figure 7. NCP1681 Bypass Capacitor and ZCD Component Placement

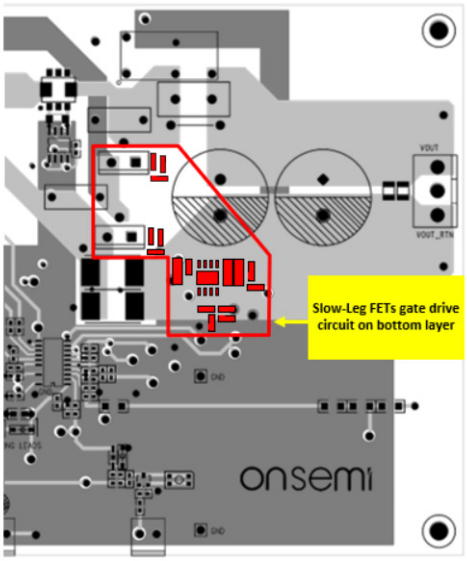

Figure 8. NCP1681 Slow−Leg Circuit

EMI Filter

EMI Filter components should be placed close together, and close to the AC input. EMI Filter design and component selection is dictated by individual EMI needs of converter. Make sure that the EMI filter is placed away from high frequency and high voltage switch nodes so that it doesn't pick up radiated noise. Often times, a boost inductor with a large gap should be shielded and grounded so that it doesn't accidentally radiate flux into other components and in particular EMI filter. Figure 9. shows an example of a tight EMI filter layout.

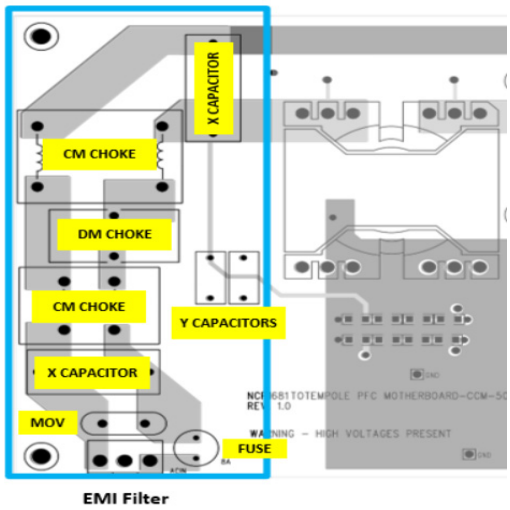

Figure 9. NCP1681 Motherboard EMI Filter Circuit

Motherboard Routing

Power Section

When routing the power section, it is best to follow the four different modes during the full AC cycle, and keep the current loops as small and short as possible to avoid injecting switching noise into low−voltage signal circuits. Shown below is the schematic current path, and it's equivalent in the layout:

Positive Line Cycle, Inductor Charging Mode

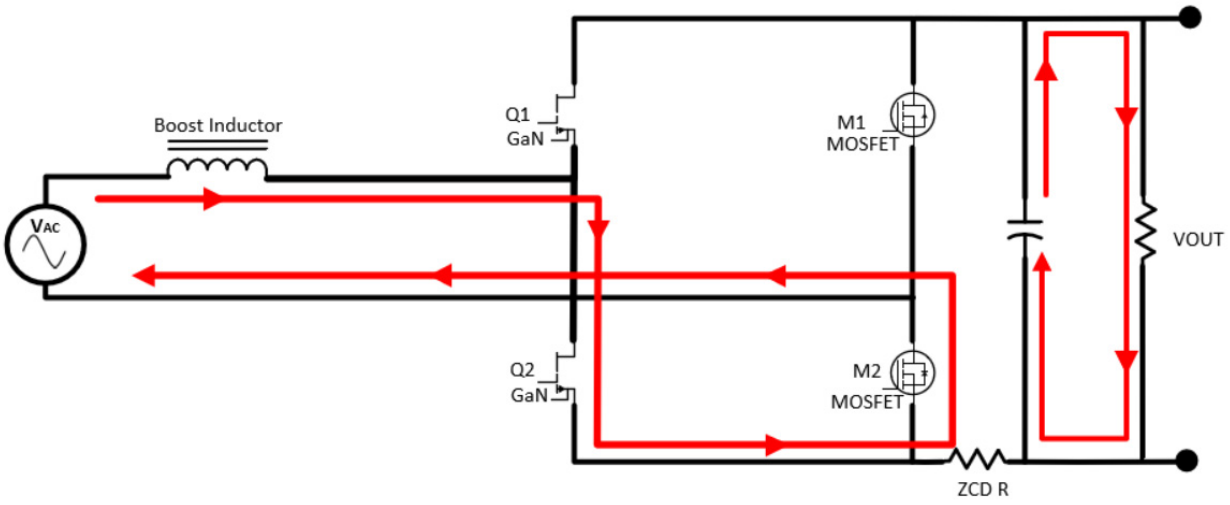

Figure 10. NCP1681 Positive Line Cycle, Charging Mode

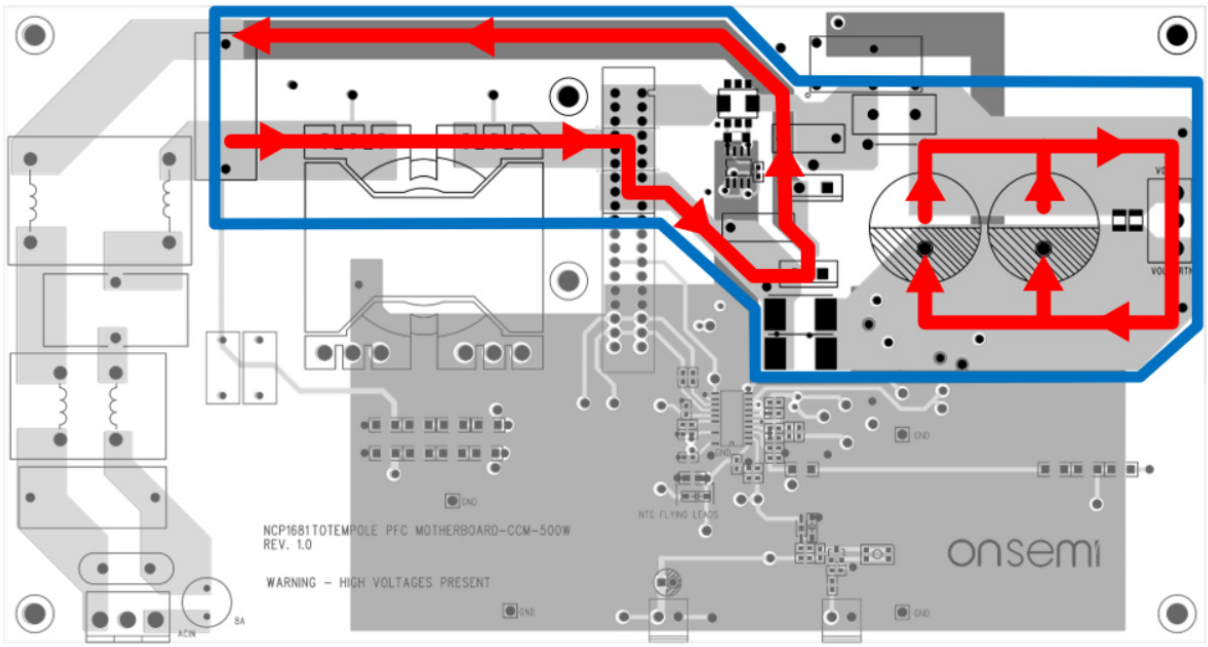

Figure 11. NCP1681 Motherboard Positive Line Cycle, Charging Mode

Positive Line Cycle, inductor discharge mode*

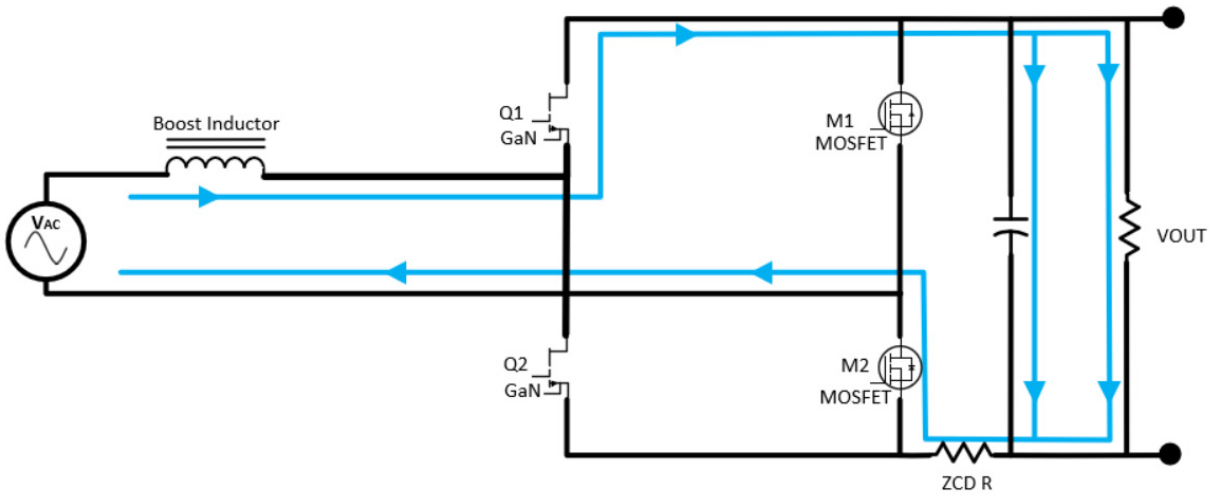

Figure 12. NCP1681 Positive Line Cycle, Afterflow Mode

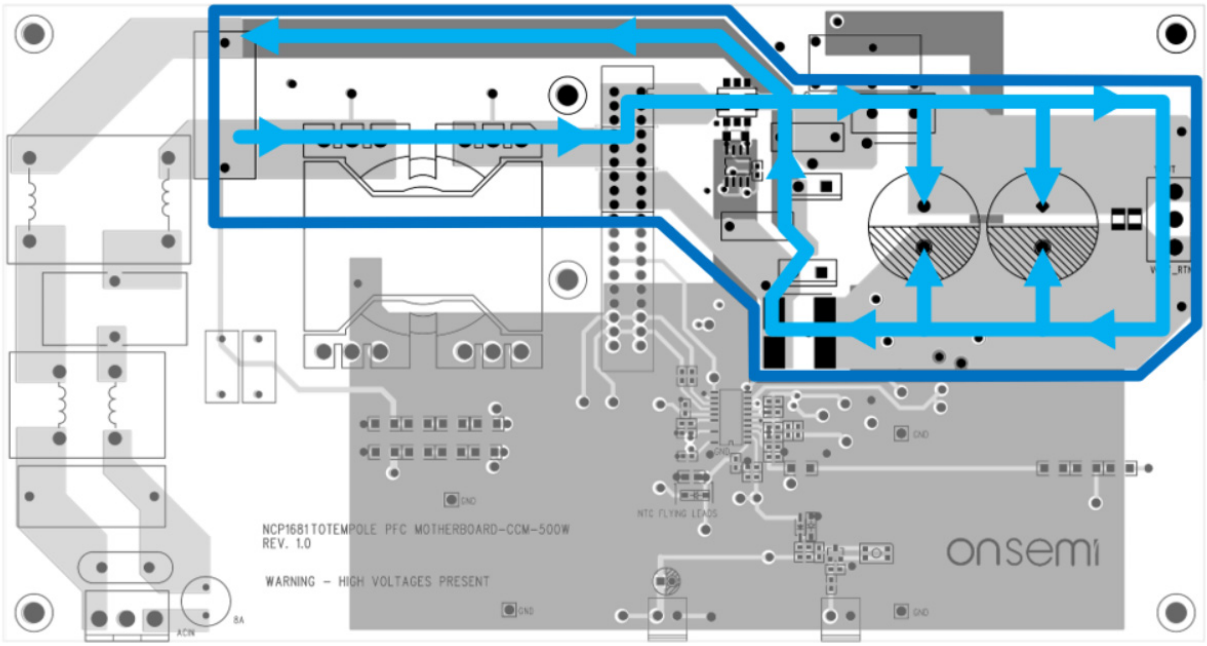

Figure 13. NCP1681 Motherboard Positive Line Cycle, Afterflow Mode

* **Note:** The loop created by the Afterflow routing and current path was dictated by the “wall” created by the high−speed daughter card placement, which forced the return path to cross the input path. Switching noise−sensitive components were kept out of that loop.

Negative Line Cycle, Inductor Charging Mode

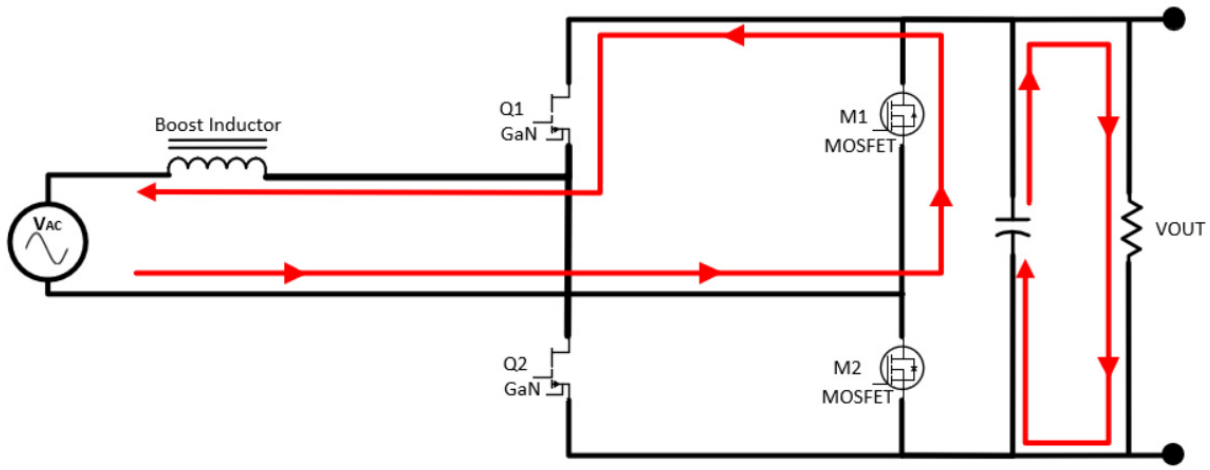

Figure 14. NCP1681 Negative Line Cycle, Charging Mode

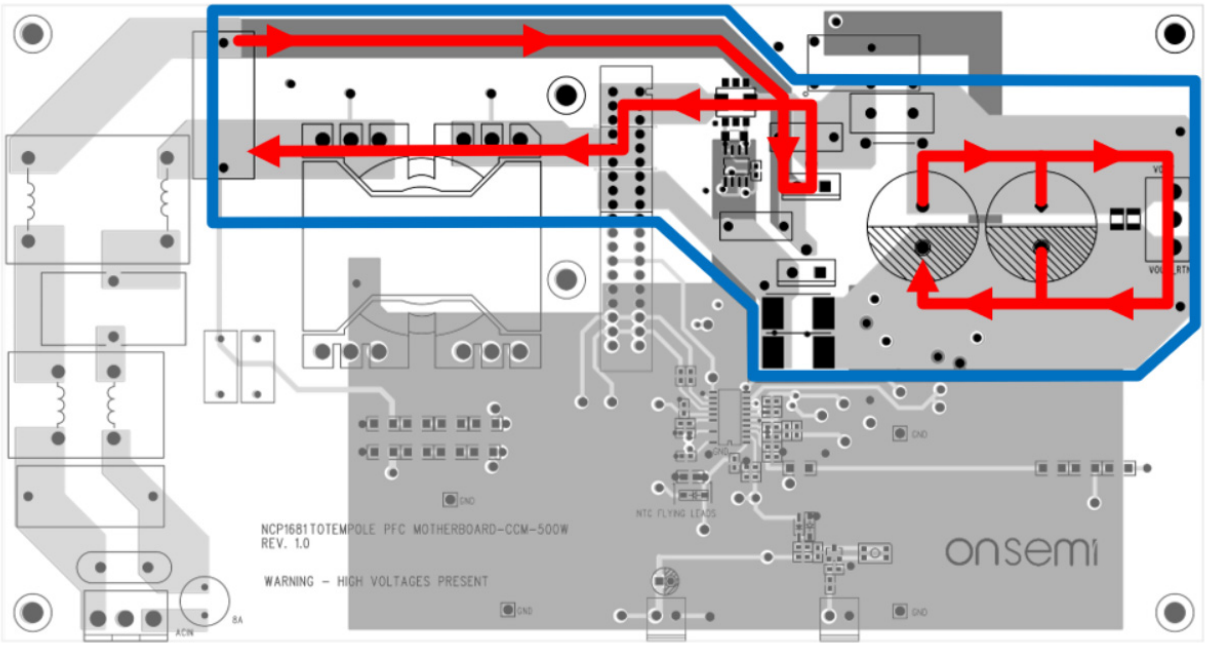

Figure 15. NCP1681 Motherboard Negative Line Cycle, Charging Mode

Negative Line Cycle, Inductor Discharge Mode

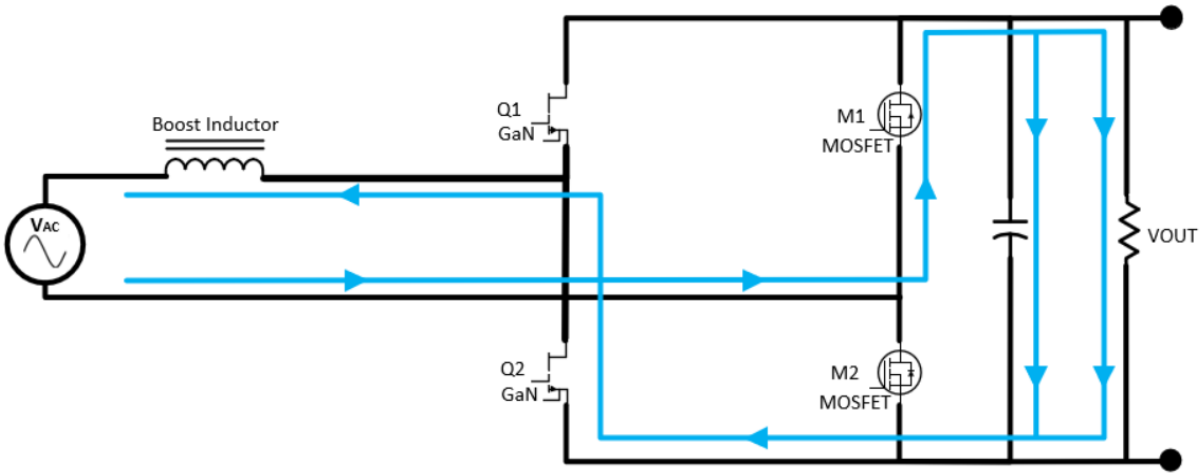

Figure 16. NCP1681 Negative Line Cycle, Afterflow Mode

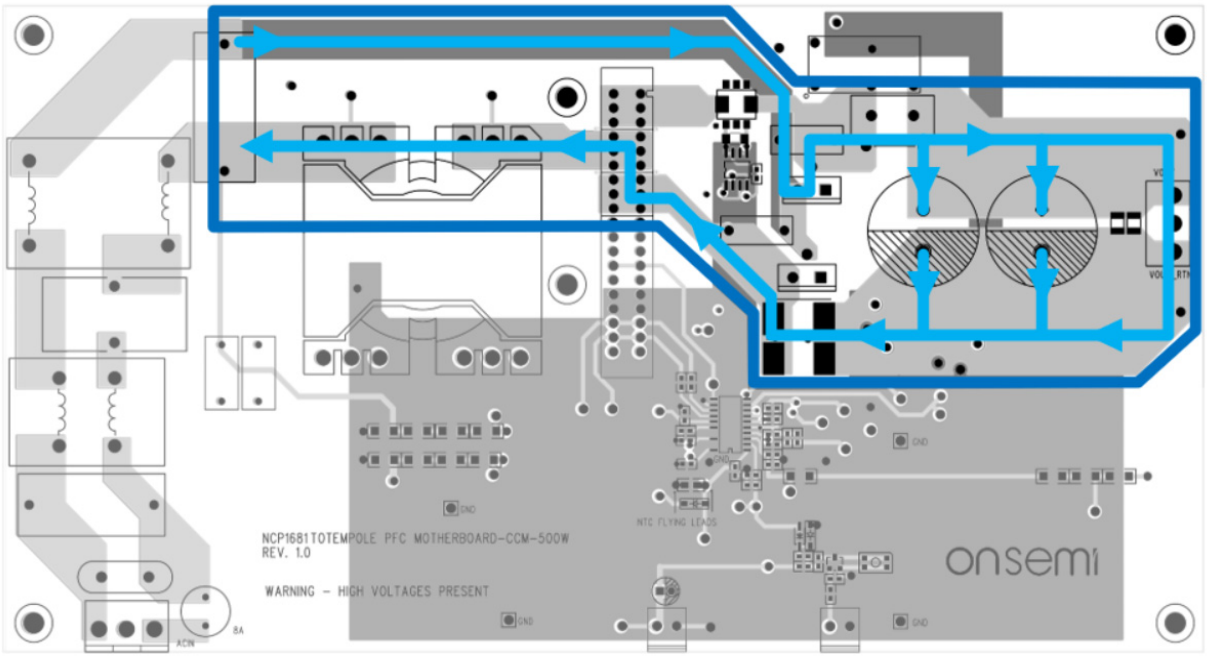

Figure 17. NCP1681 Motherboard Negative Line Cycle, Afterflow Mode

Low−Voltage Signal Routing

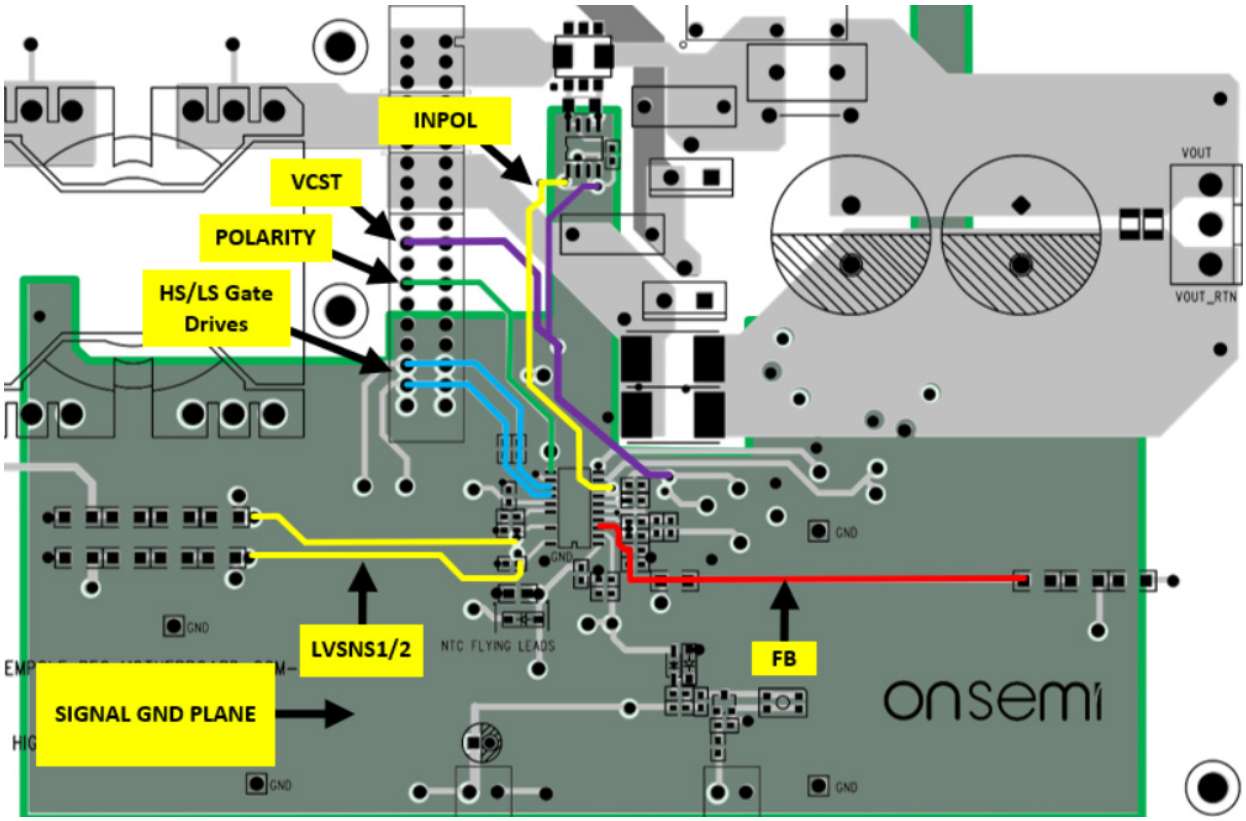

Figure 18. NCP1681 Motherboard Low−Voltage Signals

- As shown in Figure 18, keep all Low−voltage signals direct and over the Signal GND Plane as much as possible to use the shielding the Signal GND plane provides.
- Because all signals shown are low−voltage, the Signal GND Plane can be used as a return path to the controller. This keeps all returns as short as possible.

ZCD Routing

The ZCD circuit is important as it controls the 1−D operation. The ZCD signal needs to be clean, short and noise free. The difficulty is that the ZCD resistors are also a part of the high−speed/high−current switching path. Care must be excersized in routing the ZCD sense paths. Follow the below steps to help keep the ZCD signal clean.

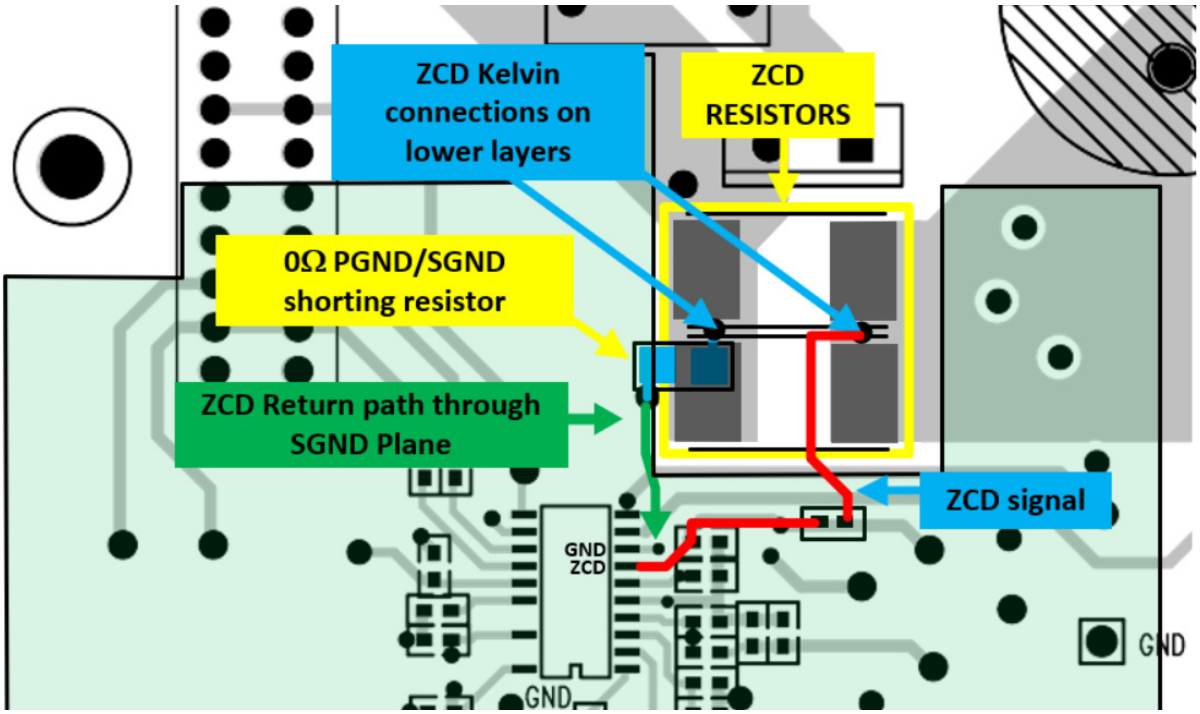

Figure 19. NCP1681 Motherboard ZCD Circuit

- Use a Kelvin connection from the ZCD resistors to route the ZCD signal to the controller. If the ZCD resistors don't have a Kelvin pin, via−connect the ZCD sense trace to the ZCD resistors.
- Keep the ZCD signal as short and as shielded as possible to the controller.
- The 0 Ω PGND/SGND shorting resistor needs to be kept close to the ZCD resistor and the controller, as it's the return connection for the ZCD signal. One side of the resistor connects through a Kelvin connection to the ZCD resistors. The other side connects to the SGND plane.

High−Speed Daughter Card

The high−speed daughter card is a unique circuit board, as it has both power and signal−level circuits on it, and they must be separated. As the signals are separated on the daughtercard, daughter card position and routing are important.

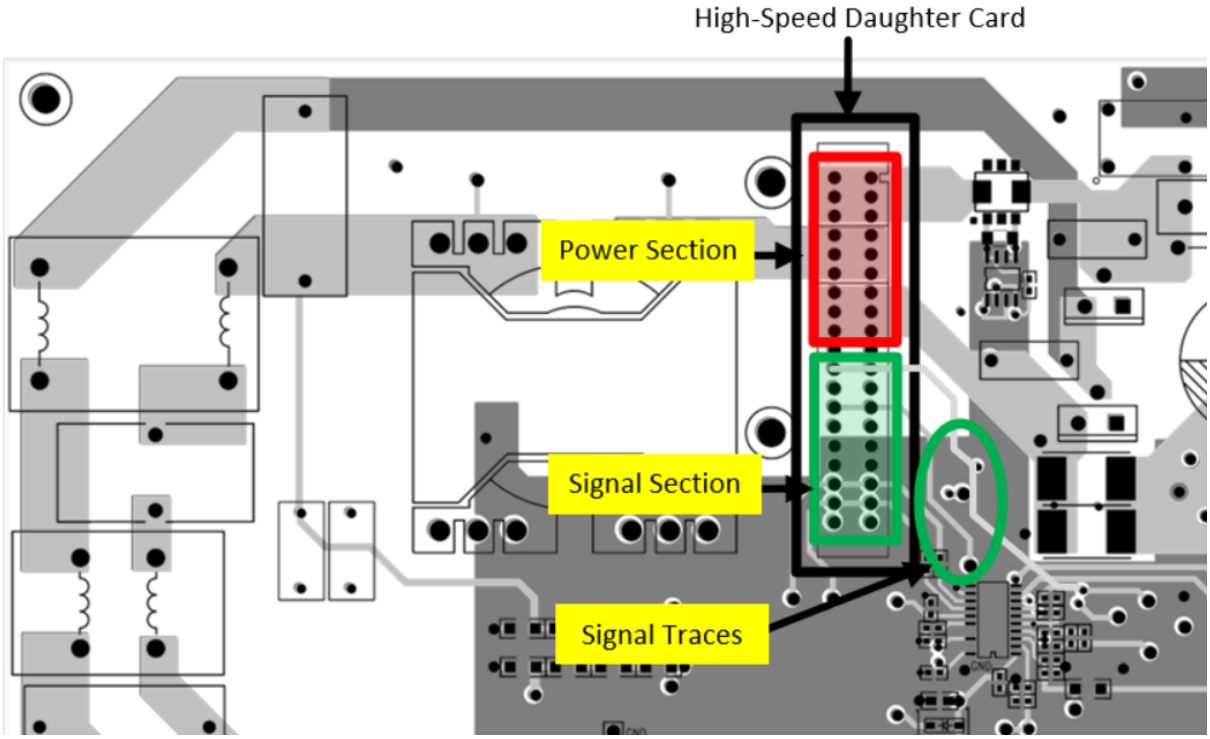

Figure 20. NCP1681 High−Speed Daughter Card Placement and Routing

- Extend Signal GND plane under the signal section of the daughter card.
- Keep the power paths away from the signal section of the board.
- Route the signal traces away from the power section and try to route them over the signal GND plane

Motherboard Grounding

The high−speed, high−current Power Ground path on the TPFC must be kept electrically connected, but physically separated from the Signal Ground. The noise generated on the Power Ground can affect the low voltage signals like ZCD and introduce noise related errors to the controller.

- Use a separate Signal GND plane under all low−voltage (signal) components.
- Try to route all low−voltage signals over the Signal GND Plane.
- Keep all high−power ground return paths separate from signal ground paths if possible.

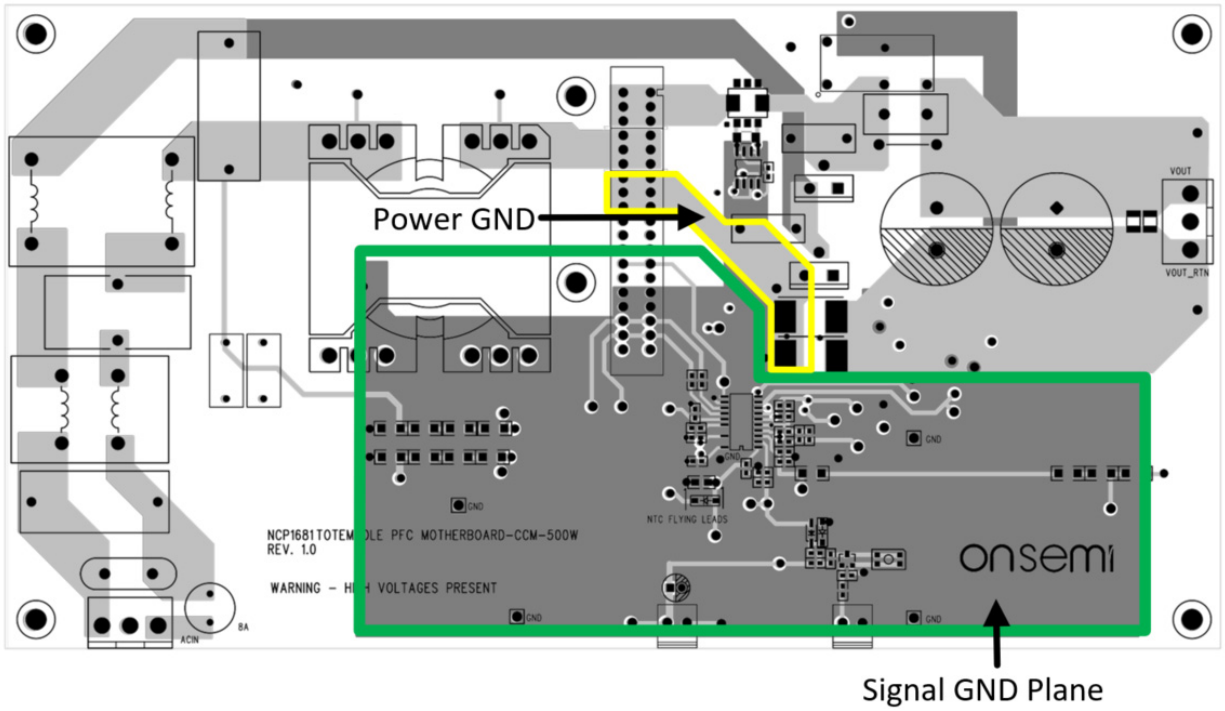

Figure 21. NCP1681 Power GND and Signal GND Plane

- As Power Ground and Signal Ground must be electrically connected, a single−point connection should be used. In this design the single−point connection used was a 0 Ω PGND/SGND resistor. Because the only current path needed from PGND to SGND is the return from ZCD, that 0Ω resistor was placed close to the ZCD resistors and the controller.

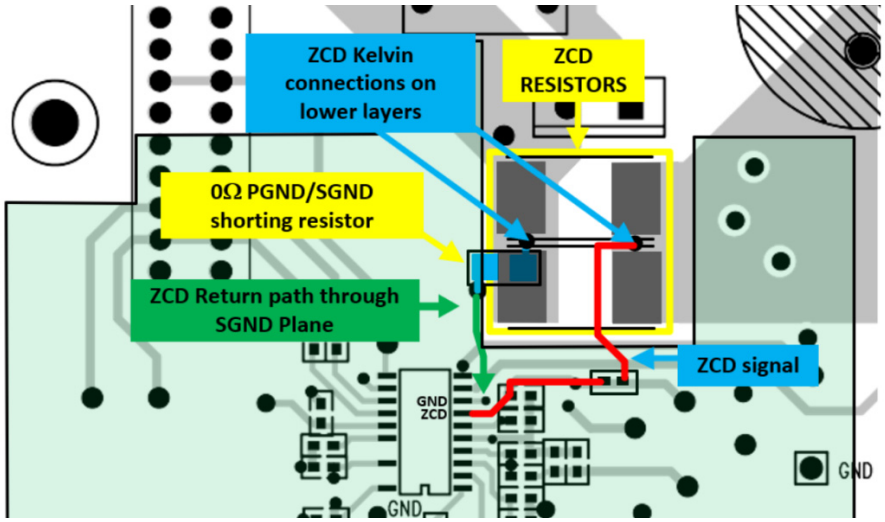

Figure 22. NCP1681 PGND/SGND Single−Point Connection Resistor Placement

Thermal Management

Thermal management of the power devices must be considered when laying out this design.

- Keep all power traces as wide and thick as possible. This will keep DC losses low and allow component heat dissipation with the large copper areas. If feasible, multiple PCB layers can be used.

Layout design to control the temperature rise of the Fast−Leg switch circuit is critical, as these devices (ex. GaN) are usually small and without the Drain tabs that power MOSFETS have to attach heatsinks to. Heatsinking for these devices is done through heat−spreading PCB traces and planes, which can be thermally connected (but electrically isolated) to PCB−mounted heatsinks.

- Put heat−spreading planes as large as possible under the Fast−Leg power devices. Use thermal vias to connect the high−speed device power pads to the heat−spreading planes, as shown in Figure 23.
- Keep the heat−spreading planes under the Fast−Leg power devices clear of components so if needed, a heatsink can be attached to the planes for additional thermal cooling.
- If possible, use multiple PCB layers for the heat−spreader planes.

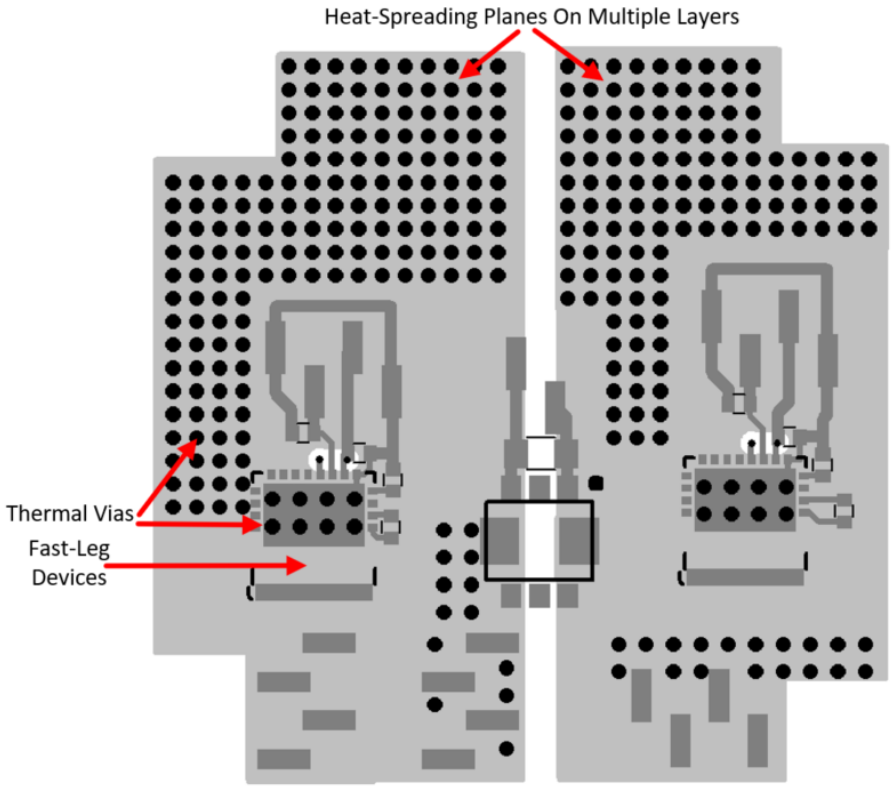

Figure 23. Fast−Leg Device Thermal Placement and Routing

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