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White Paper

Gate Drive Optocouplers for GaN Power Devices

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Introduction

Gallium nitride (GaN) power devices are gaining popularity over silicon power devices because their faster switching capability can improve overall system efficiency and reduce the size of the device and the operating cost. The technical benefits coupled with lower costs due to the increase in GaN production have increased the adoption in applications such as industrial power supplies and renewable energy inverters.

Broadcom® Inc. (formerly Avago Technologies) gate drive optocouplers are used extensively in driving silicon-based semiconductors, such as IGBT and power MOSFETs. Optocouplers provide reinforced galvanic insulation between the control circuits and the high voltages. The ability to reject high common mode noise prevents erroneous driving of the power semiconductors during high-frequency switching. This paper describes the benefits of GaN, its gate drive requirements, and the gate drive designs, tests, and performance.

Benefits of GaN

Gallium nitride is a wide bandgap (3.4 eV) compound made up of gallium and nitrogen. Bandgap is a region formed at the junction of materials where no electron exists. Wide bandgap GaN has a high breakdown voltage and a low conduction resistance. It has a higher electron velocity and a lower parasitic capacitance, which improve its switching speed.

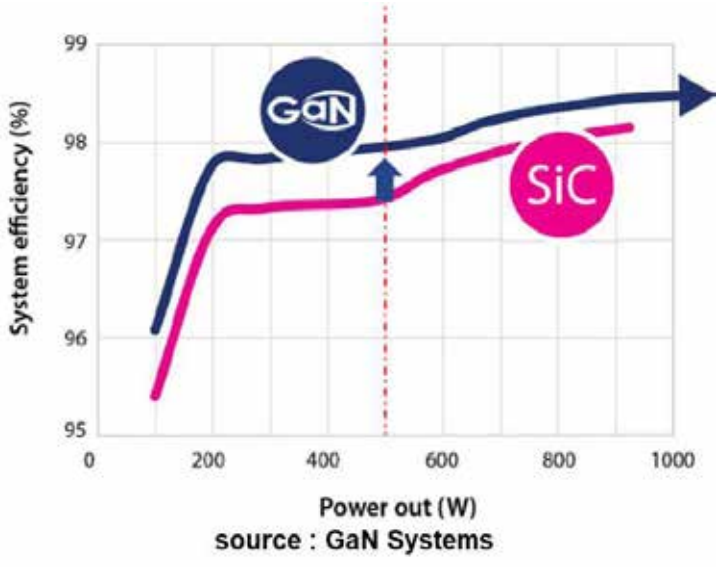
The benefits of GaN over silicon can be summarized by three main points:

- Smaller system designs
- Lower system costs
- Higher system efficiency

Figure 1: Silicon vs. GaN, Smaller Size and Lower System Costs

The smaller size and lower costs are the result of fewer and smaller peripheral components. GaN can operate in reverse conduction mode, which can eliminate an external freewheeling diode. It can operate in high frequency, which results in smaller filters and magnetics, such as inductors and transformers. GaN operates 60°C cooler than silicon, which helps to reduce the size of the heat sink.

Figure 2: Silicon vs. GaN, Higher System Efficiency



Higher efficiency is the result of lower switching and conduction loss. GaN has a higher electron velocity and a lower parasitic capacitance for low switching loss. It is also smaller in size than silicon at the same breakdown voltage and, hence, delivers lower conduction resistance.

Types of GaN and Gate Drive Requirements

Figure 3: Types of GaN and Gate Drive Requirements

	Panasonic	GaN Systems	Brand "T"	Brand "E"
Part Number	**PGA26E07BA**	**GS66508P**	**Txxxxxx**	**Exxxxxx**
Type	Normally Off (**GIT**)	Normally Off	**Normally On (Cascode)**	Normally Off
Ratings	600V/26A (56mΩ)	650/30A(50mΩ)	650V/26.5A(85mΩ)	**200/32A**
V_{GS}(max)	-10V/I_G<50mA	-10/+7V -20/+10V, transient abs max	-18/+18V	-4/6V
Vth(typ)	1.2V	1.7V	2.1V	1.6V
Cin/Qg	0.405nF/5nC	0.260nF/5.8nC	1.13nF/2.2nC	0.875nF/8.2nC
dv/dt (kV/us)	> 100kV/us	> 100kV/us	> 100kV/us	> 100kV/us
		Gate Drive Requirements		
Gate Voltage,V_{GS} Gate Current	12V <1.5A	+6V <1.2A	+10V <0.7A	+5V <0.5A
Notes	Gate DC holding current <10mA	• V_{GS} 7V abs max • Low static gate current	**Slew rate cannot be control due to Cascode topology**	• V_{GS} 6V abs max • Low V_{DS} • **Passivated Die**

Figure 3 shows the different types of GaN and their gate drive requirements. Brand E, for example, manufactures 200V GaN, used mainly for low-voltage applications, such as a 12V DC-DC converter. Brand T manufactures 600V GaN, but it is a normally-on switch. It requires a low-voltage Silicon MOS in a cascode connection to turn it into a normally-off switch that is safer to use. Due to the cascode structure, the switching speed cannot be controlled by adjusting the gate resistance, which leads to complications in fine-tuning the electromagnetic interference (EMI) and switching loss.

Panasonic and GaN Systems manufacture normally-off switches by using a P-type barrier structure under gate to deplete the high-mobility electrons during 0V gate bias. Due to the high electron mobility, the threshold of GaN, V_{TH}, is relatively lower than that of silicon MOS or IGBT. The input capacitance is also very small, less than 1 nF and only requires 5 nC to switch on.

GaN switches very fast and care should be taken when designing with a high switching dv/dt. It is important to control the high dv/dt noise coupling from the GaN to the gate driver. Otherwise, the gate drivers must have a noise immunity of more than 100kV/µs to prevent false switching of the GaN.

Because GaN devices from Panasonic and GaN Systems are normally off and easy to use, the gate drive requirements are similar to silicon MOS. Panasonic GaN has a robust gate, which allows a high gate voltage of 12V for fast turning on of the gate. GaN Systems recommends 6V to charge the gate. Due to the small gate capacitance and gate charge required, the gate current needed is relatively low at less than 1.5A.

For Panasonic GaN, the gate requires a DC holding current of approximately 10 mA to maintain it in an "ON" status. For GaN Systems, special care is required to ensure that the absolute maximum gate voltage of 7V is not exceeded.

Gate Drive Design for Panasonic GaN

Figure 4: Half Bridge Evaluation Board with Panasonic GaN and ACPL-P346

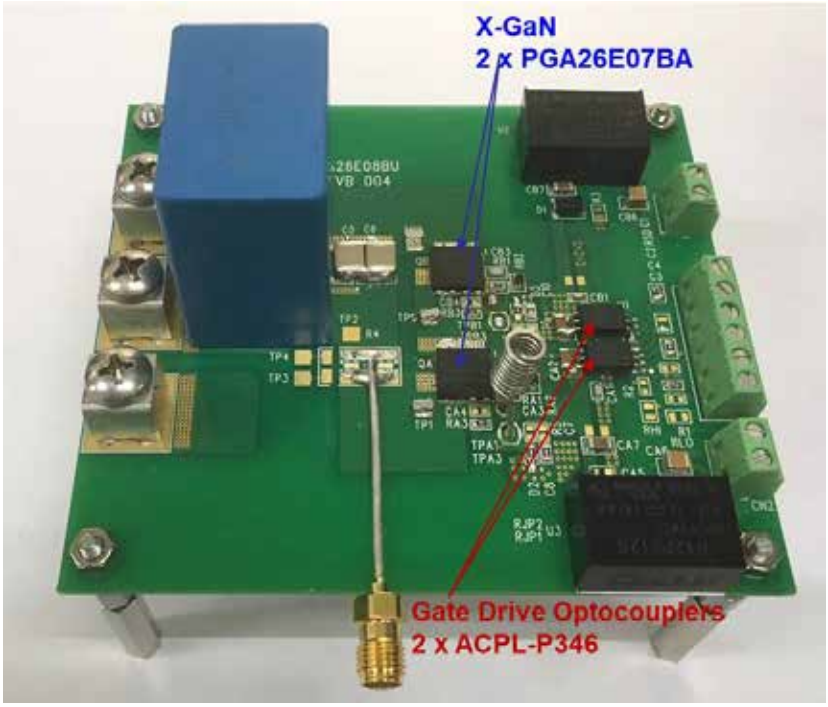
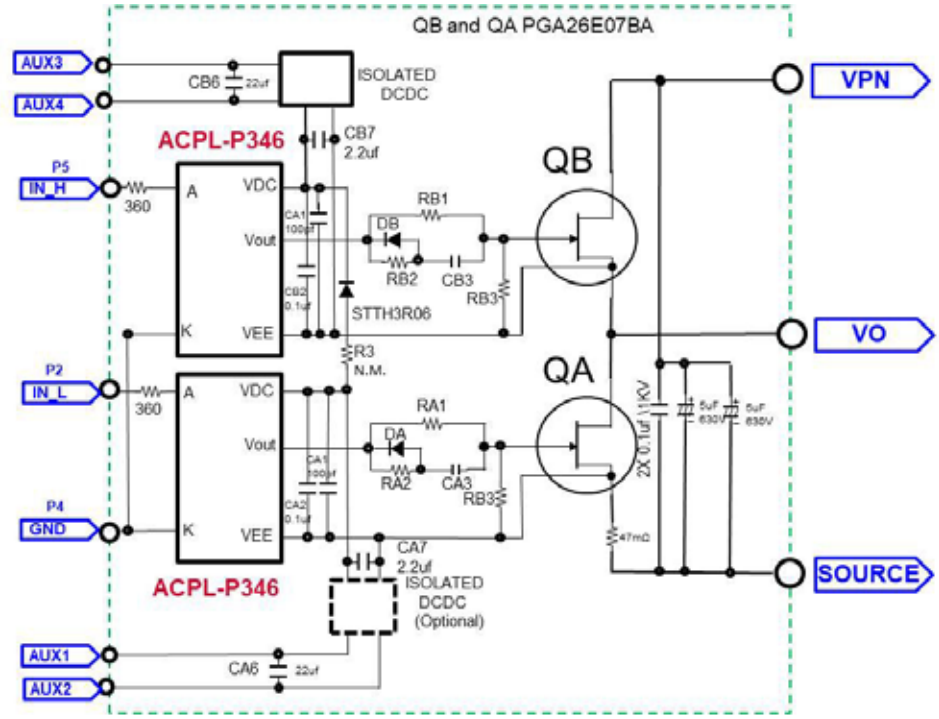


Figure 4 shows a half bridge evaluation board featuring Panasonic 600V 70-mΩ X-GaN transistor, PGA26E07BA. The gate drive is designed using two gate drive optocouplers, ACPL-P346, to drive the GaN transistor directly.

The ACPL-P346 is a basic gate driver optocoupler that isolates and drives the GaN operating at a high DC bus voltage. It has a rail-to-rail output with a 2.5A maximum output current to provide fast switching high voltage and driving current to turn on and turn off the GaN efficiently and reliably. The ACPL-P346 has maximum propagation delay times of less than 110 ns and typical rise and fall times of around 8 ns. The very high common mode rejection (CMR) of 100kV/μs (minimum) is required to isolate high transient noise during the high-frequency operation.

Figure 5: Schematic of Half Bridge Evaluation Board with Panasonic GaN and ACPL-P346



RB1,RA1	RB2,RA2	CB3,CA3	RB3,RA3	DB,DA
680Ω	22Ω	1500pF	10KΩ	BAV21WS

Figure 5 shows the schematic of the half bridge evaluation board and the ACPL-P346 gate drive design. The GaN transistors, QB and QA, require about 12.5 mA on-state current to continuously bias the transistor in on-state. This is done by the gate driver through 680Ω resistors, RB1 and RA1.

The initial in-rush charging current to switch on the GaN quickly is provided by ACPL-P346, and the peak current is limited by resistors RB2 and RA2. Capacitors CB3 and CA3 are used to turn on the GaN faster by increasing the charging current momentarily. The board has the flexibility to be powered by two isolated DC-DC supplies for the top and bottom bridges or one DC-DC with bootstrapping.

Gate Drive Design for GaN Systems GaN

Figure 6: Half Bridge Evaluation Board with GaN Systems GaN and ACPL-P346

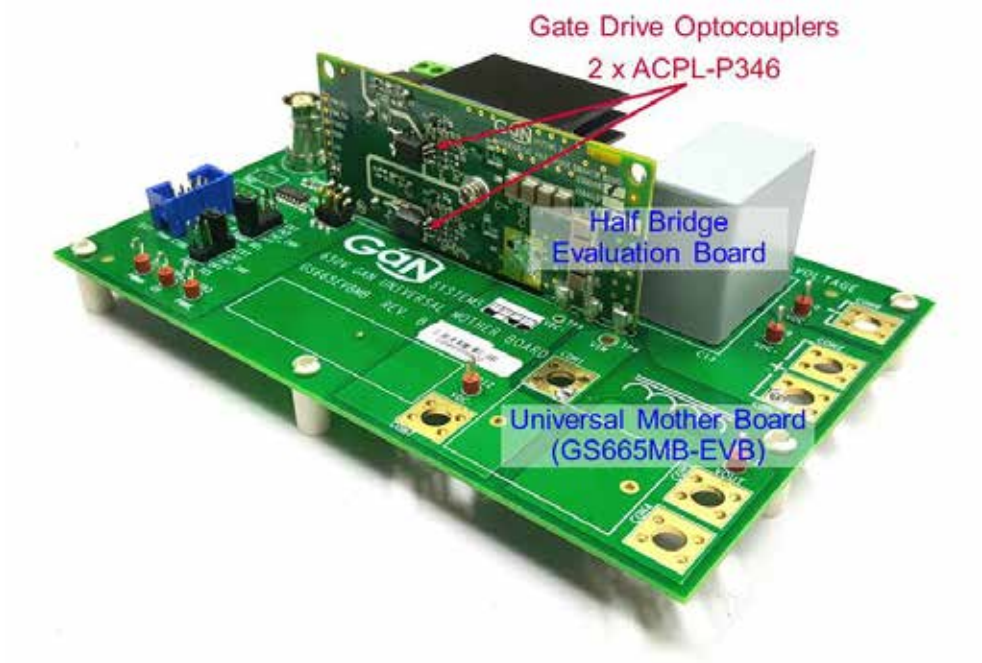
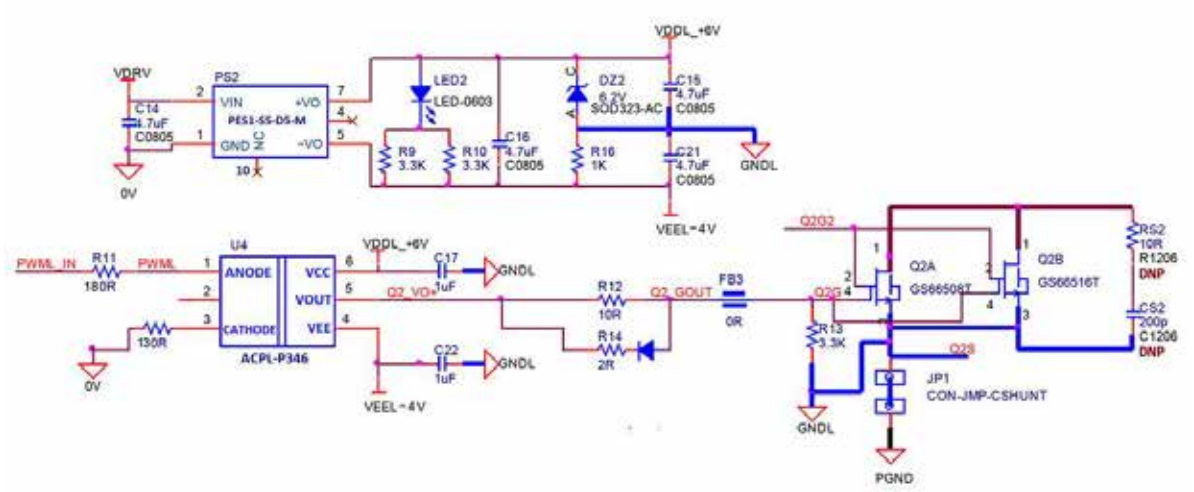


Figure 6 shows another half bridge evaluation board featuring GaN Systems' 650V E-HEMT GS66508T (30A/50m) GaN transistor. The half bridge evaluation board uses two gate drive optocouplers, ACPL-P346, to drive the GaN transistors directly. The schematic shows the bottom bridge gate bias and driver circuit. The top bridge uses the same circuitry. The isolated DC-DC, 5V to 10V converters provide +6V and –4V bipolar gate drive bias for more robust gate drive and better noise immunity. The 10V is then split into +6.2V and –3.8V bias by using a 6.2V Zener diode. The ACPL-P346 gate drive output is a combination of a 10Ω gate current-limiting resistor (for charging) and a 10Ω paralleled with 2Ω plus a diode for discharging.

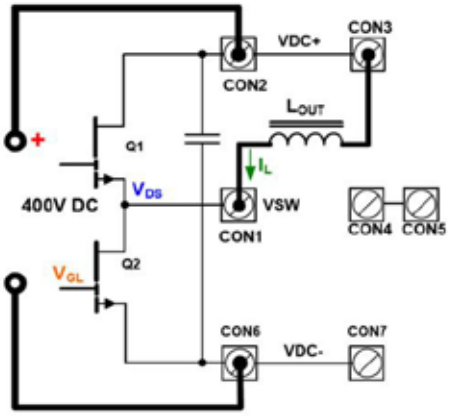
Figure 7: Schematic of ACPL-P346 Gate Drive Circuit for GaN Systems Half Bridge Evaluation Board



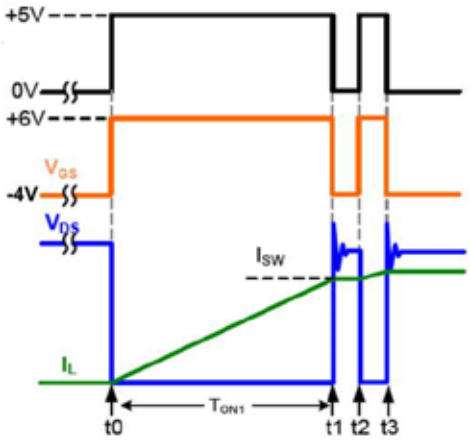
GaN Half Bridge Evaluation Board Test and Performance

Using the half bridge evaluation board from Panasonic and GaN Systems, the slew rate, switching power loss, and efficiency tests were performed on the GaN and ACPL-P346.

Figure 8: Slew Rate and Switching Power Loss Test Setup and Waveforms



Boost Configuration
(Low Side Test)



Input Double Pulse Test Pattern

An inductor of approximately 120 µH to 160 µH was connected between VDC+ and VSW to form the boost configuration, also known as the low-side test. The low-side GaN transistor Q2 was active in boost mode. A bus voltage of 400V was applied to VDC+/VDC–. A double pulse test was used for evaluating the device switching performance at high voltage and current without the need of running at high power.

The period of first pulse T_{ON1} applied to Q2 defined the switching current I_{SW}. t1 (turn-off) and t2 (turn-on) were the measurement points as they were the hard-switching transients for the half bridge circuit when Q2 was under high-switching stress.

The slew rate tests were conducted at 400V DC and around 30A hard switching.

Figure 9: Panasonic GaN and ACPL-P346 Slew Rate Test

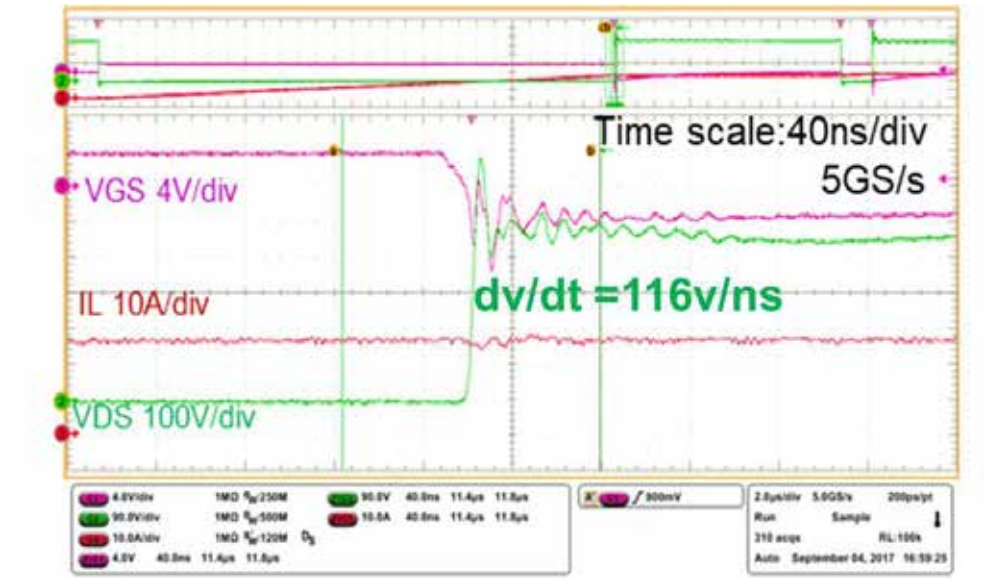
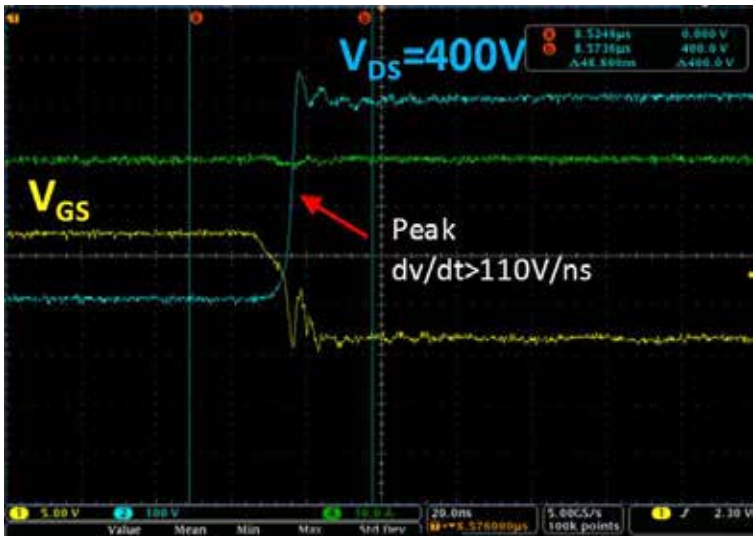


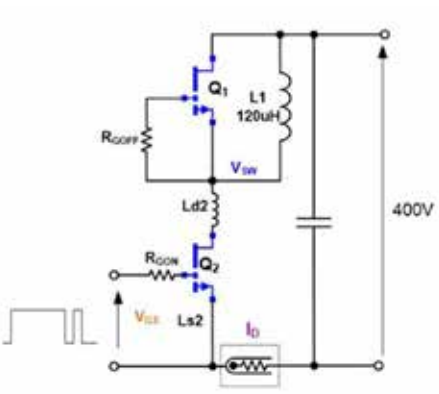
Figure 10: GaN Systems GaN and ACPL-P346 Slew Rate Test



The Q2 turn-on and turn-off slew rates (dv/dt) were measured at t1 (turn-off) and t2 (turn-on), respectively. The highest slew rates of more than 110kV/µs were measured when the GaN hard-turned-off at 400V, 30A.

ACPL-P346 has a minimum CMR of 100kV/µs. In other words, ACPL-P346 can isolate high transient dv/dt noise from the GaN switching. The scope pictures show that the GaN fast slew rates are not affecting the gate drive outputs and gate voltages.

Figure 11: Switching Power Loss Test Setup and Waveforms

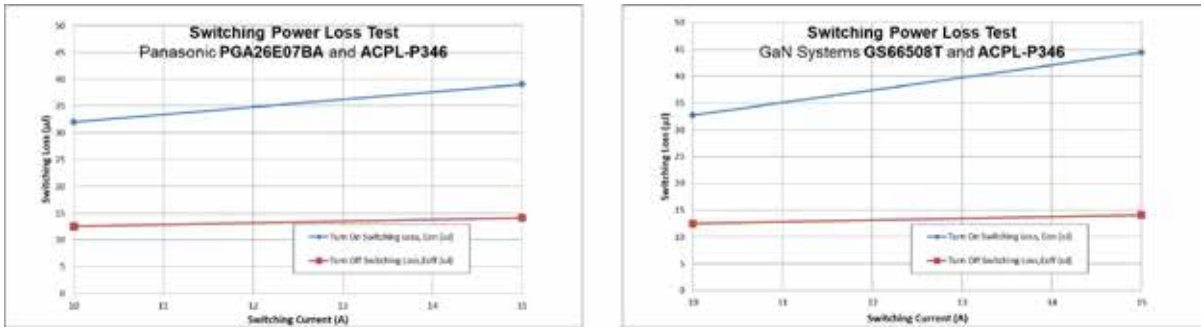


Boost Configuration
(Switching Power Loss Test)

Turn On Switching Loss Measurement

The switching-loss test used the same boost configuration with a current sensor installed for I_D measurement. The same double pulse signals and timing of the slew rate test were used for the power loss measurement. The measurement was done at the monitoring points when the GaN turned on or turned off at the target current level. The math function on the oscilloscope was used to find the multiplication of V_{DS} and I_{DS}. The measure function on the oscilloscope was then used to find the power loss, which is the area under the curve.

Figure 12: Switching Power Loss Measurements



The turn-off power losses are represented by the red line, and both GaN power losses were kept below 15µJ regardless of the inductor load current. The turn-on power losses are represented by the blue line, both GaN devices show a low loss of around 40µJ at 15A.

The half bridge evaluation boards were connected as DC-DC converters to test the efficiency of GaN in a hard-switching operation. The Panasonic GaN DC-DC was connected in boost 200V to 380V configuration, while the GaN Systems DC-DC was connected in buck 400V to 200V configuration (Q1 was turned on to charge the inductor and turned off to allow inductor current to continue discharging through the output capacitor and through Q2 as the freewheeling diode). Both converters were operated at 100-kHz frequency, room temperature, and the efficiency at different power levels tested.

Figure 13: Efficiency Test Setup

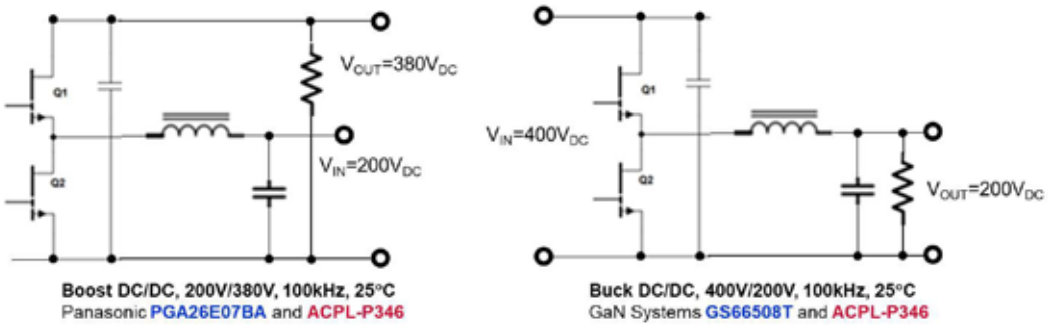
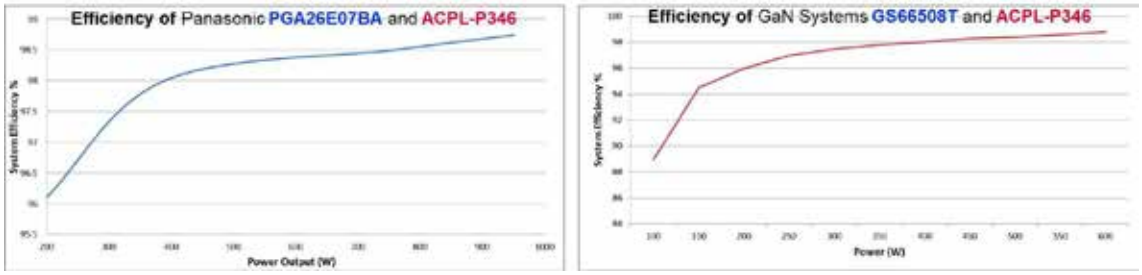


Figure 14: Efficiency Test Measurements



Both converters showed high conversion efficiency of approximately 99%.

Acknowledgement

Broadcom thanks the application teams of Panasonic Semiconductor Solutions Singapore and GaN Systems for their technical support.

References

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