ACPL-352J

Isolated SiC(Silicon Carbide)/GaN(Gallium Nitride) or IGBT Gate Driver Evaluation Board

AVAGO TECHNOLOGIES
A Broadcom Limited Company

Design Guide

Quick-Start

Visual inspection is needed to ensure that the Evaluation Board is received in good condition.

Default connections of the Evaluation Board are as shown below (see Figure 1):

1. CON1, CON2 and CON3 are provided to allow for the evaluation board to be plugged in to the main controller board (CON1 to where microcontroller is and where PWM drive signals will be generated) and to the Gate (CON2) and Source (CON3) terminals of the SiC directly. A separate cable link (with sufficient thickness) is needed to link the Drain terminal of the SiC to the OC connection point on the evaluation board. This link allows the desaturation of SiC to be sensed and protected by the ACPL-352J gate drive device.
2. CON4 is provided to allow for the external connection of +20V V_{CC2} and –4V V_{EE} supplies with respect to V_E in case U2 (DCDC converter) is not provided. To save cost, the evaluation board is able to work under a single supply of +24V across V_{CC2} and V_{EE}. When a single supply of +24V is connected externally across V_{CC2} and V_{EE}, the R6 resistor and 4.7V Z1 zener will be able to provide a loosely regulated +19.3V and 4.7V supplies at V_{CC2} and V_{EE} respectively, wrt V_E. Negative V_{EE} supply is good to have to provide fast turn-off of the SiC and to prevent Miller False turn-on effect.
3. U3 (LM78L05) regulator is provided to supply the necessary +5V DC supply at V_{CC1}. UVLO, Fault and GFault signaling logics can work only when a +5V supply is provided at V_{CC1}.
4. J1 is connected by default to allow for a single PWM signal to control the device's LED (through Pin-6 of CON1) for PWM switching at the outputs at Pin-10 and Pin-11.

Once inspection is done, the Evaluation Board can be powered up for use in the following simple steps:

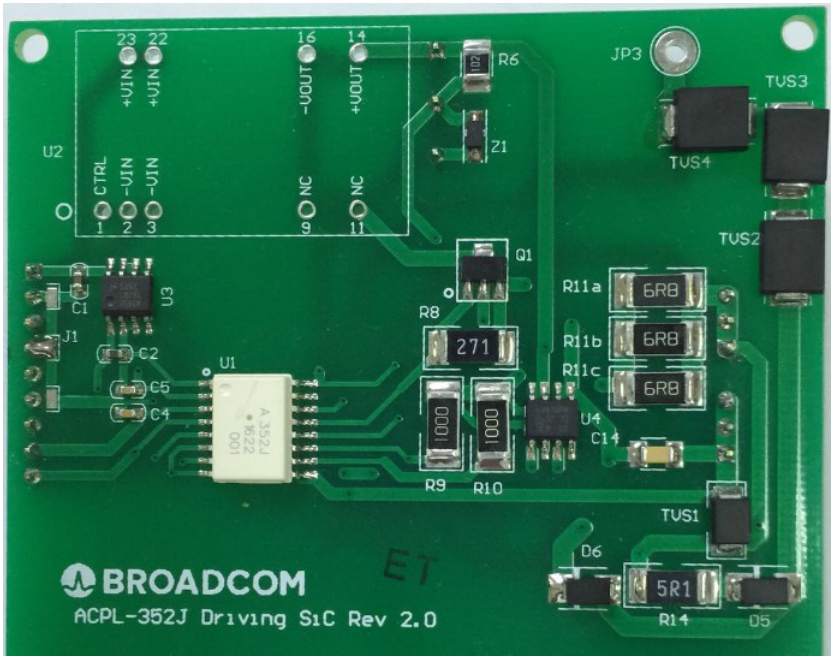
1. Plug the evaluation board to the main controller board through CON1 and to the SiC/GaN (or IGBT) directly through CON2 and CON3. Also ensure that CON4 are plugged in to the proper external supply (or supplies).
2. Connect a cable link from OC terminal (marked JP3 on PCB) to the SiC/GaN (or IGBT) drain terminal.
3. Turn-on the +12V supply to Pin-1 and 2 of CON1 and proper external supply (+24V preferred assuming U2 is not connected) to Pin-1 and 5 of CON4. These should power up V_{CC1}(through U3), V_{CC2} and V_{EE} side of the gate driver device.
4. Initiate the PWM switching signal (high frequency, 5V square-wave) to CON1's LED High pin (pin-3) and observe the SiC/GaN (or IGBT) gate driving signal output across CON2 and CON3 through an oscilloscope.
5. If needed, UVLO, Fault and GFault feedback signals can be observed after UVLO, Desat and GFault faults are simulated, respectively.

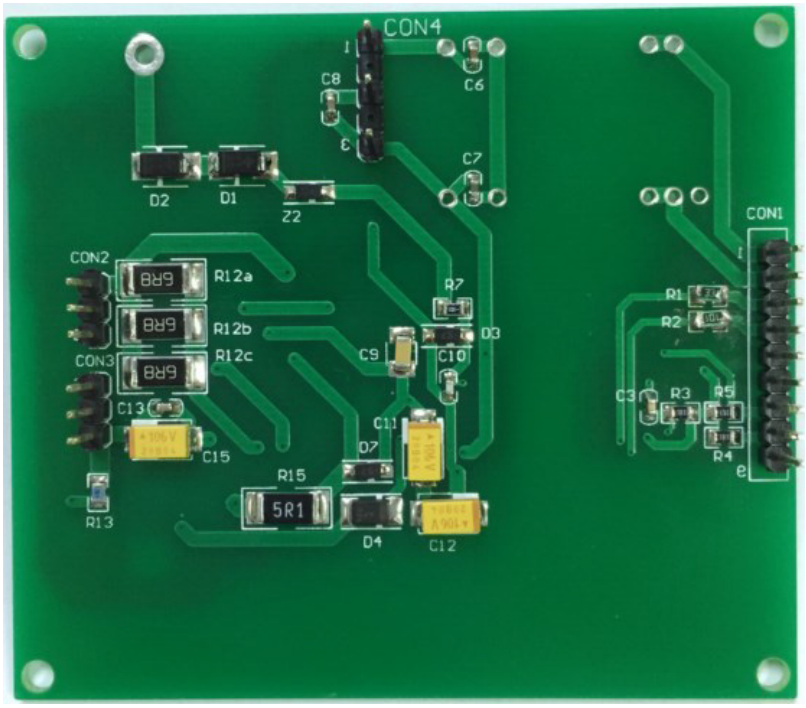
NOTE The Evaluation Board can be powered up for evaluation purposes only without the need for connection with any main controller board, and without a need for SiC/GaN (or IGBT). For stand-alone test setup, perform the following steps.

1. Connect a 47nF 25V rated capacitance across the CON2 and CON3 terminals to simulate a virtual high current rated SiC/GaN (or IGBT).
2. Connect a short cable link from OC terminal to V_E to simulate a saturated SiC/GaN (or IGBT). This short is needed to suppress Desaturation/Overcurrent Fault from occurring.
3. Assuming U2 is not connected, connect a +12V DC supply across Pin-1 and 2 of CON1, and a +24V DC supply across Pin-1 and 5 of CON4. These should power up V_{CC1}(through U3), V_{CC2} and V_{EE} side of the gate driver device.

4. Initiate the PWM switching signal (preferably 20 KHz or higher, 5V square-wave) to CON1's LED High signal pin, and observe the gate driving signal output across CON2 and CON3 through an oscilloscope.
5. If needed, UVLO, Fault and GFault feedback signals can be observed after UVLO, Desat and GFault faults are simulated, respectively.

Figure 1 Actual ACPL-352J Evaluation Board Showing Default Assembly





Descriptions of Evaluation Board Schematics and Its Various Functions

ACPL-352J is a 5.0A smart gate drive optocoupler. The high peak output current and wide operating voltage range make it ideal for driving SiC/GaN (or IGBT) directly in motor control and inverter applications.

The device features fast propagation delay with excellent timing skew performance. It provides SiC/GaN (or IGBT) gate driving capability with over current desaturation protection and functional safety reporting. This full-featured and easy-to-implement gate drive optocoupler comes in a compact, surface-mountable SO-16 package.

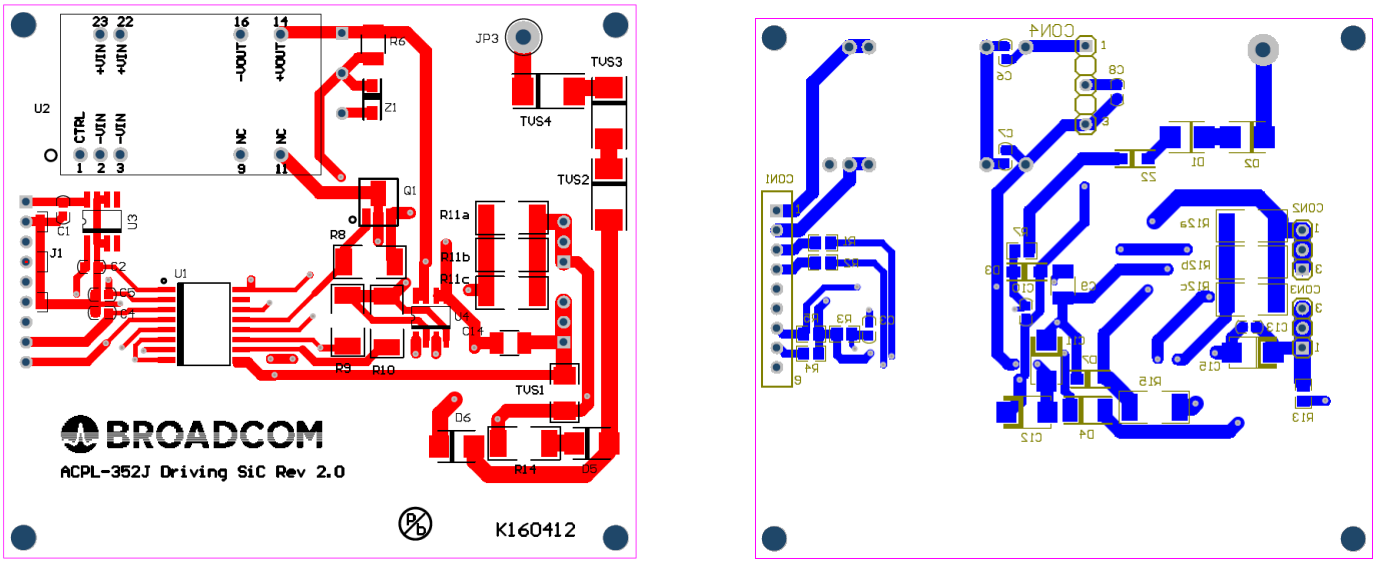
The evaluation board is specially designed to bring out the preceding outstanding features. It is designed to work with external 10A bipolar current buffer (U4) to drive up to 1200V/1000A rated SiC/GaN (or IGBT) power devices.

Full schematics of the evaluation board are as shown in Figure 3.

1. At least 50kV/µs of **HV Common Mode Rejection** are provided by the isolation barrier, and through a selection of 3:1 resistor ratio for R1/R2 for the LED current control.
2. In conjunction with U4, R11 and R12 are selected to **allow** both **turn-on and turn-off currents** to be set at the same 10A, assuming that the rise and fall times of SiC/GaN (or IGBT) are almost equal. Different R11 or R12 or both can be adjusted to catered for different rise and fall times.
3. Bidirectional TVS1 is selected to **protect** the **gate** of SiC/GaN (or IGBT) against **overvoltage** higher than 26V.
4. D1, D2, and Z2 are selected to **protect against** SiC/GaN (or IGBT) **drain desaturation** above 4V. Z2's Zener voltage needs to be adjusted if SiC/GaN (or IGBT)'s desaturation voltage needs to be higher (or lower) than 4V.
5. Schottky diode D3 is needed to **protect against** abnormal device behavior when **negative desaturation voltage** occurs at this pin-14.
6. Schottky diode D4 is used to allow for protection against SiC/GaN (or IGBT) **Miller false turn-on** during the off period.
7. The three pieces of unidirectional SMCJ440A (TVS2~4) are **Active Clamp** used to clamp against SiC Drain overvoltage above 1320V. When SiC drain voltage went above 1320V, the 3 TVS's will conduct and turn on the SiC instantaneously. Any excess energy that causes gate voltage higher than 20V will flow through D6 and D7. D6 and D7 are schottky diodes that provide a path for the excess Drain energy to be dumped back to the VCC capacitance for storage.

NOTE For other circuit functions at various pins of the Gate Driver device, refer to its data sheet.

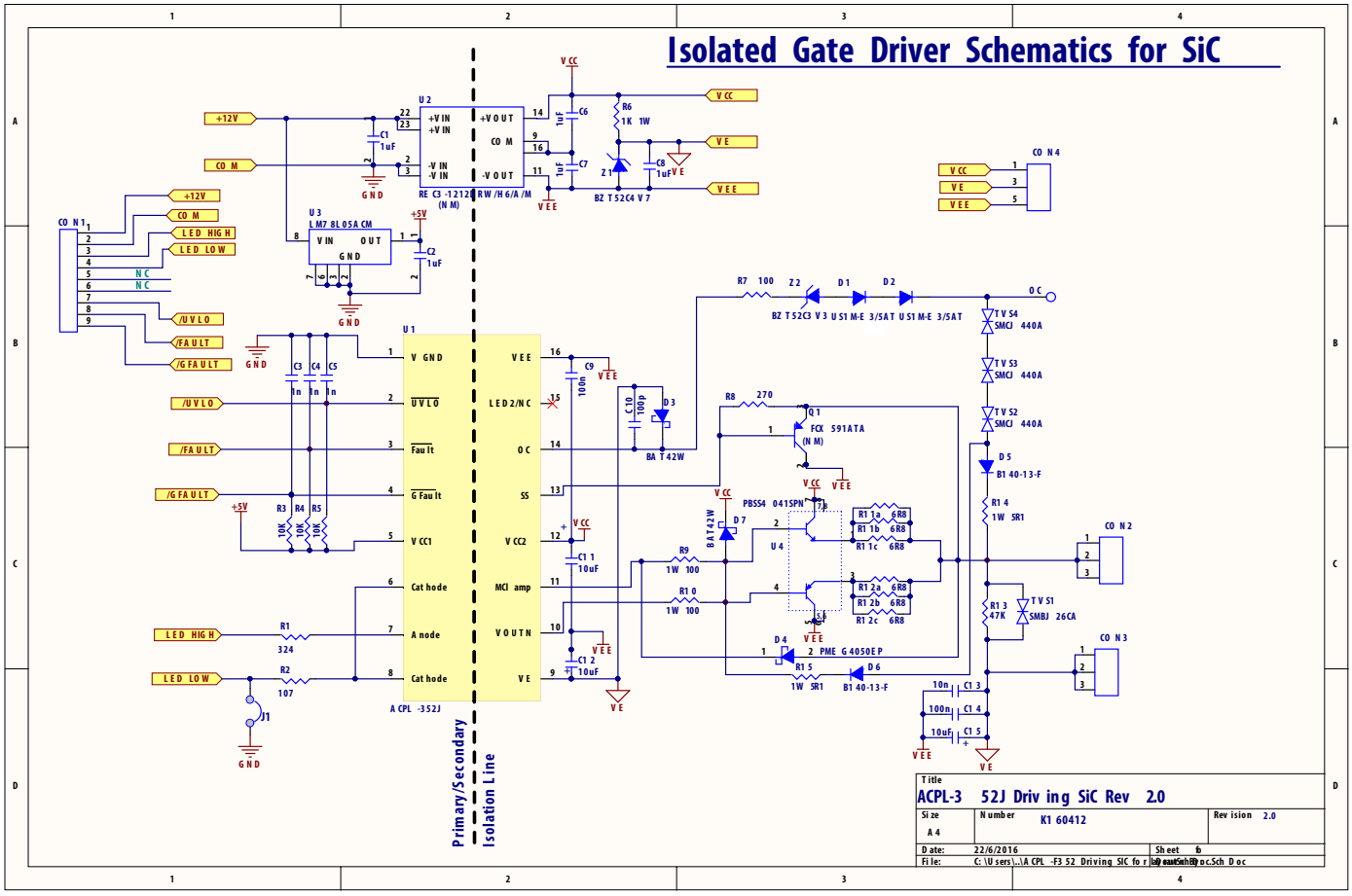
Figure 2 PCB Layouts of the Evaluation Board



Schematics

Schematics of the Evaluation Board are as shown in Figure 3.

Figure 3 Schematics of ACPL-352J Evaluation Board



Legends:

Pin-11 of ACPL-352J is also named as V_{OUTP}

The following signal names are used interchangeably in this document: Between V_{CC1} and V_{DD1}, Gnd and V_{SS1}, V_{CC2} and V_{DD2}, V_E and V_S, V_{EE} and V_{SS2}.

Application Circuit Description

Proper connections to test the evaluation board are as shown in the diagram below. Note, to get rid of unwanted high frequency noise, make use of proper PCB to solder all components as shown, including the evaluation board, SiC (rated at 1200V 1kA or below), CON1 and CON4 connections, and the three links linking evaluation board to the SiC. All connections should be as short as possible.

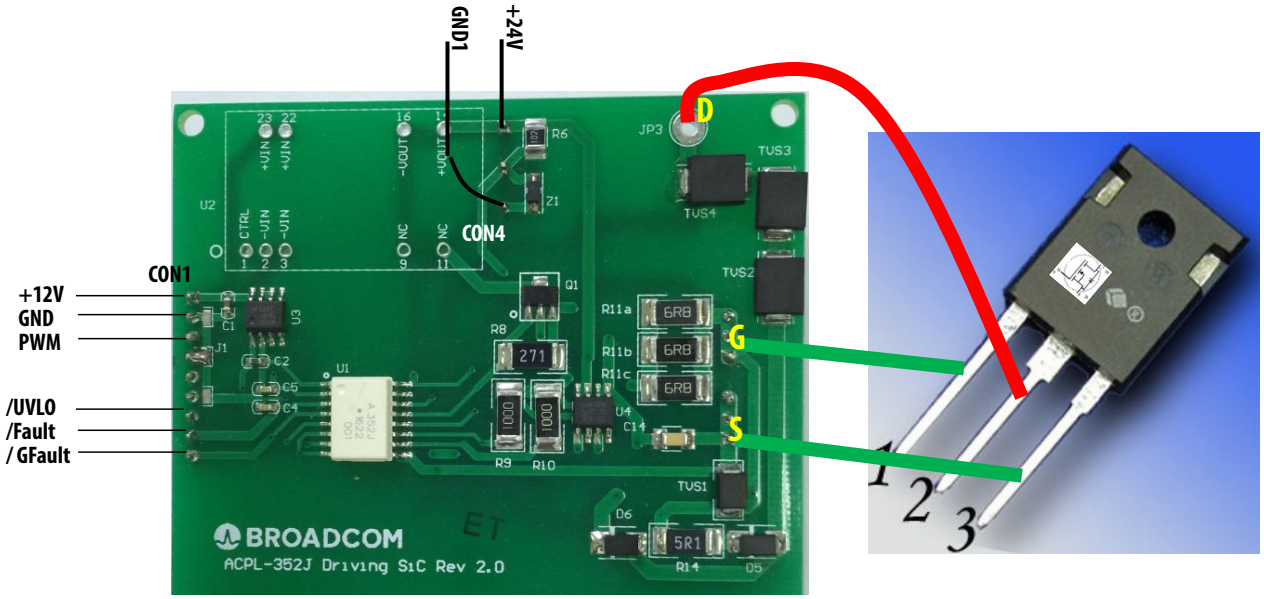
- Supply an isolated +12V across pin-1 and 2 of CON1, this will power up the isolated side when the internal regulator starts working.
- Supply a separate +24V supply across pin-1 and 3 at CON4, the U3 regulator will provide loosely regulated +19.3V and –4.7V supplies to V_{CC2} and V_{EE} respectively, wrt V_E.
- Connect CON2 and CON3 to G and S terminals of SiC, size of connections depends on drive current, and as short as possible.
- Connect/short JP3 to D terminal of SiC, as short as possible.
- Get the driving function to work by sending PWM signal across LED High and Gnd pins respectively. The signal levels should be +5V/0V wrt Gnd. Frequency should be at 20kHz, higher if SiC used is less than 1kA rated.
- Desaturation, UVLO and GFault faults can also be simulated.
- Fault signals at /UVLO, /Fault and /GFault can be monitored through a good industrial oscilloscope.

Other connections needed are HV DC Bus, Load connections and microcontroller, needed to program the PWM signal.

If SiC is not available, one can connect a 47nF capacitor across G and S terminals (and short JP3 to S terminal) to simulate a virtual 1kA SiC. Other simulation can follow the steps as shown above.

NOTE As can be seen on the board, the isolation circuitry (at the far left) is easily contained within a small area while maintaining adequate spacing for good voltage isolation and easy assembly.

Figure 4 Application Diagram of Evaluation Board



Output Measurement

A typical screen capturing the PWM input and output signal waveforms are as shown in Figure 5, using a 47nF capacitance as simulated SiC load. The output signals are showing Voutp/Clamp, Voutn and gate output across the 47nF capacitance (CON2 and CON3).

Figure 5 PWM Input Signal and Output Signal Waveforms

Figure 6 shows the /Fault signal when SiC Drain-Source short circuit is simulated.

Figure 6 /Fault Signal Reported when Drain-Source Desaturation/Short Circuit Occurs

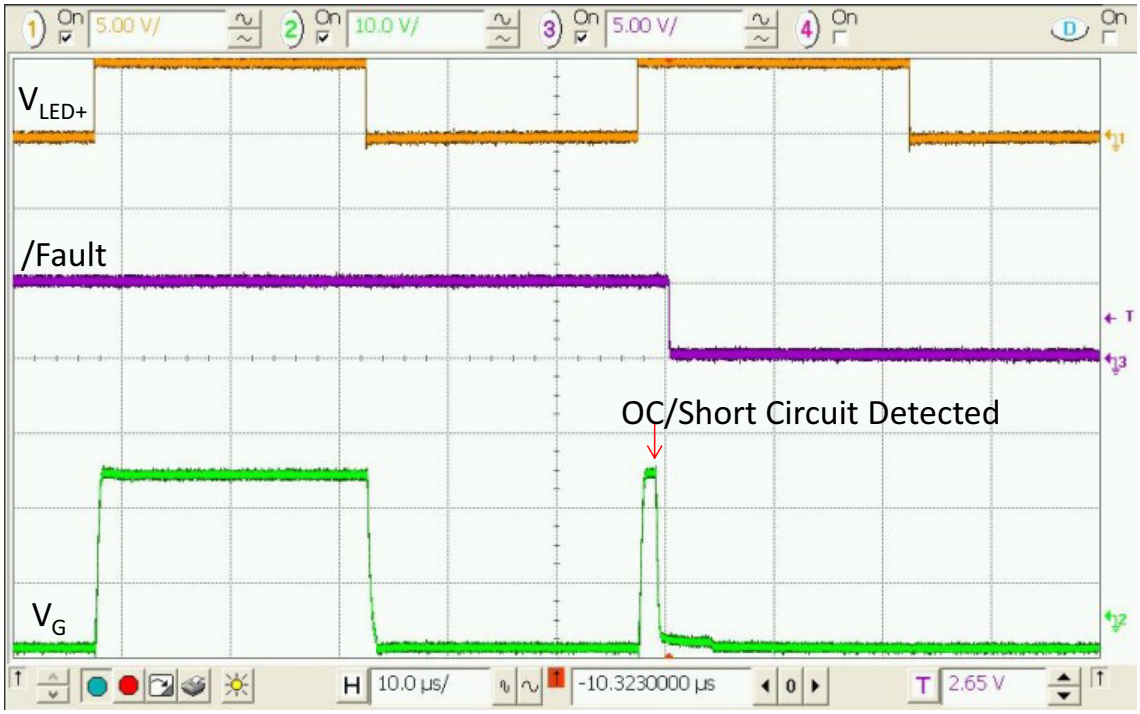


Figure 7 shows the /UVLO signal changes reported when V_{CC2} went down below UVLO- and recovers above UVLO+.

Figure 7 /UVLO Signal Changes when V_{CC2} Drops Below Regulation

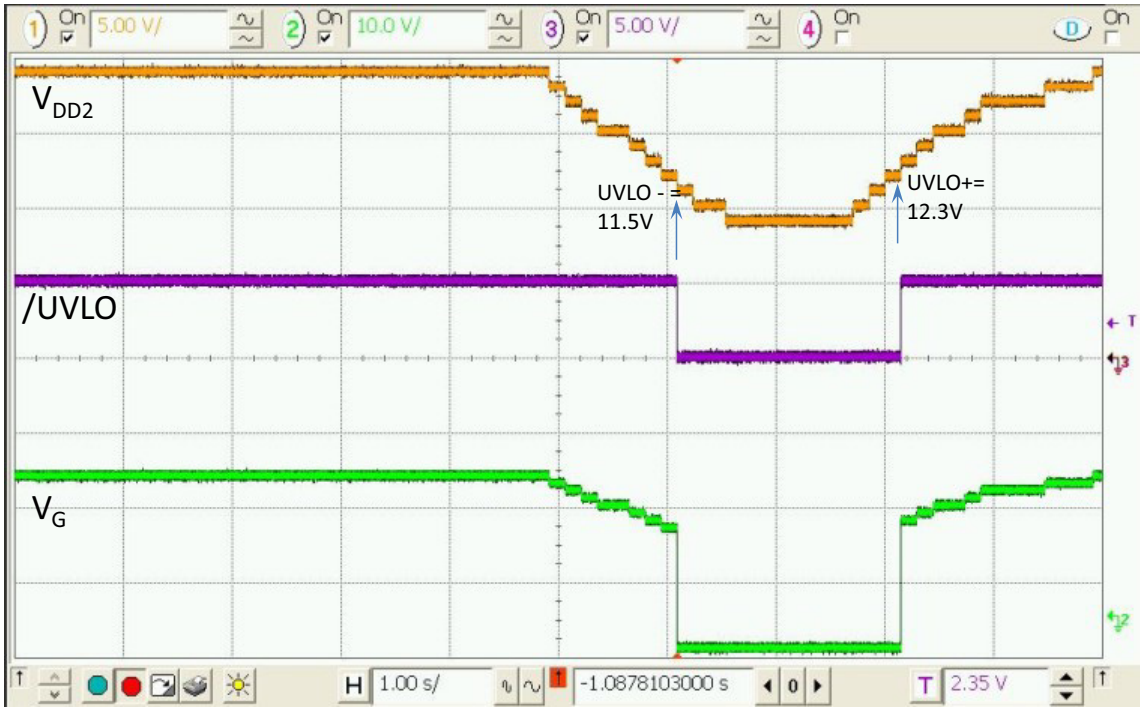


Figure 8 shows the /GFault signal reported when SiC Gate Fault is simulated. The left pane shows that /GFault signal is activated when $V_{GFaultn}$ could not recover higher than V_{CC2}–2V, while the right pane shows that /GFault signal is again activated when $V_{GFaultp}$ could not recover lower than V_{EE}+2V.

Figure 8 /GFault Signal Reported when Gate Fault Is Simulated

Note *1: C_{GF} used (1nF) is bigger than the 330pF recommended

*1: C_{GF} used (1nF) is bigger than the 330pF recommended

The preceding waveforms are captured/simulated with a 47nF capacitor instead of an actual SiC. But it is a close resemblance of the waveforms when actual SiC is used.

For product information and a complete list of distributors, please go to our web site:
www.avagotech.com

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