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Analysis of Power Dissipation and Thermal Considerations for High Voltage Gate Drivers

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APPLICATION NOTE

AND90004/D

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amount of power depending on the operating conditions. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits. High voltage gate drive IC (HVIC) is high side and low side gate drive IC designed for high−voltage, high−speed driving MOSFET for a half bridge switching application. Figure 1 shows the typical internal block diagram of HVIC. The main function blocks are the input stage, UVLO protections, level shifter and output driver stages. The gate driver losses include:

- Static losses related with static current at high and low side circuit blocks when driver is biased and not switching.
- Dynamic losses related with dynamic current when the switching signal is applied so linked to switching frequency.
- Gate driving losses related with load switch charges and also directly dependent on switching frequency.

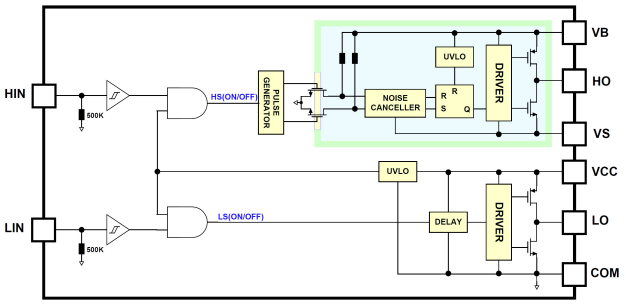


Figure 1. Block Diagram of HVIC

The bootstrap diodes losses will not be discussed in this document because the current flowing the diode will be included in dynamic losses. However, one thing not to be overlooked is the instantaneous power loss to charge the bootstrap capacitor during start up. During this time a significant current can flow through the diode to quickly charge the bootstrap capacitor and can generate relatively high losses during several switching periods. The bootstrap diode must withstand this current and power loss and this loss will add to driver internal power losses when this diode is.

Static Power Loss Analysis

The Figure 2 shows a simplified schematic of the half bridge switch network associated with high and low side driver to explain the static losses.

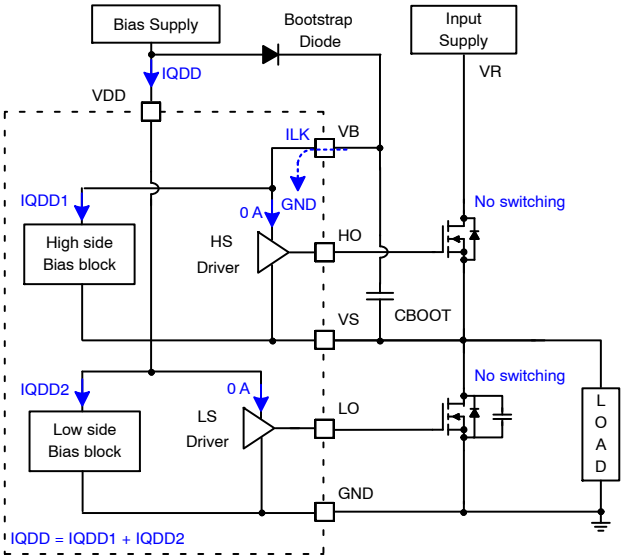


Figure 2. Simplified Circuit Diagram of Driver and Half−bridge Configuration for Static Power Losses

The static losses are due to the quiescent currents from dc voltage supplies V_{DD} to ground in the low−side driver and the leakage current in the level shifter in the high−side driver as described by the following equations.

$$P_{Static} = P_{Quiescent} + P_{Leakage} \quad \text{(eq. 1)}$$

$$P_{Quiescent} = V_{DD} \times I_{QDD} \quad \text{(eq. 2)}$$

$$P_{Leakage} = (V_R + V_{BOOT}) \times I_{LK} = (V_R + V_{DD} - V_{DBBOOT}) \times I_{LK} \quad \text{(eq. 3)}$$

Where, I_{QDD} is the quiescent current of V_{DD} supply under no input switching signal, V_{BOOT} is charged voltage on C_{BOOT}, V_{DBOOT} is the forward voltage drop on bootstrap diode, V_R is the rail voltage from input supply and I_{LK} is the leakage current at boot pin (VB pin in Figure 2). The static

power loss are permanent as soon as the driver is powered and not related to the frequency of the input signals.

However, most of power losses occur when the driver is turning *On* and *Off* the power switches. Hence, I_{QDD} is included in the operating current during switching mode, so $P_{Quiescent}$ should not be considered in this case. $P_{Leakage}$ should be considered in the case that I_{LK} is not small enough to be neglected and/or when V_{BOOT} level is very high such as in 1,200 V drivers. In case I_{LK} is not provided in the driver data sheet this loss can be ignored as it is generally small compared to others losses.

Dynamic Power Loss Analysis

Let's consider now the predominant loss sources. Figure 3 shows the circuit diagram of driver IC to address dynamic losses. The first dynamic loss is defined as the losses in the level shift (LS) in high side drive, P_{LS}.

$$P_{LS} = (V_R + V_{DD} - V_{DBOOT}) \times Q_{internal} \times f_{SW} \qquad \text{(eq. 4)}$$

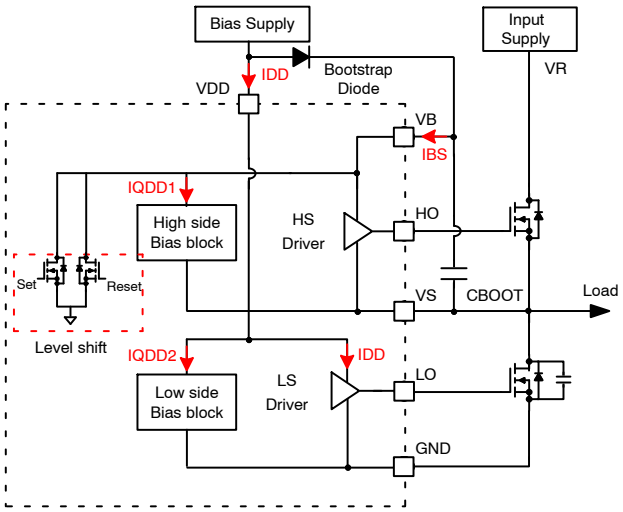


Figure 3. Simplified Circuit Diagram of Driver and Half−bridge Configuration for Dynamic and Power Losses

$Q_{internal}$ is the total gate charge of the internal LDMOS used in the level shift circuit. $Q_{internal}$ specification is not normally provided from manufacturer so not found in the datasheet. In this case as a rule of thumb $Q_{internal}$ value could be estimated around 0.6~1.5 nC for 600 V high side drivers and 0.4~1 nC for 100 − 200 V drivers. Some driver products using old technology might have relatively high $Q_{internal}$, so P_{LS} should be taken into account at high frequency operation, but in recent state of art drivers, this value is getting lower and lower so the losses can be neglected if no $Q_{internal}$ realistic value is available.

The second dynamic losses are related to operating current of output stage powered by V_{DD} and V_{BOOT} supply. While the output stages drive the external power devices, the dynamic loss (P_{OP}) is given by below equation.

$$P_{OP} = V_{DD} \times I_{DD} + (V_{DD} - V_{DBOOT}) \times I_{BS} \qquad \text{(eq. 5)}$$

I_{DD} is the operating current on V_{DD} and I_{BS} is the operating current at high side driver pin, VB. This power loss is resulting from internal current consumption under dynamic operating conditions. The internal current I_{DD} and I_{BS} should be determined under actual operating conditions referring to datasheet parameters taking into account switching frequency.

If the datasheet doesn't provide I_{DD} and I_{BS} curve versus switching frequency, the following method is recommended to calculate I_{DD} and I_{BS} for given operating conditions.

If I_{DD} (or I_{BS}) is defined at 20 kHz (F_{SW_DS}) without load, the I_{DD} (or I_{BS}) at 100 kHz (F_{SW}) is about 5 times larger than 20 kHz because it is proportional to switching frequency.

For more accurate calculation, subtract the quiescent current from I_{DD} or I_{BS} before multiplying 5.

For example, the operating current at 20 kHz (I_{PDD}) is 0.5 mA and the quiescent current (I_{QDD}) is 0.05 mA in the datasheet, I_{DD} at 100 kHz is calculated with below equation.

$$I_{DD} = (I_{PDD} - I_{QDD}) \times (F_{SW}/F_{SW\_DS}) + I_{QDD} =$$
$$= 0.45\ mA \times 5 + 0.05\ mA = \qquad \text{(eq. 6)}$$
$$= 2.25\ mA \times + 0.05\ mA = 2.3\ mA$$

F_{SW} is target frequency and F_{SW_DS} is specified frequency in the datasheet.

If I_{DD} (or I_{BS}) is specified in the datasheet with a load condition such as 1 nF capacitance, then you can eliminate the current effect of 1 nF capacitance using below equation.

$$I_{DD} = \left(I_{PDD} - \left(C_{LOAD} \times V_{DD} \times F_{SW\_DS}\right) - I_{QDD}\right) \times$$
$$\times \left(\frac{F_{SW}}{F_{SW\_DS}}\right) + I_{QDD} \qquad \text{(eq. 7)}$$

C_{LOAD} is specified capacitance of load in the datasheet.

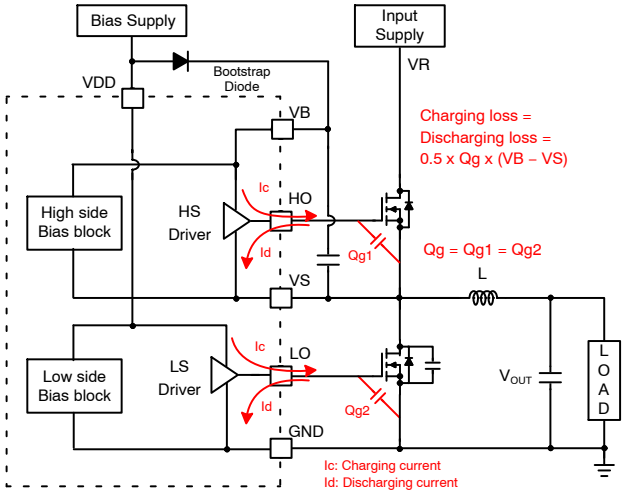


Figure 4. Simplified Circuit Diagram of Driver and Half−bridge Configuration for Gate Driving Power Losses

Gate Driving Loss Analysis

The gate driving loss in the driver is the most significant power loss resulting from supplying gate current to switch the load MOSFET *On* and O*ff* at the switching frequency. The gate driving losses are coming from charging and discharging the load capacitor (for MOSFET, the load capacitor is the input capacitor of MOSFET) and expressed by the following equation.

$$P_{charging} = P_{discharging} = 0.5 \times V_{DD} \times Q_g \times f_{sw} \quad \text{(eq. 8)}$$

Where, Q_g is the total gate charge of the external MOSFET and f_{sw} denotes the switching frequency. In case of a soft switching topology, Q_g is equal to gate to source charge (Q_{gs}) of the FET or IGBT. The total gate driving losses in high and low side drivers is then 4 times $P_{charging}$.

$$P_{gate\_driving} = 2 \times V_{DD} \times Q_g \times f_{sw} \quad \text{(eq. 9)}$$

Since the major power loss is the gate driving loss, the simplest and fastest way to calculate the losses in a driver is to sum the gate driving loss (P_{gate_drving}) and dynamic losses on V_{DD}.

These losses acount for more than 90% in recent middle voltage class high and low side driver products.

Thermal Analysis

Once the power dissipated inside the driver is calculated, we can estimate the junction temperature of the driver. This can be evaluated assuming thermal resistance or characterization was determined for a similar thermal design (heat sinking and air flow). The thermal equation is:

$$T_J = P_{TOTAL} \times R_{jx} + T_x \quad \text{(eq. 10)}$$

Where:

T_J = the junction temperature of driver die

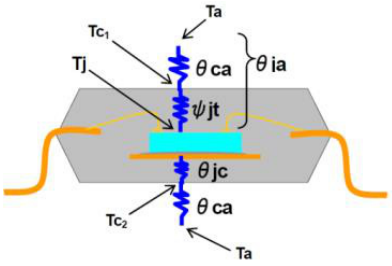
R_{jx} = thermal resistance (θ) or characterization parameter (Ψ) relating temperature rise to total power dissipation

T_x = temperature of point x as defined in the thermal characteristic table from datasheet.

The thermal information is shown in Figure 5 and Table 1. Thermal characteristic of the package is a function of several parameters such as geometry, boundary condition, test condition, etc. This requires numerical analytical tool or modeling technique that are generally cumbersome to manipulate. It can be tricky to estimate the junction temperature precisely with thermal information coming from datasheet.

So it is helpful to review the definition of thermal information.

1. θja is the Junction−to−Air Thermal Resistance. It measures theheat flow between the die junction and the air. It is mainly relevant for packages used without any external heat sink.
2. θjc is the Junction−to−Case Thermal Resistance and it measures the heat flow between the die junction and the surface of the package. It is mainly relevant for packages using some external heat sinks
3. Ψjt is the Junction−to−PKG Top Thermal Characterization Parameter and it provides correlation between die temperature and temperature of package topside. This can be used to estimate die temperature in applications
4. Ψjb is the Junction−to−Board Thermal Characterization Parameter and it provides correlation between die temperature and board temperature. This can be used to estimate die temperature in applications.



$$\theta ja = \frac{Tj - Ta}{Pd}$$

$$\psi jt = \frac{Tj - T_{C1}}{Pd}$$

$$\theta jc = \frac{Tj - T_{C2}}{Pd}$$

Figure 5. Thermal Resistance and Characterization Parameters with Package

Table 1. DEFINITION OF THERMAL RESISTANCE AND CHARACTERIZATION PARAMETERS

Item	Definitions
θja	Thermal resistance between Tj and Ta
Ψjt	Thermal characterization parameter between Tj and T_{C1}
θjc	Thermal resistance between Tj and T_{C2}
θca	Thermal resistance between Tc and Ta
Tj	Junction temperature
Ta	Ambient temperature
T_{C1}	Temperature of the top surface of IC package
T_{C2}	Temperature of the bottom surface of IC package
Pd	Maximum permissible powe

Generally, the thermal information provided in semiconductor datasheet can't cover all applications cases. For the following examples we'll only use θja for Tj calculation.

For more details on how to properly use thermal data found in datasheet, please refer to detailed Application notes: www.onsemi.com/pub/Collateral/AND8220−D.PDF.

Recommendations to Reduce T_j

In case Tj is too close to the recommended operating temperature, there are few things that could be considered.

1. Add external gate resistors to distribute the power losses: When no external gate resistor is inserted between the driver and MOSFET, the power is entirely dissipated inside the driver package. Using external gate resistor allows to share the power

losses between the internal gate resistance of driver and the inserted external resistor. The split is given by the ratio between the 2 resistors. The higher the external gate resistor is the less power dissipation happen inside the driver.

2. Reduce the switching frequency. The switching frequency is affecting most of the power losses so it could help whenever the application allows it.
3. Use heat sink. Enlarge PCB area and add more copper around the driver.
4. Reduce supply voltage VDD if possible. Latest generations of drivers and MOSFET's offer this option.

Reducing the switching frequency or supply voltage is not always possible and enlarge the PCB or add heat dissipation means is often limited. Most of the time one uses external gate resistors for various reasons such as limit ringing caused by parasitic or high dV/dt, tune gate drive strength to reduce EMI. This also has an impact on the power losses distribution. By adding external gate resistor, the gate driving power loss will be calculated as follow:

$$P_{sw} = Q_g \times V_{DD} \times f_{sw} \times \left(\frac{R_{ON}}{R_{ON} + R_{gon}} + \frac{R_{OFF}}{R_{OFF} + R_{goff}} \right) \quad \text{(eq. 11)}$$

Where, R_{ON} and R_{OFF} are the resistance value of internal pull up and down structures and R_{gon} and R_{goff} are the external gate resistors. Simply, if $R_{ON} = R_{OFF} = Rg$, the Psw will be the half of the total power dissipation compared to no external gate resistance.

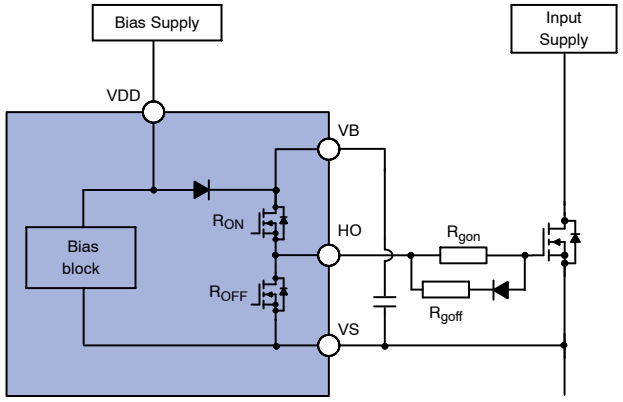


Figure 6. Internal Pull Up and Down Resistance

As an illustration for NCV51511, R_{ON} is 2 Ω and R_{OFF} is 1 Ω from the calculation of Vdd/peak pull up (or down) current. If 1 Ω is inserted between output pin and the MOSFET gate, the gate driving losses is down to 83%.

Power Dissipation in the Level Shift Circuit

Figure 7 shows the typical internal block diagram associated with level shift and timing diagram. To maintain high efficiency operation and manageable power dissipation, the level shifters should not draw any current during the on−time of the main switches. The level shift shown in Figure 7 (a) is widely used technique called pulsed latch level transistors.

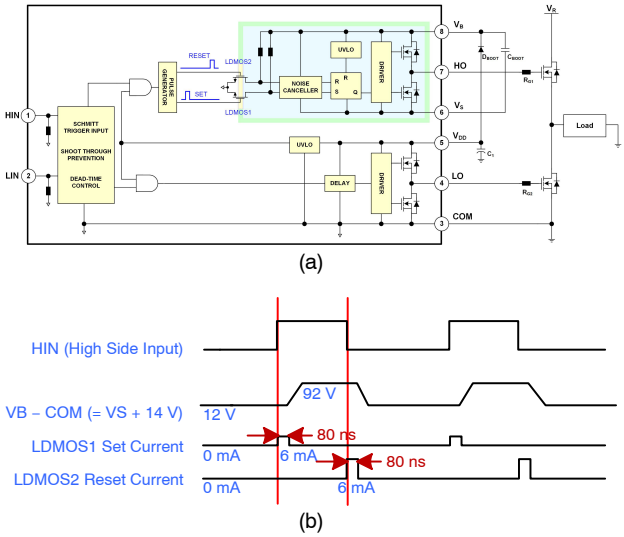


Figure 7. (a) Typical Internal Block Diagram of HVIC. (b) Associated Waveform of Level Shift

To calculate the power dissipation in the level shifter, we assume the test conditions are the same as NCV51511 case study: Temp = 25°C, V_{DD} = 12 V, V_{DBOOT} = 1 V, V_R = 80 V, Freq = 100 kHz, T_{on} = 80 ns, and I_d = 6 mA for level shift circuit.

Q_p of Set and Reset can estimated

$$SetQ_P = Isubd \times T_{ON} = 6\ mA \times 80\ ns = 0.48\ nC \quad \text{(eq. 12)}$$

$$ResetQ_P = Isubd \times T_{ON} = 6\ mA \times 80\ ns = 0.48\ nC \quad \text{(eq. 13)}$$

From the Q_p, the power dissipation for the case of set and reset period.

$$P_{D,set} = (V_{DD} - V_{DBOOT}) \times Q_P \times Freq = 11\ V \times 0.48\ nC \times \times 100\ kHz = 0.57\ mW \quad \text{(eq. 14)}$$

$$P_{D,reset} = (V_R + V_{DD} - V_{DBOOT}) \times Q_P \times Freq = 91\ V \times \times 0.48\ nC \times 100\ kHz = 4.37\ mW \quad \text{(eq. 15)}$$

The total power dissipation of level shift is the sum of $P_{d,set}$ and $P_{d,reset}$. Here, $P_{d,set}$ is significantly smaller than $P_{d,rest}$, we can ignore $P_{d,set}$ and simply take into account $P_{d,rest}$.

Application to NCV51511

NCV51511 power loss calculation and thermal estimation will be developed in this section. The total power dissipation is calculated under below conditions:

- Ambient temperature: 25°C
- V_{DD} = 12 V and V_R = 80 V
- Switching frequency = 100 kHz
- Gate resistance R_g = 0 Ω
- Q_G of external MOSFET is 80 nC
- $Q_{internal}$ = 0.48 nC
- V_{DBOOT} = 1 V
- I_{LK} = 10 μA

The circuit implementation is depicted in Figure 8.

1. Static losses are calculated by leakage current in the level shift stage at VB pin.

   $$P_{Leakage} = (80\ V + 12\ V - 1\ V) \times 10\ \mu A = 0.1\ mW$$

   This static loss in high side section can be ignored as the leakage current is small and V_{BOOT} is low for this driver.

2. Dynamic losses can be estimated by the level shifting circuit and operating the operating current associated with internal CMOS circuitry.

   $$P_{LS} = (80\ V + 12\ V - 1\ V) \times 0.48\ nC \times 100\ kHz =$$
   $$= 4.368\ mW$$

   The dynamic loss on level shift is described in the appendix in detail. To calculate this power loss exactly, the key information normally not shown in the datasheet are needed such as gate charge of high voltage MOSFET for level shift ($Q_{internal}$). This power loss is not completely negligible, but the amount of power is still small.

   $$P_{OP} = 12\ V \times 0.5\ mA + 11\ V \times 0.5\ mA = 11.5\ mW$$

   The operating current must be taken as shown in datasheet characteristic curve like the Figure 8 considering the frequency and load capacitance

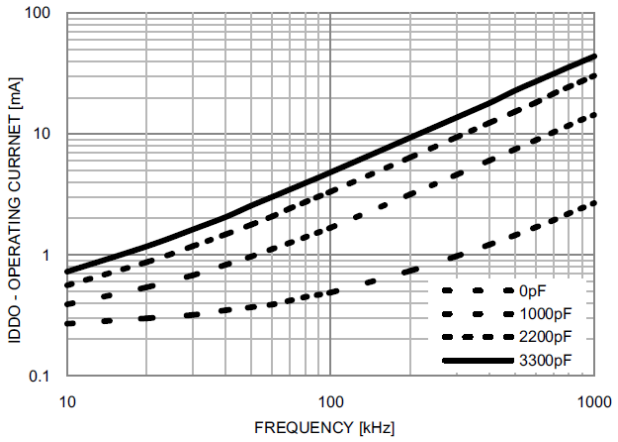


Figure 8. I_{DD} Operating Current vs. Frequency

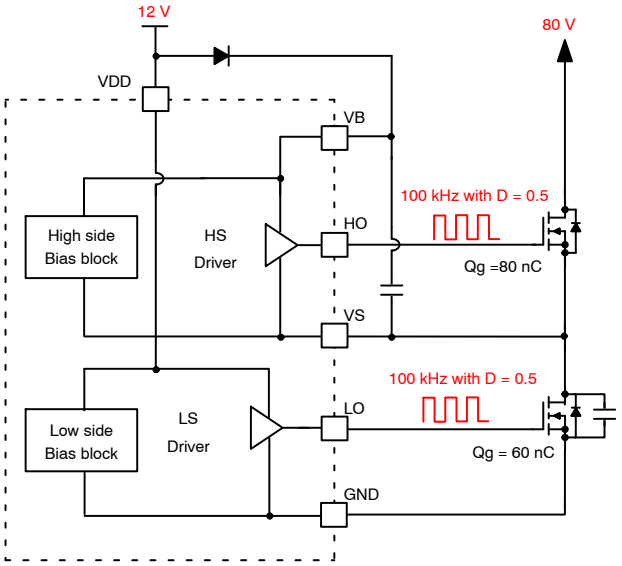


Figure 9. Half−bridge Configuration for the Case Study

3. Gate driving losses can be calculated by

   $$P_{gate\_driving} = 2 \times 12\ V \times 80\ nC \times 100\ kHz$$
   $$= 192\ mW$$

4. Total power losses is the summation of 1 and 2 and 3.

   $$P_{total} = P_{Leakage} + P_{LS} + P_{OP} + P_{gate\ driving} =$$
   $$= 0.9\ mW + 4.4\ mW + 11.5\ mW + 192\ mW =$$
   $$= 208.8\ mW$$

The total power dissipation of NCV51511 in this operating conditions is 209 mW and the majority of power loss comes from gate driving loss that represents 92% of power loss and 5.5% power loss is generated by dynamic losses at VDD and VB pin. So 97.5% power losses can be obtained by the following.

$$P_{(97\%\ of\ total)} = 2 \times V_{DD} \times Q_g \times f_{sw} + V_{DD} \times (I_{DDO} + I_{BSO}) \quad \text{(eq. 16)}$$

All parameters to calculate about 97% power dissipation could be quickly found in the datasheet and the application conditions. So as a rule of thumb, the total IC power dissipation could be gate driving loss neglecting the static losses and level shift loss in middle voltage gate driver.

Once the power dissipation is estimated, the junction temperature can be predicted using the thermal resistance described in the datasheet. The Table 2 shows the thermal characteristics of NCV51511 that is housed into SOIC−8 package with exposed pad (EP). EP can certainly improve the thermal performance hence the thermal resistance is way smaller than standard SOIC−8. The thermal resistance of junction to air (θ_{JA}) of NCV51511 is 39°C/W while the general SOIC−8 is between 150~200°C/W.

Table 2. THERMAL INFORMATION OF NCV51511

Symbol	Parameter	Value	Unit
θJA	Thermal Resistance Junction−Air*	39	°C/W
ΨJL	Thermal characterization parameter Junction−Lead	15	°C/W
ΨJT	Thermal characterization parameter Junction−Case (TOP)	6	°C/W

*As mounted on a 76.2 x 114.3 x 1.6 mm FR4 substrate with a Multi−layer of 1 oz copper traces and heat spreading area. As specified for a JEDEC 51−7 conductivity test PCB. Test conditions were under natural convection or zero air flow

These thermal information offers various approaches to estimate junction temperature using following equations when the ambient, package lead or case top temperature are measured or given. It could be that there would be small difference between the calculation and real junction temperature. Measurement set up from the information of datasheet (JEDEC) is not identical to the real application such as the PCB material and trace copper thickness and area or even the number of total PCB layer but still it gives a close enough estimation to help designers to know the thermal margin they have.

- Total power dissipation = 209 mW.
- If θ_{JA} and Ta are given

  $T_J = 0.21 \times 39 + Ta = 8.19 + Ta\ (°C)$
- If Ψ_{JL} is known and lead temperature can be measured (T_{Lead})

  $T_J = 0.21 \times 15 + T_{Lead}\ °C = 3.15 + T_{Lead}\ (°C)$
- If Ψ_{JT} is known and case−top temperature can be measured (T_{Top})

  $T_J = 0.21 \times 6 + T_{Top}\ °C = 1.26 + T_{Top}\ (°C)$

This estimation of the junction temperature (Tj) provide useful guidance to take any action if Tj is getting too close to the max recommended operating temperature range described in the datasheet.

Application to FAN73912

A final example is FAN73912 and operating conditions are as below

- V_{DD} = 20 V and V_B = 800 V
- Switching frequency = 20 kHz
- Gate resistance $R_g = 0\ \Omega$
- Q_G of external MOSFET is 10 nC
- $Q_{internal}$ = 2 nC
- V_{DBOOT} = 1 V
- $I_{LK} = 50\ \mu A$

1. Static losses

   $P_{Leakage} = (800\ V + 20\ V - 1\ V) \times 50\ \mu A =$

   $= 40.95\ mW$

   The leakage current are specified in the datasheet as I_{SD}.
2. Dynamic losses

   $P_{LS} = (800\ V + 20\ V - 1\ V) \times 2\ nC \times 20\ kHz =$

   $= 32.8\ mW$

   $P_{OP} = 20\ V \times 0.1\ mA + 19\ V \times 2\ mA = 40\ mW$
3. Gate driving losses

   $P_{gate\_driving} = 2 \times 20\ V \times 10\ nC \times 20\ kHz = 8\ mW$
4. Total power losses

   $P_{total} = P_{Leakage} + P_{LS} + P_{OP} + P_{gate\ driving} =$

   $= 40.95\ mW + 32.8\ mW + 40\ mW + 8\ mW =$

   $= 121.75\ mW$

The total power dissipation is 121.75 mW and θ_{JA} shows with 95°C/W for 14SOIC.

θ_{JA} and Ta are given

$T_J = 0.122 \times 95 + Ta = 11.6 + Ta\ (°C)$

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