LOGIC APPLICATION HANDBOOK

PRODUCT FEATURES & APPLICATION INSIGHTS

Design Engineer's Guide

nexperia

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Product Features and Application Insights

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Preface

Nexperia is a leading expert in diodes, bipolar transistors, ESD protection devices, MOSFETs, GaN FETs and analog & logic ICs.

With an absolute focus on efficiency, Nexperia consistently produces the essential semiconductors required by every electronic design in the world: more than 90 billion annually. Products that are benchmarks in efficiency — in process, size, power and performance — with industry-leading small packages that save valuable energy and space.

Our extensive portfolio of standard functions meets both the demands of today's state-of-the art applications and the stringent standards set by the Automotive Industry. Through our continued efforts in innovation, reliability and support, we maintain the leading position in all our key product segments: Diodes and Transistors, ESD protection, MOSFETs, and Analog and Logic ICs. We develop and deliver benchmark solutions for today's and tomorrow's market requirements, drawing on a heritage of over 60 years' expertise in Semiconductors as the former Standard Products divisions of NXP and Philips.

Our successful record in innovation is the result of varied yet streamlined R&D. We combine the latest technologies with efficient processes, helping us to serve the world's most demanding industries with world-class products.

Nexperia Design Engineer's Guides:
Our program of Design Engineer's Guides has one key goal: We want to share our Expertise with you and help you to optimize your electronic designs. It is a collection of technical and application insights "from Engineer to Engineer".

The first Nexperia Design Engineers Guide, released in 2017, is our *MOSFET Application Handbook*. In this handbook, our engineers focus on how to use MOSFETs in specific applications and what the key and critical MOSFET parameters are, considering aspects like thermal conditions etc.

The Second Technical Guide of this series was launched in 2018: Our *ESD Application Handbook*. This ESD Application Handbook is focusing on Protection Concepts, Testing and Simulation for Modern Interfaces. We got so far a lot of positive feedback by our Engineering Community from Customers representing all Industries word wide. In addition to this ESD Application Handbook, Nexperia is also offering on-site Technical ESD Seminars to share our insights with our customers, cross all relevant applications like Automotive, Mobile Communication, Consumer, Computing and Industrial. At the end we want to help minimize the risk of ESD

damage — supporting the design community in protecting applications and products against ESD issues. Both Design Engineer's Guides are also available in Chinese Version.

Introducing the Logic Application Handbook
"Why a Logic Handbook?" You may ask. Well, even though logic may have been around since the days when engineers still used slide rules, today logic is still an essential part of many embedded designs.

Of course, it is the go-to resource for I/O expansion and interfacing between analog and digital domains, but in many ways, today's designers need logic more than ever. Why? Because today's systems need to be smaller, more power efficient, and more portable than ever before. That means managing tight layouts, and dealing with looped traces, which can generate cross-talk and create signal-integrity issues. It also means working with multi-layer boards, implementing real-time responses to real-world events, and supporting multitasking operations. In many cases, the right logic device makes these things easier to manage, and helps optimize operation.

In fact, while Logic is great for making these kind of minor modifications and fine-tuning performance in the later design stages, that's not all it can do! Today's logic devices let developers add features and improve functionality, so they can meet their design requirements right from the start, even before they need to think about last-minute revisions.

- In systems that use application-specific integrated circuits (ASICs), logic gates can be used to provide control or "glue" functions. Modern logic families include features, such as overvoltage tolerance, that enable them to be used as glue logic between ASICs that use different supply voltages. In some cases, this can extend the lifetime of legacy ASICs.
- In systems that use a microcontroller (MCU), logic products are used for low-cost I/O expansion. Shift registers are used for digital I/O expansion, and analog switches are used to multiplex analog sensor inputs. The combination of the two enables the selection of lower-pin count MCUs with fewer analog-to-digital converters. When used this way, standard logic enables true cost optimization of an application.
- In tablets and laptops, logic can be used for battery charging and discharging blocks, and to provide standby mode, power-down, and start-up control sequences. In docking stations and systems that support multiple displays, logic provides the bus switches, resets, and audio blocks that reduce the impact of noisy signals, and can be used to buffer the clock and data signals.

- In mobile devices such as smartphones, tablets, and cameras, logic provides multiplexing, buffering, and level-translation functions for the baseband, RF interfaces, memory, and other peripherals.
- In external speakers and other high-end audio equipment logic buffers are used to buffer the clock, sync, and data signals sent to the audio interface and docking station.

Over the last 60 years, Nexperia — starting as Philips Semiconductors and then incorporating the experience of Signetics — has supported growing global demand for logic. Today, as the No. 1 volume logic supplier in the world, Nexperia offers a broad variety of industry-leading solutions proudly serving customers across a variety of market segments. Our reputation as a trusted supplier of exceptionally high quality is reinforced by our No. 1 position in the automotive industry.

We proudly invite you to study our 3rd Nexperia Design Engineer's Guide, our *Logic Application Handbook*. The Table of Content makes it easy for you to navigate to the key chapters of interest. This book is another key milestone to build the Technical Nexperia Encyclopedia.

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Nexperia

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Chapter 1

Introduction

Nexperia logic history begins with some of the very first integrated logic devices in the 1970's with the acquisition of Signetics. Nexperia technology is built upon decades of logic development and research over the years from Signetics, Philips, NXP and Nexperia.

Nexperia's logic portfolio is already very extended and will grow further. A general document for supporting the application of discrete logic devices, covering all important aspects of applications design, is very useful for engineers and helps to establish a common understanding for both Nexperia and the customers.

This handbook is dedicated to application and design engineers who are developing and using electronic circuits, often within embedded systems for all kind of applications. The demand for discrete logic devices is widespread. Many aspects of system and board design have to be addressed and the usage of logic devices is very often generating questions and support requirements which cannot be met just by data sheets. In order to provide a compact and handy document, condensed from application notes, customer support experience and general logic knowledge, this book is meant to support development engineers who are dealing with logic devices.

Digital systems are running at faster speeds, operating at lower voltages, and they are becoming more integrated. Many functions can be integrated into FPGAs or ASICs/SOCs, however, this does not mean that generic standard logic will disappear. Designers may choose to design with standard logic for the following reasons:

- The addition of features in next generation products with lower power consumption
- Space constraints requiring small packaging
- Bus driving capability
- Interfacing between mixed voltage systems and voltage level translation
- Need for hot insertion capability
- Need for bus switching.
- Need for I/O expansion of embedded systems

To create a content suitable for application engineers using Nexperia's logic devices, we are trying to take the designers point of view.

Each chapter of the book is addressing aspects of designing with logic devices and the systems they are used in. We start with basics of logic theory and circuit elements: logic equations, binary code and basic logic functions are introduced as well as circuit design aspects like CMOS gate implementations. The explanation of data sheet items is addressed and the associated properties of logic process families.

Another aspect is the power consumption of logic devices in embedded circuits, here we provide the calculation methods and explain the dependencies on process technology and topology.

As well as power, timing behavior needs to be calculated and must be understood for a circuit design. In the timing chapter, we deliver information and explanations for this.

Many behavioral aspects of logic devices need to be addressed when using them interfacing other devices. These effects are explained in the chapter Interfacing Aspects.

Background information about package types, soldering and footprints are provided in an extra chapter Package. For further system integration items like Simulation of PCB design we have created an extra chapter to enable users to successfully integrate Nexperia's logic devices into their embedded systems and verify the system before production.

The logic process families and their specific properties are addressed in another chapter with information about I/O characteristics and all technology specific information useful for selecting the suitable process family for a dedicated function.

Finally, frequently asked questions from customers are compiled in a chapter to address the most popular support issues.

Chapter 2

Logic basics, Generic Logic product properties

Digital electronic data processing uses binary numbers. Only two states exist, zero and one. These states are also referred to as true and false. In electronics input voltage ranges are defined to represent a logic low (zero) and a logic high (one). Logic products can have inputs that are described as active high or active low. An input where 1 = true is said to be an active high input whereas an input where 0 = true is said to be an active low input.

Binary code

The binary numeral system is a positional numeral system with a base or radix of 2. The single digits in a binary system are represented by 2^n with $n \geq 0 \rightarrow 2^0, 2^1, 2^2, 2^3, 2^4 \ldots$, in decimal = 1, 2, 4, 8, 16 …

Below an example how a decimal number is converted to a binary number:

$$1317_{(10)} = 1 * 2^{10} + 0 * 2^9 + 1 * 2^8 + 0 * 2^7 + 0 * 2^6 + 1 * 2^5 + 0 * 2^4 + 0 * 2^3 + 1 * 2^2 + 0 * 2^1 + 1 * 2^0$$

$$1317_{(10)} = 10100100101_{(2)}$$

Each digit of a binary number is referred to as bit in logic nomenclature. Standard calculations like adding, subtraction, multiplication and division work identical to decimal system. For example adding two numbers the digits can be added sequentially while taking care of carry bits from the single operations.

Below the example of adding 1011 plus 0011 (decimal: 11 + 3). Starting from the lowest bit 1+1 is 0 plus a carry of 1 to the next digit. 1+1+1 is 1 plus a carry again. In the next digit there is the 1 of the carry plus 0, so 1 as result. For the highest digit 1 + 0 delivers 1.

```
          1 0 1 1
        + 0 0 1 1
Carry bits ► 1 1
          1 1 1 0
```


Boolean Algebra

For elementary algebra expressions are noted down in numbers normally. In Boolean algebra the truth values *false* and true are used. These values can also be denoted with bits or binary digits, represented by logical 0 or 1.

Basic Operations in Boolean algebra are the AND and OR operation as depicted in Table 1. The AND operation delivers a true or 1 as result if all input values are equal 1. For the two input variable example both A and B need to be equal 1 for a result of 1, all other combinations deliver the result 0.

For the OR operation, all inputs need to be 0 to get a 0 as result. If at least one input variable is 1 or true, the OR operation delivers a 1.

Table 1: Basic Boolean operations AND and OR with 2 input values A and B

		AND	OR
A	B	A^B	A˅B
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1

The AND and OR operation works in the same way if more than 2 variables are involved.

An additional very important Boolean operation is the inversion. It is quite simple as Table 2 shows. A zero input variable results in a result of 1 and vice versa for a 1 as input.

Table 2: Boolean operation of Inversion

A	$\overline{A}$
0	1
1	0

Boolean algebra is identical for many rules if the operation ˅ (OR operation) is replaced by an addition and the operation ^ (AND operation) by a multiplication. The following laws known from normal algebra are common with Boolean algebra and called the monotone laws.

Associativity of ^ . . . . . A^(B^C) = (A^B)^C
Associativity of ˅ . . . . . A˅(B˅C) = (A˅B)˅C
Commutativity of ^ . . . . . A^B = B^A
Commutativity of ˅ . . . . . A˅B = B˅A
Distributivity of ^ over ˅ . . . . . A^(B˅C) = (A^B)˅(A^C)
Identity rule for ^ . . . . . A^0 = 0
Identity rule for ˅ . . . . . A˅1 = 1

There are additional laws that are valid in Boolean algebra but do not exist in normal algebra:

Annihilation of ˅ . . . . . A˅1 = 1
Idempotence of ^ . . . . . A^A = A
Idempotence of ˅ . . . . . A˅A = A
Absorptions rules . . . . . A˅(A^B) = A
. . . . . A^(A˅B) = A
Distributivity of ˅ over ^ . . . . . A˅(B^C) = (A˅B)^(A˅C)

The complementation rules are.

$$A \wedge \bar{A} = 0 \qquad A \vee \bar{A} = 1$$

A very important rule is the so called de Morgan law. It can be used to optimize and restructure logic designs. If inverted inputs are processed with an AND operation this is identical to process these variables via an OR operation and to invert the result. The same law can be applied if you process inverted input variables with an OR operation. It is identical to have an AND operation for the variables and to invert the result.

De Morgan laws:

$$\bar{A} \wedge \bar{B} = \overline{(A \vee B)} \qquad \bar{A} \vee \bar{B} = \overline{(A \wedge B)}$$

Where:
^ = logic AND, ˅ = logic OR

2.1 Basic logic gate functions

Inverter/ NOT Gate

The most simple gate function is the inverter. Below is the simple logic table of an inverter.

Table 3: Inverter or NOT Gate

Input A	Output Y
0	1
1	0

There are two styles of symbols commonly used for Gates. One is the ANSI/ IEEE Std 91/91a-1991 type, the other one is according IEC 60617-12. In English and US publications the IEC symbols can be found seldomly only. So they do not reach the high international relevance of the IEEE style.

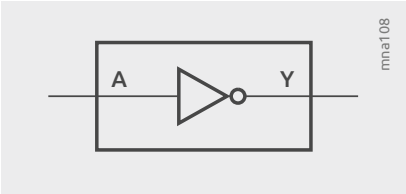


Figure 2.1a | IEEE symbol of an Inverter

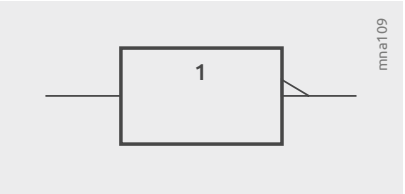


Figure 2.1b | IEC symbol of an Inverter

2.2 Logic gates

In the logic portfolio basic functions are provided to enable the direct application of Boolean algebra. For example, the logic component for the AND operation is called an AND gate. Within electrical systems these gates are often referred to as control logic

AND Gate

The 2-input AND function is depicted in Table 4. The output of an AND gate will only be high (1) if all inputs are high. All other input combinations will result in a low (0) at the output. In electronic systems with active high enable, an AND gate output can be used to prevent enabling the system until certain conditions (e.g. power and temperature status) monitored at the AND gate inputs are met. If either input is held high the output will have the same state as the other input. This enables either input to be used as an active high enable to gate data streamed on the other input.

In Figure 2.2 the symbols for a 2-input AND gate are depicted.

Table 4: 2-Input AND gate function table

Input A	Input B	Output Y
0	0	0
0	1	0
1	0	0
1	1	1

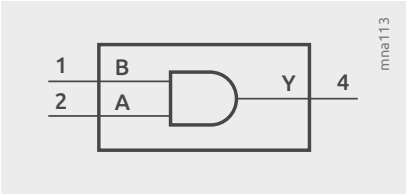


Figure 2.2a | IEEE symbol of an AND gate

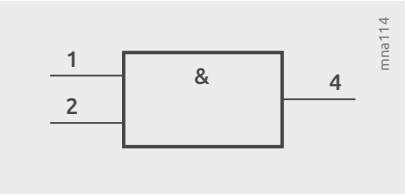


Figure 2.2b | IEC symbol of an AND gate

NAND Gate

If the output of an AND gate is inverted another basic function, a NAND gate is realized. The 2-input NAND function is depicted in Table 5. The output of a NAND gate will only be low if all inputs are high. All other input combinations will result in a high at the output. In electronic systems with active high enable, a NAND gate output can be used to disable the system if a combination of undesired conditions monitored at the NAND gate inputs have been met. If either input is held high the output will have the inverted state of the other input. This provides an active high gated inverter function.

In Figure 2.3 the symbols for a 2-input NAND gate are depicted.

Table 5: 2-Input NAND gate function table

Input A	Input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

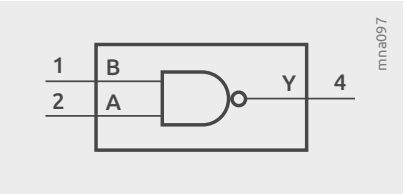


Figure 2.3a | IEEE symbol of a NAND gate

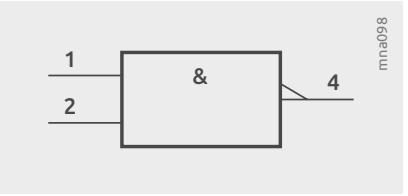


Figure 2.3b | IEC symbol of a NAND gate

OR Gate

The 2-input OR function is depicted in Table 6. The output of an OR gate will only be low if all inputs are low. All other input combinations will result in a high at the output. In electronic systems with active high enable, an OR gate output can be used to enable the system if one or more conditions (e.g. automatic or manual start) monitored at the OR gate inputs is true. If either input is held low the output will have the same state as the other input. This enables either input to be used as an active low enable to gate data streamed on the other input.

In Figure 2.4 the symbols for a 2-input OR gate are depicted.

Table 6: 2-Input OR gate function table

Input A	Input B	Output Y
0	0	0
0	1	1
1	0	1
1	1	1

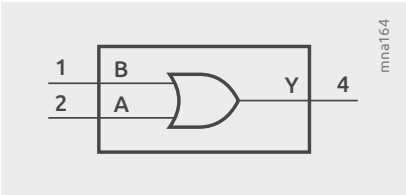


Figure 2.4a | IEEE symbol of an OR gate

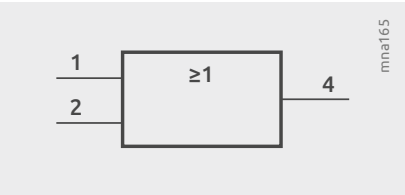


Figure 2.4b | IEC symbol of an OR gate

NOR Gate

If the output of an OR gate is inverted another basic function, a NOR gate is realized. The 2-input NOR function is depicted in Table 7. The output of a NOR gate will only be high if all inputs are low. All other input combinations will result in a low at the output. In electronic systems with active high enable, a NOR gate output can be used to disable the system if any undesired conditions monitored at the NOR gate inputs have been met. If either input is held low the output will have the inverted state of the other input. This provides an active low gated inverter function.

In Figure 2.5 the symbols for a 2-input NOR gate are depicted.

Table 7: 2-Input NOR gate function table

Input A	Input B	Output Y
0	0	1
0	1	0
1	0	0
1	1	0

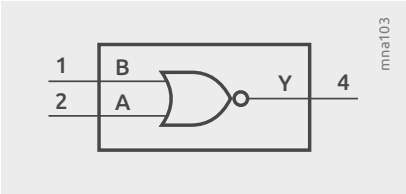


Figure 2.5a | IEEE symbol of a NOR gate

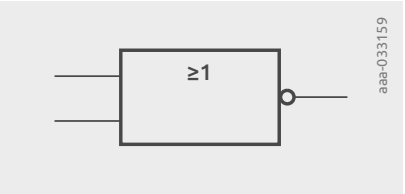


Figure 2.5b | IEC symbol of a NOR gate

Exclusive-OR (XOR) Gate

The 2-input Exclusive-OR (XOR) function is depicted in Table 8. The output of a XOR gate will only be high if only one of the inputs is high. All other input combinations will result in a low at the output. In electronic systems with active high enable, an XOR gate output can be used to enable the system if only one condition monitored at the XOR gate inputs has been met. If either input is held low the output will have the same state as the other input. If either input is held high the output will have the inverted state of the other input. This provides a dynamically controlled device that can stream data or inverted data.

In Figure 2.6 the symbols for a 2-input XOR gate are depicted.

Table 8: 2-Input Exclusive-OR-Gate

Input A	Input B	Output Y
0	0	0
0	1	1
1	0	1
1	1	0

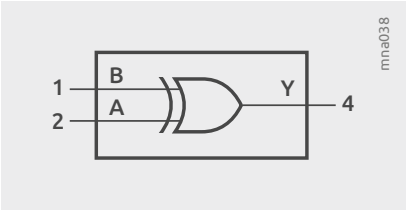


Figure 2.6a | IEEE symbol of a XOR gate

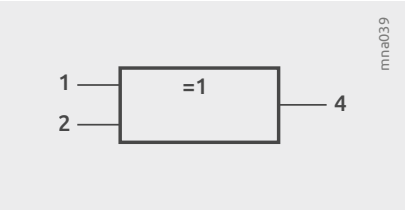


Figure 2.6b | IEC symbol of a XOR gate

Exclusive-NOR (XNOR) Gate

If an inverter is added behind an exclusive OR the function of an XNOR is realized. The 2-input Exclusive-NOR (XNOR) function is depicted in Table 9. The output of a XNOR gate will only be high if both inputs are the same. All other input combinations will result in a low at the output. In electronic systems with active high enable, an XOR gate output can be used to enable the system if both conditions monitored at the XOR gate inputs are the same. If either input is held high the output will have the same state as the other input. If either input is held low the output will have the inverted state of the other input. This provides a dynamically controlled device that can stream data or inverted data.

In Figure 2.7 the symbols for a 2-input XNOR gate are depicted.

Table 9: 2-Input Exclusive NOR-Gate

Input A	Input B	Output Y
0	0	1
0	1	0
1	0	0
1	1	1

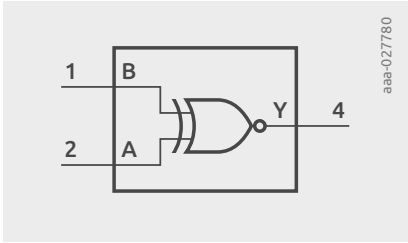


Figure 2.7a | IEEE symbol of a XOR gate

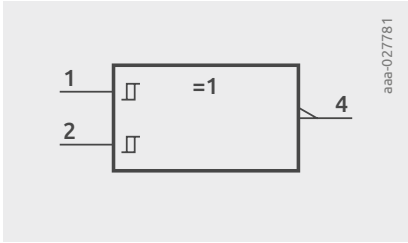


Figure 2.7b | IEC symbol of a XOR gate

2.3 Storage elements

Flipflops

A flipflop is a circuit which has two stable conditions at the output. This logic condition of a low or high state at the output does not depend on the actual setting of control inputs only but also on the history. A flipflop can store a state for an infinite time as long as a supply voltage is present. So it can store the information of one bit.

There are several types of flipflops with different topologies.

Most simple is a so-called RS-flipflop. It can be set and reset via two inputs that work level controlled.

A more important category of flipflops are D-flipflops. They have a data input D and can store the state of this signal line. Storage can be controlled by an enable signal. These flipflops are transparent from input to output as long as the enable signal is set to high level. The last logical state is stored once the enable is turned off.

The most important category of flipflops work with a so-called clock signal CLK. The input signal is sampled and stored by the rising or falling edge of the clock. The clock-driven flipflops are the basic block for many important circuits in logic designs. These are multi-bit storage devices called registers as well as counters and shift registers.

Logic devices from the standard families with storage stages have no internal power-on circuitry applying a reset to the flipflops in the IC. If a defined start condition for such devices is required, the application has to take care that after the supply voltage is ramped up into the recommended V_{CC} range, suitable controls are provided to the IC to bring it into the desired state.

If the product has a reset pin, this control can be used to clear flipflops contained in the design. This makes it easy to create a cleared state power-on condition. The timing requirements for the reset have to be obeyed. It does not work to connect a low active reset pin to the supply directly. Then V_{CC} and reset pin ramp up together and the device has no chance to perform a safe reset. In the FAQ section more advice can be found how to secure a reliable power up behavior if this is required by the target application.

A detailed explanation of flipflop types and more complex circuits designed with this basic function can be found in Chapter 6 of this handbook.

2.4 Switches

Analog Switches

Analog switches are bi-directional transmission gates, consisting of a PMOS and a NMOS transistor in parallel. They are used for switching rail to rail analog and low frequency digital signals. There are many configurations of analog switch available. Single pole single throw (SPST) is used in isolation applications. A single digital control pin is used to turn the switch on or off connecting or isolating the signal path. In the SP8T configuration three digital control pins are used to connect one input/output to one of eight output/inputs. Due to the bi-directional feature of analog switches the SP8T configuration is also known as an 8:1 analog multiplexer/demultiplexer. In Figure 2.8 an SPDT configuration is shown. Two transmission gates have one common terminal, the pole and two independent throw terminals. This configuration uses a single digital control signal S to switch the pole terminal Z to either of the throw terminals Y1 or Y2.

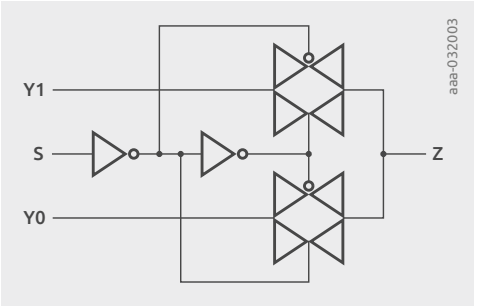


Figure 2.8 | SPDT analog switch

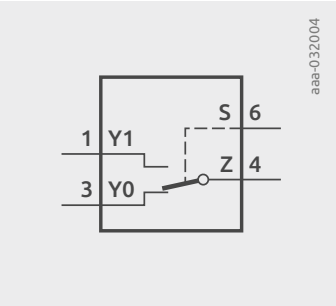


Figure 2.9 | Logic diagram SPDT switch

Many products include a control pin to allow the multiplexer to be enabled or disabled. When disabled all switches are non-conducting (off). This enables the poles of several devices to be connected to create larger multiplexer/demultiplexing solutions. Devices with this feature are identified with SPxT-Z, the -Z indicating they can be disabled.

Multiplexer configurations are used extensively in analog input expansion applications. Many microprocessors have a limited number of analog to digital converter (ADC) inputs. An analog multiplexer can be used to sequentially monitor many analog sensors using the same ADC input. On resistance (RON) and switching time (ten) specifications are provided in datasheets to enable an assessment to be made for application suitability.

Analog switches can also be used with digital signal isolation and multiplexing/demultiplexing. As they are transmission gates they will not behave as a repeater and regenerate the digital signals, care must be taken to ensure that the digital signal is not compromised by any bandwidth limitations of the analog switch. Analog switch datasheets include a −3 dB bandwidth specification to allow assessment on the effect on the digital signal to ensure signal integrity within the application.

Bus switches

If several SPxT-Z analog switches are used in parallel, data from several sources can be multiplexed onto a single data line. From a system standpoint connecting poles together does increase the effective load capacitance seen by the data signal. This will reduce the bandwidth of the solution. Bus switches have the same key parameters and are available in the same configurations as the above discussed analog switches. They can be used in isolation and multiplexing applications. To support the data rate increases in modern applications, bus switches have lower switch capacitance $C_{S(ON)}$, resulting in higher bandwidth. Additional features of bus switches include options of voltage level translation and switching signals higher than the bus switch supply voltage.

2.5 Logic data sheet parameters

Each logic device is supported by a datasheet as a result the data sheet parameters published will be explained in detail. The logic data sheets start with a general description of a device followed by a section about major features and benefits. Automotive qualified components can be identified easily via the Q100 at the end of the product name.

All logic parts exceed at least a 2 kV HBM (Human Body Model) and 1 kV CDM (Charged Device Model) ESD rating to ensure safe handling in assembly and production.

A section with ordering information follows addressing different package variants of the product. Marking code information is provided next, followed by functional diagrams as discussed above. Pinning information per package option can be found and a pin description.

A function table describes in detail how the device works exactly in dependence on all control inputs and/or a clock signal.

2.6 Limiting values

Liming values are provided in accordance with the Absolute Maximum Rating System (IEC 60134). The device is not guaranteed to function under these conditions, it is guaranteed not to be degraded if stresses are kept within the limiting values.

The limiting values start with the allowed supply voltage range from V_{CC}(min) up to V_{CC}(max). If this range is obeyed, no damage can happen to the device, but it does not need to be functional. V_{CC}(min) is equal −0.5 V in most cases. This is not a supply for operation of course. A range for the input and output voltages V_I and V_O is informed as next parameter. These values can be exceeded as long as the related clamping current limit I_{IK} and I_{OK} are obeyed.

A limiting value for the current of a single output is provided as well as an I_{CC} and I_{GND} limit which is reached for example if several outputs drive a comparably low-ohmic resistor load. If the output termination is applied towards ground, an I_{CC} current will be seen if the output state is high. If output termination is realized towards V_{CC}, additional ground current is created if the state of the output is the low-state.

Logic components can be stored at temperatures from −65 °C up to 150 °C. The power dissipation of a device is limited to the value P_{tot} for a defined temperature range. For some package options a linear derating is mentioned as a footnote with a power decrease factor of e.g. 7.8 mW/K to be applied starting for temperatures above 118 °C. P_{tot} reaches 0 mW at T_{amb} = 150 °C. An electronic component with bond wires of gold shall not exceed a die temperature or T_j above 150 °C.

2.7 Recommended operating conditions

In this section of a logic device data sheet, the ranges for V_{CC}, V_I and V_O is informed. For V_O ranges can be found for products that support the I_{OFF} feature. These components have high-ohmic output stages if the supply voltage is removed (V_{CC} = 0 V). In power down or suspend mode, the maximum value for the recommended supply voltage range can be applied.

An important parameter in the recommended operating condition section is the maximum allowed input transition and fall rate Δt/ΔV. If this condition is not fulfilled, current consumption can increase and malfunction could occur for clocked devices or in case of noise overlay to the signals.

2.8 Static characteristics

The static characteristics chapter inform the minimum voltage for a high-level input signal V_{IH}(min) and the maximum voltage for a low-level input signal V_{IL}(max) for a specific supply voltage V_{CC}. These parameters tell which area of the input voltage range is undefined or forbidden.

Figure 2.10 shows the resulting input voltage ranges dependent on V_{CC} for the logic family AUP. The signal has to stay in one of the blue areas to be processed as a low-level or high-level.

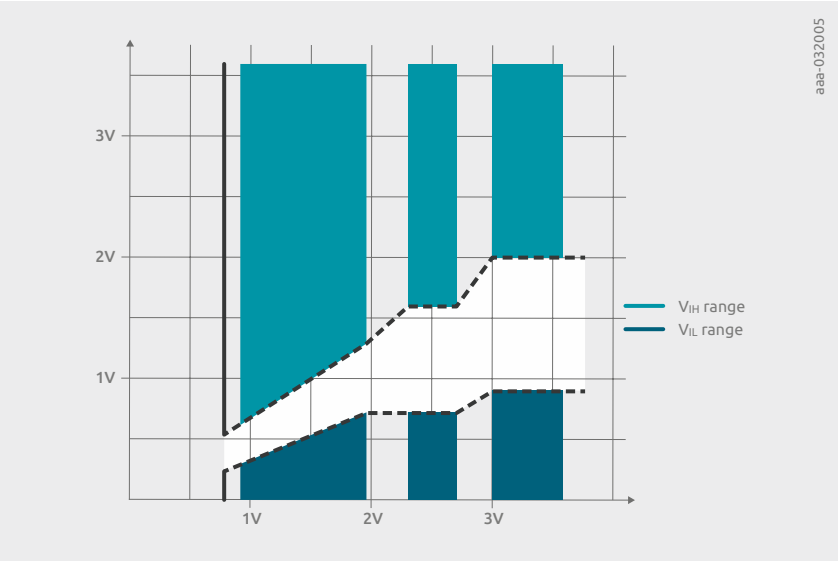


Figure 2.10 | Input voltage ranges of the logic family AUP dependent on V_{CC}

For Schmitt trigger inputs the positive going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-} is shown as transfer characteristic to define the behavior of a digital input. A Schmitt Trigger input provides a hysteresis characteristic as depicted in Figure 2.11. Schmitt Trigger inputs are tolerant to smooth transitions and quite immune against noise on the input signals. Many logic components feature a so-called Schmitt Trigger Action input. Such input does not have a wide hysteresis like a full performance Schmitt-Trigger input but performs more safely in case of noise overlay on transitions compared to a conventional input characteristic.

The static characteristics in a data sheet furthermore include the output voltages for a logic high-level V_{OH} and low-level V_{OL} for defined output currents and supply voltages. For a proper operation from a logic device output to a logic device input the relation between output and input voltage has to be in line with row 1 and 4 of Table 10.

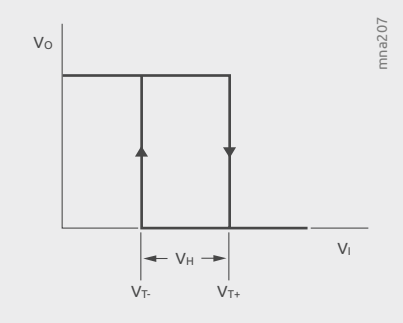


Figure 2.11 | Schmitt Trigger Input Characteristic

Table 10: Voltage requirements from output to input for a proper operation

Device 1		Device 2	Operation
V_{OH}(min)	>	V_{IH}(min)	Function guaranteed
V_{OH}(min)	<	V_{IH}(min)	Function not guaranteed
V_{OL}(max)	>	V_{IL}(max)	Function not guaranteed
V_{OL}(max)	<	V_{IL}(max)	Function guaranteed

Additional static parameters are the supply current maximum for open outputs I_{CC}(max) and the maximum input leakage current I_I(max). For devices that support the I_{OFF} feature, the maximum power-off current I_{OFF}(max) is informed for V_{CC} = 0 V and a maximum ΔI_{OFF} for V_{CC} from 0 V to 0.2 V, means that a V_{CC} turn-off is not ideal.

As an additional supply current parameter for input voltage deviating from perfect 0 V or V_{CC} low or high level condition, a maximum ΔI_{CC} current value can be found.

The above described static characteristics are provided for different temperature ranges for many logic devices in separate tables.

2.9 Dynamic characteristics

The propagation delay t_{PD} is a very important dynamic parameter of a logic device. For a gate or buffer it is the simple delay for a change at an input to a change of a logic state at the output. In Figure 2.12 an example is shown for a 2-input AND-Gate. The diagram depicts a propagation delay for the negative-going edge t_{PHL} and the opposite direction from low to high state t_{PLH}. Propagation delay is measured from a 50% level of the related transitions.

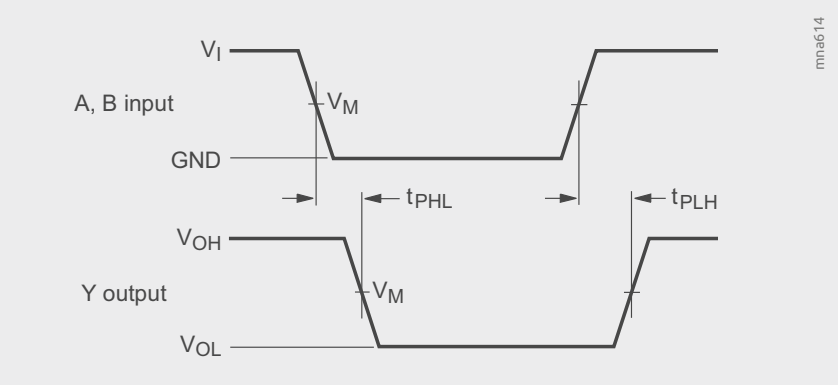


Figure 2.12 | Data input to output propagation delay

For edge-triggered devices propagation delay is defined as time between the active clock transition and the change of state at the output. Figure 2.13 is a timing diagram of a Flipflop. Propagation delay is measured from the rising edge to the change of the output signal. Beside propagation delay other important timing parameters are shown in the diagram. The data input D needs to be stable for at least the set-up time t_{su} before the active clock transition and needs to stay stable at least for the hold time t_h. f_{max} is the maximum clock frequency of a logic device. This value is a good indication for the maximum signal speed that gates can handle from a considered logic family. The parameter t_W defines the minimum pulse width for the clock input CP low state and the width of the set and reset signals. All these parameters can be found in the dynamic characteristics chapter of a data sheet.

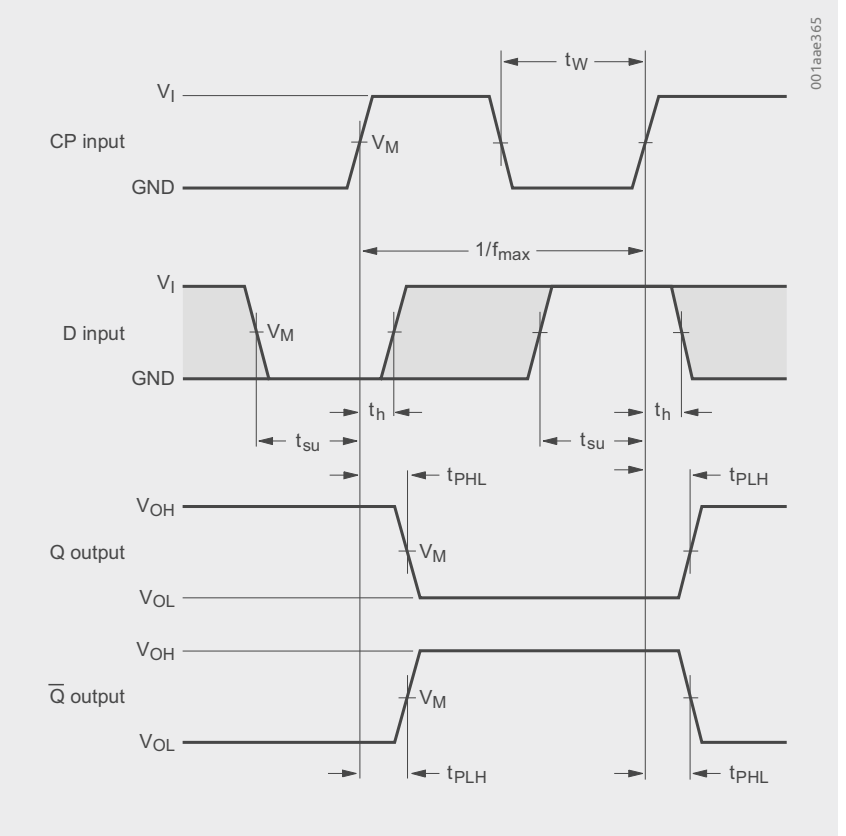


Figure 2.13 | Timing diagram of a Flipflop

The dynamic parameters are listed for different supply voltages (V_{CC}). The higher the voltage, the faster a CMOS logic device becomes. Lower temperature decreases t_{pd}.

C_{PD} is an equivalent power dissipation capacitance that supports the calculation of the dynamic power dissipation:

$$P_D = C_{PD} \times {V_{CC}}^2 \times f_i \times N + \sum [C_L \times {V_{CC}}^2 \times f_o]$$

f_I = input frequency in MHz
f_O = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = Supply voltage in V
N = number of inputs
Sum $[C_L \times V_{CC}^2 \times f_O]$ = sum of all outputs

More details about timing aspects are discussed in the chapter Timing Considerations.

Other info

The logic data sheets inform with detailed waveform diagrams and test circuit schematics how data sheet values and parameters are derived and need to be tested. In a final section of data sheets the package outline of all the variants of a product are shown together with tolerance information.

Chapter 3

Power considerations for CMOS and BiCMOS logic devices

As general purpose components, logic devices are used at different frequencies and power supply voltages in many different varieties of applications. This large diversity has produced the need to express a single parameter that can be used in determining the power dissipation of a device in a given application. This chapter describes different components of power dissipation and how they may be calculated.

3.1 Static considerations

CMOS

When a CMOS device is not switching and the input levels are GND or V_{CC}, the p-channel and n-channel transistors do not conduct at the same time; no direct MOS transistor channel path exists between V_{CC} & GND. In practice however, thermally generated minority carriers, which are present in all reverse biased diode junctions, allow a very small leakage current to flow between V_{CC} and GND. As this leakage current is typically a few nA, quiescent CMOS power dissipation is extremely low. Maximum quiescent power dissipation for the above conditions is calculated as:

$$P_D = V_{CC} \times I_{CC} \quad (1)$$

Where:
I_{CC} = specified in the device datasheet

BiCMOS

In the case of BiCMOS (Bipolar CMOS) devices; the current in the output bipolar stage is different when the output is set high or low. This results in two datasheet specifications for quiescent current $I_{CC(\text{for output low})}$ & $I_{CC(\text{for output high})}$. Quiescent power dissipation for input levels of GND or V_{CC} is calculated as:

$$P_D = V_{CC} \times (n_1 I_{CC(\text{for output low})} + n_2 I_{CC(\text{for output high})})/(n_1 + n_2) \quad (2)$$

Where:
n_1 = number of outputs LOW
n_2 = number of outputs HIGH

Input stage current due to GND < VI < VCC

In the case where the input levels of the device are not held at GND or V_{CC}, a direct MOS transistor current path can exist between V_{CC} and GND; this leads to additional supply current through the input buffer stage of CMOS devices, and additional power dissipation. In device datasheets this is represented as ΔI_{CC}, the additional current due to an input level other than V_{CC} or GND. In the case of 5.5 V logic families this parameter is generally measured at an input voltage of V_{CC} −2.1; in the case of 3.3 V logic families it's measured at an input voltage of V_{CC} −0.6 V. Static power dissipation is then calculated as:

$$P_D = V_{CC} \times [(n_1 I_{CC(\text{for output low})} + n_2 I_{CC(\text{for output high})})/(n_1 + n_2) + n\Delta I_{CC}] \quad (3)$$

Where:
n = number of inputs at the intermediate level

Note:
For CMOS $I_{CCL} = I_{CCH} = I_{CC}$, simplifying Equation (3): $P_D = V_{CC} \times [I_{CC} + n\Delta I_{CC}]$

Table 1 shows a comparison of I_{CC} and ΔI_{CC} for the '244 (octal buffer) function of several logic families.

Table 1: Power consumption of logic process families

CMOS families					
Device	Voltage	$I_{CC}Q$	V_I	ΔI_{CC}	Units
74HC244	6 V	80	V_{CC} – 2.1 V	450	µA
74AHC244	5.5 V	40	V_{CC} – 2.1 V	1500	µA
74LV244	5.5 V	20	V_{CC} – 0.6 V	500	µA
74LVC244	3.6 V	10	V_{CC} – 0.6 V	500	µA
74ALVC244	3.6 V	10	V_{CC} – 0.6 V	750	µA

BICMOS families							
Device	Voltage	I_{CCZ}	I_{CCL}	I_{CCH}	V_I	ΔI_{CC}	Units
74LVT244	3.6 V	0,19	12	0,19	V_{CC} – 0.6 V	0,2	mA

3.2 Dynamic considerations

When a device is clocked or changing state, power is dissipated through the charging and discharging of on-chip parasitic and load capacitances. Power is also dissipated at the moment the output switches when both the p-channel and the n-channel transistors are partially conducting. This transient energy loss is typically only 10% of that due to parasitic capacitance.

Power considerations for CMOS and BiCMOS logic devices

The total dynamic power dissipation per device is:

$$P_D = \Sigma(C_{PD} V_{CC}^2 f_I) + \Sigma(C_L V_{CC}^2 f_O) \quad (4)$$

Where:

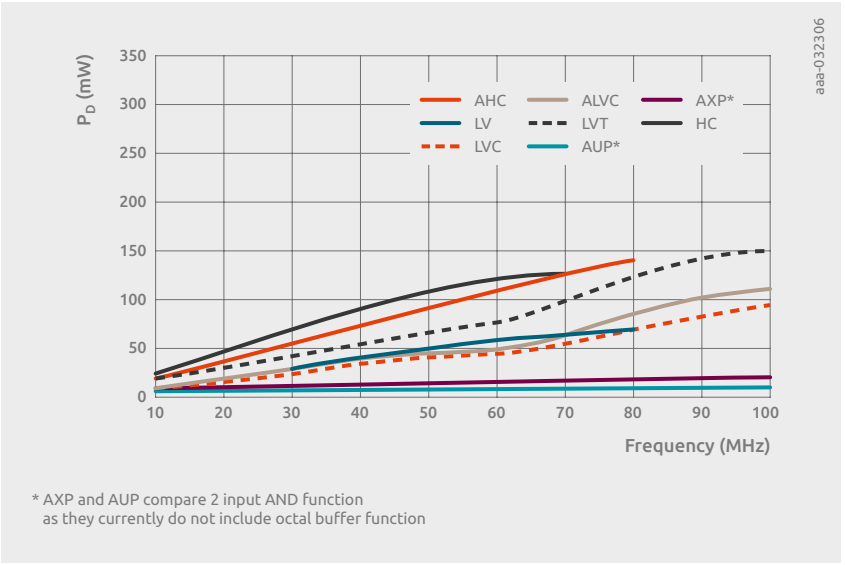
C_{PD} = power dissipation capacitance per buffer

f_I = input frequency

f_O = output frequency

C_L = total external load capacitance per output

It should be noted from the Equation (4), that C_{PD} is a useful parameter for determining power dissipation in any device for which power dissipation is a linear function of frequency. Figure 3.1 shows I_{CC} as a function of frequency for the devices listed in Table 1. From this we can conclude that for all CMOS and BiCMOS logic families C_{PD} can be used in order to determine the worst case power consumption of a device in a given application.



* AXP and AUP compare 2 input AND function as they currently do not include octal buffer function

Figure 3.1 | Power consumption over frequency for various logic process families

3.2.1 Duty cycle considerations with unbalanced outputs

In the case of unbalanced output drive, such as found in BiCMOS, the output duty cycle could also be considered. Figure 3.2 shows the effect of duty cycle on the power dissipation of the 74LVT244. It can be concluded from these measurements that the duty cycle has little effect on the total power dissipation. This is due to the switching currents within BiCMOS products being more dominant than steady state currents.

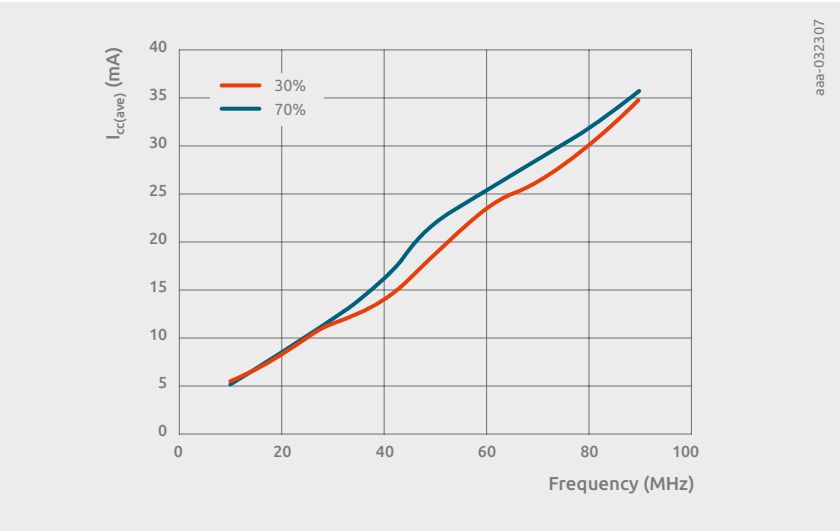


Figure 3.2 | Current consumption for different duty cycles

3.2.2 Power dissipation due to slow input rise/fall times

When an CMOS push pull stage switches, there is a brief period when both output transistors conduct. The resulting through-current is additional to the normal supply current and causes power dissipation to increase linearly with the input rise or fall time. As long as the input voltage is less than the n-channel transistor threshold voltage, or is higher than V_{CC} minus the p-channel transistor threshold voltage, one of the input transistors is always off and there is no through-current. When the input voltage equals the n-channel transistor threshold voltage (typ. 0.7 V), the n-channel transistor starts to conduct and through-current flows, reaching a maximum at $V_I = 0.5\,V_{CC}$. For devices with CMOS inputs, the maximum current is determined by the geometry of the input transistors. When Schmitt triggers are used to square pulses with long rise/fall times, through-current at the Schmitt-trigger inputs will increase the power dissipation (see Schmitt-trigger data sheets).

3.2.3 Process family related dynamic power dissipation

Dynamic power dissipation can be reduced using more advanced process technology. The table below shows a comparison of propagation delay and dynamic power dissipation for various process family devices based on the 2 input AND function. In the comparison, AUP and AXP have the lowest power consumption, generally the trend towards low power consumption of newer process families can be clearly seen.

	4.5 V to 5.5 V				3.0 V to 3.6 V			
	min	typ	max	P_D (mW)	min	typ	max	P_D (mW)
	t_{PD} (ns)				t_{PD} (ns)			
HC(T)	-	9.0	23.0	750	-	-	-	-
AHC(T)	1.0	4.6	9.0	550	1.0	6.5	14.0	240
LVC	0.5	1.7	4.0	525	0.5	2.1	4.5	229
AUP	-	-	-	-	0.9	2.2	4.3	98
AXP	-	-	-	-	-	-	-	-

	2.3 V to 2.5 V				1.65 V to 1.95 V			
	min	typ	max	P_D (mW)	min	typ	max	P_D (mW)
	t_{PD} (ns)				t_{PD} (ns)			
HC(T)	-	-	-	-	-	-	-	-
AHC(T)	-	-	-	-	-	-	-	-
LVC	0.5	2.2	5.5	111	1.0	3.4	8.0	68
AUP	1.0	2.4	4.8	45	1.3	3.0	6.1	26
AXP	0.9	2.0	3.0	41	1.2	2.6	4.1	24

	1.4 V to 1.6 V				1.1 V to 1.3 V				0.75 V to 0.85 V			
	min	typ	max	P_D (mW)	min	typ	max	P_D (mW)	min	typ	max	P_D (mW)
	t_{PD} (ns)				t_{PD} (ns)				t_{PD} (ns)			
HC(T)	-	-	-	-	-	-	-	-	-	-	-	-
AHC(T)	-	-	-	-	-	-	-	-	-	-	-	-
LVC	-	-	-	-	-	-	-	-	-	-	-	-
AUP	1.5	3.7	7.5	17.6	2.1	5.1	11.7	11.1	-	17	-	4.8
AXP	1.5	3.2	5.0	16.7	1.8	4.3	7.3	10.7	1.8	11	122	4.7

3 Power considerations for CMOS and BiCMOS logic devices

3.3 Power dissipation capacitance

C_{PD} is specified in the CMOS device data sheets, the published values being calculated from the results of tests described in this section. The test set-up is shown in Figure 3.3. The worst-case operating conditions for C_{PD} are always chosen and the maximum number of internal and output circuits are toggled simultaneously, within the constraints listed in the data sheet. Devices that can be separated into independent sections are measured per section, the others are measured per device.

The recommended test frequency for determining C_{PD} is 10 MHz, 50% duty cycle. Loading the switched outputs gives a more realistic value of C_{PD}, because it prevents transient through-current in the output stages.

The values of C_{PD} provided in datasheets have been calculated using:

$$C_{PD} = \frac{(I_{cc(ave)} \times V_{CC}) - [(C_L \times {V_{CC}}^2 \times f_o) + V_{CC} \times I_{STAT}]}{{V_{CC}}^2 \times f_I} \quad (5)$$

Where:

C_{PD} = power dissipation capacitance (per buffer)
$I_{CC(ave)}$ = supply current
V_{CC} = supply voltage
C_L = output load capacitance
f_O = output frequency
f_I = input frequency
I_{STAT} = supply current at dc (approx. zero for CMOS)

Power considerations for CMOS and BiCMOS logic devices

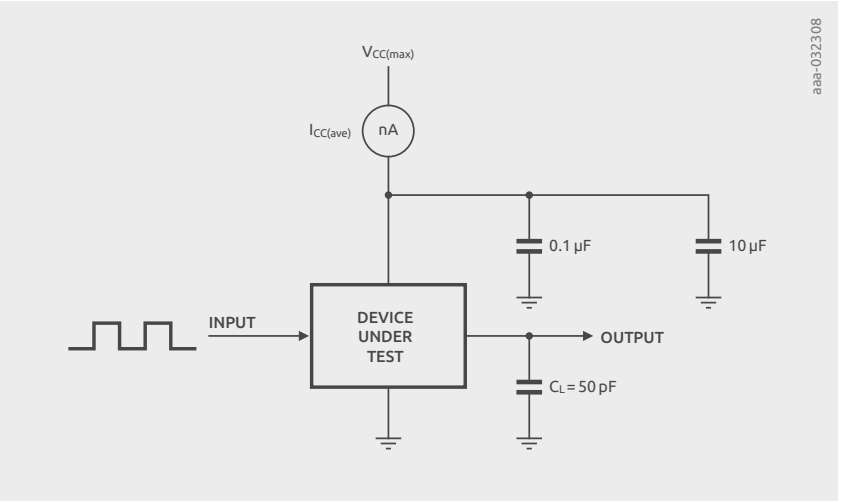


Figure 3.3 | Test set-up for C_{PD} determination

3.3.1 Example CPD calculations

CMOS

In the case of 74LVC244, I_{STAT} is negligible and can be considered as zero for the purpose of C_{PD} calculation. The test set-up for the '244 as indicated in *Conditions for C_{PD} tests* was used, with the load shown in Figure 3.3. At V_{CC} = 3.6 V, f_I = 10 MHz; $I_{CC(ave)}$ was found to be 2.24 mA.

Using Equation (5):

$$C_{PD} = \frac{(2.24\ mA \times 3.6\ V) - [(50\ pF \times 3.6\ V^2 \times 10\ MHz) + 0\ mW]}{3.6\ V^2 \times 10\ MHz}$$

$$C_{PD} = 12.2\ pF$$

BiCMOS

In the case of 74LVT244, I_{STAT} cannot be considered as negligible at low frequency. As a result, a higher frequency is recommended for modeling its C_{PD}. The test setup depicted in Figure 3.3 has been used, however at a frequency of 30 MHz. $I_{CC(ave)}$ was found to be 11.53 mA. We then apply Equation (5) with the assumption that I_{STAT} is negligible.

Using Equation (5):

$$C_{PD} = \frac{(11.53\ mA \times 3.6\ V) - (50\ pF \times 3.6\ V^2 \times 30\ MHz)}{3.6\ V^2 \times 30\ MHz}$$

$$C_{PD} = 56.8\ pF$$

Note:
Performing the measurement and calculation at 20 MHz results in a C_{PD} of 66 pF. Due to the uncertainty of I_{STAT} in a given configuration, it is recommended that a 5 to 10% guardband is used when approximating power dissipation for BiCMOS devices.

3.4 Using CPD to calculate power dissipation

3.4.1 CMOS Device Calculation

Consider a 3.6 V application in which every 40 ms a 74LVC244A device is used to buffer four 40 MHz, 75% positive duty cycle signals and two 80 MHz, 75% positive duty cycle signals, for a duration of 25 ms. The unused inputs are tied to 3.6 V, the outputs drive 30 pF loads, and when not buffering, four inputs are held at 3.0 V and two inputs held at GND.

In calculating the average power dissipation we need to consider both the power dissipation for the 15 ms when the device is not buffering, and the power dissipation for the 25 ms when the buffers are active.

In the first 15 ms the device is static and power dissipation is calculated using simplified Equation (3). In this case we have four inputs that are connected to V_{CC} −0.6 V.

$$P_{D1} = 3.6\ V \times 10\ \mu A + 4 \times 3.6\ V \times 500\ \mu A$$
$$= 7.24\ mW$$

In the second 25 ms the total power dissipation can be estimated as the combination of static the dynamic dissipation due to the four buffers and outputs switching at 40 MHz, and dynamic dissipation due to the two buffers and outputs switching at 80 MHz.

$$P_{D2} = 4 \times (C_{PD} + C_L) \times 3.6^2 \times 40\ MHz + 2 \times (C_{PD} + C_L) \times 3.6^2 \times 80\ MHz$$
$$= 87.1\ mW + 87.1\ mW$$
$$= 174.2\ mW$$

The average power dissipation is then:

$$P_{D(ave)} = (15 \times 7.24\ mW + 25\ x\ 174.2\ mW) / 40$$
$$= 111.6\ mW$$

3.4.2 BiCMOS Device Calculation

Consider the LVT244 in the same application.

In the case of BiCMOS devices, the duty cycle must be taken into consideration because I_{CCL} and I_{CCH} are not identical. In the first 15 ms of the application the static power dissipation is calculated using Equation (2) to determine quiescent power dissipation and adding the power dissipation caused by the four inputs that are connected to V_{CC} −0.6 V.

$$P_{D1} = 3.6\ V \times (6 \times I_{CC(for\ output\ high)} + 2\ x\ I_{CC(for\ output\ low)}) / 8 + 4\ x\ 3.6\ V \times \Delta I_{CC}$$
$$= 11.3\ mW + 2.9\ mW$$
$$= 14.2\ mW$$

The power dissipation in the next 25 ms contains in addition to those of the 74LVC244A case the component I_{STAT}. P_{D1} can be used to approximate I_{STAT}.

$$P_{D2} = 4 \times (C_{PD} + C_L) \times 3.6^2 \times 40\ MHz + 2\ x\ (C_{PD} + C_L) \times 3.6^2 \times 80\ MHz + 3.6 \times I_{STAT}$$
$$= 180\ mW + 180\ mW + 14.2\ mW$$
$$= 374.2\ mW$$

It should be noted that in using equation 3 to determine our dynamic dissipation components we are assuming a rail to rail output swing. As BiCMOS outputs don't swing rail to rail this will produce a worse case approximation.

The calculated average power dissipation is then:

$$PD_{(ave)} = (15 \times 14.2mW + 25 \times 374.2\ mW) / 40$$
$$= 239.2\ mW$$

3.5 Results and conclusion

Table 2: Comparison of measured and calculated results

Device	Static 15 ms			Dynamic 25 ms			Total	
		P_{D1} (mW)			P_{D2} (mW)		$P_{D(ave)}$ (mW)	
	$I_{CC(ave)}$ (mA)	Measured	Calculated	$I_{CC(ave)}$ (mA)	Measured	Calculated	Measured	Calculated
74LVC244A	0,008	0,028	7,24	48,2	173,5	174,2	108,4	111,6
74LVT244	2,5	9	14,2	102,4	368,6	374,2	233,8	239,2

Determination of power dissipation is an essential part of system design. By understanding the static and dynamic components of power dissipation, and how they can be modeled; a system designer is able to estimate the worst case power dissipation of an application.

Table 2 shows the comparison of the measured results to those calculated. The values of static and dynamic current that were calculated are within 10% of the measured values. Importantly the calculated values are higher than the measured values. This is due to the calculations being made with worse case datasheet limits. This is considered advantageous in system level power calculations, as it provides extra power budget margin in the application. It can be concluded, from the examples presented, that any device that has a linear relationship between supply current and frequency can be modeled as a single power dissipation capacitance C_{PD} for the purpose of power dissipation calculations of that device used in any application.

Conditions for C_{PD} tests

Gates
All inputs except one are held at either V_{CC} or GND, depending on which state causes the output to toggle. The remaining input is toggled at a known frequency. C_{PD} is specified per-gate.

Decoders
One input is toggled, causing the outputs to toggle at the same rate (normally one of the address-select pins is switched while the decoder is enabled). All other inputs are tied to V_{CC} or GND, whichever enables operation. C_{PD} is specified per-independent-decoder.

Multiplexers
One data input is tied HIGH and the other is tied LOW. The address-select and enable inputs are configured such that toggling one address input selects the two data inputs alternately, causing the outputs to toggle. With 3-State multiplexers, C_{PD} is specified per output function for enabled outputs.

Bilateral switches
The switch inputs and outputs are open-circuit. With the enable input active, one of the select inputs is toggled, the others are tied HIGH or LOW. C_{PD} is specified per switch.

3-State buffers and transceivers
C_{PD} is specified per buffer with the outputs enabled. Measurement is as for simple gates.

Latches
The device is clocked and data is toggled on alternate clock pulses. Other preset or clear inputs are held so that output toggling is enabled. If the device has common-locking latches, one latch is toggled by the clock. 3-State latches are measured with their outputs enabled. C_{PD} is specified per-latch.

Flip-flops
Measurement is performed as for latches. The inputs to the device are toggled and any preset or clear inputs are held inactive.

Shift registers
The register is clocked and the serial data input is toggled at alternate clock pulses (as described for latches). Clear and load inputs are held inactive and parallel data are held at V_{CC} or GND. 3-State devices are measured with outputs enabled. If the device is for parallel loading only, it is loaded with 101010..., clocked to shift the data out and then reloaded.

Counters
A signal is applied to the clock input but other clear or load inputs are held inactive. Separate values for C_{PD} are given for each counter in the device.

Arithmetic circuits
Adders, magnitude comparators, encoders, parity generators, ALUs and miscellaneous circuits are exercised to obtain the maximum number of simultaneously toggling outputs when toggling only one or two inputs.

Display drivers
C_{PD} is not normally required for LED drivers because LEDs consume so much power as to make the effect of C_{PD} negligible. Moreover, when blanked, the drivers are rarely driven at significant speeds. When it is needed, C_{PD} is measured with outputs enabled and disabled while toggling between lamp test and blank (if provided), or between a display of numbers 6 and 7.

LCD drivers are tested by toggling the phase inputs that control the segment and backplane waveforms outputs. If either type of driver (LCD or LED) has latched inputs, then the latches are set to a flow-through mode.

One-shot circuits
In some cases, when the device I_{CC} is significant, C_{PD} is not specified. When it is specified, C_{PD} is measured by toggling one trigger input to make the output a square wave. The timing resistor is tied to a separate supply (equal to V_{CC}) to eliminate its power contribution.

Chapter 4

Timing aspects of discrete devices

In a circuit design, the right timing of all participating components is essential for functionality. A wrongly calculated delay of a component or a misunderstanding of its temporal behavior could end up in a complete system failure. This chapter will explain the required fundamentals to understand the timing aspects of logic devices and successfully apply them in the design process.

4.1 Synchronous and asynchronous logic

An asynchronous circuit, or self-timed circuit, is a digital logic circuit which is not governed by a clock circuit or global clock signal. Instead it often uses signals that indicate completion of instructions and operations, specified by simple data transfer protocols. This type of circuit is contrasted with synchronous circuits, in which changes to the signal values in the circuit are triggered by single or repetitive pulse called a clock signal. Most digital devices today use synchronous circuits. However asynchronous circuits have the potential to be faster, and may also have advantages in lower power consumption, lower electromagnetic interference, and better modularity in large systems. An illustration of asynchronous and synchronous logic circuit examples is given in Figure 4.1 and Figure 4.2.

Figure 4.1 shows a symbol for asynchronous logic. In contrast to just combinatorial logic, a logic state can be stored and therefore a feedback loop is needed. An example for such an element is a simple RS Flip-Flop.

For a synchronous Logic element, the feedback loop id synchronized by an extra clock signal as shown in Figure 4.2.

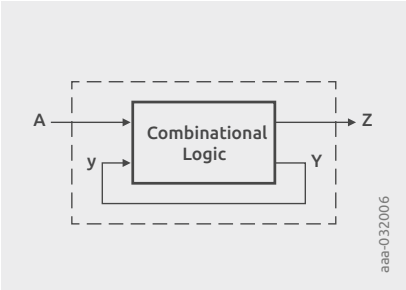


Figure 4.1 | Asynchronous Logic element

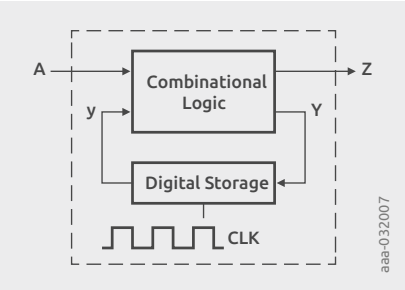


Figure 4.2 | Synchronous Logic element

4.2 Propagation delay time of a device

In digital circuits, the propagation delay, or gate delay, is the length of time which starts when the input to a logic gate becomes stable and valid to change, to the time that the output of that logic gate is stable and valid to change. In logic components datasheets this refers to the time required for the output to reach 50% of its final output level when the input changes to 50% of its final input level. Reducing gate delays in digital circuits allows them to process data at a faster rate and improve overall performance. The determination of the propagation delay of a combined circuit requires identifying the longest path of propagation delays from input to output and by adding each t_{PD} time along this path.

The difference in propagation delays of logic elements is the major contributor to glitches in asynchronous circuits as a result of race conditions.

Pulse Width t_W is the time gap between a rising edge and a falling edge of a signal. The reference signal level for measuring the time is 50% of the amplitude between high and low level. Figure 4.3 shows the measurement parameters for propagation delay (t_{pd} if $t_{PHL} = t_{PLH}$), rise and fall times ($tr = t_{TLH}$, $tf = t_{THL}$). Transition times are measured from 10% to 90% of signal level.

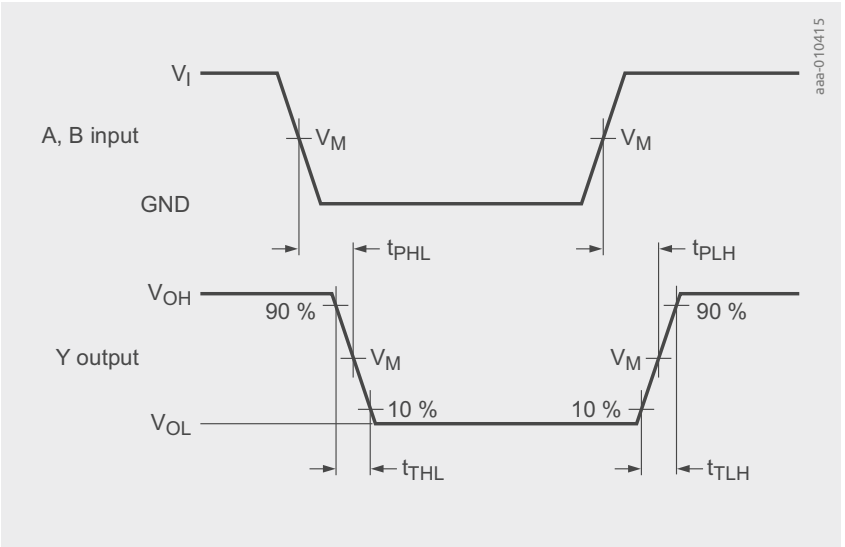


Figure 4.3 | Propagation delay measurement

4.3 Timing parameters of Flip Flops and Latches

Flip-Flops and Latches are circuits with two stable states that can be used to store state information. Flip-flops can be either level-triggered (asynchronous, transparent or opaque) or edge-triggered (synchronous, or clocked).

Propagation delay — Propagation delay for a Flip Flop is the time between the clock event (either rising or falling edge) and the output signal change. As well as for gates, 50% of the signal level is taken for measurement window.

Setup time t_{SU} — Setup time is the minimum amount of time the data input should be held steady before the clock event (either rising or falling edge), so that the data is reliably sampled by the clock.

Hold time t_H — Hold time is the minimum amount of time the data input should be held steady after the clock event, so that the data is reliably sampled by the clock. Both set-up and hold time are illustrated in Figure 4.4.

The timing parameters set-up and hold time are related to interface signal levels and are caused by internal gate delays, meaning that the clock signal needs to be propagated internally to sample the data signal.

Aperture is the sum of setup and hold time. The data input should be held steady throughout for this period of time.

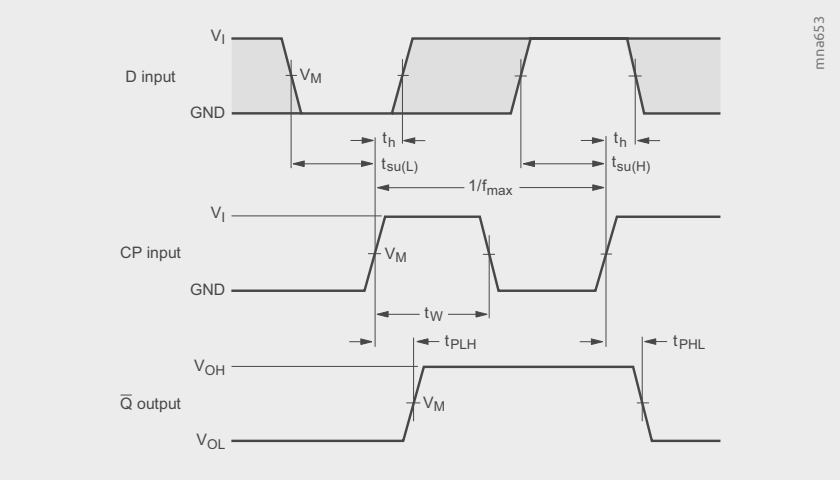


Figure 4.4 | The Clock input (CP) to output (Q) propagation delays, clock pulse width, D to CP set-up and hold times and the maximum clock input frequency

Recovery time is the minimum amount of time the asynchronous set or reset input should be inactive before the clock event, so that the data is reliably sampled by the clock. The recovery time for the asynchronous set or reset input is thereby similar to the setup time for the data input.

Removal time is the minimum amount of time the asynchronous set or reset input should be inactive after the clock event, so that the data is reliably sampled by the clock.

4.4 Skew definitions

Skew specification measurements are taken at certain conditions which may or, more likely, may not match a specific condition in a system application. However, like other AC specifications the skew specification is valuable as a "benchmark" for estimating certain circuit characteristics. Skew specifications are most valuable in clock–driving applications and applications where duty cycle characteristics are important. Three specific skew specifications are described as follows:

4.4.1 Output Skew tSK(o)

JEDEC definition: "The difference between two concurrent propagation delay times that originate at either a single input or two inputs switching simultaneously and terminate at different outputs."

This skew generally characterizes like–going edges of a single IC only. It compares t_{PLH} versus t_{PLH} (or t_{PHL} vs. t_{PHL}) for two or more output data paths. This parameter is very useful in describing output distribution capabilities of a device. tSK(o) would be most valuable to designers using the device as a clock driver, distributing clock signals. tSK(o) could be further subdivided into tSK(LH) (output rising edge) and tSK(HL) (output falling edge) skews, as can be seen in Figure 4.5.

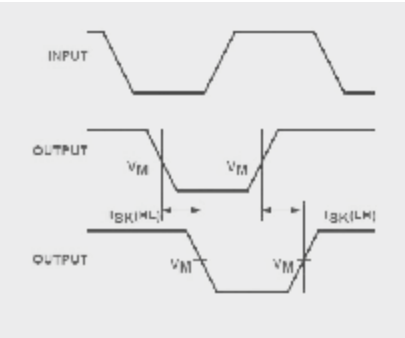


Figure 4.5 | Output skew illustration

4.4.2 Process Skew tSK(x)

JEDEC definition: "The difference between identically specified propagation delay times on any two samples of an IC at identical operating conditions."

This parameter addresses the issue of process variations by quantifying the difference between propagation delays that are caused by lot–to–lot variations. It does not include variations due to differences in supply voltage, operation temperature, output load, input edge rates, etc.

This parameter could be viewed as a tSK(o) skew over several like devices. An example of two devices with process skew is shown in Figure 4.6.

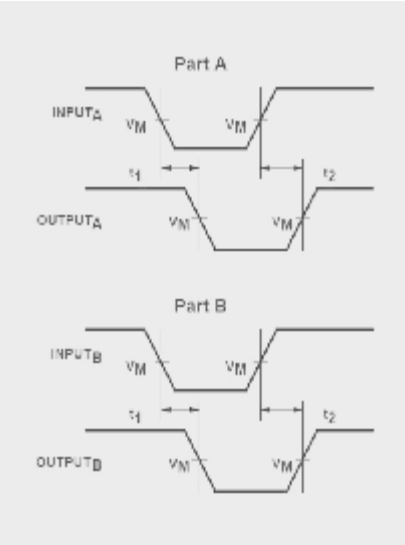


Figure 4.6 | Process Skew

4.4.3 Pulse Skew tSK(p)

JEDEC definition: "The difference between the propagation delay times t_{PHL} and t_{PLH} when a single switching input causes one or more outputs to switch."

This parameter is used to quantify duty cycle characteristics. Some applications require a nearly perfect 50% duty cycle. tSK(p) specifies the duty cycle retention characteristics of the device.

4.5 Meta stability and its mitigation

Meta stability in electronics is the ability of a digital electronics system to persist for an unbounded time in an unstable equilibrium or metastable state. In digital logic circuits, a digital signal is required to be within certain voltage or current limits to represent a '0' or '1' logic level for correct circuit operation; if the signal is within a forbidden intermediate range it may cause faulty behavior in logic gates the signal is applied to. In metastable states, the circuit may be unable to settle into a stable '0' or '1' logic level within the time required for proper circuit operation. As a result, the circuit can act in unpredictable ways, and may lead to a system failure, sometimes referred to as a "glitch".

Reasons for Meta Stability

In most cases, the cause for an undefined internal state of a logic device is the absence of input drive. The basic element of all logic devices is the inverter with a PMOS and an NMOS transistor connected with common drain and common gate. In stable state, one of them is conducting while the other is disabled. In case of an input signal driving the common gate to an intermediate voltage level between V_{CC} and GND, both PMOS and NMOS transistors are partly conducting. This intermediate state is normally occurring during switching transition. If it remains as a static state, the device is metastable and a constant current through the transistors is drawn. In addition to the undefined logic state, the increased current consumption is another reason for the necessity to avoid meta stable states in a logic circuit.

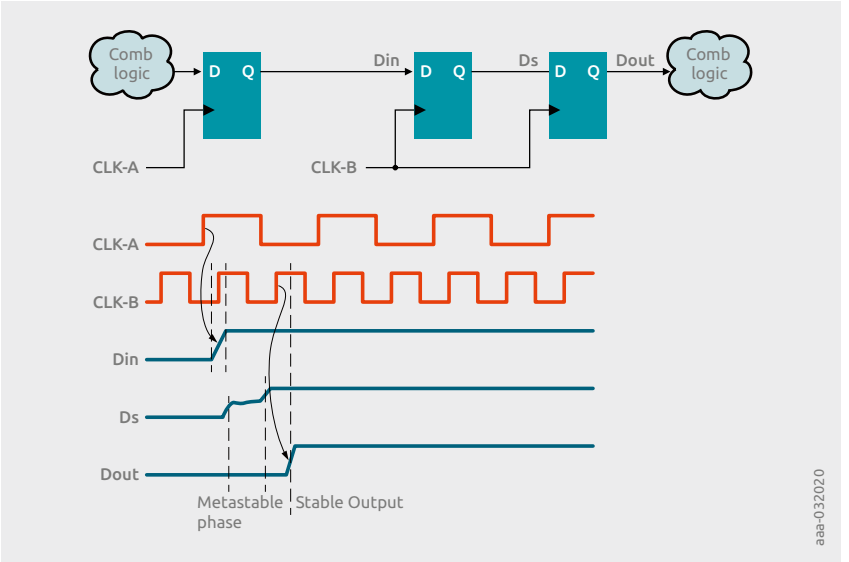


Figure 4.7 | Meta stability in a synchronizer where data crosses between 2 clock domains

Mitigation of Meta stability

As far as meta stability is caused by input signals, it is important for the circuit designer to assure that driving signals are in defined states, logic high or low.

Causes related to internal device configurations as shown in Figure 4.6, must be prevented by design measures taken by the designer. Unused inputs should always be connected to V_{CC} or ground thru an appropriate current limiting resistor.

4.6 Maximum frequency information

The operation frequency and the related data rate of logic devices is to a large extent dependent on process technology.

The maximum clock or operation frequency is specified in data sheets for those devices which are timing related such as Flip Flops and Counters. Generally, devices of the product segment 'synchronous interface logic' in Nexperia's web page have a specification for frequency.

For other devices, the best way to find out the operation frequency is to compare a timing related device of the same process family.

Chapter 5

Interfacing aspects of logic devices

The usage of discrete logic devices is associated with various aspects of interfaces. The timing was already addressed in the previous chapter. Further to timing, many more aspects need to be considered when integrating a discrete logic device into an application design. In particular, voltage level shifting needs to be addressed. Various features of logic devices are also interface related, such as Bus Hold, I_{OFF}, and Schmitt-Trigger inputs. Physical effects are affecting the interfaces of discrete device, and are therefore addressed in this chapter as well, i.e. Ground and V_{CC} bounce.

5.1 Application requirements for interfacing

A high performance of a system is very often the result of a thorough system integration. In a system integration process, all parts of the system need to be composed to form a functional unit. The primary requirements that make a component fit into the system are oriented to its interface properties such as timing, voltage and other features. In the following sub-chapters, we will explain the most important interface properties of discrete logic devices to support their integration.

Level shifting/translation

Level shifter and translator circuits are used to interface between components with different supply voltage and input-output voltage levels. A classic example is a Microcontroller with a supply voltage of 1.8 V and a peripheral device, i.e. a sensor with a supply voltage of 3.3 V. If the enable signal for the sensor is driven by a GPIO of the Microcontroller (which has 1.8 V) it needs to be level shifted to 3.3 V. There are various mechanisms for level shifting.

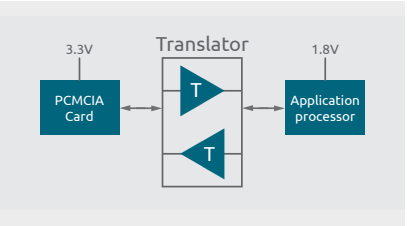


Figure 5.1 | Translating transceiver interface

Input and Output levels

Logic devices have input level requirements (Vinput high = V_{IH} and Vinput low = V_{IL}) and provide output voltage levels (V_{OH} and V_{OL}). The levels depend on the supply voltage as well as on process technology and design. Table 1 shows an extract of a data sheet table showing these figures.

Table 1: Specified input and output logic levels

Symbol	Parameter	Conditions	T_{amb} 25 °C			Unit
			Min	Typ	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	0.70 × V_{CC}	–	–	V
		V_{CC} = 0.9 to 1.95 V	0.65 × V_{CC}	–	–	V
		V_{CC} = 2.3 to 2.7 V	1.6	–	–	V
		V_{CC} = 3.0 to 3.6 V	2.0	–	–	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	–	–	0.30 × V_{CC}	V
		V_{CC} = 0.9 to 1.95 V	–	–	0.35 × V_{CC}	V
		V_{CC} = 2.3 to 2.7 V	–	–	0.7	V
		V_{CC} = 3.0 to 3.6 V	–	–	0.9	V
V_{OH}	HIGH-level input voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 µA; V_{CC} = 0.8 to 3.6 V	V_{CC} − 0.1	–	–	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	0.75 × V_{CC}	–	–	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	1.11	–	–	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	1.32	–	–	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	2.05	–	–	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	1.9	–	–	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	2.72	–	–	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	2.6	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 µA; V_{CC} = 0.8 to 3.6 V	–	–	0.1	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	–	–	0.3 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	–	–	0.31	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	–	–	0.31	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	–	–	0.31	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	–	–	0.44	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	–	–	0.31	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	–	–	0.44	V

V_{IH} is the high-level input voltage, if a voltage is applied that is > V_{IH}, it will be considered logic HIGH. V_{IL} is the low-level input voltage, if a voltage is applied that is < V_{IL}, it will be considered logic LOW. V_{OH} is the high-level output voltage at a specified output current. V_{OL} is the low-level output voltage at a specified output current.

Table 2 shows the input and output levels for TTL and CMOS products over a range of supply voltages.

Table 2: CMOS and TTL input and output voltage levels

	TTL				CMOS			
	Input Voltage		Output Voltage		Input Voltage		Output Voltage	
Voltage	V_{IH}	V_{IL}	V_{OH}	V_{OL}	V_{IH}	V_{IL}	V_{OH}	V_{OL}
5.0–15.0 V					0.7 × V_{CC}	0.3 × V_{CC}		
5.0 V	2.00	0.80	2.40	0.50	3.50	1.50	4.50	0.40
3.3 V	2.00	0.80	2.40	0.55	2.31	0.99	2.55	0.45
1.8 V					1.27	0.68	1.30	0.35
1.5 V					0.98	0.78	1.30	0.35
1.2 V					0.78	0.42	1.03	0.36

As shown in Table 3, to guarantee functionality, the V_{OH} of the driver must be higher than the V_{IH} of the receiver. Similarly, the V_{OL} of the driver must be lower than the V_{IL} of the receiver.

Table 3: Output and input voltage relations required for functionality

Device 1		Device 2	Operation
V_{OH} (min)	>	V_{IH} (min)	Function guaranteed
V_{OH} (min)	<	V_{IH} (min)	Function not guaranteed
V_{OL} (max)	>	V_{IL} (max)	Function not guaranteed
V_{OL} (max)	<	V_{IL} (max)	Function guaranteed

The existence of many voltage nodes creates issues when trying to connect circuits together. Figure 5.2 depicts H-L and L-H translation between devices of 3 different process families, in this example LVC, AUP and AXP types. As can be seen, level translation will be necessary when devices of these process types are connected in a circuit.

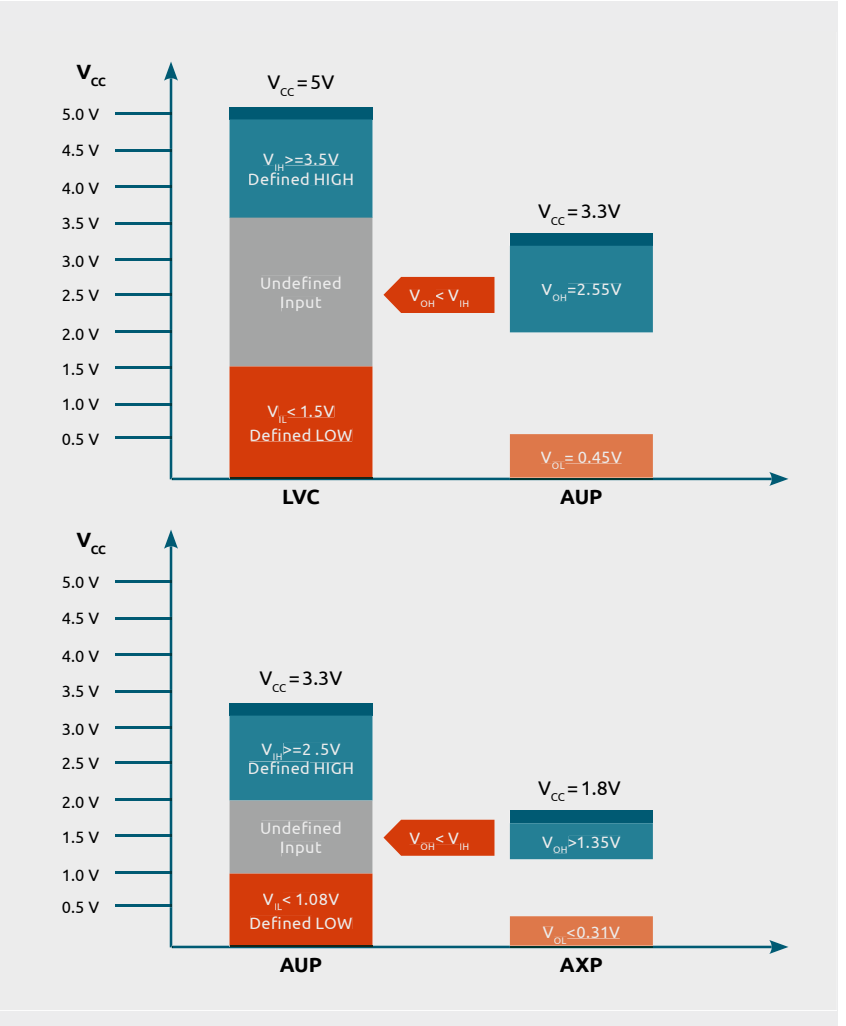


Figure 5.2 | I/O Voltage level overview for LVC, AUP, AXP

Types of translations

Uni-directional

Uni-directional translators can be either high-to-low or low-to-high level translators, but the signal direction is fixed. As an advantage, these translators only need one power supply domain, if the voltage gap between the 2 domains is within limits of < 2 V.

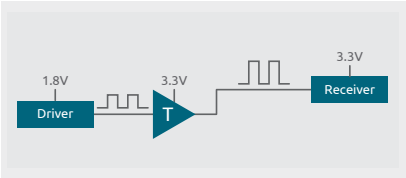


Figure 5.3 | Uni-directional low-to-high voltage translation

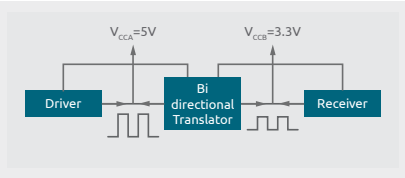


Figure 5.4 | Bi-directional LOW to HIGH and HIGH to LOW voltage translation

Bi-directional

Bi-directional translators are more flexible, both directions are supported and this is requiring dual power supply domains.

Bidirectional translation can be implemented using a direction control pin or with automatic sensing of the direction. The direction control pin needs to be driven by one of the participants, and it needs to have the right voltage level in dual supply voltage translators, in most cases this will be the V_{CCA} domain.

Auto Direction translators have no direction control pin and instead can be implemented using one of the following approaches:

- an inner circuit for sensing the driver
- a low power feedback loop that holds that last direction used and can be overwritten
- an intrinsic direction control such as a pass transistor.

Dual-supply voltage translators

Dual-supply devices have two supply voltages at different voltage ranges. These translators can be used for uni or bi-directional voltage level translation. Dual supply devices are designed for asynchronous communication between devices operating at different voltages and are also known as dual-supply voltage translators. Dual-supply voltage translators can be used for LOW to HIGH and HIGH to LOW voltage translation. These devices are supplied at V_{CCA} & V_{CCB} and interface data ports A & B operating in different voltage domains. They feature DIR pins to control signal direction. They are more power efficient than the single supply solutions.

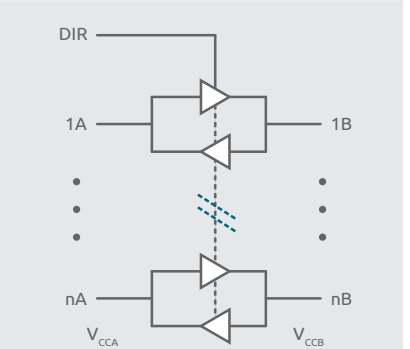


Figure 5.5 | Dual supply voltage translating transceiver

Mechanisms of translation

Clamp Diode Inputs

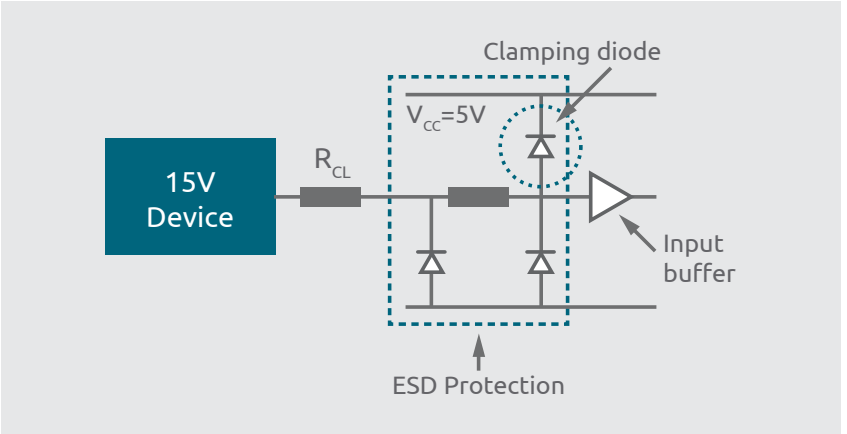


Figure 5.6 | Clamp input diode using current-limiting resistors

By using input current limiting resistors with the internal clamp diode, High to Low voltage translation is possible.

Many CMOS inputs include diodes to V_{CC} in their input ESD protection structures. Voltages higher than V_{CC} can be clamped by these diodes if current limiting resistors are used. This provides High to Low voltage translation using current limiting resistors. When voltages are higher than V_{CC}, it must be assured that the supply voltage is able to compensate the higher input voltage and does not increase the V_{CC} of the device.

Value of current limiting resistor R_{CL} can be calculated using V_{CC} values of driver and receiver devices. The input clamp diode also serves as an ESD protection.

Table 4: Output and input voltage relations required for functionality

Symbol	Parameter	Condition	Min	Max	Unit
I_{IK}	input clamping current	$V_I < -0.5\,V$ or $V_I > V_{CC} + 0.5\,V$	–	±20	mA
I_{CC}	supply current		–	50	mA
I_{GND}	supply current		−50	–	mA

Devices with input ESD diodes to V_{CC}:

A device has input ESD diodes to V_{CC} if the datasheet limiting value of I_{IK} includes the condition $V_I > V_{CC} + 0.5\,V$ and the max recommended $V_I = V_{CC}$ (see Table 4).

To use the ESD diode as a clamp diode the value of the current limiting resistors R_{CL} should be set to ensure that the limiting value of I_{IK} is not exceeded. If there are more than one inputs, ensure that the combined current does not exceed the limiting value of I_{CC}.

Advantage:
- Can be used to interface any voltage

Disadvantage:
- Requires external components

Overvoltage tolerant inputs

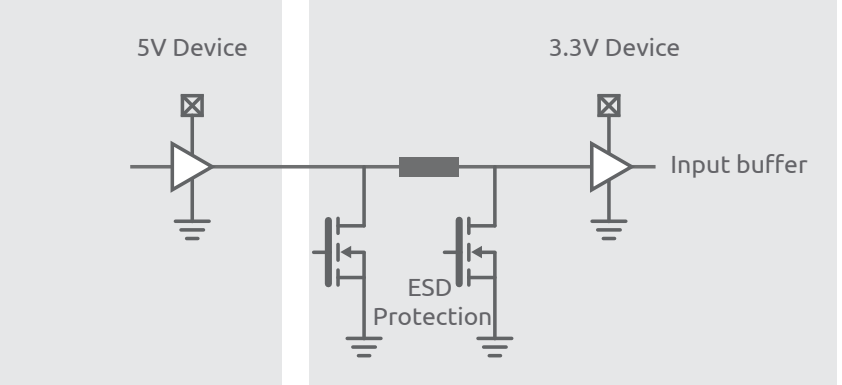


Figure 5.7 | Using overvoltage tolerant inputs to enable HIGH-to-LOW level translation

Modern CMOS ESD protection circuits provide the same ESD protection without including a diode to V_{CC}. These devices have over-voltage tolerant inputs because the recommended value of V_I is not V_{CC} but the same as the recommended maximum V_{CC}. A device specified for operation over a supply voltage range of 1.65 to 5.5 V can be used at 3.3 V with 5.5 V applied to inputs. A device with overvoltage tolerant inputs is suitable for High to Low level translation.

A device has overvoltage tolerant inputs if the datasheet limiting value of I_{IK} does not include the condition $V_I > V_{CC} + 0.5\,V$ and the max recommended V_I is not V_{CC}

Advantage:
- No external components required
- Lower system power than clamp diode solution

Disadvantage:
- Input cannot be driven at voltages greater than the recommended maximum value of V_{CC}

Open-drain outputs

An open-drain output can be pulled-up to the desired voltage level in Low to High voltage translation. The open drain output itself can only pull down, as it is implemented as a NMOS transistor with an open drain connected to the output of the device. In conduction mode, the NMOS conducts the output to GND. In devices equipped with an open-drain output, the output is pulled-up to a pull-up voltage level matching the input requirements of the device it is driving. A pull-up resistor is used on the output for level translation.

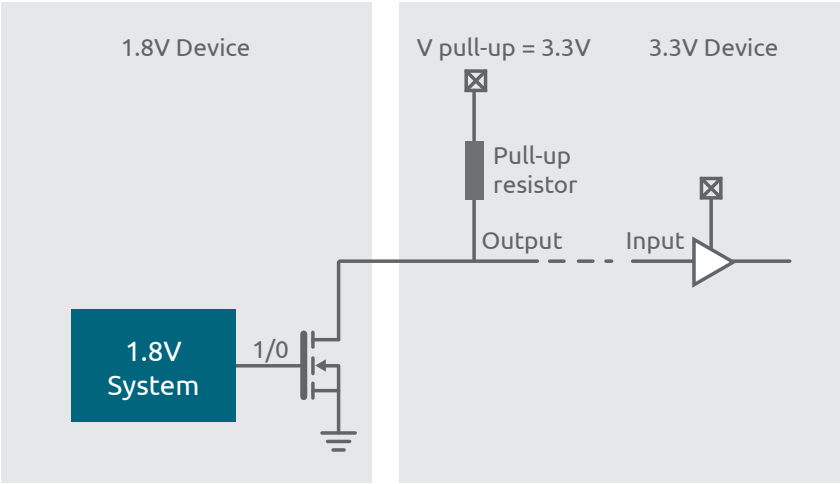


Figure 5.8 | Open-drain output and pull-up resistor for level translation

Important points to note when considering open-drain outputs with pull-up resistors for level translation:

- The output rise and fall times are dependent upon the value of pull-up resistor used.
- The pull-up may be higher than or lower than the device supply voltage
- In designs that use power-down to save battery life use devices that include I_{OFF} in the static characteristics
- How to detect devices with open-drain outputs from data sheet properties:
- Logic devices with open-drain outputs will not have a V_{OH} parameter listed in the static characteristics of the datasheet.

Advantage:

- High Low or Low High translation

Disadvantage:

- Requires external components
- Additional system power

Low threshold inputs

CMOS devices with input switching thresholds set lower than the typical $V_{CC}/2$ can be used for Low to High translation. Figure 5.9 shows an input structure of a low threshold device. The combination of N1 sizing and the drop across diode D1 determines the input threshold. The P2 PMOS reduces cross-bar current through the inverter. The AHCT and HCT families operate at 5 V and have inputs that can be interfaced to 5 V TTL or 3.3 V CMOS outputs. AUP1T operate at 3.3 V and can be used to interface to 1.8 V CMOS outputs.

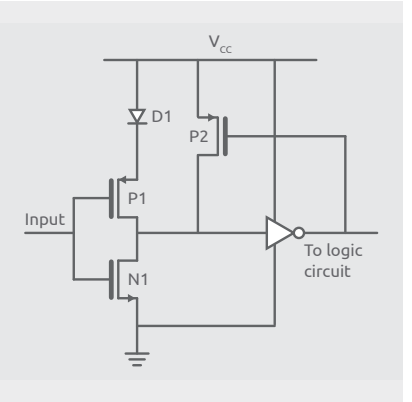


Figure 5.9 | CMOS input structure for low threshold input

Devices with low-threshold inputs can be detected from data sheet properties: They will have a ΔI_{CC} included in the static characteristics listed in the datasheet. This is the extra static current due to an input being applied that is less than V_{CC}. Table 5 shows a fraction from the data sheet table specifying the additional ΔI_{CC}.

Table 5: Parameters for devices with low-threshold inputs

Smybol	Parameter	Conditions	Min	Typ	Max	Typ
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6\,V$; $I_O = 0\,A$; $V_{CC} = 3.3\,V$	–	–	50	µA

It must be ensured that power dissipation is minimized the input should be set low as the default condition.

Advantage:

- No external components required
- Same footprint as standard function

Disadvantage:

- Higher power dissipation due to ΔI_{CC}

Examples of combinations of translation features

Overvoltage-tolerant inputs with open-drain outputs

In some cases a modular system may consist of circuits in three different voltage nodes. Control logic may be required to ensure correct functionality across all modules. A device that includes overvoltage-tolerant inputs and opendrain outputs can be used to interface between three voltage domains.

Figure 5.10 shows the 74AUP2G07 being supplied at 2.5 V and interfacing control signals between circuits at 3.3 V and 1.2 V.

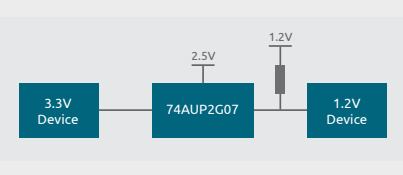


Figure 5.10 | OVT input with open drain outputs

Clamp diode inputs with open-drain outputs A device that includes an ESD protection diode and opendrain outputs can be used to interface between three voltage domains. Figure 5.11 shows the 74HC3G07 being supplied at 5.0 V and interfacing control signals between circuits at 12 V and 3.3 V Low-threshold inputs with open-drain outputs.

A device that includes low-threshold inputs and open-drain outputs can be used to interface between three voltage domains. Figure 5.12 shows the 74HCT3G07 being supplied at 5.0 V and interfacing control signals between circuits at 3.3 V and 1.8 V.

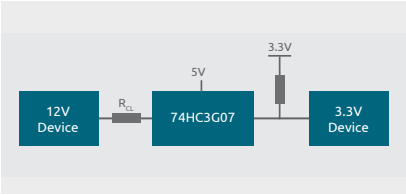


Figure 5.11 | Clamp diode inputs with open drain outputs

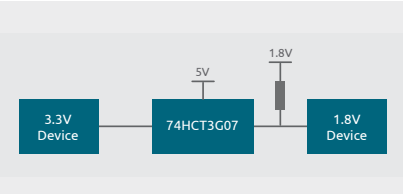


Figure 5.12 | Low threshold inputs with open drain outputs

5.2 Schmitt Trigger inputs

Schmitt trigger is a comparator circuit with hysteresis implemented. It is an active circuit which can convert an analog input signal to a digital output signal. When the input is higher than a chosen threshold, the output is high. When the input is below a different (lower) chosen threshold, the output is low, and when the input is between the two levels the output retains its value. This dual threshold action is called hysteresis.

Schmitt trigger devices are typically used in signal conditioning applications to remove noise from signals used in digital circuits, particularly mechanical contact bounce in switches. They are also used in closed loop negative feedback configurations to implement relaxation oscillators, used in function generators and switching power supplies.

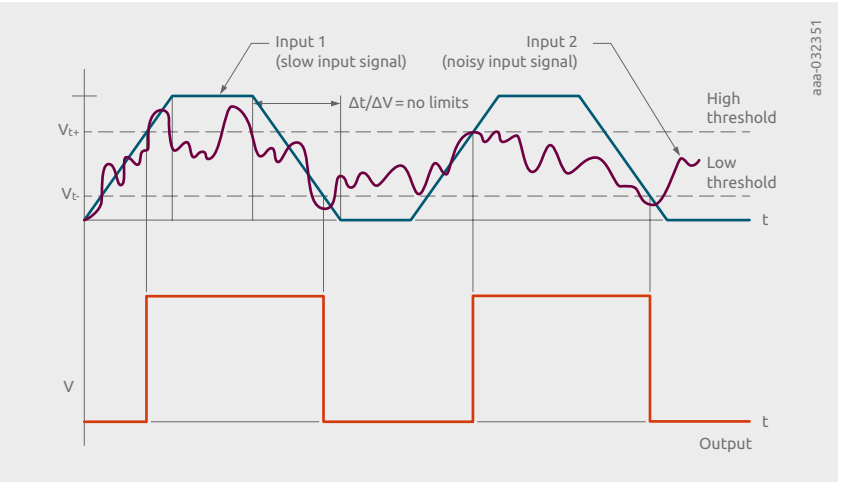


Figure 5.13 | The effect of noise compensation via Schmitt-Trigger input

A device with Schmitt-Trigger input has a specification for threshold voltage levels in the static characteristics table as shown in Figure 5.14:

A similar input function is the Schmitt trigger action, it has a smaller hysteresis than Schmitt-Trigger to improve noise immunity but will have an input and rise time limit

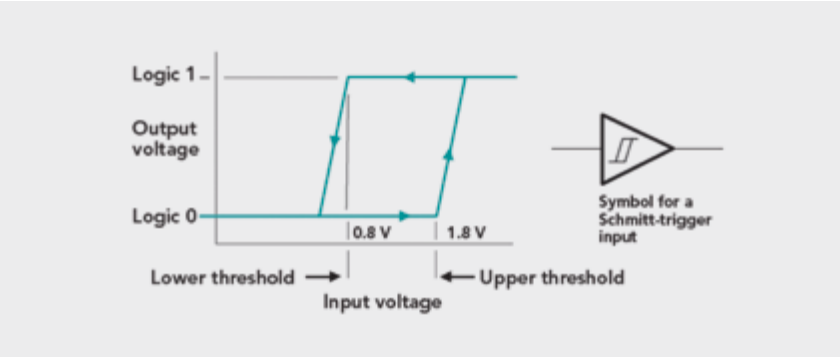


Figure 5.14 | Schmitt-Trigger Symbol and input voltage characteristics

Table 6: Schmitt-Trigger data sheet figures V_{T+}, V_{T-}, V_H

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{T+}	positive-going threshold voltage	V_{CC} = 1.8 V	0,82	1	1,14	0,79	1,14	V
		V_{CC} = 2.3 V	1,03	1,2	1,4	1	1,4	V
		V_{CC} = 3.0 V	1,29	1,5	1,71	1,26	1,71	V
		V_{CC} = 4.5 V	1,84	2,1	2,36	1,81	2,36	V
		V_{CC} = 5.5 V	2,19	2,5	2,79	2,16	2,79	V
V_{T-}	negative-going threshold voltage	V_{CC} = 1.8 V	0,46	0,6	0,75	0,46	0,78	V
		V_{CC} = 2.3 V	0,65	0,8	0,96	0,65	0,99	V
		V_{CC} = 3.0 V	0,88	1	1,24	0,88	1,27	V
		V_{CC} = 4.5 V	1,32	1,5	1,84	1,32	1,87	V
		V_{CC} = 5.5 V	1,58	1,8	2,24	1,58	2,27	V
V_H	hysteresis voltage	V_{CC} = 1.8 V	0,26	0,4	0,51	0,19	0,51	V
		V_{CC} = 2.3 V	0,28	0,4	0,57	0,22	0,57	V
		V_{CC} = 3.0 V	0,31	0,5	0,64	0,25	0,64	V
		V_{CC} = 4.5 V	0,4	0,6	0,77	0,34	0,77	V
		V_{CC} = 5.5 V	0,47	0,6	0,88	0,41	0,88	V

Summary:

- Schmitt trigger inputs will have specs of V_{t+} and V_{t-} depicted in datasheets
- Schmitt trigger action will not have Vt specs in the datasheet
- Schmitt trigger action will have rise time and fall time limitations specified for inputs in the recommended operating conditions

5.3 I_{OFF} mechanism and purpose

In a standard CMOS output circuit, body diodes of both NMOS and PMOS transistor are conducting even if the transistor is not in conduction mode. When a circuit is switched to partial power down mode, the body diode of the PMOS transistor is still conducting to the V_{CC} node if the output is connected to a certain voltage level. This is not desired and the I_{OFF} mechanism is used to mitigate this effect.

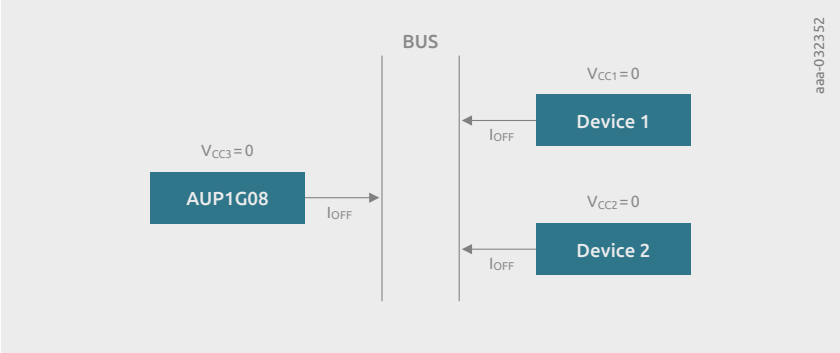


Figure 5.15 | Bus system with Logic devices featuring I_{OFF}

5.4 Ground and VCC bounce

Ground bounce is usually seen on integrated circuits where insufficient precautions have been taken to supply a logic gate with a sufficiently low resistance connection (or sufficiently high capacitance) to ground. In this phenomenon, when a transistor is turned on, enough current flows through the transistor circuit that the silicon in the immediate vicinity of the ground connection is pulled partially high, sometimes by several volts, thus raising the local ground, as perceived at the gate, to a value significantly above true ground. Relative to this local ground, the gate voltage can go negative, thus shutting off the transistor. As the excess local charge dissipates, the transistor turns back on, possibly causing a repeat of the phenomenon, sometimes up to several bounces.

V_{CC} bounce is a similar effect based on insufficient capability of the supply rail to drive the drawn current or by inductive effects of adjacent devices.

The V_{CC} node in the power subsystem is supposed to be at a constant potential or a constant voltage with respect to logic ground. Real power subsystems have varying currents drawn from them. Real power subsystems have non-zero impedances. The combination of these two result in "ripple" or V_{CC} rail bounce. Any signal line that is at a logic 1 using a CMOS driver will have this ripple riding on it unattenuated.

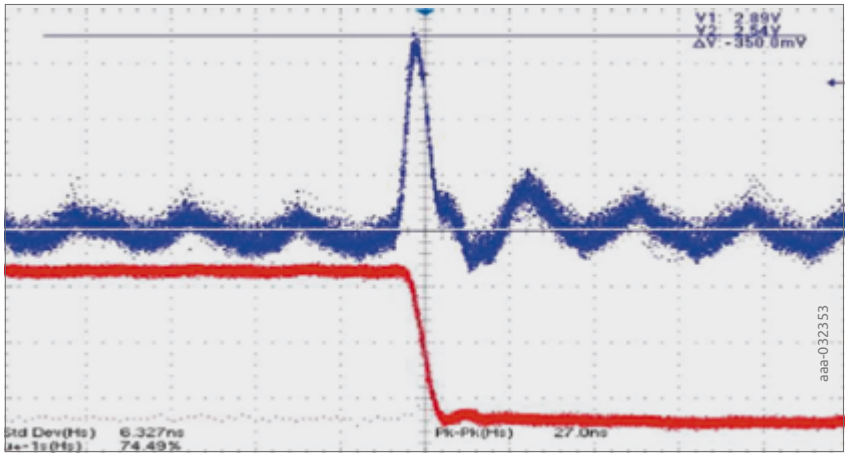


Figure 5.16 | Ground bounce effect caused by signal switching

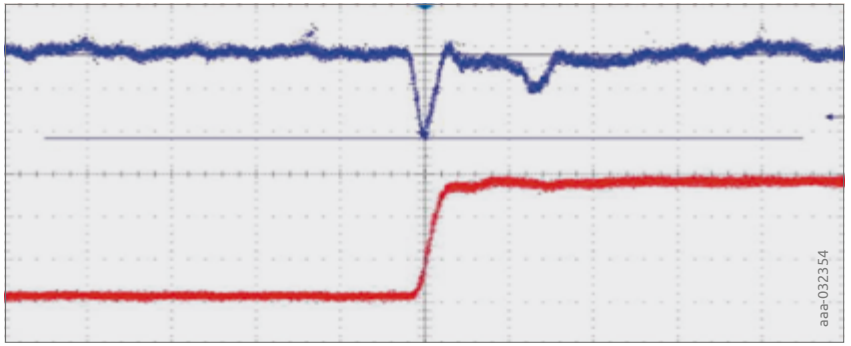


Figure 5.17 | V_{CC} bounce effect caused by signal switching

Measures to mitigate ground and V_{CC} bounce:

- Decoupling capacitors between V_{CC} and ground provide a temporary, low impedance, stable potential for the IC and localize the bounce effect to keep it from spreading to the rest of your circuit. By keeping the capacitors close to the IC, you minimize the area of inductive loop in the PCB traces and decrease the disturbance
- serially-connected current-limiting resistors to prevent excessive current from flowing into and out of the Device
- Address ground bounce in Layout/Routing implementation. Any unnecessary separation between the signal and return path will increase the inductance of that signal line and the subsequent effects of ground bounce
- Measures to reduce V_{CC} bounce are the same as described for reducing Ground bounce.

5.5 Bus Hold

CMOS device inputs are connected to the gate oxide of the NMOS and PMOS transistors and have a very high impedance. The advantage of CMOS, the very low power consumption under static conditions, is dependent on defined levels of the gate input voltage. In Figure 5.18 below we can see the CMOS input schematics and the ΔI_{CC} current/Vin curve. When V_I has a value at ~VDD/2, I_{CC} reaches its peak and that should only occur during a switching process. If the input is floating and the input voltage has a value nearby VDD/2, an unwanted ΔI_{CC} current flows which leads to undesired power consumption.

A way to mitigate this situation is to apply external pullup- or pull-down circuits. However, if these measures cannot be implemented, an internal feature that can be offered to prevent floating inputs is the Bus Hold feature.

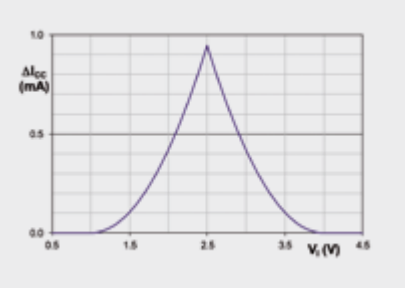


Figure 5.18 | ΔI_{CC} current over V_I

It provides a weak internal feedback inverter to the input, forming a latch together with the input stage (see Figure 5.20). By doing so, the last input level (low or high) is stored and thus the input voltage level is at a defined state, even in the absence of external voltage supply. Due to the relative weakness of the feedback inverter, the required driver strength of external signals at the input is not much increased. With this feature, floating input condition and associated increased ΔI_{CC} can be avoided.

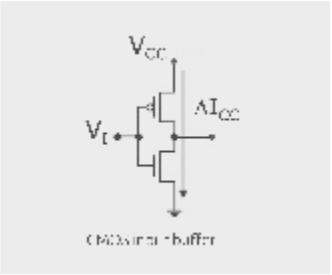


Figure 5.19 | Illustration of ΔI_{CC} current

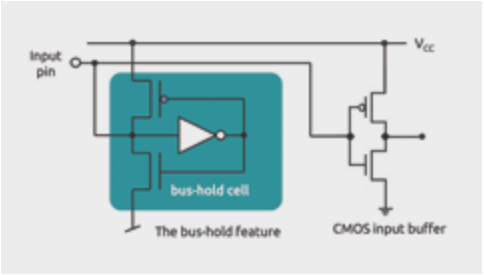


Figure 5.20 | Bus hold circuit

- Bus-Hold is a standard feature of Nexperia's LVT&ALVT bus interface products. It is available as an option in Nexperia's LVC, ALVC, and AVC bus interface products. An H is used to identify the bus-hold option (e.g. LVCH)
- Bus interface solutions from Nexperia include 8-, 16-, 18- and 32-bit buffers/inverters/drivers, flip-flops, latches/registered drivers, level shifters/translators and transceivers

In the data sheet, the Bus Hold properties are described in the table of static characteristics (Table 7). An example is shown in Figure 5.20. The high and low hold currents are the leakage currents in the device in high and low state respectively, flowing into the common drain of the feedback inverter shown in Figure 5.20. The overdrive currents are required to force the logic state to change into the respective opposite direction.

Table 7: Static characteristic table for a transceiver with Bus Hold feature

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
I_{BHL}	bus hold LOW current	V_{CC} = 1.65 V; V_I = 0.58 V	10	–	–	10	–	µA
		V_{CC} = 2.3 V; V_I = 0.7 V	30	–	–	25	–	µA
		V_{CC} = 3.0 V; V_I = 0.8 V	75	–	–	60	–	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 1.65 V; V_I = 1.07 V	−10	–	–	−10	–	µA
		V_{CC} = 2.3 V; V_I = 1.7 V	−30	–	–	−25	–	µA
		V_{CC} = 3.0 V; V_I = 2.0 V	−75	–	–	−60	–	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 1.95 V	200	–	–	200	–	µA
		V_{CC} = 2.7 V	300	–	–	300	–	µA
		V_{CC} = 3.6 V	500	–	–	500	–	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 1.95 V	−200	–	–	−200	–	µA
		V_{CC} = 2.7 V	−300	–	–	−300	–	µA
		V_{CC} = 3.6 V	−500	–	–	−500	–	µA

* All typical values are measured at T_{amb} = 25 °C.

5.6 Source Termination

With increasing systems speeds and faster logic devices, interconnect characteristics have become significant. The signal transition times of faster devices can increase transmission line effects on printed circuit board traces and cables. If not taken into consideration, signal degradation can cause data errors in a system.

Lumped and distributed systems

Series termination is one of many ways to terminate what are known as distributed systems

Electronic systems can be considered as either lumped systems or distributed systems. Factors that determine if a system is lumped or distributed include the rise time of applied signals and the delay time of the conductor.

If all points on the conductor react to a potential at the same time the system is lumped. Lumped systems have short trace lengths.

If all points on a conductor do not react to a potential at the same time the system is distributed. Distributed systems have longer trace lengths.

Generally the border between lumped and distributed systems occurs when trace length exceeds the signal rise (ps) divided by six times the delay time of the conductor (ps/in), as shown in the equation in Figure 5.21.

$$l_{con} = \frac{t_r}{6T_{con}}$$

l_{con} is the conductor length (in)
t_r is the signal rise time (ps)
T_{con} is the conductor delay (ps/in)

Figure 5.21 | Calculation of conductor length

Unlike lumped systems, distributed loads cannot be modeled using a single lumped capacitance. Transmission line models must be applied to determine the characteristic impedance of the distributed system.

If left unterminated, reflections occur in distributed systems. This is due to impedance mismatch between the output and the load it is driving. Reflections can lead to ringing on the signals. Unterminated distributed systems can lead to signal integrity issues within applications.

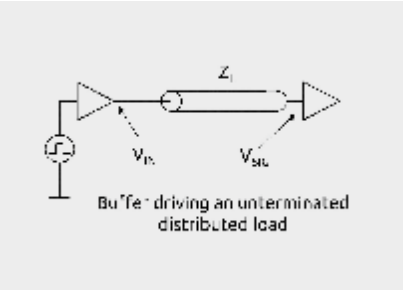


Figure 5.22 | ZL = characteristic Impedance of distributed load

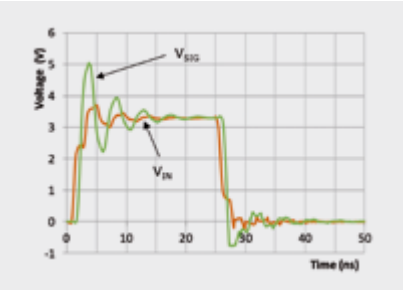


Figure 5.23 | Signal diagram for driver with distributed load

Source termination

To avoid signal integrity issues, one common way of terminating distributed systems is source termination. In source termination, the output resistance of the driver is matched to the characteristic impedance of the distributed system

The matching is done by adding a series resistor RS between the driver output and the distributed load. The value of the series resistor is set to ZL – ROUT. ZL is the characteristic impedance of the distributed system and ROUT is the output resistance of the driver. The updated circuit diagram is shown is shown in Figure 5.24, the improved Signal behaviour can be seen in Figure 5.25.

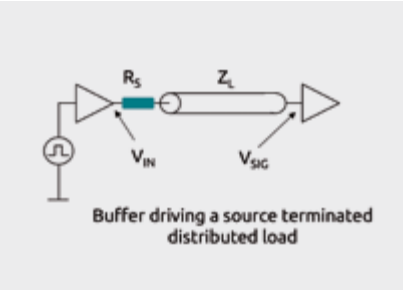


Figure 5.24 | Updated circuit of driver and load with series resistor

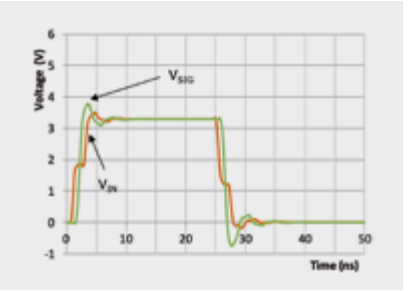


Figure 5.25 | Improved signal behavior due to added series resistor

The value of Rout is not given in the data sheet of the driver but can be calculated from data sheet figures. In the table for static characteristics, the output high level voltage V_{OH} is specified for certain levels of IO and V_{CC}. Rout is the ohmic resistance of the output stage and can be calculated like Rout = (V_{CC}-V_{OH})/IO, the values for V_{CC}, V_{OH} and IO can be taken from the static characteristics tale in the data sheet as shown in Table 8 below.

Table 8: Specification of V_{OH}

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = −100 µA; V_{CC} = 1.65 V to 3.6 V	V_{CC} − 0.2	–	–	V_{CC} − 0.3	–	V
		I_O = −4 mA; V_{CC} = 1.65 V	1.2	–	–	1.05	–	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.8	–	–	1.65	–	V
		I_O = −12 mA; V_{CC} = 2.7 V	2.2	–	–	2.05	–	V
		I_O = −18 mA; V_{CC} = 3.0 V	2.4	–	–	2.25	–	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.2	–	–	2.0	–	V

* All typical values are measured at T_{amb} = 25 °C.

Integrated source termination

Nexperia provides solutions in which output impedance matching is included. In general, the outputs are matched to a characteristic impedance of 50 ohms, making them suitable for a range of common PCB trace and cable impedances. While not providing perfect impedance matching for all loads, they can be used to reduce the amplitude of reflections in applications that are space constrained. The undershoot and overshoot performance into distributed systems of characteristic impedance from 50 to 75 ohms is acceptable.

Nexperia's advanced low voltage BiCMOS LVT & ALVT families and advanced low voltage CMOS families LVC, ALVC & AVC(M) all include source termination as an option. Many of Nexperia's 8-bit, 16-bit and 32-bit products include source termination as an option. These include buffers/inverters/drivers, flip-flops, latches/registered drivers and transceivers. When source termination is included on a transceiver device, it is included on both ports.

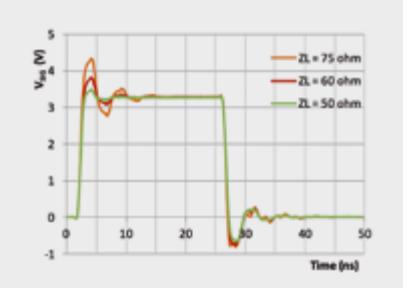


Figure 5.26 | Signal behaviour with 3 different internal source termination resistors

When source termination is included as an option within a family, a 2 is added after the family name in 8-bit devices. In 16-bit devices such as the 74LVC16244, the 2 is added after the 16. 16244 is changed to 162244 to indicate that the source termination feature is included.

Chapter 6

Analog and Logic Product Segmentation

In this Chapter, the functions and features of discrete Logic and analog devices are described. The coverage is largely corresponding to the product portfolio of Nexperia and clustered in a similar way as in the Internet portal. For various product groups, typical application examples are presented to support understanding and practical usage of the product group.

6.1 Analog ICs

Analog Switches

Analog switches can be used to transmit both, analog and digital signals. An ohmic conduction is established between input and output, implemented with MOSFETs and controlled by logic gates. The structure of an Analog Switch is basically a N-Channel FET in parallel with a P-Channel FET which allows signals to pass in either direction like shown in Figure 6.1.

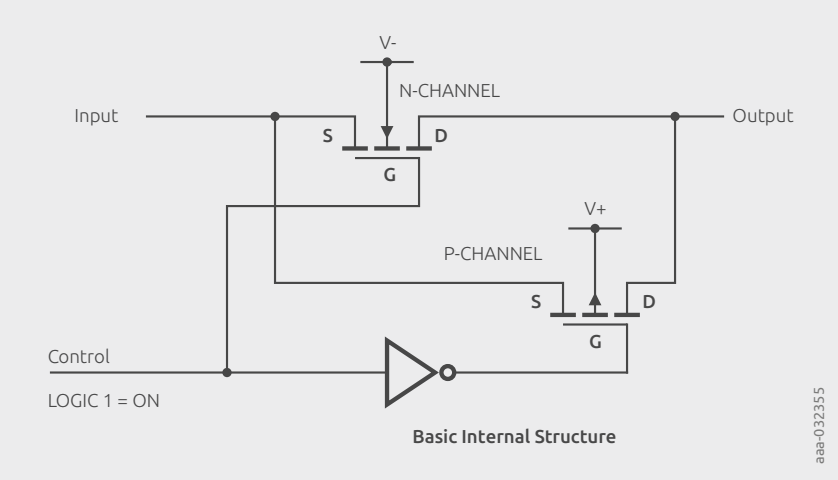


Figure 6.1 | Analog Switch circuit

There are various kinds of analog switches classified as:

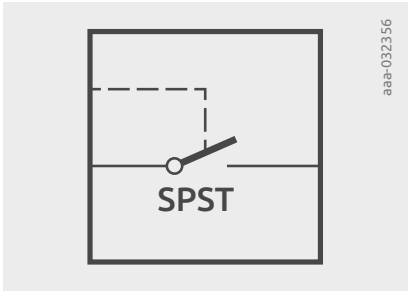


Figure 6.2a | Single pole single throw switch: one input is switched to one output

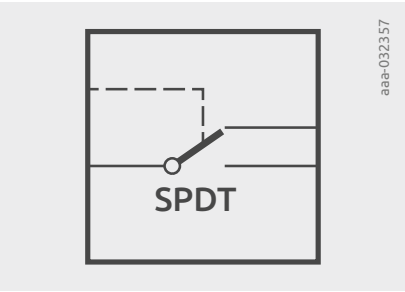


Figure 6.2b | Single pole double throw switch: one input is switched between 2 outputs

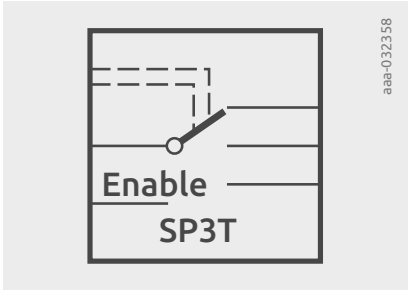


Figure 6.2c | Single pole Triple throw switch: 1 input is switched between 3 outputs

There are more permutations possible and available, such as Single pole 4 throw, Single pole 8 throw, Single pole 16 throw. In all cases, switches are bidirectional, thus input and output can be swapped.

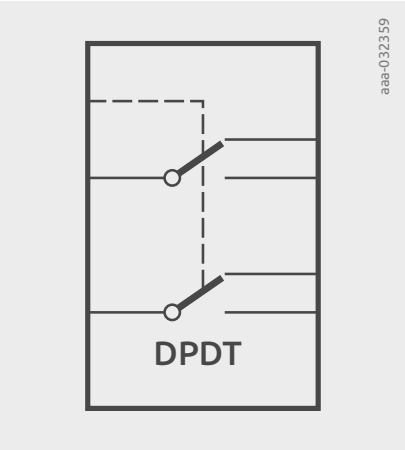


Figure 6.2d | Double pole double throw: 2 inputs are switched to 2 outputs each

Table 1: Important parameters for analog switches

Parameter	Description	Explanation
V_I	Input Voltage Range	Determines the analog signal Amplitude that can be passed without clipping
V_{IH}/V_{IL}	Switch Control Signal Levels	Digital control pin logic levels
$R_{ON(peak)}$	ON resistance (peak)	Maximum resistance of the switch when conducting
$R_{ON(flat)}$	ON resistance (flatness)	Specifies the variation of RON with input voltage
$C_{S(ON)}$ / $C_{S(OFF)}$	ON-state/ OFF-state capacitance	Total Switch and Load Capacitance affect response time, settling time, and fan out limitation
$f_{(-3dB)}$	-3dB frequency response	Bandwidth of the switch
THD	total harmonic distortion	Typical signal distortion caused by the switch
Xtalk	Crosstalk	Figure of merit for the isolation between switches
Q	Charge Injection	Defines the amount of charge coupled into the pass FET when switched on/off
MBB	Make-Before-Break	Guarantees that two Multiplexer paths are never open when signal path is changed. Disadvantage of this solution is that 2 inputs could be temporarily shorted
BBM	Break-Before-Make	Guarantees that there is only one channel active at a time and no more than one channel being active simultaneously, which excludes a scenario of two inputs being connected during transition time

Bus switches

Like analog switches, Bus switches establish an ohmic connection between terminals. In terms of functionality there are various overlaps and similarities with normal analog switches. The main difference is that Bus switches need to be able to properly disconnect in power-off mode. In a system with multiple participants sharing the same bus, access to the bus must be controlled and thus disconnecting the signal lines, also in power off mode, is an essential feature. In comparison to analog switches, the transmission speed of bus switches is typically higher with up to 500 MHz.

6.2 Asynchronous Interface Logic

In asynchronous Logic, signals are not synchronized with a clock signal. This cluster includes:

- Buffers, Inverters, Drivers with single- and multi-bit topology.
- Transceivers
- Schmitt-Triggers
- Voltage translators

Lower-drive microcontroller signals are often not capable of controlling higher-load peripherals. With high-impedance inputs and high-drive outputs asynchronous interface logic is used to improve signal integrity. Beside buffers and inverters, voltage translators are included in this section.

6.2.1 Buffers, Drivers, Inverters

A Buffer is technically a series of two Inverters which is used to refresh a weak digital signal, typically caused by a low strength drive output connected to a rather big capacitive load or many parallel inputs. The output of the buffer shall rebuild a properly shaped digital waveform and improve signal integrity. Both, non-inverting and inverting functions are available. Figure 6.3 shows the refreshing effect of a buffer.

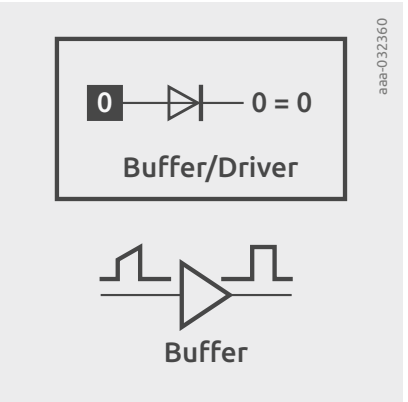


Figure 6.3 | Symbol of a buffer

6.2.2 Transceivers

A Transceiver is a bidirectional Buffer, used to receive and/or transmit data from/to a data bus. A direction control pin is used to select the direction of data flow.

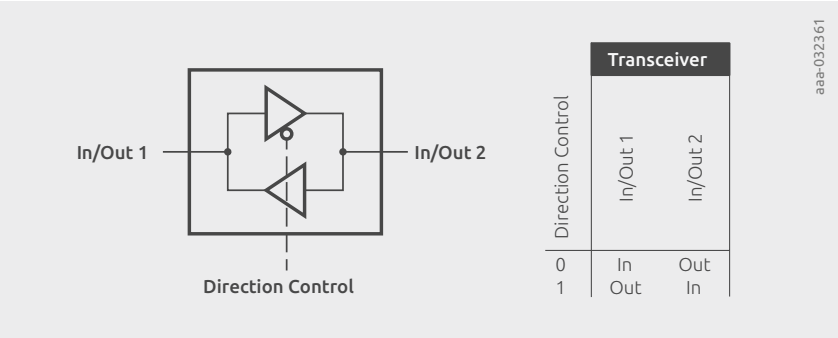


Figure 6.4 | Symbol and truth table of a transceiver

The simple transceiver is built of two buffers with direction control circuitry. Other kinds of transceivers are also including latches or registers allowing to store input values and release them to the output when needed.

Transceivers are available in many topologies such as single, dual, quad, octal, 16 or 18 bit editions related to bus connection requirements.

Various features are associated with transceivers:

- Open drain outputs
- Bus hold option for inputs maintaining the input value in case that the input is not actively driven
- Schmitt-Trigger and Schmitt-action inputs providing input hysteresis.

More information about interfacing features is available in the Interface-Chapter.

6.2.3 Schmitt-Triggers

A Schmitt Trigger device has a hysteresis behavior for the detected logic state at an input dependent on the direction of the state change. The input state and together with this also an output of a logic function does not switch at a dedicated voltage. A change of state happens later compared to a simple input if the input voltage increases or decreases towards a state change.

The distance of the transition voltages for the state changes define the width of the hysteresis called V_H. V_{T+} is the voltage where the input state changes from low level to high level whereas V_{T-} is the input voltage where the input state changes from high level to low level. In Figure 6.5 an example of a Schmitt-trigger Inverter is shown. Voltage for a state change of a Schmitt-Trigger depends on the prior state, the input tends to keep an actual state because of the hysteresis.

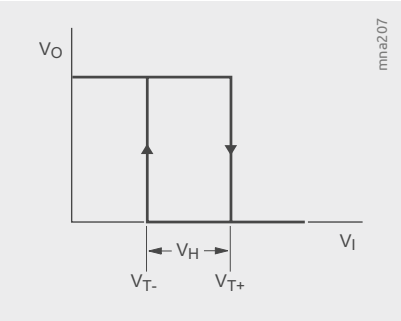


Figure 6.5 | Input to Output transfer curve for a Schmitt Trigger Inverter

This makes Schmitt Trigger inputs more stable for noisy input signals. Normal logic devices require a minimum rise and fall rate for input signals. Schmitt Trigger devices do not have such kind of restrictions because there is not a risk of undesired switching if there is noise on a smooth changing input signal.

For Schmitt Trigger components the parameter V_H, V_{T+} and V_{T-} can be found in the input characteristics of the data sheet. Devices which do feature a small width for the hysteresis of some 10 mV only are referred to as Schmitt (Trigger) action devices. This small hysteresis is not quantified in the data sheets but mentioned in the feature list.

In applications Schmitt Triggers are used for slow transition input signals and in case of noise overlay. With Schmitt Trigger Inverters, NAND or NOR gates simple oscillators can be realized. Figure 6.6 shows the example of a NAND gate-based circuit (e.g. 74HCT132). The left side NAND is coupled back from output to one input via a resistor. At this input a capacitor is applied to ground. Because of the inversion function, the capacitor is charged until the output state changes to low level, then the capacitor is discharged until the output swaps back to high level. The circuit shown works as a rectangular pulse generator. The time constant for oscillation is dependent on T = R*C. The second input of the gate works as an enable. Oscillation stops if enable is put to low level. The second gate is applied as buffer behind the oscillator.

Application example:

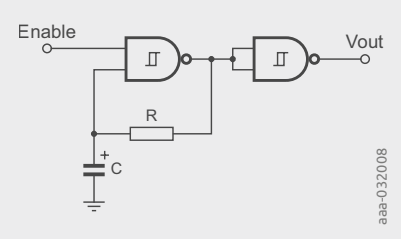


Figure 6.6 | Schmitt Trigger NAND-Gate Oscillator with output buffer gate

6.2.4 Voltage Translators

Many factors have caused the existence of the number of voltage domains in modern applications. In modular designs, newer low voltage processors might need to operate with proven peripherals which operate at higher voltages. Using translators, signals of different voltage domains can be interfaced together.
In this product section voltage translators or level-shifters with different topology can be found. The translators can be unidirectional or bidirectional with an additional direction control pin for the data flow.

Types of translations

Uni-directional

Uni-directional translators can be either high-to-low or low-to-high level translators, but the signal direction is fixed. For uni-directional translation, either single or dual supply voltage topology is possible.
There are single supply translators which can provide a voltage translation towards a lower voltage by means of an over-voltage tolerance at the inputs. This means that the logic device is supplied with 2.5 V for example and input signals from a 3.3 V-driven device are provided.

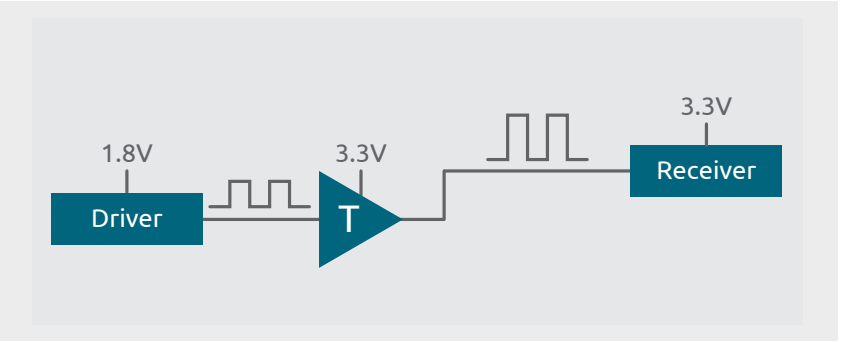


Figure 6.7 | Example showing a voltage translation device

For a translation from a low voltage towards a higher voltage logic inputs are required that feature a rather low V_{IH} rating. In this case a comparably low voltage drive can switch safely between the logical states although the supply voltage is relatively high. With open drain output devices, a level conversion from low to high level is also simple if the maximum pull-up voltage has a rather high limit.
Dual supply voltage translators give more flexibility for a level up or down translation. They have the advantage that the input levels are always perfectly matched to V_{CCA}, whereas V_{CCB} defines the output voltages.
Dedicated voltage translator devices can be identified quite easily by the letter T in the type name, e.g. 74AUP1T08 is a unidirectional, single supply device.

Bi-directional

Bi-directional translators are more flexible, both directions are supported. This is associated with dual supply voltage, a bidirectional translation with a single supply is not possible. An example of a bidirectional dual supply device is 74AUP1T45.

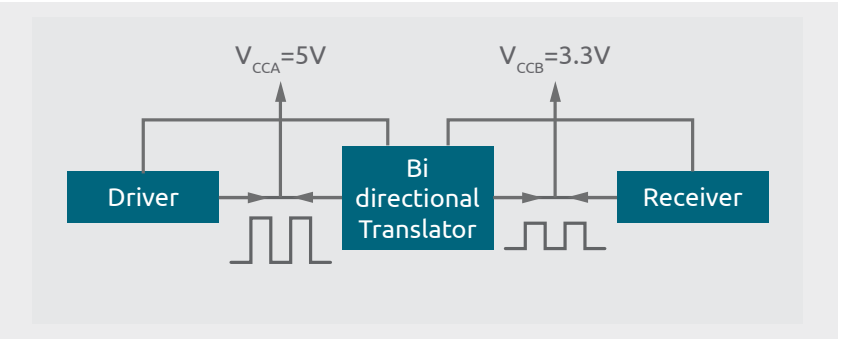


Figure 6.8 | Bidirectional translating transceiver

Dual supply versus single power supply translation

Dual-supply voltage translators can be used for Low to High and High to Low voltage translation. These devices are supplied at V_{CCA} & V_{CCB} and interface data ports A & B, operating in different voltage domains. They feature output enable (OE) and direction control (DIR) pins to enable or disable the outputs and control signal direction. They are more power efficient than the single supply solutions. Gates, buffers and shift registers are often implemented with translator function built in.

Advantage

- No ΔIcc issue as it always works with proper input voltage levels
- Low power consumption for battery operated & handheld systems
- Same interface (w.r.t firmware & hardware)
- Flexibility in translating to/from a variety of voltage nodes

Disadvantage

- Different footprint leads to change in the layout.
- Larger packages are required, extra pin for second supply.

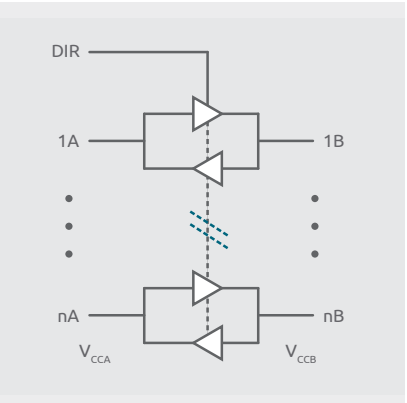


Figure 6.9 | Multi bit dual supply transceiver

6.2.5 Bi-directional translation with automatic sensing

If bi-directional translation is needed but no direction signal by the system components is available, an auto sensing translator can be used to resolve the problem. A pair of I/O spanning voltage domains can act as either inputs or outputs depending on external stimulus without the need for a dedicated direction control pin. Internally, an extra current sensing circuit detect the direction and configures the translation circuit accordingly.

LSF translators

THE LSF010x translator family is a bidirectional multi-voltage level translator with an internal pass transistor. It has a reference channel and, dependent on the type, several translation channels that can be used independently. The independent usage of the channels is meant in terms of different voltage levels as well as different directions.

Using reference channel and enable pins

The internal structure of the LSF translator is shown in Figure 6.10, as an example of an LSF0101 with one translating channel. The source of the reference channel is supplied by Vref_A, resulting in a voltage level of Vref_A + V_{TH} (~0.8 V) at the source of Vref_B and at the gates of all pass transistors in the IC. Thus, the gate voltage levels of all pass transistors is determined by Vref_A.
The enable pin of the LSF translator should be externally shorted to the Vref_B pin. If the enable pin shall be controlled dynamically, this pin should not be driven by a push-pull stage because in case of high level drive, the enable pin voltage would be forced to the supply voltage level of the driver. Instead, the enable pin should be driven with an open drain driver without a pull-up resistor, as it is already provided by Vref_B.

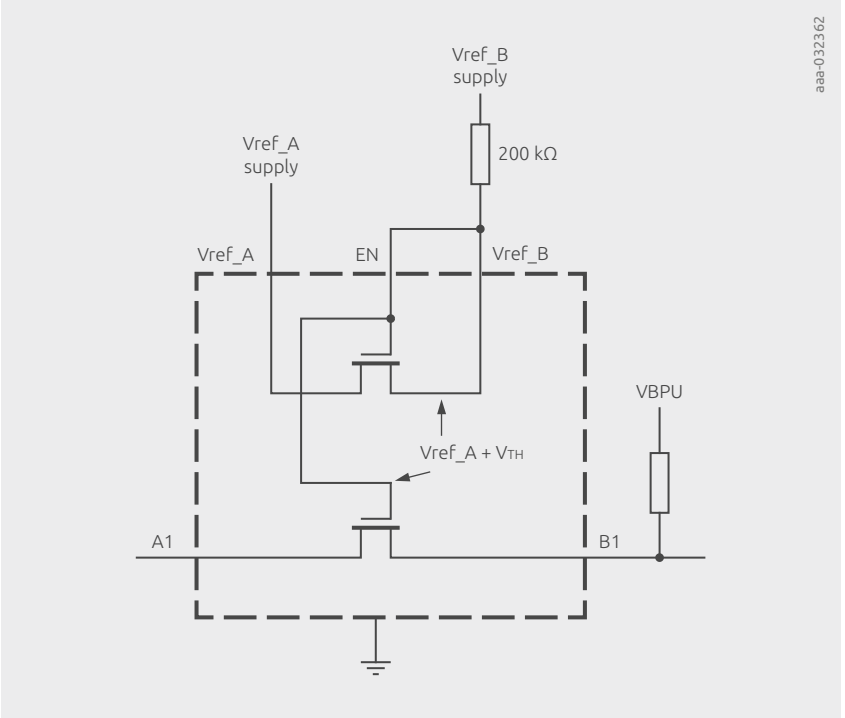


Figure 6.10 | Using enable and reference Voltage of a LSF0101 translator

Translation channel usage

If the transmitter uses a push-pull stage, the external pull-up resistors can be omitted. For open drain transmission drivers, external pull-up resistors are essential as open-drain outputs can only drive the low state actively.

Down translation

It is recommended to connect the B-side to the higher voltage. In the down translation scenario, the B-side is driving and the A-side is receiving.
When the driver is driving a low voltage, the input of the translator is pulled to low level, causing the internal transmission FET to conduct. This will open the connection to the output of the transistor and current will flow from the output through the pass transistor into the open drain of the driver. As a result, the output at the A-side is pulled down to low level.
When the driver outputs a high level, the output voltage will follow the input until the FET turns off. The output voltage will then be pulled high by via the pull-up resistor on the A-Side.

Up translation

In this use case, the A-side is driving and the B-side is receiving. When the transmitter is driving the input low, the internal pass transistor will be turned on, pulling down the output of the translator as well as in down translation scenario. When the driver is driving a high level, the output voltage will follow the input until the FET turns off. The output voltage will then be pulled high by via the pull-up resistor on the B-Side.

Multi voltage translation application Example

The LSF translator can also be used to translate different voltage levels per channel as shown in the example in Figure 6.11. It shows a scenario with one Microcontroller and three communication partners, each of them operating at a different voltage level. On the A-side, each channel is pulled up to 3.3 V via a resistor. This is important because if the Microcontroller is in receive mode, it's inputs are high impedance and without the pull-up resistors on the A-side, the input voltage of the Microcontroller I/O would have the high level of the respective transmitter from the B-side rather than the required own input voltage level.

It is also important to select the Vref_A supply voltage to the lowest in the system, in the example case in Figure 6.11, determined to 1.2 V by Receiver 2, marked with a red circle.

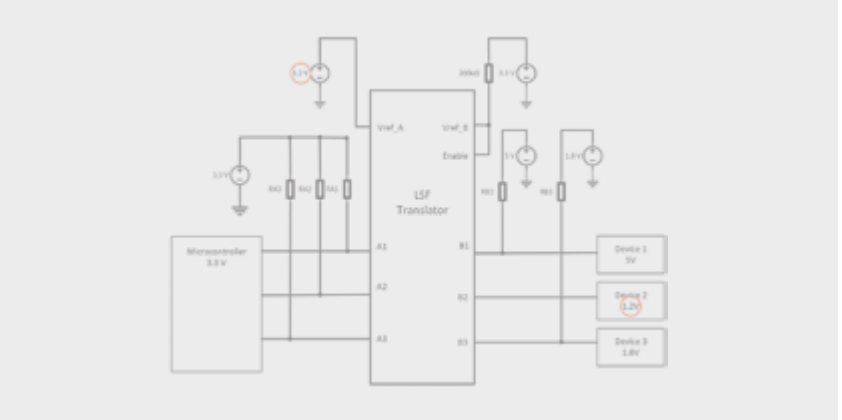


Figure 6.11 | LSF translation with multi voltage receivers

Calculating pull-up resistor values

On the A-side, pull-up resistors are only required in case of Vref_A < V_{CC} of the device on the A-side. Otherwise the A-side high level voltage will be determined by Vref_A. In case where there is only one voltage domain per side, pull-up resistors on the A-side are not needed.
For the calculation of external pull-up resistors, we assume that Vref is opening the channel of the pass transistor sufficiently so that we can use the values for Ron from the data sheet.

the pullup-resistor on the B-side shown in Figure 6.12 can be calculated using the assumptions:

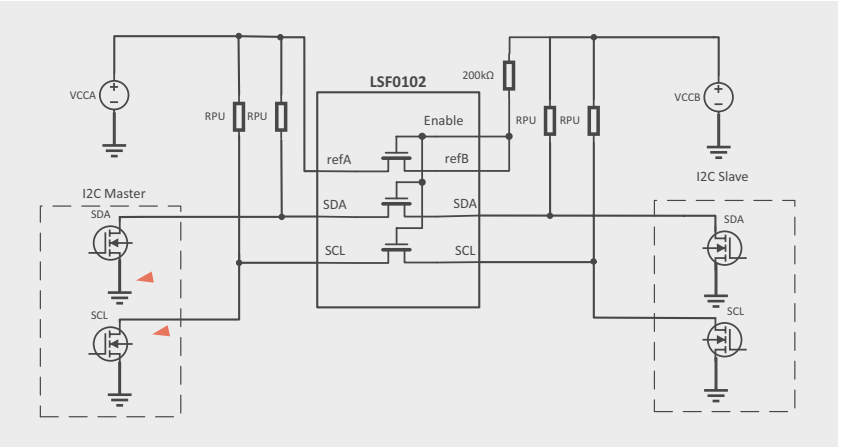


Figure 6.12 | Example of I2C translation with Master in transmission mode

The A-side is pulling down the voltage level and a current flows from B to A or the B-side is pulling low and current is flowing directly from VCCB into the target device at the B-side.

When the B-side is pulled LOW following the above assumptions, the condition will exist that the specified $V_{OL(B)}$ is higher than the $V_{IL(A)}$, so in order for the solution to operate, $V_{OL(B)}$ is lowered to be equal to $V_{IL(A)}$ in order for the I/O to register a LOW. Therefore, the voltage at B1 must be calculated to be $V_{IL(A)}$. Since no current flows through the switch, the voltage at B1 equals the voltage at A1, and the I/O is satisfied. The current path is shown in Figure 6.12. $I_{D(B)}$ is equal to the B-side driver sink current.

Equation 3 calculates Rpu when the B-side is asserted.

$$R_{pu} = \frac{V_{PU} - V_{IL(A)}}{I_{D(8)}} = \frac{3.3\ V - 0.15\ V}{15\ mA} = 210\ \Omega \quad (3)$$

The lower limit of the pull-up resistor is determined by the V_{IL} level and the drive current of the devices. The high limit of the pull-up resistor is determined by frequency requirements, too high resistance reduces the maximum frequency.

NXS translators

The second auto sense translator family we present is the NXS family. Like the LSF, it is bidirectional and capable of multi-voltage level translation. The NXS has an internal pass transistor and additional one shot circuits to accelerate rising edges of the input signals. Internal 10 kΩ pull-up resistors lift up the output voltage of a channel to the respective pull-up voltage.

To achieve faster data rates through the device, these translators include rising edge-rate acceleration circuitry to provide stronger drive for the rising edge by bypassing the integrated 10-kΩ pull-up resistors through a low impedance path during low-to-high signal transitions. A one-shot (O.S.) circuit with an associated T1/T2 PMOS transistor is used to increase switching speeds for the rising-edge input signals. When a rising edge is detected by the O.S. circuit, the T1/T2 PMOS transistors turn on momentarily to rapidly drive the port high, effectively lowering the output impedance seen on that port and speeding up rising edge inputs.

The N-channel pass-gate transistor is used to open and close the connection between the A and B ports. When a driver connected to A or B port is low, the opposite port is, in turn, pulled low by the N2 pass-gate transistor. The gate bias voltage of the pass-gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side. During a low-to-high transition, the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2), bypassing the 10 kΩ pull-up resistors, and increasing current drive capability. The one-shot is activated once the input transition reaches approximately VCCI/2, and is de-activated approximately 50 ns after the output reaches VCCO/2. During the acceleration time, the driver output resistance is between approximately 50 and 70 Ω. To avoid signal contention and minimize dynamic ICC, the user should wait for the one-shot circuit to turn off before applying a signal in the opposite direction. The pass-gate transistor T3 is on when VGS is greater than VT. When one side of T3 is held low by an external driver, with the input to T3 at 0 V, T3 will be on and the output of T3 will be held to nearly 0 V due to the on-state resistance of T3. As the input voltage rises due to a rising edge, the output voltage of T3 tracks the input until the input voltage reaches VGATE minus VT and T3 turns off. After T3 stops conducting, the input and output ports continue to rise to their respective supply voltages due to the internal pull-up resistors. In the second case, both ports start with high levels since the integrated pull-up resistors tie the inputs to the respective supply voltages, $V_{CC(A)}$ and $V_{CC(B)}$. When the input ports are pulled low by external drivers, T3 starts to conduct when VGS is greater than VT and output starts tracking the input. The source current needed for this operation must be provided by the external driver connected to the A or B port.

Input driver requirements

Since NXS level shifters are switch-type level shifters, properties of the input driver directly affect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system; the maximum data rate high-to-low output transition time (tTHL) and the propagation delay (tPHL) depend on the output impedance and the edge rate of the external driver. The limits provided in the datasheet for these parameters assume use of a driver with output impedance below 50 Ω.

Output load considerations

The maximum lumped capacitive load that can be driven depends on the one-shot pulse duration. In cases with very heavy capacitive loading, there is a risk that the output will not reach the positive rail within the one-shot pulse duration. Capacitive loads up to 150 pF can be driven without any issues using NXS level shifters.

NXB translators

NXB translators are the third bidirectional autosense translator family of Nexperia.

Figure 6.13 shows the architecture of one I/O channel of an NXB level translator. The translator incorporates a weak buffer with one-shot circuitry to improve switching speeds for rising and falling edges. When the A port is connected to a system driver and driven high, the weak 4 kΩ buffer drives the B port high in conjunction with the upper one shot, which becomes active when it senses a rising edge. The B port is driven high by both the buffer and the T1 PMOS, which lowers the output impedance seen on the B port while the one-shot circuit is active. On the falling edge, the lower one-shot is triggered and the buffer, along with the T2 NMOS, lowers the output impedance seen on the B port while the one-shot circuit is operating and the output is driven low. Figure 6.14 shows the active circuitry in the NXB I/O channel during translations from low to high and high to low.

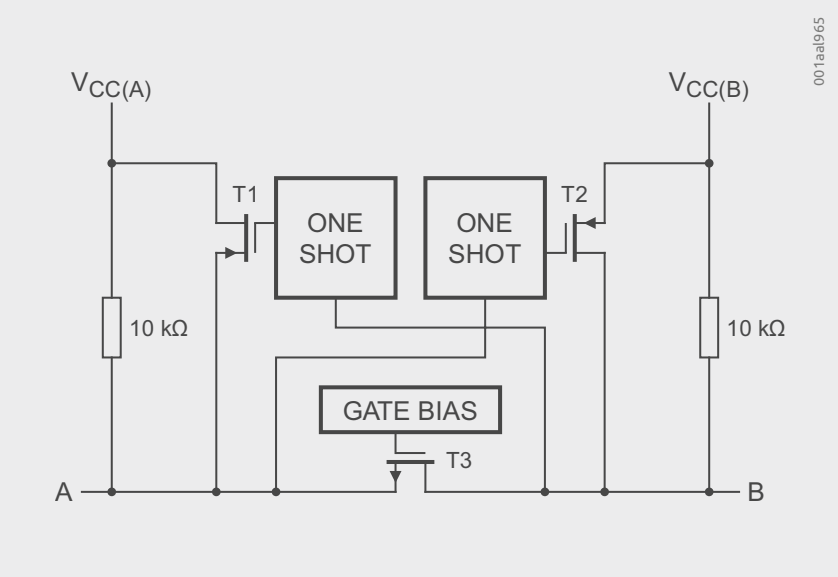


Figure 6.13 | Basic NXS Architecture

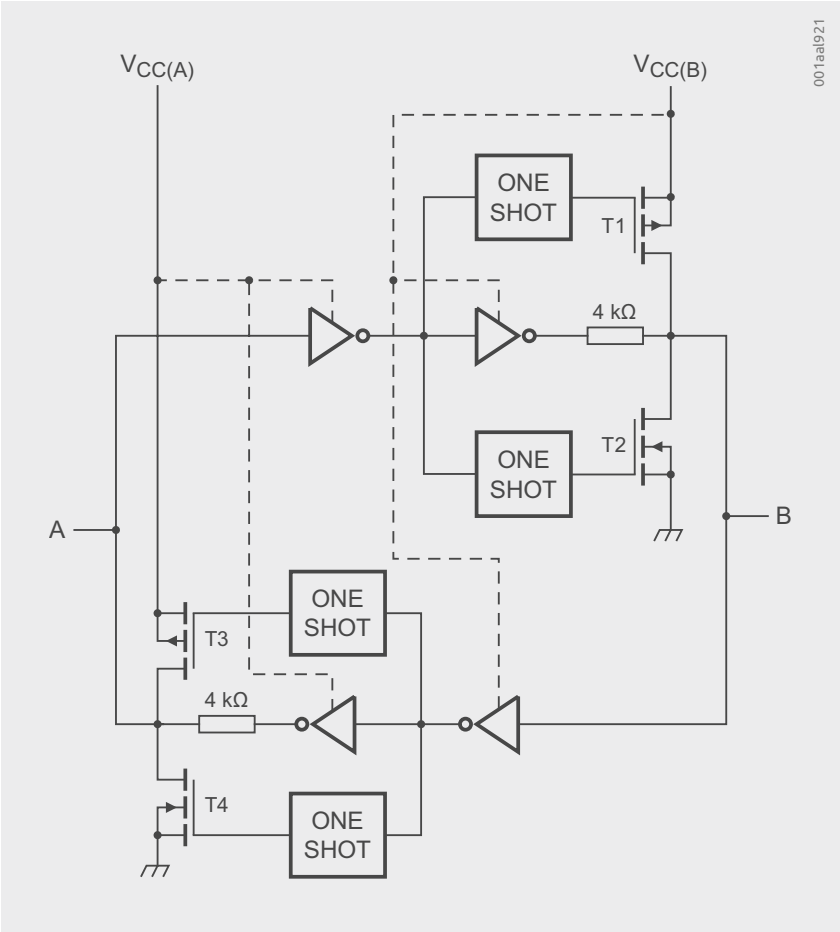


Figure 6.14 | Architecture of a NXB IO cell

6.3 Synchronous Logic

6.3.1 Flip Flops

A flipflop is a circuit with two stable conditions at the output.

An RS-Flipflop can be realized with basic gates. Figure 6.15 shows a realization with two NOR-Gates. Table 2 shows how the output reacts on the setting of the control inputs S (set) and R (reset). The input pins realize a positive control, so the flipflop can be set and reset with a high level at the corresponding input pin. With both inputs at low level, the state programmed before is stored.

If both control pins are put to high state at the same time, both outputs deliver a low state which is not a desired condition as Q and QN are not inverse anymore. After a change from this input control towards the store state, the output will acquire a random logical state. So putting both inputs to high cannot be recommended and should be avoided.

Table 2: Control table for Flipflop created with 2 NOR-Gates

Input S	Input R	Output Y	Output QN
1	0	1	0
0	1	0	1
0	0	Store	Store
1	1	0	0

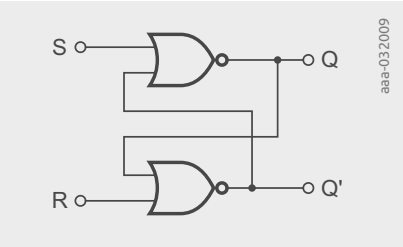


Figure 6.15 | RS-Flipflop created with NOR-Gates

If 2 NAND-Gates are connected in the same structure like the NOR-Gate approach discussed above, a circuit as depicted in Figure 6.16 is realized. We get an RS-Flipflop again but with negative control logic. This means the a low level at the set or reset input programs the state of the flipflop. With both inputs high, the storage condition is created. Putting both input pins to low is the forbidden condition which can lead to a random state after changing into the storage state.

Table 3: Control table for Flipflop created with 2 NAND-Gates

Input S	Input R	Output Q	Output $\overline{Q}$
0	1	1	0
1	0	0	1
1	1	Store	Store
0	0	1	1

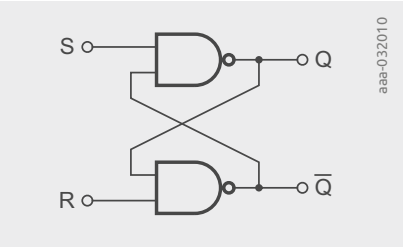


Figure 6.16 | RS-Flipflop created with NAND-Gates

6.3.2 Latch or D-flipflop with level controlled enable

A simple extension of an RS-Flipflop creates a D-Flipflop or latch like depicted in the principle schematic in Figure 6.17. The data input is one input signal to an AND-Gate which second input is connected to an Enable signal. The inverted data signal is connected to a second AND-Gate which is connected to Enable at the second input again. Behind the two AND-Gates an RS-Flipflop is placed.

If Enable is at high state the flipflop is either set or reset dependent on the state at the D-Input. While the Enable signal is high, the incoming D signal can be seen at the output Q, the latch is transparent. If Enable is low, the last state is stored.

Table 4: Function Table for Latch or level controlled D-Flipflop

Input D	Input E	Output Q
0	1	0
1	1	1
X	0	Store last state

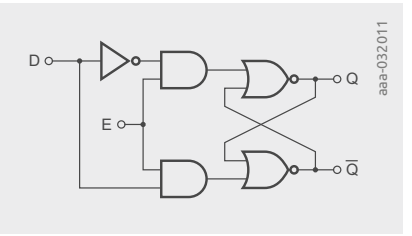


Figure 6.17 | Principle schematic of a level-controlled Latch or D-Flipflop

Different from the principle diagram in Figure 6.17, a transparent latch can be designed like shown in Figure 6.18. For Latch Enable (LE) in high state the incoming signal D is fed to the inverter towards the output, with the left side switch in on-state. The switch in the feedback loop is in off-state. If LE is turned off, incoming data are disconnected by the switch at the data input which is in off-state. The second switch feeds back the inverted QN signal to the input of the output inverter, so the current state is kept stable and stored.

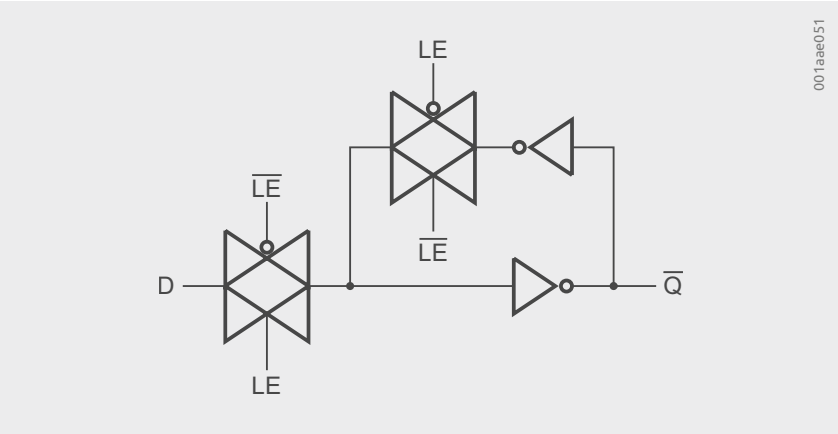


Figure 6.18 | Transparent Latch

The described level controlled D-flipflop type can also be found combined to larger multi-bit transparent latches for usage in a wider data bus. Figure 6.19 shows an 8-bit example with latch-enable control pin LE and an additional output enable OE control option with two symbol versions.

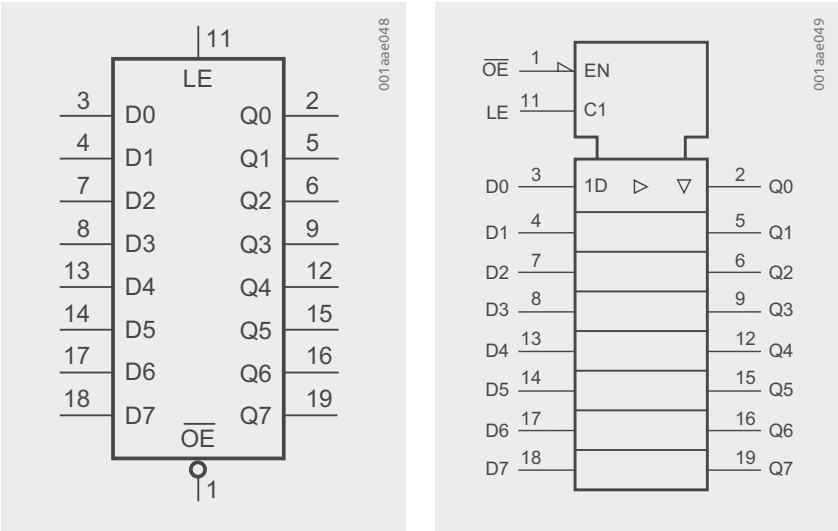


Figure 6.19 | Symbols for an 8 bit transparent latch

6.3.3 Edge triggered flipflops and registers

More complex und high speed logic designs need to be realized as a synchronous digital network. In order to cope with propagation delay variation over temperature, process spread and supply voltage, it is necessary to have an edge-driven design approach. By a defined sampling of data into storage elements with e.g. the rising edge of a master clock, different delays in the design become resynchronized and the circuit can work reliable. The overall processing delay becomes multiples of the cycle time of the clock dependent on the number of edge-controlled storage elements used in series.

6.3.4 Edge-controlled D-Flipflop

The basic element for a synchronous design is an edge-controlled D-Flipflop. Figure 6.20 shows the logic diagram of such a flipflop. There are two latched run in series. The latch enable signal, now driven by the clock signal CP (C and CN after inversion and buffering), works as described in the prior section. The control for the second latch is inverted compared to the latch at the input. While the clock is in low state, the latch placed on the data input side is transparent. The second latch is in the storage mode and outputs the logic state of the prior clock cycle. Once the clock signal changes to high state, the first latch stores the latest state from the input and the second latch becomes transparent and outputs this logical state with short delay to the rising edge of the clock.

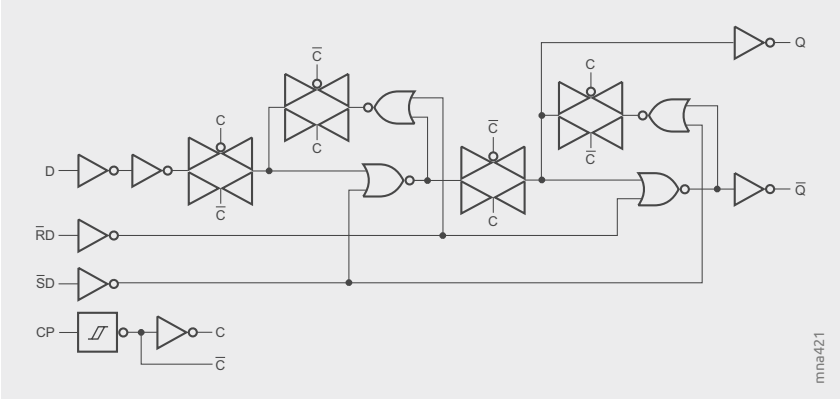


Figure 6.20 | Logic diagram of an rising clock edge triggered D-Flipflop

The schematics in Figure 6.20 includes a non-synchronous, so a direct, active low state driven set and reset function that immediately puts the latches in the circuit into the required state.

Figure 6.21 shows the IEC symbol of the described D-Flipflop with all the control pins, means a clock input for rising edge operation, a positive logic output and an inverted output, the D-input for the signal to be sampled and the low active set and reset pins for non-synchronous initialization of the flipflop.

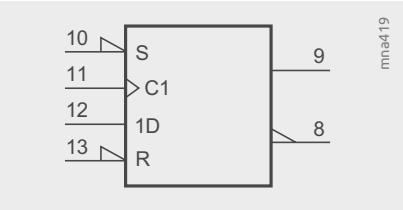


Figure 6.21 | IEC symbol of an edge-triggered D-Flipflop

6.3.5 JK-Flipflop

Another variant of an edge-controlled flipflop is a so-called JK-Flipflop. Table 5 shows the action of the flipflop dependent on the settings of the J and K input. If the input J is set to 1 while K is cleared, the flipflop will be set with the next active edge of the clock. In this case it is assumed that the flipflop works with the rising edge of the clock. If J is cleared and K is set, the flipflop is prepared to be reset with the next active clock edge. If both inputs are cleared, the flipflop stores the logical state that was present after the prior clock edge already.

Table 5: Function table of a JK-Flipflop with action on rising edge of the clock

Action	Clock	J	K	Q	$\overline{Q}$
set	▲	1	0	1	0
reset	▲	0	1	0	1
Hold/Store	▲	0	0	q	$\overline{q}$
Toggle	▲	1	1	$\overline{q}$	q

As products various variants of the flip flop type exist with either active negative edge clock operation or inverted J and K inputs. Figure 6.22 shows an example with a positive J-Input polarity and a negative polarity K input. The part also supports an asynchronous set and reset function via negative polarity activated inputs.

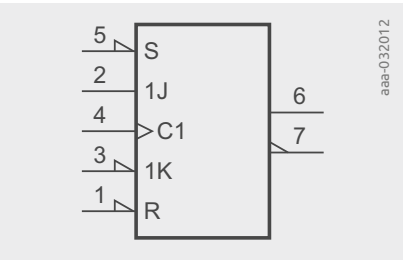


Figure 6.22 | Example of a symbol for a JK-Flipflop

6.3.6 Parallel-Registers

If many flipflop are put in parallel a register is created. It can store not a single bit only but several bits, so a multi digit word. In registers the same basic flipflop types can be found like described in the sections above. Most of the registers sample the incoming data edge-triggered. Figure 6.23 shows an example of an octal D-Flipflop register that is triggered by the positive edge of the clock signal. The outputs are enabled if the input $\overline{OE}$ is at low level.

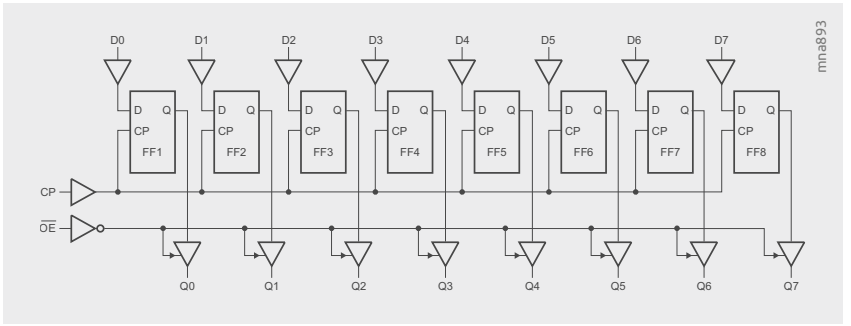


Figure 6.23 | Logic diagram of an octal register, positive clock edge triggered

In Figure 6.24 an equivalent register device based on transparent latches is depicted. While LE is high and the output are enabled, incoming data appear at the outputs. Once LE is set to low level, the latest state of the 8 bits is stored.

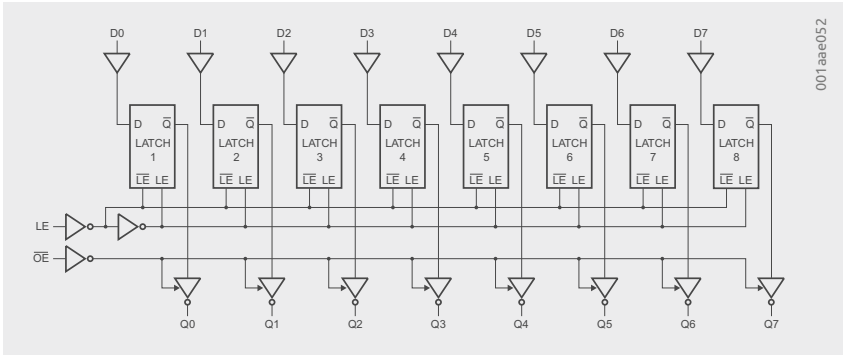


Figure 6.24 | Logic diagram of an octal transparent latch register controlled by LE

6.3.7 FIFO Registers

FiFO stands for first in first out. A FiFO Register delivers data that has been stored first also as first data to the output. Simple shift registers with a single clock work as a simple FIFO. They generate a constant delay by a number of clocks, which is the length of the shift register in bits.

More sophisticated is a flexible storage which has independent input and output clocks. Data stored into the FIFO appear at the output with the next output clock. A maximum number of data words can be stored. Such a FIFO can be used as a buffer if writing and reading clock is not identical. Input and output pointers need to be controlled correctly and it needs to be indicated whether the FIFO is empty or full. An application example is e.g. a CD-player where the output data have to run with an exact crystal clock but data read from the disc have some speed variation from the optical laser unit reading data from the rotating disc. The rotation speed has to be controlled such that the buffer FIFO compensates possible deviations of the rotation speed and thus can provide data to the output all the time. The buffer should be filled half in average, to allow a maximum safety buffer.

6.3.8 Counters

Ripple counter

If the inverted output of an edge-triggered flipflop is fed back to the D-input, the output toggles with half of the clock frequency. A clock divider by the factor 2 is created. Figure 6.25 shows the simple approach of a toggle flipflop. The state of the output is changing state with every rising edge of the clock.

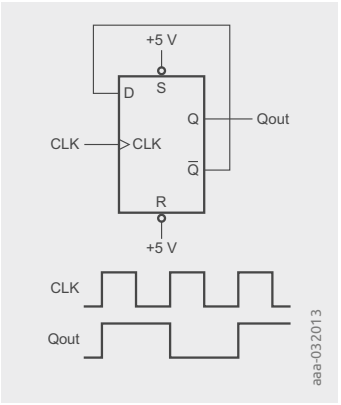


Figure 6.25 | Toggle Flipflop

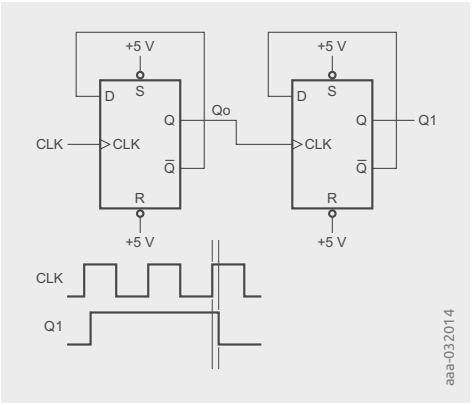


Figure 6.26 | 2 Stage Ripple-Counter

If the depicted stage of Figure 6.25 is put in series, a division of the clock by a higher factor can be realized. With N stages a division by 2^N is created for the output of the last stage in the serial structure. Figure 6.26 shows the simple example of a 2-stage Ripple-Counter which divides the clock by the factor 4. The second flipflop gets the output signal of the first stage as clock signal. Therefore the propagation delay from data input to the output of each flipflop sums up for the delay of an output Q_N according the equation: $tpd_N = (N+1) * tpd$

This behavior is the reason for the name ripple counter because state changes ripple through the entire counter from the first flipflop to the last in the series structure. If a specific state is selected by gates connected to the outputs, this can lead to spikes during the settling of the final counter condition.

Synchronous Counter

For an synchronous counter all flipflops change the state at the same time. Each flipflop gets the same clock signal. In Figure 6.27 an example of a 4-stage synchronous counter is shown. This counter supports a synchronous parallel load and reset operation. The counter has a special carry output supporting the construction of bigger counters.

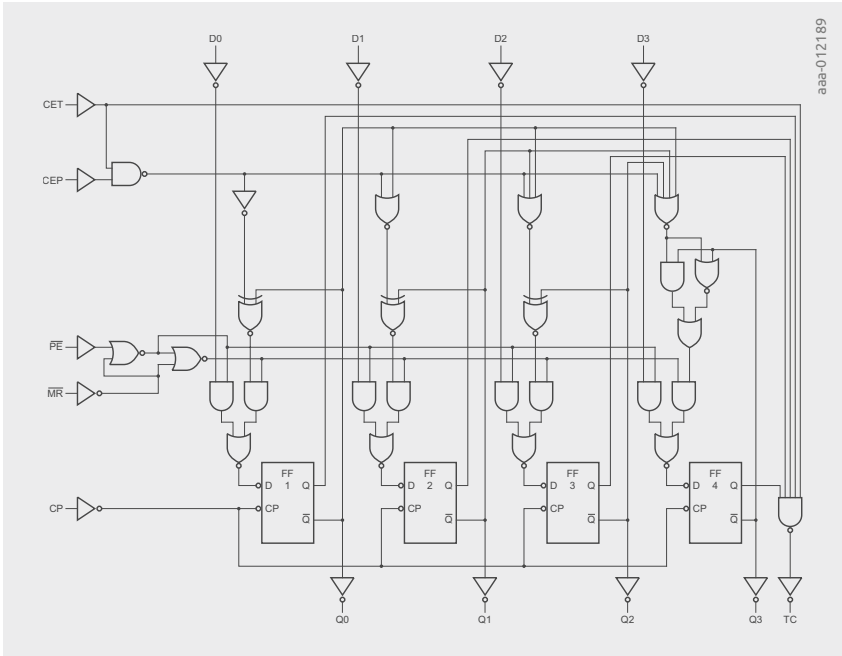


Figure 6.27 | Logic diagram of a 4-bit synchronous counter with parallel load and reset

Table 6 shows how to control the counter. A low case variable in the table indicates that the input has to be in the logical state listed at least the set-up time before the next rising edge of the clock appears. If the Reset pin $\overline{MR}$ is set to low level, the counter is cleared with the next active clock edge. This means all Outputs aquire a low state, as depicted with a capitol L in the table. The reset function has the highest priority and overrides all other functions. If the input $\overline{PE}$ is set to low level, the data applied to the Dn inputs is taken over by the flipflops with the next rising edge of the clock. If the counter shall count, both inputs, CP and CET need to be set to high level while no parallel load or reset action is initialized. For cascading of the counters, the T_C output is simply connected to the CET input of the next counter. If counter one reaches the state 15, T_C junps to high state and with the next clock cycle the second counter increments its counter state by 1.

The preset option and the reset operation can be used to modify the counter sequence. This means the counter can start at a higher value than zero by help of the parallel load or alternatively it can be reset before reaching the maximum value of 15.

Table 6: Function table of the synchronous counter shown in Figure 6.27

Operating Mode	Inputs						Outputs	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
Reset	l	▲	X	X	X	X	L	L
Parallel Load	h	▲	X	X	l	l	L	L
	h	▲	X	X	l	h	H	L
Count	h	▲	h	h	h	X	count	
Hold (do nothing)	h	X	l	l	X	X	qn	L
	h	X	X	X	l	X	qn	L

Counters are used in a lot of applications. They can be used to get exact timing windows derived from a precise clock source, to create a digital delay or to generate multiple control signals like shown in Figure 6.28. The signals can have any waveform within the distance between 2 reset signals. This could be for example a horizontal timing controller for digital TV to create memory control signals. The output register samples the outputs from the decoding block behind the counter and ensures that all signal have the same delay between clock and the outputs.

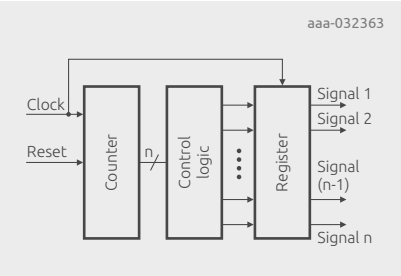


Figure 6.28 | Application example for a synchronous counter with attached decoding control network and output register

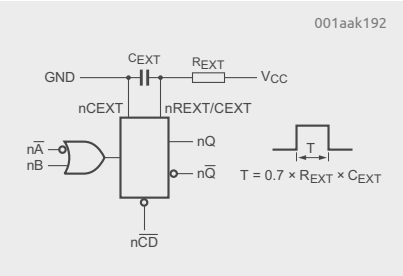


Figure 6.29 | Monostable Multivibrator

6.3.9 Monostable Multivibrator

Monostable multivibrators create an output pulse that is triggered with an edge of a digital signal. The length of the pulse is defined by a time constant realized with the selection of a proper resistor and capacitor combination. Many monostable multivibrators have a so-called retrigger function. The output pulse is extended by an additional window in time, so the output stays high, as adjusted via the RC combination restarted with every incoming trigger event. This feature can be used to detect if input pulses appear within a given time. In a conventional car the supply for the electrical fuel pump has to be turned off if no ignition pulses are present. With the described logic device such a function can be realized easily.

Figure 6.29 shows a block diagram of a monostable multivibrator which can be triggered either with the rising or falling edge of a digital signal like shown in Table 7. With $n\overline{A}$ set to high level, a rising edge at the input nB the device is triggered and the output switches to high level for the selected duration T according to the formula below.

Table 7: Function Table of a Monostable Multivibrator as depicted in Figure 6.29

Inputs			Outputs	
$n\overline{A}$	nB	nCD	nQ	$n\overline{Q}$
▼	L	H	⎍	⎍
H	▲	H	⎍	⎍
X	X	L	L	H

Big capacitors tend to change capacity over lifetime and often suffer from leakage current at high temperature. This limits the accuracy of the pulse length generated and needs to be taken into account if the devices shall be used for very long pulses.

6.4 Where to use Synchronous Interface Logic

Synchronous logic design is using a common clock signal which is provided to edge-driven flipflops in order to achieve a fully reproducible timing between processing blocks and for the whole design. A complex digital design has to be partitioned into the discrete times steps of the clock signal. If there is for example a complex decoding stage, the output of this block needs to be ready to be safely taken over by a connected flipflop stage with the next e.g. rising edge of the clock. For every assumed process spread and targeted operating temperature of the design sampling of the signals by the flipflops needs to be safe and predictable. If an asynchronous digital processing takes too long it can be necessary to introduce an additional flipflop for safe sampling of the signals.

IO expansion Logic

In case of limited IO pin count of a core processor in an application, IO expansion Logic devices can be used to generate additional interface pins.

Analog switches and Bus switches

Analog switches and Bus switches are used for IO expansion and are already described in section Analog.

Decoders/Demultiplexers

Decoders are logic devices that convert a digit al input format into another one at the output. As an example a BCD 4-bit input can be decoded to 10 separate outputs. Exactly one output is changing state for the 10 possible input combinations. Figure 6.30 shows an example for such a device. Any other combination of 3 bits at the input to 8 outputs, or a 4 bit input towards 16 outputs are further examples of decoders.

In an application the decoders can be used to select and activate a memory bank in an SSD application for example.

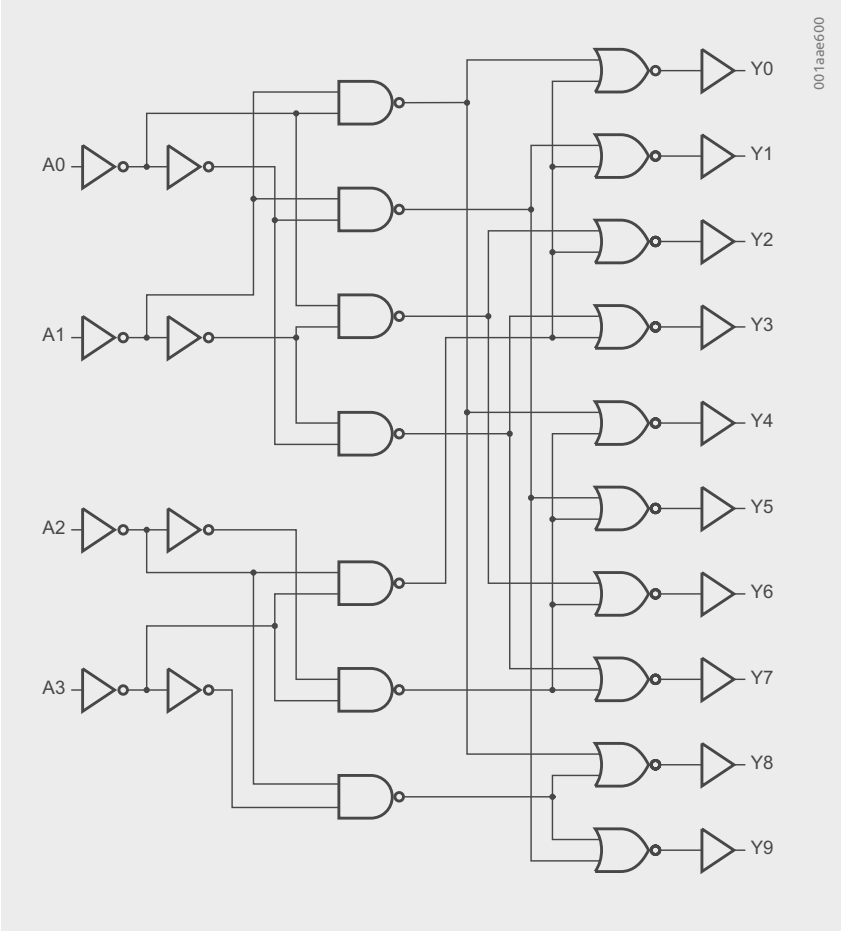


Figure 6.30 | BCD to decimal 10 outputs decoder

Digital Multiplexers

Digital multiplexers have digital inputs like a logic gate with a V_{IL}(max) and V_{IH}(min) rating. Via selection pins an input can be chosen and the incoming data stream is connected to an output. This means that data from an input to an output are re-shaped and not simply connected through like for an analog switch. Digital multiplexers can have different topologies with different number of inputs to be selected. If several multiplexers are put in parallel complete busses can be switched. Figure 6.31 shows an example of an 8 input to one output multiplexer.

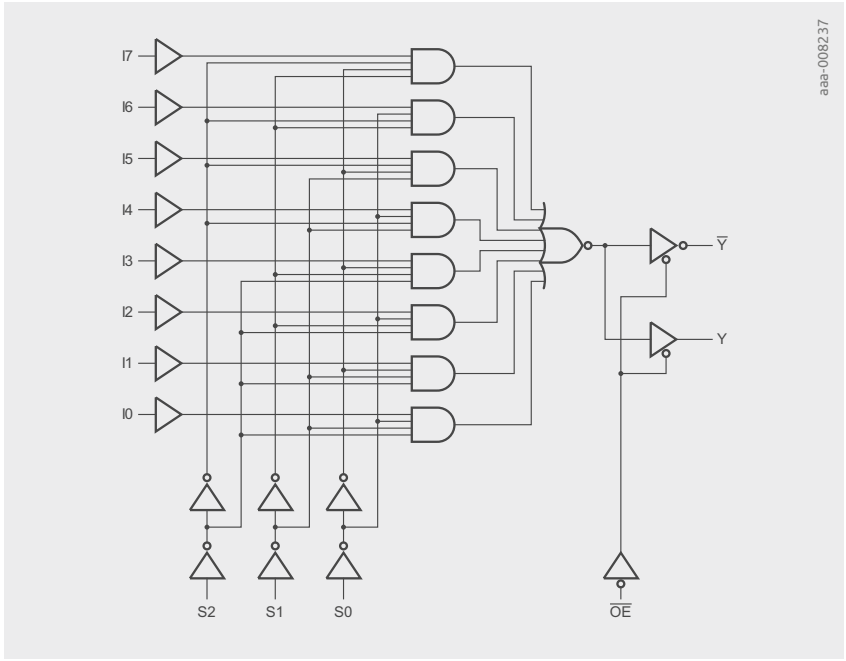


Figure 6.31 | Digital 8-to-1 multiplexer

Shift Registers

If edge-triggered D-Flipflops are put in series like depicted in Figure 6.32, a shift register is created. In the example there are 2 inputs to an AND-Gate that provides the input to the first D-Flipflop in the chain. A incoming data signal at the shift input DSA is taken over with the rising edge of the clock signal CP, if CPB is at logic high-level. The state of each flipflop is shifted to the next flipflop in the series structure with every clock cycle. Data sampled present at Q0 from FF1, appear 7 clocks later the output Q7. The whole shifter register can be cleared via the $\overline{MR}$ input.

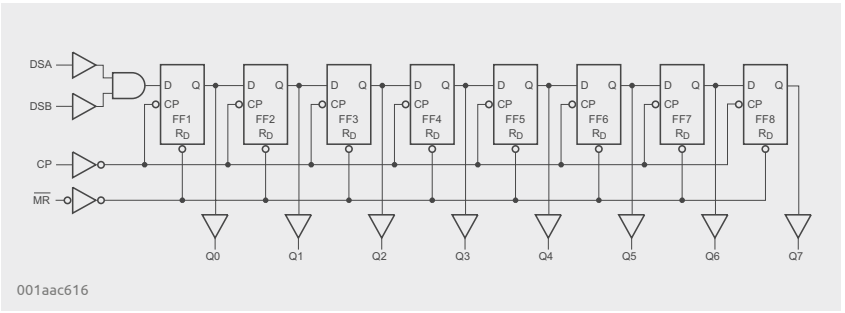


Figure 6.32 | Logic diagram of an 8-Bit Shift register

The major application area for shift registers is the serial to parallel data conversion. Therefore shift registers with an additional register connected to the outputs can be found as a useful configuration supporting this function. Once a word is shifted at the desired position in the shift register, the output register takes over this value. A new value is sampled after a new word is completed in the shift register. Figure 6.33 shows an example for such a component. SHCP is the shifting clock for the shift register. With the rising edge of STCP data are stored into the output register.

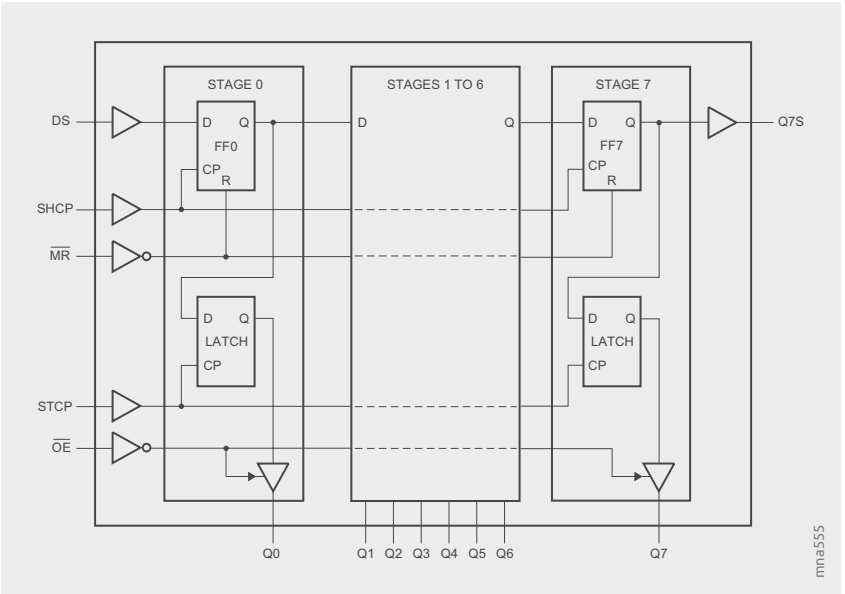


Figure 6.33 | Logic diagram of a shift register with output latch

Shift registers can be used for a parallel to serial conversion as well. This function can be realized with a shift registers featuring a parallel load function.

Figure 6.34 shows a suitable device which can convert incoming 8 bit words into a serial data stream. The parallel data is stored in the input register with the rising edge of STCP. If the parallel load input $\overline{PL}$ is at low level the clock STCP loads the input data directly into the shift register. If there is no rising clock edge while $\overline{PL}$ low, data stored in the input latch are transferred to the shift register. The shifting clock SHCP shifts data from Qn-1 to Qn and takes over new input data from the serial input DS.

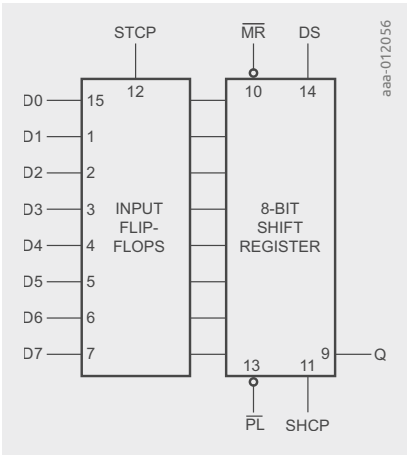


Figure 6.34 | Logic diagram of a shift register with parallel load (74HC/HCT597 as example)

Control Logic

The devices of the Control Logic segments are mainly Gates and some digital comparators.

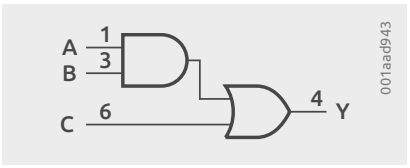


Figure 6.35 | Combination of AND and OR gate

Gates

The Gate portfolio covers simple gates like AND, NAND, OR, NOR, XOR, XNOR, some combination gates and configurable logic gates. The Basic gate functions are already well described in Chapter 2: Logic Basics.

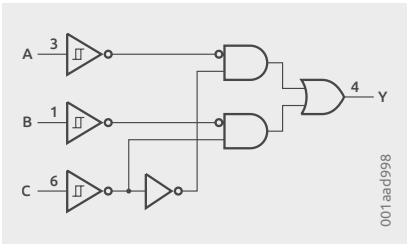


Figure 6.36 | Configurable logic gate 74AUP1G97

Combination gates are two or more discrete logic gates in a single logic solution. The integrated gates may be internally connected to generate a specific Boolean function or can remain independent. The devices include over-voltage tolerant input options and open-drain output options to facilitate interfacing between different voltage nodes. An example for a combination gate can be seen in Figure 6.35, the function is 0832: 08 for the AND gate, 32 for the OR gate.

Configurable Logic is offering various functions in a device, where the choice for the function is dependent on the external pin configuration. It can be an advantage especially when components need to be qualified for usage in an application. Flexible usage can be a factor of cost saving here. An example for a configurable gate is the 74AUP1G97, which is providing multiple configurable functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter and buffer. All inputs can be connected to V_{CC} or GND. The block diagram Figure 6.36 shows the internal circuit of the 1G97.

The possible functions that can be implemented are shown in the following figures:

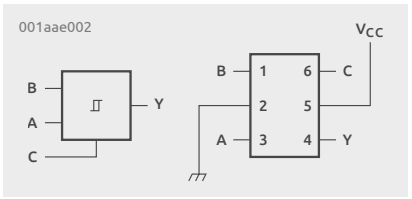


Figure 6.37a | 2-Input MUX

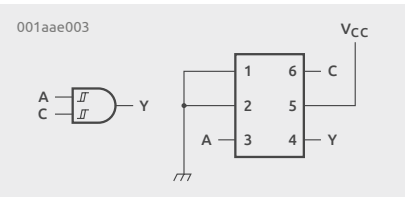


Figure 6.36b | 2-Input AND gate

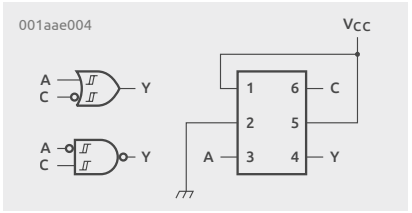


Figure 6.37c | 2-Input NAND or 2-Input OR

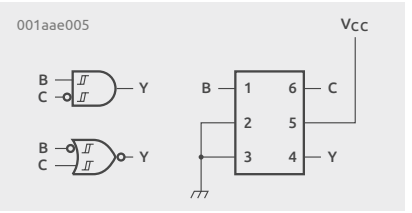


Figure 6.37d | 2-Input NOR or 2-Input AND gate

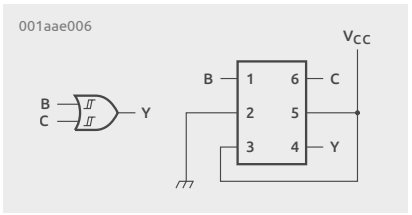


Figure 6.37e | 2-Input OR gate

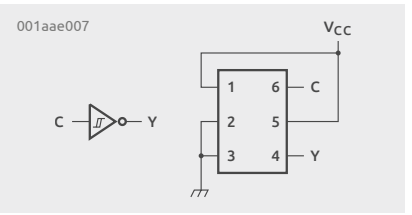


Figure 6.37f | Inverter

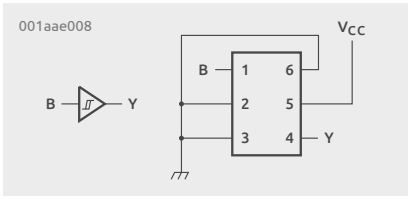


Figure 6.37g | Buffer

Digital comparators

Digital comparators perform a pairwise comparison of two input words, either 4 bit or 8 bit. The result is a one bit output indicating equality of the two input data words. This can be helpful in cases where input pins of processors are not available and only a simple comparison of data words is needed.

Chapter 7
Packages

This chapter explains and discusses various aspects of packages for Logic IC's. The sections are split into Mini Logic packages with up to 10 pins and Standard Logic packages with more than 10 pins.

7.1 Standard Logic Packages

Modern applications require improved electrical and mechanical performance, smaller size and lower cost.

Most of Logic IC packaging options support wider temperature ranges (–40°C to +125°C), and many are also offered as automotive-qualified per AEC-Q100, Grade 1 standard. Conventional logic packages such as SO and TSSOP are used in a majority of designs and it can be expected that these will be supported in the future.

In today's world, wherein ultra-compact designs can be a challenge when it comes to squeezing more functionality into a smaller space, leadless DHVQFN and XQFN packages offer smaller footprint with improved mechanical performance. Such leadless packages use pads instead of leads. These pads present a larger solderable area, creating a stronger solder interconnect with PCB. This results in a design that is more compact, and potentially more durable. Leadless packages perform better in mechanical tests like shear, pull, bend and board level thermal cycling.

For functions with more than 10 pins, DHVQFN is recommended when transitioning to leadless packages. These use the same die as TSSOP with up to 76% footprint reduction.

Table 1: Logic functions using Standard Logic package

Segment	Category	DHVQFN-14	DHVQFN-16	DHVQFN-20	DHVQFN-24	SO-14	SO-16	SO-20	SO-24	TSSOP-14	TSSOP-16	TSSOP-20	TSSOP-24	TSSOP-48	TVSOP-48	TSSOP-56	XQFN-12	XQFN-16
		SOT762	SOT763	SOT764	SOT815	SOT108	SOT109	SOT163	SOT137	SOT402	SOT403	SOT360	SOT355	SOT362	SOT480	SOT364	SOT1174	SOT1161
Asynchronous interface	Buffers/inverters/ drivers	•		•		•	•	•	•	•	•	•	•	•	•	•		
	Level shifter/ translator	•	•	•	•		•		•	•	•	•	•	•	•	•	•	•
	Printer interface													•				
	Schmitt-triggers	•				•		•		•		•						
	Transceivers			•				•				•		•	•	•		
Control logic	Digital comparators						•	•			•	•						
	Gates	•				•				•							•	
	Parity generators/ checkers					•												
I/o expansion	Analog switches	•	•		•	•	•	•	•	•	•		•					
	Bus switches	•	•	•	•	•	•	•	•	•	•	•	•	•				•
	Decoders/ demultiplexers		•		•		•		•		•		•					
	Digital multiplexer		•				•				•							
	Shift registers	•	•			•	•	•		•	•	•						
Synchronous interface	Counters/ frequency dividers	•	•			•	•	•		•	•							
	FIFO registers						•				•							
	Flip-flops	•		•	•	•	•	•	•	•	•	•	•	•		•		
	Latches/ registered drivers		•	•			•	•			•	•		•	•	•		
	Multivibrators		•			•	•				•							
	Phase locked loops						•				•							

SO
Logic functions in small outline surface mount packages

The SO or SOIC logic portfolio comprises all functions in 8-, 14-, 16-, 20-, 24-pin packages. They are surface mount packages with gull-wing pins. Pin pitch is typically 1.27 mm. SO packages provide 30 to 50% space saving compared to DIP solutions. Profile height is 70% less than DIP solutions.

Key features & benefits

- Surface mount
- 1.27 mm pitch
- Pb-free, RoHS and dark green compliant
- Temperature range −40°C to 125°C
- AEC-Q100, Grade 1 qualified
- Zero Delamination option available

TSSOP
Logic functions in thin-shrink small outline surface mount packages

The TSSOP logic portfolio comprises functions in 8-, 14-, 16-, 20-, and 24-pin packages as well as 16-bit functions in 48- 56-pin packages. They are surface mount packages with gull-wing pins. Pin pitch is typically 0.65 mm. TSSOP packages provide 35 to 65% space saving compared to SO solutions. Profile height is 35% less than SO solutions.

Key features & benefits

- Small footprint
- Surface mount
- 0.65 mm pitch
- Pb-free, RoHS and dark green compliant
- Temperature range −40°C to 125°C
- AEC-Q100, Grade 1 qualified
- Zero Delamination option available

DHVQFN
Depopulated very-thin Quad Flat-pack No-leads

The DHVQFN, sometimes abbreviated as DQFN, packages house the same silicon die as larger SO, SSOP and TSSOP packages. This ensures that along with the smaller footprint identical electrical performance is assured. Signal integrity may be improved due to lower package parasitic inductance. Its tiny size saves valuable board real estate, while the 0.5 mm pad pitch allows it to be used in existing 0.5 mm pitch assembly processes.

The package is an ideal choice for space constrained applications where PCB space and low cost assembly is critical. With their larger pads the DHVQFN packages offer easier component placement as well as improved strength, reliability, and thermal characteristics.

DHVQFN have a center pad which can be either connected to ground or to VCC or left floating, dependent on the recommendation in the data sheet. It is most important to pay attention that this pad is not accidently connected to the wrong polarity, as larger pads often suggest they are ground pads. Leaving the center pad floating is generally recommended.

To support automated optical inspection, side wettable flanks implemented on devices for automotive applications.

Key features & benefits

- Very small footprint
- Ease of assembly 0.5 mm lead pitch
- Leadless, no bent leads
- No co-planarity issues
- Pb-free, RoHS and dark green compliant
- Temperature range −40°C to 125°C
- AEC-Q100, Grade 1 qualified
- Zero Delamination
- Superior Board Level Reliability performance
- Side-wettable Flanks version optional

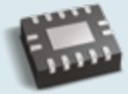
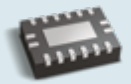
XQFN
Extremely thin quad flat package

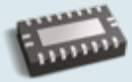
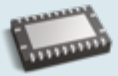
XQFN logic portfolio comprises of functions in 12 and 16 pin packages. Its tiny size saves valuable board real estate, while the 0.4 mm pad pitch allows it to be used in existing 0.4 mm assembly processes. Furthermore XQFN packages are extremely thin for height restricted applications.

Key features & benefits

- Very small footprint
- Ease of assembly 0.4 mm lead pitch
- Leadless, no bent leads
- No co-planarity issues
- Pb-free, RoHS and dark green compliant
- Temperature range −40°C to 125°C
- Extremely thin (height < 0.5 mm)
- AEC-Q100, Grade 1 qualified
- Zero Delamination option in development (Q3/20)

Table 2: Standard Logic packages

Package suffix	D	PW	BQ	D	PW	BQ	D
	SO14	TSSOP14	DQFN14	SO16	TSSOP16	DQFN16	SO20
							
Package	SOT108-1	SOT402-1	SOT762-1	SOT109-1	SOT403-1	SOT763-1	SOT163-1
Width (mm)	6.00	6.40	2.50	6.00	6.40	2.50	10.30
Length (mm)	8.65	5.00	3.00	9.90	5.00	3.50	12.80
Height (mm)	1.75	1.10	1.00	1.75	1.10	1.00	2.65
Pitch (mm)	1.27	0.65	0.50	1.27	0.65	0.50	1.27

Package suffix	PW	BQ	D	PW	BQ	DGG	DGV
	TSSOP20	DQFN20	SO24	TSSOP24	DQFN24	TSSOP48	TVSOP48
							
Package	SOT360-1	SOT764-1	SOT137-1	SOT355-1	SOT815-1	SOT362-1	SOT480-1
Width (mm)	6.40	2.50	10.30	6.40	3.50	8.10	6.40
Length (mm)	6.50	4.50	15.40	7.80	5.50	12.50	9.70
Height (mm)	1.10	1.00	2.65	1.10	1.00	1.20	1.10
Pitch (mm)	0.65	0.50	1.27	0.65	0.50	0.50	0.40

Note: The HEF4000B family uses different package suffixes than the other families.
Package suffix D corresponds to HEF4000B package suffix T and PW to TT.

7.2 Mini Logic Packages

The Mini Logic packages house the same logic families as the larger SO, TSSOP & DHVQFN packages. These packages allow the use of single gates rather than using one gate of a quad. Mini Logic packages have 10 pins or fewer. As well as reducing the complexity of board layout, Mini Logic devices are ideal glue logic to implement last minute feature additions and improve time-to-market. Their small size and lower-power consumption make them ideal for portable electronic devices.

Mini Logic is a portfolio composed of MicroPak and PicoGate packages. Leaded Mini Logic packages are known as PicoGates. They are available in TSOP, TSSOP and VSSOP with 0.95 mm, 0.65 mm and 0.5 mm pin pitch respectively. Leadless Mini Logic packages are known as MicroPak. They are available in XSON, X2SON and XQFN. They have 0.5 mm, 0.4 mm, 0.35 mm and 0.30 mm pad pitch.

Key features & benefits

- Very small footprint
- Simplify board layout
- Leaded and leadless options
- 0.95 mm, 0.65 mm, 0.50 mm, 0.40 mm, 0.35 mm & 0.30 mm pitch options
- Pb-free, RoHS and dark green compliant
- Temperature range –40°C to 125°C
- Many products AEC-Q100, Grade 1 qualified
- Zero Delamination option available
- Suitable for automotive

7.2.1 MicroPak (Extremely thin small outline no-leads)

Mini Logic leadless MicroPak packages

MicroPak XSON packages advance state of the art packaging. Originally designed for use in portable applications whose board space is limited, XSON packages allow for smaller, more compact and slimmer overall designs. MicroPak packages are an ideal choice for space constrained applications where PCB space and low cost automated assembly are critical.

XSON leadless Mini Logic packages provide up to 60% space saving over traditional leaded Mini Logic packages that are also known as PicoGate.

Table 3: Functions using Mini Logic package

Segment	Category	SOT753 TSOP-5	SOT457 TSOP-6	SOT353 TSSOP-5	SOT363 TSSOP-6	SOT505 TSSOP-8	SOT552 TSSOP-10	SOT530 TSSOP-8	SOT765 VSSOP-8	SOT886 XSON-6	SOT833 XSON-8	SOT1202 XSON-6	SOT1203 XSON-8	SOT1115 XSON-6	SOT1116 XSON-8	SOT1160 XQFN-10	SOT1269 X2SON-4	SOT1226 X2SON-5	SOT1255 X2SON-6	SOT1233 X2SON-8
Asynchronous interface	Buffers/inverters/drivers	•	•	•	•	•	•		•	•	•	•	•	•	•		•	•	•	•
	Level shifter/translator	•		•	•	•	•		•	•	•	•	•	•	•	•		•	•	•
	Schmitt-triggers	•	•	•	•	•			•	•	•	•	•	•	•		•	•	•	•
Control logic	Gates	•	•	•	•	•	•		•	•	•	•	•	•	•	•		•	•	•
I/O expansion	Analog switches	•	•	•	•	•	•								•			•	•	
	Bus switches							•	•		•									
	Decoders/demultiplexers		•		•					•		•		•						
	Digital multiplexer		•		•				•	•	•	•	•	•	•					
Synchronous interface	Counters/frequency dividers			•																
	Flip-flops	•	•	•	•	•			•	•	•	•		•	•			•	•	•
	Latches/registered drivers				•					•		•		•						
	Multivibrators					•			•		•		•		•					

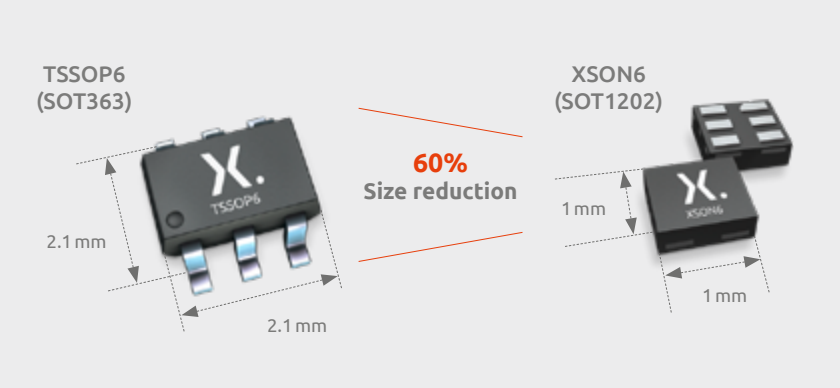


Figure 7.1 | TSSOP6 and XSON6 comparison

MicroPak packages are leadless Mini Logic packages which house the same silicon die as larger leaded PicoGate packages (refer to PicoGate section). Along with the smaller footprint, this ensures identical electrical performance. Signal integrity may also improve due to lower package parasitic inductance.

MicroPak leadless Mini Logic packages are an ideal choice for space-constrained applications where PCB space, height and low cost assembly is critical. With their larger pads, MicroPak packages offer easier component placement as well as improved strength, reliability, and thermal characteristics over similar sized BGA solutions.

MicroPak range is very broad and includes gates, analog switches, buffers/inverters/drivers, bus switches, translators, flip-flops, decoders/demultiplexers, multiplexers, latches, level-shifters, and Schmitt-trigger devices.

MicroPak solutions' tiny size saves valuable board real estate thanks to 0.5 mm, as well as state of the art 0.35 mm and 0.30 mm pad pitch while providing a more reliable bond between device and PCB. X2SON solutions are available with ≥0.4 mm pad pitch, for convenient mass production without a step-down mask.

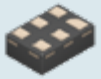
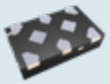
MicroPak packages include 4-pin X2SON, 5-pin X2SON, 6-pin XSON and X2SON, 8-pin XSON and X2SON, as well as 10-pin XQFN variant.

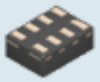
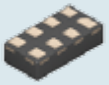
Key features & benefits

- Very small footprint
- 0.5 mm, 0.35 mm and 0.30 mm pitch options
- Low profile height (0.5 mm or 0.35 mm)
- Leadless
- No co-planarity issues
- Pb-free, RoHS and dark green compliant
- Temperature range −40°C to 125°C
- AEC-Q100, Grade 1 options available
- Zero delamination versions available

Table 4: Overview of current MiroPak packages

Package suffix	GX4	GX	GX	GN
	X2SON4	X2SON5	X2SON6	XSON6
				
Package	SOT1269-2	SOT1226	SOT1255	SOT1115
Width (mm)	0.60	0.80	0.80	1.00
Length (mm)	0.60	0.80	1.00	0.90
Height (mm)	0.32	0.35	0.35	0.35
Pitch (mm)	≥0.4	≥0.4	≥0.4	0.30

Package suffix	GS	GM	GX	GN
	XSON6	XSON6	X2SON8	XSON8
				
Package	SOT1202	SOT886	SOT1233	SOT1116
Width (mm)	1.00	1.00	0.80	1.00
Length (mm)	1.00	1.45	1.35	1.20
Height (mm)	0.35	0.50	0.35	0.35
Pitch (mm)	0.35	0.50	≥0.4	0.30

Package suffix	GS	GT	GU	
	XSON8	XSON8	XQFN10	
				
Package	SOT1203	SOT833-1	SOT1160-1	
Width (mm)	1.00	1.00	1.80	
Length (mm)	1.35	1.95	1.40	
Height (mm)	0.35	0.50	0.50	
Pitch (mm)	0.35	0.50	0.40	

MicroPak X2SON packages

The smallest logic leadless packages

First X2SON (GX) 5 pin package was introduced in 2012 to provide the smallest footprint for logic functions while ensuring pad pitch remains 0.4 mm or over, making step-down masks unnecessary. X2SON (GX) packages feature 4, 5, 6 or 8 pins and are available in low-power AUP, AXP, LV & LVC technology families, covering over one hundred logic functions. In 2018, X2SON4 was introduced; this 4-pin package option further reduces footprint by 44% compared to the 5-pin X2SON5.

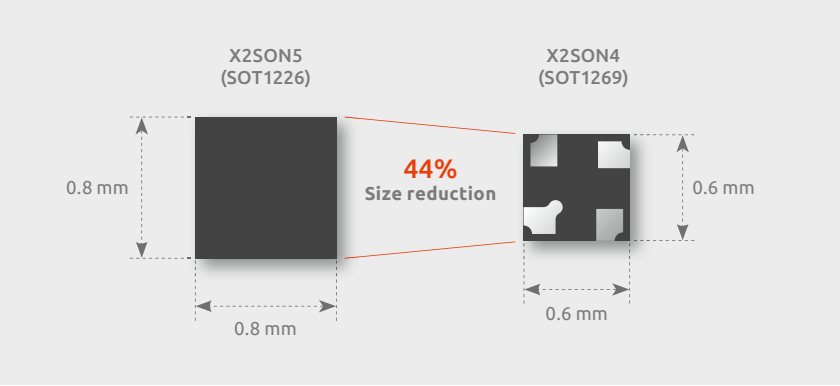


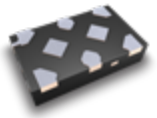
Figure 7.2 | Comparison of X2SON5 and X2SON4 package

X2SON packages are MicroPak packages also known under package suffix GX for X2SON8, X2SON6 and X2SON5 or GX4 for X2SON4. X2SON packages' tininess saves valuable board real estate and supports the miniaturization trend (see also next section regarding solder stencil thicknesses). Single, dual and triple gates are available as well as translators.

Key features & benefits

- Very small footprint (up to −36% vs. GF & −25% vs. GN packages)
- High contact area-to-chip ratio and enhanced durability
- RoHS & dark-green compliant with NiPdAu Leadframe finish
- Low profile height (0.35 mm) and low width (0.8 mm)
- Lower PCB costs, easier placement and miniaturization
- Zero Delamination

Table 5: Micropak X2SON (GX) package details

Package name	Package version		L (mm)	W (mm)	H (mm)	P (mm)	Suffix
X2SON4	SOT1269		0.6	0.6	0.32	≥ 0.4	GX4
X2SON5	SOT1226		0.8	0.8	0.35	≥ 0.4	GX
X2SON6	SOT1255-2		1.0	0.8	0.35	≥ 0.4	GX
X2SON8	SOT1233-2		1.35	0.8	0.35	≥ 0.4	GX

Trade-off: Lead pitch vs DFM incl Mask/Stencil Design

The X2SONx packages are certainly very compact, with a height of only 0.35 mm. But the most important feature is the novel placement of the contacts — by utilizing the space at the corners of the package, and for some versions, including one or even 2 terminals in the center of the part, Nexperia developed packages that provides an extremely small form factor while maintaining a pitch greater than 0.4 mm for ALL of these X2SONx versions.

To understand the full significance of this innovative design, we need to consider some details related to PCB assembly procedures.

Design for Manufacturability (DFM) is a critical factor in the success of high-volume products. At the same time, consumers expect ongoing miniaturization, especially with portable and wearable devices such as mobile phones, smart tablets, and biometric sensors. A conflict arises when package miniaturization requires a pin- or land pitch that is smaller than 0.4 mm, because this is the approximate threshold at which standard manufacturing practices can become expensive and unreliable.

When a component's pitch is less than 0.4 mm, the board-assembly process may need to be modified to ensure that reflow soldering does not result in shorts between pins. First, fine-pitch components are more likely to require costly Type 4 solder paste, rather than the standard Type 3. Type 4 paste, which has higher viscosity and smaller particle size, is more effective with small stencil apertures.

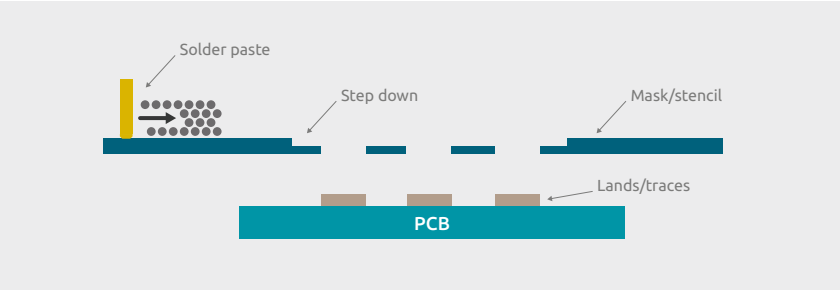


Figure 7.3 | Step down Mask technology

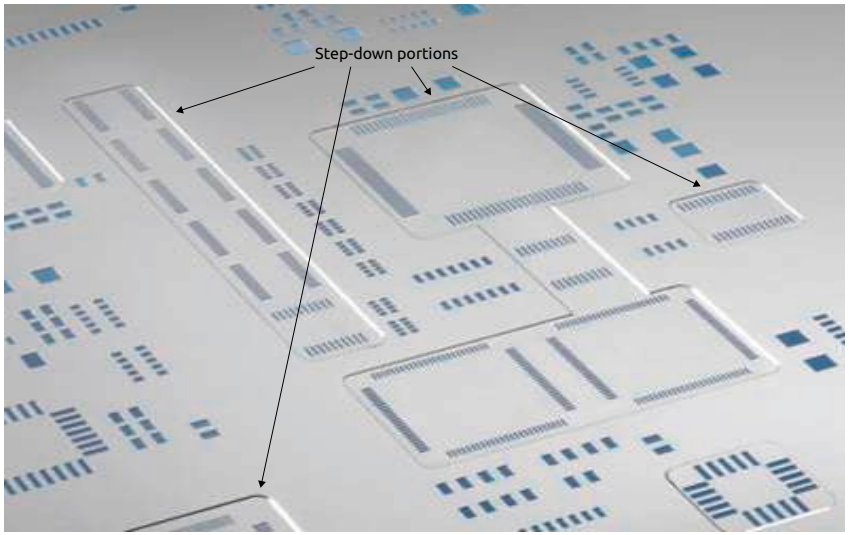


Figure 7.4 | Step down Masks on a PCB

Second, the thickness of the solder stencil must be reduced. Reducing the stencil thickness leads to a corresponding reduction in the amount of solder deposited on the pad, and this smaller quantity of solder is less likely to form a bridge between adjacent pads. In order to ensure adequate mechanical strength and accommodate smaller or tighter pitch components, the assembly process for these components with very fine-pitch will employ a so-called "step-down" stencil or mask.

Such stencils are, of course, more complex to manufacture and therefore more expensive; they are also more fragile and may need to be replaced more frequently. In addition to the increased cost, the need for a step-down stencil imposes irksome restrictions on component placement—the smaller-pitch components must be located in PCB areas that correspond to the thinner sections of the stencil.

Saving space, reducing cost

We can see from the previous discussion that X2SONx devices represent a milestone in IC packaging technology: same functionality, less board space, improved manufacturability. We achieved a significant reduction of footprint compared to GN or GF packages, while the pitch has increased to > 0.4 mm, enough to eliminate the DFM issues.

7.2.2 PicoGate (Single, dual or triple gate functions in small packages)

Single, dual or triple gate functions in small footprint packages

PicoGate portfolio comprises single-, dual-, and triple-gate functions in small 5-, 6-, 8- or 10-pin leaded packages. Compared to traditional quad-gate solutions, PicoGate allows you to select just the number of functions you need. These leaded Mini Logic packages easily allow the creation of intricate line layout patterns while saving up to 85% board space.

PicoGates are available in technology families AXP, AUP, AVC, LVC, AHC(T), HC(T), LV1T and CBTLV(D). PicoGate packages house the same logic functions as the larger SO, TSSOP & DHVQFN packages, but in single gates rather than using one gate of a quad. With the extensive portfolio of solutions, board space and lower-power consumption can be achieved.

These products are all Pb-free, RoHS and dark green compliant, and designed for use at ambient temperatures between −40°C and 125°C. Automotive variants that meet the AEC-Q100, grade 1 standard are available for a range or PicoGate solutions. PicoGate packages have a pitch of 0.95 mm, 0.65 mm, or 0.5 mm.

Nexperia's PicoGate portfolio is the industry's broadest and includes gates, level- shifters/translators, analog switches, buffers/inverters/drivers, bus switches, decoders/demultiplexers, flip-flops, multiplexers, latches and Schmitt-Trigger devices. PicoGate solutions are available in eight technology families.

Our PicoGate package range includes TSOP, TSSOP and VSSOP leaded packages (5 to 10 pins).

Key features & benefits

- Small footprint
- Simplify board layout
- 0.95 mm, 0.65 mm & 0.50 mm pitch options
- Pb-free, RoHS and dark green compliant
- Temperature range −40°C to 125°C
- AEC-Q100, Grade 1 qualified

Table 6: Picogate portfolio Parametrics and features

Family	HC(T)	AHC(T)	AUP	AVC	AXP	CBT(D)	CBTLV	LV1T
Supply voltage (V)	2 to 6.0	2 to 5.5	0.8 to 3.6	1.2 to 3.6	0.7 to 2.75	4.5 to 5.5	2.3 to 3.6	1.6 to 5.5
Propagation delay, typ (ns)	9	5	3.4	3.5	2.9	0.15	0.15	4.6
Output drive (mA)	±8	±8	±1.9	±8	±4.5	N/A	N/A	±8
Standby current (µA)	80	40	0.9	12	0.6	3	10	10
Temperature range (°C)	−40 to +125	−40 to +125	−40 to +125	−40 to +125	−40 to +85	−40 to +85	−40 to +125	−40 to +125
Automotive option	•	•	•	•		•	•	•
Features								
Over-voltage tolerant input	•	•	•	•	•	•	•	
Schmitt-trigger inputs	•	•	•		•			•
Low-threshold inputs	•	•	•		•			•
Input clamp diodes	•							•
TTL inputs	•	•				•		
Bus hold								
Power-off leakage (Ioff)			•	•	•			
Source termination								
Open-drain outputs	•	•	•		•			•
Low-delay isolation						•	•	

Table 7: PicoGate package range includes TSOP, TSSOP and VSSOP leaded packages (5 to 10 pins)

Package suffix	GW	GV	GW	GV
	TSSOP5	TSOP5	TSSOP6	TSOP6
				
Package	SOT353-1	SOT753	SOT363	SOT457
Width (mm)	1.25	1.5	1.25	1.5
Length (mm)	2.1	2.9	2.1	2.9
Height (mm)	0.95	1	0.95	1
Pitch (mm)	0.65	0.95	0.65	0.95

Package suffix	DP	DC	DP
	TSSOP8	VSSOP8	TSSOP10
			
Package	SOT505-2	SOT765-1	SOT552-1
Width (mm)	3	2.3	3.3
Length (mm)	3	2	3.3
Height (mm)	1.1	1	1.1
Pitch (mm)	0.65	0.50	0.50

7.2.3 Leads (PicoGate) or no leads (MicroPak)?

The X2SONx, like various other Nexperia logic packages, is leadless—that is, it connects to the PCB through metal pads or "lands" instead of protruding leads. There are a number of benefits associated with leadless packages. These are not specific to X2SONn devices, but it's important to recognize that these package offers not only the DFM improvements discussed already but also the following advantages over leaded devices:

- Leadless packages are actually more mechanically robust than comparable leaded packages; the pads present a larger contact area and thus allow for a stronger bond. Nexperia has abundant empirical data that confirms the reliability of leadless packages such as the X2SONn.
- The connection pads for X2SON and other leadless devices are flat metal surfaces on the bottom of the package; this eliminates assembly difficulties that can occur when the pins of a leaded package are either bent or do not exhibit sufficient coplanarity.
- Reflow soldering automatically corrects for small errors in component placement or orientation because the surface tension of molten solder naturally favors good alignment between a component and its corresponding PCB pads. However, this effect is more pronounced with leadless packages because they are smaller and lighter than comparable leaded packages.
- Even electrical performance can improve when moving from leaded to leadless devices: leadless packages offer lower parasitic inductance and thus enhanced signal integrity for high-speed applications.

Contact area vs. chip area: the key to mechanical strength

As mentioned in the previous section, leadless packages offer superior durability compared to leaded packages. The primary reason for this is quite simple: solder provides the mechanical connection between a device and the PCB, and packages that have a higher ratio of contact area to package area will have more solder relative to the size of the package/IC.

Leadless packages have far higher contact-area-to-chip-area ratio than the leaded parts. Furthermore, testing conducted by Nexperia has confirmed that leadless components can surpass leaded components in their ability to withstand both pull force and shear force.

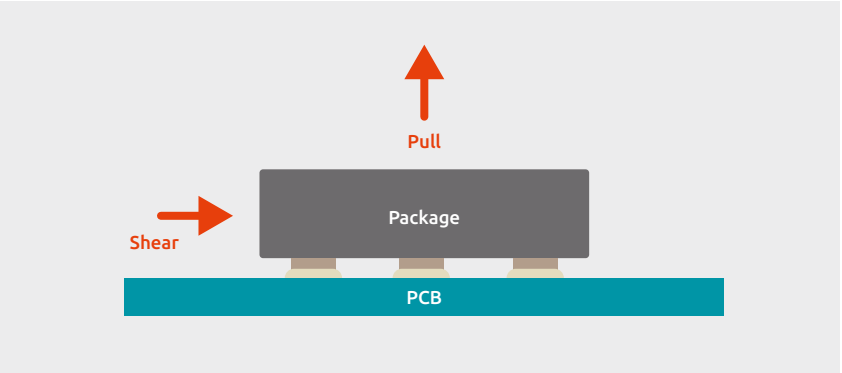


Figure 7.5 | Pull and Shear forces on a package

X2SONn devices are leadless and thus share in this enhanced durability. However, the unique geometry of the GX package with center pad(s) create an even higher contact-area-to-package-area ratio. This means that the X2SONn family of packages may be not only the world's smallest but also the world's strongest logic package.

Conclusion X2SON (GX, GX4)

Space-constrained applications have benefited immensely from the high levels of integration offered by microcontrollers, FPGAs, and sophisticated ASICs. Nonetheless, discrete logic is and will continue to be an important factor in enabling designers to produce low-cost, high-performance devices that satisfy the market's expectations for increasing portability and continuous innovation. Nexperia is committed to supplying the logic devices that engineers need, and the X2SONn packages—truly a breakthrough in IC packaging technology—are a prime manifestation of this commitment.

7.3 Package soldering aspects

Introduction

PicoGate and MicroPak packages are approximately ten to fifteen times smaller than conventional SO14 packages, providing significant miniaturization in space-constrained applications. They are available in a wide range of logic functions with a wide range of choices and deliver the right levels of performance.

PicoGate and MicroPak devices include single-, dual-, and triple-gate functions and are housed in 4-, 5-, 6-, 8- and 10-pin packages with selectable functions. To support the widest range of applications, every product in the portfolio is specified for high-temperature operation (- 40°C to +125°C). Since they perform the most popular functions and either meet or exceed competitive specifications, they eliminate single-source problems.

Picogate vs MicroPak and soldering restrictions

Picogate, or leaded SMD devices, can be soldered on PCB by 2 different solder processes called reflow process or wave soldering. The wave soldering can only be applied to leaded packages without exposed pads and lead pitches ≥0.65 mm. Leadless packages (MicroPak and also Standard Logic DHVQFN) can only be reflowed, rather than attached on board with a wave soldering process, as the pitch of the leads is smaller or equal to 0.5 mm. On top of this, any package with exposed pads, require stencil printing (reflow process).

The following note describes the mounting methods for MicroPak packages, hence using the reflow process.

MicroPak overview

Driven by applications with a very small circuit board mounting area, the MicroPak Logic family offers the most popular logic functions for space-constrained systems such as cellular phones and other portable consumer products. They can also be used as simple glue/repair logic to implement last minute design changes or to eliminate dependence on intricate line layout patterns and to simplify routing.

The MicroPak package is a plastic encapsulated package with a copper lead frame base. The package has no leads or bumps but peripheral land terminals at the bottom of the package. The terminals are soldered to solder lands on the Printed-Circuit Board (PCB), after solder paste is deposited.

MicroPak soldering information

Solder paste

Currently most of the solder pastes to be used for Nexperia's components is lead-free (Pb-free) or called SAC. Recommended is a 'no-clean'-type as due to the small stand-off height of the MicroPak, proper cleaning underneath the package is not possible.

Although low Pb-based solders (Pb ~36–38%, like Sn63Pb37) are still in use, it is advised to use Pb-free solder paste, as this is required by i.e. European legislation since July 2006.

A wide variety of Pb-free solder pastes is available, containing combinations of tin, copper, antimony, silver, bismuth, indium, and other elements. The different types of Pb-free solder pastes have a wide range of melting temperatures. Solders with a high melting point may be more suitable for the automotive industry, whereas solders with a low melting point can be used for soldering consumer IC packages.

The most common substitute for SnPb solder, is Pb-free paste SAC, which is a combination of tin (Sn), silver (Ag), and copper (Cu). These three elements are usually in the range of 1% to 4% of Ag and 0% to 1% of Cu, which is near eutectic. Well-known types are SAC105, 305 and 405, with 1,3 and 4% of Ag and 0.5% Cu resp. SAC typically has a melting temperature of around 217°C, and requires a reflow temperature of more than 235°C.

Below, the most wide-spread Pb-free solder pastes are shown:

Typical Pb-free solder	
Solder type	**Composition**
SAC 105 paste	98.5% Sn, 1% Ag, 0.5% Cu
SAC 305 paste	96.5% Sn, 3% Ag, 0.5% Cu
SAC 405 paste	95.5% Sn, 4% Ag, 0.5% Cu

A no-clean solder paste does not require cleaning after reflow soldering. If a no-clean paste is used, flux residues may be visible on the board after reflow. For more information on the solder paste, please contact your solder paste supplier.

Moisture sensitivity level and storage

The MicroPak components have a very good package moisture resistance. The Moisture Sensitivity Level (MSL) according to JEDEC J-STD-020D is MSL1, i.e. unlimited floor life under the condition of < 30°C/85%RH or in other words it is classified as not being moisture sensitive and thus does not require dry pack.

Stencil

The table below gives a first guideline regarding recommended electroformed stencil thickness for MicroPak packages with a terminal pitch of greater than or equal to 0.5 mm, between 0.4 mm to 0.5 mm and less than or equal to 0.4 mm. Side wall roughness of the apertures should be smooth to improve the solder paste release.

Typical stencil thicknesses	
Package terminal pitch	**Stencil thicknesses**
≥ 0.5 mm	150 µm
0.4 mm to 0.5 mm	100 µm or 125 µm
≤ 0.4 mm	80 µm or 100 µm

MicroPak placement

The required placement accuracy of a package depends on a variety of factors, such as package size and the terminal pitch, but also the package type itself. During reflow, when the solder is molten, a package that has not been placed perfectly may center itself on the pads: this is referred to as self-alignment. The table below gives typical placement tolerances as a function of the package terminal pitch.

Typical placement accuracies	
Package terminal pitch	**Placement tolerance**
≥ 0.65 mm	50 µm
< 0.65 mm	100 µm

Reflow soldering

The most important step in reflow soldering is the reflow itself, when the solder paste deposits melt and solder joints are formed. This is achieved by passing the boards through an oven and exposing them to a temperature profile that varies in time. A temperature profile essentially consists of three phases:

1. Preheat: the board is warmed up to a temperature that is lower than the melting point of the solder alloy. Subsequently to the preheat phase and still prior to the next phase of reflow, the soaking stage takes place with the purpose of evaporation of solvents and activation of the flux.
2. Reflow: the board is heated to a peak temperature that is well above the melting point of the solder, but below the temperature at which the components and board's Organic Solderability Preservative (OSP) finish are damaged
3. Cooling down: the board is cooled down rapidly, so that soldered joints freeze before the board exits the oven

The peak temperature during reflow has an upper and a lower limit:

- Lower limit of peak temperature; the minimum peak temperature must be at least high enough for the solder to make reliable solder joints; this is determined by solder paste characteristics; contact your paste supplier for details
- The upper limit of the peak temperature must be lower than:
  - the maximum temperature the component can withstand according to the specification
  - the temperature at which the board or the components on the board are damaged (contact your board supplier for details)

The below temperature profile for moisture sensitivity characterization is based on the IPC/JEDEC joint industry standard: J-STD-020D. The shown data is for devices with a package thickness < 2.5 mm and a package volume < 350 mm³. The temperature profile curves for a reflow process are shown in Figure 7.6. The inner curve is for fast soldering, the outer curve for slow soldering.

Table 8: temperature profile for moisture sensitivity characterization

Profile feature		SnPn eutectic assembly	Pb-free assembly
Average ramp-up rate (Tsmax to Tp)		3°C/s maximum	3°C/s maximum
Preheat	Temperature minimum (Tsmin)	100 °C	150 °C
	Temperature maximum (Tsmax)	150 °C	200 °C
	Time (tsmin to tsmax)	60 s to 120 s	60 s to 120 s
Time maintained above	Temprature (TL)	183 °C	217 °C
	Time (tL)	60 s to 150 s	60 s to 150 s
Peak/classification temperature (Tp)		235 °C	260 °C
Number of allowed reflow cycles		3	3
Time with 5°C of actual peak temperature (tp)		10 s to 30 s	20 s to 40 s
Ramp-down rate		6 °C/s maximum	6 °C/s maximum
Time 25°C to peak temprature		6 minutes maximum	8 minutes maximum

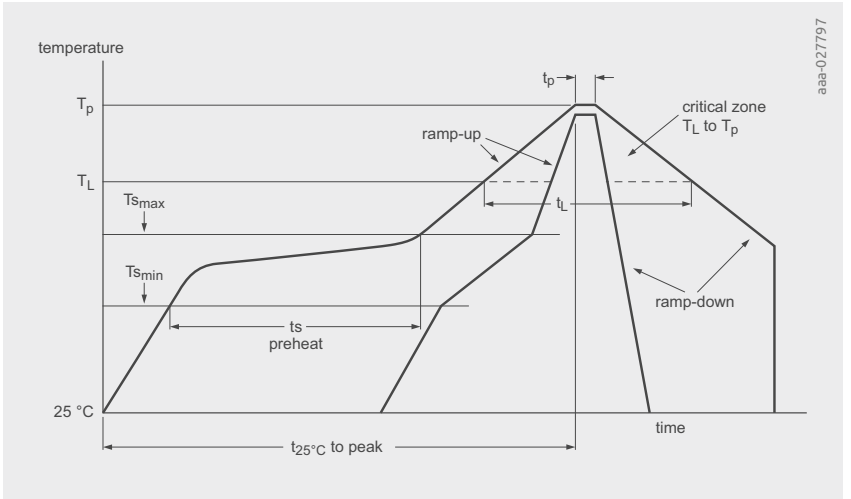


Figure 7.6 | Temperature profile of a reflow process for an XSON6 package

Every package has its own solder land information, also called reflow soldering footprint. This is normally illustrated as part of the outline-drawing available on the Nexperia Website. As an example the X2SON6 (SOT1255-2) is shown in Figure 7.7.

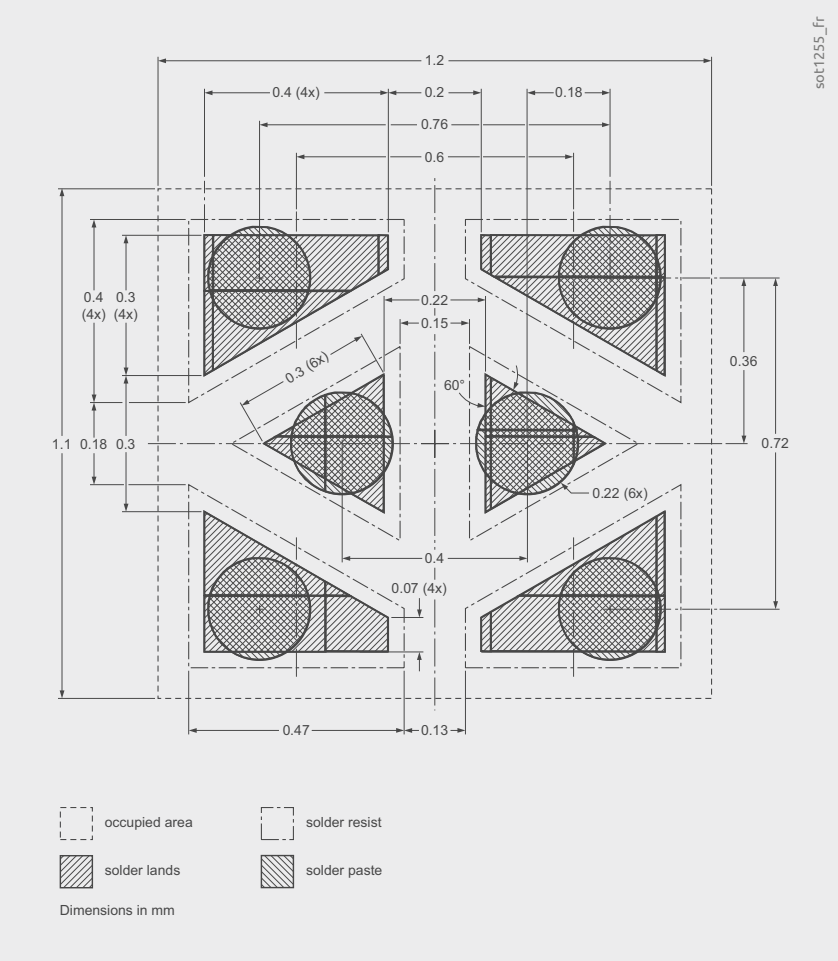


Figure 7.7 | Solder land information for an XSON6 package

7.4 Thermal resistance of packages

Logic components normally do not require or produce a lot of electrical or thermal power, however it may still be good to understand the impact of thermal resistance of the packages in the final application. Most of the times, the Printed Circuit Board (PCB) acts as heat sink for our Surface Mounted Devices, while this exposed pad (or heatsink) of the package (chip carrier to leadframe), if applicable, is directly soldered to the PCB. The thermal resistance of these packages between the chip or die and the heat sink of the package is called $R_{th(j\text{-}c)}$ (thermal resistance junction-to-case) and is measured in [K/W]. An explanation how this is measured is given in the next section.

For ease of use we will first explain the static properties of the thermal path from junction (chip or die) to PCB in its application. The internal structure of a package (simplified) consist of a die on a leadframe which is connected to the outside world via a solder layer on the PCB (see Figure 7.8).

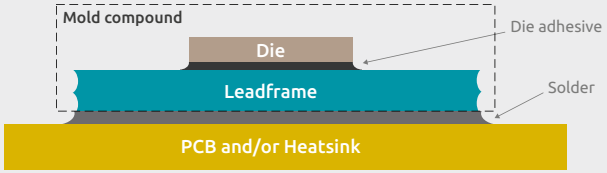


Figure 7.8 | Simplified structure of a package

This static equivalent circuit (without e.g. wirebonds) follows in analogy the electrical scheme below:

The power dissipation from the die P_D is symbolized by a current source, whereas all thermal resistances (R_{th}) are symbolized by ohmic resistors. Seen from the sketch above, the main thermal resistors are placed in sequence, with the mold compound in parallel, covering the whole structure or package. This parallel path can be neglected for most of the cases, especially having low power as valid for Logic packages.

The ambient temperature T_a is represented in the scheme below as a voltage source. With the thermal layout sketched in Figure 7.9, one can clearly distinguish between the case and the ambient impact on the performance.

The majority of the heat generated in the junction is conveyed to the case by conduction rather than convection. A measure of the effectiveness of heat conduction is the above described thermal resistance junction-to-case, $R_{th(j-c)}$, the value which is governed by the package construction of the device. Any heat transfer from the case to the surrounding air involves radiation, convection and conduction. The effectiveness of this external transfer is defined by a $R_{th(application)}$ (thermal resistance case-to ambient or application dependent value). The total thermal resistance between junction-to-ambient is consequently

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(application)}$$

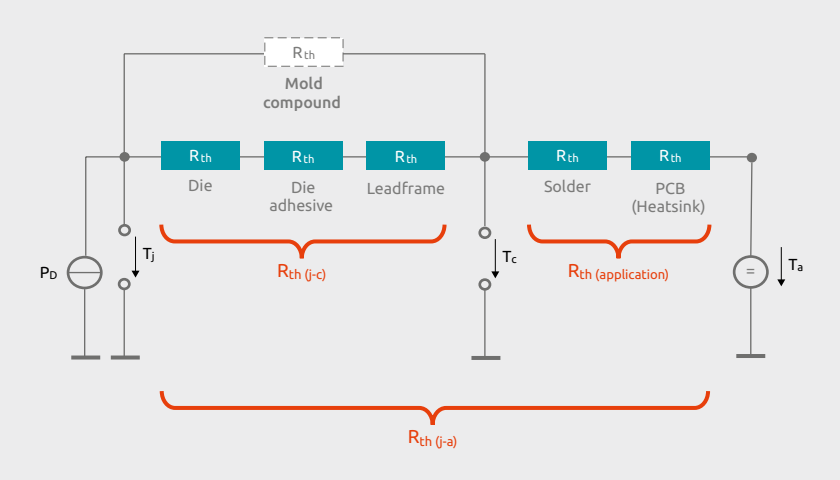


Figure 7.9 | Thermal Resistances from Junction to Ambient

The total package thermal resistance junction-to-ambient is thus application dependent, hence PCB and package connection to the board (the solder thereof) is of importance. The latter impact (ambient conditions) is often not known to the package provider. Whenever we, as Nexperia, calculate the $R_{th(j-a)}$ (thermal resistance junction-to-ambient) we have to make assumptions with a certain known PCB configuration, in our case often a PCB (1) stated by JEDEC with a 4 layer configuration and dimension of 100 × 100 mm, (2) heat transfer path top/bottom = 15 (W/m²*K) and (3) No plated through vias.

The total maximum power, P_{Dmax} of a semiconductor device can be expressed as follows

$$P_{Dmax} = \frac{T_{jmax} - T_a}{R_{th(j-a)}} = \frac{T_{jmax} - T_a}{R_{th(j-c)} + R_{th(application)}}$$

where

T_{jmax} is the maximum junction temperature and Ta is the highest ambient temperature likely to be reached under the most unfavorable conditions. The function $P_{Dmax} = f(Ta)$ or

$$P_{Dmax} = \frac{-T_a}{R_{th(j-a)}} + \frac{T_{jmax}}{R_{th(j-a)}}$$

reveals a descending straight line of gradient:

$$\frac{-1}{R_{th(j-a)}}$$

with its zero at T_{jmax}.

Derating factor

It should be noted that in the data sheets of the products from Nexperia the total power dissipation is given as a function of the package (case) temperature T_C, because the application-specific thermal resistances are not known to us. This function, like the previous one, is a descending straight line. The slope now has the value $1/R_{(th(j-c)}$. The zero remains at T_{jmax}, i.e. 150°C. The slope of this straight line is called derating factor and is measured in [mW/K]. The total power dissipation P_{Dmax} or P_{tot} remains constant until a certain T_C, at which the power derates linearly down to the T_{jmax} @ 150°C. In the example below a Package is determined by a derating of 7.8 mW/K starting at a case temperature T_C of 118°C.

The limiting case temperature T_C is defined by the die-junction temperature T_{jmax} subtracted by the multiplication of the thermal resistance $R_{th(j-c)}$ and the total power dissipation P_{Dmax}, whereas the derating factor is defined by the total power divided by the temperature difference between the die-junction temperature T_{jmax} and the "limiting" case temperature T_C defined above.

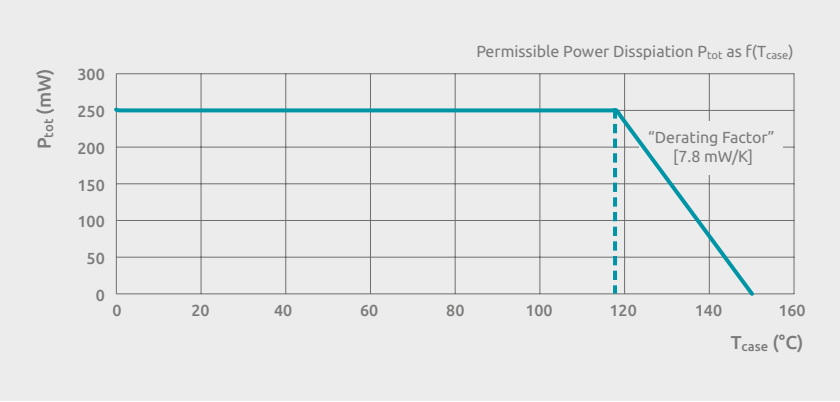


Figure 7.10 | Example of a package with a derating factor of 7.8 mW/K starting at 118°C

7.5 Thermal characterization of packages – Explanation and possible setup

All our Logic packages exhibit or consume only low thermal power, but in case of necessity for certain applications we would like to explain a bit more on thermal measurements incl some background on it. Generally speaking, only a fraction of the thermal power is exhibiting at the top side, but for completeness reasons we explain how to measure this and where it is used for:

Junction-to-Package $\Psi_{th(j-top)}$

This parameter provides a correlation between chip temperature and temperature of package at the top side. It is used to estimate chip temperature in certain applications and is not to be confounded with the thermal resistance $R_{th(j-c)}$!

Set-up:
The package must be mounted on a standard board (e.g. FR4 PCB with JEDEC defined 4 layers) with a thermocouple on top of its package. When driving this package in a standard test environment (e.g. a wind tunnel) one has to apply a KNOWN amount of power to the die while the temperature of the chip (T_j or $T_{junction}$) and the temperature of the top of the package (T_{top}) (via the thermocouple) will be measured.

Calculations:

$$\Psi_{th(j-top)} = \frac{T_j - T_{top}}{Power}$$

Again: It has to be mentioned that this $\Psi_{th(j-top)}$ is not a thermal resistance and it is only used to estimate the junction temperature from a measurement of top of package in actual applications

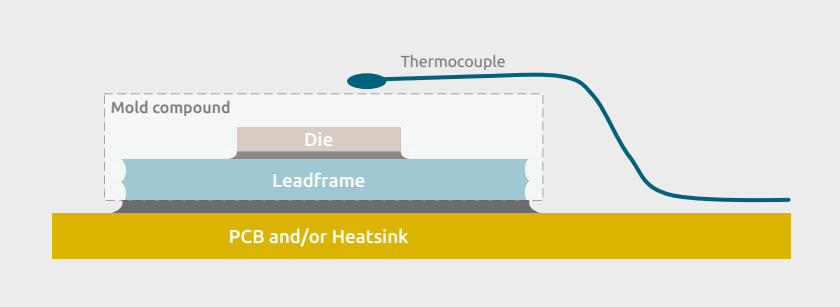


Figure 7.11 | Measurement of case temperature

Thermal Resistance Junction-to-Case $R_{th(j-c)}$

This parameter is of much higher interest and importance as this is a better reflectance of real applications in the field, including the use of external heat sinks. It represents the thermal resistance between the chip-junction temperature and the case temperature of the package in "real life", including possible external heat sinks on the package. Contribution factors, like the die, the die attach material (adhesive or solder) and leadframe, have been discussed in the former section.

Set-up to measure:
The package has to be mounted on a standard board (e.g. FR4 PCB with JEDEC defined 4 layers) or socket while the package must be in "perfect" physical (thermal) contact with a temperature stabilized plate (preferably water-cooled). Any air flow around the package has to be minimized to ensure that the whole heat flux from the package exhibits to the cold plate rather than redirected by convection and evaporation. Also here a KNOWN amount of power has to be applied to the die while the temperature of the chip (T_j or $T_{junction}$) and the temperature of the case of the package (T_c or T_{case}) will be measured. The T_{case} is different with respect to the T_{top} as it represents the temperature of the package (case) at the position where the package is connected to the heatsink, assuming that the majority of the heat flow is directed towards either top or bottom only (depending on application and design), hence no significant portion of radiation or side wall conduction exist. Therefore, the use of thermal grease or thermal pads between the package and the PCB, and or external heat sink, is highly recommended, but only in case of necessity.

Calculations:

$$R_{th(j-c)} = \frac{T_j - T_c}{Power}$$

A low thermal resistance $R_{th(j-c)}$ indicates that the heat flux from the die to the heatsink is high, hence a high absorption of the heat (thermal power) can be guaranteed. A possible setup for $R_{th(j-c)}$ measurement is sketched below:

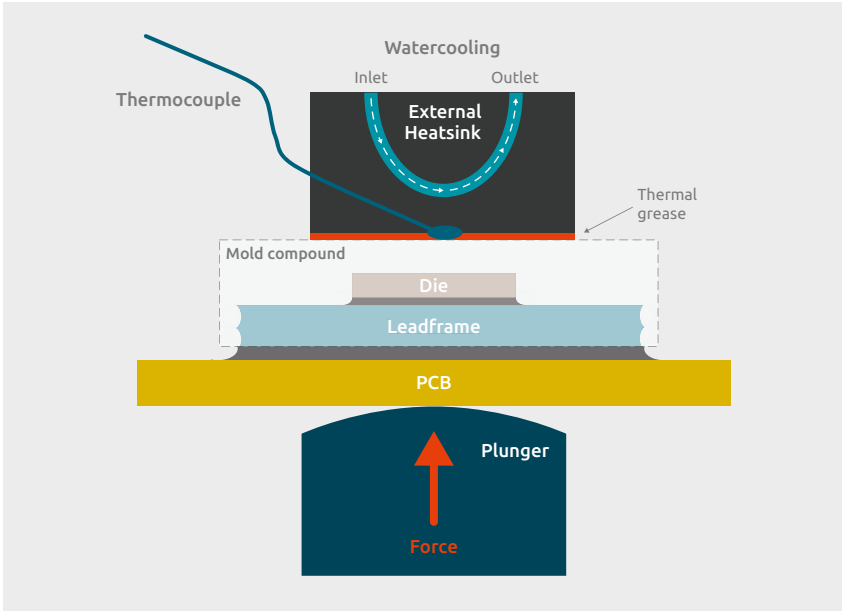


Figure 7.12 | Measurement of case temperature underneath a heat sink

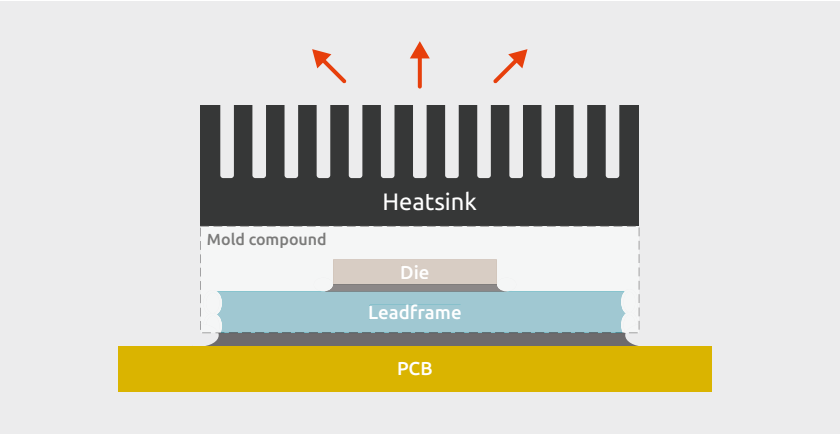


Figure 7.13 | External Heatsink on a package

For high power applications, which is unlikely for Logic IC designs, an external heatsink should be attached to the package to improve the thermal performance of the application specific part of the resistance junction-to-ambient $R_{th(j-a)}$. See sketch below.

Chapter 8

Automotive Quality

The operating environment of automobile semiconductor components is much more hostile than that of semiconductors used in the home or portable applications. For instance, A television set will generally spend its operating lifetime within an ambient temperature range of 0°C to 40°C. Due to internal heating, its semiconductor devices can be expected to operate between 20°C and 60°C. By comparison, an automobile is likely to start at temperatures lower than −20°C and, in some cases, operate within the engine compartment at temperatures approaching 150°C.

To ensure the reliability of automotive electronics, the Automotive Electronics Council introduced its AEC-Q100 standard, which outlines procedures to be followed to ensure integrated circuits meet the quality and reliability levels required by automotive applications. Due to a long history in automotive Nexperia's automotive (-Q100) portfolio meets all requirements and exceed some.

Benefits of an automotive portfolio

AEC-Q100 product qualification and reliability monitoring

Operating at elevated temperatures reduces the lifetime of a semiconductor and temperature cycling has a negative impact on the stability of a package. In cases where there is no history of a product's reliability within automotive applications, a series of stresses to simulate the life cycle within an automotive environment must be applied to guarantee conformance to the AEC-Q100 standard.

To ensure continued reliability, Nexperia logic maintains an extensive reliability monitoring program that often exceeds the AEC requirement; the results of which are published half-yearly. These QSUM reports are available upon request via your Nexperia sales representative.

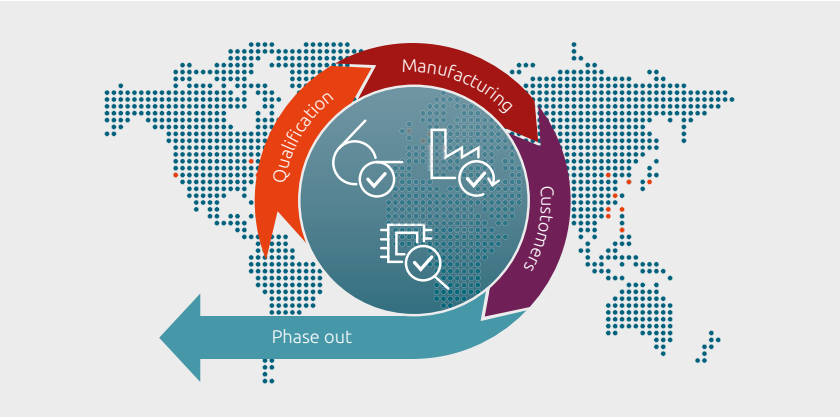


Figure 8.1 | Product life cycle

Tightened manufacturing process controls

Q100 devices are manufactured in TS16949 certified and VDA approved production facilities; they are flagged as automotive lots to ensure they receive highest priority and to facilitate traceability for improved quality analysis. Moreover, they are subjected to additional process flow quality gates and stricter rules for lot dispositioning and maverick lot handling ensures any outlier lots, which are lots that although they pass a quality gate are not within an acceptable distribution, are assigned to standard, non-automotive, types.

Six Sigma design, zero-defect test and inspection methodology

Six sigma design philosophy is applied to all Q100 devices. This ensures that an end-user application designed to the datasheet limits can tolerate a shift as high as one and a half sigma in Nexperia's manufacturing processes. As the process control limits are much tighter than one and a half sigma, this virtually guarantees trouble-free end-user applications. During the electrical test process, average test limits or statistical test limits are applied to screen outliers within automotive lots.
Figure 8.2 shows the distribution of devices passing a test and the calculated statistical test limits in yellow. Although the outliers are within the upper and lower specification limits, they are not delivered as Q100 products.

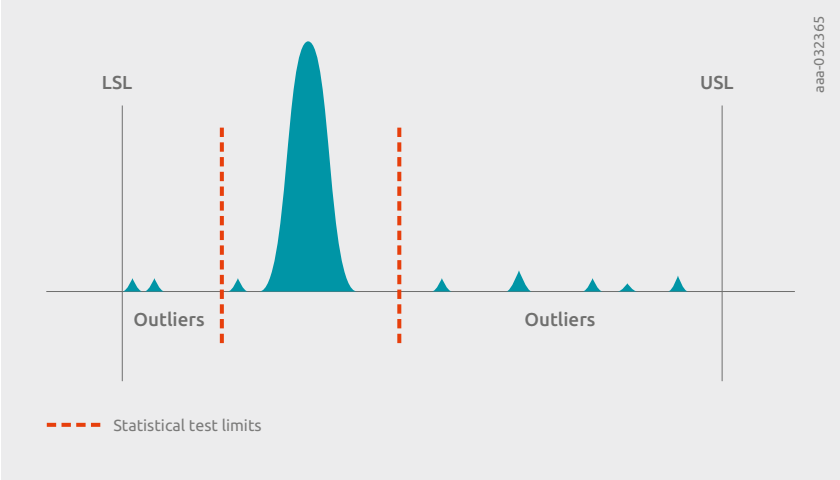


Figure 8.2 | Application of statistical test limits

Dedicated website and datasheets

A summary of Nexperia logic's Q100 portfolio including a search by function and a parametric search within each function can be found at *www.nexperia.com/products/automotive/logic*, and unlike the standard types, each Q100 device has a dedicated datasheet confirming that it has been qualified in accordance with AEC-Q100 and is suitable for automotive applications.

Priority technical support

Nexperia's first and second tier technical support teams give Q100 product design-in assistance their highest priority, and upon request, AEC-Q100 production part approval process (PPAP) qualification data will be made available. Due to the stricter qualification requirements of automotive end-user applications, a 180-day process change notification (PCN) approval cycle is applied for Q100 products instead of the 90 day PCN approval cycle for standard types. In the unlikely event of a quality issue, Nexperia logic guarantees a 10 day through put time with initial verification within 24 hours for its Q100 portfolio.

Chapter 9

Logic Families

Nexperia offers a wide range of Logic process families. The overview of all families with properties and features is given in the following tables. In the following chapters, the most important focus process families are described in more detail. The structure for each chapter is:

Structure of the Logic process family chapters

- Construction: brief description of process properties like gate length, input capacity and other properties that devices of this family have in common
- Input Output structure: some information specific to the interface structure such as voltages and features
- Input Output figures: Simulation figures for I/V curves are shown here. Very useful for analysis of interface behaviour.
- Operating conditions: the specified properties from the data sheets are listed in tables, such as limited and recommended conditions, static and dynamic characteristics. Generally valid for devices of the respective process family
- Power calculation: a formula is given here, as well as in the data sheets
- Special features: some families have special feature, i.e. Bus hold on inputs. These are described here.

Overview of the Nexperia's Logic process family portfolio:

Table 1: High voltage families

Family	ABT	AHC(T)	CBT(D)	HC(T)	HEF	LV-A(T)	LVnT	LVC	NPIC
Supply voltage (V)	4.5 to 5.5	2 to 5.5	4.5 to 5.5	2 to 6.0	3 to 15	2 to 5.5	1.6 to 5.5	1.6 to 5.5	4.5 to 5.5
Propagation delay, typ (ns)	2	5	0,25	9	90	3,4	3,1	1,7	5
Output drive(mA)	-0,5	±8	N/A	±8	±3	±12	±8	±24	±100
Standby current (µA)	500	40	3	80	600	20	10	10	200
Temprature range (°C)	−40 to +85	−40 to +125	−40 to +85	−40 to +125	−40 to +85	−40 to +125	−40 to +125	−40 to +125	−40 to +125
Automotive option		•	•	•	•	•	•	•	•
Portfolio									
Standard Logic	•	•		•	•	•		•	•
Mini Logic		•	•	•			•	•	
Features									
Over-voltage tolerant inputs		•	•	•*		•	•	•	•
Schmitt-trigger inputs		•		•	•	•		•	
Low-threshold inputs		•		•			•		
TTL inputs	•	•	•	•		•			
Input clamp diodes				•	•				•
Power-off leakage (Ioff)	•					•		•	
Open-drain outputs		•		•		•		•	•
Low-delay isolation			•						

* 4049 & 4050 functions only

Table 2: Low voltage families

Family	ALVC	ALVT	AUP	AVC	AXP	CB3Q	CBTLV(D)	AUP1T	LVC	LVT
Supply voltage (V)	1.2 to 3.6	2.3 to 3.6	0.8 to 3.6	1.2 to 3.6	0.7 to 2.75	2.3 to 3.6	2.3 to 3.6	2.3 to 3.6	1.2 to 3.6	2.7 to 3.6
Propagation delay, typ (ns)	2	1,5	3,4	1	2,9	0,2	0,15	4	4	2
Output drive(mA)	±24	-32/64	±1.9	±8	±4.5	N/A	N/A	±4	±24	-32/64
Standby current (µA)	40	90	0,9	20	0,6	400	10	1,5	20	120
Temprature range (°C)	–40 to +85	–40 to +85	–40 to +125	–40 to +85	–40 to +85	–40 to +85	–40 to +125	-40 to +125	–40 to +125	–40 to +85
Automotive option	•		•	•			•	•	•	•
Portfolio										
Standard Logic	•	•		•		•	•		•	•
Mini Logic			•	•	•		•	•		
Features										
Over-voltage tolerant inputs	•*	•	•	•	•	•	•	•	•	•
Schmitt-trigger inputs	•		•		•			•	•	•
Low-threshold inputs			•		•			•		
Input clamp diodes								•		
Bus hold	•	•		•					•	•
Power-off leakage (Ioff)		•	•	•	•	•		•	•	•
Source termination	•	•							•	•
Open-drain outputs			•		•				•	
Low-delay isolation						•	•			

* Non bus hold versions only

9.1 The HC/HCT/HCU Logic Family

Introduction to family / General description

The 74HC/HCT/HCU high-speed Si-gate CMOS logic family combines the low power advantages of the HEF4000B family with the high speed and drive capability of low power Schottky CMOS. The family has the same pin-out as older 74 series and provides the same circuit functions.

The basic family of buffered devices, designated as 74HC, operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as 74HCT with the same features and functions as the "HC-types", will operate at standard TTL power supply voltage (5 V ± 10%) and logic input levels (0.8 to 2.0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the 74HCU, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal-controlled oscillators and other types of feedback circuits which operate in the linear mode.

Construction

The HC/HCT/HCU family devices are built in a the 5 V CMOS technology with a gate length of 1.2 micron. The process technology is Pb-Free, RoHS and Dark Green compliant. Bond wiring is done with copper.

Input Output structures

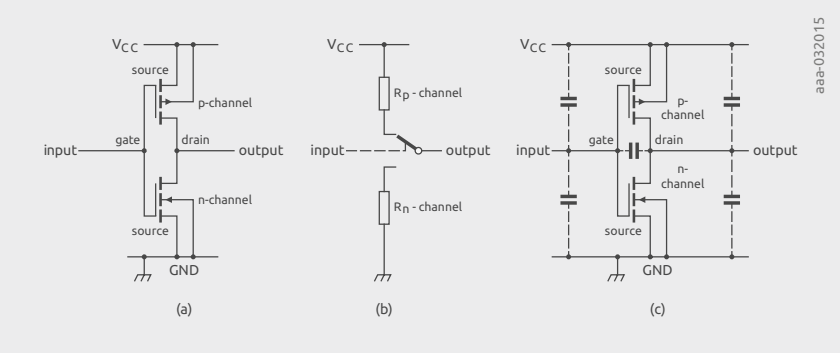


Figure 9.1 | Input structure of HC(T) family devices

The input structure of the HC/HCT/HCU logic family provides ESD protection and low capacitive coupling

Latch-up protected inputs:

Latch-up is the creation of a low-impedance path between the power supply rails caused by the triggering of parasitic bipolar structures (SCRs) by input, output or supply over-voltages. These overvoltages induce currents that can exceed maximum device ratings. When the low-impedance path remains after removal of the triggering voltage, the device is said to have latch-up.

Overvoltage protected inputs:

Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

ESD protection: the input structure has rail-to-rail Diodes, as illustrated in Figure 9.2.

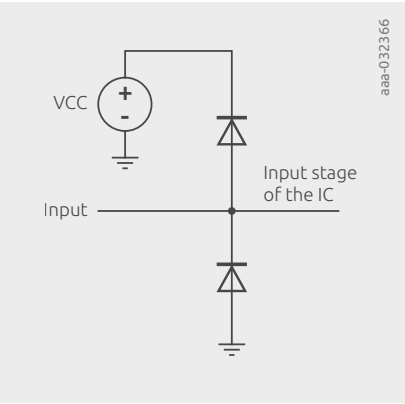


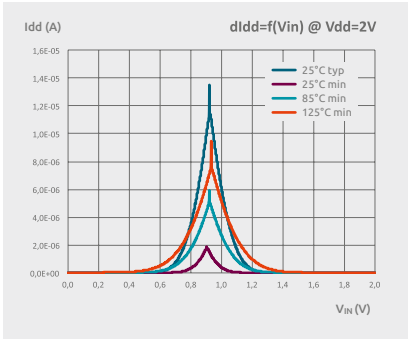
Figure 9.2 | ESD protection circuit for HC(T) input stages

HBM JESD22-A114F exceeds 2000 V
MM JESD22-A115-A exceeds 200 V

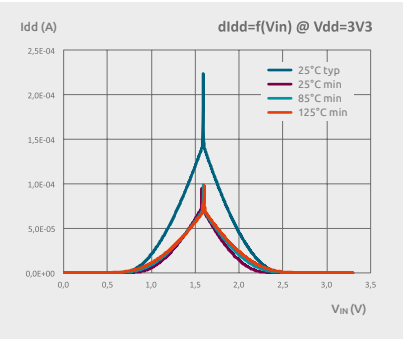
It is recommended to drive all logic inputs with a defined value, not to leave them floating

Input Output characteristics

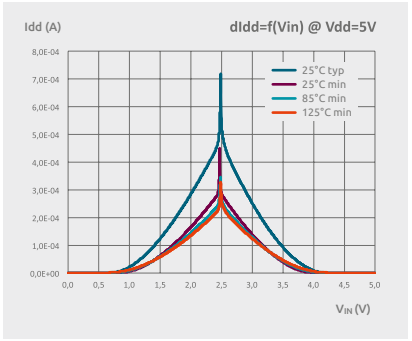
Input characteristics



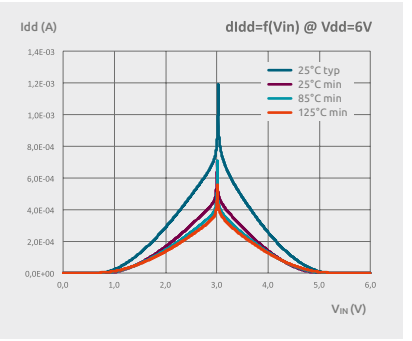
HC input curves at 2V



HC input curves at 3V3

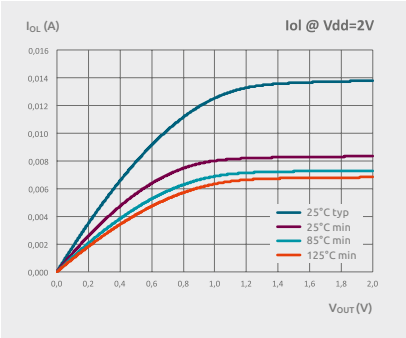


HC input curves at 5V

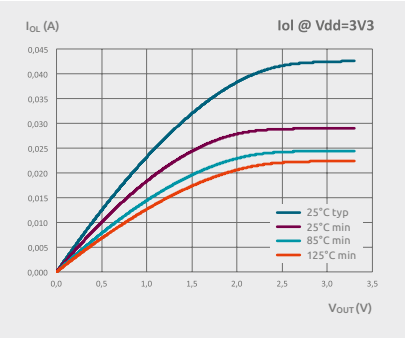


HC input curves at 6V

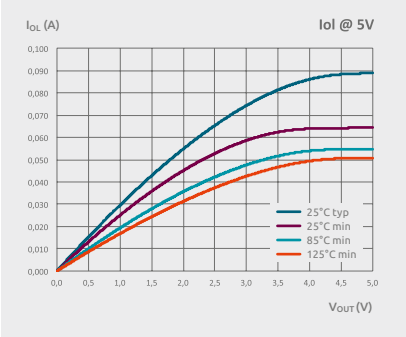
Output characteristics



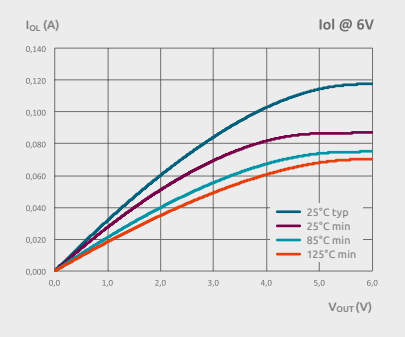
HC output curves at 2V



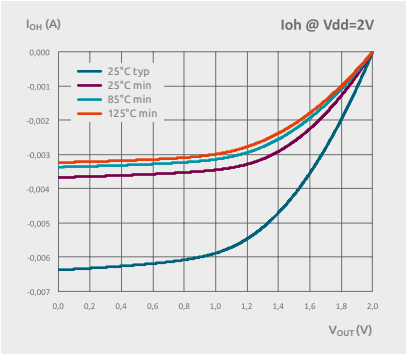
HC output curves at 3V3



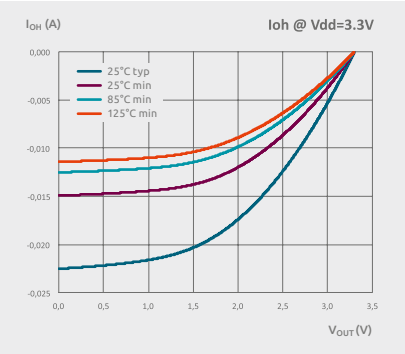
HC output curves at 5V



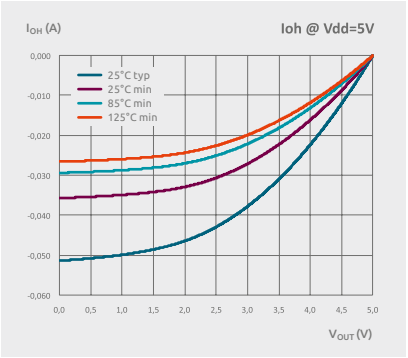
HC output curves at 6V



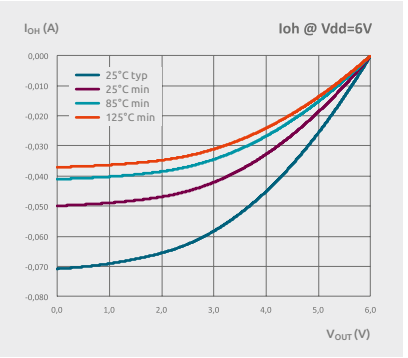
HC output curves at 2V



HC output curves at 3.3V



HC output curves at 5V



HC output curves at 6V

Operating Conditions

Table 3: Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0,5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	–	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	–	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	–	±25	mA
I_{CC}	supply current		–	+100	mA
I_{GND}	ground current		−100	–	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation		–	500	mW

Table 4: Recommended operating conditions

Symbol	Parameter	Conditions	74HC74-Q100			74HCT74-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2,0	5,0	6,0	4,5	5,0	5,5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	–	–	625	–	–	–	ns/V
		V_{CC} = 4.5 V	–	1,67	139	–	1,67	139	ns/V
		V_{CC} = 6.0 V	–	–	83	–	–	–	ns/V

Table 5: Static characteristics

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
74HC74-Q100								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1,5	1,2	–	1,5	–	V
		V_{CC} = 4.5 V	3,15	2,4	–	3,15	–	V
		V_{CC} = 6.0 V	4,2	3,2	–	4,2	–	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	–	0,8	0,5	–	0,5	V
		V_{CC} = 4.5 V	–	2,1	1,35	–	1,35	V
		V_{CC} = 6.0 V	–	2,8	1,8	–	1,8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = −4.0 mA; V_{CC} = 4.5 V	3,84	4,32	–	3,7	–	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5,34	5,81	–	5,2	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = 4.0 mA; V_{CC} = 4.5 V	–	0,15	0,33	–	0,4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	–	0,16	0,33	–	0,4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	–	–	±1.0	–	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	–	–	40	–	80	µA
C_I	input capacitance		–	3,5	–	–	–	pF
74HCT74-Q100								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 to 5.5 V	2,0	1,6	–	2,0	–	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 to 5.5 V	–	1,2	0,8	–	0,8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V						
		I_O = −4 mA	3,84	4,32	–	3,7	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V						
		I_O = 4.0 mA	–	0,15	0,33	–	0,4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	–	–	±1.0	–	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	–	–	40	–	80	µA
ΔI_{CC}	additional supply current	$V_I = V_{CC}$ − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 to 5.5 V; I_O = 0 A						
		per input pin; nD, nRD inputs	–	70	315	–	343	µA
		per input pin; nSD, nCP input	–	80	360	–	392	µA
C_I	input capacitance		–	3,5	–	–	–	pF

* All typical values are measured at T_{amb} = 25 °C.

Table 6: Dynamic characteristics

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
74HCT74-Q100								
t_W	pulse width	nCP HIGH or LOW						
		V_{CC} = 2.0 V	100	19	–	120	–	ns
		V_{CC} = 4.5 V	20	7	–	24	–	ns
		V_{CC} = 6.0 V	17	6	–	20	–	ns
		nSD, nRD LOW						
		V_{CC} = 2.0 V	100	19	–	120	–	ns
		V_{CC} = 4.5 V	20	7	–	24	–	ns
		V_{CC} = 6.0 V	17	6	–	20	–	ns
t_{rec}	recovery time	nSD, nRD						
		V_{CC} = 2.0 V	40	3	–	45	–	ns
		V_{CC} = 4.5 V	8	1	–	9	–	ns
		V_{CC} = 6.0 V	7	1	–	8	–	ns
t_{su}	set-up time	nD to nCP						
		V_{CC} = 2.0 V	75	6	–	90	–	ns
		V_{CC} = 4.5 V	15	2	–	18	–	ns
		V_{CC} = 6.0 V	13	2	–	15	–	ns
t_h	hold time	nD to nCP						
		V_{CC} = 2.0 V	3	−6	–	3	–	ns
		V_{CC} = 4.5 V	3	−2	–	3	–	ns
		V_{CC} = 6.0 V	3	−2	–	3	–	ns
f_{max}	maximum frequency	nCP						
		V_{CC} = 2.0 V	4,8	23	–	4,0	–	MHz
		V_{CC} = 4.5 V	24	69	–	20	–	MHz
		V_{CC} = 5 V; C_L = 15 pF	–	76	–	–	–	MHz
		V_{CC} = 6.0 V	28	82	–	24	–	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} [3]	–	24	–	–	–	pF

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
74HCT74-Q100								
t_{pd}	propagation delay	nCP to nQ, nQ [1]						
		V_{CC} = 4.5 V	–	18	44	–	53	ns
		V_{CC} = 5 V; C_L = 15 pF	–	15	–	–	–	ns
		nSD to nQ, nQ [1]						
		V_{CC} = 4.5 V	–	23	50	–	60	ns
		V_{CC} = 5 V; C_L = 15 pF	–	18	–	–	–	ns
		nRD to nQ, nQ [1]						
		V_{CC} = 4.5 V	–	24	50	–	60	ns
		V_{CC} = 5 V; C_L = 15 pF	–	18	–	–	–	ns
t_t	transition time	nQ, nQ [1]						
		V_{CC} = 4.5 V	–	7	19	–	22	ns
t_W	pulse width	nCP HIGH or LOW						
		V_{CC} = 4.5 V	23	9	–	27	–	ns
		nSD, nRD LOW						
		V_{CC} = 4.5 V	20	9	–	24	–	ns
t_{rec}	recovery time	nSD, nRD						
		V_{CC} = 4.5 V	8	1	–	9	–	ns
t_{su}	set-up time	nD to nCP						
		V_{CC} = 4.5 V	15	5	–	18	–	ns
t_h	hold time	nD to nCP						
		V_{CC} = 4.5 V	3	−3	–	3	–	ns
f_{max}	maximum frequency	nCP						
		V_{CC} = 4.5 V	22	54	–	18	–	MHz
		V_{CC} = 5 V; C_L = 15 pF	–	59	–	–	–	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} − 1.5 V [3]	–	29	–	–	–	pF

* All typical values are measured at Tamb = 25 °C.
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

Power calculations

Static Power Consumption can be calculated by the following:

Ps (Static Power) = I_{CC} (supply current) + Delta I_{CC} (per input where $V_{in} = V_{CC} - 2.1\,V$) + Ii (input leakage current per input when $V_{in} = 0$ or 5 V) + Iout (sum of all output current)

Dynamic Power Consumption for the device can be calculated by the following equation:

C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$$P_D = C_{PD} \times {V_{CC}}^2 \times f_i \times N + \sum [C_L \times {V_{CC}}^2 \times f_o]$$

Where:

f_I = input frequency in MHz
f_O = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in V
N = number of inputs switching
$\sum [C_L \times V_{CC}^2 \times f_O]$ = sum of outputs

Special Features

Bus Hold, Unbuffered output, Schmitt vs Schmitt Action (particularly for confusion on LVC family), onboard translation as specific to that particular family

Summary

- Input levels:
  For 74HC00: CMOS level
  For 74HCT00: TTL level
- Complies with JEDEC standard no. 7A
- Multiple package options
- Specified from -40C to +125C

9.2 The AHC/AHCT Logic Family

Introduction to family / General description

The AHC/AHCT family is an Advanced version of the HC/HCT family with lower noise, lower power consumption, higher speed (lower propagation delay), higher output drive current and overvoltage protected inputs. Functions are pin compatible with HC/HCT devices and available as both standard (quad/hex/octal) and MiniLogic (single/dual/triple) versions.

Applications

The AHC family is designed for operation from 2.0 to 5.5 V to provide support for CMOS level designs while the AHCT family is optimized for operation at TTL levels (4.5 to 5.5 V). All devices can support up to 8 mA output drive current.

The key applications addressed by this logic family are:

- Industrial applications in general
- Consumer electronics
- Computer peripherals
- Communications

Construction

AHC/AHCT devices are built on a 1.2-micron process on an 8 inch wafer production facility. All devices use copper wire bonds.

Input Output structures

All AHC/AHCT devices have overvoltage tolerant inputs, allowing input signals to exceed the Vcc supply ($V_{in} = 5.5\,V$ max regardless of V_{CC}). External driving of the output pins should be limited to V_{CC}.

Inputs are protected from ESD damage (HBM EIA/JESD22-A114E exceeds 2000 V, MM EIA/JESD22-A115-A exceeds 200 V, CDM EIA/JESD22-C101C exceeds 1000 V).

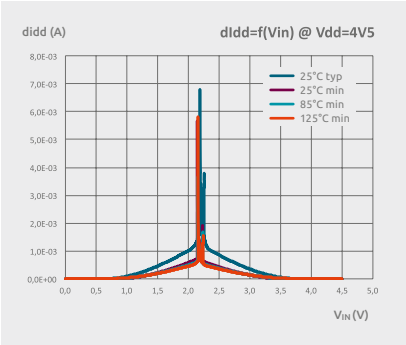
Input/output clamping current must be limited to 20 mA to prevent damage to the ESD protection circuits. Note that the input and output voltage ratings may be exceeded if the input and output current ratings are observed

All inputs have Schmitt Trigger Action except for 10 devices which have True Schmitt Triggers (74AHC/AHCT132, -14, -1G14, -1G17, -3G14). Schmitt Trigger Action input provide improved tolerance to input noise but do not have the long rise/fall times of True Schmitt Triggers. Schmitt Trigger action is indicated in the datasheet by the presence of the Transfer Characteristics Vt+, Vt- and Vh.

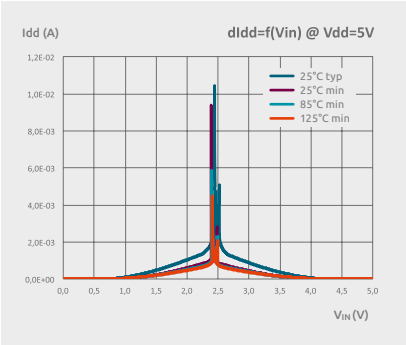
It is recommended to drive all logic inputs with a defined value, not to leave them floating.

AHC/AHCT input and output characteristics

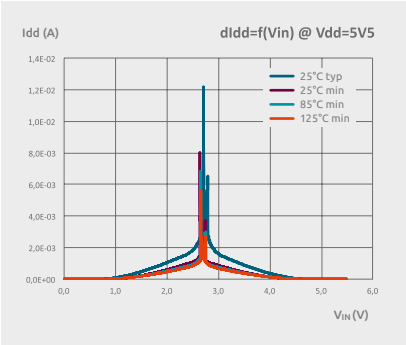
AHC Input figures



AHC input curves at 4V5

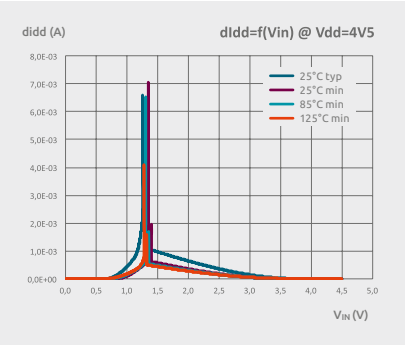


AHC input curves at 5V

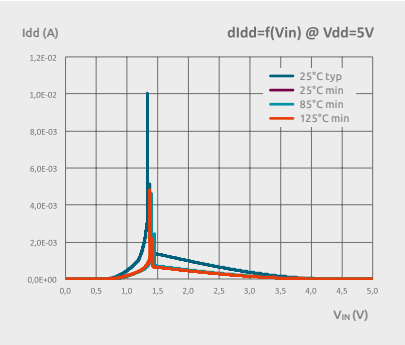


AHC input curves at 5V5

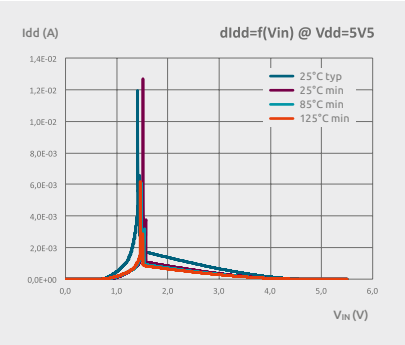
AHCT Input figures



AHCT input curves at 4V5

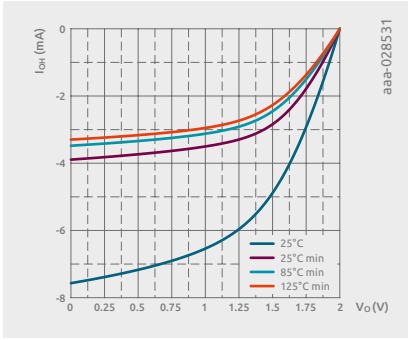


AHCT input curves at 5V

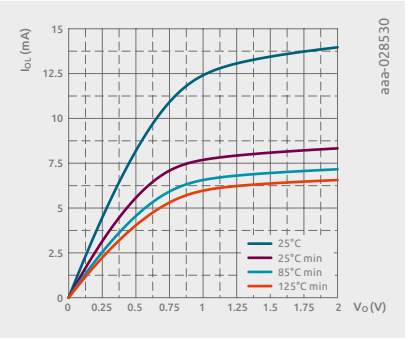


AHCT input curves at 5V5

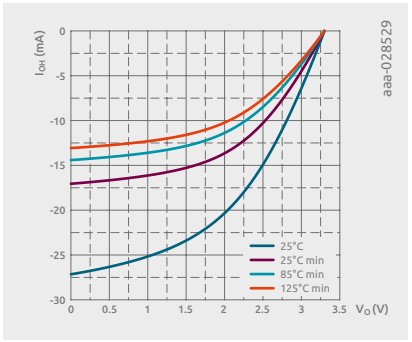
Outputs



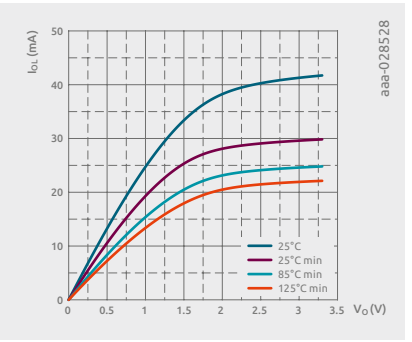
I_{OH} at 2.0 V



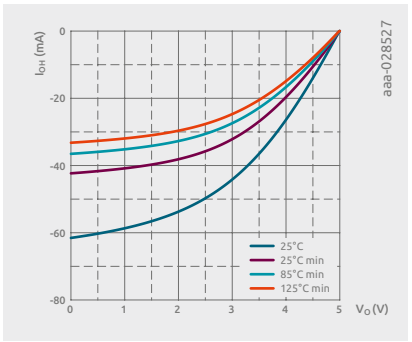
I_{OL} at 2.0 V



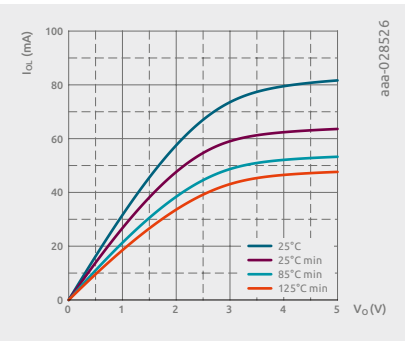
I_{OH} at 3.3 V



I_{OL} at 3.3 V



I_{OH} at 5.0 V



I_{OL} at 5.0 V

Operating Conditions

Table 7: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0,5	+7,0	V
V_I	input voltage		−0,5	+7,0	V
I_{IK}	input clamping current	$V_I < -0.5$ V *	−20	–	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V *	−20	+20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	−25	+25	mA
I_{CC}	supply current		–	+75	mA
I_{GND}	ground current		−75	–	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C **	–	500	mW

* The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

** For SOT108-1 (SO14) package: Ptot derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: Ptot derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: Ptot derates linearly with 9.6 mW/K above 98 °C.

Table 8: Recommended operating conditions

Symbol	Parameter	Conditions	74AHC74			74AHCT74			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2,0	5,0	5,5	4,5	5,0	5,5	V
V_I	input voltage		0	–	5,5	0	–	5,5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.0 to 3.6 V	–	–	100	–	–	–	ns/V
		V_{CC} = 4.5 to 5.5 V	–	–	20	–	–	20	ns/V

Table 9: Static characteristics

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC74										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1,5	–	–	1,5	–	1,5	–	V
		$V_{CC} = 3.0$ V	2,1	–	–	2,1	–	2,1	–	V
		$V_{CC} = 5.5$ V	3,85	–	–	3,85	–	3,85	–	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	–	–	0,5	–	0,5	–	0,5	V
		$V_{CC} = 3.0$ V	–	–	0,9	–	0,9	–	0,9	V
		$V_{CC} = 5.5$ V	–	–	1,65	–	1,65	–	1,65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = -50$ µA; $V_{CC} = 2.0$ V	1,9	2,0	–	1,9	–	1,9	–	V
		$I_O = -50$ µA; $V_{CC} = 3.0$ V	2,9	3,0	–	2,9	–	2,9	–	V
		$I_O = -50$ µA; $V_{CC} = 4.5$ V	4,4	4,5	–	4,4	–	4,4	–	V
		$I_O = -4.0$ mA; $V_{CC} = 3.0$ V	2,58	–	–	2,48	–	2,40	–	V
		$I_O = -8.0$ mA; $V_{CC} = 4.5$ V	3,94	–	–	3,80	–	3,70	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 50$ µA; $V_{CC} = 2.0$ V	–	0	0,1	–	0,1	–	0,1	V
		$I_O = 50$ µA; $V_{CC} = 3.0$ V	–	0	0,1	–	0,1	–	0,1	V
		$I_O = 50$ µA; $V_{CC} = 4.5$ V	–	0	0,1	–	0,1	–	0,1	V
		$I_O = 4.0$ mA; $V_{CC} = 3.0$ V	–	–	0,36	–	0,44	–	0,55	V
		$I_O = 8.0$ mA; $V_{CC} = 4.5$ V	–	–	0,36	–	0,44	–	0,55	V
I_I	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ to 5.5 V	–	–	0,1	–	1,0	–	2,0	µA

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	–	–	2,0	–	20	–	40	µA
C_I	input capacitance	$V_I = V_{CC}$ or GND	–	3	10	–	10	–	10	pF
74AHCT74										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ to 5.5 V	2,0	–	–	2,0	–	2,0	–	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ to 5.5 V	–	–	0,8	–	0,8	–	0,8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V								
		$I_O = -50$ µA	4,4	4,5	–	4,4	–	4,4	–	V
		$I_O = -8.0$ mA	3,94	–	–	3,80	–	3,70	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V								
		$I_O = 50$ µA	–	0	0,1	–	0,1	–	0,1	V
		$I_O = 8.0$ mA	–	–	0,36	–	0,44	–	0,55	V
I_I	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 0$ to 5.5 V	–	–	0,1	–	1,0	–	2,0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	–	–	2,0	–	20	–	40	µA
ΔI_{CC}	additional supply current	per input pin; $V_I = VCC - 2.1$ V; other pins at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ to 5.5 V	–	–	1,35	–	1,5	–	1,5	mA
C_I	input capacitance	$V_I = V_{CC}$ or GND	–	3	10	–	10	–	10	pF

Table 10: Dynamic characteristics

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	Min	Max	
74AHC74										
t_{pd}	propagation delay	nCP to nQ, nQ; [1]								
		$V_{CC} = 3.0$ to 3.6 V; $C_L = 15$ pF	–	5,2	11,9	1,0	14,0	1,0	15,0	ns
		$V_{CC} = 3.0$ to 3.6 V; $C_L = 50$ pF	–	7,4	15,4	1,0	17,5	1,0	19,5	ns
		$V_{CC} = 4.5$ to 5.5 V; $C_L = 15$ pF	–	3,7	7,3	1,0	8,5	1,0	9,5	ns
		$V_{CC} = 4.5$ to 5.5 V; $C_L = 50$ pF	–	5,2	9,3	1,0	10,5	1,0	12,0	ns
		nSD, nRD to nQ, nQ								
		$V_{CC} = 3.0$ to 3.6 V; $C_L = 15$ pF	–	5,4	12,3	1,0	14,5	1,0	15,5	ns
		$V_{CC} = 3.0$ to 3.6 V; $C_L = 50$ pF	–	7,7	15,8	1,0	18,0	1,0	20,0	ns
		$V_{CC} = 4.5$ to 5.5 V; $C_L = 15$ pF	–	3,7	7,7	1,0	9,0	1,0	10,0	ns
		$V_{CC} = 4.5$ to 5.5 V; $C_L = 50$ pF	–	5,3	9,7	1,0	11,0	1,0	12,5	ns
f_{max}	maximum frequency	$V_{CC} = 3.0$ to 3.6 V; $C_L = 15$ pF	80	125	–	70	–	70	–	MHz
		$V_{CC} = 3.0$ to 3.6 V; $C_L = 50$ pF	50	75	–	45	–	45	–	MHz
		$V_{CC} = 4.5$ to 5.5 V; $C_L = 15$ pF	130	170	–	110	–	110	–	MHz
		$V_{CC} = 4.5$ to 5.5 V; $C_L = 50$ pF	90	115	–	75	–	75	–	MHz
t_W	pulse width	CP HIGH or LOW; nSD, nRD LOW								
		$V_{CC} = 3.0$ to 3.6 V	6,0	–	–	7,0	–	7,0	–	ns
		$V_{CC} = 4.5$ to 5.5 V	5,0	–	–	5,0	–	5,0	–	ns

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	Min	Max	
t_{su}	set-up time	nD to nCP								
		V_{CC} = 3.0 to 3.6 V	6,0	–	–	7,0	–	7,0	–	ns
		V_{CC} = 4.5 to 5.5 V	5,0	–	–	5,0	–	5,0	–	ns
t_h	hold time	nD to nCP								
		V_{CC} = 3.0 to 3.6 V	0,5	–	–	0,5	–	0,5	–	ns
		V_{CC} = 4.5 to 5.5 V	0,5	–	–	0,5	–	0,5	–	ns
t_{rec}	recovery time	nRD to nCP								
		V_{CC} = 3.0 to 3.6 V	5,0	–	–	5,0	–	5,0	–	ns
		V_{CC} = 4.5 to 5.5 V	3,0	–	–	3,0	–	3,0	–	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [2]	–	12	–	–	–	–	–	pF
74AHCT74										
t_{pd}	propagation delay	nCP to nQ, nQ [1]								
		V_{CC} = 4.5 to 5.5 V; C_L = 15 pF	–	3,3	7,8	1,0	9,0	1,0	10,0	ns
		V_{CC} = 4.5 to 5.5 V; C_L = 50 pF	–	4,8	8,8	1,0	10,0	1,0	11,0	ns
		nSD, nRD to nQ, nQ								
		V_{CC} = 4.5 to 5.5 V; C_L = 15 pF	–	3,7	10,4	1,0	12,0	1,0	13,0	ns
		V_{CC} = 4.5 to 5.5 V; C_L = 50 pF	–	5,3	11,4	1,0	13,0	1,0	14,5	ns
f_{max}	maximum frequency	V_{CC} = 4.5 to 5.5 V; C_L = 15 pF	100	160	–	80	–	80	–	MHz
		V_{CC} = 4.5 to 5.5 V; C_L = 50 pF	80	140	–	65	–	65	–	MHz
t_W	pulse width	CP HIGH or LOW; nSD, nRD LOW								
		V_{CC} = 4.5 to 5.5 V	5,0	–	–	5,0	–	5,0	–	ns
t_{su}	set-up time	nD to nCP								
		V_{CC} = 4.5 to 5.5 V	5,0	–	–	5,0	–	5,0	–	ns

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	Min	Max	
t_h	hold time	nD to nCP								
		V_{CC} = 4.5 to 5.5 V	0	–	–	0	–	0	–	ns
t_{rec}	recovery time	nRD to nCP								
		V_{CC} = 4.5 to 5.5 V	3,5	–	–	3,5	–	3,5	–	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [2]	–	16	–	–	–	–	–	pF

* Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

Power calculations

Static Power Consumption can be calculated by the following:

Ps (Static Power) = I_{CC} (supply current) + Delta I_{CC} (per input where $V_{in} = V_{CC} - 2.1$ V) + Ii (input leakage current per input when V_{in} = 0 or 5 V) + Iout (sum of all output current)

Dynamic Power Consumption for the device can be calculated by the following equation:

$$P_D = C_{PD} \times {V_{CC}}^2 \times f_i \times N + \sum [C_L \times {V_{CC}}^2 \times f_o]$$

Where:
f_I = input frequency in MHz
f_O = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in V
N = number of inputs switching
$\sum [C_L \times V_{CC}^2 \times f_O]$ = sum of outputs

Special Features

An overview of features available for the AHC logic family:

- 8-bit bus interface functions
- MiniLogic gates
- Analog switch functions
- TTL level input/outputs (AHCT family)
- Schmitt trigger inputs
- Shift registers
- Clock dividers
- Open drain outputs
- Over voltage tolerant inputs

Summary

The advanced high-speed CMOS AHC(T) logic family is a speed upgrade of HC(T) with over-voltage tolerant inputs for true mixed voltage applications. Nexperia provides AHC products for use in 2.0 V to 6.0 V CMOS applications and AHCT products for use in 4.5 V to 5.5 V TTL applications.

- 5 ns typical propagation delay
- Output drive capability IOH/ IOL = ±8 mA
- Low power
- 5 V tolerant inputs
- Low noise: VOLP = 0.8 V (max.)

9.3 The LVC Logic Family

Introduction to family / General description

Nexperia offers the feature rich Low Voltage CMOS (LVC) logic portfolio to enable the migration of electronic solutions from 5.5 V to lower power mixed 5.5 V / 3.3 V and beyond. The LVC family includes Standard Logic functions with supply range 1.65 V to 3.3 V, as well as Mini Logic functions with supply range 1.65 V to 5.5 V. Compared to older logic families, it has a much lower I_{CC}. The power consumption is very low due to very small CPD which is lower than in competition devices. The LVC family offers features like overvoltage tolerant inputs and I_{OFF} circuitry as well as Schmitt-Trigger (action) inputs for many devices.

Applications

The LVC logic device family supports the trend to lower supply voltages. It can therefore be applied in applications like

- Computing, servers
- Telecom and networking equipment
- Advanced bus interface
- Industrial and Automotive

Construction

The LVC family devices are built in 5 V CMOS125 technology with a gate length of 600 nm. The process technology is Pb-free, RoHS and Dark Green compliant. Bond wiring is done with copper.

Input Output structures

Inputs

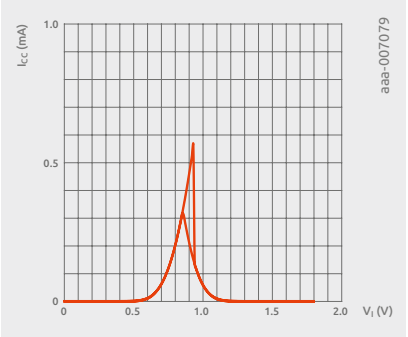
There are two types of input circuits in the LVC family.

Schmitt-trigger action input. This input has a small amount of hysteresis built into the input switching levels. The hysteresis is not formally specified but it does allow the input to be tolerant to input slew rates as high as 20 ns/V at V_{CC} = 1.65 V to 2.7 V and 10 ns/V at V_{CC} = 2.7 V to 5.5 V. The Schmitt-trigger action input may be preceded by a bus-hold cell to define unused inputs. This bus-hold cell does not affect the performance of the device.

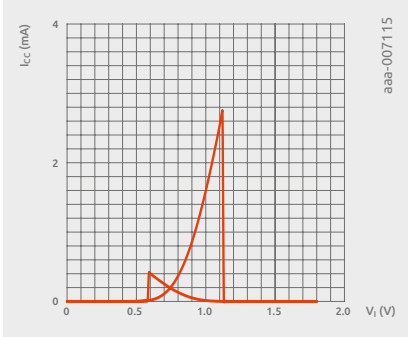
Schmitt-trigger input. This input has much higher input hysteresis which is formally specified in the datasheet. The advantage of true Schmitt-trigger inputs is that they are tolerant to very slow edges. The following figures show a side by side comparison of the IV characteristics of the Schmitt-trigger action input and the Schmitt-trigger input.

All inputs are 5 V tolerant.

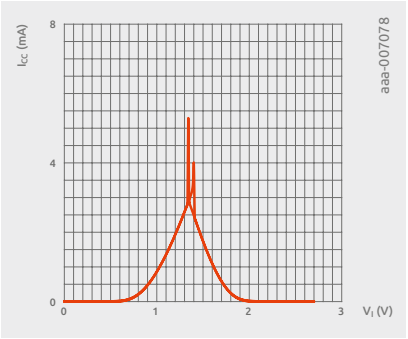
It is recommended to drive all logic inputs with a defined value, not to leave them floating.



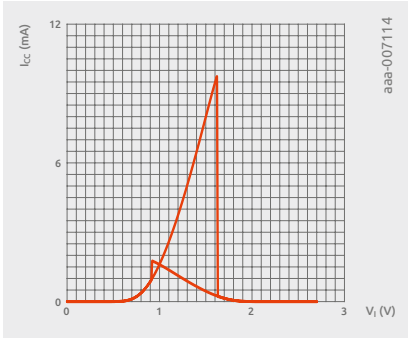
1.8 V Schmitt action



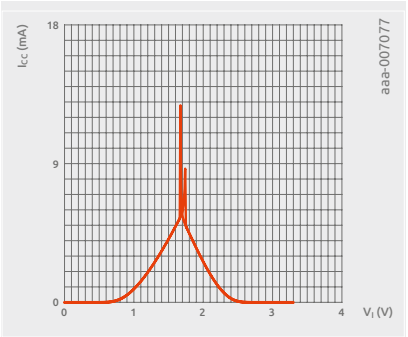
1.8 V Schmitt trigger



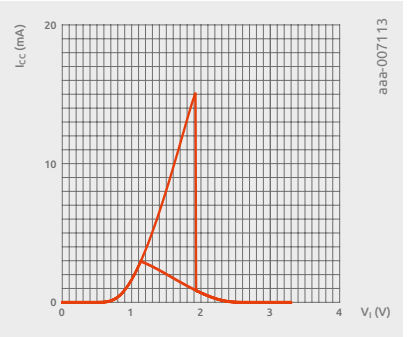
2.7 V Schmitt action



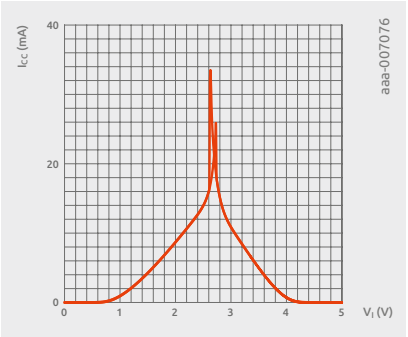
2.7 V Schmitt trigger



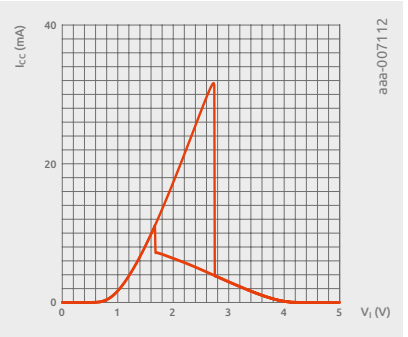
3.3 V Schmitt action



3.3 V Schmitt trigger



5.0 V Schmitt action



5.0 V Schmitt trigger

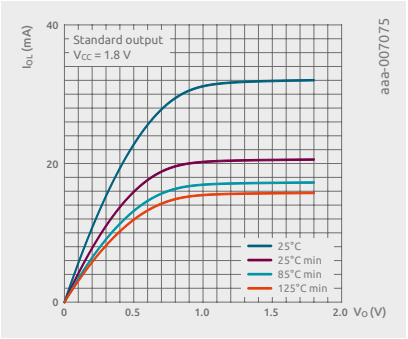
Outputs

Three types of output drivers are used in the LVC family.

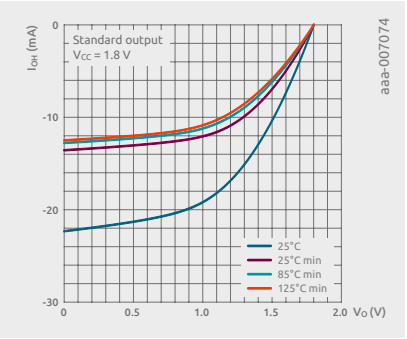
The standard output is used in the standard logic devices. It provides a balanced 24 mA output drive at 3.3 V.

The source terminated output is used in standard logic devices that feature source termination for better matching in distributed load applications such as transmission lines. It has a balanced 12 mA output drive at 3.3 V.

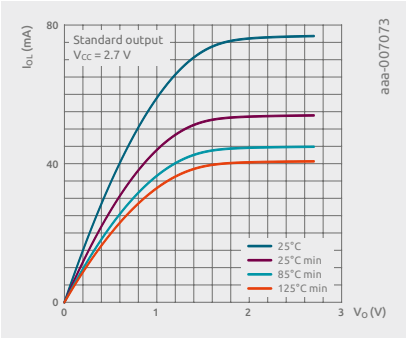
The Mini Logic output is suitable for use over a wider supply voltage range. It provides a balanced 24 mA output drive at 3.3 V and a balanced 32 mA output drive at 5.0 V. The following figures show a side by side comparison of the IV characteristics of all three outputs.



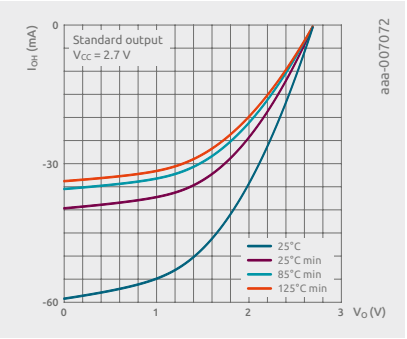
I_{OL} at 1.8 V



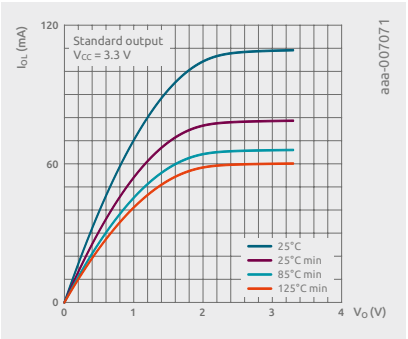
I_{OH} at 1.8 V



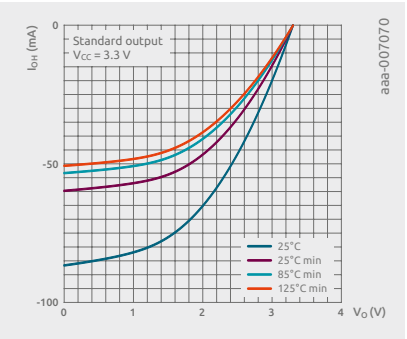
I_{OL} at 2.7 V



I_{OH} at 2.7 V



I_{OL} at 3.3 V



I_{OH} at 3.3 V

Operating Conditions

Table 11: Limiting values of the LVC family devices

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0,5	+6,5	V
I_{IK}	input clamping current	$V_I < 0\,V$	−50	–	mA
V_I	input voltage	*	−0,5	+6,5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0\,V$	–	±50	mA
V_O	output voltage	Active mode *	−0,5	V_{CC} + 0.5	V
		Power-down mode; $V_{CC} = 0\,V$ *	−0,5	+6,5	V
I_O	output current	$V_O = 0\,V$ to V_{CC}	–	±50	mA
I_{CC}	supply current		–	100	mA
I_{GND}	ground current		−100	–	mA
P_{tot}	total power dissipation	$T_{amb} = -40\,°C$ to $+125\,°C$ **	–	300	mW
T_{stg}	storage temperature		−65	+150	°C

* The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

** For TSSOP8 packages: above 55 °C the value of Ptot derates linearly with 2.5 mW/K.
For VSSOP8 packages: above 110 °C the value of Ptot derates linearly with 8.0 mW/K.
For XSON8 and XQFN8 packages: above 118 °C the value of Ptot derates linearly with 7.8 mW/K.

Recommended operating conditions

Table 12: Recommended operating conditions for the mini LVC logic devices (≤10 pins)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1,65	5,5	V
V_I	input voltage		0	5,5	V
V_O	output voltage	Active mode	0	VCC	V
		Power-down mode; $V_{CC} = 0\,V$	0	5,5	V
T_{amb}	ambient temperature		−40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ to $2.7\,V$	–	20	ns/V
		$V_{CC} = 2.7$ to $5.5\,V$	–	10	ns/V

Table 13: Recommended operating conditions for the standard LVC logic devices (>10 pins)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	1,65	–	3,6	V
		for low-voltage applications	1,2	–	3,6	V
V_I	input voltage		0	–	5,5	V
V_O	output voltage		0	–	V_{CC}	V
T_{amb}	ambient temperature		−40	–	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	–	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	–	10	ns/V

Static characteristics

Table 14: Static characteristics for mini Logic devices (≤10 pins)

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 to 1.95 V	0.65 V_{CC}	–	–	0.65 V_{CC}	–	V
		V_{CC} = 2.3 to 2.7 V	1,7	–	–	1,7	–	V
		V_{CC} = 2.7 to 3.6 V	2,0	–	–	2,0	–	V
		V_{CC} = 4.5 to 5.5 V	0.7 V_{CC}	–	–	0.7 V_{CC}	–	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 to 1.95 V	–	–	0.35 V_{CC}	–	0.35 V_{CC}	V
		V_{CC} = 2.3 to 2.7 V	–	–	0,7	–	0,7	V
		V_{CC} = 2.7 to 3.6 V	–	–	0,8	–	0,8	V
		V_{CC} = 4.5 to 5.5 V	–	–	0.3 V_{CC}	–	0.3 V_{CC}	V

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = −100 µA; V_{CC} = 1.65 to 5.5 V	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	V
		I_O = −4 mA; V_{CC} = 1.65 V	1,2	1,54	–	0,95	–	V
		I_O = −8 mA; V_{CC} = 2.3 V	1,9	2,15	–	1,7	–	V
		I_O = −12 mA; V_{CC} = 2.7 V	2,2	2,50	–	1,9	–	V
		I_O = −24 mA; V_{CC} = 3.0 V	2,3	2,62	–	2,0	–	V
		I_O = −32 mA; V_{CC} = 4.5 V	3,8	4,11	–	3,4	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 to 5.5 V	–	–	0,10	–	0,10	V
		I_O = 4 mA; V_{CC} = 1.65 V	–	0,07	0,45	–	0,70	V
		I_O = 8 mA; V_{CC} = 2.3 V	–	0,12	0,30	–	0,45	V
		I_O = 12 mA; V_{CC} = 2.7 V	–	0,17	0,40	–	0,60	V
		I_O = 24 mA; V_{CC} = 3.0 V	–	0,33	0,55	–	0,80	V
		I_O = 32 mA; V_{CC} = 4.5 V	–	0,39	0,55	–	0,80	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 to 5.5 V	–	±0.1	±1	–	±1	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	–	±0.1	±2	–	±2	µA

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 to 5.5 V; I_O = 0 A	–	0,1	4	–	4	µA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6$ V; I_O = 0 A; V_{CC} = 2.3 to 5.5 V	–	5	500	–	500	µA
C_I	input capacitance		–	4,0	–	–	–	pF

* All typical values are measured at T_{amb} = 25 °C.

Table 15: Static characteristics for standard Logic devices (> 10 pins)

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1,08	–	–	1,08	–	V
		V_{CC} = 1.65 to 1.95 V	0.65 × V_{CC}	–	–	0.65 × V_{CC}	–	V
		V_{CC} = 2.3 to 2.7 V	1,7	–	–	1,7	–	V
		V_{CC} = 2.7 to 3.6 V	2,0	–	–	2,0	–	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	–	–	0,12	–	0,12	
		V_{CC} = 1.65 to 1.95 V	–	–	0.35 × V_{CC}	–	0.35 × V_{CC}	
		V_{CC} = 2.3 to 2.7 V	–	–	0,7	–	0,7	
		V_{CC} = 2.7 to 3.6 V	–	–	0,8	–	0,8	

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = −100 µA; V_{CC} = 1.65 to 3.6 V	V_{CC} − 0.2	–	–	V_{CC} − 0.3	–	V
		I_O = −4 mA; V_{CC} = 1.65 V	1,2	–	–	1,05	–	V
		I_O = −8 mA; V_{CC} = 2.3 V	1,8	–	–	1,65	–	V
		I_O = −12 mA; V_{CC} = 2.7 V	2,2	–	–	2,05	–	V
		I_O = −18 mA; V_{CC} = 3.0 V	2,4	–	–	2,25	–	V
		I_O = −24 mA; V_{CC} = 3.0 V	2,2	–	–	2,0	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 to 3.6 V	–	–	0,2	–	0,3	V
		I_O = 4 mA; V_{CC} = 1.65 V	–	–	0,45	–	0,65	V
		I_O = 8 mA; V_{CC} = 2.3 V	–	–	0,6	–	0,8	V
		I_O = 12 mA; V_{CC} = 2.7 V	–	–	0,4	–	0,6	V
		I_O = 24 mA; V_{CC} = 3.0 V	–	–	0,55	–	0,8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	–	±0.1	±5	–	±20	µA
I_{CC}	supply current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	–	0,1	10	–	40	µA

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 2.7 to 3.6 V; $V_I = V_{CC} - 0.6$ V; I_O = 0 A	–	5	500	–	5000	µA
C_I	input capacitance	V_{CC} = 0 to 3.6 V; V_I = GND to V_{CC}	–	4	–	–	–	pF

Dynamic characteristics

Table 16: Dynamic characteristics for mini logic

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
t_{pd}	propagation delay	CP to Q, Q; [1]						
		V_{CC} = 1.65 to 1.95 V	1,5	6,0	13,4	1,5	13,4	ns
		V_{CC} = 2.3 to 2.7 V	1,0	3,5	7,1	1,0	7,1	ns
		V_{CC} = 2.7 V	1,0	3,5	7,1	1,0	7,1	ns
		V_{CC} = 3.0 to 3.6 V	1,0	3,5	5,9	1,0	5,9	ns
		V_{CC} = 4.5 to 5.5 V	1,0	2,5	4,1	1,0	4,1	ns
		SD to Q, Q; [1]						
		V_{CC} = 1.65 to 1.95 V	1,5	6,0	12,9	1,5	12,9	ns
		V_{CC} = 2.3 to 2.7 V	1,0	3,5	7,0	1,0	7,0	ns
		V_{CC} = 2.7 V	1,0	3,5	7,0	1,0	7,0	ns
		V_{CC} = 3.0 to 3.6 V	1,0	3,0	5,9	1,0	5,9	ns
		V_{CC} = 4.5 to 5.5 V	1,0	2,5	4,1	1,0	4,1	ns

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
t_{pd}	propagation delay	RD to Q, Q; [1]						
		V_{CC} = 1.65 to 1.95 V	1,5	5,0	12,9	1,5	12,9	ns
		V_{CC} = 2.3 to 2.7 V	1,0	3,5	7,0	1,0	7,0	ns
		V_{CC} = 2.7 V	1,0	3,5	7,0	1,0	7,0	ns
		V_{CC} = 3.0 to 3.6 V	1,0	3,0	5,9	1,0	5,9	ns
		V_{CC} = 4.5 to 5.5 V	1,0	2,5	4,1	1,0	4,1	ns
t_W	pulse width	CP HIGH or LOW						
		V_{CC} = 1.65 to 1.95 V	6,2	–	–	6,2	–	ns
		V_{CC} = 2.3 to 2.7 V	2,7	–	–	2,7	–	ns
		V_{CC} = 2.7 V	2,7	–	–	2,7	–	ns
		V_{CC} = 3.0 to 3.6 V	2,7	1,3	–	2,7	–	ns
		V_{CC} = 4.5 to 5.5 V	2,0	–	–	2,0	–	ns
		SD and RD LOW						
		V_{CC} = 1.65 to 1.95 V	6,2	–	–	6,2	–	ns
		V_{CC} = 2.3 to 2.7 V	2,7	–	–	2,7	–	ns
		V_{CC} = 2.7 V	2,7	–	–	2,7	–	ns
		V_{CC} = 3.0 to 3.6 V	2,7	1,6	–	2,7	–	ns
		V_{CC} = 4.5 to 5.5 V	2,0	–	–	2,0	–	ns
t_{rec}	recovery time	SD or RD						
		V_{CC} = 1.65 to 1.95 V	1,9	–	–	1,9	–	ns
		V_{CC} = 2.3 to 2.7 V	1,4	–	–	1,4	–	ns
		V_{CC} = 2.7 V	1,3	–	–	1,3	–	ns
		V_{CC} = 3.0 to 3.6 V	+1,2	−3,0	–	+1,2	–	ns
		V_{CC} = 4.5 to 5.5 V	1,0	–	–	1,0	–	ns

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
t_{su}	set-up time	D to CP						
		V_{CC} = 1.65 to 1.95 V	2,9	–	–	2,9	–	ns
		V_{CC} = 2.3 to 2.7 V	1,7	–	–	1,7	–	ns
		V_{CC} = 2.7 V	1,7	–	–	1,7	–	ns
		V_{CC} = 3.0 to 3.6 V	1,3	0,5	–	1,3	–	ns
		V_{CC} = 4.5 to 5.5 V	1,1	–	–	1,1	–	ns
t_h	hold time	D to CP						
		V_{CC} = 1.65 to 1.95 V	1,5	–	–	1,5	–	ns
		V_{CC} = 2.3 to 2.7 V	1,0	–	–	1,0	–	ns
		V_{CC} = 2.7 V	1,0	–	–	1,0	–	ns
		V_{CC} = 3.0 to 3.6 V	1,0	0,6	–	1,0	–	ns
		V_{CC} = 4.5 to 5.5 V	1,0	–	–	1,0	–	ns
f_{max}	maximum frequency	CP						
		V_{CC} = 1.65 to 1.95 V	80	–	–	80	–	MHz
		V_{CC} = 2.3 to 2.7 V	175	–	–	175	–	MHz
		V_{CC} = 2.7 V	175	–	–	175	–	MHz
		V_{CC} = 3.0 to 3.6 V	175	280	–	175	–	MHz
		V_{CC} = 4.5 to 5.5 V	200	–	–	200	–	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3 V [2]	–	15	–	–	–	pF

* Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

Table 17: Dynamic characteristics for standard logic

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
t_{pd}	propagation delay	nCP to nQ, nQ [1]						
		V_{CC} = 1.2 V	–	15	–	–	–	ns
		V_{CC} = 1.65 to 1.95 V	1,0	5,0	10,3	1,0	11,9	ns
		V_{CC} = 2.3 to 2.7 V	1,8	2,9	5,8	1,8	6,7	ns
		V_{CC} = 2.7 V	1,0	2,7	6,0	1,0	7,5	ns
		V_{CC} = 3.0 to 3.6 V	1,0	2,6	5,2	1,0	6,5	ns
		nSD to nQ, nQ						
		V_{CC} = 1.2 V	–	15	–	–	–	ns
		V_{CC} = 1.65 to 1.95 V	0,5	4,0	10,6	0,5	12,2	ns
		V_{CC} = 2.3 to 2.7 V	1,0	2,4	6,1	1,0	7,1	ns
		V_{CC} = 2.7 V	1,0	2,9	6,4	1,0	8,0	ns
		V_{CC} = 3.0 to 3.6 V	1,0	2,2	5,4	1,0	7,0	ns
		nRD to nQ, nQ						
		V_{CC} = 1.2 V	–	15	–	–	–	ns
		V_{CC} = 1.65 to 1.95 V	0,5	4,1	10,7	0,5	12,4	ns
		V_{CC} = 2.3 to 2.7 V	1,0	2,4	6,1	1,0	7,1	ns
		V_{CC} = 2.7 V	1,0	3,0	6,4	1,0	8,0	ns
		V_{CC} = 3.0 to 3.6 V	1,0	2,2	5,4	1,0	7,0	ns
t_W	pulse width	clock HIGH or LOW						
		V_{CC} = 1.65 to 1.95 V	5,0	–	–	5,0	–	ns
		V_{CC} = 2.3 to 2.7 V	4,0	–	–	4,0	–	ns
		V_{CC} = 2.7 V	3,3	–	–	4,5	–	ns
		V_{CC} = 3.0 to 3.6 V	3,3	1,3	–	4,5	–	ns
		set or reset LOW						
		V_{CC} = 1.65 to 1.95 V	5,0	–	–	5,0	–	ns
		V_{CC} = 2.3 to 2.7 V	4,0	–	–	4,0	–	ns
		V_{CC} = 2.7 V	3,3	–	–	4,5	–	ns
		V_{CC} = 3.0 to 3.6 V	3,3	1,7	–	4,5	–	ns

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	
t_{rec}	recovery time	set or reset						
		V_{CC} = 1.65 to 1.95 V	1,5	–	–	1,5	–	ns
		V_{CC} = 2.3 to 2.7 V	1,5	–	–	1,5	–	ns
		V_{CC} = 2.7 V	1,5	–	–	1,0	–	ns
		V_{CC} = 3.0 to 3.6 V	+1,0	-3,0	–	1,0	–	ns
t_{su}	set-up time	nD to nCP						
		V_{CC} = 1.65 to 1.95 V	3,0	–	–	3,0	–	ns
		V_{CC} = 2.3 to 2.7 V	2,5	–	–	2,5	–	ns
		V_{CC} = 2.7 V	2,2	–	–	2,2	–	ns
		V_{CC} = 3.0 to 3.6 V	2,0	0,8	–	2,0	–	ns
t_h	hold time	nD to nCP						
		V_{CC} = 1.65 to 1.95 V	2,0	–	–	2,0	–	ns
		V_{CC} = 2.3 to 2.7 V	1,5	–	–	1,5	–	ns
		V_{CC} = 2.7 V	1,0	–	–	1,0	–	ns
		V_{CC} = 3.0 to 3.6 V	+1,0	-0,2	–	1,0	–	ns
f_{max}	maximum frequency	nCP						
		V_{CC} = 1.65 to 1.95 V	100	–	–	80	–	MHz
		V_{CC} = 2.3 to 2.7 V	125	–	–	100	–	MHz
		V_{CC} = 2.7 V	150	–	–	120	–	MHz
		V_{CC} = 3.0 to 3.6 V	150	250	–	120	–	MHz
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 to 3.6 V [2]	–	–	1,0	–	1,5	ns
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to V_{CC} [3]						
		V_{CC} = 1.65 to 1.95 V	–	12,4	–	–	–	pF
		V_{CC} = 2.3 to 2.7 V	–	16,0	–	–	–	pF
		V_{CC} = 3.0 to 3.6 V	–	19,1	–	–	–	pF

* Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

Power calculations

The static power consumption calculation is much dependent on the input voltage level: if it is properly set to either V_{CC} or GND level, we can use the static supply current I_{CC} for calculating the power consumption: $P_{static} = V_{CC} \times I_{CC}$

In case Vin is at some intermediate level and the device is operating in undefined state, both NMOS and PMOS transistors of the input stage may be conducting and then we need to use the

The dynamic power consumption calculation is:

$$P_{dyn} = C_{PD} \times {V_{CC}}^2 \times f_i \times N + \sum [C_L \times {V_{CC}}^2 \times f_o]$$

Where:

f_I = input frequency in MHz
f_O = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = number of inputs switching
$\sum(C_L \times V_{CC}^2 \times f_O)$ = sum of inputs

An additional current through the devices can be caused by driving the devices with a voltage nearby $V_{CC}/2$ causing both NMOS and PMOS transistor of the input stage to be conducting, although not fully conducting. The ΔI_{CC} values are listed in the static characteristics.

These characteristics are generally valid for devices of the LVC family, please look at the respective data sheet for more specific details of Power calculations.

Special Features

To reduce standby current, many applications use advanced power management that powers down unused circuits within the application. To support this partial power down architecture a logic family must not have any leakage paths to the supply rails when the supply voltage (V_{CC}) is 0 V. LVC includes I_{OFF} circuitry that prevents current paths through inputs and outputs when $V_{CC} = 0$ V.

A couple of 16/32 bit Buffers/line drivers (LVCH) have Bus hold functionality for the inputs, holding the last input stage when inputs are temporarily disconnected.

An overview of features available for the AUP logic family:

- Bus hold inputs
- Schmitt-Trigger/Schmitt Action inputs
- Over voltage tolerant inputs
- Open drain outputs
- Source termination
- Dual supply translations

Summary

Nexperia offers the feature rich Low Voltage CMOS (LVC) logic portfolio to enable the migration of electronic solutions from 5.5 V to lower power mixed 5.5 V / 3.3 V and beyond. The LVC family includes Standard Logic functions with supply range 1.65 V to 3.3 V, as well as Mini Logic functions with supply range 1.65 V to 5.5 V. Some key features are:

- 4 ns typical propagation delay
- 24 mA balanced output drive
- Wide supply range
- 5 V tolerant I/O
- Series termination options
- Bus Hold options
- Over voltage tolerant inputs
- I_{OFF} circuitry
- AEC-Q100 compliant options
- Fully specified (-40 to +125°C)
- Pb-free, RoHS compliant and Dark Green

9.4 The AVC Logic Family

Introduction to family / General description

Nexperia's AVC (Advanced Very low voltage CMOS) logic family is optimized for high performance bus interface applications. Operating with sub 2 ns propagation delays, AVC meets the demands of new digital systems that require low power consumption, very high bus speeds in excess of 100 MHz, and low noise. AVC is targeted for new high performance workstations, PCs, telecommunications equipment, and data communications equipment.

New circuit techniques have been pioneered that give AVC unique properties. Optimized for 2.5 V systems, AVC also operates at 3.3 V and 1.8 V to support mixed voltage systems. AVC also features a power-off disable output circuit that isolates the outputs during power-down modes. This chapter will provide designers better insight into this new family for use in their applications.

Construction

The AVC family is built in 3.3 V CMOS technology with 0.35 µm gate length. The process technology is Pb-Free, RoHS and Dark Green compliant. Bond wiring is done with copper.

Input and output structure

Input Structures

AVC inputs use a CMOS totem pole inverter as shown in Figure 9.3. The circuit does not have the overshoot clamping diode from the input to V_{CC} that is used in classic CMOS circuits. Since there is no current path to V_{CC}, the voltage may be raised above the V_{CC} level and allows interfacing in 1.8 V to 3.3 V systems.

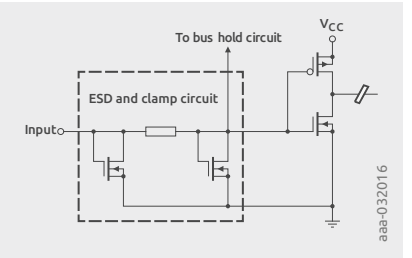


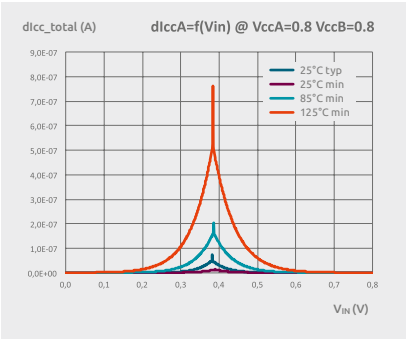
Figure 9.3 | Simplified AVC input structure

Since the circuit is CMOS, care must still be taken to ensure that the inputs don't float. When inputs float, the voltage level may reach the threshold level such that both transistors in the totem pole structure will conduct, causing a current path from V_{CC} and ground, wasting power.

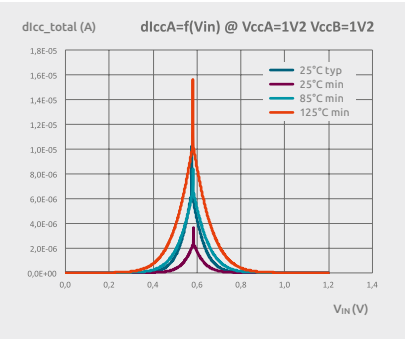
It is recommended to drive all logic inputs with a defined value, not to leave them floating.

Input and Output figures

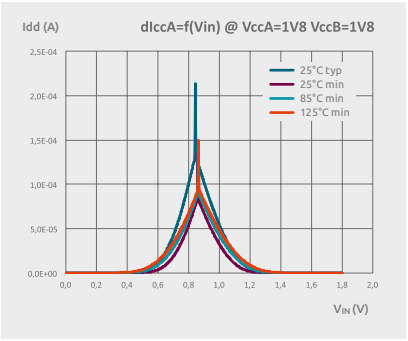
AVC Input Figures



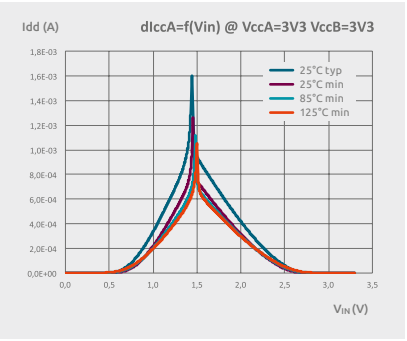
AVC input at 0.8V



AVC input at 1V2

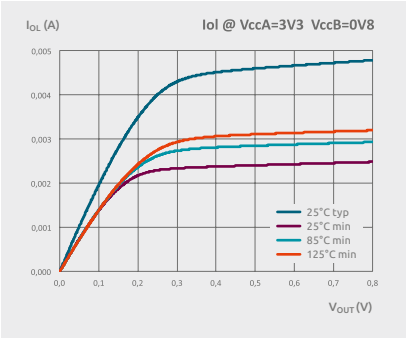


AVC input at 1V8

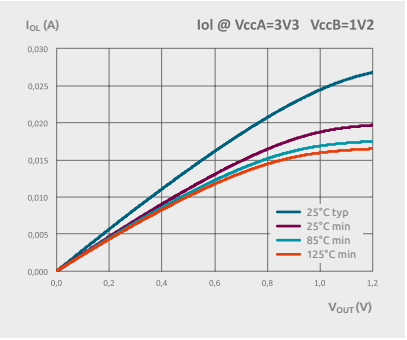


AVC input at 3V3

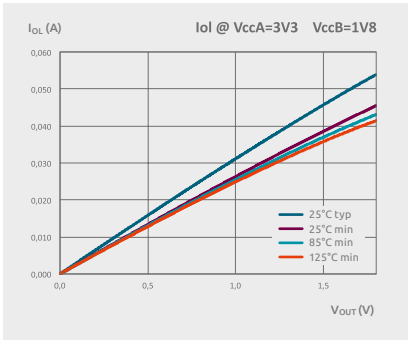
Output figures



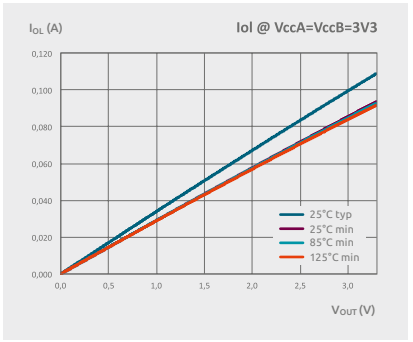
AVC output at 0.8V



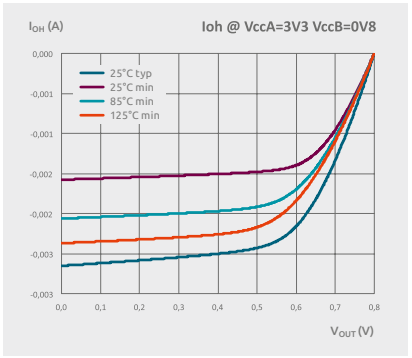
AVC output at 1V2



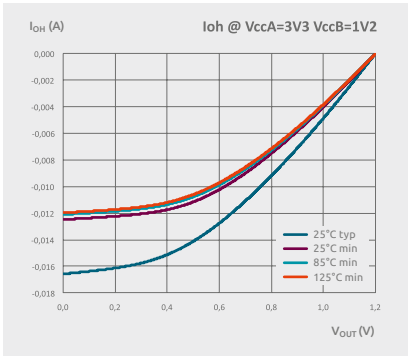
AVC output at 1V8



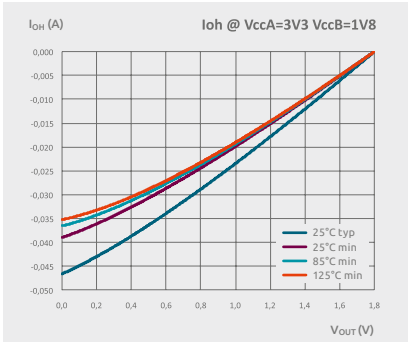
AVC output at 3V3



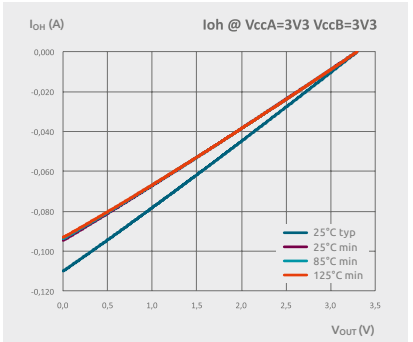
AVC output at 0V8



AVC output at 1V2



AVC output at 1V8



AVC output at 3V3

Operating Conditions

Table 18: Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+4,6	V
I_{IK}	input clamping current	$V_I < 0\,V$	–	−50	mA
V_I	input voltage	*	−0.5	+4,6	V
I_{OK}	output clamping current	$V_O < 0\,V$	−50	–	mA
V_O	output voltage	output HIGH or LOW *	−0.5	$V_{CC}+0.5$	V
		output 3-state *	−0.5	+4,6	V
I_O	output current	$V_O = 0\,V$ to V_{CC}	–	±50	mA
I_{CC}	supply current		–	+100	mA
I_{GND}	ground current		−100	–	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\,°C$ to $+85\,°C$ **	–	500	mW

* The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
** Above 60 °C, the value of P_{tot} derates linearly with 5.5 mW/K.

Table 19: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	according to JEDEC Low Voltage Standards	1,4	–	1,6	V
			1,65	–	1,95	V
			2,3	–	2,7	V
			3,0	–	3,6	V
		for low-voltage applications	1,2	–	3,6	V
V_I	input voltage		0	–	3,6	V
V_O	output voltage	output HIGH or LOW	0	–	V_{CC}	V
		output 3-state	0	–	3,6	V
T_{amb}	ambient temperature	in free air	−40	–	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.4$ to $1.6\,V$	0	–	40	ns/V
		$V_{CC} = 1.65$ to $2.3\,V$	0	–	30	ns/V
		$V_{CC} = 2.3$ to $3.0\,V$	0	–	20	ns/V
		$V_{CC} = 3.0$ to $3.6\,V$	0	–	10	ns/V

Table 20: Static characteristics

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			Unit
			Min	Typ*	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2\,V$	V_{CC}	–	–	V
		$V_{CC} = 1.4$ to $1.6\,V$	$0.65 \times V_{CC}$	0,9	–	V
		$V_{CC} = 1.65$ to $1.95\,V$	$0.65 \times V_{CC}$	0,9	–	V
		$V_{CC} = 2.3$ to $2.7\,V$	1,7	1,2	–	V
		$V_{CC} = 3.0$ to $3.6\,V$	2,0	1,5	–	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2\,V$	–	–	GND	V
		$V_{CC} = 1.4$ to $1.6\,V$	–	0,9	$0.35 \times V_{CC}$	V
		$V_{CC} = 1.65$ to $1.95\,V$	–	0,9	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ to $2.7\,V$	–	1,2	0,7	V
		$V_{CC} = 3.0$ to $3.6\,V$	–	1,5	0,8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100\,\mu A$; $V_{CC} = 1.65$ to $3.6\,V$	$V_{CC} - 0.20$	V_{CC}	–	V
		$I_O = -3\,mA$; $V_{CC} = 1.4\,V$	$V_{CC} - 0.35$	$V_{CC} - 0.23$	–	V
		$I_O = -4\,mA$; $V_{CC} = 1.65\,V$	$V_{CC} - 0.45$	$V_{CC} - 0.25$	–	V
		$I_O = -8\,mA$; $V_{CC} = 2.3\,V$	$V_{CC} - 0.55$	$V_{CC} - 0.38$	–	V
		$I_O = -12\,mA$; $V_{CC} = 3.0\,V$	$V_{CC} - 0.70$	$V_{CC} - 0.48$	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100\,\mu A$; $V_{CC} = 1.65$ to $3.6\,V$	–	GND	0,20	V
		$I_O = 3\,mA$; $V_{CC} = 1.4\,V$	–	0,10	0,35	V
		$I_O = 4\,mA$; $V_{CC} = 1.65\,V$	–	0,10	0,45	V
		$I_O = 8\,mA$; $V_{CC} = 2.3\,V$	–	0,26	0,55	V
		$I_O = 12\,mA$; $V_{CC} = 3.0\,V$	–	0,36	0,70	V
I_I	input leakage current	per pin; $V_I = V_{CC}$ or GND; $V_{CC} = 1.4$ to $3.6\,V$	–	0,1	2,5	µA
I_{OFF}	power-off leakage current	V_I or $V_O = 3.6\,V$; $V_{CC} = 0.0\,V$	–	±0.1	±10	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND				
		$V_{CC} = 1.4$ to $2.7\,V$	–	0,1	5	µA
		$V_{CC} = 3.0$ to $3.6\,V$	–	0,1	10	µA

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			Unit
			Min	Typ*	Max	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A				
		V_{CC} = 1.4 to 2.7 V	–	0,1	20	µA
		V_{CC} = 3.0 to 3.6 V	–	0,2	40	µA
C_I	input capacitance		–	5	–	pF

* All typical values are measured at T_{amb} = 25 °C.

Table 21: Dynamic characteristics

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			Unit
			Min	Typ*	Max	
t_{pd}	propagation delay	nCP to nQn; [1]				
		V_{CC} = 1.2 V	–	3,1	–	ns
		V_{CC} = 1.4 to 1.6 V	1,2	2,4	8,4	ns
		V_{CC} = 1.65 to 1.95 V	1,0	2,0	6,7	ns
		V_{CC} = 2.3 to 2.7 V	0,8	1,5	4,1	ns
		V_{CC} = 3.0 to 3.6 V	0,7	1,3	3,3	ns
t_{en}	enable time	$n\overline{OE}$ to nQn, nBn; [1]				
		V_{CC} = 1.2 V	–	5,4	–	ns
		V_{CC} = 1.4 to 1.6 V	1,6	3,9	8,5	ns
		V_{CC} = 1.65 to 1.95 V	2,3	3,3	6,7	ns
		V_{CC} = 2.3 to 2.7 V	0,9	2,3	4,3	ns
		V_{CC} = 3.0 to 3.6 V	0,7	2,0	3,4	ns
t_{dis}	disable time	$n\overline{OE}$ to nQn; [1]				
		V_{CC} = 1.2 V	–	5,6	–	ns
		V_{CC} = 1.4 to 1.6 V	2,5	4,5	9,4	ns
		V_{CC} = 1.65 to 1.95 V	1,8	3,3	7,8	ns
		V_{CC} = 2.3 to 2.7 V	1,0	1,8	4,2	ns
		V_{CC} = 3.0 to 3.6 V	1,2	2,0	3,9	ns

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			Unit
			Min	Typ*	Max	
t_W	pulse width	HIGH; nCP				
		V_{CC} = 1.2 V	–	0,8	–	ns
		V_{CC} = 1.4 to 1.6 V	–	0,5	–	ns
		V_{CC} = 1.65 to 1.95 V	3,1	0,3	–	ns
		V_{CC} = 2.3 to 2.7 V	2,5	0,2	–	ns
		V_{CC} = 3.0 to 3.6 V	2,5	0,2	–	ns
t_{su}	set-up time	nDn to nCP				
		V_{CC} = 1.2 V	–	−0.6	–	ns
		V_{CC} = 1.4 to 1.6 V	2,7	−0.3	–	ns
		V_{CC} = 1.65 to 1.95 V	1,9	−0.3	–	ns
		V_{CC} = 2.3 to 2.7 V	1,4	−0.2	–	ns
		V_{CC} = 3.0 to 3.6 V	1,4	−0.1	–	ns
t_h	hold time	nDn to nCP				
		V_{CC} = 1.2 V	–	0,8	–	ns
		V_{CC} = 1.4 to 1.6 V	1,3	0,7	–	ns
		V_{CC} = 1.65 to 1.95 V	1,2	0,6	–	ns
		V_{CC} = 2.3 to 2.7 V	1,1	0,5	–	ns
		V_{CC} = 3.0 to 3.6 V	1,1	0,4	–	ns
f_{max}	maximum frequency	V_{CC} = 1.2 V	–	250	–	MHz
		V_{CC} = 1.4 to 1.6 V	–	300	–	MHz
		V_{CC} = 1.65 to 1.95 V	160	320	–	MHz
		V_{CC} = 2.3 to 2.7 V	200	350	–	MHz
		V_{CC} = 3.0 to 3.6 V	200	350	–	MHz
C_{PD}	power dissipation capacitance	per input; V_I = GND to V_{CC} [2]				
		outputs enabled	–	66	–	pF
		outputs disabled	–	1	–	pF

* Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V respectively.
[1] t_{pd} is the same as t_{PLH} and t_{PHL}. t_{en} is the same as t_{PZL} and t_{PZH}. t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

Table 22: Propagation Delay

Parameter	Characteristic Values		
Supply Voltage	1.65–1.95 V	2.3–2.7 V	3.0–3.6 V
Input Voltage	3.6 V	3.6 V	3.6 V
Maximum Propagation Delay[1]	3.2 ns	1.9 ns	1.7 ns

1: 74AVC16245

Power calculations

AVC is constructed using a 0.35 micron CMOS fabrication process resulting in low current consumption. Figure 9.4 shows simulation data of I_{CC} at various frequencies for single and multiple output switching:

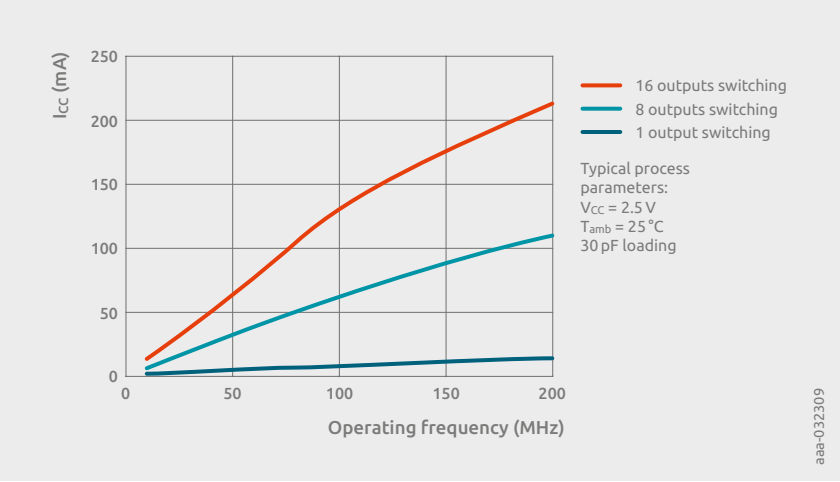


Figure 9.4 | I_{CC} over frequency

Dynamic power dissipation can be calculated by the following formula:

$$P_D = C_{PD} \times V_{CC}{}^2 \times f_{IN} + \sum (C_L \times V_{CC}{}^2 \times f_{OUT})$$

Where:

C_{PD} = power dissipation capacitance per buffer, latch, or flip-flop
f_{IN} = input frequency
f_{OUT} = output frequency
C_L = output load capacitance
$\sum (C_L \times V_{CC}{}^2 \times f_{OUT})$ = sum of outputs

For an example, with a typical C_{PD} of 20 pF for an AVC16244, 15 pF loading, 100 MHz operation, and 2.5 V V_{CC}, power dissipation is 162.5 mW with 16 outputs switching.

Special Features

Output Protection: I_{OFF}

Another feature of AVC is the output protection circuit. In mixed voltage systems, when the output node is tied to a bus from a higher voltage system, the original diode connection provides a current path to V_{CC} when the output node is 0.6 V higher than the AVC device's V_{CC}. This current can damage the diode, and a current path now exists between the two power supplies. Damage can also occur from the higher voltage supply charging the lower voltage supply.

To protect the diodes, the cathodes are switched rather than hard-wired to V_{CC}. A comparator senses the output node voltage and shorts out the diode when the voltage rises above the AVC device's V_{CC} by 0.6 V. This works in the 3-State mode only, and the current path to V_{CC} is eliminated, allowing the output to be raised above V_{CC} in a mixed voltage system. While the device is powered down, the diodes are disconnected, and only leakage current of 10uA maximum is present when a voltage is applied to the output. This current parameter is called I_{OFF}, and the protection feature is useful for power-down modes.

Bus Hold

Also, floating inputs can cause output oscillation, creating excessive current and heat which can damage the device. To keep inputs from floating, a common practice is to tie a pull-up resistor of several thousand ohms between the input and V_{CC}. Although effective, this adds board component count and extra power dissipation. Another solution is to use a device with an integrated bus hold cell. AVC devices have an option to integrate this bus hold feature on inputs. This is designated in the part type with an "H" by calling it 74AVCH. Figure 9.5 shows a bus hold cell:

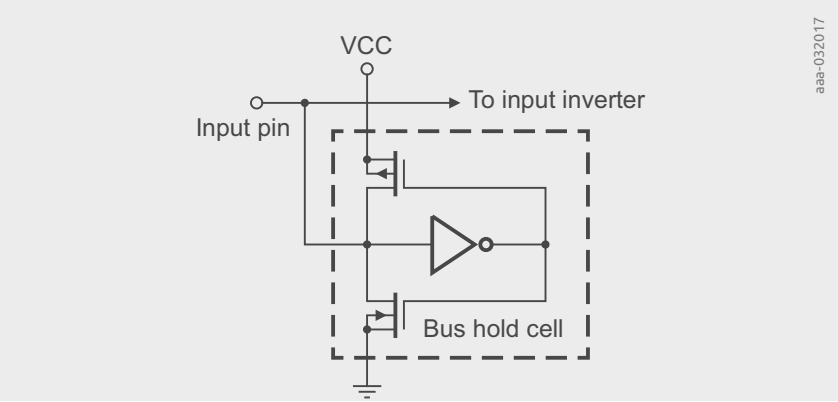


Figure 9.5 | Simplified bus holder cell

The cell consists of two inverters to keep the logic level the same at the input node. The inverters are comprised of small MOS transistors with weak drive capability in the order of several hundred microamps. When the input starts to float, the PMOS or NMOS structures pull the bus to the V_{CC} or ground rail of the last valid logic state. The cell requires a small amount of current, called IBHH or IBHL, to sustain the logic HIGH and LOW threshold levels. Also, the cell needs several hundred microamps, called IBHHO or IBHLO, to overdrive the cell and flip the logic level from 3-State to a HIGH or LOW. These specifications are shown in Table 23. Simulation data for the bus hold current characteristics are shown in Figure 9.6. The user must also take considerations when the bus hold cell is connected to existing external pull-up or pull-down resistors. When using external resistors, or when a connected ASIC has them built-in, the resistor value must be low enough to allow sufficient current to overpower the bus hold cell and drive the input past the threshold point to the HIGH or LOW state.

Table 23: Bus hold current specification

Symbol	Parameter	T_{amb}	Unit	Test Conditions	
		−40 to +85°C Min.		V_{CC} (V)	V_I (V)
I_{BHL}	Bus hold LOW sustaining current	25	μA	1.65	0.35 V_{CC}
		45	μA	2.3	0.7 V
		75	μA	3.0	0.8 V
I_{BHH}	Bus hold HIGH sustaining current	−25	μA	1.65	0.65 V_{CC}
		−45	μA	2.3	1.7 V
		−75	μA	3.0	2.0 V
I_{BHLO}	Bus hold LOW overdrive current	200	μA	1.95	
		300	μA	2.7	
		450	μA	3.6	
I_{BHHO}	Bus hold HIGH overdrive current	−200	μA	1.95	
		−300	μA	2.7	
		−450	μA	3.6	

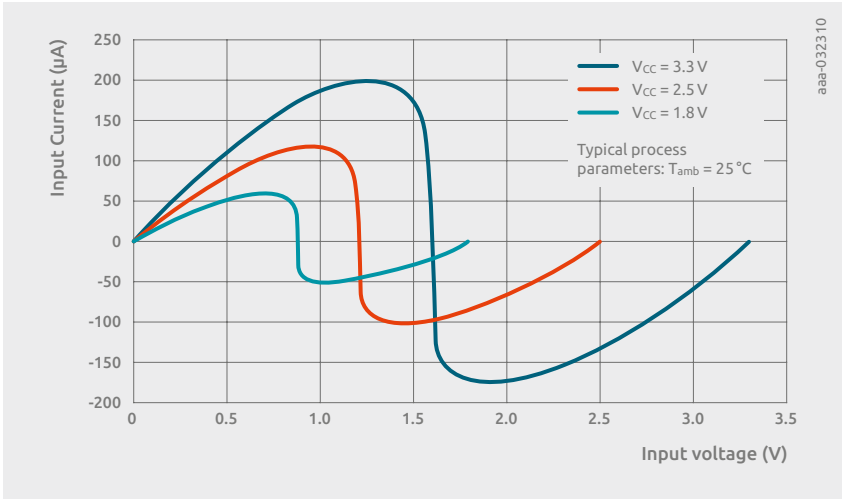


Figure 9.6 | Bus Hold current characteristics

Summary

The AVC family offers a solution for new designs needing the highest performance in 1.8 V, 2.5 V, and 3.3 V systems. AVC offers a line of bus interface functions for today's high performance, low voltage systems.

9.5 The AUP Logic Family

Introduction to family / General description

The AUP family of Si-gate CMOS devices uses advanced process technology and next generation packaging technology to create extremely small functions that consume very little power. The devices are available in single (1G), dual (2G) and triple (3G) gate formats.

Multiple standard, combination and configurable logic functions are available in the AUP family as well as low threshold input variants and dual supply voltage level translators.

Due to its advanced process technology AUP provides very low static and dynamic power dissipation.

Applications

The AUP logic devices are specifically designed for battery powered mobile applications with which are demanding low energy consumption for operation. Examples are:

- Cellular handsets and smart phones
- MP3 players and mobile video players
- DSCs and digital camcorders
- Portable handhelds (PDAs, GPS devices, notebook PCs)
- Consumer entertainment (LCD TVs, DVD+R/W systems, STBs)
- Portable instrumentation

The low propagation delay and the wide voltage range are making this family suitable for mixed voltage applications. 3.6 V tolerant inputs enable a device supplied at 1.8 V to interface between 3.3 V and 1.8 V systems. Options with low-threshold inputs (1T) can interface between 1.2 V and 3.3 V systems when supplied with 3.3 V. The portfolio also includes dual supply uni-directional and bi-directional voltage level translators. Schmitt trigger action at all inputs improves noise immunity and makes the circuit tolerant to slower input rise and fall times across the entire range of supply voltage.

Construction

The AUP family devices are built in CMOS035 technology with a gate length of 350 nm. The process technology is Pb-free, RoHS and Dark Green compliant. Bond wiring is done with copper.

Input Output structures

The AUP family devices are built with overvoltage tolerant input stages (3.6 V) and allows a supply range of 0.8 V to 3.6 V.

All configurable logic devices have Schmitt trigger inputs with ~400 mV Hysteresis @V_{CC} = 1.2 V. Some Buffer, Inverter and NAND gate types have Schmitt-trigger inputs as well. All other devices have Schmitt-trigger actions, which causes a smaller hysteresis of about 60 mV @V_{CC} = 1.2 V. The hysteresis leads to a higher noise immunity.

It is recommended to drive all logic inputs with a defined value, not to leave them floating.

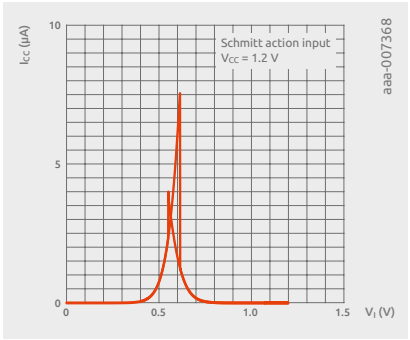
Input figures

There are two types of input circuits in the AUP family.

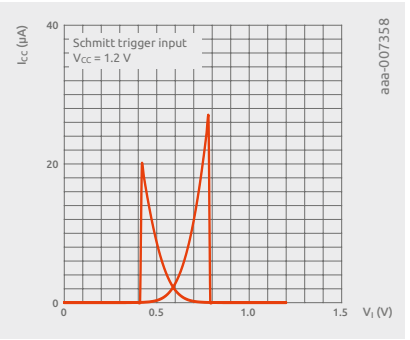
Schmitt-trigger action input — This input has a small amount of hysteresis built into the input switching levels. The hysteresis is not formally specified but it does allow the input to be tolerant to input slew rates as high as 20 ns/V at V_{CC} = 1.65 V to 2.7 V and 10 ns/V at V_{CC} = 2.7 V to 5.5 V. The Schmitt-trigger action input may be preceded by a bus-hold cell to define unused inputs. This bus-hold cell does not affect the performance of the device.

Schmitt-trigger input — This input has much higher input hysteresis which is formally specified in the datasheet. The advantage of true Schmitt-trigger inputs is that they are tolerant to very slow edges.

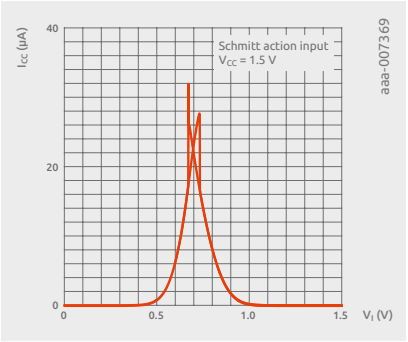
The following figures show a side by side comparison of the IV characteristics of the Schmitt-trigger action input and the Schmitt-trigger input.



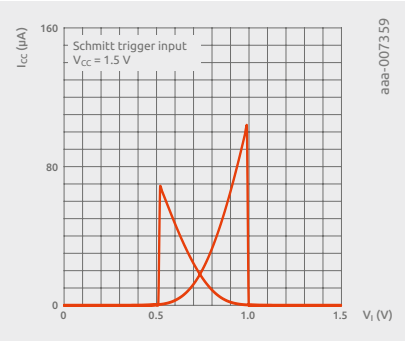
1.2 V Schmitt action



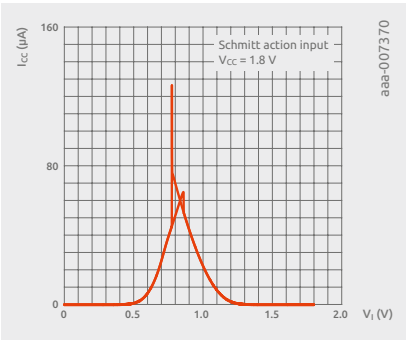
1.2 V Schmitt trigger



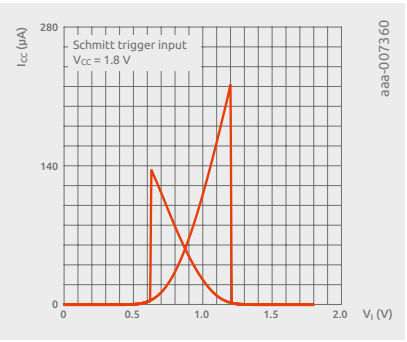
1.5 V Schmitt action



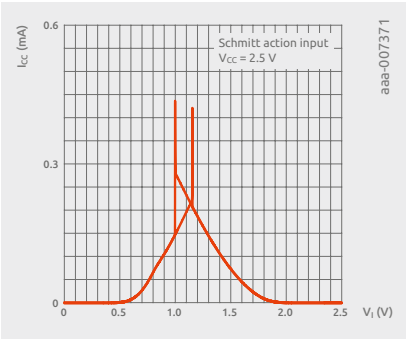
1.5 V Schmitt trigger



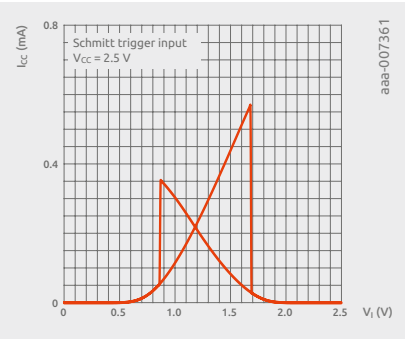
1.8 V Schmitt action



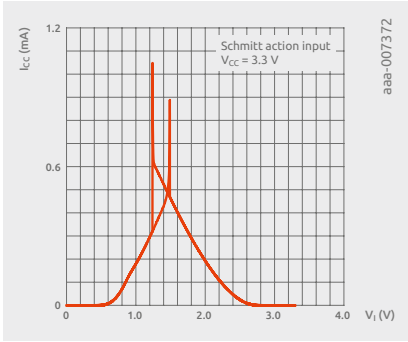
1.8 V Schmitt trigger



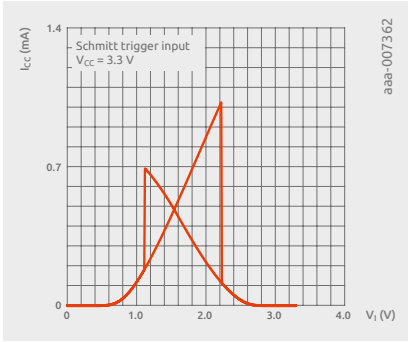
2.5 V Schmitt action



2.5 V Schmitt trigger



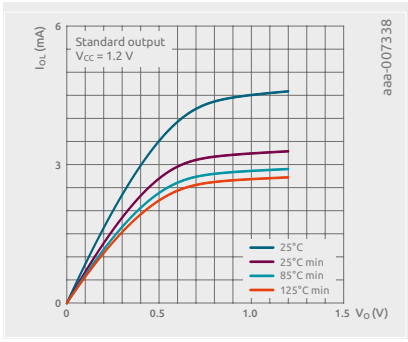
3.3 V Schmitt action



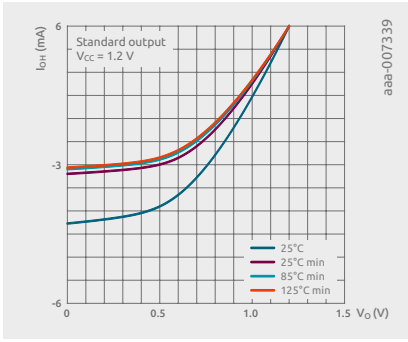
3.3 V Schmitt trigger

Output figures

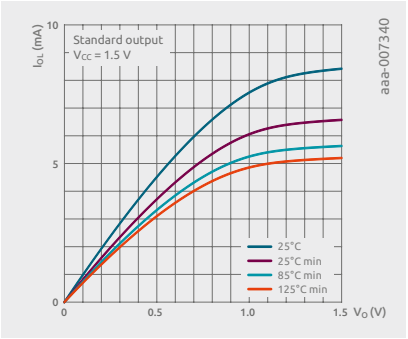
An AUP device provides a balanced 1.9 mA output drive at V_{CC} = 1.8 V. The following table of output figures shows the measured output characteristics of the AUP family devices for 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V.



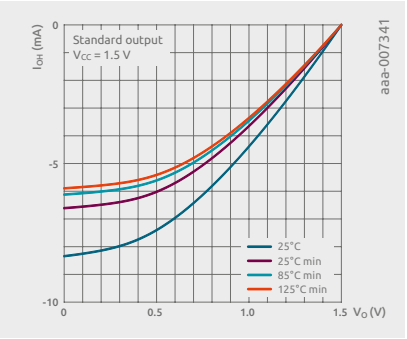
I_{OL} at 1.2 V



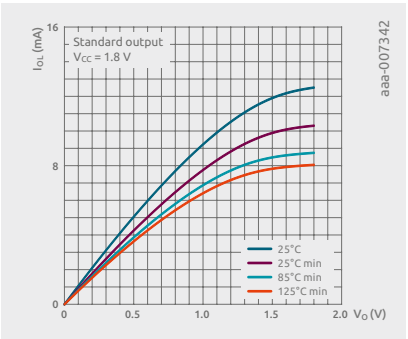
I_{OH} at 1.2 V



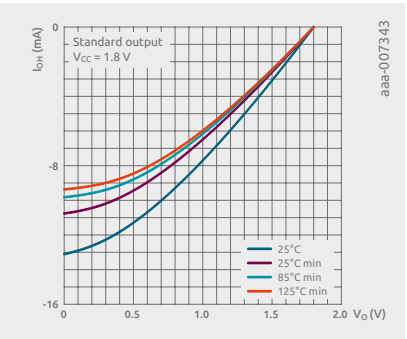
I_{OL} at 1.5 V



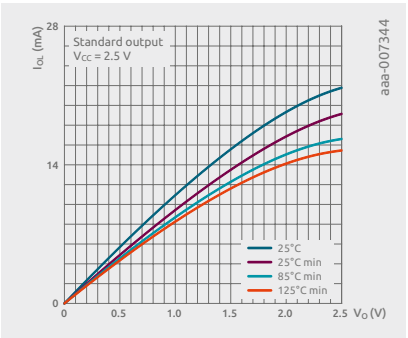
I_{OH} at 1.5 V



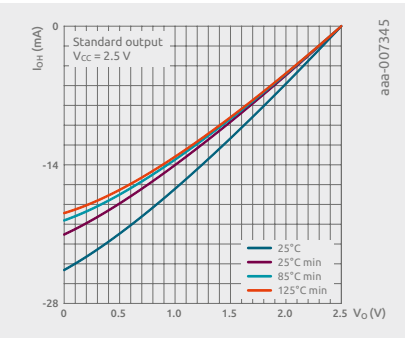
I_{OL} at 1.8 V



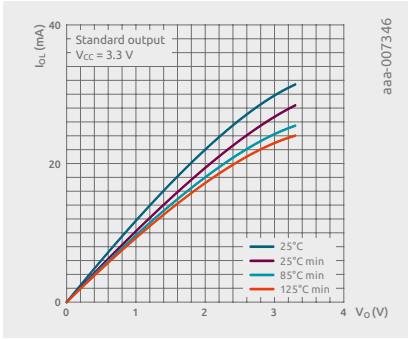
I_{OH} at 1.8 V



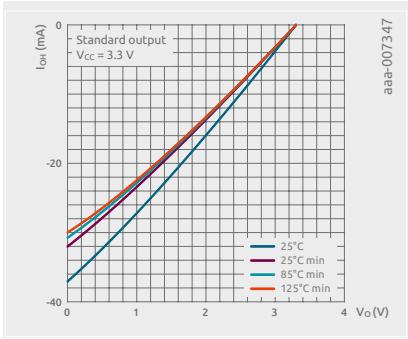
I_{OL} at 2.5 V



I_{OH} at 2.5 V



I_{OL} at 3.3 V



I_{OH} at 3.3 V

Operating Conditions

Table 24: Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0,5	+4,6	V
I_{IK}	input clamping current		−0,5	+4,6	V
V_I	input voltage	Active mode and Power-down mode	−0,5	+4,6	V
I_{OK}	output clamping current	$V_I < 0$ V	−50	–	mA
V_O	output voltage	$V_O < 0$ V	−50	–	mA
I_O	output current	$V_O = 0$ V to V_{CC}	–	±20	mA
I_{CC}	supply current		–	+50	mA
I_{GND}	ground current		−50	–	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	–	250	mW

Table 25: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0,8	3,6	V
V_I	input voltage		0	3,6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	3,6	V
T_{amb}	ambient temperature		−40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 0.8 to 3.6 V	–	200	ns/V

Table 26: Static characteristics

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	0.70 × V_{CC}	–	–	0.70 × V_{CC}	–	0.75 × V_{CC}	–	V
		V_{CC} = 0.9 to 1.95 V	0.65 × V_{CC}	–	–	0.65 × V_{CC}	–	0.70 × V_{CC}	–	V
		V_{CC} = 2.3 to 2.7 V	1,6	–	–	1,6	–	1,6	–	V
		V_{CC} = 3.0 to 3.6 V	2,0	–	–	2,0	–	2,0	–	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	–	–	0.30 × V_{CC}	–	0.30 × V_{CC}	–	0.25 × V_{CC}	V
		V_{CC} = 0.9 to 1.95 V	–	–	0.35 × V_{CC}	–	0.35 × V_{CC}	–	0.30 × V_{CC}	V
		V_{CC} = 2.3 to 2.7 V	–	–	0,7	–	0,7	–	0,7	V
		V_{CC} = 3.0 to 3.6 V	–	–	0,9	–	0,9	–	0,9	V

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = −20 µA; V_{CC} = 0.8 to 3.6 V	V_{CC} − 0.1	–	–	V_{CC} − 0.1	–	V_{CC} − 0.11	–	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	0.75 × V_{CC}	–	–	0.7 × V_{CC}	–	0.6 × V_{CC}	–	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	1,11	–	–	1,03	–	0,93	–	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1,32	–	–	1,30	–	1,17	–	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	2,05	–	–	1,97	–	1,77	–	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1,9	–	–	1,85	–	1,67	–	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2,72	–	–	2,67	–	2,40	–	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2,6	–	–	2,55	–	2,30	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 µA; V_{CC} = 0.8 to 3.6 V	–	–	0,1	–	0,1	–	0,11	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	–	–	0.3 × V_{CC}	–	0.3 × V_{CC}	–	0.33 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	–	–	0,31	–	0,37	–	0,41	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	–	–	0,31	–	0,35	–	0,39	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	–	–	0,31	–	0,33	–	0,36	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	–	–	0,44	–	0,45	–	0,50	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	–	–	0,31	–	0,33	–	0,36	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	–	–	0,44	–	0,45	–	0,50	V

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 to 3.6 V	–	–	±0.1	–	±0.5	–	±0.75	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 to 3.6 V; V_{CC} = 0 V	–	–	±0.2	–	±0.5	–	±0.75	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 to 3.6 V; V_{CC} = 0 to 0.2 V	–	–	±0.2	–	±0.6	–	±0.75	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 to 3.6 V	–	–	0,5	–	0,9	–	1,4	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 3.3 V; per pin [1]	–	–	40	–	50	–	75	mA

[1] One input at V_{CC} − 0.6 V, other input at V_{CC} or GND.

Table 27: Dynamic characteristics

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	Min	Max	
C_L = 5 pF										
t_{pd}	propagation delay	CP to Q, Q; [1]								
		V_{CC} = 0.8 V	–	25,4	–	–	–	–	–	ns
		V_{CC} = 1.1 to 1.3 V	2,9	6,7	14,0	2,6	14,2	2,6	14,2	ns
		V_{CC} = 1.4 to 1.6 V	2,4	4,5	7,6	2,3	8,3	2,3	8,6	ns
		V_{CC} = 1.65 to 1.95 V	1,9	3,5	5,7	1,7	6,5	1,7	6,8	ns
		V_{CC} = 2.3 to 2.7 V	1,7	2,6	3,8	1,4	4,4	1,4	4,7	ns
		V_{CC} = 3.0 to 3.6 V	1,5	2,2	3,1	1,2	3,4	1,2	3,7	ns

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	SD to Q, Q; [1]								
		V_{CC} = 0.8 V	–	19,6	–	–	–	–	–	ns
		V_{CC} = 1.1 to 1.3 V	2,7	5,6	11,0	2,5	11,4	2,5	11,5	ns
		V_{CC} = 1.4 to 1.6 V	2,4	4,0	6,3	2,2	6,9	2,2	7,3	ns
		V_{CC} = 1.65 to 1.95 V	2,0	3,3	4,9	1,7	5,6	1,7	5,9	ns
		V_{CC} = 2.3 to 2.7 V	1,9	2,7	3,7	1,7	4,0	1,7	4,2	ns
		V_{CC} = 3.0 to 3.6 V	1,8	2,5	3,2	1,5	3,6	1,5	3,8	ns
		RD to Q, Q; [1]								
		V_{CC} = 0.8 V	–	19,2	–	–	–	–	–	ns
		V_{CC} = 1.1 to 1.3 V	2,6	5,5	11,0	2,5	11,3	2,5	11,5	ns
		V_{CC} = 1.4 to 1.6 V	2,3	3,9	6,3	2,2	6,8	2,2	7,3	ns
		V_{CC} = 1.65 to 1.95 V	1,9	3,2	5,0	1,8	5,6	1,8	5,9	ns
		V_{CC} = 2.3 to 2.7 V	1,9	2,6	3,6	1,7	4,1	1,7	4,3	ns
		V_{CC} = 3.0 to 3.6 V	1,8	2,4	3,3	1,5	3,6	1,5	3,8	ns
f_{max}	maximum frequency	CP								
		V_{CC} = 0.8 V	–	53	–	–	–	–	–	MHz
		V_{CC} = 1.1 to 1.3 V	–	203	–	170	–	170	–	MHz
		V_{CC} = 1.4 to 1.6 V	–	347	–	310	–	300	–	MHz
		V_{CC} = 1.65 to 1.95 V	–	435	–	400	–	390	–	MHz
		V_{CC} = 2.3 to 2.7 V	–	550	–	490	–	480	-	MHz
		V_{CC} = 3.0 to 3.6 V	–	619	–	550	–	510	–	MHz
C_L = 15 pF										
t_{pd}	propagation delay	CP to Q, Q; [1]								
		V_{CC} = 0.8 V	–	32,4	–	–	–	–	–	ns
		V_{CC} = 1.1 to 1.3 V	3,5	8,3	17,6	3,3	17,8	3,3	18,0	ns
		V_{CC} = 1.4 to 1.6 V	3,2	5,6	9,5	2,8	10,5	2,8	11,1	ns
		V_{CC} = 1.65 to 1.95 V	2,7	4,6	7,2	2,5	8,1	2,5	8,6	ns
		V_{CC} = 2.3 to 2.7 V	2,4	3,6	5,2	2,2	5,8	2,2	6,2	ns
		V_{CC} = 3.0 to 3.6 V	2,2	3,2	4,4	2,0	4,9	2,0	5,2	ns

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	SD to Q, Q; [1]								
		V_{CC} = 0.8 V	–	26,7	–	–	–	–	–	ns
		V_{CC} = 1.1 to 1.3 V	3,3	7,3	14,7	3,1	15,2	3,1	15,4	ns
		V_{CC} = 1.4 to 1.6 V	3,2	5,2	8,3	2,9	9,0	2,9	9,5	ns
		V_{CC} = 1.65 to 1.95 V	2,8	4,3	6,4	2,5	7,1	2,5	7,5	ns
		V_{CC} = 2.3 to 2.7 V	2,8	3,7	5,1	2,2	5,5	2,2	5,8	ns
		V_{CC} = 3.0 to 3.6 V	2,5	3,5	4,6	2,4	5,0	2,4	5,2	ns
		RD to Q, Q; [1]								
		V_{CC} = 0.8 V	–	26,1	–	–	–	–	–	ns
		V_{CC} = 1.1 to 1.3 V	3,2	7,2	14,5	3,1	15,0	3,1	15,2	ns
		V_{CC} = 1.4 to 1.6 V	3,1	5,1	8,4	2,7	9,2	2,7	9,7	ns
		V_{CC} = 1.65 to 1.95 V	2,7	4,3	6,5	2,6	7,3	2,6	7,7	ns
		V_{CC} = 2.3 to 2.7 V	2,6	3,6	5,0	2,4	5,5	2,4	5,8	ns
		V_{CC} = 3.0 to 3.6 V	2,4	3,4	4,6	2,3	5,0	2,3	5,2	ns
f_{max}	maximum frequency	CP								
		V_{CC} = 0.8 V	–	50	–	–	–	–	–	MHz
		V_{CC} = 1.1 to 1.3 V	–	181	–	120	–	120	–	MHz
		V_{CC} = 1.4 to 1.6 V	–	301	–	190	–	160	–	MHz
		V_{CC} = 1.65 to 1.95 V	–	407	–	240	–	190	–	MHz
		V_{CC} = 2.3 to 2.7 V	–	422	–	300	–	270	–	MHz
		V_{CC} = 3.0 to 3.6 V	–	481	–	320	–	300	–	MHz
C_L = 5 pF, 10 pF, 15 pF and 30 pF										
t_W	pulse width	CP HIGH or LOW								
		V_{CC} = 1.1 to 1.3 V	–	2,1	–	2,7	–	2,7	–	ns
		V_{CC} = 1.4 to 1.6 V	–	1,1	–	1,5	–	1,5	–	ns
		V_{CC} = 1.65 to 1.95 V	–	0,9	–	1,6	–	1,6	–	ns
		V_{CC} = 2.3 to 2.7 V	–	0,6	–	1,7	–	1,7	–	ns
		V_{CC} = 3.0 to 3.6 V	–	0,6	–	1,9	–	1,9	–	ns

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	Min	Max	
t_W	pulse width	SD or RD LOW								
		V_{CC} = 1.1 to 1.3 V	–	4,2	–	11,3	–	11,5	–	ns
		V_{CC} = 1.4 to 1.6 V	–	2,3	–	6,2	–	6,4	–	ns
		V_{CC} = 1.65 to 1.95 V	–	1,8	–	4,8	–	5,0	–	ns
		V_{CC} = 2.3 to 2.7 V	–	1,2	–	3,3	–	3,5	–	ns
		V_{CC} = 3.0 to 3.6 V	–	1,1	–	2,6	–	2,8	–	ns
t_{su}	set-up time	D to CP HIGH								
		V_{CC} = 0.8 V	–	3,4	–	–	–	–	–	ns
		V_{CC} = 1.1 to 1.3 V	–	0,6	–	1,2	–	1,2	–	ns
		V_{CC} = 1.4 to 1.6 V	–	0,3	–	0,6	–	0,6	–	ns
		V_{CC} = 1.65 to 1.95 V	–	0,4	–	0,5	–	0,5	–	ns
		V_{CC} = 2.3 to 2.7 V	–	0,2	–	0,4	–	0,4	–	ns
		V_{CC} = 3.0 to 3.6 V	–	0,3	–	0,4	–	0,4	–	ns
		D to CP LOW								
		V_{CC} = 0.8 V	–	3,0	–	–	–	–	–	ns
		V_{CC} = 1.1 to 1.3 V	–	0,5	–	1,2	–	1,2	–	ns
		V_{CC} = 1.4 to 1.6 V	–	0,3	–	0,7	–	0,7	–	ns
		V_{CC} = 1.65 to 1.95 V	–	0,4	–	0,7	–	0,7	–	ns
		V_{CC} = 2.3 to 2.7 V	–	0,5	–	0,7	–	0,7	–	ns
		V_{CC} = 3.0 to 3.6 V	–	0,6	–	0,8	–	0,8	–	ns
t_h	hold time	D to CP								
		V_{CC} = 0.8 V	–	−1,9	–	–	–	–	–	ns
		V_{CC} = 1.1 to 1.3 V	–	−0,3	–	0,5	–	0,5	–	ns
		V_{CC} = 1.4 to 1.6 V	–	−0,2	–	0,2	–	0,2	–	ns
		V_{CC} = 1.65 to 1.95 V	–	−0,2	–	0,1	–	0,1	–	ns
		V_{CC} = 2.3 to 2.7 V	–	−0,2	–	0,1	–	0,1	–	ns
		V_{CC} = 3.0 to 3.6 V	–	−0,2	–	0,1	–	0,1	–	ns

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		T_{amb} −40 °C to +125 °C		Unit
			Min	Typ*	Max	Min	Max	Min	Max	
t_{rec}	recovery time	RD								
		V_{CC} = 1.1 to 1.3 V	–	−0,5	–	-0,9	–	−0,9	–	ns
		V_{CC} = 1.4 to 1.6 V	–	−0,2	–	-0,6	–	−0,6	–	ns
		V_{CC} = 1.65 to 1.95 V	–	−0,2	–	-0,4	–	−0,4	–	ns
		V_{CC} = 2.3 to 2.7 V	–	−0,1	–	-0,1	–	−0,1	–	ns
		V_{CC} = 3.0 to 3.6 V	–	−0,1	–	-0,1	–	−0,1	–	ns
		SD								
		V_{CC} = 1.1 to 1.3 V	–	−0,5	–	−0,3	–	−0,3	–	ns
		V_{CC} = 1.4 to 1.6 V	–	−0,4	–	−0,1	–	−0,1	–	ns
		V_{CC} = 1.65 to 1.95 V	–	−0,3	–	0	–	0	–	ns
		V_{CC} = 2.3 to 2.7 V	–	−0,2	–	0,1	–	0,1	–	ns
		V_{CC} = 3.0 to 3.6 V	–	−0,1	–	0,1	–	0,1	–	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [2]								
		V_{CC} = 0.8 V	–	2,8	–	–	–	–	–	pF
		V_{CC} = 1.1 to 1.3 V	–	2,9	–	–	–	–	–	pF
		V_{CC} = 1.4 to 1.6 V	–	3,0	–	–	–	–	–	pF
		V_{CC} = 1.65 to 1.95 V	–	3,0	–	–	–	–	–	pF
		V_{CC} = 2.3 to 2.7 V	–	3,5	–	–	–	–	–	pF
		V_{CC} = 3.0 to 3.6 V	–	3,9	–	–	–	–	–	pF

* All typical values are measured at nominal V_{CC}.
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

Power calculations

The static power consumption calculation is much dependent on the input voltage level: if it is properly set to either V_{CC} or GND level, we can use the static supply current I_{CC} for calculating the power consumption: $P_{static} = V_{CC} \times I_{CC}$

In case Vin is at some intermediate level and the device is operating in undefined state, both NMOS and PMOS transistors of the input stage may be conducting and then we need to use the

The dynamic power consumption calculation is:

$$P_{dyn} = C_{PD} \times {V_{CC}}^2 \times f_i \times N + \sum [C_L \times {V_{CC}}^2 \times f_o]$$

Where:

f_I = input frequency in MHz
f_O = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = number of inputs switching
$\sum(C_L \times V_{CC}^2 \times f_O)$ = sum of inputs

Special Features

AUP devices are fully specified for partial power-down applications that use the I_{OFF} feature. The I_{OFF} circuitry disables the output, preventing damage caused by backflow current passing through the device when it is powered down.

Combination logic offers two or more unique functions in a single package. The functions are either stand alone or they can be cascaded.

Figure 9.7a shows a buffer and inverter with no internal connection as a stand-alone example and Figure 9.7b shows the output of an AND gate being applied to one of the inputs of an OR gate as a cascaded example.

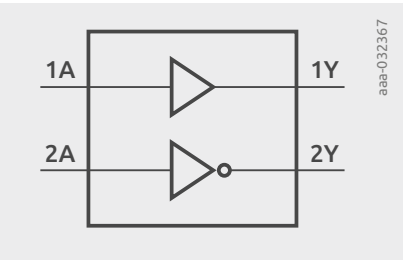


Figure 9.7a | Stand-alone combination logic

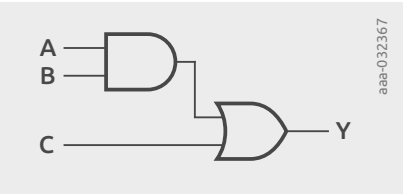


Figure 9.7b | Cascaded combination logic

Combination logic is typically the integration of discrete logic solutions to known issues on PCB. Solutions based on combination logic have lower total cost, including pick and place cost, and reduced PCB area. It also helps to optimize and simplify the PCB layout and signal routing.

An overview of features available for the AUP logic family:

- Low threshold inputs
- Schmitt-Trigger/Schmitt Action inputs
- 3.6 V tolerant I/O's
- Open drain outputs
- Power-off protection (I_{OFF})
- Dual supply translations

Summary

Designed for high-performance, low-power applications, these low-voltage, Si-gate CMOS devices provide logic solutions with very low static and dynamic power dissipation. Some key features are:

- Very low dynamic power dissipation (CPD)
- t_{pd} of 2.5 ns at V_{CC} of 2.5 V
- Wide supply voltage range (0.8 V to 3.6 V)
- Schmitt-trigger action on all inputs
- Low-threshold input options
- 1.9 mA balanced output drive
- Over-voltage tolerant I/Os
- Fully specified (-40 to +85°C and -40 to +125°C)
- Automotive options (-Q100 suffix)
- Pb-free, RoHS compliant and Dark Green

9.6 The AXP Logic Family

Introduction to family / General description

The AXP family of Si-gate CMOS devices uses low threshold process technology and next-generation packaging to deliver extremely small logic functions. All AXP solutions offer low propagation delay and standby current, enabling both high-speed and low power dissipation capacitance Applications.

AXP provides higher speed than AUP but retains low power dissipation capacitance (CPD). Because of its use of low threshold transistors, AXP is the first logic family fully specified at 0.8 V, allowing to migrate applications from 1.8 V and 1.2 V easily.

Types released in AXP technology can support overvoltage-tolerant inputs, Schmitt-trigger inputs, low-threshold inputs, partial power-down circuitry and open-drain outputs.

Construction

The AXP family devices are built in C050 process with a gate length of 250 nm. This approach results in a typical input capacitance of 0.5 pF. AXP devices are modelled as a 0.8 pF capacitance on the input supply (CPDI) and a 7.6 pF capacitance on the output supply (CPDO). The power consumption capacitance, C_{PD}, is typically at 2.9 pF. The process technology is Pb-free, RoHS and Dark Green compliant. Bond wiring is done with copper.

Input Output structures

The AXP family devices are built with overvoltage tolerant input stages (3.6 V) and allows a supply range of 0.7 V to 2.75 V.

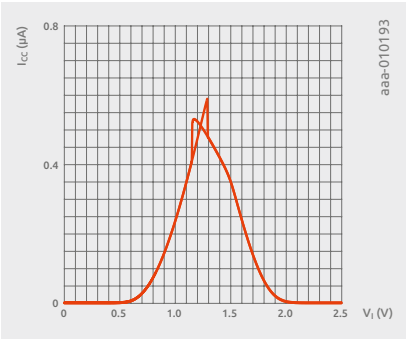
It is recommended to drive all logic inputs with a defined value, not to leave them floating.

Input Output figures

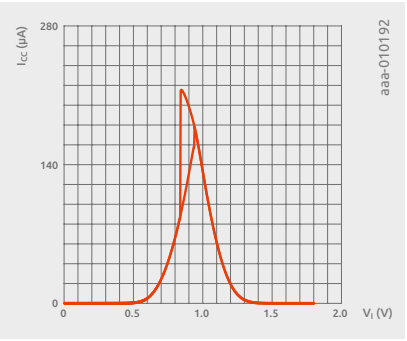
Input figures

The AXP inputs are fully specified for supply voltage ranges of 2.3–2.7 V, 1.65–1.95 V, 1.4–1.6 V, 1.1–1.3 V and 0.75–0.85 V. The ESD protection circuit used results in the input being over voltage tolerant to 2.75 V. This tolerance permits the application of input signals that exceed the supply voltage. The input options include Schmitt-trigger inputs and Schmitt-trigger action inputs. Schmitt-trigger action makes the input tolerant of slower input transition rates. Hysteresis is not specified, but the input can tolerate input transition rise and fall rates of 200 ns/V. Schmitt-trigger inputs include an input hysteresis specification and have no restriction on input transition rates.

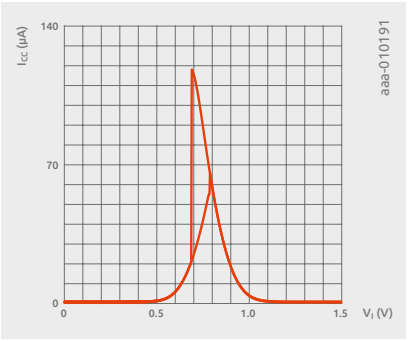
The following figures show the typical characteristics of the Schmitt-trigger action input.



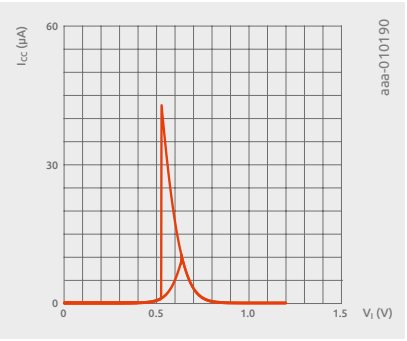
2.5 V Schmitt action



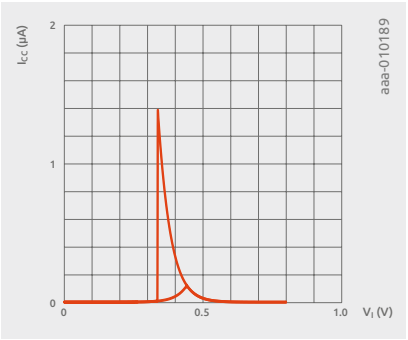
1.8 V Schmitt action



1.5 V Schmitt action

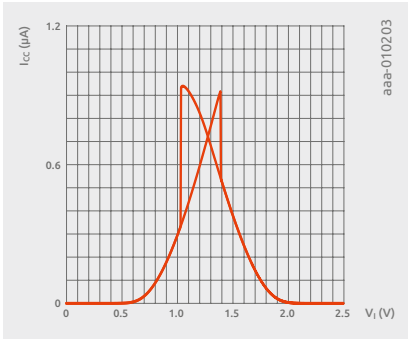


1.2 V Schmitt action

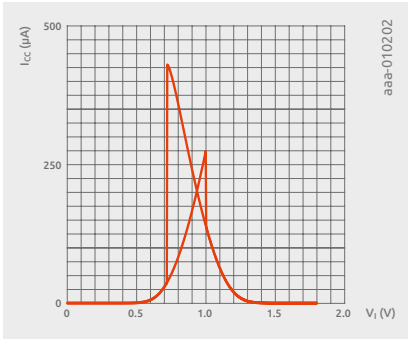


0.8 V Schmitt action

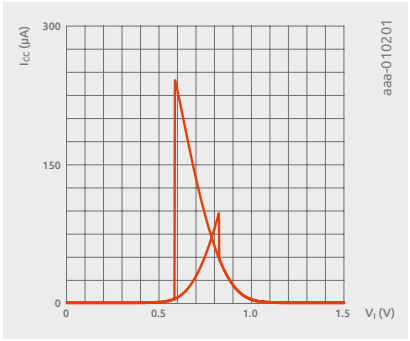
The following figures show the typical characteristics of the Schmitt-trigger input.



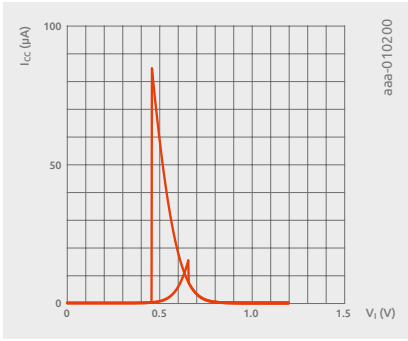
2.5 V Schmitt trigger



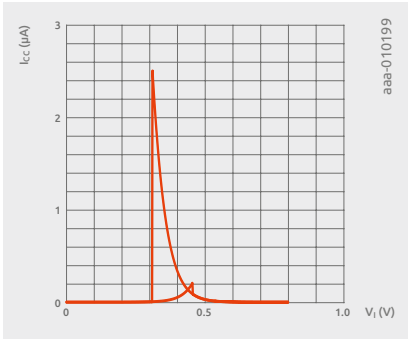
1.8 V Schmitt trigger



1.5 V Schmitt trigger



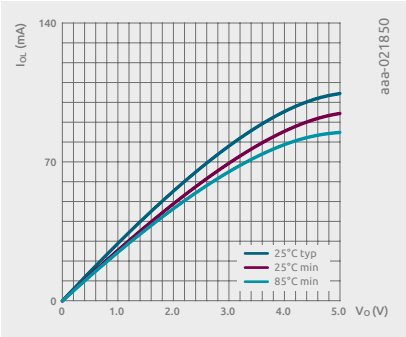
1.2 V Schmitt trigger



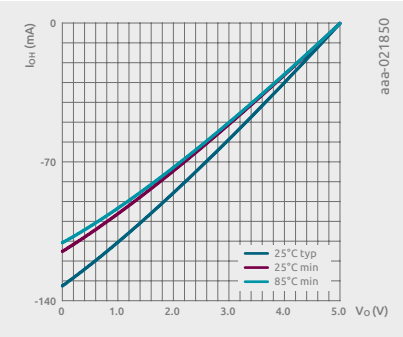
0.8 V Schmitt trigger

Output figures

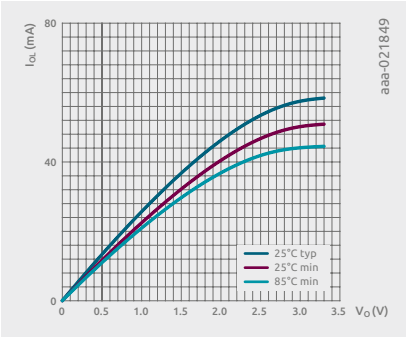
The output is fully specified for supply voltage ranges of 4.5–5.5 V, 3.0–3.6 V, 2.3–2.7 V, 1.65–1.95 V and 1.4–1.6 V. To support partial power down mode, the output features I_{OFF}, which ensures there is no current leakage path through the outputs when the device supply voltage is set to 0 V.



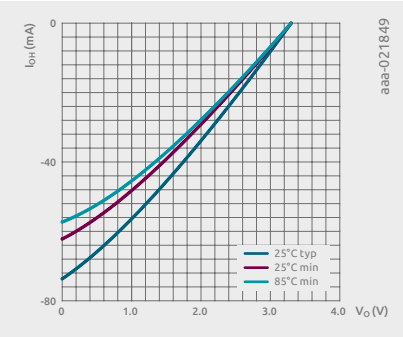
I_{OL} at 5.0 V



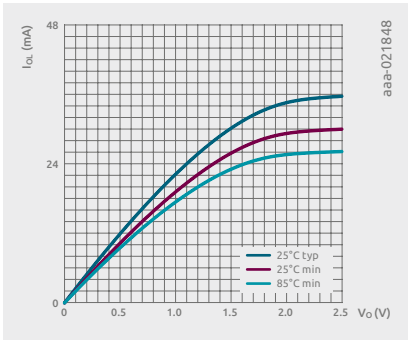
I_{OH} at 5.0 V



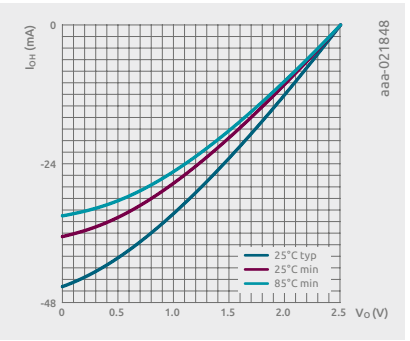
I_{OL} at 3.5 V



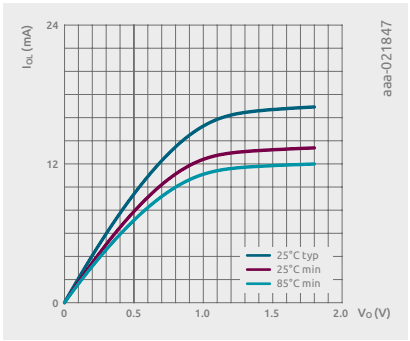
I_{OH} at 3.5 V



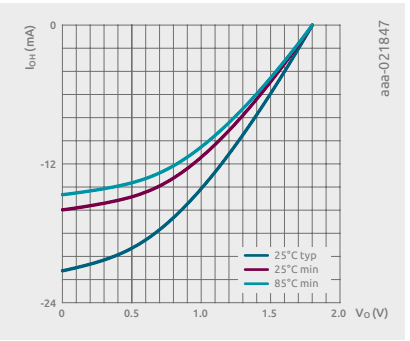
I_{OL} at 2.5 V



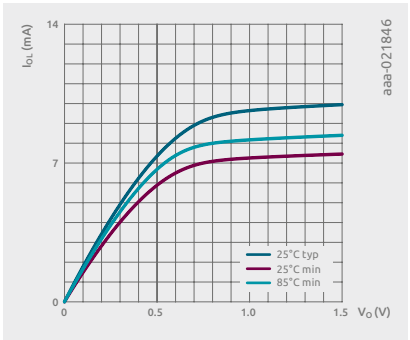
I_{OH} at 2.5 V



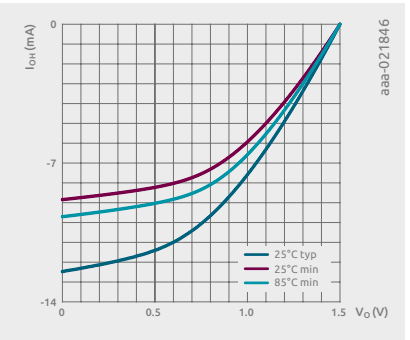
I_{OL} at 1.8 V



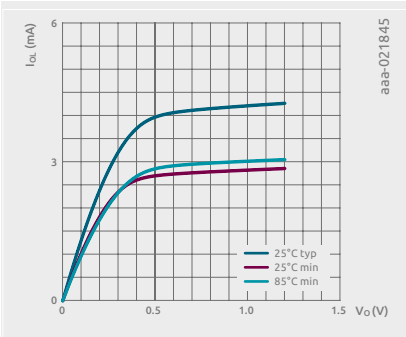
I_{OH} at 1.8 V



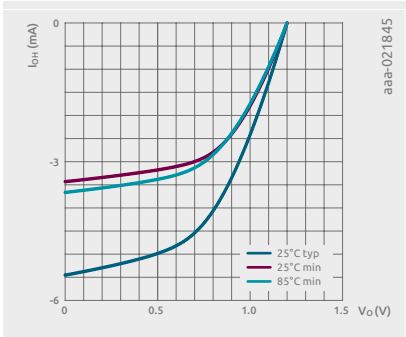
I_{OL} at 1.5 V



I_{OH} at 1.5 V



I_{OL} at 1.2 V



I_{OH} at 1.2 V

Operating Conditions

Table 28: Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0,5	+3,3	V
I_{IK}	input clamping current	$V_I < 0\,V$	−50	–	mA
V_I	input voltage	*	−0,5	+3,3	V
I_{OK}	output clamping current	$V_O < 0\,V$	−50	–	mA
V_O	output voltage	*	−0,5	+3,3	V
I_O	output current	$V_O = 0\,V$ to V_{CC}	–	±20	mA
I_{CC}	supply current		–	50	mA
I_{GND}	ground current		−50	–	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\,°C$ to $+85\,°C$	–	250	mW

* The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Table 29: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0,7	2,75	V
V_I	input voltage		0	2,75	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0\,V$	0	2,75	V
T_{amb}	ambient temperature		−40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.7\,V$ to $2.75\,V$	0	200	ns/V

Table 30: Static characteristics

At recommended operating conditions, unless otherwise specified; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		Unit
			Min	Typ*	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 0.75 to 0.85 V	$0.75\,V_{CC}$	–	–	$0.75\,V_{CC}$	–	V
		V_{CC} = 1.1 to 1.95 V	$0.65\,V_{CC}$	–	–	$0.65\,V_{CC}$	–	V
		V_{CC} = 2.3 to 2.7 V	1,6	–	–	1,6	–	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.75 to 0.85 V	–	–	$0.25\,V_{CC}$	–	$0.25\,V_{CC}$	V
		V_{CC} = 1.1 to 1.95 V	–	–	$0.35\,V_{CC}$	–	$0.35\,V_{CC}$	V
		V_{CC} = 2.3 to 2.7 V	–	–	0,7	–	0,7	V

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		Unit
			Min	Typ*	Max	Min	Max	
V_{OH}	HIGH-level output voltage	I_O = -20 µA; V_{CC} = 0.7 V	–	0,69	–	–	–	V
		I_O = -100 µA; V_{CC} = 0.75 V	0,65	–	–	0,65	–	V
		I_O = -2 mA; V_{CC} = 1.1 V	0,825	–	–	0,825	–	V
		I_O = -3 mA; V_{CC} = 1.4 V	1,05	–	–	1,05	–	V
		I_O = -4.5 mA; V_{CC} = 1.65 V	1,2	–	–	1,2	–	V
		I_O = -8 mA; V_{CC} = 2.3 V	1,7	–	–	1,7	–	V
V_{OL}	LOW-level output voltage	I_O = 20 µA; V_{CC} = 0.7 V	–	0,01	–	–	–	V
		I_O = 100 µA; V_{CC} = 0.75 V	–	–	0,1	–	0,1	V
		I_O = 2 mA; V_{CC} = 1.1 V	–	–	0,275	–	0,275	V
		I_O = 3 mA; V_{CC} = 1.4 V	–	–	0,35	–	0,35	V
		I_O = 4.5 mA; V_{CC} = 1.65 V	–	–	0,45	–	0,45	V
		I_O = 8 mA; V_{CC} = 2.3 V	–	–	0,7	–	0,7	V
I_I	input leakage current	V_I = 0 to 2.75 V; V_{CC} = 0 to 2.75 V [1]	–	0,001	±0.1	–	±0.5	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 to 2.75 V; V_{CC} = 0 V [1]	–	0,01	±0.1	–	±0.5	µA
ΔI_{OFF}	additional power- off leakage current	V_I or V_O = 0 V or 2.75 V; V_{CC} = 0 to 0.1 V [1]	–	0,02	±0.1	–	±0.5	µA
I_{CC}	supply current	V_I = 0 V or V_{CC}; I_O = 0 A [1]	–	0,01	0,3	–	0,6	µA

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		Unit
			Min	Typ*	Max	Min	Max	
ΔI_{CC}	additional supply current	V_I = V_{CC} − 0.5 V; I_O = 0 A; V_{CC} = 2.5 V	–	2	100	–	150	µA

[1] Typical values are measured at V_{CC} = 1.2 V.

Table 31: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	T_{amb} 25 °C			T_{amb} −40 °C to +85 °C		Unit
			Min	Typ*	Max	Min	Max	
t_{pd}	propagation delay	A to Y [1]						
		V_{CC} = 0.75 to 0.85 V	3	11	33	2	100	ns
		V_{CC} = 1.1 to 1.3 V	1,8	4,3	7,0	1,7	7,3	ns
		V_{CC} = 1.4 to 1.6 V	1,5	3,1	4,7	1,3	5,1	ns
		V_{CC} = 1.65 to 1.95 V	1,2	2,6	3,8	1,1	4,1	ns
		V_{CC} = 2.3 to 2.7 V	1,0	2,0	2,8	0,9	3,1	ns
t_t	transition time	V_{CC} = 2.7 V [2]	–	–	–	1,0	–	ns
C_I	input capacitance	V_I = 0 V or V_{CC}; V_{CC} = 0 to 2.75 V	–	0,5	–	–	–	pF
C_O	output capacitance	V_O = 0 V; V_{CC} = 0 V	–	1,0	–	–	–	pF
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = 0 V to V_{CC} [3]						
		V_{CC} = 0.75 to 0.85 V	–	2,3	–	–	–	pF
		V_{CC} = 1.1 to 1.3 V	–	2,3	–	–	–	pF
		V_{CC} = 1.4 to 1.6 V	–	2,4	–	–	–	pF
		V_{CC} = 1.65 to 1.95 V	–	2,4	–	–	–	pF
		V_{CC} = 2.3 to 2.7 V	–	2,7	–	–	–	pF

* All typical values are measured at nominal V_{CC}.
[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

Power calculations

The static power consumption calculation is much dependent on the input voltage level: if it is properly set to either V_{CC} or GND level, we can use the static supply current I_{CC} for calculating the power consumption: $P_{static} = V_{CC} \times I_{CC}$

In case Vin is at some intermediate level and the device is operating in undefined state, both NMOS and PMOS transistors of the input stage may be conducting and then we need to use the

The dynamic power consumption calculation is:

$$P_{dyn} = C_{PD} \times {V_{CC}}^2 \times f_i \times N + \sum [C_L \times {V_{CC}}^2 \times f_o]$$

Where:

f_I = input frequency in MHz
f_O = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = number of inputs switching
$\sum(C_L \times V_{CC}^2 \times f_O)$ = sum of inputs

Special Features

- Wide supply voltage range and fully specified at 0.8 V
- Very low dynamic power dissipation & standby current (0.6 µA)
- Typical 2.9 ns low propagation delay at V_{CC} of 1.8 V
- Schmitt action on all inputs & overvoltage tolerant inputs
- ±4.5 mA balanced output drive

Summary

Designed for high-performance, low-power applications, these low-voltage, Si-gate CMOS devices provide logic solutions with very low static and dynamic power dissipation.

9.7 The LVT/ALVT Logic Family

Introduction to family / General description

Nexperia has two low voltage families optimized for backplane driving applications: LVT (Low Voltage Technology) and ALVT (Advanced LVT). The purpose of this note is to provide better insight into both families for optimal use by designers in their applications.

ALVT family devices are intended primarily for fast low voltage bus driver applications, especially driving low bus impedances such as backplanes. For this range of applications, a number of parameters are important such as operating voltage range, propagation delay, drive capability and power. Other important factors, discussed below, are power-up/down characteristics, 5 Volt input and output capability, bus hold and ground bounce.

Construction

Both families are fabricated using QUBiC, an advanced BiCMOS process, where the best properties of bipolar transistors (f_T = 17 GHz) are combined with optimized CMOS (0.65–0.8 micron). In addition, special components can be built in such as Schottky diodes and zener diodes for specific requirements. QUBiC processing enables short propagation delay times combined with low power dissipation, low noise and high output drive. The process also allows low temperature dependency of AC and DC characteristics.

Due to the trade-off between speed and ground bounce, ALVT focuses on bus-wide devices with multiple GND and V_{CC} pins (flow-through architecture). ALVT devices have versions with built-in damping resistors (for example, '2244 or '162244) to minimize undershoot, especially for driving memory busses.

ALVT is different from LVT in two ways. First ALVT is fully specified at V_{CC} = 2.5 V, and second, it is about 40% faster than LVT. Due to the trade-off between speed and ground bounce, ALVT focuses on bus-wide devices with multiple GND and V_{CC} pins (flow-through architecture). Having the same speed in a standard pin 8 bit device would require the speed to be tuned down to a level comparable to LVT. As a result, LVT has a much wider product portfolio with a variety of 8 to 10-bit bus functions and also some very fast, lower drive gates and flip-flops. Both families have versions with built-in damping resistors (for example, '2244 or '162244) to minimize undershoot, especially for driving memory busses.

Input Output structures

Figure 9.8 gives a simplified version of the internal buffer circuit, with the output enable function (OE) and other details (some of which will be discussed later) omitted. Its purpose is to show the basic aspects of the internal circuit so that applying LVT circuits is made easier and certain aspects of the datasheet are clarified. The input uses a small CMOS inverter stage with a low input capacitance, so no drive energy is needed. The output LOW is bipolar (Q4) with a small (M7) in parallel, and the output HIGH is a combination of a bipolar transistor (Q2) and PMOS (M4) to pull the output to the full V_{CC}. Bipolar transistors introduce less bounce than pure CMOS. The NMOS M7 is very small and therefore does not affect ground bounce. The PMOS transistor M4 is delayed via the inverters INV1/INV2 so that it becomes active somewhat later than Q2 with only a minimal effect on V_{CC} bounce. This construction enables the best possible trade-off between speed and bounce.

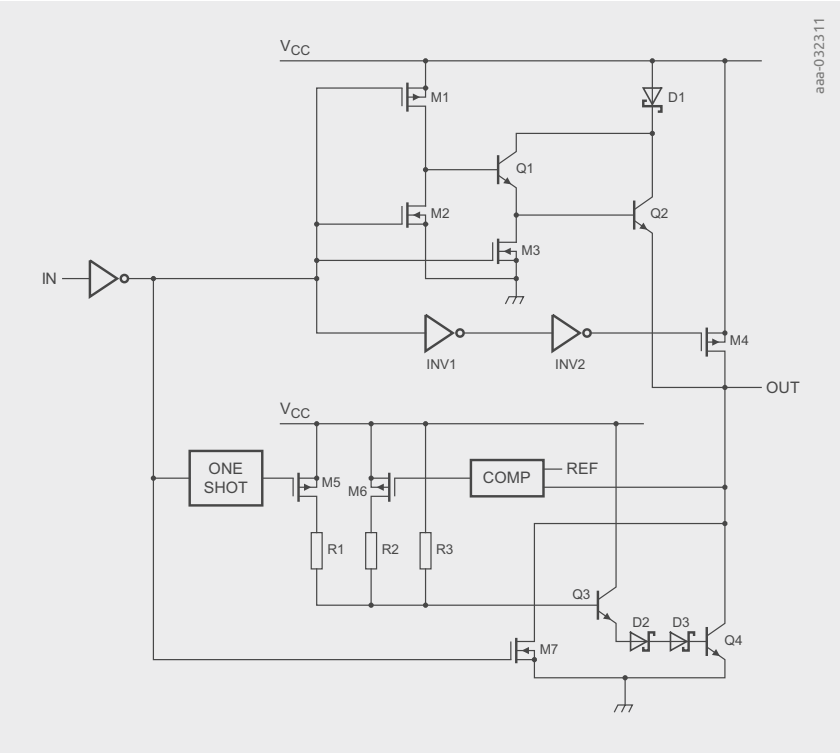


Figure 9.8 | Simplified ALVT circuit

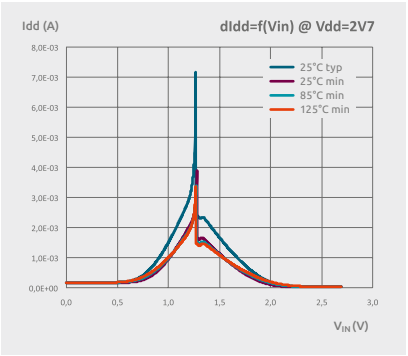
The drive of Q2 in the active HIGH state, taken care of by M1, M2 and Q1, is standard for advanced BiCMOS and makes optimum use of MOS and bipolar transistors to get the fastest, lowest internal capacitance inverter. M3 ensures a fast turn-off of Q2 when the output goes LOW or into 3-state. When the output is forced LOW, a 'power-on-demand' circuit is activated. A one shot delivers Q4 with a high base current (via M5, R1 and Q3), which will quickly pull the output low. Additional base current is provided via M6/R2 and R3. The path M6/R2 is connected to the output voltage via a very fast comparator. When the output drops lower than approximately 1 V, the current path via M6/R2 is blocked. The diodes D2/D3 prevent deep saturation of Q4 to enable quick turn-off.

This, at first sight, rather complex circuit ensures a very fast transition to around 1 V, and below that value the output voltage smooths out somewhat so that the amount of ringing generated is kept to a minimum. Also, when the output is active LOW, a very low current is drained from the supply voltage. When a glitch appears on the output trying to pull the output HIGH, the diodes D2/D3 stop conducting, providing base current into Q3/Q4 so that the bus is pulled LOW again. This structure provides an excellent dynamic behavior, little ringing and good glitch suppression combined with low power dissipation. When the output is in 3-state or active HIGH, only a small bias current flows (for the power-up/down circuit discussed in Section 3.1) while in the active LOW state some current flows via R3, which may vary somewhat among part types. Therefore I_{CCH} and I_{CCZ} are low, while I_{CCL} is somewhat higher.

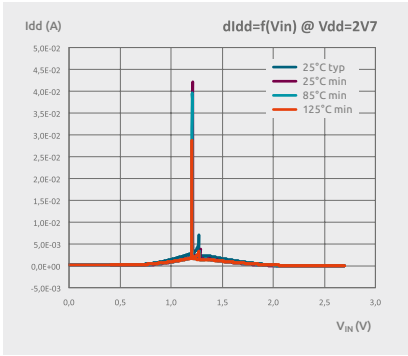
It is recommended to drive all logic inputs with a defined value, not to leave them floating.

Input and Output figures

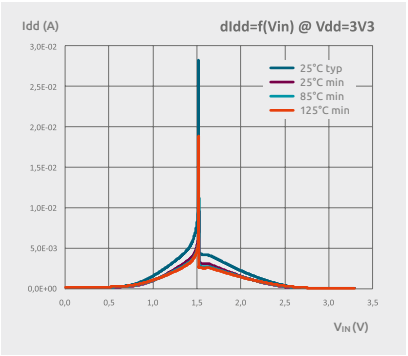
Input Figures for ALVT



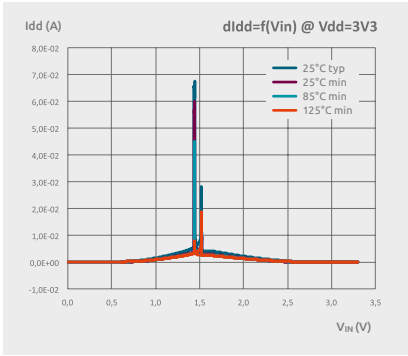
ALVT input curves at 2V7



ALVT Schmitt-Trigger input curves at 2V7

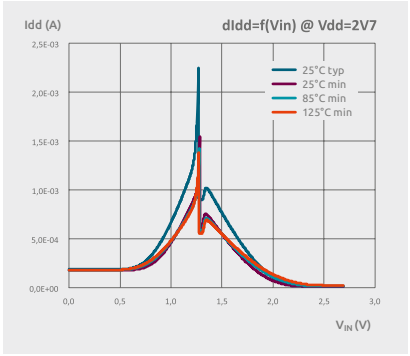


ALVT input curves at 3V3

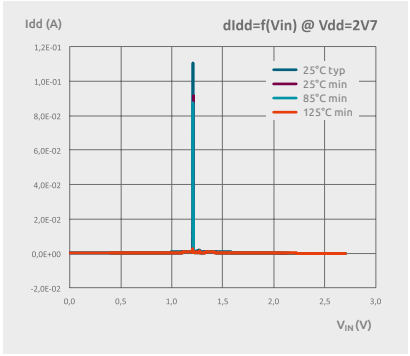


ALVT Schmitt-Trigger input curves at 3V3

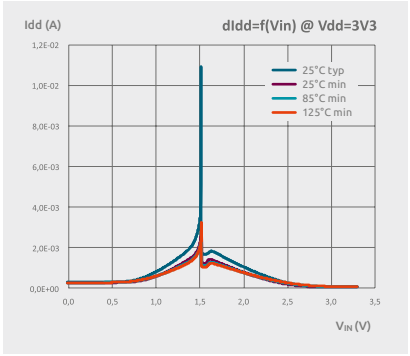
Input Figures for LVT



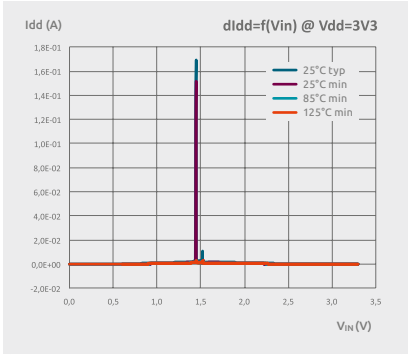
LVT input curves at 2V7



LVT Schmitt-Trigger input curves at 2V7

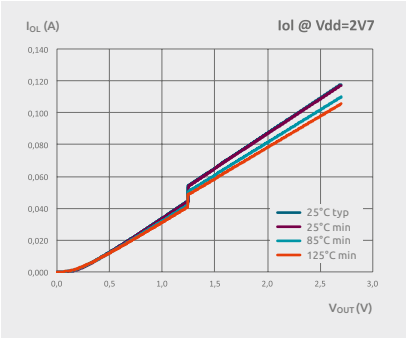


LVT input curves at 3V3

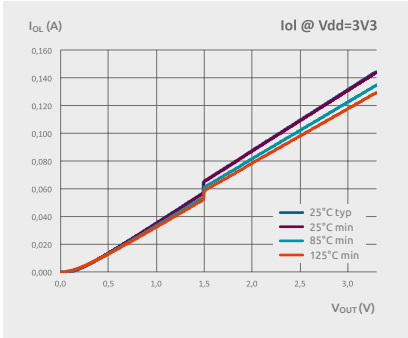


LVT Schmitt-Trigger input curves at 3V3

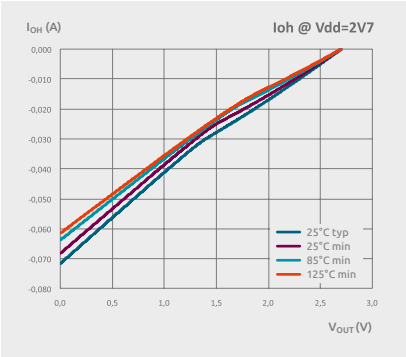
Output figures for ALVT



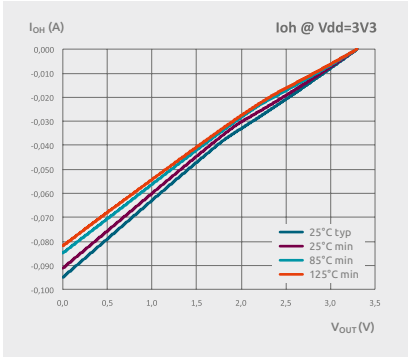
ALVT output curves at 2V7



ALVT output curves at 3V3

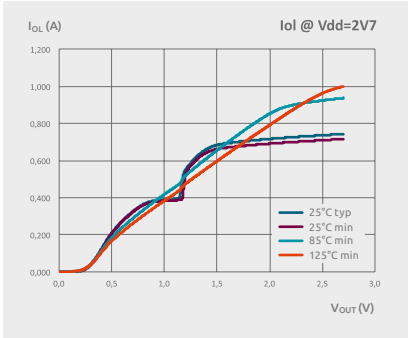


ALVT output curves at 2V7

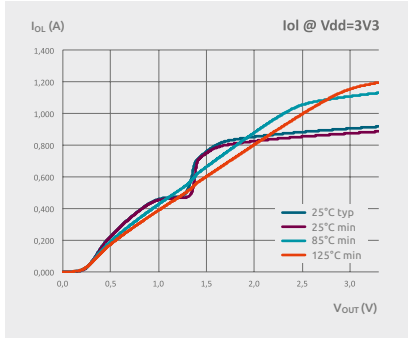


ALVT output curves at 3V3

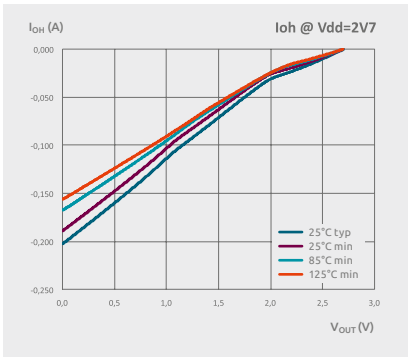
Output figures for LVT



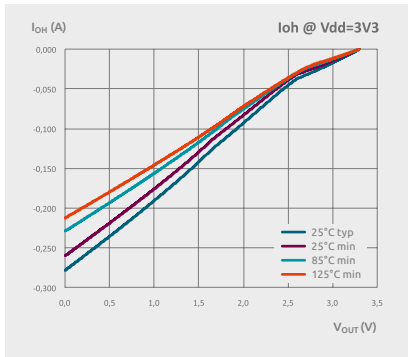
LVT output curves at 2V7



LVT output curves at 3V3



LVT output curves at 2V7



LVT output curves at 3V3

Operating Conditions of ALVT

Table 32: Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0,5	+4,6	V
V_I	input voltage	*	−1,2	+7,0	V
V_O	output voltage	output in OFF-state or HIGH-state *	−0,5	+7,0	V
I_{IK}	input clamping current	$V_I < 0$ V	–	−50	mA
I_{OK}	output clamping current	$V_O < 0$ V	–	−50	mA
I_O	output current	output in LOW-state	–	128	mA
		output in HIGH-state	–	−64	mA
T_{stg}	junction temperature		−65	+150	°C
T_j	storage temperature	**	–	150	°C

* The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

** The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

Table 33: Recommended operating conditions

Symbol	Parameter	Conditions	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		Unit
			Min	Max	Min	Max	
V_{CC}	supply voltage		2,3	2,7	3,0	3,6	V
V_I	input voltage		0	5,5	0	5,5	V
I_{OH}	HIGH-level output current		–	-8	–	−12	mA
I_{OL}	LOW-level output current	none	–	12	–	12	mA
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	–	10	–	10	ns/V
T_{amb}	ambient temperature	free-air	−40	+85	−40	+85	°C

Table 34: Static characteristics

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
V_{CC} = 2.5 V ± 0.2 V						
V_{IK}	input clamping voltage	V_{CC} = 2.3 V; I_{IK} = −18 mA	–	−0,85	−1,2	V
V_{IH}	HIGH-level input voltage		1,7	–	–	V
V_{IL}	LOW-level input voltage		–	–	0,7	V
V_{OH}	HIGH-level output voltage	V_{CC} = 2.3 to 3.6 V; I_O = -100 µA	V_{CC} − 0.2	VCC	–	V
		V_{CC} = 2.3 V; I_O = -8 mA	1,8	2,1	–	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.3 V; I_O = 100 µA	–	0,07	0,2	V
		V_{CC} = 2.3 V; I_O = 24 mA	–	0,3	0,5	V
		V_{CC} = 2.3 V; I_O = 8 mA	–	–	0,4	V
$V_{OL(pu)}$	power-up LOW-level output voltage	V_{CC} = 2.7 V; I_O = 1 mA; V_I = V_{CC} or GND [1]	–	–	0,55	V
I_I	input leakage current	all input pins				
		V_{CC} = 0 V or 2.7 V; V_I = 5.5 V [2]	–	0,1	10	µA
		control pins				
		V_{CC} = 2.7 V; V_I = V_{CC} or GND	–	0,1	±1	µA
		data pins; [2]				
		V_{CC} = 2.7 V; V_I = V_{CC}	–	0,1	1	µA
		V_{CC} = 2.7 V; V_I = 0 V	–	0,1	−5	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 to 4.5 V	–	0,1	±100	µA
I_{BHL}	bus hold LOW current	data inputs; V_{CC} = 2.3 V; V_I = 0.7 V	-	90	–	µA
I_{BHH}	bus hold HIGH current	data inputs; V_{CC} = 2.3 V; V_I = 1.7 V	-	−10	–	µA
I_{EX}	external current	output in HIGH-state when $V_O > V_{CC}$; V_O = 5.5 V; V_{CC} = 2.3 V	–	10	125	µA

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
$I_{O(pu/pd)}$	power-up/ power-down output current	$V_{CC} \leq 1.2$ V; $V_O = 0.5$ V to V_{CC}; V_I = GND or V_{CC}; $\overline{nOE}$ = don't care [3]	–	1	±100	µA
I_{OZ}	OFF-state output current	$V_{CC} = 2.7$ V; $V_I = V_{IL}$ or V_{IH}				
		output HIGH-state; $V_O = 2.3$ V	–	0,5	5	µA
		output LOW-state; $V_O = 0.5$ V	–	0,5	−5	µA
I_{CC}	supply current	$V_{CC} = 2.7$ V; V_I = GND or V_{CC}; $I_O = 0$ A				
		outputs HIGH-state	–	0,04	0,1	mA
		outputs LOW-state	–	2,3	4,5	mA
		outputs disabled [4]		0,04	0,1	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 2.3$ to 2.7 V; one input at $V_{CC} - 0.6$ V; other inputs at V_{CC} or GND [5]	–	0,04	0,4	mA
C_I	input capacitance	$V_I = 0$ V or V_{CC}	–	3	–	pF
C_O	output capacitance	$V_O = 0$ V or V_{CC}	–	9	–	pF
$V_{CC} = 3.3$ V ± 0.3 V						
V_{IK}	input clamping voltage	$V_{CC} = 3.0$ V; $I_{IK} = -18$ mA	–	−0,85	−1,2	V
V_{IH}	HIGH-level input voltage		2,0	–	–	V
V_{IL}	LOW-level input voltage		–	–	0,8	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 3.0$ to 3.6 V; $I_O = -100$ µA	$V_{CC} - 0.2$	V_{CC}	–	V
		$V_{CC} = 3.0$ V; $I_O = -32$ mA	2,0	2,3	–	V
V_{OL}	LOW-level output voltage	$V_{CC} = 3.0$ V				
		$I_O = 100$ µA	–	0,07	0,2	V
		$I_O = 16$ mA	–	0,25	0,4	V
		$I_O = 32$ mA	–	0,3	0,5	V
		$I_O = 64$ mA	–	0,4	0,55	V

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
$V_{OL(pu)}$	power-up LOW-level output voltage	$V_{CC} = 3.6$ V; $I_O = 1$ mA; $V_I = V_{CC}$ or GND [1]	–	–	0,55	V
I_I	input leakage current	all input pins;				
		$V_{CC} = 0$ V or 3.6 V; $V_I = 5.5$ V	–	0,1	10	µA
		control pins				
		$V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND	–	0,1	±1	µA
		data pins; [2]				
		$V_{CC} = 3.6$ V; $V_I = V_{CC}$	–	0,5	1	µA
		$V_{CC} = 3.6$ V; $V_I = 0$ V	–	0,1	−5	µA
I_{OFF}	power-off leakage current	$V_{CC} = 0$ V; V_I or $V_O = 0$ to 4.5 V	–	0,1	±100	µA
I_{BHL}	bus hold LOW current	data inputs; $V_{CC} = 3$ V; $V_I = 0.8$ V	75	130	–	µA
I_{BHH}	bus hold HIGH current	data inputs; $V_{CC} = 3$ V; $V_I = 2.0$ V	−75	-140	–	µA
I_{BHLO}	bus hold LOW overdrive current	data inputs; $V_{CC} = 3.6$ V; $V_I = 0$ to 3.6 V [6]	500	–	–	µA
I_{BHHO}	bus hold HIGH overdrive current	data inputs; $V_{CC} = 3.6$ V; $V_I = 0$ to 3.6 V [6]	−500	–	–	µA
I_{EX}	external current	output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5$ V; $V_{CC} = 3.0$ V	–	10	125	µA
$I_{O(pu/pd)}$	power-up/ power-down output current	$V_{CC} \leq 1.2$ V; $V_O = 0.5$ V to V_{CC}; V_I = GND or V_{CC}; $\overline{nOE}$ = don't care [7]	–	1	±100	µA
I_{OZ}	OFF-state output current	$V_{CC} = 3.6$ V; $V_I = V_{IL}$ or V_{IH}				
		output HIGH-state; $V_O = 3.0$ V	–	0,5	5	µA
		output LOW-state; $V_O = 0.5$ V	–	0,5	-5	µA

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A				
		outputs HIGH-state	–	0,07	0,1	mA
		outputs LOW-state	–	5,1	7	mA
		outputs disabled [4]	–	0,07	0,1	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3 to 3.6 V; one input at V_{CC} – 0.6 V; other inputs at V_{CC} or GND [5]	–	0,04	0,4	mA
C_I	input capacitance	V_I = 0 V or V_{CC}	–	3	–	pF
C_O	output capacitance	V_O = 0 V or V_{CC}	–	9	–	pF

* All typical values for V_{CC} = 2.5 V ± 0.2 V are measured at V_{CC} = 2.5 V and T_{amb} = 25 °C.
All typical values for V_{CC} = 3.3 V ± 0.3 V are measured at V_{CC} = 3.3 V and Tamb = 25 °C.
[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
[2] Unused pins at V_{CC} or GND.
[3] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to (2.5 ± 0.2) V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.
[4] I_{CC} with outputs disabled is measured with outputs pulled to V_{CC} or GND.
[5] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
[6] This is the bus hold overdrive current required to force the input to the opposite logic state.
[7] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1,2 V to (3.3 ± 0.3) V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.

Table 35: Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
V_{CC} = 2.5 V ± 0.2 V						
t_{PLH}	LOW to HIGH propagation delay	nCP to nQn	1,0	4,4	7,0	ns
t_{PHL}	HIGH to LOW propagation delay	nCP to nQn	1,0	3,8	6,4	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nQn	1,5	4,6	7,5	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nQn	1,0	2,8	4,6	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nQn	1,5	3,5	5,5	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nQn	1,0	3,7	5,7	ns
t_{su}	set-up time	nDn to nCP HIGH	1,5	0,1	–	ns
		nDn to nCP LOW	2,0	0,5	–	ns
t_h	hold time	nDn to nCP HIGH	0,3	–0,5	–	ns
		nDn to nCP LOW	0,5	–0,1	–	ns
t_W	pulse width	nCP HIGH or LOW	1,5	–	–	ns
f_{max}	maximum frequency	nCP	150	–	–	MHz
V_{CC} = 3.3 V ± 0.3 V						
t_{PLH}	LOW to HIGH propagation delay	nCP to nQn	1,0	3,2	5,0	ns
t_{PHL}	HIGH to LOW propagation delay	nCP to nQn	1,0	3,2	4,7	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nQn	1,0	3,4	5,6	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nQn	0,5	2,3	3,7	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nQn	1,5	3,7	5,4	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nQn	1,5	3,0	4,3	ns
t_{su}	set-up time	nDn to nCP HIGH or LOW	1,5	0,1	–	ns
t_h	hold time HIGH	nDn to nCP HIGH or LOW	0,5	0,1	–	ns
t_W	pulse width	nCP HIGH or LOW	1,5	–	–	ns
f_{max}	maximum frequency	nCP	150	–	–	MHz

* All typical values for V_{CC} = 2.5 V ± 0.2 V are measured at V_{CC} = 2.5 V and T_{amb} = 25 °C.
All typical values for V_{CC} = 3.3 V ± 0.3 V are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

Operating Conditions of LVT

Table 36: Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0,5	+4,6	V
V_I	input voltage	*	−0,5	+7,0	V
V_O	output voltage	output in OFF-state or HIGH-state *	−0,5	+7,0	V
I_{IK}	input clamping current	$V_I < 0$ V	−50	–	mA
I_{OK}	output clamping current	$V_O < 0$ V	−50	–	mA
I_O	output current	output in LOW-state	–	128	mA
		output in HIGH-state	−64	–	mA
T_{stg}	junction temperature		−65	+150	°C
T_j	storage temperature	**	–	+150	°C

* The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

** The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

Table 37: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2,7	–	3,6	V
V_I	input voltage		0	–	5,5	V
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	–	–	10	ns/V
T_{amb}	ambient temperature		−40	–	+85	°C

Table 38: Static characteristics

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			Unit
			Min	Typ*	Max	
V_{IK}	input clamping voltage	$V_{CC} = 2.7$ V; $I_{IK} = -18$ mA	–	−0,85	−1,2	V
V_{IH}	HIGH-level input voltage		2,0	–	–	V
V_{IL}	LOW-level input voltage		–	–	0,8	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 3.0$ V; $I_{OH} = -12$ mA	2,0	–	–	V
V_{OL}	LOW-level output voltage	$V_{CC} = 3.0$ V; $I_{OL} = 12$ mA	–	–	0,8	V
I_{OH}	HIGH-level output current		–	–	−12	mA
I_{OL}	LOW-level output current		–	–	12	mA
$V_{OL(pu)}$	power-up LOW-level output voltage	$V_{CC} = 3.6$ V; $I_O = 1$ mA; V_I = GND or V_{CC} [1]	–	0,1	0,55	V
I_I	input leakage current	all input pins [2]				
		$V_{CC} = 0$ V or 3.6 V; $V_I = 5.5$ V	–	0,4	10	µA
		control pins [2]				
		$V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND	–	0,1	±1	µA
		I/O data pins; $V_{CC} = 3.6$ V [2]				
		$V_I = V_{CC}$	–	0,1	1	µA
		$V_I = 0$ V	–	−0,4	-5	µA
I_{OFF}	power-off leakage current	$V_{CC} = 0$ V; V_I or $V_O = 0$ to 4.5 V	–	0,1	±100	µA
I_{BHL}	bus hold LOW current	nDn inputs; $V_{CC} = 3$ V; $V_I = 0.8$ V	75	135	–	µA
I_{BHH}	bus hold HIGH current	nDn inputs; $V_{CC} = 3$ V; $V_I = 2.0$ V	−75	-135	–	µA
I_{BHLO}	bus hold LOW overdrive current	nDn inputs; $V_{CC} = 3.6$ V; $V_I = 0$ to 3.6 V [3]	500	–	–	µA

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			Unit
			Min	Typ*	Max	
I_{BHHO}	bus hold HIGH overdrive current	nDn inputs; V_{CC} = 3.6 V; V_I = 0 to 3.6 V [3]	–	–	−500	µA
I_{CEX}	output high leakage current	output in HIGH-state when $V_O > V_{CC}$; V_O = 5.5 V; V_{CC} = 3.0 V	–	50	125	µA
$I_{O(pu/pd)}$	power-up/ power-down output current	$V_{CC} \leq 1.2$ V; V_O = 5.0 V to V_{CC}; V_I = GND or V_{CC}; $n\overline{OE}$ = don't care [4]	–	1	±100	µA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; $V_I = V_{IH}$ or V_{IL}				
		V_O = 3.0 V	–	0,5	5	µA
		V_O = 0.5 V	–	0,5	−5	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A				
		outputs HIGH	–	0,07	0,12	mA
		outputs LOW	–	4	6	mA
		outputs disabled [5]	–	0,07	0,12	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3 to 3.6 V; one input at V_{CC} − 0.6 V; other inputs at V_{CC} or GND [6]	–	0,1	0,2	mA
C_I	input capacitance	V_I = 0 V or 3.0 V	–	3	–	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or 3.0 V	–	9	–	pF

* All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
[1] For valid test results, data must not be loaded into the flip-flops after applying power.
[2] Unused pins at V_{CC} or GND.
[3] This is the bus-hold overdrive current required to force the input to the opposite logic state.
[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.
[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.
[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

Table 39: Dynamic characteristics

Symbol	Parameter	Conditions	T_{amb} −40 °C to +85 °C			Unit
			Min	Typ*	Max	
f_{max}	maximum frequency	nCP; V_{CC} = 3.0 to 3.6 V	150	–	–	MHz
t_{PLH}	LOW to HIGH propagation delay	nCP to nQn				
		V_{CC} = 2.7 V	–	–	6,2	ns
		V_{CC} = 3.0 to 3.6 V	1,5	3,0	5,3	ns
t_{PHL}	HIGH to LOW propagation delay	nCP to nQn				
		V_{CC} = 2.7 V	–	–	5,1	ns
		V_{CC} = 3.0 to 3.6 V	1,5	3,0	4,9	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nQn				
		V_{CC} = 2.7 V	–	–	6,9	ns
		V_{CC} = 3.0 to 3.6 V	1,5	3,5	5,6	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nQn				
		V_{CC} = 2.7 V	–	–	6,0	ns
		V_{CC} = 3.0 to 3.6 V	1,5	3,2	4,9	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nQn				
		V_{CC} = 2.7 V	–	–	5,7	ns
		V_{CC} = 3.0 to 3.6 V	1,5	3,5	5,4	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nQn				
		V_{CC} = 2.7 V	–	–	5,1	ns
		V_{CC} = 3.0 to 3.6 V	1,5	3,2	5,0	ns
t_{su}	set-up time	nDn to nCP				
		V_{CC} = 2.7 V	2,0	–	–	ns
		V_{CC} = 3.0 to 3.6 V	2,0	0,7	–	ns
t_h	hold time	nDn to nCP				
		V_{CC} = 2.7 V	0,1	–	–	ns
		V_{CC} = 3.0 to 3.6 V	0,8	0	–	ns
t_{WH}	pulse width HIGH	nCP				
		V_{CC} = 2.7 V	1,5	–	–	ns
		V_{CC} = 3.0 to 3.6 V	1,5	0,6	–	ns
t_{WL}	pulse width LOW	nCP				
		V_{CC} = 2.7 V	3,0	–	–	ns
		V_{CC} = 3.0 to 3.6 V	3,0	1,6	–	ns

* Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

Special Features

Powering-up/Powering-down

LVT and ALVT have a feature that is useful for live insertion and removal. A circuit is built into these families that monitors the supply voltage and ensures that the output is forced to a 3-state mode when V_{CC} is lower than 1.2 V. Then, the transistor does not conduct and the external OE signal is overruled and the output goes into 3-state mode. Normally, when removing a board in a live system, the power supply is removed first and high currents into the output circuit are prevented. Above 1.2 V the transistor will start to conduct and the part may again become active (i.e., the external OE enables the output). It's the task of the system designer to ensure that an external circuit forces the correct OE signal when V_{CC} is higher than 1.2 V.

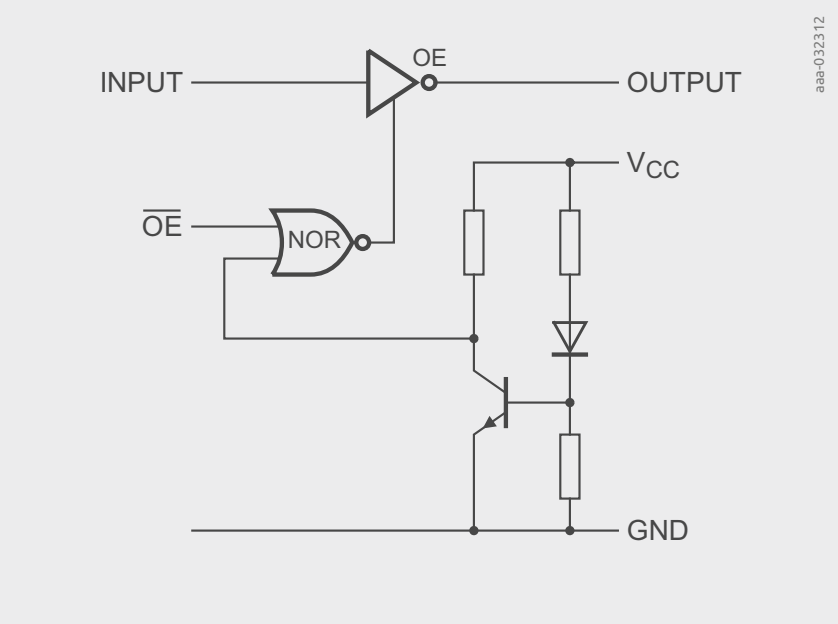


Figure 9.9 | Power-up state

Bus Hold

All ALVT products have integrated bus hold inputs. A bus hold circuit allows CMOS input pins to be left open: the input is always defined to be LOW or HIGH via the small MOS transistors that serve as dynamic pull-up or pull-down resistors. To allow 5 V on the inputs, a Schottky diode is inserted between input and the PMOS transistor, blocking any current V_{CC}, even when the part is powered down.

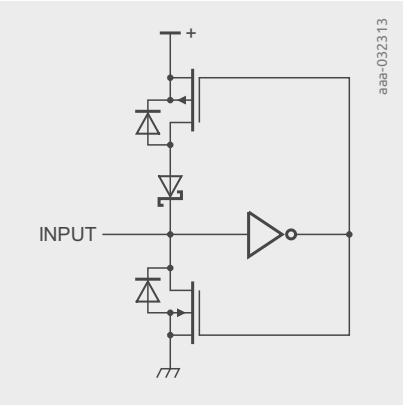


Figure 9.10 | Bus Hold circuit

Summary

Both LVT and ALVT logic families are optimized for use as backplane drivers. These parts combine very fast switching with low power dissipation. The clever design makes them an ideal choice for use in backplanes in high-end EDP and telecom applications. In other areas also where very short propagation delays are a must, both families excel. Added features such as automatic 3-state when the part's output is tied to a higher voltage make them an ideal choice in many mixed mode 3 V–5 V systems.

Chapter 10
FAQ

What is the maximum operating frequency of a logic device?

Datasheets for synchronous logic devices (clock dependent) provide a maximum operating frequency (example 74HC165 is rated at 56 MHz maximum frequency at specific voltage/drive values). Datasheets for asynchronous logic devices (general gates, not clock dependent) do not typically provide this data. In general, logic devices can be clocked to about 100 MHz before capacitive loading of the PCB and external circuitry become the limiting factor. IBIS models are available for most devices which allow simulation at specific user frequencies.

What are the output drive of various logic families?

Nexperia logic devices have output drive capability between 3 mA (HEF-family) and 100 mA (NPIC). See Appendix for complete table of output drive current by family

What is the difference between a Schmitt Trigger and Schmitt Trigger "Action" input?

Schmitt Trigger adds hysteresis to an input signal to reduce the impact of noise that occurs around the transition point. "True" Schmitt triggers will list two switching thresholds in the datasheet for Vt+ (LO-HI transition) and Vt- (HI-LO transition). The Schmitt Trigger feature allows input signals with long transitions times. There is no maximum input transition fall and rise rate to be obeyed ($\Delta t/\Delta V$).

Schmitt Trigger "Action" inputs will have a much smaller hysteresis that is not specified in the datasheet (no Vt+/Vt- listing), a maximum transition fall and rise rate is required for the input signals, like for a standard logic input.

A standard (non-Schmitt or any type) input will have time/volt rise time of 10–20 ns max. A Schmitt trigger "action" input will have a time/volt rise time of 20–100 ns max. A "true" Schmitt trigger device will have an essentially infinite time/volt rise time.

What happens to a logic gate above or below the maximum rated temperature?

Operation of a logic device should be limited to the datasheet rating (Ta = −40°C to +125°C for most devices).

Operation above this rating can exceed the maximum junction temperature (+150°C) and impact lifetime or lead to damage the device. Operation below this rating may cause the device to violate the datasheet specifications for power/voltage/timing (due to temperature-reduced on-state resistance).

What is the operating lifetime of a logic gate?

Operating lifetime is a measure of how long the device will operate in a biased (powered on) condition. Logic devices have no specific design lifetime and with MTBF calculated at 304 billion hours (74AUP1G08GM) gates may operate "forever". Real world applications show that devices powered continually for over 50 years show no sign of degradation.

What is the expected manufacturing EOL of a logic gate?

Nexperia logic devices have extremely long manufacturing lifetimes: some have been in continuous production since the 1970's. For timelines into the future, see our "Longevity" section on the website which lists devices (by package type) which are guaranteed to be in production for at least 10 years. In general: "we will make parts until customers stop buying them"

What is the difference between gold and copper wire bonding?

Historically integrated circuits used gold bond wire between the package leadframe and the die. This was due to the ease of attaching gold wire to the die pads. Recent innovations in copper ultrasonic welding now makes it possible to wire bond with copper. Besides the much lower cost for the wire, copper is actually a better conductor than gold (conductivity of copper = 58 Ωm^{-1} and for gold = 45 Ωm^{-1}).

Are logic functions standardized by part number?

Logic device part numbers from all logic suppliers contain a standard "function part number" following the process family. For example 74LVC08 indicates a logic device in the LVC process family and "08" indicates the function in a "two input AND". See the appendix for list of most common function numbers.

Can I supply a signal voltage to an input/output when V_{CC} = 0 V?

Older logic families may consume excess power and may even "back-drive" the device (leak enough power from the input/output pins to the V_{CC} supply rail to inadvertently energize the logic device). Newer logic families (LVC, AUP, AXP, LV-A etc.) have a feature called "I_{off}" which isolates the output pins from the internal circuits of the logic device when V_{CC} = 0. At the input the over-voltage tolerance feature lets the inputs stay high-ohmic without a supply voltage. In this case there is no diode path from the input to the V_{CC} rail (see input stage schematics in the logic family chapters).

Can I drive an LED directly from a logic gate?

It depends. LEDs consume from a few mA to amps of drive current. Logic families can drive from a few mA to 24 mA (LVC family) or even 100 mA (NPIC family). Always confirm that the output drive of the Logic family is compatible with the drive requirements of the LED.

Can I pull up an open-drain output to higher than V_{CC}?

Consult the datasheet for the Vo specification. For example, the 74HC06 (triple inverter with open-drain outputs) has a V_{CC} rating of 2.0 V–6.0 V and a Vo of 0 V to V_{CC}. However, the 74LVC1G06 (single inverter with open-drain output) has a V_{CC} range of 1.65 V–5.5 V and Vo range of 0 V–5.5 V. The output of the HC cannot exceed V_{CC} but the output of the LVC variant can.

Can I use a gate to drive the V_{CC} of the rest of the circuit? Can it discharge the V_{CC} capacitance?

The output drive capability of the supplying logic gate must always be observed. See the Appendix listing of output drive capability of a logic family. As the receiving logic gate will have a decoupling capacitor V_{CC} to ground, the inrush charging current of the capacitor must be added to the calculation.

Can I use a Nexperia logic device for military or aerospace or life critical applications?

Nexperia logic device datasheets explicitly state "Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk".

What is the most common mode of failure of a logic device?

The primary failure modes of logic gates are EOS (Electrical Over Stress) or ESD (Electro Static Discharge). EOS typically occurs when exceeding the output drive capability of the device, resulting in localized die heating and damage. FA (Failure Analysis) reports will show thermal damage to the die near the output drive transistors. ESD damage occurs when voltage exceeding the ESD protection level of the device (typically 2 kV) enters through an input or output pin and causes vaporization or burn-through of an internal trace (usually not one of the output drivers which are more robust in general)

How do the AUP and AUC logic families compare?

AUP and AUC are both low voltage logic families (AUP V_{CC} range 0.8 V–3.6 V and AUC V_{CC} range 1 V–3.6 V). Propagation delay of the AUC family is faster (1.5 ns versus 3.8 ns for AUP) while the static power consumption of AUP is less (0.5 uA versus 10 uA for the AUC). AUP trades off some performance for lower power consumption.

How can I cross reference from one vendor package to another?

Most logic suppliers adhere to IEEE "SOT" package standards. For example, a SOT-363 will have the same mechanical dimensions across all suppliers. See the Appendix for a listing of the Packaging Codes for the most common industry package types.

How can I cross reference from one vendor process to another?

Logic process families (74HCxx, 74AUP1Gxx, etc.) were created to support a particular microprocessor family in a particular timeframe, therefore all logic suppliers tend to use the same silicon process. Family name is usually the same (HC is same for all suppliers) but some families are not obvious. For a complete list of compatible logic process families, see the Appendix.

How much heat does a part generate? How do I use thermal coefficient values?

Device datasheets provide the P_{tot} (Total Power Dissipation) value, indicating the maximum power (heat) that the package type can dissipate. Thermal Resistance values ($Rth_{(j\text{-}a)}$, $Rth_{(j\text{-}c)}$) are listed on the website (not the datasheet) and provide the thermal resistance from Junction-to-Ambient and Junction-to-Case in degrees Kelvin/Watt. To calculate the exact current consumption (and thus power dissipation) of a device in your specific application, see the Chapter on "Power Considerations"

On dual supply devices, is there a restriction which supply has to be the higher or lower one of the two V_{CC} levels?

Most dual voltage supply devices have no restriction if $V_{CC(A)}$ is the lower or higher supply compared to $V_{CC(B)}$. This can be determined by the relationship of $V_{CC(A)}$ to $V_{CC(B)}$. For example, the 74AVC4T245 datasheet indicates that $V_{CC(A)}$ and $V_{CC(B)}$ are both valid 0.8 V to 3.6 V and thus independent of each other (either can be higher/lower than the other) For optimal system design you establish $V_{CC(A)}$ first if you are presenting signals to the "A" side of the device that references "Pins A and DIR are referenced to $V_{CC(A)}$" (example 74AUP1T45)

What is a packing suffix? Why is it not in the datasheet?

The packing suffix is part of the orderable number and indicates the method in which the devices are shipped. Example 74AUP1G08GM is available with a ,132 suffix (shipped as Reel 7" Q3/T4 orientation) or with a ,115 suffix (shipped as Reel 7" Q1/T1 orientation). Some newer devices may include a single alphanumeric (example "X") in place of this three-digit number. Nexperia chooses not to include this information in the device datasheet as it has no bearing on the electrical characteristics of the device. For a complete listing of Nexperia packing codes, please see the appendix. Note that not all packing methods are available for all devices. Always consult our website for valid part/packing combinations.

What are the modern replacements for historical TTL, LS, S logic devices?

Historic logic families can sometimes be replaced with modern equivalents with certain precautions taken. Most legacy logic families operated at 4.5 V–5.5 V with Tpd Propagation Delay speeds no faster than 10 ns. The biggest difference to today logic devices is the amount of output drive required due to the large fanout requirements: often 16 mA–64 mA. Modern 74HCTxx and 74AHCTxx devices can match V_{CC} requirements and meet/exceed Tpd but output current is limited to 8 mA. Carefully evaluate your actual output drive requirements to determine if 74HCT/74AHCT are viable replacements.

What does the suffix "-Q100" indicate?

The Q100 suffix (example 74AHC1G00GW-Q100) indicates that the logic device has been designed and manufactured to pass Automotive AEC-Q100 Qualification. Q100 devices have tightened process controls including: TS16949 and VDA approved production facilities, flagged as automotive lots, subjected to additional process flow quality gates and stricter rules for lot dispositioning and maverick lot handling. For complete benefits of Q100 Logic, see our Q100 Logic portfolio Brochure

What happens if I exceed the V_{CC} rating?

Exceeding V_{CC} for any period of time will cause higher-than-normal temperatures of the components on the die. Duration of the overvoltage and the amount of overvoltage will determine if there is an impact to the expected lifetime of the device based on increased Arrhenius Activation Energy. All datasheets include V_{CC} specifications under Limiting Values and Recommended Operating Conditions. V_{CC} operation under the wider Limiting Values will not affect device lifetime but may cause voltage/timing values in the datasheet to be exceeded. Always design for Recommended Operating Conditions

The AXP family only shows V_{il}/V_{ih} values for certain ranges of V_{CC}. What if I want to operate between those ranges?

As seen in the following graph, values of V_{il}/V_{ih} are only provided for certain values of V_{CC}. The discontinuities between voltage ranges can be linearly approximated

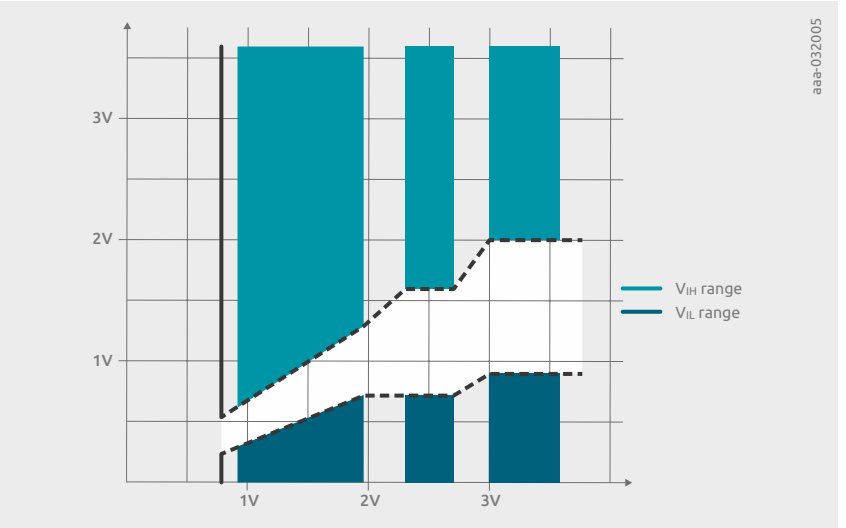


Figure 10.1 | Input voltage ranges of the logic family AUP dependent on V_{CC}

What is a Date Code and how do I read it? What do the top markings mean?

The size of the logic package determines the amount/type of data printed. For large packages (greater than 10 pins) there will be three lines of information. Line 1 contains the device part number. It may be concatenated for long part numbers (ex: 74AVC8T245 will concatenate to AVC8T245). Line 2 contains the Manufacturing Lot number (an internal number but useful for tracing batches for Failure Analysis). Line 3 contains the Manufacturing locations (Diffusion/Assembly/Test) and the Date Code (format Year/week number). There may or may not be a Nexperia logo on the device: in some cases the older NXP logo will remain. For more details, see the Appendix.

For smaller devices (8 pins and smaller) special coding is used due to space limitations. The device part number will be represented by a 3-digit alphanumeric code (this code is included in the datasheet). The date code is written in binary on the edges of the package: left side contains the Last Digit of Year (ie 0110 = 6 = 2016), right side contains Month Number Code (ex: 0001 = January). See the Appendix for details

What is MSL and what does it have to do with package storage?

MSL (Moisture Sensitivity Level) indicates the devices proclivity to absorbing humidity from the ambient environment. Absorbed humidity can cause issues during reflow and wave soldering operations ("popcorn" delamination of packages due to escape of trapped steam). Most Nexperia devices are MSL = 1 which indicates an unlimited floor life out of the shipping bag (no effect to humidity). MSL data is available for each device on our website.

What is MTBF and what does it tell me about the lifetime of a part? How does it compare to FIT?

MTBF (Mean Time Between Failures) is a predicted elapsed time between inherent failures of the logic device. It is inversely related to IFR measure in FITs.

Intrinsic Failure Rate (IFR)

The "plateau" of the failure rate curve consists of random failures, and the failure rate is relatively low and constant. This is the best behaviour observed in large populations of mature components, and is commonly referred to as the "useful life" of the product. The Intrinsic Failure Rate (IFR) is usually defined by the Failure-In-Time (FIT); one FIT being one failure in 1 billion device hours of operation.

The formula used to calculate the Intrinsic Failure Rate, expressed in FIT's, is as follows:

$$IFR = \frac{n_C(n)}{N \cdot t \cdot A} \cdot 10^9 \text{ [FIT]}$$

Where

IFR = Intrinsic Failure Rate in *FIT*
n = Observed number of failures (excluding early failures!)
$n_c(n)$ = Corrected number of failures, using 60% confidence intervals with Poisson statistics
N = Number of products tested
t = Duration of test at elevated temperature, in hours
A = Arrhenius acceleration factor energy (E_A = 0.7 eV, Tref = 55 °C)

Throughout this Quality Summary, the Arrhenius acceleration factor is calculated with an activation energy (E_A) of 0.7 eV and a reference temperature of 55°C. As in the case for the Early Failure Rate determination, the IFR calculations are based on the data collected from SHTL and DHTL tests (stresses with electrical bias at elevated temperature), and all FIT data are calculated by accumulating the applicable results over a period of 12 months.

Mean Time Between Failures (MTBF)

$$MTBF = \frac{1}{IFR \cdot 10^{-9}} \text{ [hours]}$$

Where

MTBF = Mean Time Between Failures in *hours*
IFR = Intrinsic Failure Rate in FIT

What is RoHS, REACH and Green and Dark Green mean?

These terms all indicate the compliance of the device to various environmental standards, EU RoHS Compliant, EU/CN RoHS Compliance, Halogen-Free, Lead-Free. Etc.

For a complete listing, see our website at
www.nexperia.com/quality/environmental-indicators

What is the purpose of the center pad DQFN "BQ"-suffix packages

The center pad on the BQ package (example 74AVC2T245BQ SOT763-1) was originally designed as heat pad for high power devices (Class D amplifiers. etc.). As logic devices have low power dissipation, this heat pad is no longer required but remains for package compatibility. Please note that the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered the solder land should remain floating or be connected to GND or V_{CC} as indicated by the datasheet. Most devices allow connection to GND but select devices (ex. 74HC4051BQ) should connect only to V_{CC}.

What is the difference between 74HC and 74HCT families? (also 74AHC and 74AHCT)

The "T" in each of these indicates the family has been optimized for "TTL" input voltage levels. While both families can operate at TTL supply levels V_{CC} = 4.5–5.5 V (HC family can operate 2.0–6.0 V), the HCT family inputs are matched to legacy TTL signal levels (V_{il} = 1.2 V, V_{ih} = 1.6 V) compared to HC (V_{ll} = 2.1, V_{ih} = 2.4 V) at the same V_{CC}. Output drive for the two families is identical. HCT family has slightly slower propagation delay tpd. Because of the similarities, these two device families will share the same datasheet (ex: 74HC00 and 74HCT00)

What is the difference between A and non-A devices?

An "A" suffix on a logic device (example 74LVC14A) indicates that the device has been redesigned, impacting one or more specifications from the original specification. The "A" suffix has a special meaning when used with the LV family, example indicating that the "A" version has the iOff feature (input/outputs are isolated when V_{CC} = 0). You should carefully evaluate any changes from the "non-A" to the "A" version before replacing it

What should I do with pins I don't need on a device?

Unused input pins on all logic device must always be connected to V_{CC} or GND. Unconnected input pins will float due to intrinsic leakage paths on the die. As the signal voltage crosses a transition level (V_{il}, V_{ih}), the device will switch outputs, causing a brief slump on the power supply rail. This slump in V_{CC} can cause the V_i, V_{ih} levels to change, causing the device to switch output states back again. This creates an oscillation loop, resulting in high current consumption, possibly causing catastrophic damage to the device. Unused output-only pins can be left unterminated safely.

Why do some buffers have termination resistors in them?

Certain devices such as the 74LVC2245 have termination resistors in each of the output driver lines. This resistor is added for impedance matching into 50 ohm cables to reduce overshoot and undershoot. The second "2" in the part number differentiates this device from the standard output (no terminal resistor) 74LVC245 device

Why do the 74LVC2G74/1G74 have different part numbers but same function? Both are single gate but the part number indicates one has two gates included

Nexperia (then Philips/NXP) created the original device 74LVC1G74 (single D-type flip-flop). A competitor released a functional equivalent later but named it the 74LVC2G74. The exact reason is unknown: either a simple mistake or an ingenious method to create an apparent sole-source part number. To clear this confusion, Nexperia now provides the same silicon under either part number, 74LVC1G74 and 74LVC2G74: one to match the original name and one to match the competition name. There is no electrical difference between these two devices and they are in fact the same silicon, package and top marking. We apologize for any confusion this caused but we didn't start it!

Why is the drive current of a device important? How does it relate to Vol and Voh?

Each logic family has a maximum output drive capability. As the output load increases, V_{OH} voltage levels fall respectively V_{OL} levels rise due to loading of the output stage. Past the maximum rated output drive of the family (example 74HC00 8 mA) V_{OL}/V_{OH} no longer meet standard TTL/LVTTL voltage levels. The maximum I_{CC} supply current (found in Limiting Values of the datasheet) should not be used as maximum output drive capability.

Is it allowed to operate a device below the absolute V_{CC} limit rating but outside the recommended operating conditions?

Lifetime testing has been performed for Recommended Values only. Operating above these limits can lead to reduced lifetime. Also note that Static and Dynamic parameters listed in the datasheet may not be accurate outside of Recommended Values.

Why are the outputs of logic devices with flipflops not cleared after power-on?

Devices from standard logic families have no dedicated power-on circuitry that puts the flip-flops into a default condition after V_{CC} has been ramped up. For devices that have a reset pin, a reset cycle can be applied immediately after power is up. For this it needs to be mentioned that it is not allowed to connect a low active reset pin to V_{CC} directly. This approach does not work because the timing conditions for a proper reset action are not fulfilled. In Fig.xx a simple solution is depicted. A low pass filter is applied to the $\overline{MR}$ pin. The capacitor is charged from V_{CC} by the resistor R and keeps low level for some time until V_{CC} has reached minimum voltage for proper operation and additional hold time has to be provided for the reset signal.

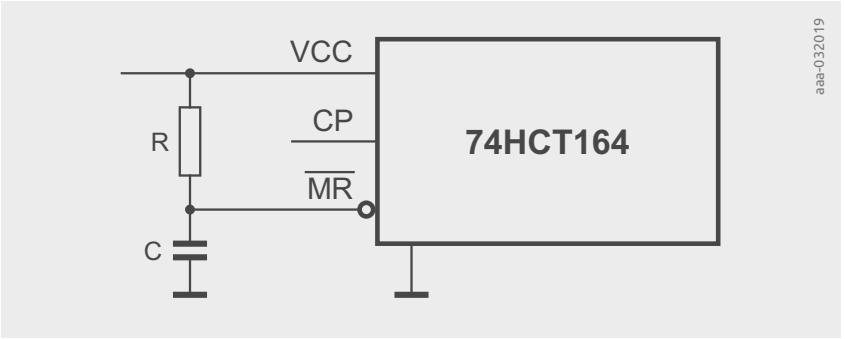


Figure 10.2 | Simple power-on reset generation for low-active reset pins

Top 10 Design Errors with Logic

- Violating Vin/Vout levels
- Violating setup/hold times in flip flops and latched inputs
- Un-terminated/floating inputs
- No decoupling capacitor
- Exceeding output drive capability (damage or low voltage levels)
- Exceeding Fmax
- Violating rise/fall times (and solutions)
- Operation outside of temperature range
- Understanding power calculations
- Understanding translation methodologies, (single/dual supply, selecting single V_{CC})

Appendix

List of Common 7400 and 4000 Logic Functions

Typical nomenclature: 74HCxx or HEF4xxx

Function Number	Boolean Function
-00	Quad 2-input NAND gate
-01	Quad 2-input NAND gate with open collector outputs
-02	Quad 2-input NOR gate
-03	Quad 2-input NAND gate with open collector outputs (different pinout than 7401)
-04	Hex Inverter
-05	Hex Inverter with open collector outputs
-06	Hex Inverter Buffer/Driver with 30V open collector outputs
-07	Hex Buffer/Driver with 30V open collector outputs
-08	Quad 2-input AND gate
-09	Quad 2-input AND gate with open collector outputs
-10	Triple 3-input NAND gate
-11	Triple 3-input AND gate
-12	Triple 3-input NAND gate with open collector outputs
-13	Dual Schmitt trigger 4-input NAND gate
-14	Hex Schmitt trigger Inverter
-15	Triple 3-input AND gate with open collector outputs
-16	Hex Inverter Buffer/Driver with 15V open collector outputs
-17	Hex Buffer/Driver with 15V open collector outputs
-18	Dual 4-input NAND gate with schmitt trigger inputs
-19	Hex Schmitt trigger Inverter
-20	Dual 4-input NAND gate
-21	Dual 4-input AND gate
-22	Dual 4-Input NAND gate with open collector outputs
-23	Expandable Dual 4-input NOR gate with strobe

Function Number	Boolean Function
-24	Quad 2-input NAND gate gates with Schmitt-trigger line-receiver inputs.
-25	Dual 4-input NOR gate with Strobe
-26	Quad 2-input NAND gate with 15V open collector outputs
-27	Triple 3-input NOR gate
-28	Quad 2-input NOR Buffer
-30	8-input NAND gate
-31	Hex Delay Elements
-32	Quad 2-input OR gate
-33	Quad 2-input NOR Buffer with open collector outputs
-34	Low-power dual supply translating buffer
-36	Quad 2-input NOR Gate (different pinout than -02)
-37	Quad 2-input NAND Buffer
-38	Quad 2-input NAND Buffer with open collector outputs
-39	Quad 2-input NAND Buffer
-40	Dual 4-input NAND Buffer
-41	Binary-coded decimal to Decimal Decoder/Nixie tube Driver
-42	BCD to Decimal Decoder
-43	Excess-3 to Decimal Decoder
-44	Excess-3-Gray code to Decimal Decoder
-45	BCD to Decimal Decoder/Driver
-46	BCD to Seven-segment display Decoder/Driver with 30V open collector outputs
-47	BCD to 7-segment Decoder/Driver with 15V open collector outputs
-48	BCD to 7-segment Decoder/Driver with Internal Pullups
-49	BCD to 7-segment Decoder/Driver with open collector outputs
-50	Dual 2-Wide 2-input AND-OR-Invert Gate (one gate expandable)

Function Number	Boolean Function
-51	Dual 2-Wide 2-Input AND-OR-Invert Gate
-52	Expandable 4-Wide 2-input AND-OR Gate
-53	Expandable 4-Wide 2-input AND-OR-Invert Gate
-54	4-Wide 2-Input AND-OR-Invert Gate
-55	2-Wide 4-Input AND-OR-Invert Gate (-H version is expandable)
-56	50:1 Frequency divider
-57	60:1 Frequency divider
-58	2-Input & 3-Input AND-OR Gate
-59	2-Input & 3-Input AND-OR-Invert Gate
-60	Dual 4-input Expander
-61	Triple 3-input Expander
-62	3-2-2-3-Input AND-OR Expander
-63	Hex Current Sensing Interface Gates
-64	4-2-3-2-Input AND-OR-Invert Gate
-65	4-2-3-2-Input AND-OR-Invert Gate with open collector output
-66	Single-pole single-throw analog switch
-67	16-channel analog multiplexer/ demultiplexer
-68	Dual 4 Bit Decade Counters
-69	Dual 4 Bit Binary Counters
-70	AND-Gated Positive Edge Triggered J-K Flip-Flop with Preset and Clear
-71	AND-OR-Gated J-K Master-Slave Flip-Flop with Preset or AND-Gated R-S Master-Slave Flip-Flop with Preset and Clear
-72	AND Gated J-K Master-Slave Flip-Flop with Preset and Clear
-73	Dual J-K Flip-Flop with Clear
-74	Dual D Positive Edge Triggered Flip-Flop with Preset and Clear
-75	4-bit Bistable Latch
-76	Dual J-K Flip-Flop with Preset and Clear
-77	4-bit Bistable Latch

Function Number	Boolean Function
-78	Dual J-K Flip-Flop with Preset, Common Clear, and Common Clock or Dual Negative Edge Triggered J-K Flip-Flop with Preset, Common Clear, and Common Clock
-79	Dual D Flip-Flop
-80	Gated Full Adder
-81	16-bit Random Access Memory
-82	2-bit Binary Full Adder
-83	4-bit Binary Full Adder
-84	16-bit Random Access Memory
-85	4-bit Magnitude Comparator
-86	Quad 2-input XOR gate
-87	4-bit True/Complement/Zero/One Element
-88	256-bit Read-only memory
-89	64-bit Random Access Memory
-90	Decade Counter (separate Divide-by-2 and Divide-by-5 sections)
-91	8-bit Shift Register, Serial In, Serial Out, Gated Input
-92	Divide-by-12 Counter (separate Divide-by-2 and Divide-by-6 sections)
-93	4-bit Binary Counter (separate Divide-by-2 and Divide-by-8 sections)
-94	4-bit Shift register, Dual Asynchro-nous Presets
-95	4-bit Shift register, Parallel In, Parallel Out, Serial Input
-96	5-bit Parallel-In/Parallel-Out Shift register, Asynchronous Preset
-97	Synchronous 6-bit Binary Rate Multiplier
-98	4-bit Data Selector/Storage Register
-99	4-bit Bidirectional Universal Shift register
-100	Dual 4-Bit Bistable Latch
-101	AND-OR-Gated J-K Negative-Ed-ge-Triggered Flip-Flop with Preset
-102	AND-Gated J-K Negative-Edge-Trig-gered Flip-Flop with Preset and Clear
-103	Dual J-K Negative-Edge-Triggered Flip-Flop with Clear

Function Number	Boolean Function
-104	J-K Master-Slave Flip-Flop
-105	J-K Master-Slave Flip-Flop
-106	Dual J-K Negative-Edge-Triggered Flip-Flop with Preset and Clear
-107	Dual J-K Flip-Flop with Clear or Dual J-K Negative-Edge-Triggered Flip-Flop with Clear
-108	Dual J-K Negative-Edge-Triggered Flip-Flop with Preset, Common Clear, and Common Clock
-109	Dual J-Not-K Positive-Edge-Triggered Flip-Flop with Clear and Preset
-110	AND-Gated J-K Master-Slave Flip-Flop with Data Lockout
-111	Dual J-K Master-Slave Flip-Flop with Data Lockout
-112	Dual J-K Negative-Edge-Triggered Flip-Flop with Clear and Preset
-113	Dual J-K Negative-Edge-Triggered Flip-Flop with Preset
-114	Dual J-K Negative-Edge-Triggered Flip-Flop with Preset, Common Clock and Clear
-116	Dual 4-bit Latches with Clear
-118	Hex Set/Reset Latch
-119	Hex Set/Reset Latch
-120	Dual Pulse Synchronizer/Drivers
-121	Monostable Multivibrator
-122	Retriggerable Monostable Multivibrator with Clear
-123	Dual Retriggerable Monostable Multivibrator with Clear
-124	Dual Voltage-Controlled Oscillator
-125	Quad Bus Buffer with Three-State Outputs, Negative Enable
-126	Quad Bus Buffer with Three-state Outputs, Positive Enable
-128	Quad 2-input NOR Line Driver
-130	Quad 2-input AND gate Buffer with 30V open collector outputs
-131	Quad 2-input AND gate Buffer with 15V open collector outputs
-132	Quad 2-input NAND Schmitt trigger

Function Number	Boolean Function
-133	13-Input NAND gate
-134	12-Input NAND gate with Three-state Output
-135	Quad Exclusive-OR/NOR Gate
-136	Quad 2-Input XOR gate with open collector outputs
-137	3 to 8-line Decoder/Demultiplexer with Address Latch
-138	3 to 8-line Decoder/Demultiplexer
-139	Dual 2 to 4-line Decoder/Demultiple-xer
-140	Dual 4-input NAND Line Driver
-141	BCD to Decimal Decoder/Driver for cold-cathode indicator/NIXIE Tube
-142	Decade Counter/Latch/Decoder/ Driver for Nixie Tubes
-143	Decade Counter/Latch/De-coder/7-segment Driver, 15 mA Constant Current
-144	Decade Counter/Latch/De-coder/7-segment Driver, 15V open collector outputs
-145	BCD to Decimal Decoder/Driver
-147	10-Line to 4-Line Priority Encoder
-148	8-Line to 3-Line Priority Encoder
-150	16-Line to 1-Line Data Selector/ Multiplexer
-151	8-Line to 1-Line Data Selector/ Multiplexer
-152	8-Line to 1-Line Data Selector/ Multiplexer
-153	Dual 4-Line to 1-Line Data Selector/ Multiplexer
-154	4-Line to 16-Line Decoder/ Demultiplexer
-155	Dual 2-Line to 4-Line Decoder/ Demultiplexer
-156	Dual 2-Line to 4-Line Decoder/ Demultiplexer with open collector outputs
-157	Quad 2-Line to 1-Line Data Selector/ Multiplexer, Noninverting
-158	Quad 2-Line to 1-Line Data Selector/ Multiplexer, Inverting

Function Number	Boolean Function
-159	4-Line to 16-Line Decoder/ Demultiplexer with open collector outputs
-160	Synchronous 4-bit Decade Counter with Asynchronous Clear
-161	Synchronous 4-bit Binary Counter with Asynchronous Clear
-162	Synchronous 4-bit Decade Counter with Synchronous Clear
-163	Synchronous 4-bit Binary Counter with Synchronous Clear
-164	8-bit Parallel-Out Serial Shift Register with Asynchronous Clear
-165	8-bit Serial Shift Register, Parallel Load, Complementary Outputs
-166	Parallel-Load 8-Bit Shift Register
-167	Synchronous Decade Rate Multiplier
-168	Synchronous 4-Bit Up/Down Decade Counter
-169	Synchronous 4-Bit Up/Down Binary Counter
-170	4 by 4 Register File with open collector outputs
-171	16-Bit Multiple Port Register File with Three-state Outputs
-173	Quad D-type flip-flop; positive-edge trigger; 3-state
-174	Hex D-type flip-flop with reset; positi-ve-edge trigger
-175	Quad D-type flip-flop with reset; positive-edge trigger
-191	Presettable synchronous 4-bit binary up/down counter
-193	Presettable synchronous 4-bit binary up/down counter
-194	4-bit bidirectional universal shift register
-200	256-bit RAM with Three-state Outputs
-201	256-bit (256x1) RAM with three-state outputs
-206	256-bit RAM with open collector outputs

Function Number	Boolean Function
-209	1024-bit (1024x1) RAM with three-state output
-210	Octal Buffer
-219	64-bit (16x4) RAM with Noninverting three-state outputs
-221	Dual Monostable Multivibrator with Schmitt trigger input
-222	16 by 4 Synchronous FIFO Memory with three-state outputs
-224	16 by 4 Synchronous FIFO Memory with three-state outputs
-225	Asynchronous 16x5 FIFO Memory
-226	4-bit Parallel Latched Bus Transceiver with three-state outputs
-230	Octal Buffer/Driver with three-state outputs
-232	Quad NOR Schmitt trigger
-237	1-of-8 Decoder/Demultiplexer with Address Latch, Active High Outputs
-238	1-of-8 Decoder/Demultiplexer, Active High Outputs
-239	Dual 2-of-4 Decoder/Demultiplexer, Active High Outputs
-240	Octal Buffer with Inverted three-state outputs
-241	Octal Buffer with Noninverted three-state outputs
-242	Quad Bus Transceiver with Inverted three-state outputs
-243	Quad Bus Transceiver with Noninverted three-state outputs
-244	Octal Buffer with Noninverted three-state outputs
-245	Octal Bus Transceiver with Noninverted three-state outputs
-246	BCD to 7-segment Decoder/Driver with 30V open collector outputs
-247	BCD to 7-segment Decoder/Driver with 15V open collector outputs
-248	BCD to 7-segment Decoder/Driver with Internal Pull-up Outputs
-249	BCD to 7-segment Decoder/Driver with open collector outputs

Function Number	Boolean Function
-251	8-line to 1-line Data Selector/ Multiplexer with complementary three-state outputs
-253	Dual 4-line to 1-line Data Selector/ Multiplexer with three-state outputs
-255	Dual 4-bit Addressable Latch
-256	Dual 4-bit Addressable Latch
-257	Quad 2-line to 1-line Data Selector/ Multiplexer with Noninverted three-state outputs
-258	Quad 2-line to 1-line Data Selector/ Multiplexer with Inverted three-state outputs
-259	8-bit Addressable Latch
-260	Dual 5-Input NOR Gate
-261	2-bit by 4-bit Parallel Binary Multiplier
-265	Quad Complementary Output Elements
-266	Quad 2-Input XNOR gate with open collectorOutputs
-269	8-bit bidirectional binary counter
-270	2048-bit (512x4) Read Only Memory with open collector outputs
-271	2048-bit (256x8) Read Only Memory with open collector outputs
-273	8-bit Register with Reset
-274	4-bit by 4-bit Binary Multiplier
-275	7-bit Slice Wallace tree
-276	Quad J-Not-K Edge-Triggered Flip-Flops with Separate Clocks, Common Preset and Clear
-278	4-bit Cascadeable Priority Registers with Latched Data Inputs
-279	Quad Set-Reset Latch
-280	9-bit Odd/Even Parity bit Generator/ Checker
-281	4-bit Parallel Binary Accumulator
-283	4-bit Binary Full adder
-284	4-bit by 4-bit Parallel Binary Multiplier (low order 4 bits of product)

Function Number	Boolean Function
-285	4-bit by 4-bit Parallel Binary Multiplier (high order 4 bits of product)
-287	1024-bit (256x4) Programmable read-only memory with three-state outputs
-288	256-bit (32x8) Programmable read-only memory with three-state outputs
-289	64-bit (16x4) RAM with open collector outputs
-290	Decade Counter (separate divide-by-2 and divide-by-5 sections)
-291	4-bit Universal Shift register, Binary Up/Down Counter, Synchronous
-292	Programmable Frequency Divider/ Digital Timer
-293	4-bit Binary Counter (separate divide-by-2 and divide-by-8 sections)
-294	Programmable Frequency Divider/ Digital Timer
-295	4-Bit Bidirectional Register with Three-state outputs
-297	Digital Phase-Locked-Loop Filter
-298	Quad 2-Input Multiplexer with Storage
-299	8-Bit Bidirectional Universal Shift/ Storage Register with three-state outputs
-301	256-bit (256x1) Random access memory with open collector output
-309	1024-bit (1024x1) Random access memory with open collector output
-310	Octal Buffer with Schmitt trigger inputs
-314	1024-bit random access memory
-320	Crystal controlled oscillator
-322	8-bit Shift register with Sign Extend, three-state outputs
-323	8-bit Bidirectional Universal Shift/ Storage Register with three-state outputs
-324	Voltage Controlled Oscillator (or Crystal Controlled)
-332	3-input OR-gate

Function Number	Boolean Function
-340	Octal Buffer with Schmitt trigger inputs and three-state inverted outputs
-341	Octal Buffer with Schmitt trigger inputs and three-state noninverted outputs
-344	Octal Buffer with Schmitt trigger inputs and three-state noninverted outputs
-348	8 to 3-line Priority Encoder with three-state outputs
-350	4-bit Shifter with three-state outputs
-351	Dual 8-line to 1-line Data Selectors/ Multiplexers with three-state outputs and 4 Common Data Inputs
-352	Dual 4-line to 1-line Data Selectors/ Multiplexers with Inverting Outputs
-353	Dual 4-line to 1-line Data Selectors/ Multiplexers with Inverting three-state outputs
-354	8 to 1-line Data Selector/Multiplexer with Transparent Latch, three-state outputs
-356	8 to 1-line Data Selector/Multiplexer with Edge-Triggered Register, three-state outputs
-361	Bubble memory function timing generator
-362	Four-Phase Clock Generator/Driver (aka TIM9904)
-365	Hex Buffer with Noninverted three-state outputs
-366	Hex Buffer with Inverted three-state outputs
-367	Hex Buffer with Noninverted three-state outputs
-368	Hex Buffer with Inverted three-state outputs
-370	2048-bit (512x4) Read-only memory with three-state outputs
-371	2048-bit (256x8) Read-only memory with three-state outputs
-373	Octal Transparent Latch with three-state outputs
-374	Octal Register with three-state outputs

Function Number	Boolean Function
-375	Quad Bistable Latch
-376	Quad J-Not-K Flip-flop with Common Clock and Common Clear
-377	8-bit Register with Clock Enable
-378	6-bit Register with Clock Enable
-379	4-bit Register with Clock Enable and Complementary Outputs
-380	8-bit Multifunction Register
-381	4-bit Arithmetic Logic Unit/Function Generator with Generate and Propagate Outputs
-382	4-bit Arithmetic Logic Unit/Function Generator with Ripple Carry and Overflow Outputs
-384	Bilateral switch
-385	Quad 4-bit Adder/Subtractor
-386	Quad 2-Input XOR gate
-387	1024-bit (256x4) Programmable read-only memory with open collector outputs
-388	4-bit Register with Standard and Three-state Outputs (-LS388 is equivalent to AMD Am25LS2518 , functional equivalent to Am2918 and Am25S18)
-390	Dual 4-bit Decade Counter
-393	Dual 4-bit Binary Counter
-395	4-bit Universal Shift register with three-state outputs
-398	Quad 2-input Multiplexers with Storage and Complementary Outputs
-399	Quad 2-input Multiplexer with Storage
-408	8-bit Parity Tree
-412	Multi-Mode Buffered 8-bit Latches with three-state outputs and Clear (74S412 is equivalent to Intel 8212, TI TIM8212)
-423	Dual Retriggerable Monostable Multivibrator
-424	Two-Phase Clock Generator/Driver (74LS424 is equivalent to Intel 8224, TI TIM8224)

Function Number	Boolean Function
-425	Quad Gates with three-state outputs and Active Low Enables
-426	Quad Gates with three-state outputs and Active High Enables
-428	System Controller for 8080A (74S428 is equivalent to Intel 8228, TI TIM8228)
-438	System Controller for 8080A (74S438 is equivalent to Intel 8238, TI TIM8238)
-440	Quad Tridirectional Bus Transceiver with Noninverted open collector outputs
-441	Quad Tridirectional Bus Transceiver with Inverted open collector outputs
-442	Quad Tridirectional Bus Transceiver with Noninverted three-state outputs
-443	Quad Tridirectional Bus Transceiver with Inverted three-state outputs
-444	Quad Tridirectional Bus Transceiver with Inverted and Noninverted three-state outputs
-448	Quad Tridirectional Bus Transceiver with Inverted and Noninverted open collector outputs
-450	16-to-1 Multiplexer with Complementary Outputs
-451	Dual 8-to-1 Multiplexer
-452	Dual Decade Counter, Synchronous
-453	Dual Binary Counter, Synchronous (Motorola, "plain" TTL)
-453	Quad 4-to-1 Multiplexer
-454	Dual Decade Up/Down Counter, Synchronous, Preset Input
-455	Dual Binary Up/Down Counter, Synchronous, Preset Input
-456	NBCD (Natural Binary Coded Decimal) Adder
-460	Bus Transfer Switch
-461	8-bit Presettable Binary Counter with three-state outputs
-462	Fiber-Optic Link Transmitter
-463	Fiber-Optic Link Receiver

Function Number	Boolean Function
-465	Octal Buffer with three-state outputs
-468	Dual MOS-to-TTL Level Converter
-470	2048-bit (256x8) Programmable read-only memory with open collector outputs
-471	2048-bit (256x8) Programmable read-only memory with three-state outputs
-472	Programmable read-only memory with open collector outputs
-473	Quad D Flip-Flop with Three-state Outputs
-473	Programmable read-only memory with three-state outputs
-474	Hex D Flip-Flop with Common Clear
-474	Programmable read-only memory with open collector outputs
-475	Quad D Edge-Triggered Flip-Flop with Complementary Outputs and Asynchronous Clear
-475	Programmable read-only memory with three-state outputs
-476	Presettable Decade (Bi-Quinary) Counter/Latch
-477	Presettable Binary Counter/Latch
-478	4-bit Parallel-Access Shift Register
-479	4-bit Parallel-Access Shift Register with Asynchronous Clear and Complementary QD Outputs
-480	9-bit Odd/Even Parity bit Generator and Checker
-481	4-bit Arithmetic Logic Unit and Function Generator
-481	4-bit Slice Processor Elements
-482	Lookahead Carry Generator
-482	4-bit Slice Expandable Control Elements
-483	Dual Carry-Save Full adder
-484	BCD to Binary Converter
-484	BCD-to-Binary Converter (mask programmed SN74S371 ROM)
-485	Binary to BCD Converter
-485	Binary-to-BCD Converter (mask programmed SN74S371 ROM)

Function Number	Boolean Function
-486	512-bit (64x8) Read-only memory with open collector outputs
-487	1024-bit (256x4) Read only memory with open collector outputs
-488	256-bit (32x8) Programmable read-only memory with open collector outputs
-489	64-bit (16x4) RAM with Inverting three-state Outputs
-490	Synchronous Up/Down Decade Counter
-490	Dual Decade Counter
-491	Synchronous Up/Down Binary Counter
-491	10-bit Binary Up/Down Counter with Limited Preset and three-state logic outputs
-492	Synchronous Up/Down Decade Counter with Clear
-493	Synchronous Up/Down Binary Counter with Clear
-494	4-bit Bidirectional Universal Shift Register
-495	4-bit Parallel-Access Shift Register
-496	Presettable Decade Counter/Latch
-497	Presettable Binary Counter/Latch
-498	8-bit Bidirectional Universal Shift Register
-498	8-bit Bidirectional Shift Register with Parallel Inputs and three-state outputs
-499	8-bit Bidirectional Universal Shift Register with J-Not-K Serial Inputs
-508	8-bit Multiplier/Divider
-511	BCD to 7-segment latch/decoder/driver
-514	4-to-16 line decoder/demultiplexer with input latches
-516	Binary up/down counter
-517	Dual 64-bit static shift register
-518	Dual BCD counter
-520	8-bit Comparator - as -521 but with different input circuit
-521	8-bit Comparator

Function Number	Boolean Function
-526	Fuse Programmable Identity Comparator, 16 Bit
-527	Fuse Programmable Identity Comparator, 8 Bit + 4 Bit conventional Identity Comparator
-528	Fuse Programmable Identity Comparator, 12 Bit
-531	Octal Transparent Latch with 32 mA three-state outputs
-532	Octal Register with 32 mA three-state outputs
-533	Octal Transparent Latch with Inverting Three-state logic outputs
-534	Octal Register with Inverting three-state outputs
-535	Octal Transparent Latch with Inverting three-state outputs
-536	Octal Register with Inverting 32 mA three-state outputs
-537	BCD to Decimal Decoder with three-state outputs
-538	1 of 8 Decoder with three-state outputs
-539	Dual 1 of 4 Decoder with three-state outputs
-540	Inverting Octal Buffer with three-state outputs
-541	Non-inverting Octal Buffer with three-state outputs
-543	Octal latched transceiver with dual enable; 3-state
-544	Octal D-type registered transceiver; inverting; 3-state
-555	1-of-4 decoder/demultiplexer
-557	1-to-64 bit variable length shift register
-558	8-Bit by 8-Bit Multiplier with three-state outputs
-560	4-bit Decade Counter with three-state outputs
-561	4-bit Binary Counter with three-state outputs
-563	8-bit D-Type Transparent Latch with Inverting three-state outputs

Function Number	Boolean Function
-564	8-bit D-Type Edge-Triggered Register with Inverting three-state outputs
-568	Decade Up/Down Counter with three-state outputs
-569	Binary Up/Down Counter with three-state outputs
-573	Octal D-Type Transparent Latch with three-state outputs
-574	Octal D-Type Edge-Triggered Flip-flop with three-state outputs
-575	Octal D-Type Flip-Flop with Synchronous Clear, three-state outputs
-576	Octal D-Type Flip-Flop with inverting three-state outputs
-577	Octal D-Type Flip-Flop with Synchronous Clear, inverting three-state outputs
-580	Octal Transceiver/Latch with inverting three-state outputs
-585	4-bit magnitude comparator
-589	8-bit Shift Register with Input Latch, three-state outputs
-590	8-Bit Binary Counter with Output Registers and three-state outputs
-592	Binary Counter with Input Registers
-593	8-Bit Binary Counter with Input Registers and three-state outputs
-594	Serial-in Shift register with Output Registers
-595	Serial-in Shift register with Output Latches
-596	Serial-in Shift register with Output Registers and open collector outputs
-597	Serial-out Shift register with Input Latches
-598	Shift register with Input latches
-600	Dynamic Memory Refresh Controller, Transparent and Burst Modes, for 4K or 16K DRAMs (74LS600 is equivalent to TI TIM99600)
-601	Dynamic Memory Refresh Controller, Transparent and Burst Modes, for 64K DRAMs (-LS601 is equivalent to TI TIM99601)

Function Number	Boolean Function
-602	Dynamic Memory Refresh Controller, Cycle Steal and Burst Modes, for 4K or 16K DRAMs (74LS602 is equivalent to TI TIM99602)
-603	Dynamic Memory Refresh Controller, Cycle Steal and Burst Modes, for 64K DRAMs (74LS603 is equivalent to TI TIM99603)
-604	Octal 2-input Multiplexer with Latch, High-Speed, with Three-state outputs (74LS604 is equivalent to TI TIM99604)
-605	Octal 2-input Multiplexer with Latch, High-Speed, with open collector outputs (74LS605 is equivalent to TI TIM99605)
-606	Octal 2-input Multiplexer with Latch, Glitch-Free, with Three-state outputs (74LS606 is equivalent to TI TIM99606)
-607	Octal 2-input Multiplexer with Latch, Glitch-Free, with open collector outputs (74LS607 is equivalent to TI TIM99607)
-608	Memory Cycle Controller (74LS608 is equivalent to TI TIM99608)
-610	Memory Mapper, Latched, Three-state Outputs (74LS610 is equivalent to TI TIM99610)
-611	Memory Mapper, Latched, open collector outputs (74LS611 is equivalent to TI TIM99611)
-612	Memory Mapper, Three-state logic Outputs (74LS612 is equivalent to TI TIM99612)
-613	Memory Mapper, open collector outputs (74LS613 is equivalent to TI TIM99613)
-620	Octal Bus Transceiver, Inverting, Three-state Outputs
-621	Octal Bus Transceiver, Noninverting, open collector outputs
-622	Octal Bus Transceiver, Inverting, open collector outputs
-623	Octal Bus Transceiver, Noninverting, Three-state outputs

Function Number	Boolean Function
-624	Voltage-Controlled Oscillator with Enable Control, Range Control, Two-Phase Outputs
-625	Dual Voltage-Controlled Oscillator with Two-Phase Outputs
-626	Dual Voltage-Controlled Oscillator with Enable Control, Two-Phase Outputs
-627	Dual Voltage-Controlled Oscillator
-628	Voltage-Controlled Oscillator with Enable Control, Range Control, External Temperature Compensation, and Two-Phase Outputs
-629	Dual Voltage-Controlled Oscillator with Enable Control, Range Control
-630	16-bit Error Detection and Correction (EDAC) with three-state outputs
-631	16-bit Error Detection and Correction (EDAC) with open collector outputs
-632	32-bit Error Detection and Correction (EDAC)
-638	Octal Bus Transceiver with Inverting three-state outputs
-639	Octal Bus Transceiver with Noninverting three-state outputs
-640	Octal Bus Transceiver with Inverting three-state outputs
-641	Octal Bus Transceiver with Noninverting open collector outputs
-642	Octal Bus Transceiver with Inverting open collector outputs
-643	Octal Bus Transceiver with Mix of Inverting and Noninverting three-state outputs
-644	Octal Bus Transceiver with Mix of Inverting and Noninverting open collector outputs
-645	Octal Bus Transceiver
-646	Octal Bus Transceiver/Latch/Multiplexer with Noninverting three-state outputs
-647	Octal Bus Transceiver/Latch/Multiplexer with Noninverting open collector outputs

Function Number	Boolean Function
-648	Octal Bus Transceiver/Latch/Multiplexer with Inverting three-state outputs
-649	Octal Bus Transceiver/Latch/Multiplexer with Inverting open collector outputs
-651	Octal Bus Transceiver/Register with Inverting three-state outputs
-652	Octal Bus Transceiver/Register with Noninverting three-state outputs
-653	Octal Bus Transceiver/Register with Inverting three-state and open collector outputs
-654	Octal Bus Transceiver/Register with Noninverting three-state and open collector outputs
-657	Octal transceiver with parity generator/checker; 3-state
-658	Octal Bus Transceiver with Parity, Inverting
-659	Octal Bus Transceiver with Parity, Noninverting
-664	Octal Bus Transceiver with Parity, Inverting
-665	Octal Bus Transceiver with Parity, Noninverting
-668	Synchronous 4-bit Decade Up/Down Counter
-669	Synchronous 4-bit Binary Up/Down Counter
-670	4 by 4 Register File with three-state outputs
-671	4-bit Bidirectional Shift register/ Latch /Multiplexer with three-state outputs
-672	4-bit Bidirectional Shift register/ Latch/Multiplexer with three-state outputs
-673	16-bit Serial-in Serial-Out Shift register with Output Storage Registers, three-state outputs
-674	16-bit Parallel-in Serial-out Shift register with three-state outputs
-677	16-bit Address Comparator with Enable

Function Number	Boolean Function
-678	16-bit Address Comparator with Latch
-679	12-bit Address Comparator with Latch
-680	12-bit Address Comparator with Enable
-681	4-bit Parallel Binary Accumulator
-682	8-bit Magnitude Comparator
-683	8-bit Magnitude Comparator with open collector outputs
-684	8-bit Magnitude Comparator
-685	8-bit Magnitude Comparator with open collector outputs
-686	8-bit Magnitude Comparator with Enable
-687	8-bit Magnitude Comparator with Enable
-688	8-bit Equality Comparator
-689	8-bit Magnitude Comparator with open collector outputs
-690	4-bit Decimal Counter/Latch/ Multiplexer with Asynchronous Reset, Three-State Outputs
-691	4-bit Binary Counter/Latch/ Multiplexer with Asynchronous Reset, Three-State Outputs
-692	4-bit Decimal Counter/Latch/ Multiplexer with Synchronous Reset, Three-state Outputs
-693	4-bit Binary Counter/Latch/ Multiplexer with Synchronous Reset, Three-state Outputs
-694	4-bit Decimal Counter/Latch/ Multiplexer with Synchronous and Asynchronous Resets, three-state outputs
-695	4-bit Binary Counter/Latch/ Multiplexer with Synchronous and Asynchronous Resets, three-state outputs
-696	4-bit Decimal Counter/Register/ Multiplexer with Asynchronous Reset, three-state outputs
-697	4-bit Binary Counter/Register/ Multiplexer with Asynchronous Reset, three-state outputs

Function Number	Boolean Function
-698	4-bit Decimal Counter/Register/ Multiplexer with Synchronous Reset, three-state outputs
-699	4-bit Binary Counter/Register/ Multiplexer with Synchronous Reset, three-state outputs
-716	Programmable Decade Counter (-LS716 is equivalent to Motorola MC4016)
-718	Programmable Binary Counter (74LS718 is equivalent to Motorola MC4018)
-724	Voltage Controlled Multivibrator
-740	Octal Buffer/Line Driver, Inverting, three-state outputs
-741	Octal Buffer/Line Driver, Noninverting, three-state outputs, Mixed enable polarity
-744	Octal Buffer/Line Driver, Noninverting, three-state logic outputs
-748	8 to 3-line priority encoder
-779	8-bit bidirectional binary counter (3-State)
-783	Synchronous Address Multiplexer (74LS783 is equivalent to Motorola MC6883)
-790	Error Detection and Correction (EDAC)
-794	8-Bit Register with Readback
-795	Octal Buffer with Three-state logic outputs (74LS795 is equivalent to 81LS95)
-796	Octal Buffer with Three-state logic outputs (74LS796 is equivalent to 81LS96)
-797	Octal Buffer with Three-state logic outputs (74LS797 is equivalent to 81LS97)
-798	Octal Buffer with Three-state logic outputs (74LS798 is equivalent to 81LS98)
-804	Hex 2-input NAND Drivers
-805	Hex 2-input NOR Drivers
-808	Hex 2-input AND Drivers

Function Number	Boolean Function
-821	10-bit D-type flip-flop; positive-edge trigger; 3-state
-823	9-bit D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state
-827	10-bit buffer/line driver; non-inverting; 3-state
-0832	Low-power 3-input AND-OR gate
-832	Hex 2-input OR Drivers
-841	10-bit transparent latch with 5 V tolerant inputs/outputs; 3-state
-848	8 to 3-line Priority Encoder with three-state outputs
-873	Octal Transparent Latch
-874	Octal D-Type Flip-flop
-876	Octal D-Type Flip-flop with Inverting Outputs
-878	Dual 4-bit D-Type Flip-flop with Synchronous Clear, Noninverting three-state outputs
-879	Dual 4-bit D-Type Flip-flop with Synchronous Clear, Inverting three-state outputs
-880	Octal Transparent Latch with Inverting Outputs
-882	32-bit Lookahead Carry Generator
-885	Low-power dual function gate
-888	8-bit Slice Processor
-894	12-stage shift-and-store register LED driver
-899	9-bit dual latch transceiver with 8-bit parity generator/checker (3-State)
-926	4-digit counter/display driver
-935	3.5-digit Digital Voltmeter (DVM) support chip for Multiplexed 7-segment displays (MM-C935 = AD-D3501CCN)
-936	3.75-digit Digital Voltmeter (DVM) support chip for Multiplexed 7-segment displays (MM74C936 = AD-D3701CCN)
-1005	hex inverting buffer with open-collector output

Function Number	Boolean Function
-1035	hex noninverting buffers with open-collector outputs
-1403	3.3 V combined 8-bit bus receiver and 4-bit bus driver
-2241	3.3V Octal buffer/line driver with 30 Ohm series termination resistors; 3-State
-2244	Octal buffer/line driver with 30 Ω series termination resistors (3-State)
-2245	Octal transceiver with direction pin and 30 Ohm series termination resistors (3-State)
-2952	Octal registered transceiver with 5 V tolerant inputs/outputs; 3-state
-2960	Error Detection and Correction (EDAC) (74F2960 is equivalent to AMD Am2960)
-2961	EDAC Bus Buffer, Inverting
-2962	EDAC Bus Buffer, Noninverting
-2968	Dynamic Memory Controller
-2969	Memory Timing Controller for use with EDAC
-2970	Memory Timing Controller for use without EDAC
-3037	Quad 2-input NAND 30Ohm driver
-3125	Quadruple FET bus switch
-3126	Quad FET bus switch
-3157	2-channel analog multiplexer/ demultiplexer
-3208	Low-power 3-input OR-AND gate
-3244	Octal bus switch with quad output enables
-3245	Octal bus switch
-3251	1-of-8 FET multiplexer/demultiplexer
-3253	Dual 1-of-4 FET multiplexer/ demultiplexer
-3257	Quad 1-of-2 multiplexer/demultiplexer
-3306	Dual bus switch
-3384	10-bit bus switch with 5-bit output enables
-3861	10-bit bus switch with output enable
-4002	Dual 4-Input NOR gate

Function Number	Boolean Function
-4015	Dual 4-bit shift registers
-4016	Quadruple bilateral switches
-4017	5-Stage ÷10 Johnson Counter
-4024	7 Stage Ripple Carry Binary Counter
-4028	BCD to Decimal Decoder
-4040	12-stage binary ripple counter
-4046	Phase-locked loop and voltage-cont-rolled oscillator
-4049	Hex Inverting Buffer
-4050	Hex buffer/converter (non-inverting)
-4051	High-Speed CMOS Logic 8-Channel Analog Multiplexer/Demultiplexer
-4052	Dual 4-Channel Analog Multiplexer/ Demultiplexers
-4053	Triple 2-Channel Analog Multiplexer/ Demultiplexers
-4059	Programmable Divide-by-N Counter
-4060	14-stage binary ripple counter with oscillator
-4066	Quad bilateral switches
-4067	16-Channel Analog Multiplexer/ Demultiplexer
-4075	Triple 3-input OR gate
-4078	8-Input OR/NOR gate
-4094	8-bit Three-state Shift Register/Latch
-4245	Octal dual supply translating transceiver; 3-state

Function Number	Boolean Function
-4316	Quad analog switch
-4351	8-channel analog multiplexer/ demultiplexer with latch
-4353	Triple 2-channel analog multiplexer/ demultiplexer with latch
-4511	BCD to 7-Segment Decoder
-4514	4-to-16 line decoder/demultiplexer with input latches
-4515	4-to-16 line decoder/demultiplexer with input latches; inverting
-4520	Dual 4-bit Synchronous Binary Counter
-4538	Dual Retriggerable Precision Monostable Multivibrator
-4851	8-channel analog multiplexer/ demultiplexer with injection-current effect control
-4852	Dual 4-channel analog multiplexer/ demultiplexer with injection-current effect control
-5555	Programmable delay timer with oscillator
-6323	Programmable ripple counter with oscillator; 3-state
-7007	hex buffer (like 7407, however push-pull outputs)
-7014	Hex non-inverting precision Schmitt-trigger
-7266	Quad 2-input XNOR gate (Exclusive NOR, Equivalence test)

Output Drive Current by Logic Family

Logic Family	Supply Voltage	Standby Current	Max Drive
		µA	mA
AXP	0.7–2.75	0.6	8
AUP	0.8–3.6	0.9	4
LV	1.0–3.6	20	8
AVC	1.2–3.3	20	8
LVC	1.2–3.6	20	24
ALVC	1.2–3.6	40	24
AHC	2.0–6.0	40	8
HC	2.0–6.0	80	8
ALVT	2.3–3.6	90	64
LVT	2.7–3.6	120–190	64
FAST	4.5–5.5	90	24
ABT	4.5–5.5	250	64
NPIC	4.5–5.5 (LED output to 33 V)	200	100
HEF	5.0–15.0	600	3 (gates, LED output to 20 mA)

Common Package Suffix by Company

Competitor Suffix	Competitor	Nexperia Standard Suffix	Nexperia HEF Suffix	Package Name	SOT #
DW	Diodes Inc	GW		SC88	363
FW4	Diodes Inc	GF		XSON6	891
FZ4	Diodes Inc	GM		XSON6	886
S14	Diodes Inc	D	T	SO14	108
SE	Diodes Inc	GW		SC70	353
T14	Diodes Inc	PW	TT	TSSOP14	402
W5	Diodes Inc	GV		SO5	753
BQ	Fairchild (ON Semi)	BQ		DHVQFN14	762
BQ	Fairchild (ON Semi)	BQ		DHVQFN16	763
BQ	Fairchild (ON Semi)	BQ		DHVQFN20	764
CM	Fairchild (ON Semi)	D	T	SO14	108
CN	Fairchild (ON Semi)	N	P	DIP14	27
FH(X)	Fairchild (ON Semi)	GF		XSON8	1089
G	Fairchild (ON Semi)	EC		LFBGA96	536
G	Fairchild (ON Semi)	EC		LFBGA114	537

Competitor Suffix	Competitor	Nexperia Standard Suffix	Nexperia HEF Suffix	Package Name	SOT #
K8	Fairchild (ON Semi)	DC		VSSOP8	765
KX8	Fairchild (ON Semi)	GD		XSON8U	996
L6	Fairchild (ON Semi)	GM		XSON6	886
L8	Fairchild (ON Semi)	GM		XQFN8U	902
M	Fairchild (ON Semi)	D		SO8	96
M	Fairchild (ON Semi)	D	T	SO14	108
M	Fairchild (ON Semi)	D	T	SO16	162
M	Fairchild (ON Semi)	D	T	SO20	163
M5	Fairchild (ON Semi)	GV		SO5	753
ME	Fairchild (ON Semi)	DL		SSOP48	370
ME	Fairchild (ON Semi)	DL		SSOP56	371
MEA	Fairchild (ON Semi)	DL		SSOP48	370
MEA	Fairchild (ON Semi)	DL		SSOP56	371
MSA	Fairchild (ON Semi)	DB		SSOP20	339
MSA	Fairchild (ON Semi)	DB		SSOP24	340
MSA	Fairchild (ON Semi)	DB		SSOP28	341
MT	Fairchild (ON Semi)	DGG		TSSOP48	362
MT	Fairchild (ON Semi)	DGG		TSSOP56	364
MTC	Fairchild (ON Semi)	PW		TSSOP24	355
MTC	Fairchild (ON Semi)	PW	TT	TSSOP20	360
MTC	Fairchild (ON Semi)	PW	TT	TSSOP14	402
MTC	Fairchild (ON Semi)	PW	TT	TSSOP16	403
MTC	Fairchild (ON Semi)	PW		TSSOP8	530
MTD	Fairchild (ON Semi)	DGG		TSSOP48	362
MTD	Fairchild (ON Semi)	DGG		TSSOP56	364
MTD	Fairchild (ON Semi)	DGG		TSSOP64	646
MX	Fairchild (ON Semi)	D		SO16	162
N	Fairchild (ON Semi)	N	P	DIP14	27
N	Fairchild (ON Semi)	N	P	DIP16	38
N	Fairchild (ON Semi)	N	P	DIP24	101
N	Fairchild (ON Semi)	N		DIP24	101
N	Fairchild (ON Semi)	N		DIP28	117
N	Fairchild (ON Semi)	N	P	DIP20	146
NT	Fairchild (ON Semi)	N		DIP24	101
P5	Fairchild (ON Semi)	GW		SC70	353
P6	Fairchild (ON Semi)	GW		SC88	363
P6X	Fairchild (ON Semi)	GW		SC88	363

Competitor Suffix	Competitor	Nexperia Standard Suffix	Nexperia HEF Suffix	Package Name	SOT #
PC	Fairchild (ON Semi)	N	P	DIP14	27
PC	Fairchild (ON Semi)	N	P	DIP16	38
PC	Fairchild (ON Semi)	N	P	DIP24	101
PC	Fairchild (ON Semi)	N		DIP28	117
PC	Fairchild (ON Semi)	N	P	DIP20	146
QSC	Fairchild (ON Semi)	DK		SSOP24	556
QSC	Fairchild (ON Semi)	DS		SSOP16	519
QSC	Fairchild (ON Semi)	DS		SSOP20	724
SC	Fairchild (ON Semi)	D		SO8	96
SC	Fairchild (ON Semi)	D	T	SO14	108
SC	Fairchild (ON Semi)	D		SO28	136
SC	Fairchild (ON Semi)	D	T	SO16	162
SC	Fairchild (ON Semi)	D	T	SO16	162
SC	Fairchild (ON Semi)	D	T	SO20	163
SPC	Fairchild (ON Semi)	N		DIP24	101
T	Fairchild (ON Semi)	DGG		TSSOP56	364
WM	Fairchild (ON Semi)	D		SO28	136
WM	Fairchild (ON Semi)	D	T	SO16	162
WM	Fairchild (ON Semi)	D	T	SO20	163
BF	IDT	EC		LFBGA96	536
CD	IDT	N	P	DIP20	146
DC	IDT	D		SO8	96
DC	IDT	D	T	SO14	108
DJ	IDT	DGV		TSSOP48	480
PA	IDT	DGG		TSSOP48	362
PA	IDT	DGG		TSSOP56	364
PC	IDT	DK		SSOP24	556
PC	IDT	DS		SSOP16	519
PC	IDT	DS		SSOP20	724
PF	IDT	DGV		TSSOP48	480
PF	IDT	DGV		TSSOP56	481
PG	IDT	PW		TSSOP24	355
PG	IDT	PW	TT	TSSOP20	360
PG	IDT	PW	TT	TSSOP14	402
PG	IDT	PW	TT	TSSOP16	403
PS	IDT	D	T	SO24	137
PS	IDT	D	T	SO20	163

Competitor Suffix	Competitor	Nexperia Standard Suffix	Nexperia HEF Suffix	Package Name	SOT #
PV	IDT	DL		SSOP48	370
PV	IDT	DL		SSOP56	371
PY	IDT	DB		SSOP20	339
2G	On Semi	DB	TS	SSOP16	338
AMX	On Semi	GM		XSON6	886
CMX	On Semi	GF		XSON6	891
CMX	On Semi	GF		XSON8	1089
CPG	On Semi	N	P	DIP14	27
D	On Semi	D		SO8	96
D	On Semi	D	T	SO14	108
D	On Semi	D		SO28	136
D	On Semi	D	T	SO24	137
D	On Semi	D	T	SO16	162
D	On Semi	D	T	SO16	162
D	On Semi	D	T	SO20	163
D	On Semi	PW		TSSOP8	530
DF	On Semi	GW		SC88	363
DFT	On Semi	GW		SC70	353
DG	On Semi	D	T	SO14	108
DR2G	On Semi	D		SO20	163
DT	On Semi	DGG		TSSOP48	362
DT	On Semi	PW		TSSOP24	355
DT	On Semi	PW	TT	TSSOP14	402
DT	On Semi	PW	TT	TSSOP16	403
DT	On Semi	PW		TSSOP8	530
DT	On Semi	PW		TSSOP10	552
DT	On Semi	PW	TT	TSSOP20	360
DTT	On Semi	GV		SO5	753
DW	On Semi	D	T	SO16	162
DWR2G	On Semi	D		SO20	163
EP	On Semi	GM		XQFN10U	1049
MN	On Semi	BQ		DHVQFN16	763
MN	On Semi	BQ		DHVQFN20	764
NG	On Semi	N	P	DIP14	27
NG	On Semi	N	P	DIP16	38
NG	On Semi	N		DIP24	101
NG	On Semi	N		DIP24	101

Competitor Suffix	Competitor	Nexperia Standard Suffix	Nexperia HEF Suffix	Package Name	SOT #
NG	On Semi	N		DIP28	117
NG	On Semi	N		CDIP28	135
NG	On Semi	N	P	DIP20	146
OM	On Semi	GU-16		XQFN16	1161
P	On Semi	N	P	DIP14	27
P	On Semi	N	P	DIP16	38
P	On Semi	N	P	DIP24	101
P	On Semi	N	P	DIP24	101
P	On Semi	N		DIP28	117
P	On Semi	N	P	DIP20	146
QZ	On Semi	DK		SSOP24	556
QZ	On Semi	DS		SSOP16	519
QZ	On Semi	DS		SSOP20	724
SQL	On Semi	GW		SC70	353
SQL	On Semi	GW		SC88	363
US	On Semi	DC		VSSOP8	765
USGH	On Semi	DC		VSSOP8	765
CM	Renesas	GW		SC70	353
CM	Renesas	GW		SC88	363
P	Renesas	N	P	DIP14	27
P	Renesas	N	P	DIP16	38
P	Renesas	N	P	DIP24	101
P	Renesas	N		DIP24	101
P	Renesas	N		DIP28	117
P	Renesas	N		CDIP28	135
P	Renesas	N	P	DIP20	146
RP	Renesas	D		SO8	96
RP	Renesas	D	T	SO14	108
RP	Renesas	D		SO28	136
RP	Renesas	D	T	SO24	137
RP	Renesas	D	T	SO16	162
RP	Renesas	D	T	SO16	162
RP	Renesas	D	T	SO20	163
T	Renesas	DGG		TSSOP48	362
T	Renesas	DGG		TSSOP56	364
T	Renesas	DGG		TSSOP64	646
T	Renesas	DP		TSSOP8	505

Competitor Suffix	Competitor	Nexperia Standard Suffix	Nexperia HEF Suffix	Package Name	SOT #
T	Renesas	PW		TSSOP24	355
T	Renesas	PW	TT	TSSOP20	360
T	Renesas	PW	TT	TSSOP14	402
T	Renesas	PW	TT	TSSOP16	403
T	Renesas	PW		TSSOP8	530
T	Renesas	PW		TSSOP10	552
US	Renesas	DC		VSSOP8	765
B1R	ST Micro	N	P	DIP14	27
B1R	ST Micro	N	P	DIP16	38
B1R	ST Micro	N	P	DIP20	146
BEY	ST Micro	N	P	DIP14	27
BEY	ST Micro	N	P	DIP16	38
BM1	ST Micro	D	T	SO14	108
BM1	ST Micro	D	T	SO24	137
BM1	ST Micro	D	T	SO16	162
BM1	ST Micro	D	T	SO20	163
C	ST Micro	GW		SC70	353
DTR	ST Micro	GM		XSON6	886
DTR	ST Micro	PW	TT	TSSOP20	360
MO13	ST Micro	D	T	SO14	108
MO13	ST Micro	D	T	SO24	137
MO13	ST Micro	D	T	SO16	162
MO13	ST Micro	D	T	SO20	163
MTR	ST Micro	D	T	SO14	108
MTR	ST Micro	D	T	SO24	137
MTR	ST Micro	D	T	SO16	162
MTR	ST Micro	D	T	SO20	163
RM13	ST Micro	D	T	SO14	108
RM13	ST Micro	D	T	SO24	137
RM13	ST Micro	D	T	SO16	162
RM13	ST Micro	D	T	SO20	163
STR	ST Micro	GV		SO5	753
TTR	ST Micro	DGG		TSSOP48	362
TTR	ST Micro	PW	TT	TSSOP20	360
TTR	ST Micro	PW	TT	TSSOP14	402
TTR	ST Micro	PW	TT	TSSOP16	403
D	TI	D		SO8	96

Competitor Suffix	Competitor	Nexperia Standard Suffix	Nexperia HEF Suffix	Package Name	SOT #
D	TI	D	T	SO14	108
D	TI	D	T	SO16	162
DA	TI	DR		TSSOP32	487
DAE	TI	DR		TSSOP32	487
DB	TI	DB		SSOP14	337
DB	TI	DB	TS	SSOP16	338
DB	TI	DB		SSOP20	339
DB	TI	DB		SSOP24	340
DB	TI	DB		SSOP28	341
DBQ	TI	DS		SSOP16	519
DBV	TI	GV		SO5	753
DCK	TI	GW		SC70	353
DCK	TI	GW		SC88	363
DCT	TI	DP		TSSOP8	505
DCU	TI	DC		VSSOP8	765
DCU	TI	GD		XSON8U	996
DDC	TI	GV		SO5	753
DDU	TI	DC		VSSOP8	765
DGG	TI	DGG		TSSOP48	362
DGG	TI	DGG		TSSOP56	364
DGG	TI	DGG		TSSOP64	646
DGV	TI	DGV		TSSOP48	480
DGV	TI	DGV		TSSOP56	481
DL	TI	DL		SSOP48	370
DL	TI	DL		SSOP56	371
DPW	TI	GX		X2SON5	1226
DQE	TI	GF		XSON8	1089
DQE	TI	GS		XSON8	1203
DQM	TI	GM			1309
DRY	TI	GM		XSON6	886
DSF	TI	GS		XSON6	1202
DW	TI	D		SO28	136
DW	TI	D	T	SO24	137
DW	TI	D	T	SO16	162
DW	TI	D	T	SO20	163
E	TI	N	P	DIP14	27
E	TI	N	P	DIP16	38

Competitor Suffix	Competitor	Nexperia Standard Suffix	Nexperia HEF Suffix	Package Name	SOT #
E	TI	N	P	DIP24	101
E	TI	N		DIP28	117
E	TI	N	P	DIP20	146
F	TI	N		CDIP28	135
G	TI	DG		TVSOP80	647
G	TI	DGG		TSSOP48	362
GKE	TI	EC		LFBGA96	536
GKF	TI	EC		LFBGA114	537
GQL	TI	EV		VFBGA56	702
J	TI	N		CDIP28	135
L8	TI	GM		XQFN8U	902
M	TI	D		SO8	96
M	TI	D	T	SO14	108
M	TI	D		SO28	136
M	TI	D	T	SO24	137
M	TI	D	T	SO16	162
M	TI	D	T	SO16	162
M	TI	D	T	SO20	163
M96	TI	D		SO16	162
N	TI	N	P	DIP14	27
N	TI	N	P	DIP16	38
N	TI	N	P	DIP24	101
N	TI	N		DIP24	101
N	TI	N		DIP28	117
N	TI	N	P	DIP20	146
NE	TI	N	P	DIP16	38
NT	TI	N		DIP24	101
PW	TI	PW		TSSOP24	355
PW	TI	PW	TT	TSSOP20	360
PW	TI	PW	TT	TSSOP14	402
PW	TI	PW	TT	TSSOP16	403
PW	TI	PW		TSSOP8	530
PW	TI	PW		TSSOP10	552
RHL	TI	BQ		DHVQFN24	815
RSE	TI	GM		XQFN8U	902
RSV	TI	GU-16		XQFN16	1161
RSW	TI	GU		UQFN	1160

Competitor Suffix	Competitor	Nexperia Standard Suffix	Nexperia HEF Suffix	Package Name	SOT #
RUT	TI	GU-12			1174
TK	TI	TK		HVSON10	650
TPA	TI	DGG		TSSOP48	480
TPV	TI	DL		SSOP56	371
YEB	TI	UK		WLCSP4	n/a
YEC	TI	UK		WLCSP6	n/a
YEG	TI	UK		WLCSP12	n/a
YZB	TI	UK		WLCSP4	n/a
YZC	TI	UK		WLCSP6	n/a
YZG	TI	UK		WLCSP12	n/a
YZP	TI	GM		XSON6	886
YZP	TI	GT		XSON8	833
YZT	TI	UK		WLCSP12	n/a
ZKE	TI	EC		LFBGA96	536
ZKF	TI	EC		LFBGA114	537
ZQL	TI	EV		VFBGA56	702
BF	Toshiba	D	T	SO14	108
BF	Toshiba	D	T	SO24	137
BF	Toshiba	D	T	SO16	162
BF	Toshiba	D	T	SO20	163
BP	Toshiba	N	P	DIP14	27
BP	Toshiba	N	P	DIP16	38
F	Toshiba	GV		SO5	753
FE	Toshiba	GW		SC88	363
FK	Toshiba	DC		VSSOP8	765
FN	Toshiba	D	T	SO14	108
FN	Toshiba	D	T	SO16	162
FS	Toshiba	DB		SSOP24	340
FS	Toshiba	PW		TSSOP24	355
FT	Toshiba	DB		SSOP14	337
FT	Toshiba	DB	TS	SSOP16	338
FT	Toshiba	DB		SSOP20	339
FT	Toshiba	DGG		TSSOP48	362
FT	Toshiba	DGG		TSSOP56	364
FT	Toshiba	DL		SSOP48	370
FT	Toshiba	DL		SSOP56	371
FT	Toshiba	PW	TT	TSSOP20	360

Competitor Suffix	Competitor	Nexperia Standard Suffix	Nexperia HEF Suffix	Package Name	SOT #
FT	Toshiba	PW	TT	TSSOP14	402
FT	Toshiba	PW	TT	TSSOP16	403
FTG	Toshiba	HR		HXQFN16U	1039
FU	Toshiba	GW		SC70	353
FU	Toshiba	GW		SC88	363
FW	Toshiba	D		SO8	96
FW	Toshiba	D		SO28	136
FW	Toshiba	D	T	SO16	162
P	Toshiba	N	P	DIP14	27
P	Toshiba	N	P	DIP16	38
P	Toshiba	N		DIP24	101
P	Toshiba	N	P	DIP20	146

Competitor Logic Family to Nexperia Logic Family Cross Reference

Competitor	Competitor Logic Family	Nexperia Logic Family	Similarity	Comments
Diodes Inc	AHC	AHC	exact	
Diodes Inc	AHCT	AHCT	exact	
Diodes Inc	AUP	AUP	exact	
Diodes Inc	AVC	AVC	exact	
Diodes Inc	HC	HC	exact	
Diodes Inc	HCT	HCT	exact	
Diodes Inc	LV	LV	exact	
Diodes Inc	LVC	LVC	exact	
Diodes Inc	LVT	LVT	exact	
Fairchild (ON Semi)	ABT	ABT	exact	
Fairchild (ON Semi)	AC	AHC	near	AHC is only 8 mA vs 24 mA drive current, but lower noise. No clamp diode in AHC makes it 5 V tolerant, AC is not. AHC has wider temp range
Fairchild (ON Semi)	ACT	AHCT	near	AHCT is only 8mA vs 24 mA drive current, but lower noise. No clamp diode in AHCT makes it 5 V tolerant, AC is not. AHCT has wider temp range
Fairchild (ON Semi)	ALS	ABT	near	ABT is similar speed and VCC range but only half the drive current of ALS
Fairchild (ON Semi)	AS	ABT	near	Similar speed, similar drive currents

Competitor	Competitor Logic Family	Nexperia Logic Family	Similarity	Comments
Fairchild (ON Semi)	C	HEF	near	ex: 74C74. VCC = 3–15 V, tpd = 70–140 ns, 2 mA output
Fairchild (ON Semi)	CD4K	HEF	exact	
Fairchild (ON Semi)	F	F	exact	
Fairchild (ON Semi)	FSA	LVC	near	family name for switches, same as NC7WB. 1.65–5.5 VCC
Fairchild (ON Semi)	FST	CBT	exact	
Fairchild (ON Semi)	FXLH	AUP	exact	
Fairchild (ON Semi)	FXLP	AUP1T	near	
Fairchild (ON Semi)	HC	HC	exact	
Fairchild (ON Semi)	HCT	HCT	exact	
Fairchild (ON Semi)	LCX/H	LVC	near	LVC is wider operating VCC, slightly faster Tpd. Both are 24 mA drive
Fairchild (ON Semi)	LS	ABT	near	ABT is faster (1–4 vs 2–10 ns) , higher driver current (64/32 vs 24/15 mA drive)
Fairchild (ON Semi)	LVT/H	LVT	exact	
Fairchild (ON Semi)	LVX	LV	near	LVX is wider operating range, LV is not 5 V input tolerant
Fairchild (ON Semi)	NC7NZ	LVC3G	exact	
Fairchild (ON Semi)	NC7S	AHC1G	near	"S" speed logic. Single gate, 2.0–6.0 V, 2 mA drive, 3.5 ns. AHC is 8 mA, 5 nS, 2–6 VCC: not quite as fast
Fairchild (ON Semi)	NC7SB	LVC1G	near	Single channel switch process crosses to LVC switches. Same as Fairchild FSA family. Ex: 3157
Fairchild (ON Semi)	NC7SP	AUP1G	exact	Single gate version
Fairchild (ON Semi)	NC7ST	HC1G	near	Single gate. "compatible with HC but half drive current" per Fairchild site
Fairchild (ON Semi)	NC7SV	AUP1G	near	Single gate. 1–12 nS, 24 mA drive. Similar to AUP but more drive current. FSC calls SP a "cross" for SV. AUP is slightly better VCC
Fairchild (ON Semi)	NC7SZ	LVC1G	exact	Single gate. Both families are 1.65–5.5 V VCC with 24 mA drive.
Fairchild (ON Semi)	NC7WB	LVC2G	near	Switch process crosses to LVC switches. Same as Fairchild FSA family
Fairchild (ON Semi)	NC7WP	AUP2G	near	Dual gate devices. AUP is slightly better VCC range, higher drive current (4 mA vs 2.6), same speeds. 0.9–3.6 V, 2–27 nS, 2.6 mA drive
Fairchild (ON Semi)	NC7WT	HC2G	exact	Dual gate variant

Competitor	Competitor Logic Family	Nexperia Logic Family	Similarity	Comments
Fairchild (ON Semi)	NC7WV	AUP2G	near	Dual gate. AUP is slightly better VCC. WV family has Schmitt trigger inputs. Mostly dual gates
Fairchild (ON Semi)	NC7WZ	LVC2G	near	Dual gate. Both families are 1.65–5.5 V VCC with 24 mA drive. WZ family has Schmitt trigger inputs. Dual gate devices
Fairchild (ON Semi)	VCX/H	ALVCH	exact	
Fairchild (ON Semi)	VHC/T	AHC/T	near	Traditionally crosses to HC. AHC is slightly less power. Note that Nexperia does make a limited number of VHC devices also
IDT	ALVC	ALVC	exact	
IDT	ALVC/H	ALVC/H	exact	
IDT	CBTLV	CBTLV	exact	
IDT	FCT (3V)	LVT	exact	
IDT	FCT (5V)	ABT	exact	
IDT	LVC	LVC	exact	
IDT	QS3VH	LVC	near	QS3VH is a fast bus process similar to Nexperia LVC
IDT	VH	LVC	near	VH = 2.3–3.6 VCC, V = 1.2–3.6 VCC, 5 V tolerant
On Semi	14xxx	HEF	exact	No differences but name
On Semi	AC	AHC	near	5 nS tPD, 24 mA output. AHC will work for all but high power drive applications
On Semi	ACT	AHCT	near	AHCT is only 8 mA vs 24 mA drive current, but lower noise. No clamp diode in AHCT makes it 5 V tolerant, AC is not. AHCT has wider temp range
On Semi	CBTL	CBTL	exact	Bus switch process
On Semi	HC	HC	exact	
On Semi	HCT	HCT	exact	
On Semi	LCX	LVC	near	LVC is wider operating VCC, slightly faster Tpd. Both are 24 mA drive
On Semi	LVX	LV	near	LV is wider operating range, LV is not 5V input tolerant
On Semi	NL17SG	AUP	near	0.9–3.6 V, 4.6 V tolerant pins
ON Semi	NL17SH	HC	exact	tpd = 3 nS, 2–5 V VCC, single gate. Example NL17SH00
ON Semi	NL17SHT	HCT	exact	
On Semi	NL17SV	AUP	exact	

Competitor	Competitor Logic Family	Nexperia Logic Family	Similarity	Comments
On Semi	NL17SZ	LVC	exact	
On Semi	NL27WZ	LVC	exact	
On Semi	NL37WZ	LVC3G	exact	Ex: Triple buffer
On Semi	NL7SZ	LVC	exact	
On Semi	NL7WB	LVC	exact	
On Semi	NLSX	NTS	exact	Dual voltage bidirectional level translators
On Semi	NLU	AHCT	near	5.5 V VCC, TTl outputs, 8 mA drive, 3.8 ns prop delay, overvolt tolerant inputs
ON Semi	NLV	HEF	near	HEF with Q100 grade
On Semi	NLX	LVC	exact	For 74LVC2G14, etc
On Semi	VCX	ALVCH	exact	
On Semi	VHC	AHC	near	Traditionally crosses to HC. AHC is slightly less power. Note that Nexperia does make a limited number of VHC devices also
On Semi	VHCT	AHCT	near	Traditionally crosses to HC. AHC is slightly less power. Note that Nexperia does make a limited number of VHC devices also
Pericom	STX	AHC1G	exact	ex P174STX1G08
Renesas	AC	AHC	near	5 nS tPD, 24 mA output. AHC will work for all but high power drive applications
Renesas	ACT	AHCT	near	5 nS tPD, 24 mA output. AHC will work for all but high power drive applications
Renesas	ALVC	ALVC	exact	per Renesas website
Renesas	BC	ABT	exact	5 nS tPD, 15/64 mA output
Renesas	CBT	CBT	exact	
Renesas	HC	HC	exact	
Renesas	HCT	HCT	exact	
Renesas	LD	HEF	near	For LED drive, up to 30 V, 200 mA drive. Similar to HEF but note that some are even higher voltage.
Renesas	LS	ABT	near	ABT is faster(1–4 vs 2–10 ns) , higher driver current (64/32 vs 24/15 mA drive)
Renesas	LV	LV	exact	For 1 and 2 gate devices only (per Renesas website)

Competitor	Competitor Logic Family	Nexperia Logic Family	Similarity	Comments
Renesas	LV-A	LV, AHC	near	Renesas declares Nexperia LV and AHC are both crosses to LV-A
Renesas	LVC-B	LVC	exact	From Renesas website
ST Micro	AC	AHC	near	5 nS tPD, 24 mA output. AHC will work for all but high power drive applications
ST Micro	ACT	AHCT	near	AHCT is only 8 mA vs 24 mA drive current, but lower noise. No clamp diode in AHCT makes it 5 V tolerant, AC is not. AHCT has wider temp range
ST Micro	ALVC	ALVC	exact	
ST Micro	AUP	AUP	exact	
ST Micro	HC	HC	exact	
ST Micro	HCF	HEF	exact	
ST Micro	HCT	HCT	exact	
ST Micro	LCX	LVC	near	LVC is wider operating VCC, slightly faster Tpd. Both are 24 mA drive. "Speed of AC/ACT, less power"
ST Micro	LVC	LVC	exact	
ST Micro	LVX	LV	near	LV is wider operating range, LV is not 5 V input tolerant
ST Micro	V	LVC	near	V = (VCC = 2.5 V, Tpd = 4.8 ns, 8 mA drive, overvolt tolerant), LVC=(1.65–5.5 VCC, Tpd = 3.7 ns, 24 mA drive, overvolt tolerant). 1G, 2G variety
ST Micro	VCX	ALVCH	exact	
ST Micro	VHC	AHC	exact	
ST Micro	VHCT	AHCT	exact	
TI	ABT	ABT	exact	
TI	AHC	AHC	exact	
TI	AHCT	AHCT	exact	
TI	ALS	ABT	near	ABT is similar speed and VCC range but only half the drive current of ALS
TI	ALVC	ALVC	exact	
TI	ALVT	ALVT	exact	
TI	AUC	AUP	near	AUP is similar to AUC. A bit slower, a bit less power.
TI	AUP	AUP	exact	
TI	AVC	AVC	exact	
TI	CBT	CBT	exact	
TI	CBTLV	CBTLV	exact	

Competitor	Competitor Logic Family	Nexperia Logic Family	Similarity	Comments
TI	CD4000	HEF	exact	No differences but name
TI	F	F	exact	
TI	FCT	ABT	exact	
TI	HC	HC	exact	
TI	HCT	HCT	exact	
TI	LV	LV	exact	
TI	LVC	LVC	exact	
TI	LVT	LVT	exact	
Toshiba	AC	AHC	near	5 nS tPD, 24 mA output. AHC will work for all but high power drive applications
Toshiba	ACT	AHCT	near	AHCT is only 8 mA vs 24 mA drive current, but lower noise. No clamp diode in AHCT makes it 5 V tolerant, AC is not. AHCT has wider temp range
Toshiba	HC	HC	exact	
Toshiba	HCT	HCT	exact	
Toshiba	LCX	LVC	near	LVC is wider operating VCC, slightly faster Tpd. Both are 24 mA drive
Toshiba	LVX	LV	near	LV is wider operating range, LV is not 5 V input tolerant
Toshiba	TC4	HEF	exact	example TC4049
Toshiba	TC4xxx	HEF	exact	
Toshiba	TC7MA	ALVCH	near	Obsolete family number. Has been replaced with newer family name
Toshiba	TC7MET	AHCT	near	Obsolete family number. Has been replaced with newer family name
Toshiba	TC7MH	AHC	exact	Obsolete family number. Has been replaced with newer family name
Toshiba	TC7MZ	LVC	near	Obsolete family number. Has been replaced with newer family name
Toshiba	TC7PA	LVC	exact	Single and dual gate VCX parts. 1.8–3.6 VCC
Toshiba	TC7PG	AUP	near	0.9–3.6 VCC dual gate, 8 ma drive, 2 nS. Closest to AUC family: AUP has less drive current
Toshiba	TC7PH	AHC	near	2–5.5 VCC, 8 mA drive 5 nS. 5.3 nS. Closest to AHC
Toshiba	TC7PH	AHC	near	Obsolete family number. Has been replaced with newer family name

Competitor	Competitor Logic Family	Nexperia Logic Family	Similarity	Comments
Toshiba	TC7S	AHC	near	2G Dual Gate devices in HC family. 2–6 VCC, 2.6 mA drive, 5 nS. Similar to AHC
Toshiba	TC7SA	LVC	exact	1.8–3.6 VCC, 24 mA. 2.8–7.4 nS "VCX equivalent" per Toshiba
Toshiba	TC7SET	AHCT	near	1 gate devices 4.5–5.5 VCC, 8 mA drive, 5 nS. Closest to AHCT. HC is not quite fast enough
Toshiba	TC7SG	AUP	near	1 gate devices 0.9–3.6 VCC, 8 mA drive, 2–5 nS. AUP has less drive current, LV has drive but not speed.
Toshiba	TC7SH	AHC	near	1G Single gate version of VHC family. 2–5.5 VCC, 8 mA drive, 4–5 nS
Toshiba	TC7SZ	LVC	exact	1 gate devices of LCX family. 1.6–5.5 VCC, 32 mA drive, 2–3nS.
Toshiba	TC7W	HC	near	2–6 VCC, 5 mA drive, dual gate, <10 ns. AHC. Single gate version of HCT logic
Toshiba	TC7WG	LV	near	LVP family 0.9–3.6 VCC, 8 mA drive, 2–3 nS. LV is a bit slower, AUP not as much drive current. 1,2,3 G devices
Toshiba	TC7WH	AHC	near	2 and 3 gate devices in VHCT family. 2–5.5 VCC, 8 mA drive, 3–5nS. 1,2,3 gates
Toshiba	TC7WT	HCT	near	High speed TTL input 4.5–5.5 VCC, 6mA drive, 15 nS.
Toshiba	TC7WT	HCT	near	Obsolete family number. Has been replaced with newer
Toshiba	TC7WZ	LVC	near	SHS series. "Matches LCX performance". 32 mA drive, 3 ns, 1.65–5.5. 1,2,3 gate devices. LVC VCC is not quite as wide
Toshiba	VCX	ALVCH	exact	
Toshiba	VHC	AHC	exact	
Toshiba	VHCT	AHCT	exact	

Abbreviations

ADC	Analog to Digital Convertor
µF	Micro Farad
AHCT	Advanced High-speed Cmos with Transistor–transistor logic voltages
ALVT	Advanced Low-Voltage BiCMOS Technology
AND	logical function
ANSI	American National Standards Institute
ASIC	Application-Specific Integrated Circuits
AUP	Advanced Ultralow Power
AVC	Advanced Very-low-voltage CMOS
AXP	Advanced eXtremely low voltage and Power
BBM	Break Before Make
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
Cl	Load capacitance
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
CP	Clock Input
Cpd	Equivalent power dissipation capacitance
CS	Switch Capacitance
Cs(on)	On-state capacitance
D-Flipflop	Data or Delay Flipflop
DIR	Direction
D-Latch	Delay Latch
ESD	Electrostatic Discharge
f	Frequency
f–3dB	Frequency with -3dB attenuation/loss
FAQ	Frequently Asked Questions
FET	Field Effect Transistor
fi	Input frequency
FIFO	first in first out
fo	Output frequency
FPGA	Field-Programmable Gate Array
GND	Supply ground reference level
GPIO	General - Purpose Input/ Output
HBM	Human Body Model
HCT	High-speed Cmos with Transistor – transistor logic voltages
I/O	Input and Output
IC	Integrated Circuit
Icc	Supply current
Icch	quiescent current when the output is logic high
Iccl	quiescent current when the output is logic low
ID	Drain current
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
Ignd	Current in supply ground pin
Iik	Input clamping current
Il	Input leakage current

Ioff	Off state current
Iok	Output clamping current
Istat	Static supply current
JEDEC	Joint Electron Device Engineering Council
LVC	Low Voltage Complementary metal oxide semiconductor
LVT	Low-Voltage BiCMOS Technology
MBB	Make before break
MCU	Micro Controller Unit (microcontroller)
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MR	Master Reset
NAND	Not AND, logical function
nF	Nano Farad
NMOST	N-channel Metal Oxide Semiconductor Transistor
NOR	NOT OR, logical function
OE	Output Enable
OR	logical function
OVT	Over Voltage Tolerant
PCB	Printed Circuit Board
PD	Power dissipation
pF	piko Farad
PMOST	P-channel Metal Oxide Semiconductor Transistor
Ptot	Total power dissipation
Q	Charge
Q100	Automotive Electronics Council -Q100 qualification specification
R&D	Research and Development
Rcl	Current Limiting Resistor
RF	Radio Frequency
Ron	Resistance of a transitor in on-state
RPU	Pull-up Resistor
RS flip-flop	Reset Set flip flop
SOC	System On Chip
SP3T	Single Pole Triple Throw
SP8T	Single pole 8 throw
SPDT	Single Pole Double Throw
SPST	Single pole single throw
Ten	Enable time
Tf	Fall time
Th	Hold time
THD	Total Harmonic Distortion
T_j	Junction temperature
Tpd	Propagation delay time
Tphl	Propagation delay time for logic high to low transition
Tplh	Propagation delay time for logic low to high transition
Tr	Rise time
Tsk	Skew time
Tskhl	Skew time for logic high to low transition
Tsklh	Skew time for logic low to high transition
Tsu	Setup time
Tthl	Fall time for logic high to low transition

TTL	Transistor Transistor Logic
Ttlh	Rise time for logic low to high transition
Tw	Pulse width time
US	United States
VCC	Supply Voltage
VEE	Negative Supply Voltage
VGS	Gate Source Voltage
Vi	Input voltage
Vih	Input voltage for a logic high level signal
Vil	Input voltage for a logic low level signal
Vo	Output voltage
VOH	Output high voltage
VOL	Output low voltage
VSS	Ground voltage
VT	Threshold Voltage
VT–	Negative going threshold voltage
VT+	Positive going threshold voltage
XNOR	Excusive- Not OR, logical funtion
XOR	Excusive-OR, logical funtion
Xtalk	cross talk
ZL	characteristic impedance

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