Two-level, slew-rate control reduces temperature stress of semiconductors in power modules

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Abstract

It is difficult to optimize the switching performance of IGBTs with only one fixed value for the gate resistor. This is especially true if the level of dv/dt during switching needs to be limited, as is the case for typical motor drives, and applications where conducted EMI levels need to be controlled. In this paper, we present evaluations of a simple slew-rate control gate driver IC that is operated in a 22 kW inverter. The operating advantages for an industrial motor drive in terms of junction temperature are presented by relevant measurements.

1 Introduction

Slew-rate drivers are available on the market today ([1], [2]) but are targeted for high-performance systems. Therefore, due to their size and complexity, they are not suitable for lower power and cost-sensitive converter designs. The goal of this study was to design a 22 kW drive inverter with a structure similar to that of commercial inverters. The inverter uses a novel two-level, slew-rate control (2L-SRC) gate driver IC, which is a very simple isolated gate driver using only 8 pins. The IC enables the user to alternate the value of the gate resistor between two different values, and to implement any changes on a cycle-to-cycle basis of the pulse width modulation.

2 What are the advantages of a dual-gate resistor value?

The dv_{CE}/dt level of an IGBT turn-on event is usually higher at low temperatures and low currents. This means that if the dv_{CE}/dt level is to be limited, the value of the gate resistor needs to be increased. Such limitations of dv_{CE}/dt are common in motor drives, where the motor current also contains zero crossings. That is why the gate resistance should be dimensioned at 0 for example, or perhaps at 1/10 of the rated current of the power module, and at room temperature. It is known that high dv_{CE}/dt has detrimental effects on motors ([3], [4]). These effects include voltage doubling at the motor windings with longer motor cables, high-step voltage changes across the stator end-windings, and others

While allowing the dv_{CE}/dt levels to be capped, the higher gate resistor value causes higher switching losses, and thus, reduces the efficiency of the converter. It also causes higher junction temperatures, reduces the lifetime of the power modules, and increases cooling requirements.

If, however, two gate resistors can be used, higher gate resistor values can be applied for turn-on at low currents and low temperatures, thus limiting dv_{CE}/dt levels. Also, lower gate resistor values can be used for turn-on at higher currents and temperatures to minimize losses.

On the other hand, the inductive turn-off overshoot may violate the power transistor's breakdown voltage V_{br}. The turn-off at short circuit or overcurrent is especially critical. It is possible to mitigate this risk by increasing the gate resistance for turn-off. This results in higher switching losses, which in turn increases junction temperatures and cooling requirements.

Fig. 1 shows a schematic diagram for the proposed gate drive circuit using the 2L-SRC driver IC 1ED3241MC12H. The driver IC has a single control input for fast or slow switching (/INF), and

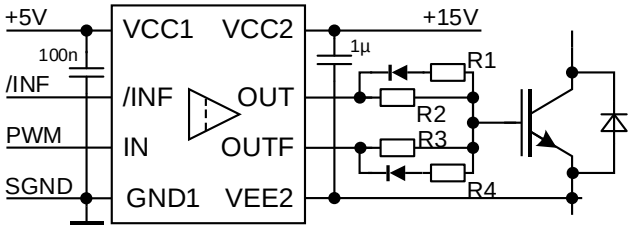

Fig. 1 Schematic diagram of the proposed dual-gate resistor gate-drive circuit using 1ED3241MC12H.

a separate control input for the PWM signal (IN). For fast operation, both output terminals OUT and OUTF switch at the same time in parallel, so that the IGBT gate is driven by the correlated combination of R1, R2, R3, and R4 in parallel. During slow operation, the IGBT is driven only by a combination of R1 and R1 in parallel with R2.

3 Testing environment

The inverter depicted in Fig. 2 served as the testing environment. The dimensions of the inverter are similar to those of commercially available inverters with a power density reaching 2.35 kW/dm³. The device operates a 100 A, 1200 V power module at the conditions given in Table 1.

Table 1 Key parameters and operating conditions of the inverter

Parameter	Value
Output power P_{OUT}	22 kW
Input voltage V_{IN}	3~, 400 V
Switching frequency f_p	4 kHz
Ambient temperature T_{amb}	25°C
Power factor Cos ϕ	~0.98
PWM scheme	Sine
Power module	FP100R12W3T7

The load is a three-phase R-L load with a particularly high resistive component, which results in a particularly high power factor. However, one can assume that the load current will not change during turn-on and turn-off.

The gate resistor values were selected in line with the double-pulse characterization results, aimed at keeping the inverter's dv_{CE}/dt below 5 V/ns for all operating conditions. This design rule takes into account the variation of temperatures and collector currents. Fig. 3 shows a diagram of the results of such a characterization obtained on a double-pulse test bench.

Fig. 2 Drives inverter for testing two-level slew-rate control

The test results shown in Fig. 3 indicate that the target of 5 V/ns is met at a gate resistance of e.g. $R_{G,on}$ = 3.7 Ω for turn-on at low currents of 10 A. Such double-pulse test results are usually too

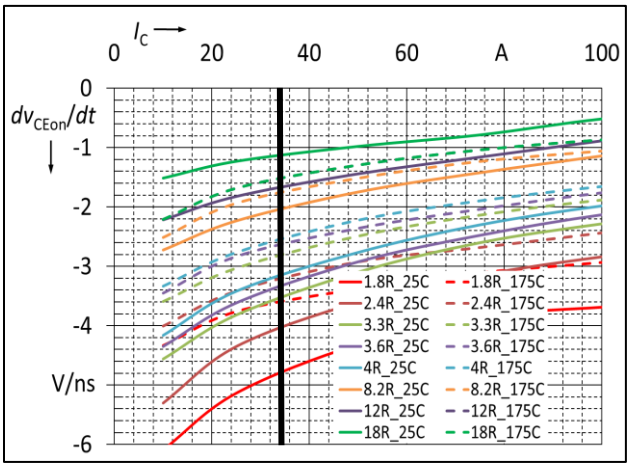

Fig. 3 Example of a turn-on dv_{CE}/dt diagram of the power module used measured on an optimized test bench.

optimistic for commercial applications, as the applications cannot be optimized in the same way as laboratory tests. Therefore, a value of 18 Ω was selected for slow turn-off. Double-pulse tests had been performed also for evaluating dv_{CE}/dt at turn-off resulted in the turn-off gate resistance $R_{G,off}$ at high currents. These two values would be the selected values for a conventional gate driver.

Selecting gate resistances for the two-level, slew-rate control gate driver also requires that the changeover point be defined, which is depicted in Fig. 3 by the black vertical line, at an instantaneous collector current of I_C = 35 A. The line divides the diagram into two sections, defining the transition between fast switching and slow switching. Each area has its own gate resistor value for reaching the target of 5 V/ns for turn-on and turn-off. These gate resistance values are given in Table 2.

Table 2 Gate resistor values for fast and slow switching

$R_{G,on,slow}$	18 Ω
$R_{G,on,fast}$	3.7 Ω
$R_{G,off,slow}$	11.2 Ω
$R_{G,off,fast}$	3.1 Ω

The resistances for $R_{G,on,slow}$ and $R_{G,off,slow}$ are selected to yield a very slow switching speed, which indicates EMI-friendly behavior. The resistances for fast switching ($R_{G,on,fast}$, $R_{G,off,fast}$) are considerably lower. Clearly, fast switching is more efficient when it is activated in the appropriate operating range. However, severe oscillations could be triggered, if such low gate resistances are used at very low currents [6].

4 Measurements

The measurements in this section compare the results of 3 different modes of operation:

- Mode 1: slow turn-on, fast turn-off
- Mode 2: fast turn-on, slow turn-off
- 2L-SRC-mode with
  - I_C < 35 A: slow turn-on, fast turn-off
  - I_C > 35 A: fast turn-on, slow turn-off

The correlated gate resistor value for each mode is given in Table 3. The 2L-SRC mode combines both mode 1 and mode 2 depending on the instantaneous phase current. Table 4 shows the recalculated physical resistor values of resistors R1 through R4.

Table 3 Effective gate resistor values for fast and slow switching

	Mode1	2L-SRC	Mode 2
$R_{G,on,slow}$	18 Ω	18 Ω	–
$R_{G,on,fast}$	–	3.7 Ω	3.7 Ω
$R_{G,off,slow}$	–	11.2 Ω	11.2 Ω
$R_{G,off,fast}$	3.1 Ω	3.1 Ω	–

An analysis of the switching speed is shown in Fig. 4. The upper graph in Fig. 4 depicts 1000 sampled waveforms of turn-on events, which represents a good variety of these occurrences. The sampling of the waveforms is synchronized to the load current frequency, so that switching waveforms are sampled randomly. The lower graph shows a histogram of the sampled waveforms structured in dv/dt clusters. Each bar represents the number of events with a width of 0.05 V/ns starting at 1 V/ns on the left side. As seen in Fig. 4, the transients range from 0.5 V/ns to 4.5 V/ns, and thus do not exceed 5 V/ns. The IGBT is therefore driven within the expected range of 5 V/ns.

Table 4 Selected gate resistor values R1, R2, R3, and R4

R1	30 Ω
R2	18 Ω
R3	51 Ω
R4	4.7 Ω

Fig. 5 is the synopsis of all three modes of operation at 2 different current levels, 4.5 A r.m.s. (left column) and 50 A r.m.s. (right column). The number of events at a given switching speed is depicted for turn-on (top row) and turn-off (bottom row). The results of 2L-SRC and mode 1 are in

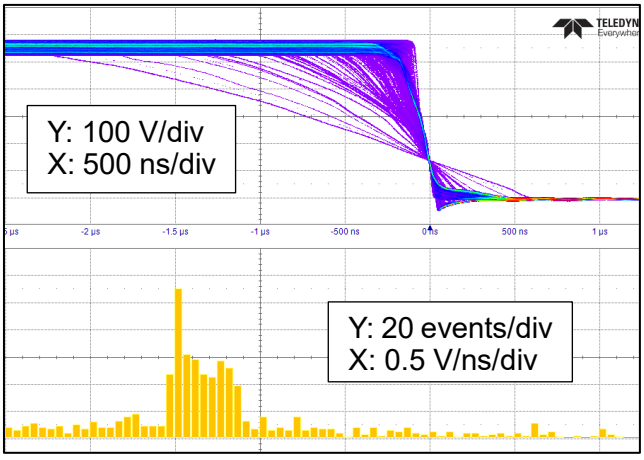

Fig. 4 Example of a set of turn-off waveforms (top) and histographic analysis of dv_{CE}/dt (bottom).

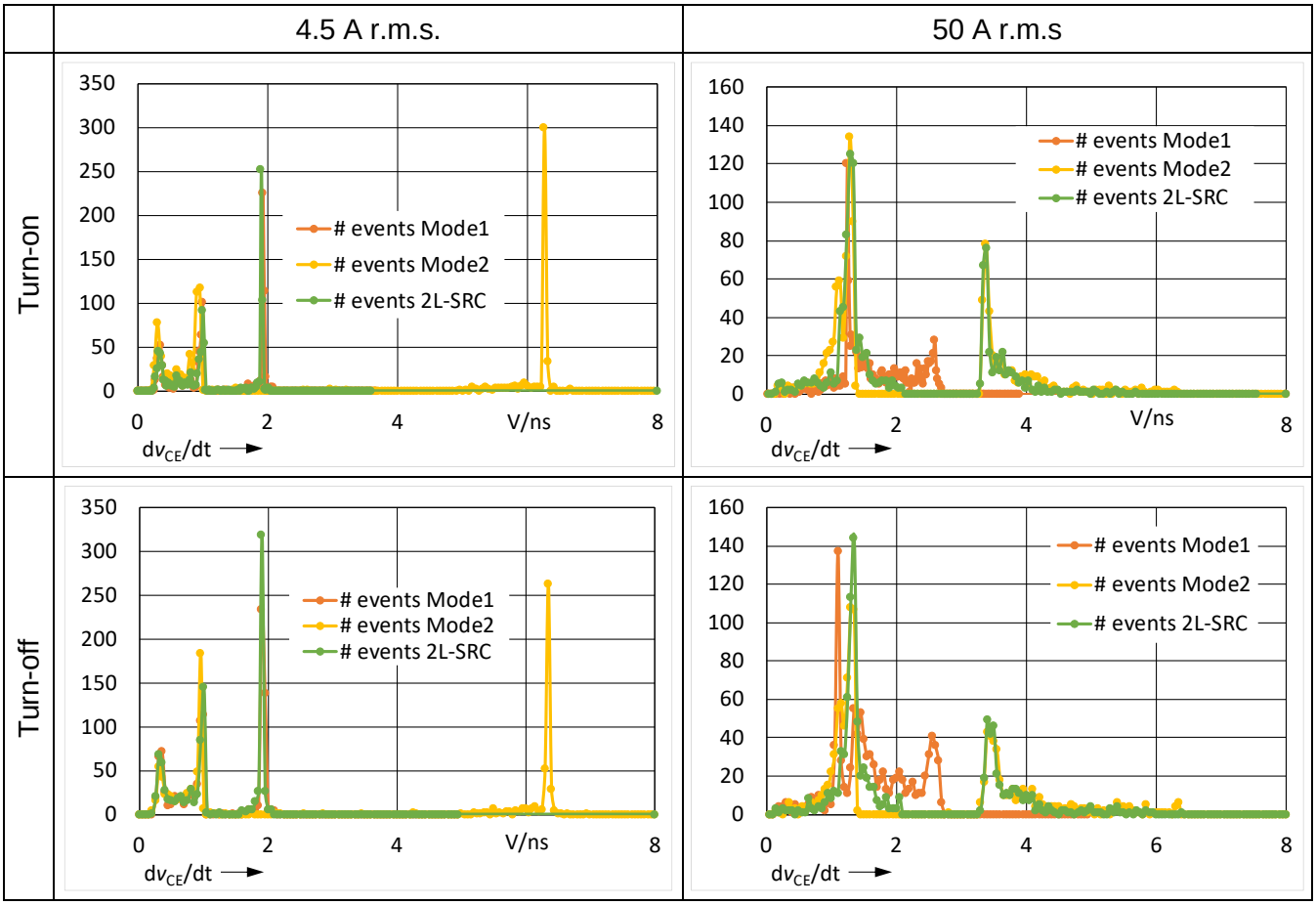

Fig. 5 Results of dv_{CE}/dt events for mode 1, mode 2 and 2L-SRC-mode (top: turn-on; bottom: turn-off; left: I_C = 4.5 A r.m.s.; right: I_C = 50 A r.m.s.)

principle similar, as 2L-SRC remains constantly in mode 1, as the change point of 35 A is never reached. While the faster switching mode 2 shows a clear peak at dv_{CE}/dt of more than 6 V/ns, the slower switching mode 1 and the 2L-SRC mode have a peak at lower than 2 V/ns. Both peaks at 4.5 A turn-on are active turn-on events. The turn-off diagram at 4.5 A can be interpreted below 1 V/ns in such a way that the instantaneous phase current is high enough to fully charge up the output capacitance of the IGBT after its turn-off. The peaks at 2 V/ns and above 6 V/ns are caused by the active turn-on of the opposite switch in that half bridge. The phase current is not high enough to charge the output capacitance up to the DC-link voltage. Thus, the turn-on of the opposite switch pulls up the collector-emitter voltage.

At high phase currents of 50 A r.m.s., the dv_{CE}/dt covers a larger range, with high peaks at 1 to 1.5 V/ns for all three modes, and a second peak above 3 V/ns for 2L-SRC and mode 2. The same interpretation regarding the second peak is possible at the turn-off with 50 A r.m.s., but at a lower level. The phase current is usually at levels that are sufficient to charge the output capacitance and only a few events had been measured above 3 V/ns.

As a summary, 2L-SRC operation of 1ED3241MC12H combines low dv_{CE}/dt rates at low current operation with faster and efficient dv_{CE}/dt rates at high load current operation.

Fig. 6 depicts the measured surface temperature of an IGBT and its freewheeling diode. The tests were performed with a thermocouple connected to the surface of the IGBT and diode in question. The fan speed was fixed at 80% of its maximum speed so that results would not be influenced by the fan's speed control. The solid lines represent the results during 2L-SRC operation mode, and the dashed lines represent the results of mode 1. The graph illustrates clearly that both the IGBT and the diode have the lowest temperature at high phase currents. Therefore, the diode is more than 12°C colder during 2L-SRC mode than during mode 1, and the IGBT is more than 7°C colder than during mode 1. The dotted line represents the temperatures at operation with mode 2. The temperatures of the IGBT and its freewheeling diode are still higher in mode 2 compared to the operation in 2L-SRC mode.

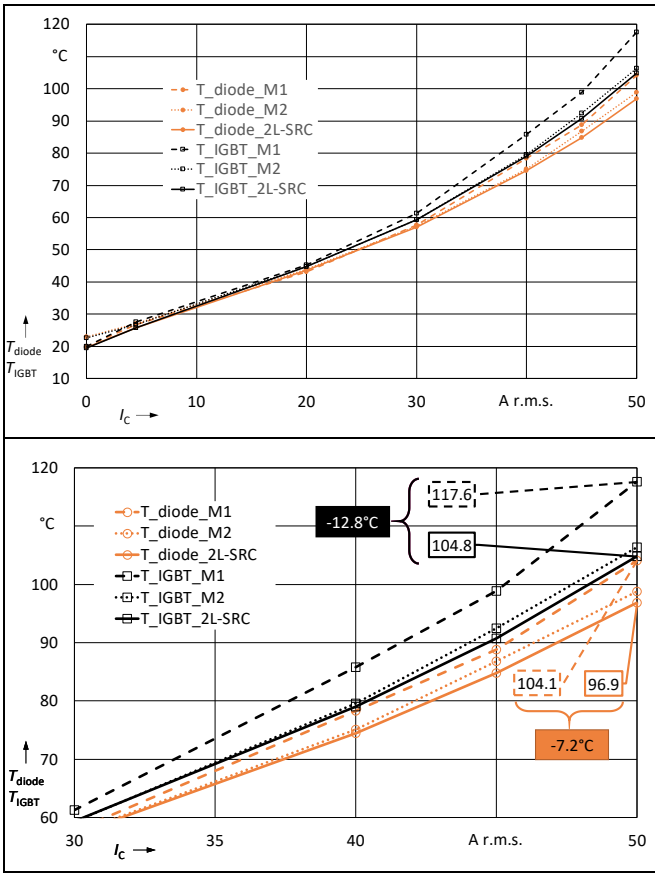

Fig. 6 Surface temperature of an IGBT and a diode of the inverter over full load range (top) and zoomed into upper phase-current range (bottom).

Fig. 7 shows a temperature measurement of the IGBT and diode surface during the load cycling of the inverter. The cycling parameters are given in detail in Table 5. The load cycle lasts 300 seconds at a high-load to low-load ratio of 1:4, resulting in low-load intervals of 240 seconds and high-load intervals of 60 seconds.

It can be seen that the temperature difference for mode 1 is highest and reaches ΔT_J = 32 °C, because the slow turn-on switching at high current dissipates more energy compared to mode 2, which uses lower gate resistance for turn-on. Thus, mode 2 dissipates less energy during high load operation resulting in ΔT_J = 29 °C. Fig. 7 depicts, again, that operating the inverter in 2L-SRC mode yields in the lowest temperature difference. 2L-SRC mode operates with higher gate resistance in low load, thus losses are slightly high during low load leading to a slightly higher temperature there. On the other side, 2L-SRC shows best performance during high load operation, therefore, the temperature difference is the lowest between low load and high load with ΔT_J = 27 °C.

Table 5 Load cycle parameters

High-load interval	60 s
Low-load interval	240 s
Cycle period	300 s
Low-load phase current	25 A r.m.s.
High-load phase current	45 A r.m.s.

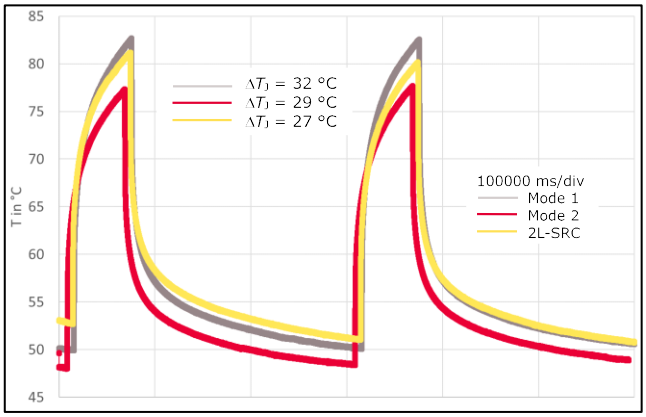

Fig. 7 Surface temperature of an IGBT and a diode of the inverter during load cycling in mode 1 (dashed), mode 2 (dotted) and 2L-SRC mode (solid).

5 Conclusion

The new 1ED3241MC12H gate driver IC, which has implemented the two-level slew-rate control, was evaluated in a 22 kW drive inverter. The 2L-SRC technique meets the requirements of smooth switching at low-phase current levels as well as efficient switching at high-phase current levels. The 2L-SRC is therefore ideally suited to successfully passing tests regarding conducted electro-magnetic interference, while achieving lowest losses compared to operating only in mode 1 or only in mode 2. In addition, the low losses enable cost-cutting measures to be taken like heat sink reduction.

The load-cycling test has proven that the 2L-SRC gate drive technique can considerably reduce the temperature stress on power electronic transistors and diodes. Reducing the operating temperature has also positive effects, for example, on the lifetime of the power module. When using the 2L-SRC gate driver IC 1ED3241MC12H, these effects are very easy to achieve.

6 References

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