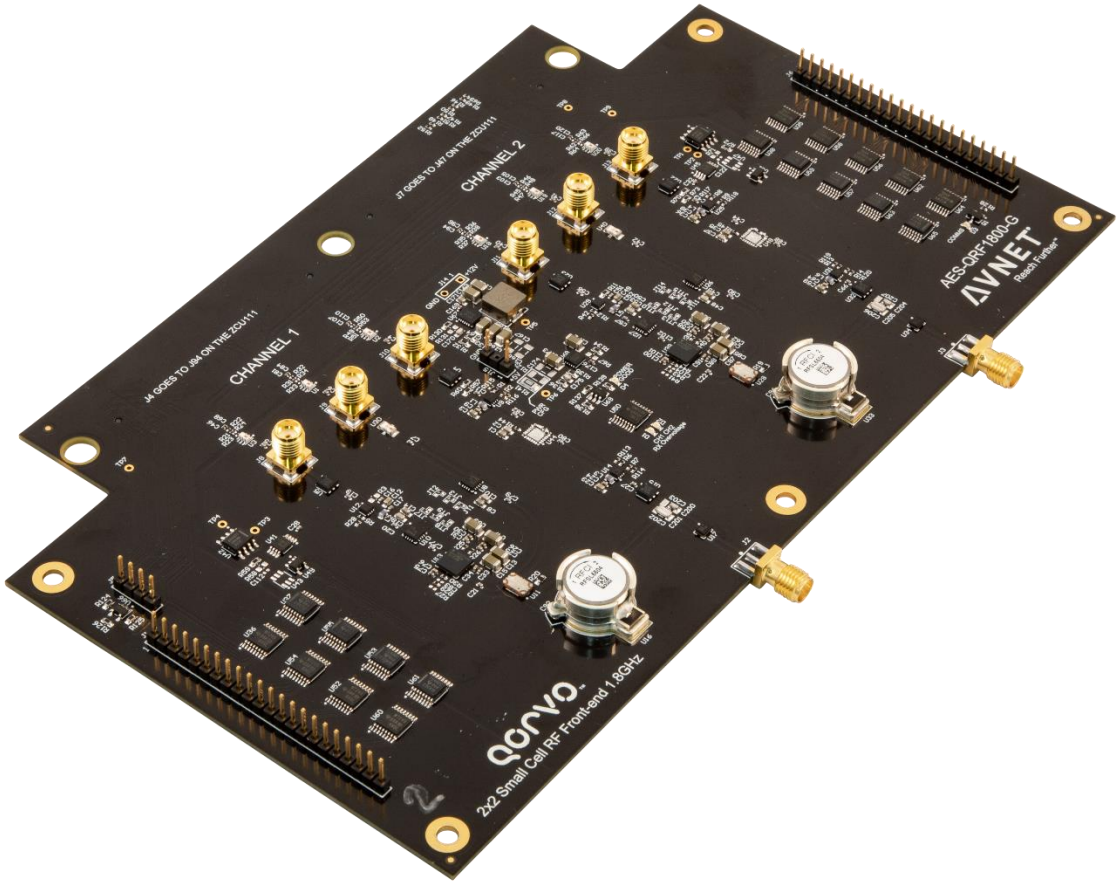

Qorvo 2-Channel RF Front-end 1.8 GHz Card Hardware User's Guide

Version 2.0

Contents

1 Document Control

Document Version: 2.0

Document Date: 22 March 2020

2 Version History

Version	Date	Comment
1.2	24 Oct 2019	Initial Release
1.3	11 Nov 2019	Added detail to Appendix A – Alternate Build
2.0	22 Mar 2020	Added Performance section. Updates for new Reverse Variant (RVS) configuration. Updated doc title to reflect RVS configuration.

3 Introduction

The Qorvo 2-Channel RF Front-end 1.8GHz Card mates with the Xilinx Zynq UltraScale+ RFSoC ZCU111 Evaluation Board, enabling direct RF-sampling radio prototype within the LTE 1800MHz frequency band.

The ZCU111 has an XCZU28DR Zynq RFSoC device with eight 12-bit ADC's that can operate up to 4GHZ and eight 14-bit DAC's that can operate up to 6.5GHz. The Qorvo uses 4 ADC channels and 2 DAC channels in order to support a 2-channel Frequency Division Duplex (FDD) configuration with observation paths for digital pre-distortion (DPD).

The Qorvo card (part # AES-LPA-QRF1800-RVS-G) may be purchased stand alone, or bundled in the Zynq® UltraScale+™ RFSoC Development Kit.

This document describes the features and use of the Qorvo RF card. For a description of the ZCU111, see the Xilinx User Guide, UG1271 [1].

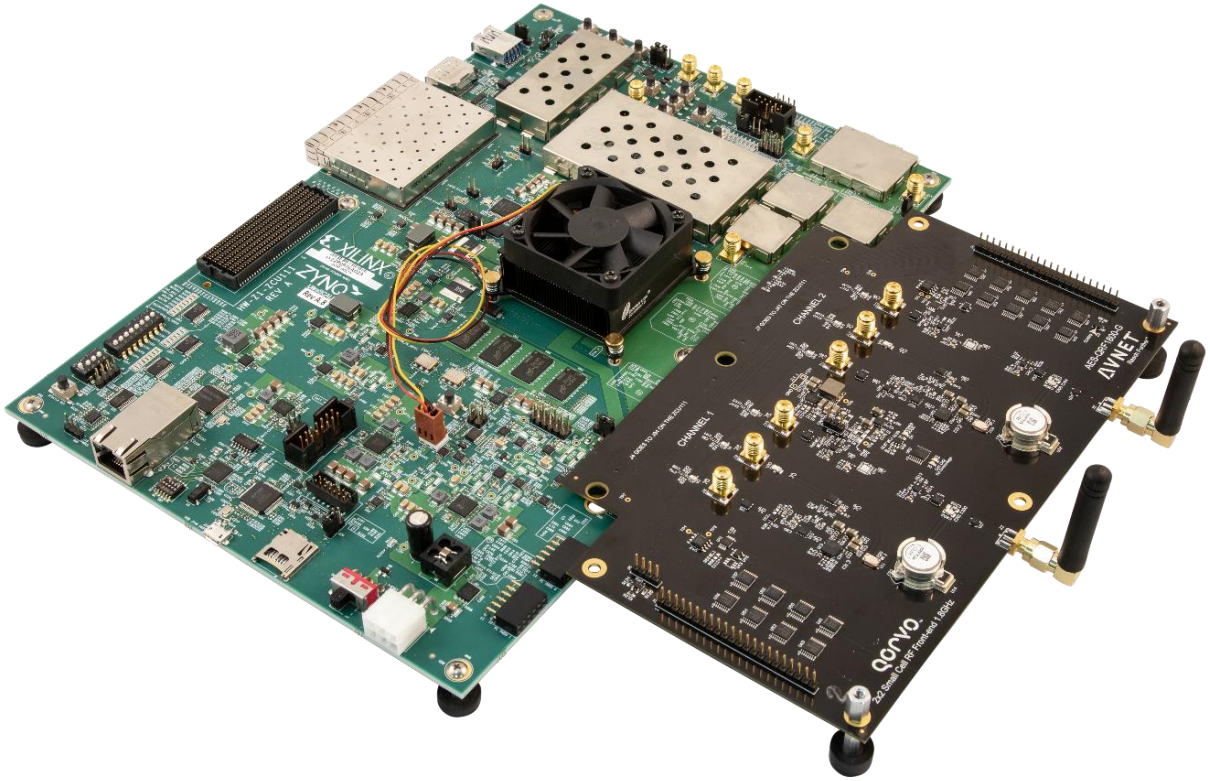

Figure 1 – The Qorvo RF Card plugged into a Xilinx ZCU111 development board

3.1 Zynq UltraScale+ RFSoC Development Kit

The Avnet Zynq UltraScale+ RFSoC Development Kit enables system architects to explore the entire signal chain from antenna to digital using tools from MathWorks and industry-leading RF components from Qorvo. We extend the functionality of the Xilinx Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit by adding a Qorvo 2-Channel RF front-end 1.8 GHz Card for over-the-air transmission, plus native connection to MATLAB® & Simulink® with Avnet's RFSoC Explorer® application.

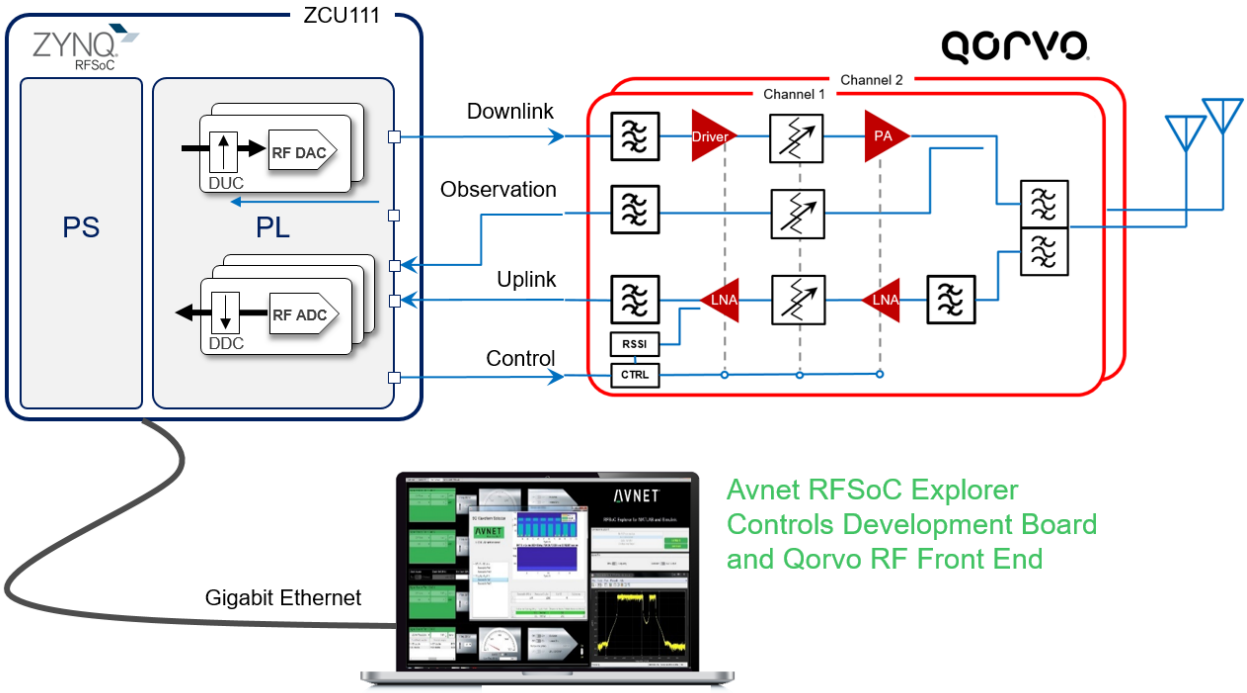

Figure 2 – Using the Avnet RFSoC Explorer tool for MATLAB and Simulink

3.2 Glossary

Term	Definition
ADC	Analog to Digital Converter
BAW	Bulk Acoustic Wave
BOM	Bill of Materials
CE	European Conformity marking
DAC	Digital to Analog Converter
dB	Decibel
DPD	Digital Pre-Distortion
DSA	Digital Step Attenuator
EEPROM	Electrically Erasable Programmable Read-only Memory
FCLK	Fabric Clock
FCC	Federal Communications Commission
FDD	Frequency Division Duplexing
GPIO	General Purpose Input / Output
I2C	Inter-Integrated Circuit interface
IC	Industry Canada (certification)
IPMI	Intelligent Platform Management Interface
LNA	Low Noise Amplifier
LTE	Long Term Evolution 4G telecommunications standard
PA	Power Amplifier
PL	Zynq UltraScale+ RFSoC Programmable Logic
PS	Zynq UltraScale+ RFSoC Processing System
RF	Radio Frequency
RFMC	RF Mezzanine Card
RFSoC	Radio Frequency System-on-Chip
RMS	Root Mean Square
Rx	Receive
SAM	Serial Addressable Mode
SPI	Serial Peripheral Interface
Tx	Transmit
TCL	Tool Command Language

3.3 Reference Documents

[1] ZCU111 Evaluation Board User Guide

[2] AES-QRF1800-G Schematic for Qorvo 2-Channel RF Front-end 1.8 GHz Card

[3] Xilinx Vivado Design Suite

[4] Xilinx Software Development Kit

[5] Zynq UltraScale+ RFSoC RF Data Converter 2.1 LogiCORE IP Product Guide (PG269)

[6] Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics (DS926)

4 Architecture and Features

This section provides a summary of the board features.

4.1 List of Features

- Two channels, each with Tx, Rx and DPD (Digital Pre Distortion) Observation path
- Default tuning to LTE Band 3 / 1800 MHz FDD System
- Alternate tuning options available as BOM variants
- OTA testing as single channel UE, base station, or loopback
- Channel 1: TX @ 1842.5MHz, RX @ 1747.5MHz
- Channel 2: TX @ 1747.5MHz, RX @ 1842.5MHz
- Digital Step Attenuators in TX, RX, and DPD paths
- 75 MHz bandpass filters in TX and RX paths
- 180 MHz TX observation bandpass filters for Digital Pre-distortion (DPD)
- QPA9903 0.5 Watt High-Efficiency Linearizable Power Amplifiers
- QPL9096 Ultra Low-Noise Bypass LNAs
- RMS Power Detector & Overvoltage protection circuit

4.2 Block Diagram

The Avnet Qorvo 2-Channel RF front-end 1.8 GHz (AES-LPA-QRF1800-RVS-G) is a two channel Frequency Division Duplex (FDD) RF front end operating in LTE Band 3.

Channel 1 and Channel 2 topologies, shown in the diagram below, are identical. The frequency plan for the two channels are symmetrical as summarized below.

- Channel 1: TX @ 1842.5MHz, RX @ 1747.5MHz
- Channel 2: TX @ 1747.5MHz, RX @ 1842.5MHz

NOTE: a previous version of this card (AES-LPA-QRF1800-G) was configured with identical frequency plan for both channels allowing a 2x2 MIMO small cell configuration.

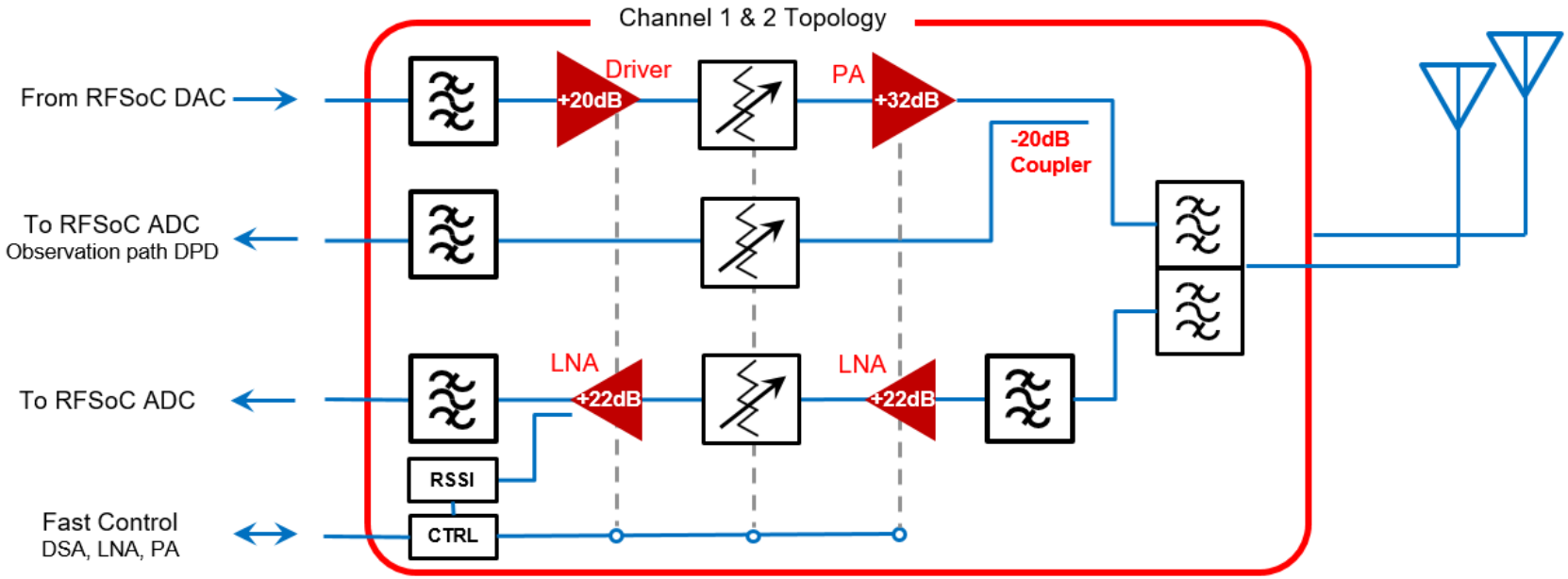

Figure 3 – Block Diagram

5 Functional Description

The following sections provide brief descriptions of each feature provided on the board.

5.1 ZCU111 Interface

Two Samtec RFMC (RF Mezzanine Card) LPAM connectors on the Qorvo RF card plug into the corresponding LPAF connectors on the ZCU111. These connectors carry the analog I/O associated with RFSoC, as well as the digital control signals.

The diagram below illustrates how components inside the ZU28 are connected to the daughter card via these LPAF/LPAM connectors.

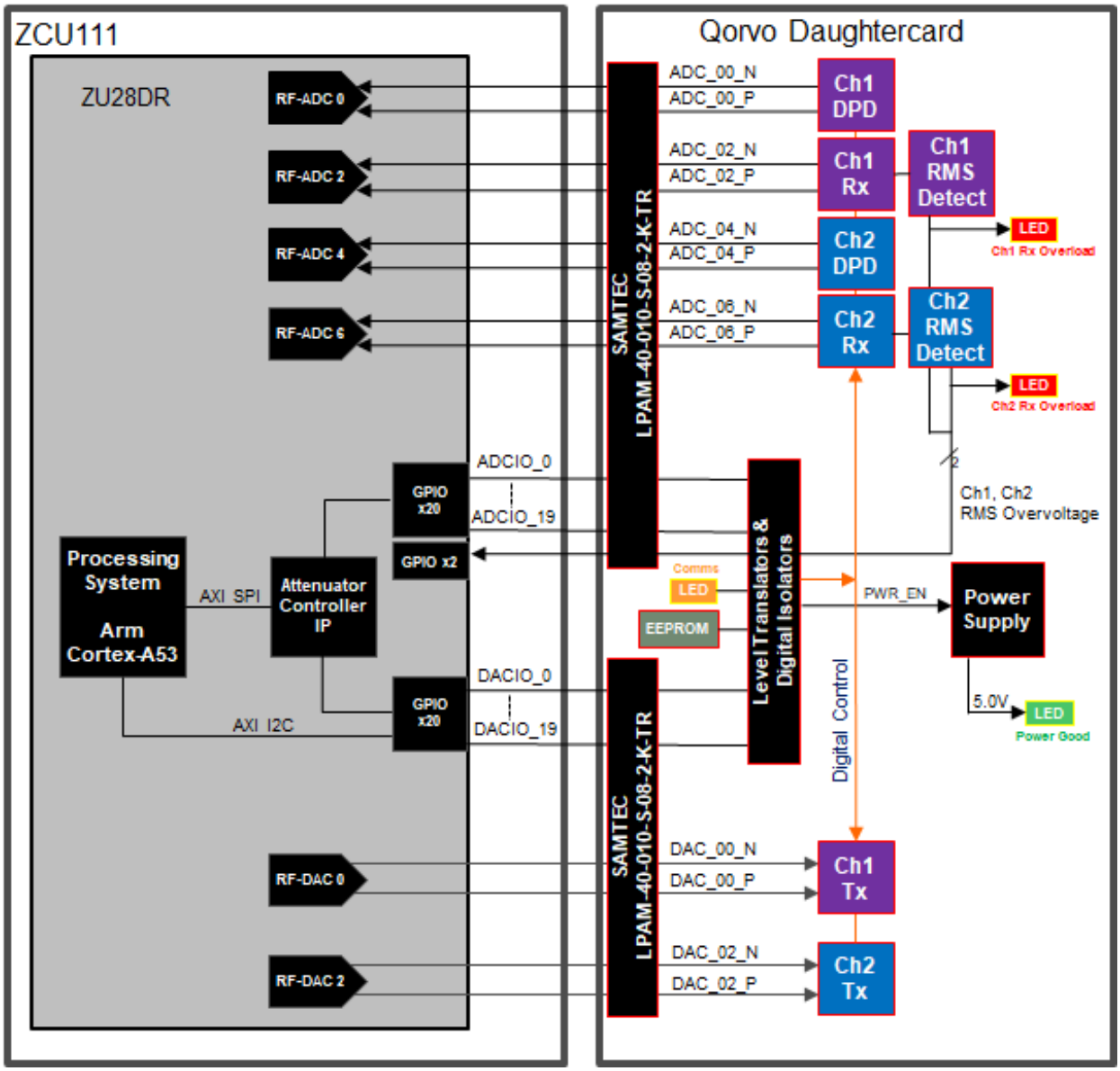

Figure 4 – Controlling the Qorvo card from the RFSoC Processing System

5.2 Digital Isolation

The ZCU111 has digital components running at high frequencies, while the Qorvo RF card may be sensitive to minor disturbances. It is therefore desirable to isolate the ZCU111 from RF noise and to isolate RF signals on the Qorvo card from digital noise sources.

There are a number of possible power configurations, as discussed under Power Options. When the ZCU111 and Qorvo card are powered separately as in the diagram below, the digital ground from the ZCU111, DGND, is not connected to the Qorvo card's RF ground, RGND. **Note that this is not the factory default power configuration and that here external 5V to the Qorvo card requires R140 and R141 to be removed**.

The digital isolators used to achieve separation are the Texas Instruments devices:

- ISO7140 (4 channels forward) and
- ISO7141 (3 channels forward, 1 channel back).

The Qorvo attenuators use 5V logic. The isolators can level shift between 3V and 5V. Since the ZCU111 Zynq banks used for digital I/O are configured for 1.8V, separate level translators are used to convert the Zynq signals to/from 3.3V, while the isolators level shift between 3.3V and 5V.

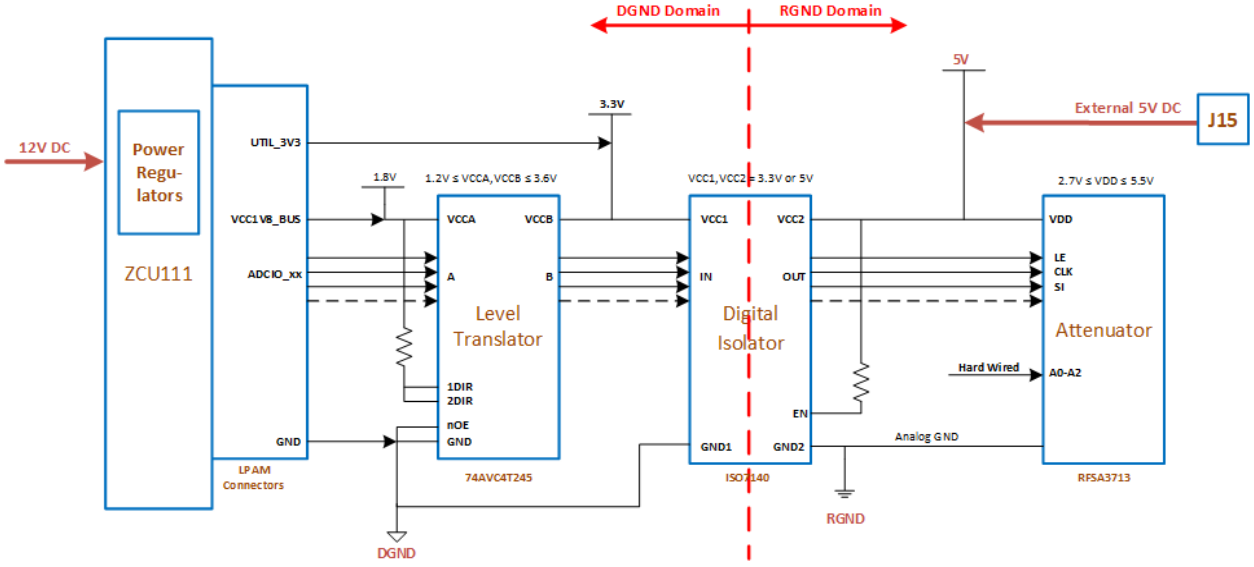

Figure 5 – External 5V configuration and Isolators for Separate DGND and RGND Domains

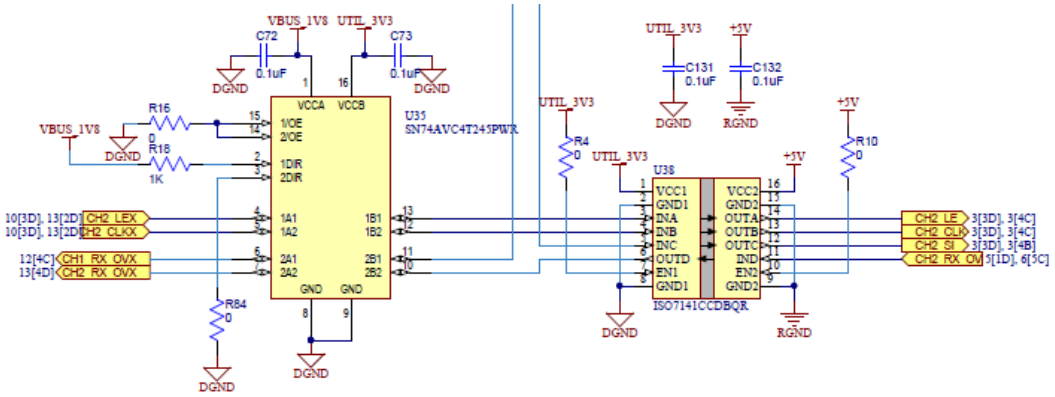

Figure 6 – Example Level Translation and Digital Isolation

5.3 Power Options

The power diagram in the previous section (Digital Isolation) is not the default configuration. It shows the Qorvo card powered with an external 5V supply. For demonstrations and development it is mostly convenient to not have a second power supply and to **power the Qorvo card directly from the ZCU111. This is the default configuration** and in this case DGND and RGND are not separated, but are connected through a resistor, **R140, which must be removed for any the "external power" configuration**.

The diagram below shows the default configuration, where the Qorvo card is powered from the ZCU111 and R140 and R141 are placed. Note that since DGND and RGND are connected, much of the isolation is effectively lost. In this case 5V is generated by an on-board buck converter and LDO.

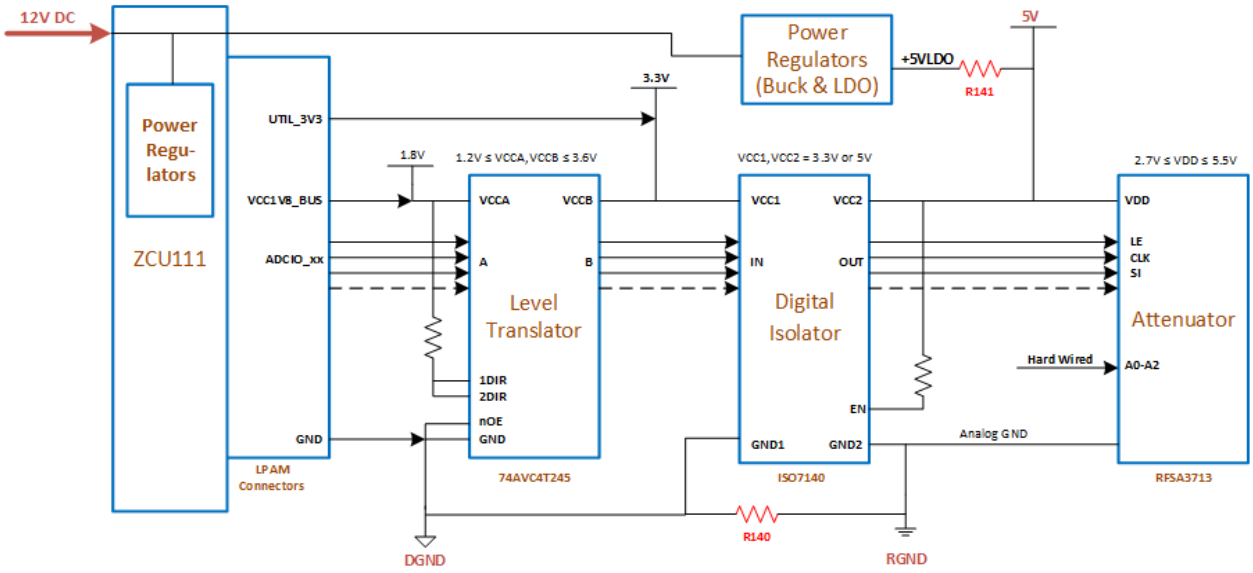

Figure 7 – Factory Default Configuration with 12V from the ZCU111

It is also possible to power the Qorvo card stand-alone on the bench, from either 12V or 5V. The power options all require various resistor configurations. The table on sheet 11 of the schematic [2] clearly specifies which resistors need to be placed or removed for each option.

	Operation	R129	R140	R141	R131	Power Source
Default →	ZCU111	DNP	0	0	DNP	12V on J4
	Stand Alone w/ 12V	DNP	DNP	0	DNP	12V on J14
	Stand Alone w/ 5V	DNP	DNP	DNP	X	5V on J15
	ZCU111 w/ external 5V	DNP	DNP	DNP	X	5V on J15
	ZCU111 w/ external 12V	NOT ALLOWED				

Figure 8 – Possible Power Configurations

5.4 Attenuators Digital Step Attenuator (DSA) Devices Control Interfaces

There are both parallel and serial Digital Step Attenuator (DSA) devices on this board.

5.4.1 Parallel DSA Control Interface

The two Rx attenuators are Qorvo TQP4M9071 devices.
https://www.qorvo.com/products/p/TQP4M9071

These devices can operate from DC to 4GHz. The TQP4M9071 has a 6-bit parallel interface where one LSB presents 0.5dB of attenuation. A parallel control interface is much faster than a serial interface. For procedures like Automatic Gain Control (AGC) it is important that there is a fast response time and that the attenuation can be updated rapidly. This is why parallel attenuators are being used in the receive path.

5.4.2 Serial DSA Control Interface

There are not enough GPIO available for a 6-bit interface to all 6 DSA's. It is not as important to change the attenuation in the Tx or DPD paths as it is for the receive path. Therefore the Tx and DPD attenuators are the Qorvo RFSA3713 (https://www.qorvo.com/products/p/RFSA3713), which uses a proprietary serial interface.

The RFSA3713 can operate from 5MHz to 6GHz. It is a 7-bit attenuator, where each step represents 0.25dB of attenuation. The maximum clock rate for the serial control interface is 25MHz. In the reference design this clock is 5MHz, and it is created by dividing down a 100MHz fabric clock (FCLK) from the PS by 10 and then using this to run the state machine.

The serial interface used by the RFSA3713 is 3-wire "Serial Addressable Mode" (SAM). There is a separate serial bus for each of the two channels and the address of the attenuator is specified by the hard wiring on its address pins.

Serial Addressable Mode Address Word Truth Table

Address Word								Address Setting
A7	A6	A5	A4	A3	A2 (MSB)	A1	A0	
X	X	X	X	X	L	L	L	000
X	X	X	X	X	L	L	H	001
X	X	X	X	X	L	H	L	010
X	X	X	X	X	L	H	H	011
X	X	X	X	X	H	L	L	100
X	X	X	X	X	H	L	H	101
X	X	X	X	X	H	H	L	110
X	X	X	X	X	H	H	H	111

Serial Addressable Mode Timing Diagram

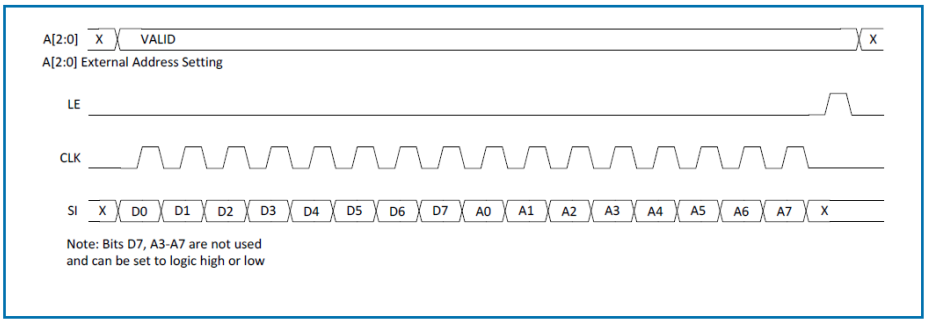

Figure 9 – Addressing and Timing for the Serial Addressable Mode Interface

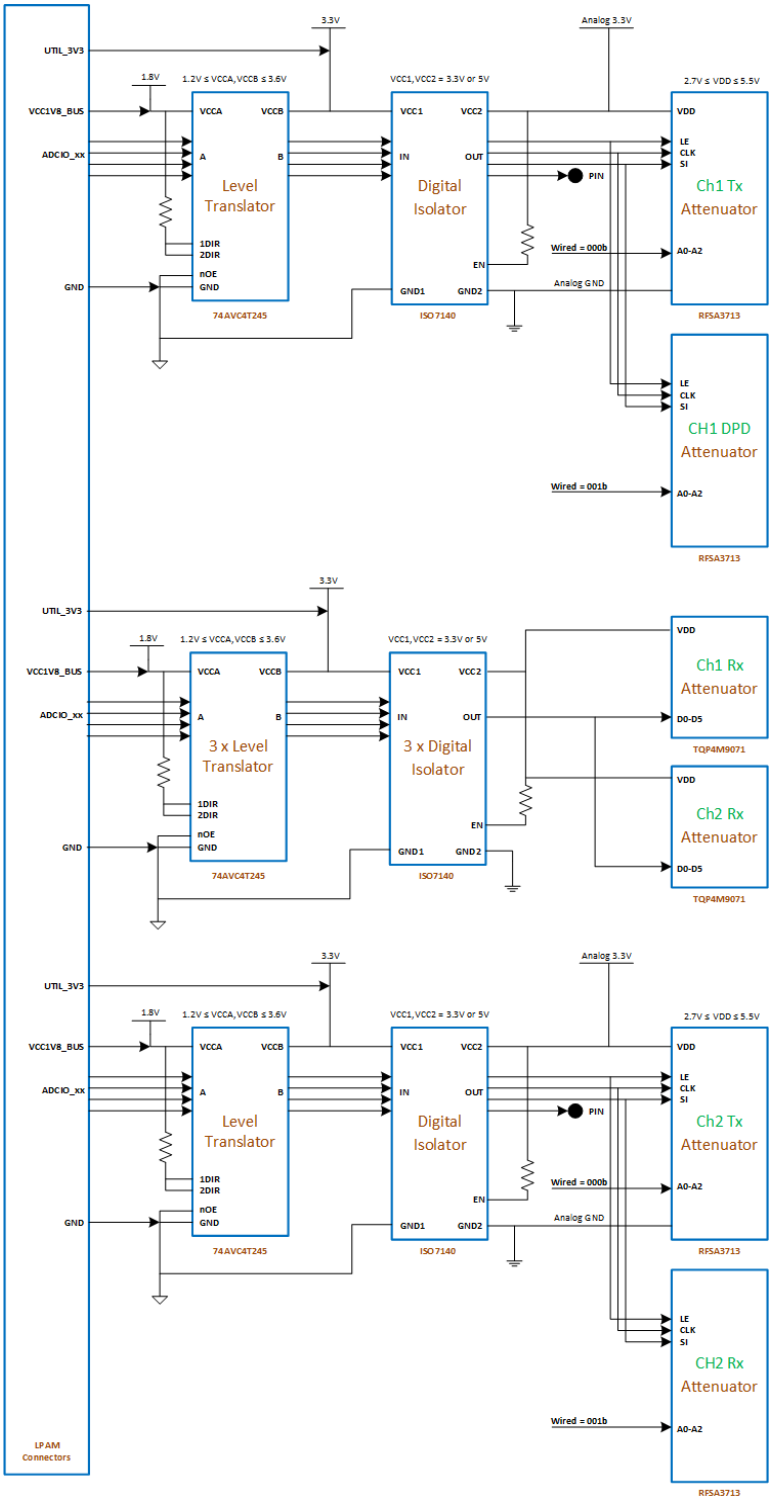

Figure 10 – Attenuator Control Interfaces

The programmable logic and software in the Avnet reference design implements the serial protocol for these attenuators. See 5.5.

The image below shows data being clocked out to one of the attenuators on the Channel 1 serial bus. The serial clock here is 5MHz. The first signal, LE, is the latch enable signal, which toggles after the serial data in (SI) has been clocked in.

Figure 11 – Scope Capture of SAM signals for Writing to an Attenuator

5.5 Rebuilding the Reference Design

The Avnet reference design project for the **Avnet RFSoC Kit** is on GitHub. This reference design is for the ZCU111 interfaced with the Qorvo card. It is a Vivado project that can be re-built from sources in the online repository, using the instructions that are also in the repository.

The GitHub repository is at https://github.com/AvnetDev/qorvo1800

Note that **the AvnetDev repository is not public**. Developers may contact Avnet for access, i.e. a user name and password.

Once access is granted by logging in, the content can be browsed or it can be cloned to a local directory.

Under Linux the tip version of the repository can be cloned with:
git clone https://github.com/AvnetDev/qorvo1800.git

Under Windows the command to clone the tip version of the repository would be:
git clone git://github.com/AvnetDev/qorvo1800.git

For Windows it is important that a reasonably recent version of the Git executable is being used. From a command prompt, the **git version** command can be used. At the time of this document, the latest version is 2.22.0.
The latest version can be installed from https://git-scm.com/download/win.

At the time of this document, the latest code is in the "revB" directory and the build instructions are in the file https://github.com/AvnetDev/qorvo1800/blob/master/revB/zcu111_build_instr.txt.

These instructions will direct the user to unzip the repository to a local directory and to then run the TCL script from the TCL command window in Vivado. This will re-create and then build the project.

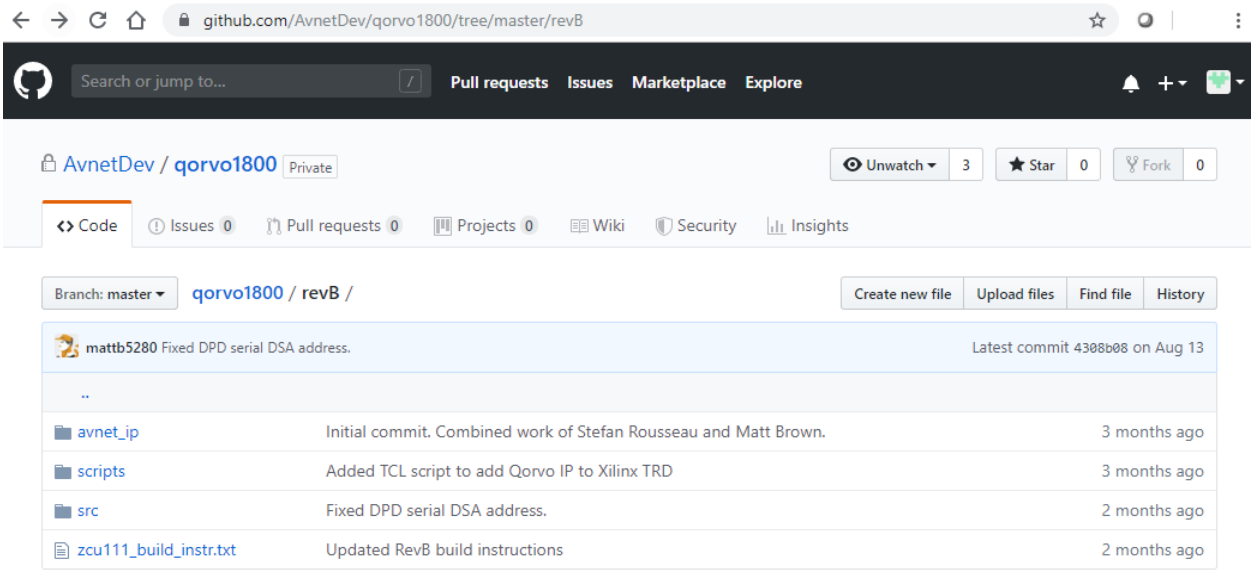

Figure 12 – GitHub Repository for the Avnet Reference Design

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5.6 SPI Controller

The programmable logic for controlling the attenuators, the power supply and the COMMS LED on the daughter card has an SPI interface to the processor system. This allows user software in the Zynq Processor System (PS) to access the Programmable Logic (PL) through AXI-4 to control the DSA's and other digital signals. This can be done through a serial port or, ultimately, from MathWorks.

The Avnet reference design (see 5.5) software implementation uses the **spidev** Linux driver. The Vivado project instantiates an axi_quad_spi component and the custom qorvo_spi component that maps the interface to the control signals.

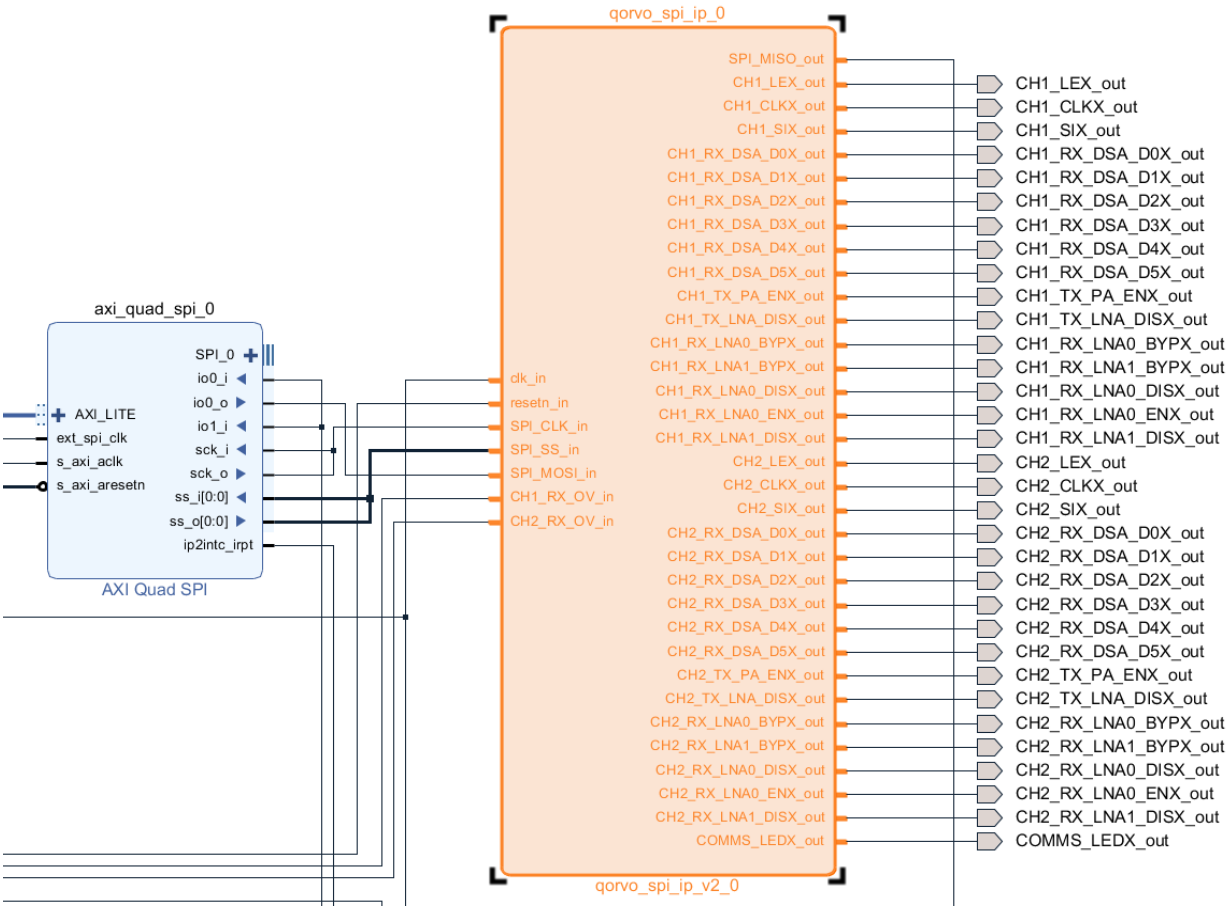

Figure 13 – The Qorvo Card SPI Interface in the Vivado Project

Most of the signals driven from this interface behave like typical GPIO in that the user can directly drive them to logic '0' or '1' levels. There are two serial interfaces for the Tx and DPD attenuators in the two channels though. This interface is not SPI, but a similar write-only interface called "Serial Addressable Mode" (SAM). See 5.4.2.

5.7 GPIO Assignments

There are 40 digital control signals available through RFMC LPAF connectors J47 and J94 on ZCU111. They are the 1.8V ADCIO (20 signals on J47) and DACIO (20 signals on J94) lines from the RFSoC ZU+ device.

The table below shows how the GPIO pins have been assigned. Note that the Zynq firmware pin number assignments can be found in the Vivado project file **qorvo_spi_slave.xdc**. This file can be found in the Avnet reference design (see 5.5) inside the pl\qorvo1800\revB\src folder.

Table 1 – Assignments for Digital GPIO from the ZCU111

ZCU111 Signal	Zynq Pin #	ZCU111 LPAF Pin	Qorvo Card Signal	Qorvo Card Test Pin	Description
DACIO_00	A9	J94 pin A37	I2C_ SCLX	J5 pin 3	I2C clock for EEPROM
DACIO_01	A10	J94 pin A39	I2C_ SDAX	J5 pin 2	I2C data for EEPROM
DACIO_02	A6	J94 pin B36	CH1_RX_LNA0_BYPX	J1 pin 13	Ch1 Rx LNA0 Bypass
DACIO_03	A7	J94 pin B38	CH1_RX_LNA1_BYPX	J1 pin 14	Ch1 Rx LNA1 Bypass
DACIO_04	A5	J94 pin B40	CH1_RX_LNA0_DISX	J1 pin 15	Ch1 Rx LNA0 Disable
DACIO_05	B5	J94 pin C37	CH1_RX_LNA0_ENX	J1 pin 16	Ch1 Rx LNA0 Enable
DACIO_06	C5	J94 pin C39	CH1_RX_OVX		Ch1 Rx Over-voltage
DACIO_07	C6	J94 pin D36	CH1_TX_PA_ENX	J1 pin 11	Ch1 Tx PA Enable
DACIO_08	B9	J94 pin D38	CH1_RX_LNA1_DISX	J1 pin 17	Ch1 Rx LNA1 Disable
DACIO_09	B10	J94 pin D40	CH1_TX_LNA_DISX	J1 pin 12	Ch1 Tx LNA Disable
DACIO_10	B7	J94 pin E37	CH1_LEX	J1 pin 2	Ch1 Tx and DPD DSA Serial Latch Enable
DACIO_11	B8	J94 pin E39	CH1_CLKX	J1 pin 3	Ch1 Tx and DPD DSA Serial Clock
DACIO_12	D8	J94 pin F36	CH1_SIX	J1 pin 4	Ch1 Tx and DPD DSA Serial Data
DACIO_13	D9	J94 pin F38	CH1_RX_DSA_D0X	J1 pin 5	Ch2 Rx DSA Data bit 0
DACIO_14	C7	J94 pin F40	CH1_RX_DSA_D1X	J1 pin 6	Ch2 Rx DSA Data bit 1
DACIO_15	C8	J94 pin G37	CH1_RX_DSA_D2X	J1 pin 7	Ch2 Rx DSA Data bit 2
DACIO_16	C10	J94 pin G39	CH1_RX_DSA_D3X	J1 pin 8	Ch2 Rx DSA Data bit 3
DACIO_17	D10	J94 pin H36	CH1_RX_DSA_D4X	J1 pin 9	Ch2 Rx DSA Data bit 4
DACIO_18	D6	J94 pin H38	CH1_RX_DSA_D5X	J1 pin 10	Ch2 Rx DSA Data bit 5
DACIO_19	E7	J94 pin H40		TP7	Spare
ADCIO_00	AP5	J47 pin A2	COMMS_LEDX	J6 pin 18	Yellow LED control
ADCIO_01	AP6	J47 pin A4		TP8	Spare
ADCIO_02	AR6	J47 pin B1	CH2_RX_LNA0_BYPX	J6 pin 13	Ch2 Rx LNA0 Bypass

ZCU111 Signal	Zynq Pin #	ZCU111 LPAF Pin	Qorvo Card Signal	Qorvo Card Test Pin	Description
ADCIO_03	AR7	J47 pin B3	CH2_RX_LNA1_BYPX	J6 pin 14	Ch2 Rx LNA1 Bypass
ADCIO_04	AV7	J47 pin B5	CH2_RX_LNA0_DISX	J6 pin 15	Ch2 Rx LNA0 Disable
ADCIO_05	AU7	J47 pin C2	CH2_RX_LNA0_ENX	J6 pin 16	Ch2 Rx LNA0 Enable
ADCIO_06	AV8	J47 pin C4	CH2_RX_OVX		Ch2 Rx Over-voltage
ADCIO_07	AU8	J47 pin D1	CH2_TX_PA_ENX	J6 pin 11	Ch2 Tx PA Enable
ADCIO_08	AT6	J47 pin D3	CH2_RX_LNA1_DISX	J6 pin 17	Ch2 Rx LNA1 Disable
ADCIO_09	AT7	J47 pin D5	CH2_TX_LNA_DISX	J6 pin 12	Ch2 Tx LNA Disable
ADCIO_10	AU5	J47 pin E2	CH2_LEX	J6 pin 2	Ch2 Tx and DPD DSA Serial Latch Enable
ADCIO_11	AT5	J47 pin E4	CH2_CLKX	J6 pin 3	Ch2 Tx and DPD DSA Serial Clock
ADCIO_12	AU3	J47 pin F1	CH2_SIX	J6 pin 4	Ch2 Tx and DPD DSA Serial Data
ADCIO_13	AU4	J47 pin F3	CH2_RX_DSA_D0X	J6 pin 5	Ch2 Rx DSA Data bit 0
ADCIO_14	AV5	J47 pin F5	CH2_RX_DSA_D1X	J6 pin 6	Ch2 Rx DSA Data bit 1
ADCIO_15	AV6	J47 pin G2	CH2_RX_DSA_D2X	J6 pin 7	Ch2 Rx DSA Data bit 2
ADCIO_16	AU1	J47 pin G4	CH2_RX_DSA_D3X	J6 pin 8	Ch2 Rx DSA Data bit 3
ADCIO_17	AU2	J47 pin H1	CH2_RX_DSA_D4X	J6 pin 9	Ch2 Rx DSA Data bit 4
ADCIO_18	AV2	J47 pin H3	CH2_RX_DSA_D5X	J6 pin 10	Ch2 Rx DSA Data bit 5
ADCIO_19	AV3	J47 pin H5		TP9	Spare

5.8 EEPROM and I2C Interface

U66 on the Qorvo card is 1Kbit EEPROM from Microchip. It uses a 2-wire I2C interface. The purpose of this device is to store a board ID so that software can distinguish this board from other daughter card. It would also be possible to store a device ID and/or calibration parameters that are unique to a specific board's serial number.

Currently this functionality has not been implemented yet.

Avnet has Intelligent Platform Management Interface (IPMI) EEPROMs for identification on some boards. Inside the Avnet reference design (see 5.5), the RFTOOL codebase includes modules for I2C communication.

I2C can be accessed from the ZCU111 through the LPAM/LPAF connectors. During production the EEPROM can also be programmed from the I2C test header, J5.

Table 2 – I2C Header J5 Pin Assignments

Pin #	Signal	Description
1	VBUS_1V8	1.8V
2	I2C_ SDAX	I2C data
3	I2C_ SCLX	I2C clock
4	DGND	Digital Ground

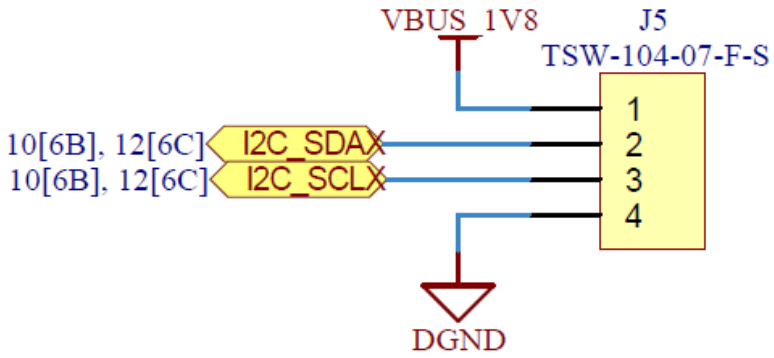

Figure 14 – The I2C Test Header

5.9 Digital Test Pins

There are two test header strips, J1 and J6, which can be used to drive the digital control signals from an external source.

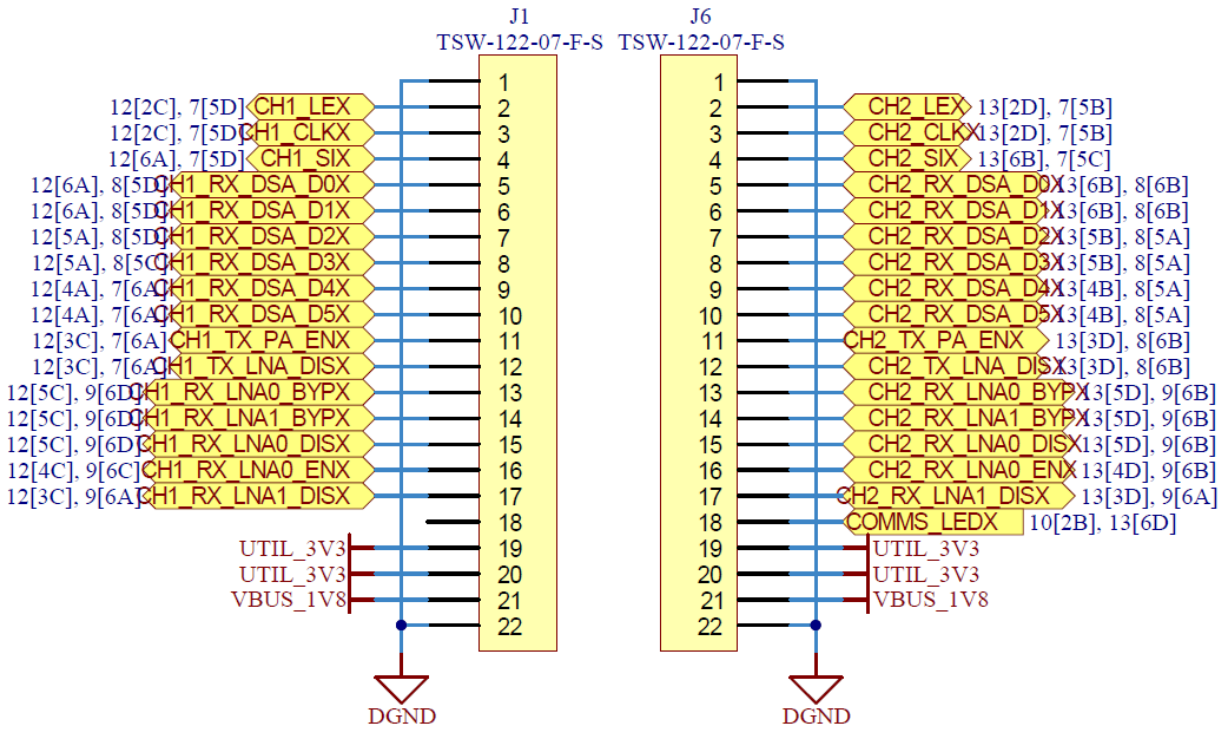

Figure 15 – Digital Test Pin Header Strips

The reason for having 3.3V on multiple pins is that when the card is powered externally on one 3.3V pin, the second 3.3V pin may be used to jumper between pins 20 and 21 in order to short out the level translator.

Table 3 – Test Header Pin Assignments

Pin #	Signal	Description
J1 pin 1	DGND	Digital Ground
J1 pin 2	CH1_LEX	Ch1 Tx and DPD DSA Serial Latch Enable
J1 pin 3	CH1_CLKX	Ch1 Tx and DPD DSA Serial Clock
J1 pin 4	CH1_SIX	Ch1 Tx and DPD DSA Serial Data
J1 pin 5	CH1_RX_DSA_D0X	Ch2 Rx DSA Data bit 0
J1 pin 6	CH1_RX_DSA_D1X	Ch2 Rx DSA Data bit 1
J1 pin 7	CH1_RX_DSA_D2X	Ch2 Rx DSA Data bit 2
J1 pin 8	CH1_RX_DSA_D3X	Ch2 Rx DSA Data bit 3

Pin #	Signal	Description
J1 pin 9	CH1_RX_DSA_D4X	Ch2 Rx DSA Data bit 4
J1 pin 10	CH1_RX_DSA_D5X	Ch2 Rx DSA Data bit 5
J1 pin 11	CH1_TX_PA_ENX	Ch1 Tx PA Enable
J1 pin 12	CH1_TX_LNA_DISX	Ch1 Tx LNA Disable
J1 pin 13	CH1_RX_LNA0_BYPX	Ch1 Rx LNA0 Bypass
J1 pin 14	CH1_RX_LNA1_BYPX	Ch1 Rx LNA1 Bypass
J1 pin 15	CH1_RX_LNA0_DISX	Ch1 Rx LNA0 Disable
J1 pin 16	CH1_RX_LNA0_ENX	Ch1 Rx LNA0 Enable
J1 pin 17	CH1_RX_LNA1_DISX	Ch1 Rx LNA1 Disable
J1 pin 18		Unused
J1 pin 19	UTIL_3V3	3.3V
J1 pin 20	UTIL_3V3	3.3V
J1 pin 21	VBUS_1V8	1.8V
J1 pin 22	DGND	Digital Ground
J6 pin 1	DGND	Digital Ground
J6 pin 2	CH2_LEX	Ch2 Tx and DPD DSA Serial Latch Enable
J6 pin 3	CH2_CLKX	Ch2 Tx and DPD DSA Serial Clock
J6 pin 4	CH2_SIX	Ch2 Tx and DPD DSA Serial Data
J6 pin 5	CH2_RX_DSA_D0X	Ch2 Rx DSA Data bit 0
J6 pin 6	CH2_RX_DSA_D1X	Ch2 Rx DSA Data bit 1
J6 pin 7	CH2_RX_DSA_D2X	Ch2 Rx DSA Data bit 2
J6 pin 8	CH2_RX_DSA_D3X	Ch2 Rx DSA Data bit 3
J6 pin 9	CH2_RX_DSA_D4X	Ch2 Rx DSA Data bit 4
J6 pin 10	CH2_RX_DSA_D5X	Ch2 Rx DSA Data bit 5
J6 pin 11	CH2_TX_PA_ENX	Ch2 Tx PA Enable
J6 pin 12	CH2_TX_LNA_DISX	Ch2 Tx LNA Disable
J6 pin 13	CH2_RX_LNA0_BYPX	Ch2 Rx LNA0 Bypass
J6 pin 14	CH2_RX_LNA1_BYPX	Ch2 Rx LNA1 Bypass

Pin #	Signal	Description
J6 pin 15	CH2_RX_LNA0_DISX	Ch2 Rx LNA0 Disable
J6 pin 16	CH2_RX_LNA0_ENX	Ch2 Rx LNA0 Enable
J6 pin 17	CH2_RX_LNA1_DISX	Ch2 Rx LNA1 Disable
J6 pin 18	COMMS_LEDX	Yellow LED control
J6 pin 19	UTIL_3V3	3.3V
J6 pin 20	UTIL_3V3	3.3V
J6 pin 21	VBUS_1V8	1.8V
J6 pin 22	DGND	Digital Ground

5.10 Status LEDs

These are the status LED's on the board:

Table 4 – Status LEDs

LED	Color	Description
D1	Red	Ch1 Rx LNA0 Overload (see 5.13.1)
D2	Red	Ch2 Rx LNA0 Overload (see 5.13.1)
D3	Yellow	Software-controlled Comms indicator
D4	Green	Power Good

5.11 RFMC Connector Pin Assignments

The two tables below show the ZCU111 LPAF connector pin assignments, as per the Xilinx documentation for the board (table 3-21 of the ZCU111 Board User Guide [1]).

	H	G	F	E	D	C	B	A
1	DAC_AVTT	DAC_AVTT	GND	12V	12V	12V	12V	12V
2	DAC_AVTT	DAC_AVTT	GND	GND	GND	GND	GND	GND
3	GND	GND	GND	GND	GND	GND	GND	GND
4	GND	GND	GND	GND	GND	DAC_CLKIN_0_P	DAC_CLKIN_0_N	GND
5	GND	DAC_CLKIN_1_P	DAC_CLKIN_1_N	GND	GND	GND	GND	GND
6	GND	GND	GND	GND	GND	GND	GND	GND
7	GND	GND	GND	GND	GND	DAC_CLKIN_2_P	DAC_CLKIN_2_N	GND
8	GND	DAC_CLKIN_3_P	DAC_CLKIN_3_N	GND	GND	GND	GND	GND
9	GND	GND	GND	GND	GND	GND	GND	GND
10	GND	GND	GND	GND	GND	DAC_00_P	DAC_00_N	GND
11	GND	DAC_01_P	DAC_01_N	GND	GND	GND	GND	GND
12	GND	GND	GND	GND	GND	GND	GND	GND
13	GND	GND	GND	GND	GND	DAC_02_P	DAC_02_N	GND
14	GND	DAC_03_P	DAC_03_N	GND	GND	GND	GND	GND
15	GND	GND	GND	GND	GND	GND	GND	GND
16	GND	GND	GND	GND	GND	DAC_04_P	DAC_04_N	GND
17	GND	DAC_05_P	DAC_05_N	GND	GND	GND	GND	GND
18	GND	GND	GND	GND	GND	GND	GND	GND
19	GND	GND	GND	GND	GND	DAC_06_P	DAC_06_N	GND
20	GND	DAC_07_P	DAC_07_N	GND	GND	GND	GND	GND
21	GND	GND	GND	GND	GND	GND	GND	GND
22	GND	GND	GND	GND	GND	DAC_08_P	DAC_08_N	GND
23	GND	DAC_09_P	DAC_09_N	GND	GND	GND	GND	GND
24	GND	GND	GND	GND	GND	GND	GND	GND
25	GND	GND	GND	GND	GND	DAC_10_P	DAC_10_N	GND
26	GND	DAC_11_P	DAC_11_N	GND	GND	GND	GND	GND
27	GND	GND	GND	GND	GND	GND	GND	GND
28	GND	GND	GND	GND	GND	DAC_12_P	DAC_12_N	GND
29	GND	DAC_13_P	DAC_13_N	GND	GND	GND	GND	GND
30	GND	GND	GND	GND	GND	GND	GND	GND
31	GND	GND	GND	GND	GND	DAC_14_P	DAC_14_N	GND
32	GND	DAC_15_P	DAC_15_N	GND	GND	GND	GND	GND
33	GND	GND	GND	GND	GND	GND	GND	GND
34	3V3	3V3	3V3	3V3	3V3	3V3	3V3	3V3
35	GND	SPARE_02	GND	SPARE_01	GND	DACIO_VADJ	GND	DACIO_VADJ
36	DACIO_17	GND	DACIO_12	GND	DACIO_07	GND	DACIO_02	GND
37	GND	DACIO_15	GND	DACIO_10	GND	DACIO_05	GND	DACIO_00
38	DACIO_18	GND	DACIO_13	GND	DACIO_08	GND	DACIO_03	GND
39	GND	DACIO_16	GND	DACIO_11	GND	DACIO_06	GND	DACIO_01
40	DACIO_19	GND	DACIO_14	GND	DACIO_09	GND	DACIO_04	GND

Figure 16 – RFMC DAC LPAF Connector J94, Vertical Orientation (A1 Upper Right Corner)

	H	G	F	E	D	C	B	A
1	ADCIO_17	GND	ADCIO_12	GND	ADCIO_07	GND	ADCIO_02	GND
2	GND	ADCIO_15	GND	ADCIO_10	GND	ADCIO_05	GND	ADCIO_00
3	ADCIO_18	GND	ADCIO_13	GND	ADCIO_08	GND	ADCIO_03	GND
4	GND	ADCIO_16	GND	ADCIO_11	GND	ADCIO_06	GND	ADCIO_01
5	ADCIO_19	GND	ADCIO_14	GND	ADCIO_09	GND	ADCIO_04	GND
6	GND	I2C_SCL	GND	I2C_SDA	GND	ADCIO_VADJ	GND	ADCIO_VADJ
7	3V3	3V3	3V3	3V3	3V3	3V3	3V3	3V3
8	GND	GND	GND	GND	GND	GND	GND	GND
9	GND	ADC_00_P	ADC_00_N	GND	GND	GND	GND	GND
10	GND	GND	GND	GND	GND	ADC_01_P	ADC_01_N	GND
11	GND	GND	GND	GND	GND	GND	GND	GND
12	GND	ADC_02_P	ADC_02_N	GND	GND	GND	GND	GND
13	GND	GND	GND	GND	GND	ADC_03_P	ADC_03_N	GND
14	GND	GND	GND	GND	GND	GND	GND	GND
15	GND	ADC_04_P	ADC_04_N	GND	GND	GND	GND	GND
16	GND	GND	GND	GND	GND	ADC_05_P	ADC_05_N	GND
17	GND	GND	GND	GND	GND	GND	GND	GND
18	GND	ADC_06_P	ADC_06_N	GND	GND	GND	GND	GND
19	GND	GND	GND	GND	GND	ADC_07_P	ADC_07_N	GND
20	GND	GND	GND	GND	GND	GND	GND	GND
21	VCM	VCM	VCM	VCM	VCM	VCM	VCM	VCM
22	GND	GND	GND	GND	GND	GND	GND	GND
23	GND	ADC_08_P	ADC_08_N	GND	GND	GND	GND	GND
24	GND	GND	GND	GND	GND	ADC_09_P	ADC_09_N	GND
25	GND	GND	GND	GND	GND	GND	GND	GND
26	GND	ADC_10_P	ADC_10_N	GND	GND	GND	GND	GND
27	GND	GND	GND	GND	GND	ADC_11_P	ADC_11_N	GND
28	GND	GND	GND	GND	GND	GND	GND	GND
29	GND	ADC_12_P	ADC_12_N	GND	GND	GND	GND	GND
30	GND	GND	GND	GND	GND	ADC_13_P	ADC_13_N	GND
31	GND	GND	GND	GND	GND	GND	GND	GND
32	GND	ADC_14_P	ADC_14_N	GND	GND	GND	GND	GND
33	GND	GND	GND	GND	GND	ADC_15_P	ADC_15_N	GND
34	GND	GND	GND	GND	GND	GND	GND	GND
35	GND	ADC_CLKIN_1_P	ADC_CLKIN_1_N	GND	GND	GND	GND	GND
36	GND	GND	GND	GND	GND	ADC_CLKIN_0_P	ADC_CLKIN_0_N	GND
37	GND	GND	GND	GND	GND	GND	GND	GND
38	GND	ADC_CLKIN_3_P	ADC_CLKIN_3_N	GND	GND	GND	GND	GND
39	GND	GND	GND	GND	GND	ADC_CLKIN_2_P	ADC_CLKIN_2_N	GND
40	GND	GND	GND	GND	GND	GND	GND	GND

Figure 17 – RFMC RF-ADC LPAF Connector J47, Vertical Orientation (A1 in Upper Right Corner)

The tables below show the Qorvo-side connector pin assignments for the RFMC LPAM connectors.

Table 5 – Channel 1 RFMC J4 (mates with ZCU111 J94)

Conn.	Pin #	ZCU111 Chip Pin #	ZCU111 Signal Name	Qorvo Signal Name
J4A	1			12V
	34			UTIL_3V3
	35			VBUS_1V8
	37	A9	DACIO_00	I2C_SCLX
	39	A10	DACIO_01	I2C_SDAX
J4B	1			12V
	10			**DAC_00_N**
	19			**DAC_06_N**
	22			NC
	34			UTIL_3V3
	36	A6	DACIO_02	CH1_RX_LNA0_BYPX
	38	A7	DACIO_03	CH1_RX_LNA1_BYPX
	40	A5	DACIO_04	CH1_RX_LNA0_DISX
J4C	1			12V
	10			**DAC_00_P**
	19			**DAC_06_P**
	34			UTIL_3V3
	35			VBUS_1V8
	37	B5	DACIO_05	CH1_RX_LNA0_ENX
	39	C5	DACIO_06	CH1_RX_OVX
J4D	1			12V
	34			UTIL_3V3
	36	C6	DACIO_07	CH1_TX_PA_ENX

Conn.	Pin #	ZCU111 Chip Pin #	ZCU111 Signal Name	Qorvo Signal Name
	38	B9	DACIO_08	CH1_RX_LNA1_DISX
	40	B10	DACIO_09	CH1_TX_LNA_DISX
J4E	1			12V
	34			UTIL_3V3
	37	B7	DACIO_10	CH1_LEX
	39	B8	DACIO_11	CH1_CLKX
J4F	34			UTIL_3V3
	36	D8	DACIO_12	CH1_SIX
	38	D9	DACIO_13	CH1_RX_DSA_D0X
	40	C7	DACIO_14	CH1_RX_DSA_D1X
J4G	34			UTIL_3V3
	37	C8	DACIO_15	CH1_RX_DSA_D2X
	39	C10	DACIO_16	CH1_RX_DSA_D3X
J4H	34			UTIL_3V3
	36	D10	DACIO_17	CH1_RX_DSA_D4X
	38	D6	DACIO_18	CH1_RX_DSA_D5X
	40	E7	DACIO_19	TP7

Table 6 – Channel 2 RFMC J7 (mates with ZCU111 J47)

Conn.	Pin #	ZCU111 Chip Pin #	ZCU111 Signal Name	Qorvo Signal Name
J7A	2	AP5	ADCIO_00	COMMS_LEDX
	4	AP6	ADCIO_01	TP8
	6			VBUS_1V8
	7			UTIL_3V3
J7B	1	AR6	ADCIO_02	CH2_RX_LNA0_BYPX

Conn.	Pin #	ZCU111 Chip Pin #	ZCU111 Signal Name	Qorvo Signal Name
	3	AR7	ADCIO_03	CH2_RX_LNA1_BYPX
	5	AV7	ADCIO_04	CH2_RX_LNA0_DISX
	7			UTIL_3V3
	10			**ADC_01_N**
	13			**ADC_03_N**
	16			**ADC_05_N**
	19			**ADC_07_N**
J7C	2	AU7	ADCIO_05	CH2_RX_LNA0_ENX
	4	AV8	ADCIO_06	CH2_RX_OVX
	6			VBUS_1V8
	7			UTIL_3V3
	10			**ADC_01_P**
	13			**ADC_03_P**
	16			**ADC_05_P**
	19			**ADC_07_P**
J7D	1	AU8	ADCIO_07	CH2_TX_PA_ENX
	3	AT6	ADCIO_08	CH2_RX_LNA1_DISX
	5	AT7	ADCIO_09	CH2_TX_LNA_DISX
	7			UTIL_3V3
J7E	2	AU5	ADCIO_10	CH2_LEX
	4	AT5	ADCIO_11	CH2_CLKX
	7			UTIL_3V3
J7F	1	AU3	ADCIO_12	CH2_SIX
	3	AU4	ADCIO_13	CH2_RX_DSA_D0X
	5	AV5	ADCIO_14	CH2_RX_DSA_D1X

Conn.	Pin #	ZCU111 Chip Pin #	ZCU111 Signal Name	Qorvo Signal Name
	7			UTIL_3V3
J7G	2	AV6	ADCIO_15	CH2_RX_DSA_D2X
	4	AU1	ADCIO_16	CH2_RX_DSA_D3X
	7			UTIL_3V3
J7H	1	AU2	ADCIO_17	CH2_RX_DSA_D4X
	3	AV2	ADCIO_18	CH2_RX_DSA_D5X
	5	AV3	ADCIO_19	TP9
	7			UTIL_3V3

5.12 Pi Pad Attenuators

There are –2 dB balanced Pi pad attenuators on the Qorvo card PCB between the RFSoC ADC/DAC connections within the SAMTEC LPAF connector and the baluns on the Qorvo card.

Resistor values are shown below. Also note the 100 nF AC coupling capacitors.

Target performance: better than –10 dB return loss up to 4 GHz.

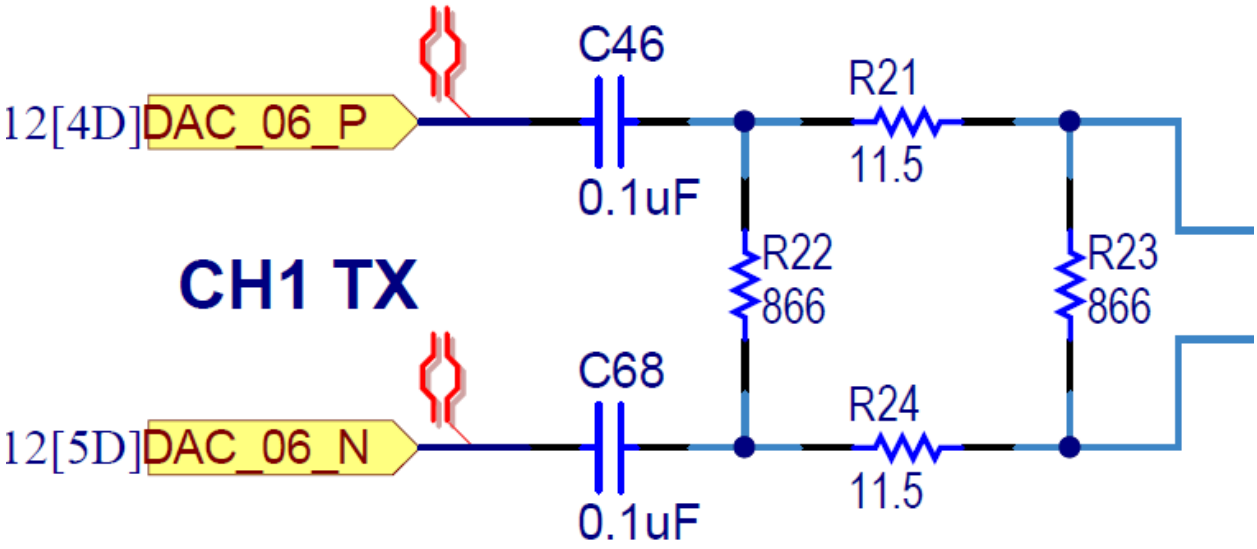

Figure 18 – Pi Pad Attenuators in the DAC Path

5.13 ADC Input Protection

It is important that the ADC inputs of the RFSoC device on ZCU111 be protected from out-of range external inputs.[1] The Rx LNA's can therefore be shut down or bypassed through combination over-voltage detection and user controls via software.

5.13.1 RX-side ADC Over-voltage Protection

An Analog Devices AD8361 mean-responding power detector at the output of the QPL9096 (LNA0) in each channel of RX signal chain monitors the signal level driving into the ADC. The power detector is resistively coupled at the output of QPL9096 LNA through 453Ω to form a voltage divider with the input impedance of AD8361, resulting in an attenuation factor of ~0.14. The protection circuit is nominally set to trigger when the LNA output reaches +5 dBm (50Ω), to account for estimated combined insertion loss of 4 dB through TQQ0302 BAW filter, pi network, balun and LPAM connector to the RFSoC ADC inputs on ZCU111.

The linear voltage output of the RMS detector drives a non-inverting op amp with make-up gain of 4 to compensate for the attenuation of the resistive coupling, followed by an open-loop op-amp comparator whose voltage threshold is set to trigger at 1.2 V, which corresponds to the maximum input level of 1V pk-pk at the RFSoC ADC input pins. Under this condition the LNA immediately switches to the (LNA OFF, Bypass OFF) state, whereby the RFSoC ADC input will reduce to signal ground through a 10K pull-down resistor at the output of the LNA0. This mechanism is intended to protect the RFSoC ADC inputs from inadvertent over-voltage, and is independent of any operational state of the ZCU111.

Note that the LNA over-voltage detection signals, CH1_RX_OV and CH2_RX_OV, are routed back to the ZCU111 GPIO so that software can reliably detect this hardware condition.

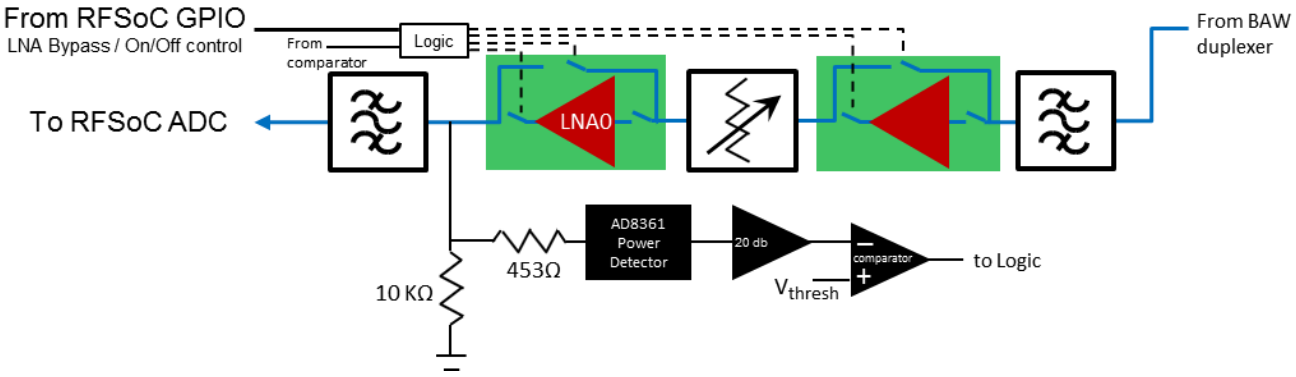

Figure 19- Rx-Side ADC over-voltage protection

[1] The RF-ADC input buffer contains an internal over voltage feature offering protection for signals in the range defined in the Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics (DS926). Full-scale input voltage is rated at 1V pk-pk (1 dBm into 100 Ω on-die termination). Signals exceeding this maximum are not permitted, and care must be taken externally to ensure that such voltages are not presented to the RF-ADC inputs.

Rx LNA Bypass Mechanisms

The LNA0 QPL9096 V_{SD} control input (pin 5) is driven by discrete logic on the Qorvo card combining ZCU111 GPIO signals through LPAF/M, and the comparator and AD8361 power detector. These signals are also routed to the Digital Test Pins, for scenarios where the Qorvo card may be used in standalone mode within a test harness independent of the ZCU111.

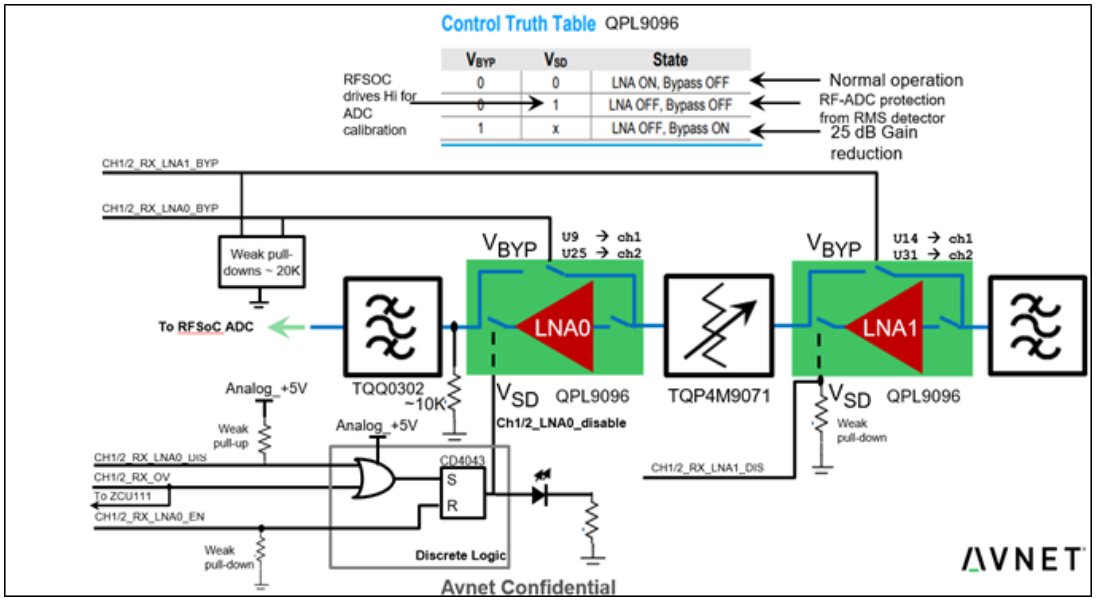

Figure 20 – Rx-Side LNA Control

The relation between the LNA0 Enable, Disable one Over Voltage signals is illustrated in this table from sheet 6 of the schematic [2].

Disable	Over Voltage	Enable	SD	LNA0 Operation
1	X	X	1	Disabled
X	1	X	1	Disabled
0	0	0	NC	No Change
0	0	1	0	Enabled

Figure 21 – Truth Table for LNA0 Operation

5.14 Directional Coupler

In the Observation (DPD) path, a Directional Coupler (Ch1 reference designator U11) is used for the following functions:

- It isolates the observation path from the main transmit path.
- This is a waveguide so either port 1 or port 2 could have been used as the input
- As configured, the chip provides "forward power" at port 3, while port 4 is isolated, seeing only small amounts of “back power”.

5.15 Circulator

After the Directional Coupler, the DPD signal passes through a Circular Isolator (Ch1 reference designator U16).

- It ensures any reflected signal due to impedance mismatch at U17 is circulated to ground instead of coming back towards the transmitter.
- The RF circulator is "behind" the duplexer to maximize the Noise Figure of the receiver chain. In other words, putting the circulator at the antenna would make the Rx signal traverse the circulator path (port 2 to port 3) and then the duplexer. This topology removes the circulator from the Rx path altogether.

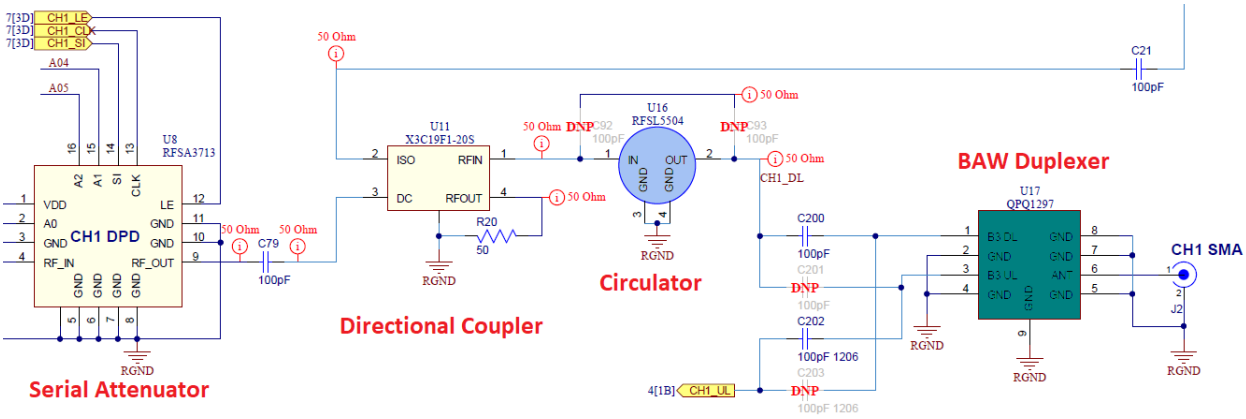

Figure 22 – DPD path Directional Coupler and Circulator

6 Regulatory and Compliance Information

The Qorvo card can radiate radio frequency energy and has not been tested for CE, FCC, or IC compliance. The intended use is for demonstration, engineering development, or evaluation purposes.

There are no constraints on operating temperature range, beyond thermal relief experimentation.

No environmental requirements such as moisture sensitivity, shock and vibration are relevant.

REGULATORY COMPLIANCE INFORMATION

FCC WARNING

This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Use of the kit should be limited to a development lab environment only.

CE WARNING

This evaluation kit is for use by professionals for their research and development purposes. The kit may not be put into service for use on a regular basis, or integrated into an end product (Annex I.4 of the RED). This kit is does not bear the CE mark of certification. As such, this kit may be operated only within the requirements of RED section 1.6.2.5, Custom-built evaluation kits.

7 Performance

Tests results reported for Channel 1 path.

7.1 Uplink (RX) Path

The receive path includes a digital step attenuator (DSA). Each plot line reports performance at a different attenuator state. For the receive path DSA, maximum attenuation is at state 00 while zero attenuation is at state 63. Measured from edge SMA at J2 to vertical SMA at J10.

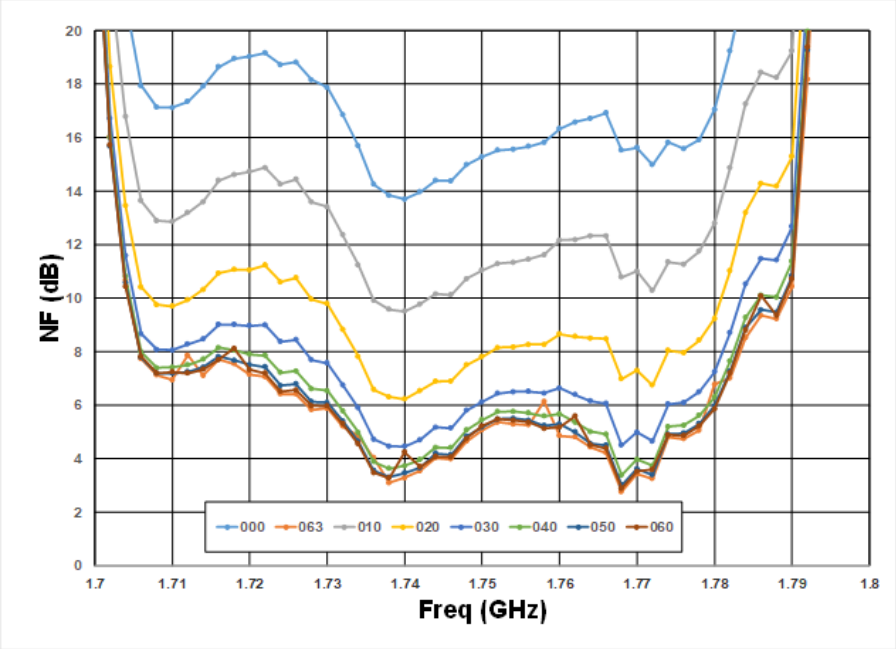

Figure 23 - Noise Figure vs Frequency vs DSA Attenuation States

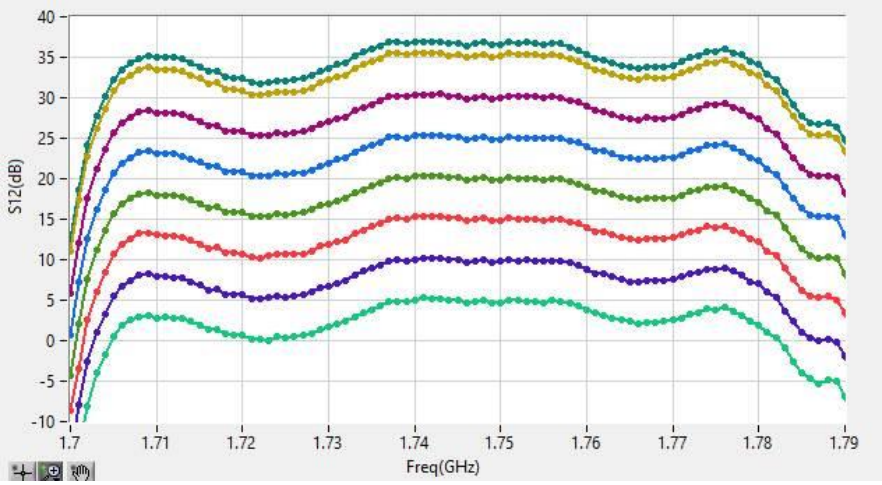

Figure 24 – Ch1 RX Gain vs DSA Attenuation States

7.2 Downlink (TX) Path

The transmit path includes a digital step attenuator (DSA). Each plot line reports performance at a different attenuator state. For the transmit path DSA, maximum attenuation is at state 127 while zero attenuation is at state 00. Measured from vertical SMA at J8 to edge SMA at J2.

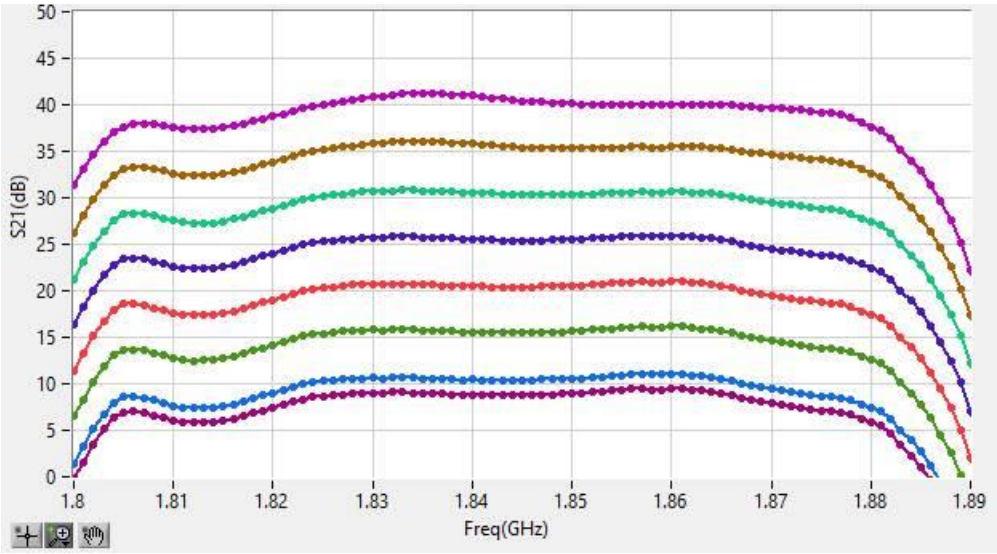

Figure 25 – Ch1 TX Gain vs DSA Attenuation Sates

7.3 DPD Observation Path

The DPD observation path includes a digital step attenuator (DSA). Each plot line reports performance at a different attenuator state. For the DPD path DSA, maximum attenuation is at state 127 while zero attenuation is at state 00. Measured from vertical SMA at J8 to edge SMA at J9.

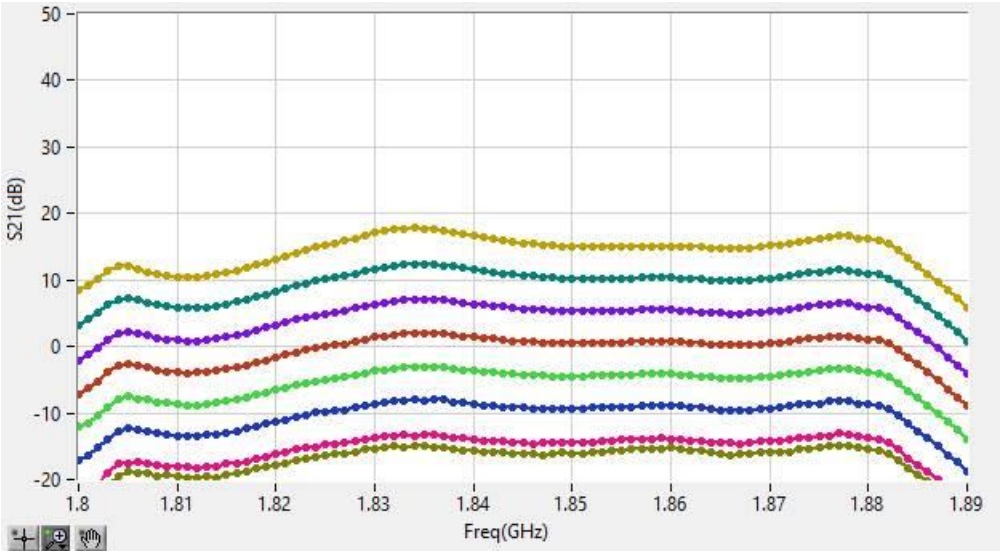

Figure 26 - Ch1 TX to DPD Gain vs. DSA Attenuation States

8 Getting Help and Support

If additional support is required, Avnet has many avenues to search depending on your needs.

For documentation, technical specifications, and videos visit the Avnet RFSoC kit page:

www.avnet.com/rfsockit

If you have questions, please use the RFSoC Kit forum on our Element 14 ZedBoard Community page:

https://www.element14.com/zedboardcommunity

9 Appendix A – Alternate Build Option

The Qorvo Card is a 2-channel FDD system with duplexers and filters tuned for specific uplink (RX) and downlink (TX) center frequencies. Both channels are identical in the production build.

- Downlink means a signal transmitted *from* the **DAC of RFSoC** , through the TX signal chain of the Qorvo card, *to* a user-equipment radio receiver
- LTE-band 3 calls for downlink max bandwidth ~75 MHz, centered at 1842.5 MHz
- Uplink means a signal received at the RX signal chain of the Qorvo card, through the **ADC of RFSoC**, *from* a user-equipment radio transmitter
- LTE-band 3 calls for uplink max bandwidth ~75 MHz, centered at 1747.5 MHz

The Avnet Qorvo 2-Channel RF front-end 1.8 GHz (AES-LPA-QRF1800-RVS-G) is a two channel Frequency Division Duplex (FDD) RF front end operating in LTE Band 3.

Channel 1 and Channel 2 circuit topologies are identical. The frequency plan for the two channels are symmetrical as summarized below.

- Channel 1: TX @ 1842.5MHz, RX @ 1747.5MHz
- Channel 2: TX @ 1747.5MHz, RX @ 1842.5MHz

This frequency plan enables OTA testing as single channel UE, base station, or loopback between Channel 1 and 2.

The PCB was designed to allow swapping uplink and downlink paths, making the frequency plan for both channels identical. The motivation for this feature was to enable, with only component changes, a system which could support a 2x2 MIMO small cell base station configuration. In this configuration, the frequency plan would be:

- Channel 1: TX @ 1842.5MHz, RX @ 1747.5MHz
- Channel 2: TX @ 1842.5MHz, RX @ 1747.5MHz

Component Modifications

Configuring the card as a 2x2 MIMO system requires the following component modifications. [2]

1. Enable CH2 downlink at 1842.5 MHz by replacing bandpass filter TQQ302 with TQQ0303 at U23, and replacing RF Circulator Isolator RFSL5408 with RFSL5504 at U33.
2. Enable CH2 uplink at 1747.5 MHz by replacing TQQ303 with TQQ0302 at U22 and U32.

[2] Inquiries for factory-modified Qorvo cards may be directed to your local Avnet FAE

3. Enable CH2 duplexer to receive at 1747.5 MHz and transmit at 1842.5 MHz by moving two capacitors to swap connections to the pins of the QPQ1297 Band 3 BAW Duplexer at U34. See Figure 28 and **Error! Reference source not found.**.

The required component changes are summarized in the table below, where NORMAL PRODUCTION is the configuration that supports 2x2 MIMO and REVERSE VARIANT is the factory configuration.

Normal Production	Reverse Variant	Description	Manufacturer	Part Number
U22, U32	U23	Signal Conditioning Band3 Uplnk BW 75MHz LowDrift BAW	QORVO	TQQ0302
U23	U22, U32	Signal Conditioning Band3 Dnlnk BW 75MHz LowDrift BAW	QORVO	TQQ0303
U33		Isolator, 1805-1880MHz, 20W	RFMW	RFSL5504
	U33	Isolator, 1710-1785MHz, 20W	RFMW	RFSL5408
C204	C205	CAP CER 100PF 50V C0G/NP0 0603	KEMET	C0603C101K5GACTU
C206	C207	CAP CER 100PF 50V C0G/NP0 1206	KEMET	C1206C101J5GACTU

Cap swap info:

- RF Transmit Channel 1 caps are identical across variants.
- RF Transmit Channel 2 requires a capacitor swap to enable the NORMAL variant

The changes are shown in the follow two schematic diagrams.

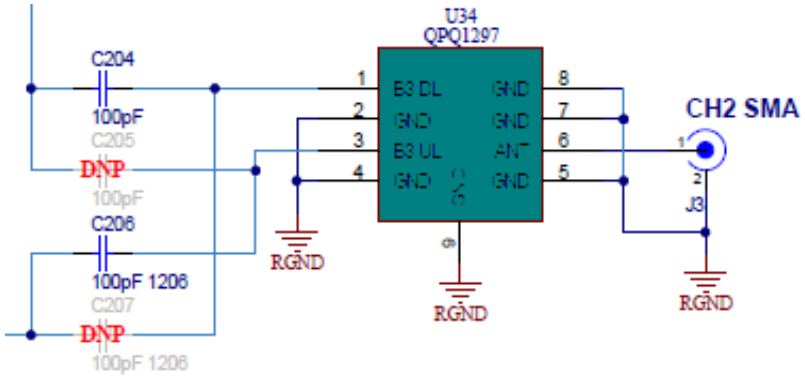

Figure 27 – Normal RF Transmit Channel 2

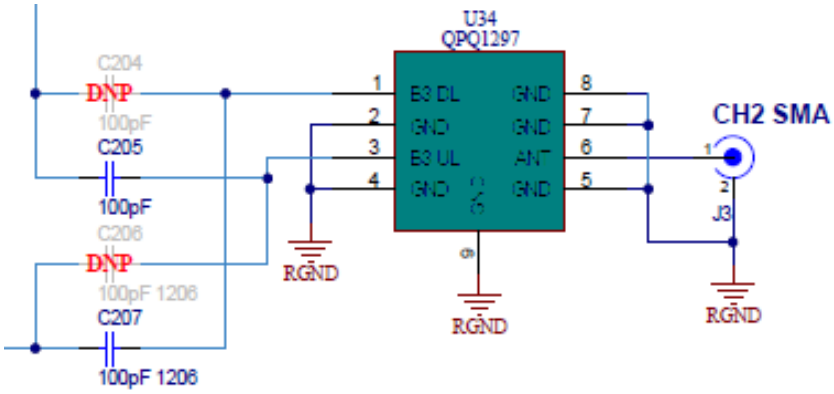

Figure 28 – Reverse RF Transmit Channel 2

The PCB has landing pad provisions for swapping connections to the Channel 2 duplexer.

The NORMAL configuration is an optional way to configure the card, but requires modification to the board which will void the standard warranty for the Qorvo card. Only attempt these changes if you have adequate board rework equipment and expertise.

For the NORMAL configuration C207 can be re-soldered to location of C206. Likewise, C205 can be re-soldered to location of C204.