

FACT SHEET i.MX 93 APPLICATIONS PROCESSOR FAMILY

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i.MX 93 applications processors deliver efficient machine learning (ML) acceleration, energy flex architecture and state-of-the-art security to support energy-efficient edge computing. i.MX 93 processors offer fast and efficient ML inferencing along with a rich set of peripherals and high-performance application cores for automotive, industrial and consumer IoT market segments.

TARGET APPLICATIONS

- Automotive: domain controller compute off-load engine, driver monitoring system, audio, speech recognition, cost-effective gateway
- Industrial Automation: gateways, remote I/O controllers, industrial scanners, HMI, machine vision
- Building Control and Energy: energy meters, EV charging
- Smart Home: home security hub, smart doorbell, smart lock, smart thermostat, AV receivers
- Smart City: smart lighting, safety and security, traffic control

PERFORMANCE COMPUTE ENGINE

The i.MX 93 applications processors are the first in the i.MX portfolio to integrate the scalable Arm® Cortex®-A55 core, bringing best-in-class performance and energy efficiency to Linux-based edge applications. Based on Arm's DynamIQ technology, the A55 core features the latest Armv8-A architecture extensions with dedicated instructions to accelerate machine learning (ML).



NEURAL PROCESSING UNIT (NPU)

The i.MX 93 family marks the industry's first implementation of the Arm[®] Ethos[™]-U65 microNPU. A dedicated neural processing unit (NPU), Ethos-U65 delivers a combination of performance and efficiency with an optimized footprint that enables developers to create high-performance, costeffective and energy-efficient ML applications.

BUILT-IN MCU

A 250 MHz Arm[®] Cortex[®]-M33 processor performs timecritical real-time compute and control. It can eliminate the need for an external microcontroller in the system design. The integrated Cortex-M33 core associated with the CAN FD interfaces provides a robust local control network for industrial applications. Additionally, the built-in Arm Cortex M33 in conjunction with the NPU can be used for low-power wake-word detection.

i.MX 935X/933X BLOCK DIAGRAM

		11 mm x 11 mm pkg								
System Clock		Main CPU		External DRAM						
Oscillator		2x Arm [®] Cortex [®] -A55		X16 LPDDR4/LF	PDDR4X (Inline ECC)					
Ditt.		32 kB I-cache 32 kB D-cache								
PLLs		NEON 64 kB L2 Cache FPU								
		256 kB L3 (Cache (ECC)							
Low Power Real Time Domain										
System Control		Low Power Security MCU		Connectivity and I/O						
DMA		Arm Cortex-M33		UART/USART x2, SPI x2						
Watchdog, Periodic Timer		16 kB+16 kB Code+Sys Cache		l²C x2, I3C						
Timer/PWM x2	2, Timer x2	FPU MF	PU NVIC	CAN	I-FD					
Temperature Sensor		256 kB TCM/OCRAM w/ECC		2-lane I ² S TDM Tx/Rx						
				8-ch PDM Mic Input						
					MQS					
		EdgeLock [®] S	ecure Enclave							
Crypto	Tamper Detection	Secure Clock	Secure Boot	eFuse Key Storage	Random Number					
		Eloy (Jomain							
System	Control	ML and Multimodia		Connectivity and I/O						
DM			5-lane I2S TDM Tx/Rx_SPDIF		UART/USART x6 SPI x6					
Watchdog x3 Periodic Timer		5-lane I ² S TDM	Tx/Rx SPDIE	UART/USAR	T x6 SPL x6					
Watchdog x3, P	eriodic Timer	5-lane I ² S TDM 8 bpp Parallel YU	Tx/Rx, SPDIF V/RGHB Camera	UART/USAR	RT x6, SPI x6					
Watchdog x3, P Timer/PWM x2	eriodic Timer 2. Timer x2	5-lane I ² S TDM 8 bpp Parallel YU 24 bpp Parallel	Tx/Rx, SPDIF V/RGHB Camera	UART/USAR I²C xế CAN	RT x6, SPI x6 5, I3C I-FD					
Watchdog x3, P Timer/PWM x2 Secure	eriodic Timer 2, Timer x2 ITAG	5-lane I²S TDM 8 bpp Parallel YU 24 bpp Parallel 2D Gra	Tx/Rx, SPDIF V/RGHB Camera RGB Display aphics	UART/USAR I²C xt CAN Flexi	RT x6, SPI x6 5, I3C I-FD 0 x2					
Watchdog x3, P Timer/PWM x Secure v	eriodic Timer 2, Timer x2 JTAG	5-lane I²S TDM 8 bpp Parallel YU 24 bpp Parallel 2D Gra High-efficie	Tx/Rx, SPDIF V/RGHB Camera I RGB Display aphics ancy NPU	UART/USAR I ² C xf CAN Flexi ADC (4-cha	RT x6, SPI x6 5, I3C I-FD O x2 nnel, 12-bit)					
Watchdog x3, P Timer/PWM x Secure s	eriodic Timer 2, Timer x2 JTAG I ory	5-lane I ² S TDM 8 bpp Parallel YU ¹ 24 bpp Parallel 2D Gra High-efficie MIPI-CSI 2-1	Tx/Rx, SPDIF V/RGHB Camera I RGB Display aphics ency NPU ane w/PHY	UART/USAR I ² C x6 CAN Flexi ADC (4-cha 2x Gigabit Ethe	RT x6, SPI x6 S, I3C I-FD O x2 nnel, 12-bit) rmet (1 w/TSN)					
Watchdog x3, P Timer/PWM x2 Secure x Mem 3x SD/SDIO 3.0	eriodic Timer 2, Timer x2 JTAG I ory D/eMMC 5.1	5-lane I ² S TDM 8 bpp Parallel YU ¹ 24 bpp Parallel 2D Gra High-efficie MIPI-CSI 2-1 MIPL-DSI 4-1	Tx/Rx, SPDIF V/RGHB Camera I RGB Display aphics ency NPU ane w/PHY ane w/PHY	UART/USAR I ² C x6 CAN Flexi ADC (4-cha 2x Gigabit Ethe	RT x6, SPI x6 S, I3C I-FD O x2 nnel, 12-bit) ernet (1 w/TSN) B 2 0					
Watchdog x3, P. Timer/PWM x2 Secure x Mem 3x SD/SDIO 3.0 Octal SPI FLASH	eriodic Timer 2, Timer x2 JTAG Iory D/eMMC 5.1 w/Inline Crypto	5-lane I ² S TDM 8 bpp Parallel YU ¹ 24 bpp Parallel 2D Gra High-efficie MIPI-CSI 2-I MIPI-DSI 4-I	Tx/Rx, SPDIF V/RGHB Camera I RGB Display aphics ency NPU ane w/PHY ane w/PHY	UART/USAR I ² C x6 CAN FlexI ADC (4-cha 2x Gigabit Ethe 2x US	RT x6, SPI x6 5, I3C I-FD O x2 nnel, 12-bit) ernet (1 w/TSN) SB 2.0					
Watchdog x3, P. Timer/PWM x2 Secure x 3x SD/SDIO 3.0 Octal SPI FLASH 640 kB OCR/	eriodic Timer 2, Timer x2 JTAG 0/eMMC 5.1 w/Inline Crypto \M w/ECC	5-lane I ² S TDM 8 bpp Parallel YU ¹ 24 bpp Parallel 2D Gra High-efficie MIPI-CSI 2-I MIPI-DSI 4-I 4-lane LVE	Tx/Rx, SPDIF V/RGHB Camera I RGB Display aphics ancy NPU ane w/PHY ane w/PHY DS w/PHY	UART/USAR I ² C x6 CAN FlexI ADC (4-cha 2x Gigabit Ethe 2x US	RT x6, SPI x6 5, I3C I-FD O x2 nnel, 12-bit) ernet (1 w/TSN) SB 2.0					

CAMERA INTERFACES AND IMAGE PROCESSING

The i.MX 93 family contains MIPI-CSI and parallel image sensor interfaces along with the NPU to support both monochrome and RGB (color) vision applications. The application processor offers a 2-lane MIPI-CSI camera interface capable of supporting 1080-p60 resolution and enables direct connection to external camera module and ISP. The application processors offer capabilities including down scaling, color space conversion, de-interlacing, alpha insertion, cropping and rotation of images for machine vision and other ML-related applications.

DISPLAY AND MULTIMEDIA

The i.MX 93 applications processors contain a 4-lane MIPI-DSI capable of supporting 1080p60 resolution, a 4-lane LVDS and parallel display interfaces capable of 720p60 resolution. Additionally, it features a high-efficiency pixel pipeline to perform 2D graphics processing to realize cost-effective GUI solutions. It is capable of image rotation (90°, 180°, 270°), image resize, color space conversion, multiple pixel format support (RGB, YUV444, YUV422, YUV420, YUV400) and standard 2D-DMA operations.

SYSTEM SECURITY

The i.MX 93 family implements security via NXP's EdgeLock® secure enclave, a preconfigured, self-managed and autonomous security subsystem. EdgeLock eases the complexity of implementing robust, device-wide security intelligence for IoT applications through autonomous management of critical security functions, such as root of trust, run-time attestation, trust provisioning, secure boot, key management and cryptographic services while also simplifying the path to industry-standard security certifications. The secure enclave functions like a "security HQ" or fortress inside the i.MX 93 SoCs, overseeing all security functions to protect systems against physical and network attacks. Fine-grained key management capabilities are augmented by extensive crypto services for advanced attack resistance. The secure enclave also intelligently tracks power transitions when applications are running to help prevent new attack surfaces from emerging. These attacks may include hardware reverse engineering, malware insertion, modifying/replacing the device image, version rollback attacks and physical attacks.

ENHANCED RELIABILITY

The i.MX 93 contains error correcting codes (ECC) in most of the internal memories such as L1, L2, L3 caches of the Arm Cortex-A55, the TCM of the Cortex-M33 and internal on-chip memory as well as the DDR interface for enhanced reliability.

ENERGY FLEX ARCHITECTURE

For fine-grained power management, the i.MX 93 applications processors implement NXP's innovative energy flex architecture where power and clock frequency of heterogenous domains such as the application domain (Cortex-A55s), real-time domain (Cortex-M33, peripherals) and flex domains (NPU, DDR, etc.) can be individually controlled to provide the maximum flexibility to achieve the lowest power consumption possible tuned to use cases. Additionally, the EVK would also have the capability to measure power on the various supply pins.

RICH SET OF HIGH-SPEED AND MEMORY INTERFACES

The i.MX 93 processors offer the latest high-speed interfaces for connectivity and fast data transfer with 2x USB 2.0, 3x SD/SDIO 3.01, 2x Gbit Ethernet with EEE, AVB, IEEE 1588 and TSN in one port for precise, low latency control loops, in addition to 2x CAN-FD interfaces. The memory interfaces supported are 16-bit LPDDR4/LPDDR4X (Inline ECC) and eMMC 5.1. The memory solution is optimized for the density, performance and price point.

INDUSTRY 4.0

Ethernet-based communication networks are critical to implement Industry 4.0. The i.MX 93 processors have two high-speed Ethernet interfaces — a gigabit Ethernet MAC along with Time-Sensitive Networking (TSN) hardware capability and <u>NXP's real-time edge software</u>. These features support Ethernet-connected deterministic control with precise time-synchronization. A second gigabit Ethernet port supports multiple data networks and gateway applications.

HIGH SCALABILITY WITH PIN-COMPATIBLE PLATFORM OPTIONS

The i.MX 93 applications processors family, part of the <u>EdgeVerse™ portfolio platform</u>, offers multiple SoCs with a scalable option to move up or down depending on the application needs. The different products in the i.MX 93 family include capabilities such as an integrated NPU and the number of Cortex-A55 cores. Additionally, pin-to-pin compatibility is planned between i.MX 93 and future i.MX 9 series product families.

COMPREHENSIVE SOFTWARE SUPPORT

NXP's Yocto-based enablement software provides flexibility to our customers to customize the BSPs to their specific needs. NXP provides quarterly releases with the latest and greatest kernel patches and bug fixes to support the customers in their design. NXP also provides binary blobs for all advanced IPs to enable a seamless experience for customers while porting and integrating their applications and offloading their workloads to these IPs. Additionally, NXP supports FreeRTOS and a plethora of commercial RTOS from partners to address Real-time customer applications enabling developers a quick and easy migration path.

Leveraging the broad Arm community, i.MX 93 builds technology alliances to enable better customer solutions and faster time-to-market. Join fellow i.MX developers online at www.imxcommunity.org.

NXP also offers the <u>eIQ™ ML Software Development</u>. <u>Environment</u>, a collection of libraries and development tools for building machine learning applications targeting i.MX applications processors and MCUs. The eIQ Toolkit leverages

open-source technologies and is fully integrated into NXP's Yocto development environments, allowing the development of complete system-level applications with ease.

HARDWARE TOOLS

The i.MX 93 evaluation kit (EVK) will enable SoC evaluation and system prototyping. Multiple accessory boards are planned to facilitate i.MX 93 processors' evaluation for applications such as camera modules and display panels.

Expert Package Design For Simplified System Design

The i.MX 93 will initially be available with a 11x11mm 0.5mm pitch package with routing channels.

Extended Industrial, Consumer and Automotive Qualified

i.MX 93 applications processors supports the following qualifications:

- Extended industrial temperature range (-40 °C to 125 °C Tj)
- Standard industrial temperature range (-40 °C to 105 °C Tj)
- Consumer application temperature range (0 °C to 95 °C Tj)
- Automotive temperature range (-40 °C to 125 °C Tj)

Supply Longevity

i.MX 93 processors will be part of NXP's Product Longevity program ensuring supply continuity and preserves your engineering investment for embedded designs for 15 years.

https://www.nxp.com/products/product-information/nxpproduct-programs/product-longevity:PRDCT_LONGEVITY_ HM

i.MX 93 PRODUCTS BY QUALIFICATION AND PACKAGES

PN	Part Diff.	NPU	Arm CPU	Package	
MIMX9352xxxxxxx	52	Y	2x	11x11mm	
MIMX9351xxxxxx	51	Y	1x	(198 IO pins)	
MIMX9332xxxxxxx	32	N	2x		
MIMX9331xxxxxxx	31	N	1x		
MIMX9321xxxxxxx	21	Y	1x	9x9mm (138 IO pins)	
MIMX9311xxxxxxx	11	N	1x		

i.MX 93 PRODUCT FEATURES

Package	Camera Interface	Display Interface	Networking & Connectivity	Audio
11x11 mm (198 IO pins) & 14x14 mm	1) 2-lane 1080p30 MIPI CSI 2) Parallel camera	1) 4-lane 1080p60 MIPI DSI 2) 4-lane LVDS 3) Parallel display	1) 2x GbE 2) 2x USB 2.0	7x I2S TDM
9x9 mm (138 IO pins)	1) Parallel camera	1) Parallel display	1) 1x GbE 2) 1x USB 2.0	3x I2S TDM

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