
# PSMN3R3-80YSF

**NextPower 80 V, 3.1 mOhm, 160 A, N-channel MOSFET in LFPAK56 package**

**1 August 2023** **Objective data sheet**

## 1. General description

NextPower 80 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

## 2. Features and benefits

- Low $Q_{rr}$ for higher efficiency and lower spiking
- 160 A $I_D$ [max] – demonstrated continuous current rating
- Low $Q_G$ × $R_{DSon}$ Figure of Merit (FOM) for high efficiency switching applications
- Strong avalanche energy rating ($E_{as}$)
- Avalanche rated and 100% tested
- Halogen free and RoHS compliant LFPAK56E package

## 3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in DC-DC
- Brushless DC (BLDC) motor control
- USB Power Delivery (PD) adapters
- Full-bridge and half-bridge applications
- Flyback and resonant topologies

## 4. Quick reference data

**Table 1. Quick reference data**

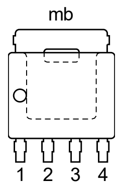
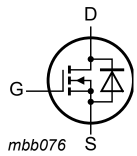
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | - | 80 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | | - | - | 160 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 300 | W |
| $T_j$ | junction temperature | | | -55 | - | 175 | °C |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 12 | | - | 2.5 | 3.1 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 105 °C; Fig. 13 | | - | 4 | 5 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 25 A; $V_{DS}$ = 40 V; $V_{GS}$ = 10 V; Fig. 14; Fig. 15 | | [tbd] | 15.5 | [tbd] | nC |
| $Q_{G(tot)}$ | total gate charge | | | [tbd] | 72 | [tbd] | nC |
| **Avalanche ruggedness** | | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 49 A; $V_{sup}$ ≤ 80 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 113 µs; Fig. 4 | [1] | - | - | 289 | mJ |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Source-drain diode** | | | | | | | |
| $Q_r$ | recovered charge | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 40 V; Fig. 18 | | - | 36 | - | nC |

[1] Protected by 100% test

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S | source | <br>**LFPAK56; Power-SO8 (SOT669)** |  |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMN3R3-80YSF | LFPAK56; Power-SO8 | plastic, single-ended surface-mounted package; 4 terminals | SOT669 |

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).* $T_j$ *= 25 °C unless otherwise stated.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | 80 | V |
| $V_{DGR}$ | drain-gate voltage | 25 °C ≤ $T_j$ ≤ 175 °C; $R_{GS}$ = 20 kΩ | | - | 80 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 300 | W |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | | - | 160 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; Fig. 2 | | - | 145 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C; Fig. 3 | | - | 820 | A |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| $T_{sld(M)}$ | peak soldering temperature | | | - | 260 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | | - | 100 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C | | - | 820 | A |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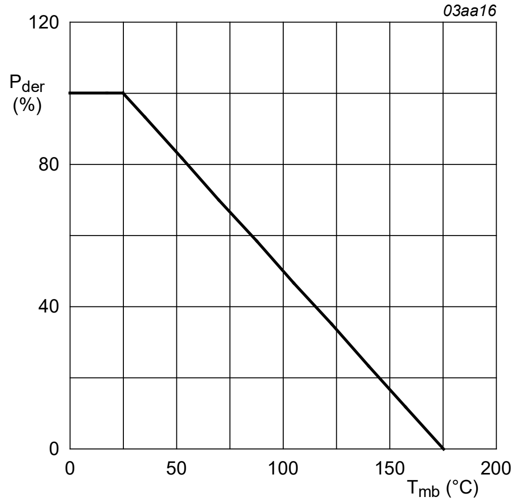
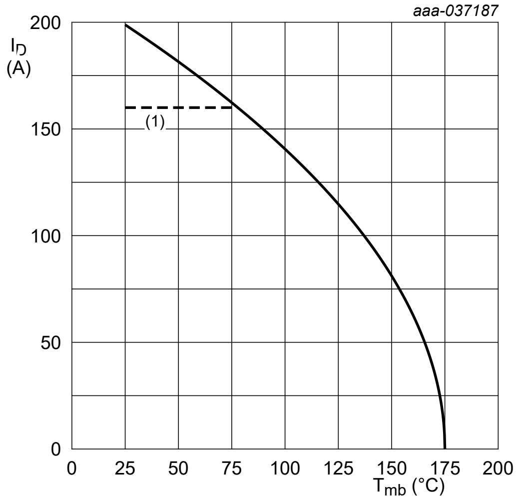
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 49 A; $V_{sup} \leq$ 80 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 113 µs; Fig. 4 | [1] | - | 289 | mJ |
| $I_{AS}$ | non-repetitive avalanche current | $V_{sup}$ = 80 V; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $R_{GS}$ = 50 Ω | [1] | - | 49 | A |

[1] Protected by 100% test




$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

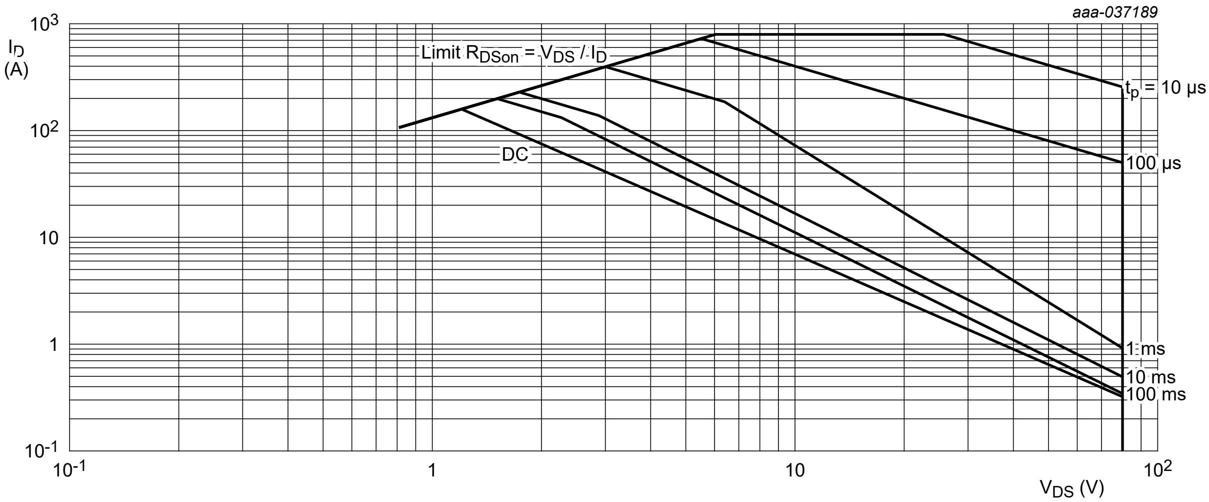
**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**




$V_{GS} \geq$ 10 V

(1) 160 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

**Fig. 2. Continuous drain current as a function of mounting base temperature**




$T_{mb}$ = 25 °C; $I_{DM}$ is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**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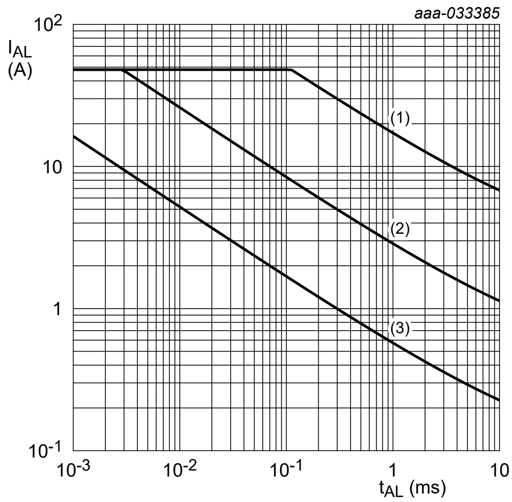


(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

**Fig. 4. Avalanche rating; avalanche current as a function of avalanche time**

## 8. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | | - | 0.43 | 0.5 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Fig. 6 | | - | 42 | - | K/W |
| | | Fig. 7 | | - | 85 | - | K/W |

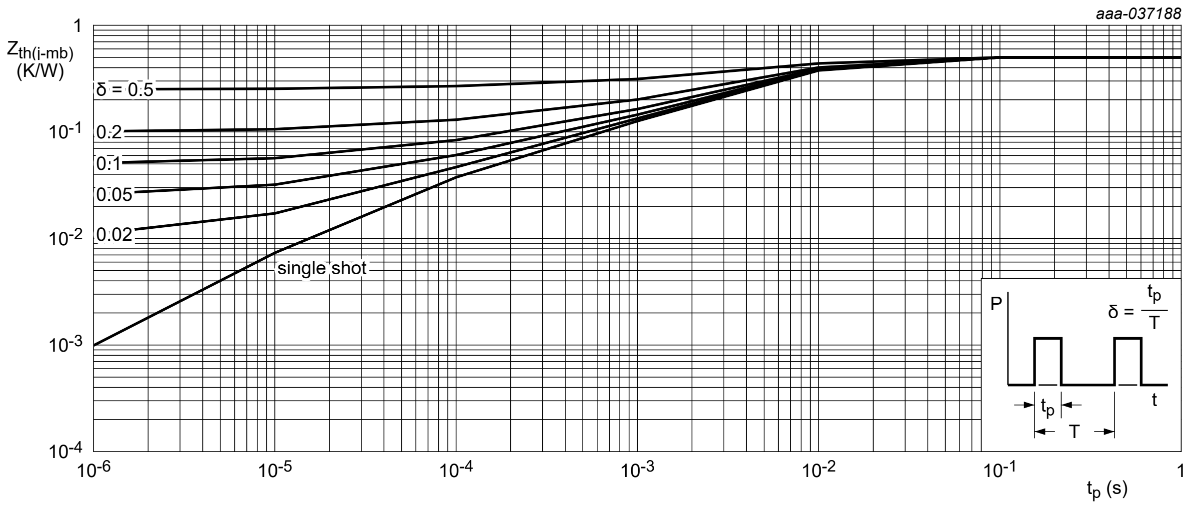


**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**


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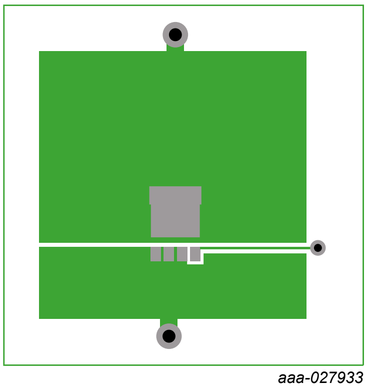
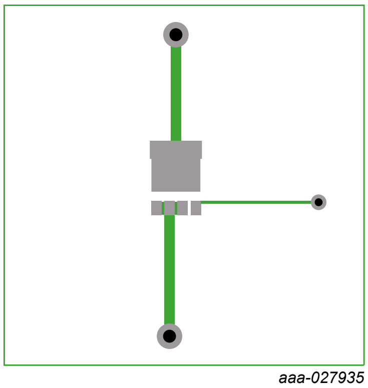



Copper area 25.4 mm square; 70 µm thick on FR4 board

**Fig. 6. PCB layout for thermal resistance from junction to ambient**




70 µm thick copper on FR4 board

**Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient**

# 9. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 80 | 89 | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 72 | 85 | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 25 °C; Fig. 11 | | 2.2 | 3 | 3.8 | V |
| | | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 175 °C | | - | 2 | - | V |
| | | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = -55 °C | | - | 3.4 | - | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | 25 °C ≤ $T_j$ ≤ 150 °C | | - | -7.8 | - | mV/K |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 80 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 0.07 | 1 | µA |
| | | $V_{DS}$ = 80 V; $V_{GS}$ = 0 V; $T_j$ = 125 °C | | - | 2 | 100 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| | | $V_{GS}$ = -20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 12 | | - | 2.5 | 3.1 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 105 °C; Fig. 13 | | - | 4 | 5 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 175 °C; Fig. 13 | | - | 5.8 | 7.1 | mΩ |
| $R_G$ | gate resistance | f = 1 MHz; $T_j$ = 25 °C | | [tbd] | 0.7 | [tbd] | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 40 V; $V_{GS}$ = 10 V; Fig. 14; Fig. 15 | | [tbd] | 72 | [tbd] | nC |
| | | $I_D$ = 0 A; $V_{DS}$ = 0 V; $V_{GS}$ = 10 V | | - | 63 | - | nC |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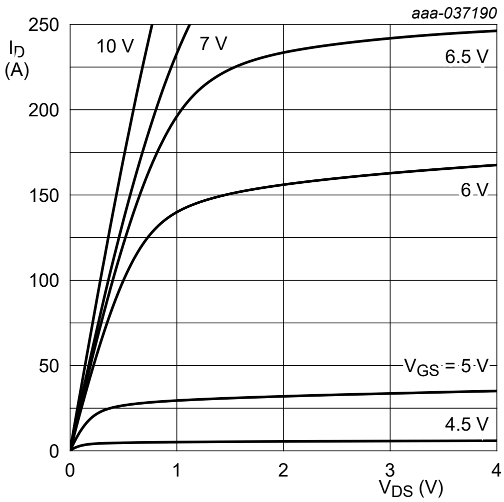
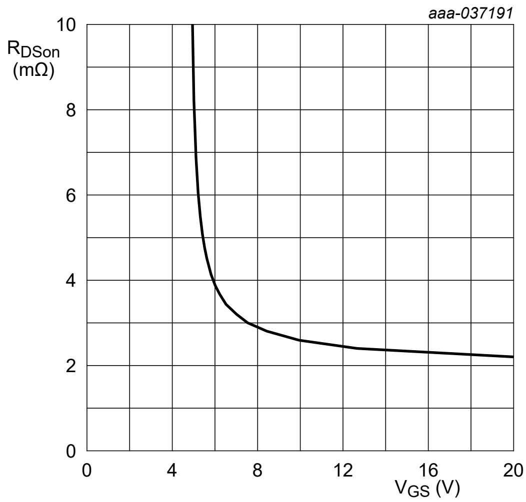
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $Q_{GS}$ | gate-source charge | $I_D$ = 25 A; $V_{DS}$ = 40 V; $V_{GS}$ = 10 V; Fig. 14; Fig. 15 | | [tbd] | 21.7 | [tbd] | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | | - | 13.4 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | | - | 8.3 | - | nC |
| $Q_{GD}$ | gate-drain charge | | | [tbd] | 15.5 | [tbd] | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D$ = 25 A; $V_{DS}$ = 40 V; Fig. 14; Fig. 15 | | - | 4.7 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 40 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 16 | | [tbd] | 4990 | [tbd] | pF |
| $C_{oss}$ | output capacitance | | | [tbd] | 1420 | [tbd] | pF |
| $C_{rss}$ | reverse transfer capacitance | | | [tbd] | 41 | [tbd] | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 40 V; $R_L$ = 1.6 Ω; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 5 Ω | | - | 20 | - | ns |
| $t_r$ | rise time | | | - | 18.5 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 38 | - | ns |
| $t_f$ | fall time | | | - | 22 | - | ns |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 17 | | - | 0.81 | 1 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 25 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 40 V; Fig. 18 | | - | 38.4 | - | ns |
| $Q_r$ | recovered charge | | | - | 36 | - | nC |




$T_j$ = 25 °C

**Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values**




$T_j$ = 25 °C; $I_D$ = 25 A

**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**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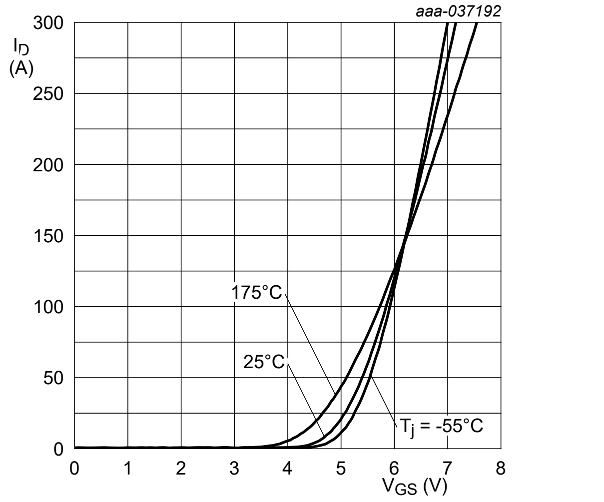
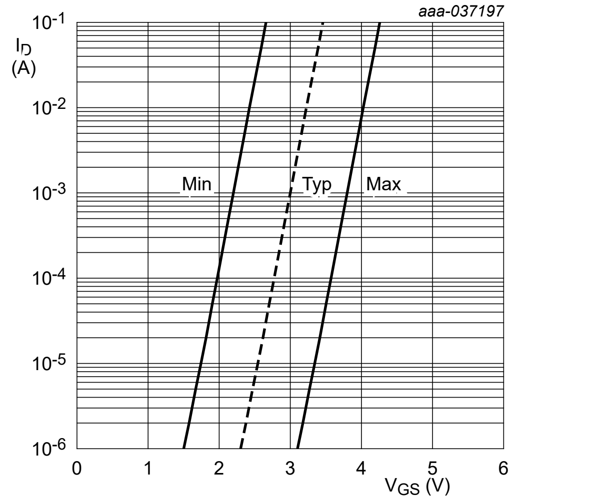


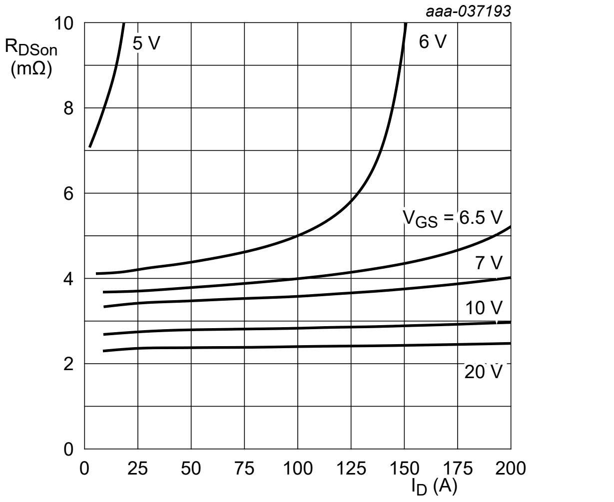

$V_{DS}$ = 8 V

**Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



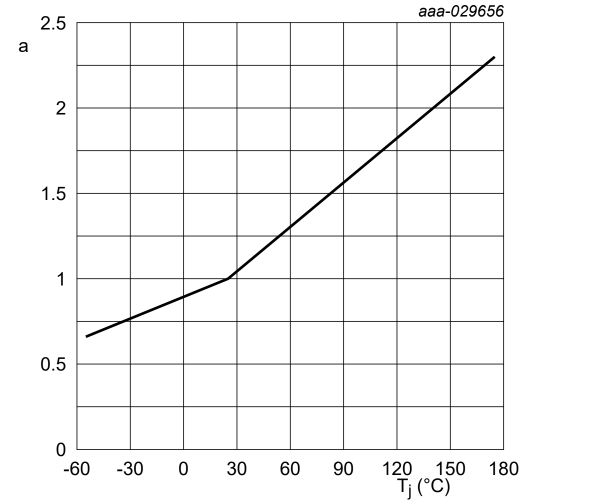

$T_j$ = 25 °C; $V_{DS}$ = 5 V

**Fig. 11. Sub-threshold drain current as a function of gate-source voltage**




$T_j$ = 25 °C

**Fig. 12. Drain-source on-state resistance as a function of drain current; typical values**




$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

**Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature**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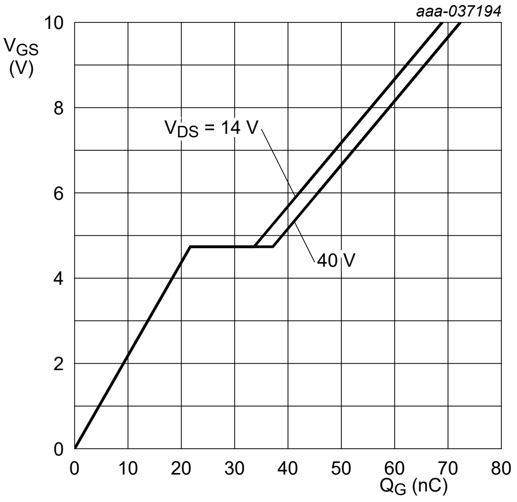



$T_j$ = 25 °C; $I_D$ = 25 A

**Fig. 14. Gate-source voltage as a function of gate charge; typical values**

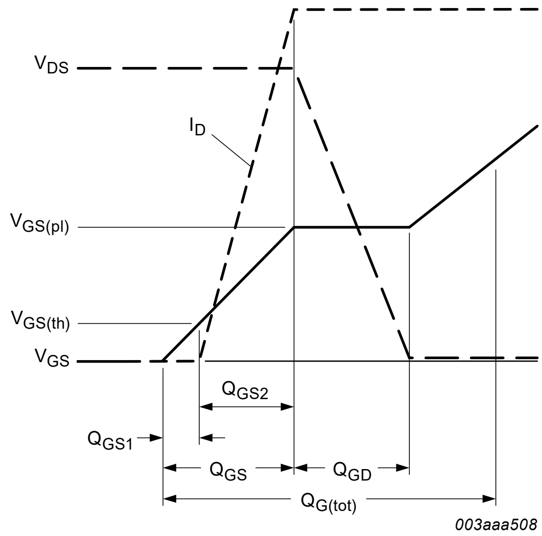
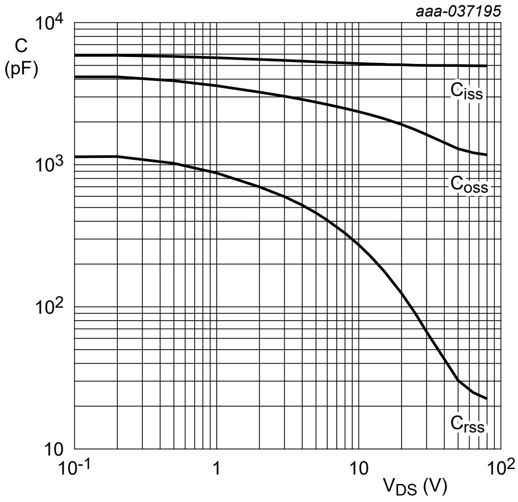
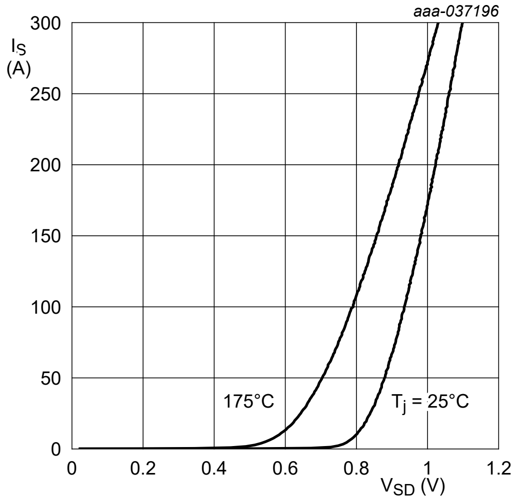



**Fig. 15. Gate charge waveform definitions**




$V_{GS}$ = 0 V; f = 1 MHz

**Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**




$V_{GS}$ = 0 V

**Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

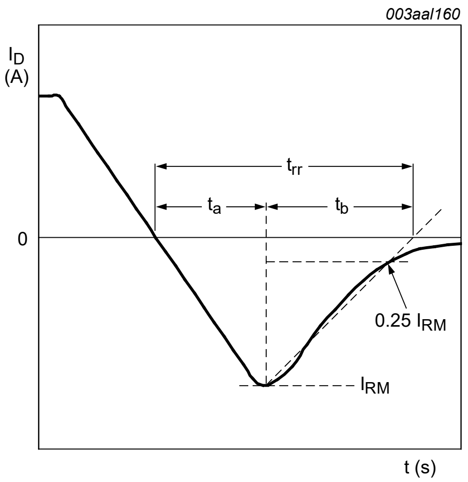



**Fig. 18. Reverse recovery timing definition**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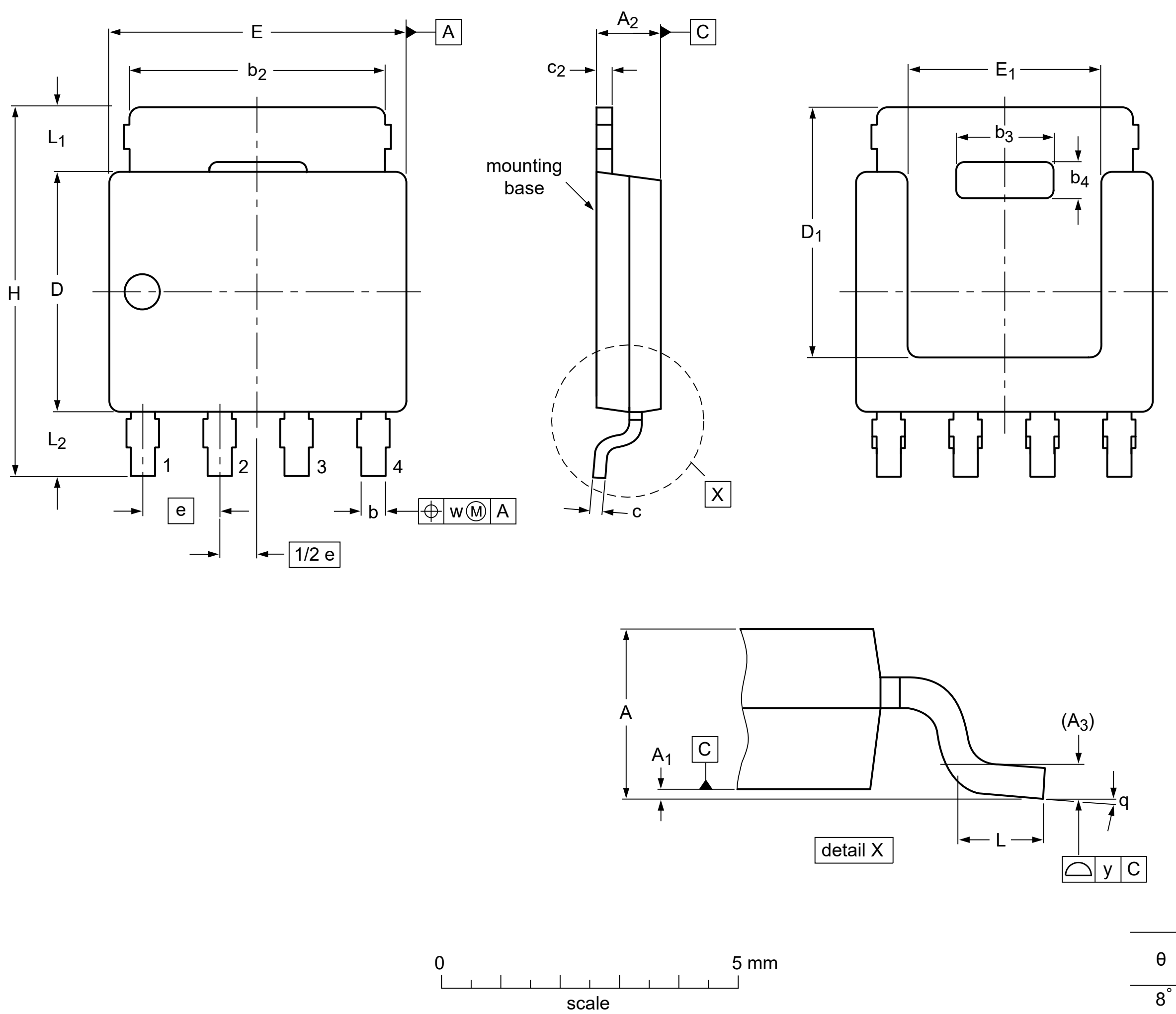
# 10. Package outline

**Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads** **SOT669**




Dimensions (mm are the original dimensions)

| Unit(1) | | A | $A_1$ | $A_2$ | $A_3$ | b | $b_2$ | $b_3$ | $b_4$ | c | $c_2$ | D(1) | $D_1$(1) | E(1) | $E_1$(1) | e | H | L | $L_1$ | $L_2$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.20 | 0.15 | 1.10 | | 0.50 | 4.41 | 2.2 | 0.9 | 0.25 | 0.30 | 4.10 | 4.20 | 5.0 | 3.3 | | 6.2 | 0.85 | 1.3 | 1.3 | | | 8° |
| | nom | | | | 0.25 | | | | | | | | | | | 1.27 | | | | | 0.25 | 0.1 | |
| | min | 1.01 | 0.00 | 0.95 | | 0.35 | 3.62 | 2.0 | 0.7 | 0.19 | 0.24 | 3.80 | | 4.8 | 3.1 | | 5.8 | 0.40 | 0.8 | 0.8 | | | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

*sot669_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT669 | | MO-235 | | | | ~~11-03-25~~<br>13-02-27 |

**Fig. 19. Package outline LFPAK56; Power-SO8 (SOT669)**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## 11. Soldering

**Footprint information for reflow soldering** **SOT669**

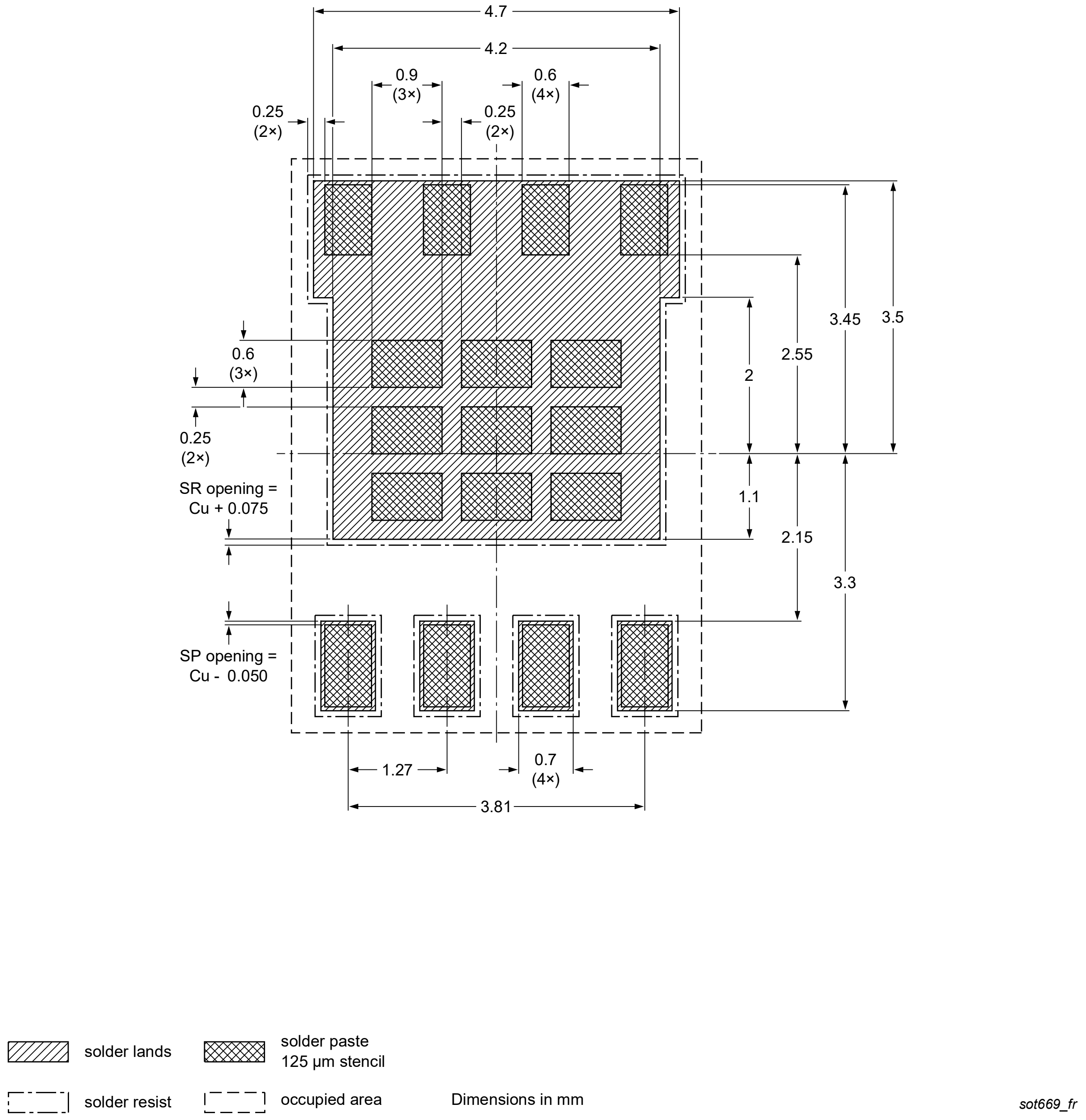


**Fig. 20. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)**

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**Wave soldering footprint information for LFPAK56 package** **SOT669**

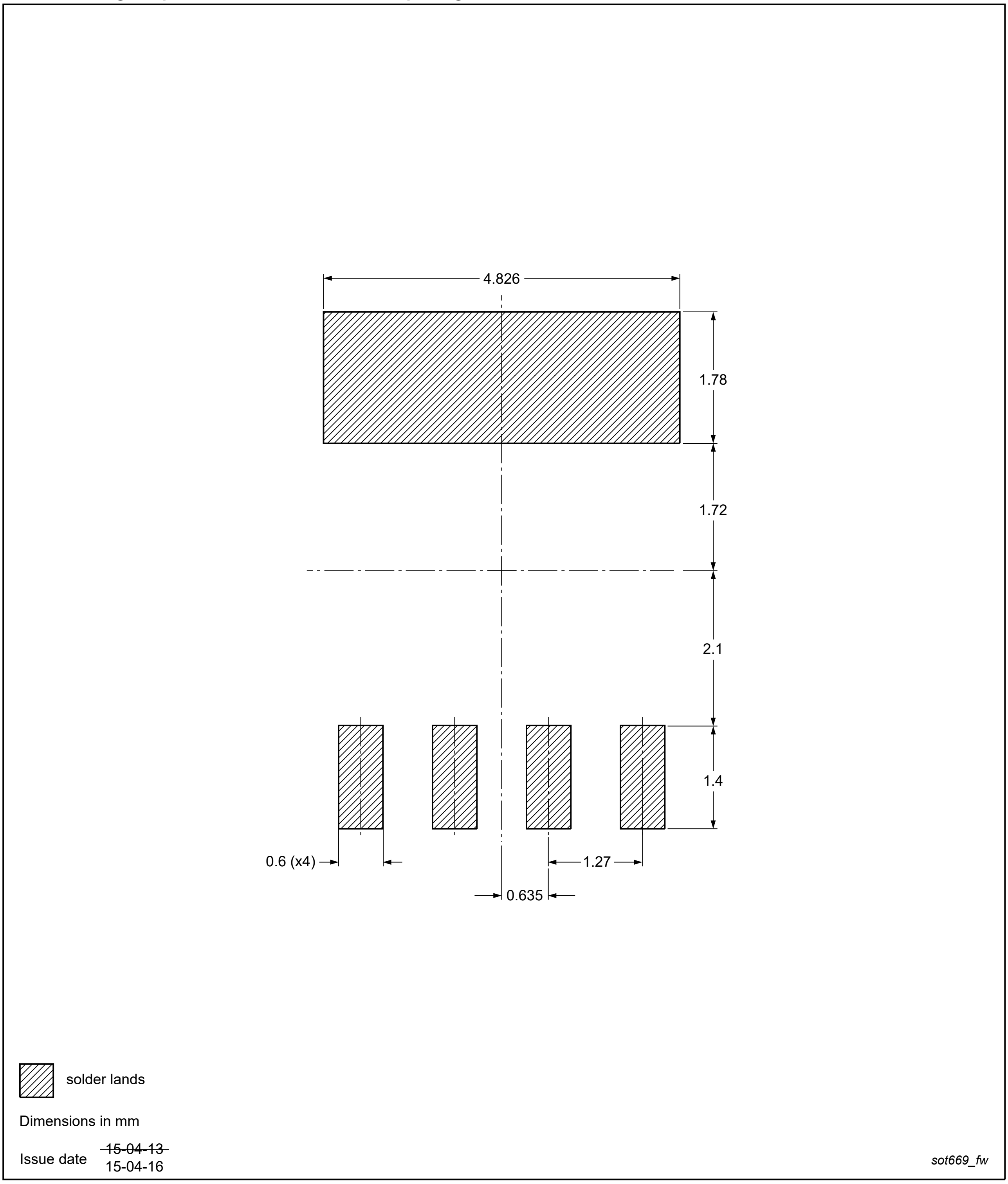


**Fig. 21. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)**


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### Data sheet status

| Document status [1][2] | Product status [3] | Definition |
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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**Date of release: 1 August 2023**