Technical Advantages of onsemi's New Elite Power Simulator and Self-Service PLECS Model Generator

AND90216/D

Introduction

The purpose of this application note is to explain the technical advantages included in the online Elite Power Simulator and Self−Service PLECS Model Generator (SSPMG) offered through **onsemi**. This note provides more details on how the online tools have been implemented and the features available. The application note begins by covering some basics with regards to SPICE and PLECS models. Next details behind switching loss extraction techniques and the influence of parasitics are covered. The concept and benefits of a virtual switching loss environment are introduced. This virtual environment also includes the ability to study system performance dependencies on semiconductor process variation. Finally, a PLECS model valid for both hard and soft switching and the associated ramifications are detailed. The conclusion explains the reasons why the **onsemi** tools are more accurate compared to other industry tools for power electronic system level simulation.

Physical and Scalable SPICE Modeling

Physical and Scalable SPICE modeling based on semiconductor physics was introduced to replace inaccurate behavioral SPICE models. Such behavioral models do not represent complex modern power devices such as SiC MOSFETs and IGBTs. **onsemi**'s physical SPICE models capture advanced affects like Reverse Recovery, Self−Heating, and electrical parameter variation due to process technology distribution in manufacturing. A core scalable model is generated first and then, multiple products within the same technology have models generated through dialing in the specific die layout and package parameters.

Details of **onsemi**'s Physical and Scalable Modeling are covered in the following papers[1,2,3,4]. Such modeling capabilities form the backbone of **onsemi**'s advanced PLECS modeling capabilities which are detailed in the pursuant sections.

PLECS Basic

PLECS is not a SPICE−based circuit simulator, where the focus is on low−level behavior of circuit components[5]. Rather, PLECS facilitates the modeling and simulation of complete systems with optimized device models for maximum speed and accuracy. As such power transistors like SiC MOSFETs are treated as simple switches that can be easily configured to demonstrate losses associated with conduction and switching transitions. The PLECS models, referred to as "thermal models", are composed of look−up tables for conduction and switching losses, along with a thermal chain in the form of a Cauer or Foster equivalent network. Generally, the measurement based loss tables are consistent with datasheets provided by the manufacturer. During simulation, PLECS interpolates and/or extrapolates using the loss tables to get the bias point conduction and switching losses for the circuit operation.

Double Pulse Tester to Measure Switching Losses

One most common way to measure switching losses is the double pulse tester. The theoretical schematic is shown on the Figure 1.

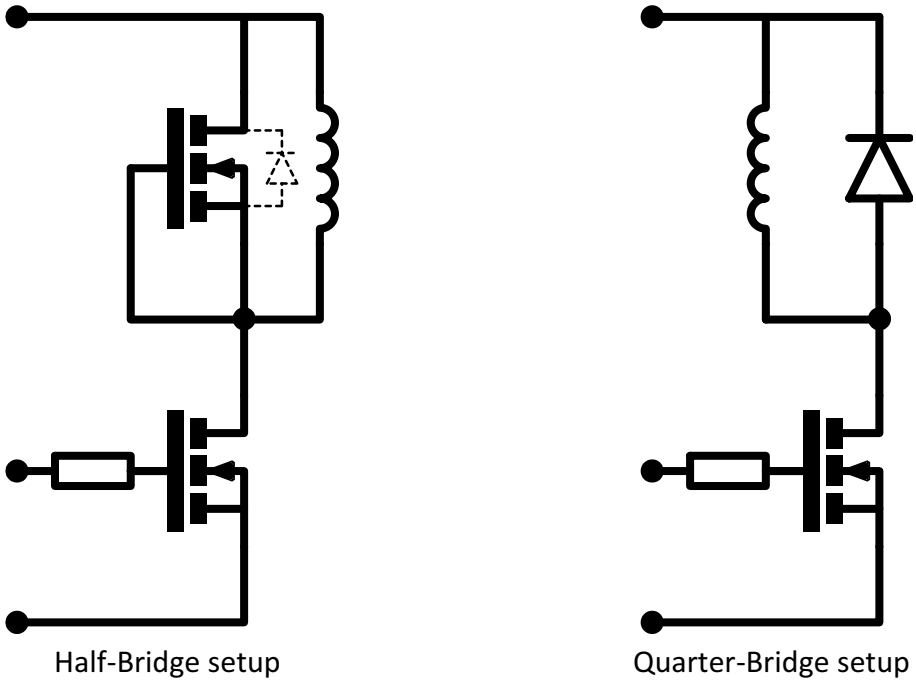

Figure 1. Basic Double Pulse Tester schematics

It can be a half−bridge structure or a quarter−bridge structure. At the origin, we consider the inductor current to be Zero or, in other words, the inductor is fully discharged. The principle is the following:

In a first step, the low side switch is turned on and the current in the inductor starts increasing. When the inductor current reaches the measurement point, the low side switch is turned off. At that moment, we measure turn off losses for this current. Then, the inductor current continues to flow due to the free−wheeling diode in the high side. As the voltage drop of the diode is almost zero and the duration is short, the inductor current is considered to be constant during that phase. Finally, the low side switch is turned on again and the turn−on losses are measured with almost the same inductor current than during turn−off. In this configuration, the switch is turned−on in hard switching.

As we can see in the white paper “SiC simulation”[6], the way the double pulse tester is setup, Half− or Quarter−Bridge, can influence switching losses. A SiC Schottky diode has a much lower QC than a MOSFET body−diode Q_{RR}. As this charge/energy in the high side switch/diode is dissipated in the lower side switch at turn−on, the setup (and so external components) can influence the main switch losses. This setup may be referred to as a “Boost” type double pulse tester. The switching inductor is attached to the input voltage. The active switch is connected at the low side. The passive switch, which can be a simple diode, is connected on the high side and shorted to the opposite input rail of the main switch.

Double Pulse Alternate Schematic

From the previous paragraph, we can derive a “Buck” type double pulse tester as shown in Figure 2 with all the previous “Boost” type.

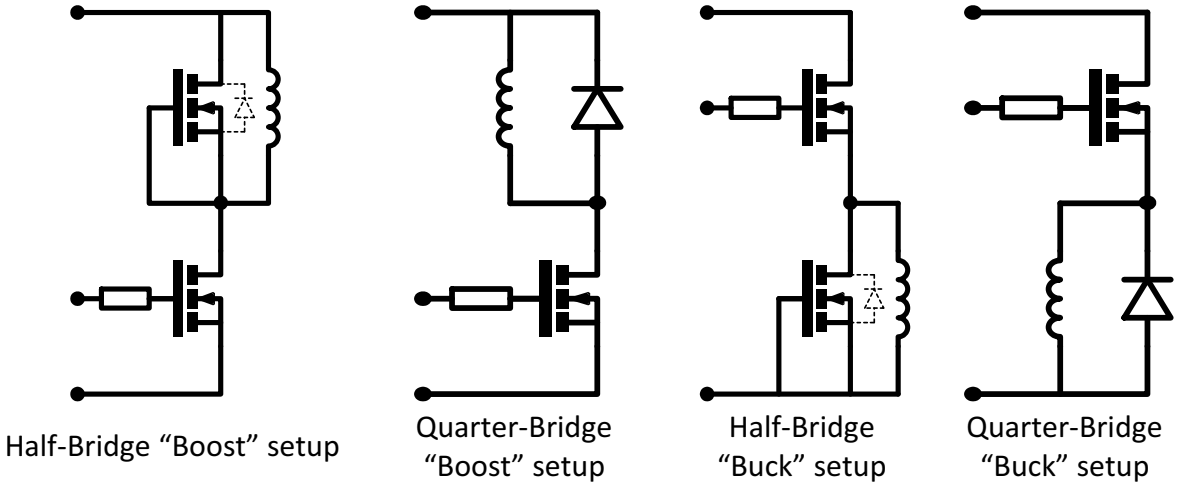

Figure 2. Double Pulse “Boost” and “Buck” Tester Schematics

In this “Buck” structure, it is easier to see the output is shorted to ground. The active switching is in the upper side and the passive switch (that can also be a diode) is in the lower side. Results obtained are the same as the “Buck” type if fully symmetrical compared to the “Boost” type. But, in practice, this “Buck” type requires a more complex measurement setup because the high side switch is floating. It is well known that direct or low side probes are much better than differential or high side probes. Therefore, this setup is rarely used in practice.

Parasitic Effects

In this section, we will analyze some of the major external contributors to switching losses in the active device. We have seen already in the white paper “SiC Simulation”[6] the impact of the high side component: diode or MOSFET. In the same paper, we can also find the influence of package leakage or parasitic components. But the package influence is already capture inside the **onsemi** physical and scalable product model.

Inductor Capacitor

The first component that interferes with the active switch losses is the switching inductor parasitic capacitor (Figure 3). See the white paper “Using Physical and Scalable Simulation Models to Evaluate Parameters and Application Results”[7] for more details on its effect. Using the schematic in the following figure, Eon, Eoff are plotted vs. the inductor parasitic capacitor with the 22 mΩ/1200 V M3S SiC MOSFET (NTH4L022N120M3S) in an almost ideal double pulse tester.

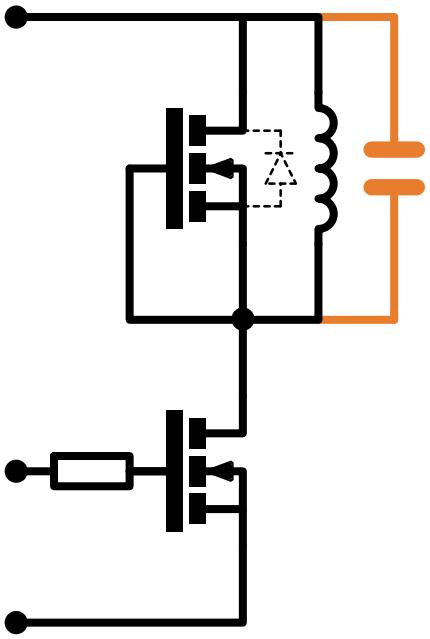

Figure 3. Inductor Parasitic Capacitor to Simulate Losses on a Double Pulse Tester

An inductor with a 10 pF parasitic capacitor is a very good inductor. An inductor with a 100 pF parasitic capacitor is an average inductor. Finally, an inductor with a 1 nF parasitic capacitor is a very bad inductor. Figures 4 and 5 show the impact of such parasitic capacitor on rise and fall time for Drain current and voltage.

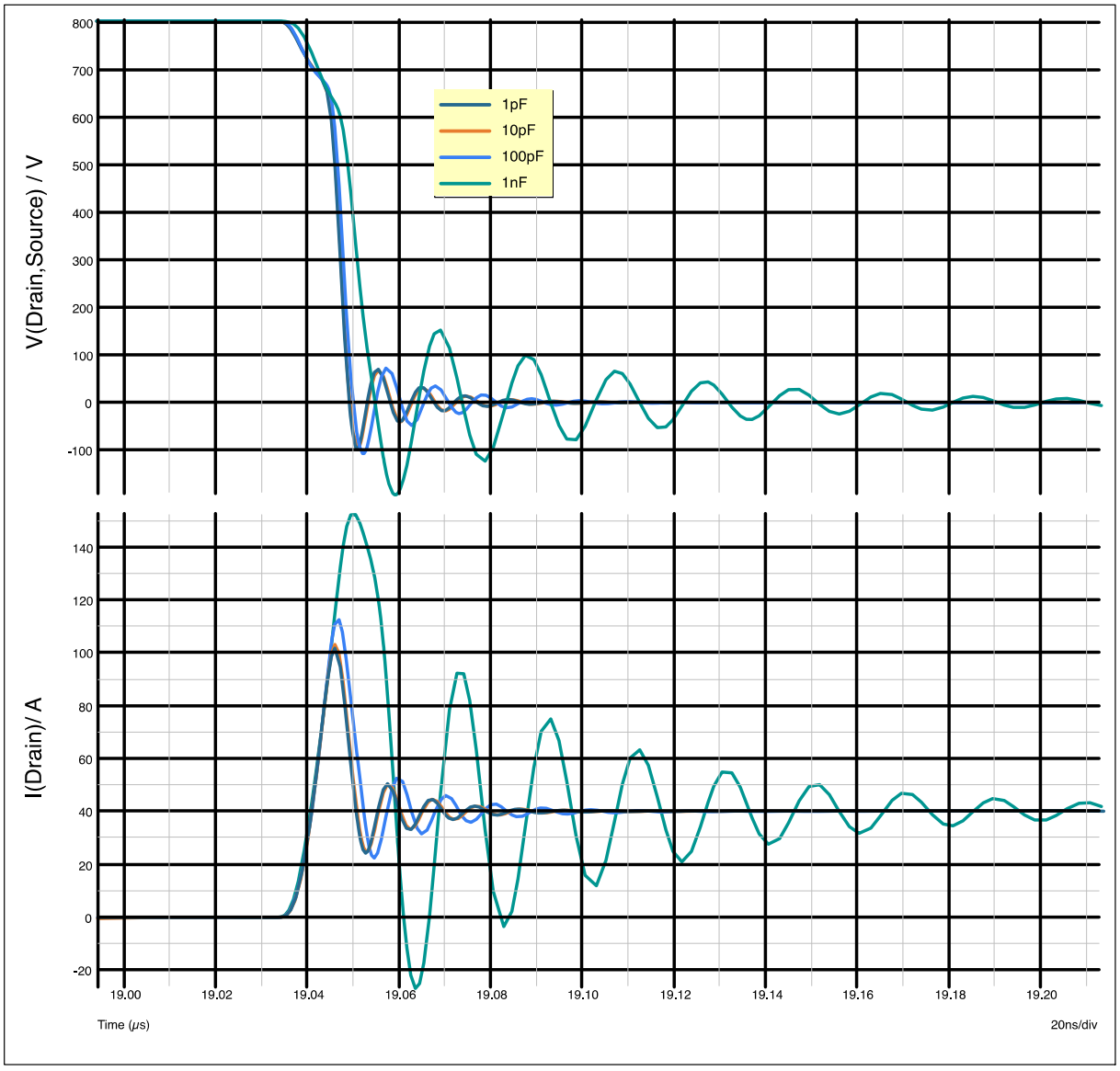

Figure 4. Drain Voltage and Current at Turn−On depending on Switching Inductor Parasitic Capacitor Values

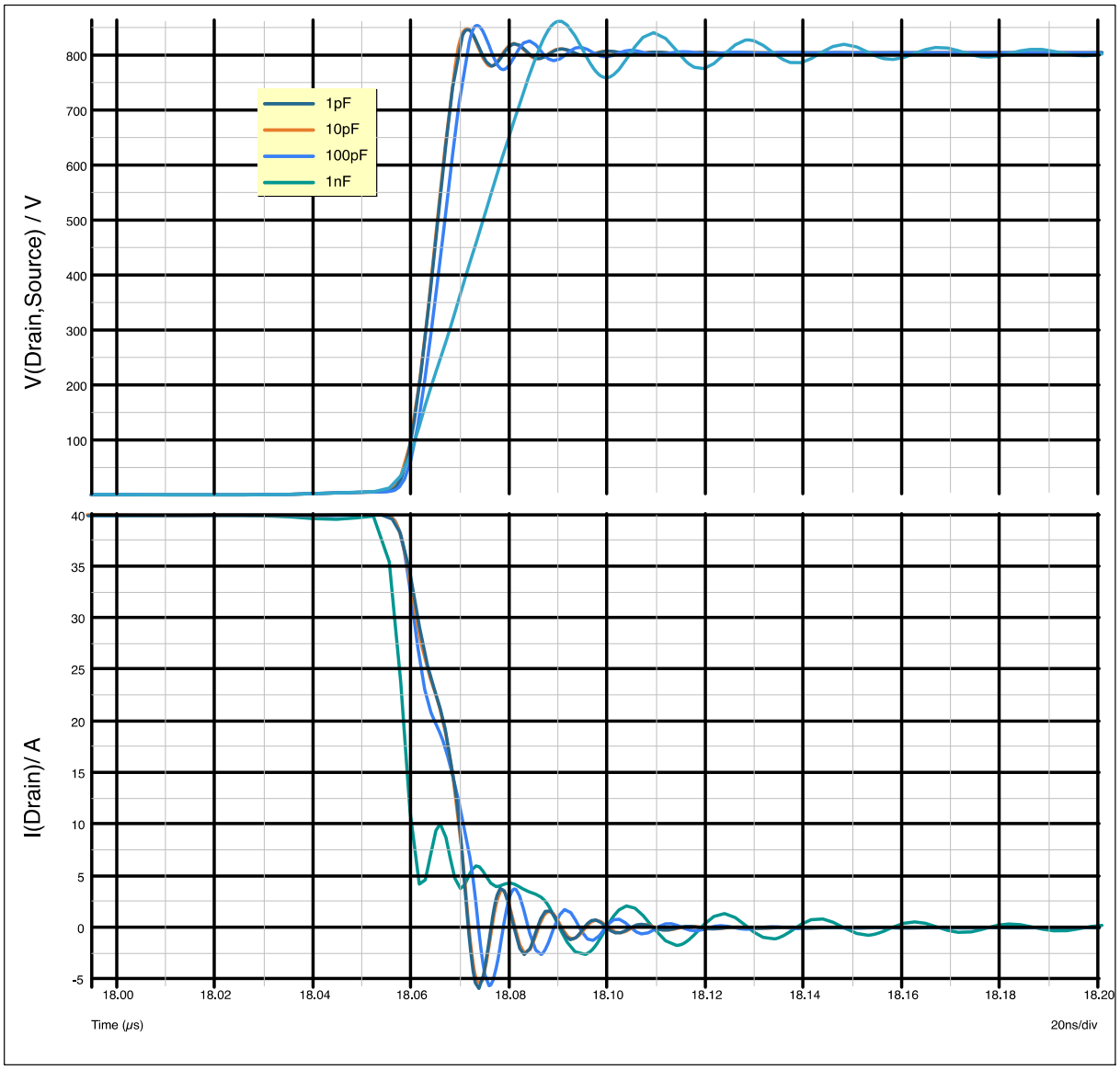

Figure 5. Drain Voltage and Current at Turn−Off Depending on Switching Inductor Parasitic Capacitor Values

At turn−on, the big current spike increases due to the inductor parasitic capacitor. In a double pulse tester, it is easy to understand this parasitic capacitor increases the output capacitance C_{OSS}. At turn−off, the drain voltage rise time increases with the capacitor value. This is normal because more time is needed to charge the larger capacitor with a fixed current value.

We can see the impact of the inductor parasitic capacitor on the Eon losses in the next figure. With the very bad inductor, losses generated by the inductor parasitic capacitor are much higher than the native MOSFET capacitor (C_{OSS}). On Figure 6, we can that the MOSFET Eon losses are almost the double caused by the bad inductor.

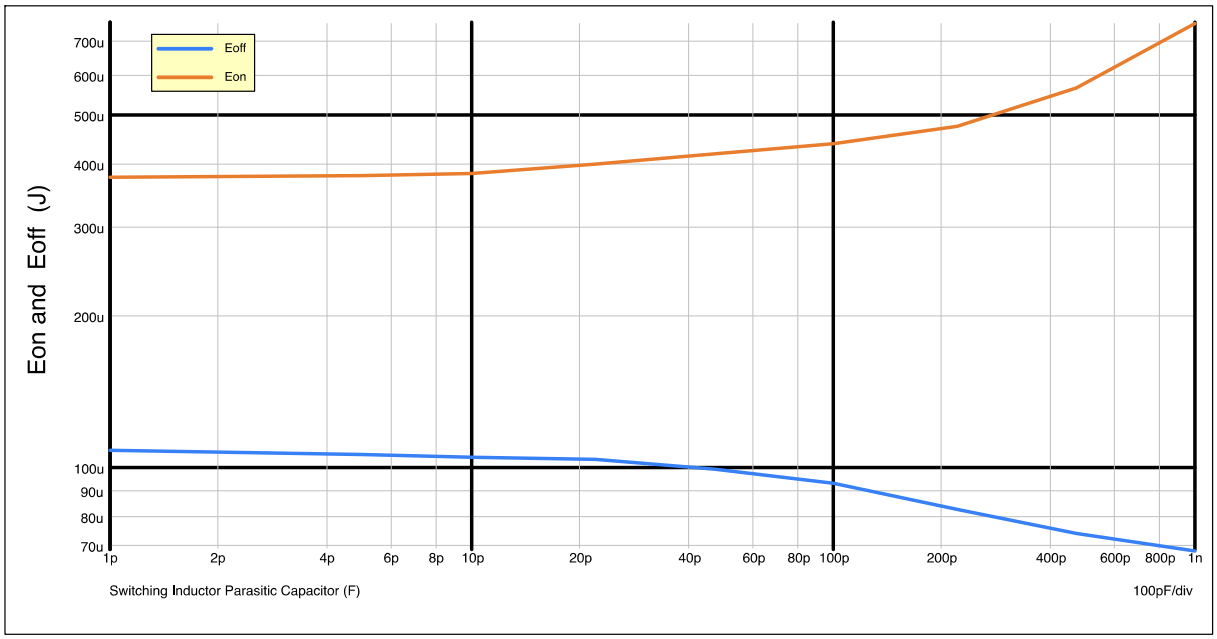

Figure 6. Switching Inductor Parasitic Capacitor Effect on Turn−On and Turn−Off Losses

The results or the effects will be the same in a “buck” stage. Considering a large decoupling capacitor on the input and at the output, the capacitors (C_{IN}, C_{OUT} and $C_{Parasitic}$) are in series. The equivalent capacitor has a value in the range of the inductor parasitic capacitor which should be the smaller. This equivalent capacitor is in parallel with the MOSFET as shown in the next theoretical schematic (Figure 7).

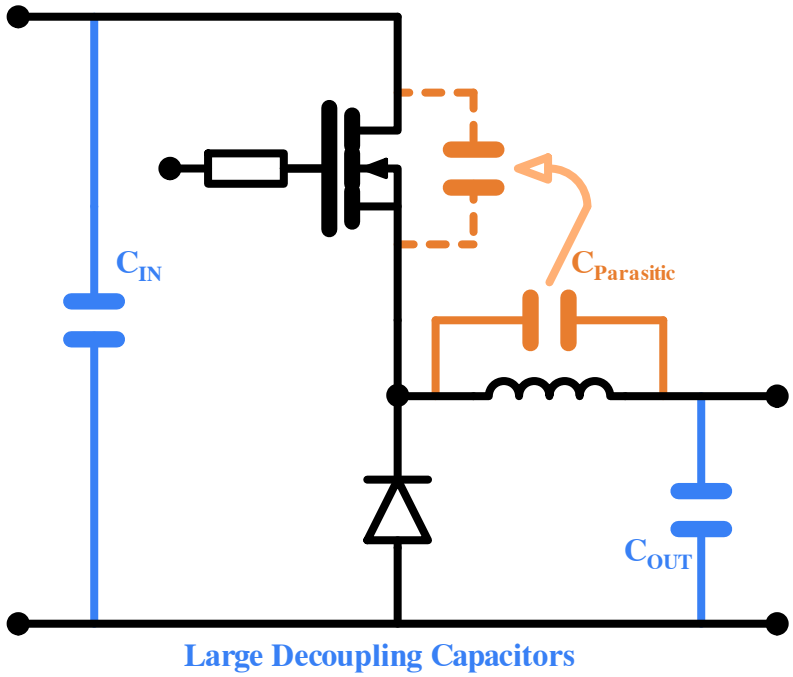

Figure 7. Switching Inductor Parasitic Capacitor Equivalent Effect

The use of planar inductors in small compact DC−DC converters induces this phenomenon as layers (or turns) are stacked with a very small inter−layer distance leading to a big parasitic capacitor of the inductor. Already at low voltages, this parasitic capacitor can be an issue. With high voltage applications deployed using SiC, the effect of the inductor’s parasitic capacitor is even more significant.

PCB Leakage Inductance

The second parasitic element we will discuss here is the PCB leakage inductor. All experimental power designers know that the smaller the switching loop is, the better are the performances. However, in some case, to reduce EMI, a ferrite bead is used to slow down the current ramping edge by creating a small delay to allow the drain voltage to fall. Slowing down the current ramp to allow the voltage to reach "zero" is also beneficial to reduce losses. The following experiment uses an ideal double pulse tester with added variable leakage inductance in the switching loop (See Figure 8). This will model larger switching loops where the the distance between the various PCB components involved in the switching are increasingly further from each other.

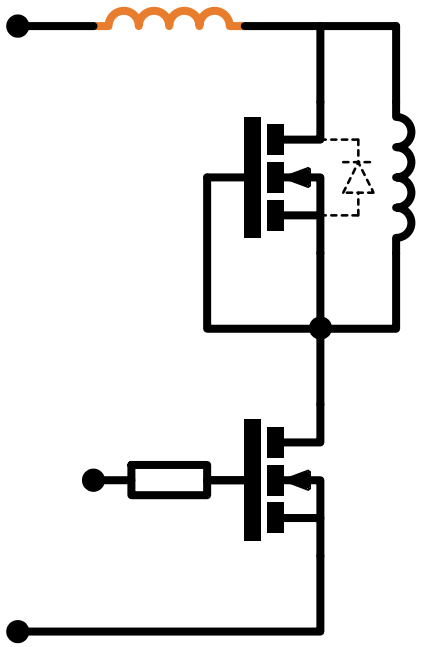

Figure 8. Layout Parasitic Inductor to Simulate Losses on a Double Pulse Tester

Figures 9 and 10 show the Drain current and Drain−to−Source voltage change variation with the PCB leakage inductance.

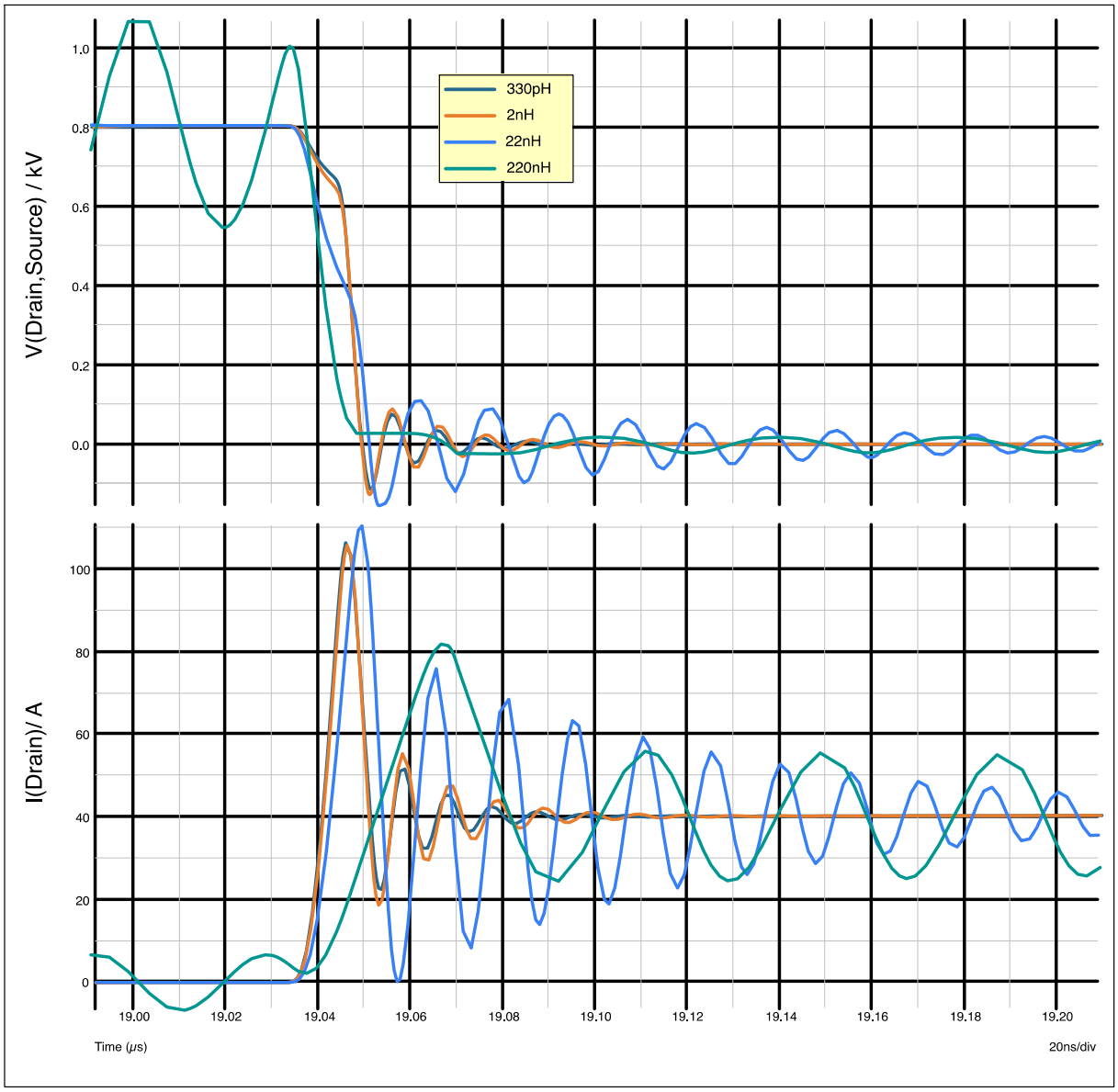

Figure 9. Drain Voltage and Current at Turn−On Depending on Layout Parasitic Inductor Values

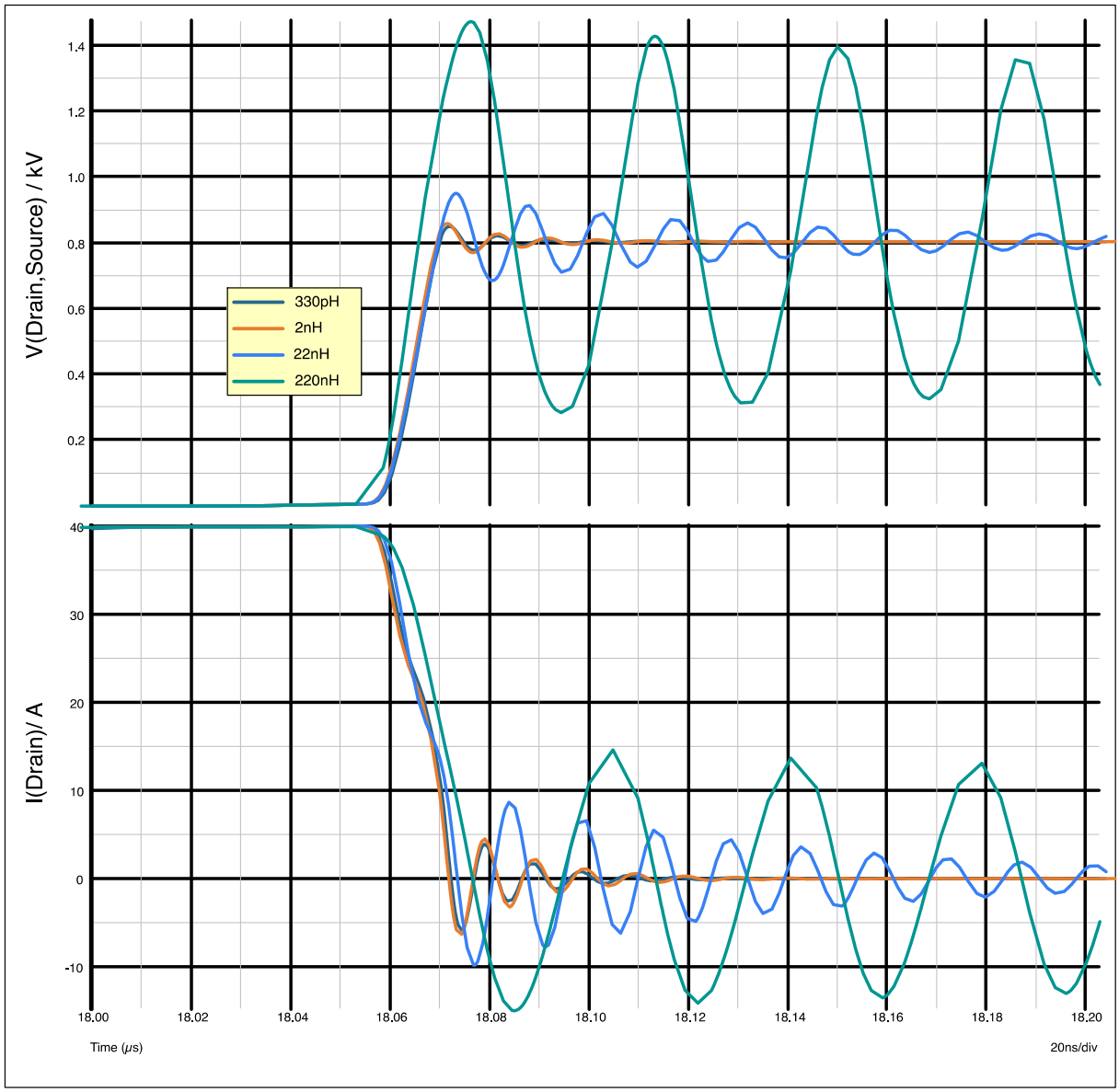

Figure 10. Drain Voltage and Current at Turn−Off Depending on Layout Parasitic Inductor Values

At turn−on as expected, the voltage falling slope (dV/dt) is similar while the ramping slope of the current (dI/dt) is slower when the PCB inductor increases. This creates a delay, and so, decreases the Eon losses like in a soft switching case. At turn off, the current falling edge is delayed compared to the voltage edge rising which induces more loss. The switching losses are plotted in Figure 11.

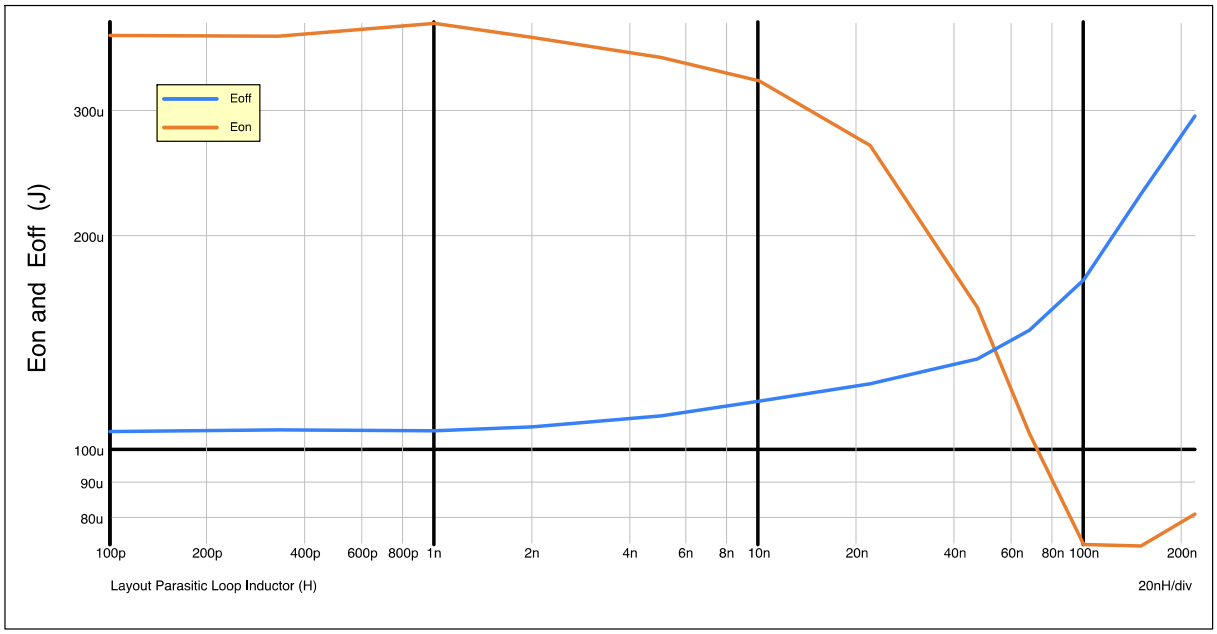

Figure 11. Layout Parasitic Inductor Effect on Turn−On and Turn−Off Losses

Since Eoff is generally lower than Eon, is there a compromise possible to decrease the total losses Etotal?

Figure 12 plots the turn−on, turn−off and total switching losses as a function of the PCB leakage inductor.

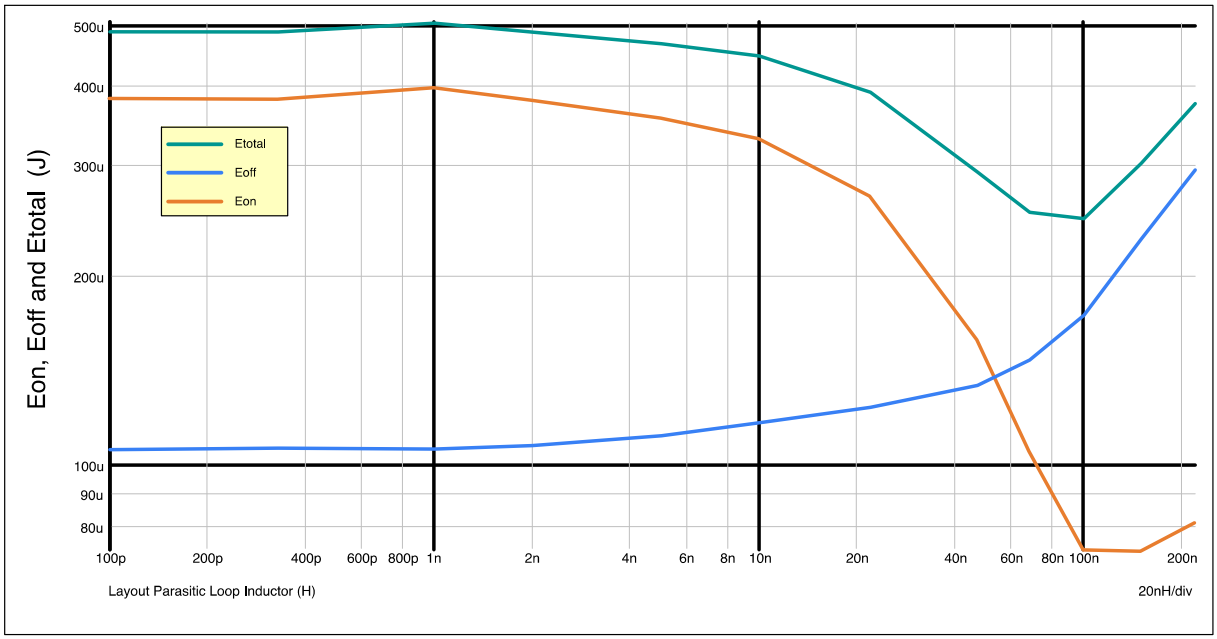

Figure 12. Layout Parasitic Inductor Effect on Turn−On, Turn−Off and Total Switching Losses

There is what appears to be an “optimum” value for Total Switching losses with 100 nH layout parasitic inductor. However, this large inductor value induces large ringing as shown by the green curves in Figures 9 and 10. The EMI content of the current and voltage is significant and will also impact the design, requiring complex filtering. A suitable compromise is difficult to find since EMI issues are always tricky to solve.

Decoupling Capacitor

As realized with the inductor parasitic capacitor, the decoupling capacitor can play the same role because due to the series capacitor network. In this case, the capacitor should be small and in the same range as the inductor parasitic capacitor. However, what happens if the switching inductor is almost ideal? It is intuitive that the bus voltage will decrease. In real world applications, a designer needs to

find a compromise between the number of decoupling capacitors and the voltage drop on the bus. This compromise should be sought to minimize the effect on the losses.

The impact on losses is evaluated through deploying the same double pulse tester and including an input filter with varying decoupling capacitor. (See Figure 13)

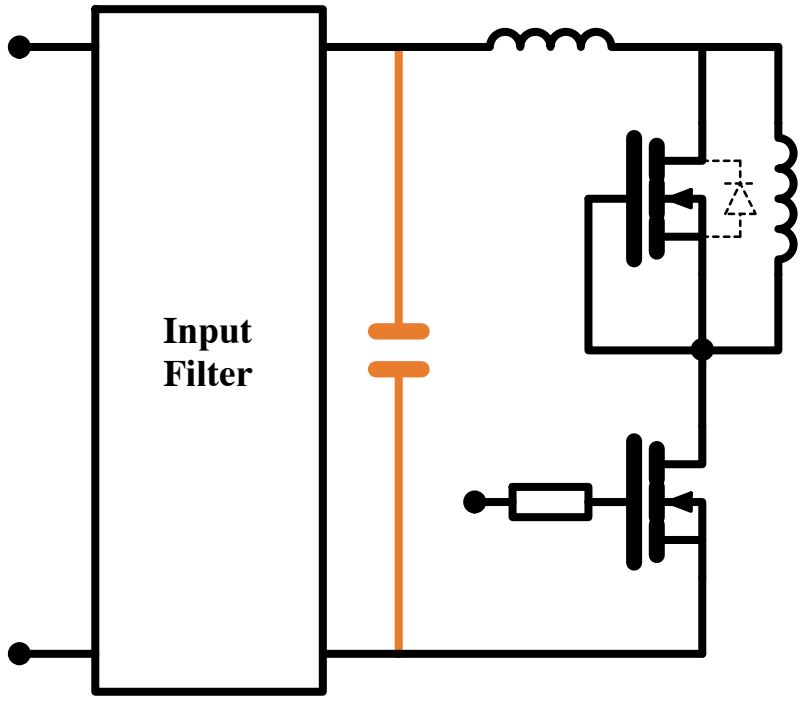

Figure 13. Decoupling Capacitor and Input Filter to Simulate Losses on a Double Pulse Tester

Figure 14 displays the same curves (Eon, Eoff) as a function of the decoupling capacitor value.

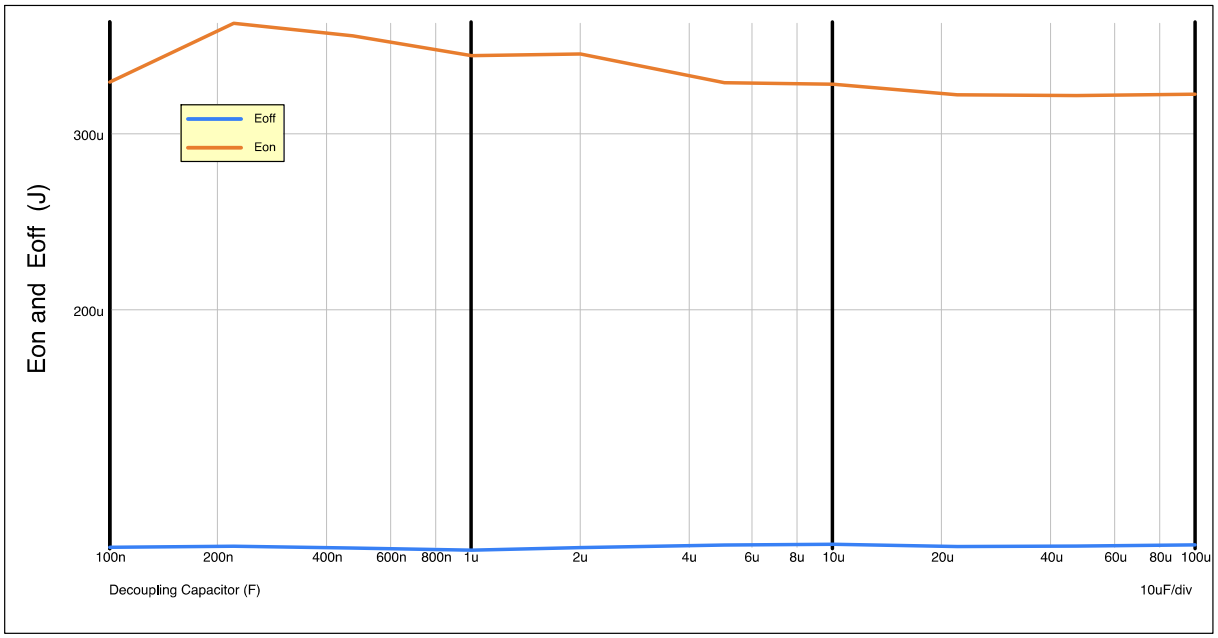

Figure 14. Decoupling Capacitor Effect on Turn−On and Turn−Off Losses

Below 200 nF, Eon decreases since the Drain voltage also decreases dramatically. Between 1 μF and 10 μF Eon decreases slightly which is mostly insignificant. Above 10 μF, the effect on Eon is negligible. So, a decoupling capacitor value in between 1 μF to 10 μF for a current in the range of 40 A is suitable.

Shunt Resistor

A shunt resistor to sense current has resistive losses which can slightly damp (due to a relatively low value) the resonant network composed of the PCB leakage Inductor, the load inductor capacitor, and the decoupling capacitor.

Including a shunt resistor in the double pulse tester demonstrates if the shunt (and its position) will affect the losses. (See Figure 15)

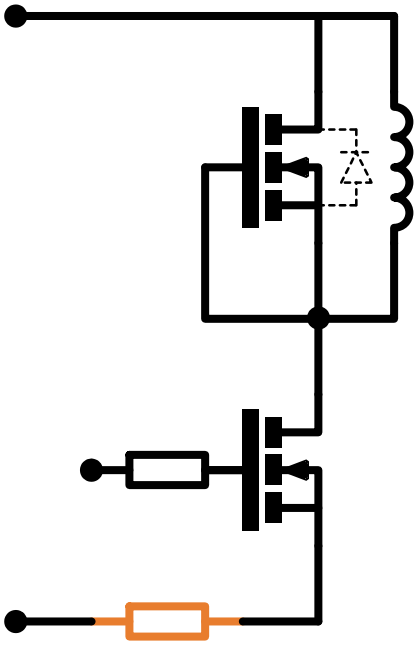

Figure 15. Shunt Resistor to Simulate Losses on a Double Pulse Tester

Figure 16 plots the losses as a function of the Shunt value.

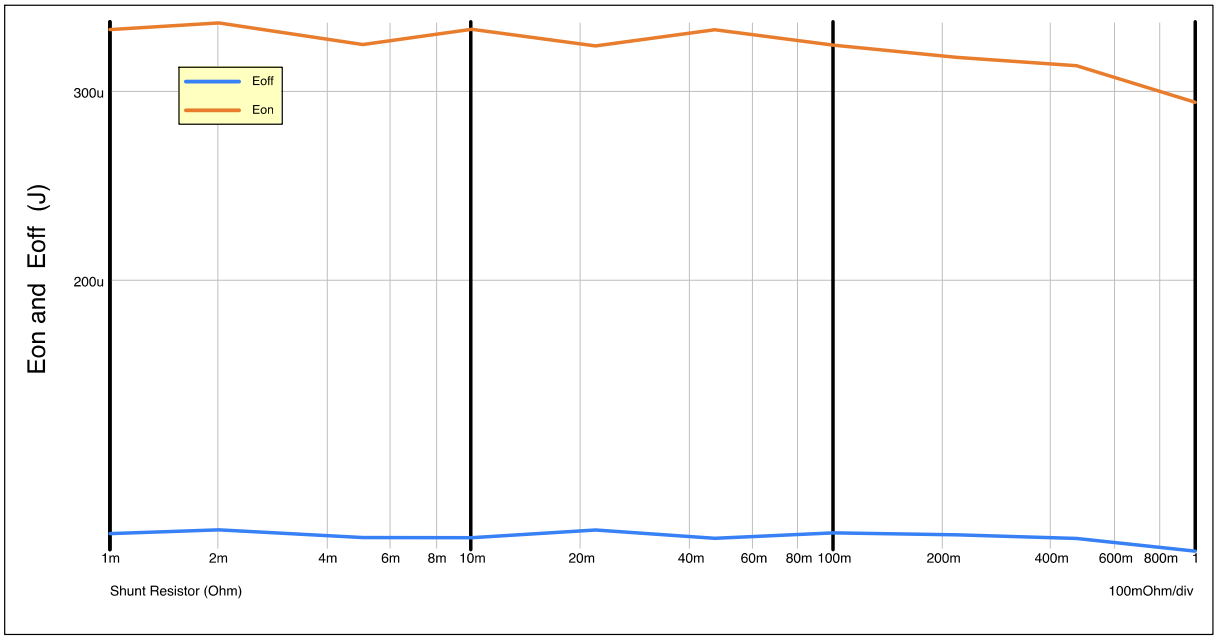

Figure 16. Shunt Resistor Effect on Turn−On and Turn−Off Losses

Unrealistic large shunt values for a current of 40 A decrease Eon and Eoff losses. However this energy loss decrease does not compensate larger the conduction losses of the shunt when its values are above 100 mΩ.

Measurement approach.

To generate Eon and Eoff that represent the device losses, a double pulse tester must be built as ideal as possible with minimal parasitic effects. In this case, an inductor with a very low parasitic capacitor, a very short switching loop and a high decoupling capacitor value are implemented. The cost or size of any given component is irrelevant since the setup is not made for large scale production.

A Half− or Quarter−Bridge structure is used based on the application focus. For Solar Boost, Quarter−Bridge is preferred. For other applications, Half−Bridge is preferred.

Is double pulse tester a good way to measure losses?

The answer to the question is YES, depending on the quality of the tester, if we want to measure the lowest losses with minimal effect of parasitic elements. **onsemi**'s advanced double pulse tester is a very good tool for this purpose. It allows the comparison of the **onsemi** portfolio between various die sizes (and so $R_{DS(on)}$) and packages from generation to generation.

However, a follow−on question is what losses matter to the customer and their applications? The **onsemi** tester is one of an infinite number of parasitic boundary conditions in a double pulse test environment. Clearly when a customer evaluates losses in their real application, the device will not operate in the **onsemi** tester environment. The loss values given in the datasheet for example will not reflect the losses in the customer environment.

The best way to evaluate losses in the customer application is to introduce the precise parasitic elements in a specific double pulse tester. In other words, this double pulse tester becomes specific to your application. However, it is not practical to make a new measurement set up or tune an existing setup for every new design or new customer applications. In addition, one must consider when there are several stages, for example in a Dual Active Bridge. Here, the primary and secondary could be different in terms of operating point, layout, and elements involved such as decoupling capacitor and the inductor parasitic capacitor measured on a particular side. As a result, the double pulse tester needs to be tuned to evaluate losses in each stage and configuration. Quickly one realizes this is a never−ending job by itself.

Is there another way for a power electronic designer to obtain highly accurate loss models for their application?

An alternative to this complex and limited measurement−based approach is a virtual platform based on Simulation. Such an approach can only work with very accurate simulation models for the components. Simple stated simulation benefits are governed by the well known "Garbage−in, Garbage−out" theory. The proven Physical and Scalable SPICE[1,2,3,4] models provided by **onsemi** enable designers to realize the most accurate loss models for their application through fast simulations as opposed to time consuming, expensive measurement based methods. Designers can build parametric simulations to run several cases in one cycle and obtain results rapidly through automation. Realizing the abundance of benefits to our customers of such an approach, **onsemi** has introduced the Self−Service PLECS Model Generator (SSPMG), available on **onsemi**.

Extended Switching Loss Simulation Schematic PLECS Models

In SSPMG, **onsemi** has included more than 30 parameters to tune the double pulse tester simulation schematic to extract SiC MOSFET discrete and power module losses. Figure 18 displays the schematic for discrete products. All the parameters are made to reflect all particular cases and all possible stages in the applications. In addition, gate drive voltages can be customized.

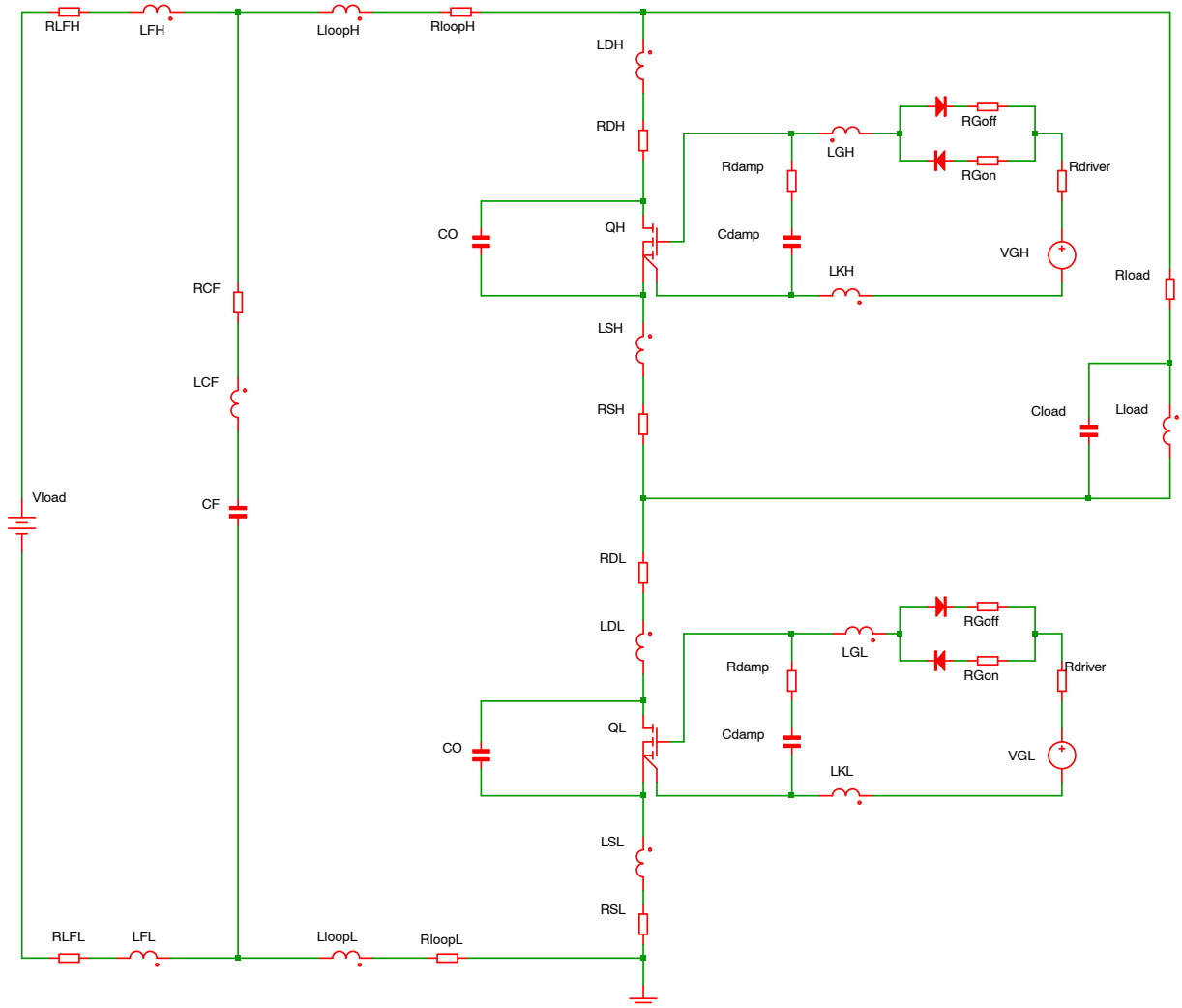

Figure 17. Discrete Product Classical Double Pulse Tester Schematic with Parasistics Introduced to Reflect Real Applications

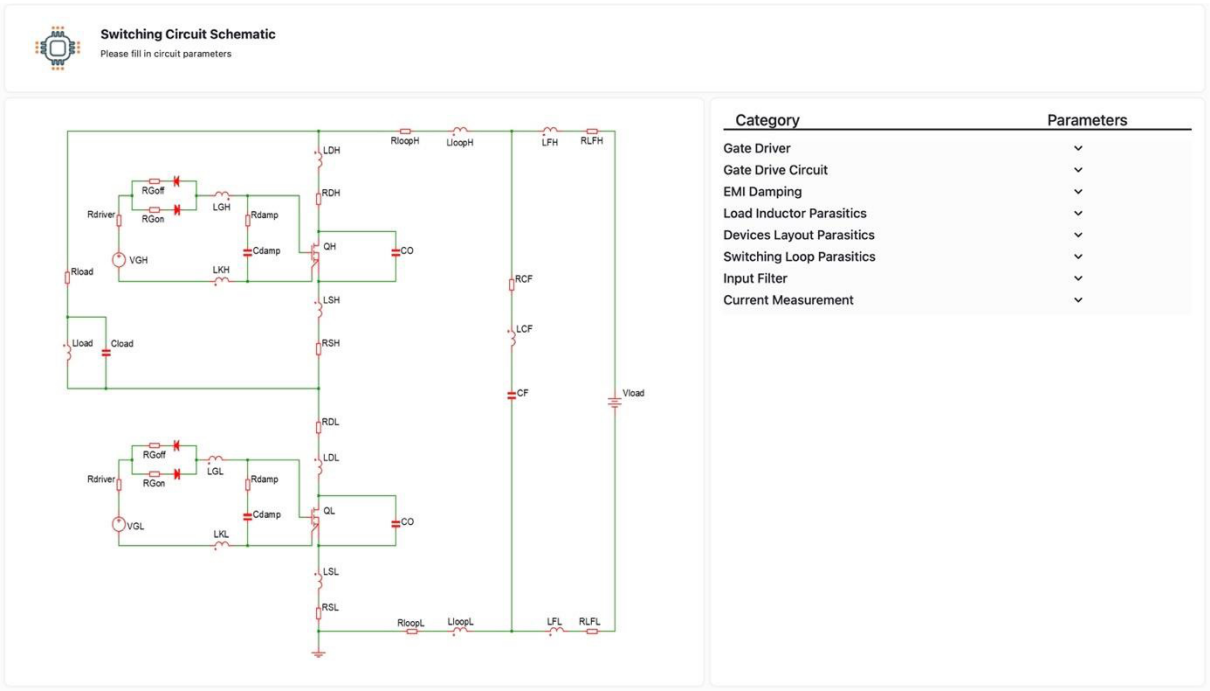

Figure 18. Discrete Product Double Pulse Tester Schematic for PLECS Model Generation

To generate the PLECS model, the user enters the parameter values for the schematic in the table shown on the right side of Figure 18. The complete list is shown in Figure 19.

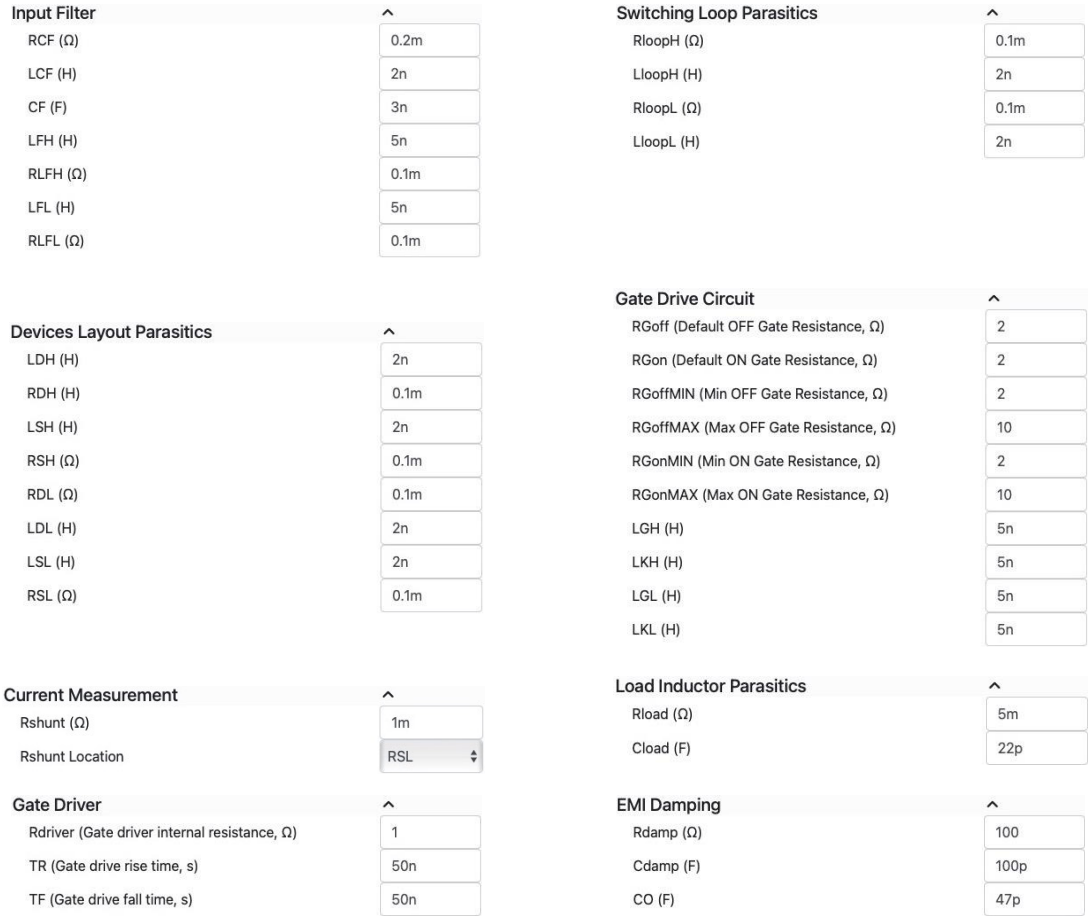

Figure 19. Example Parameters Values for the Double Pulse Tester to Generate the PLECS Model

The user enters parameters based on engineering expertise, knowledge of layout limits, parasitic elements reasonable values, stage structure, …

Not all parameters are needed and may not be present on the user application case. For example, a capacitor in parallel between drain−to−source may or may not be used to damp drain voltage dv/dt for EMI purpose.

By default, most of the parameters are set to zero. In this case, it reflects only the device performances and not the device performances in a particular case of use.

Figure 20 displays the SSPMG operating range definition used to generate the PLECS model for hard switching.

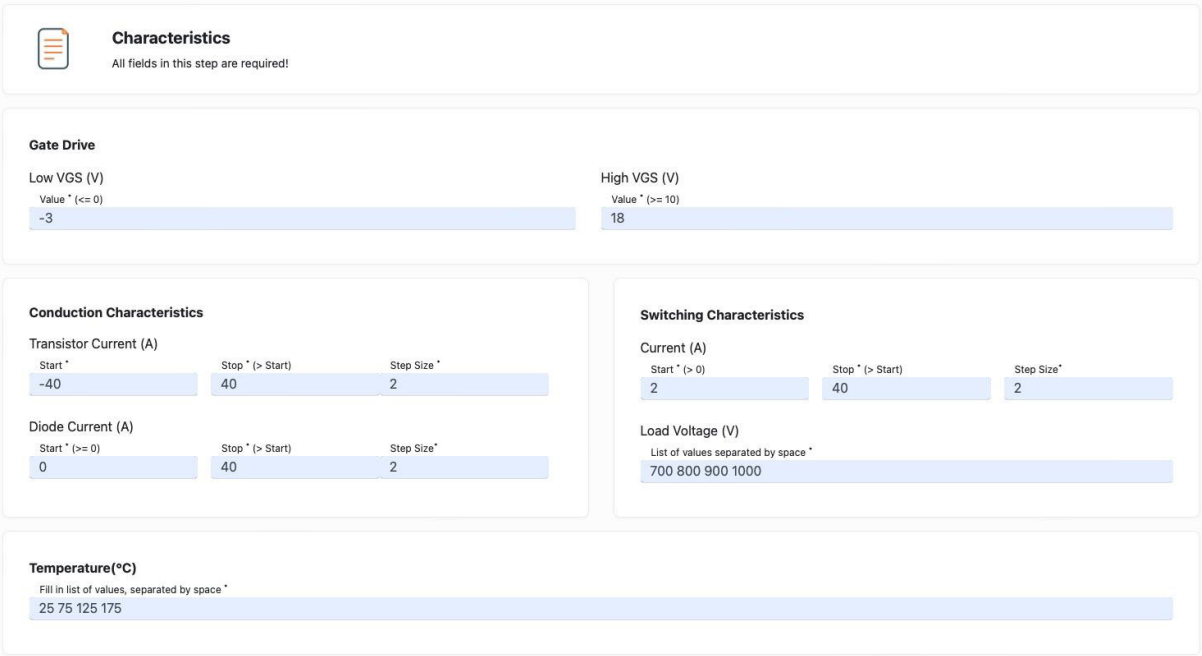

Figure 20. Operating Range Setting for Hard Switching Only

Improving Accuracy by Dense Loss Tables in PLECS Models

As stated earlier, semiconductor losses both conduction and switching are highly nonlinear with respect to current, voltage, and temperature. Typical datasheet based PLECS models are not very dense due to the time−consuming nature of the measurements. This can directly lead to inaccurate interpolation and highly inaccurate extrapolation during circuit simulation as shown in Figure 21. In SSPMG, the user can set the range (within device specification limits) and the density of the loss tables according to their needs. The results are obtained in minutes. With this capability, the user can ensure accurate interpolation and no extrapolation by PLECS during circuit simulation. The default PLECS models in the Elite Power Simulator are already dense in nature.

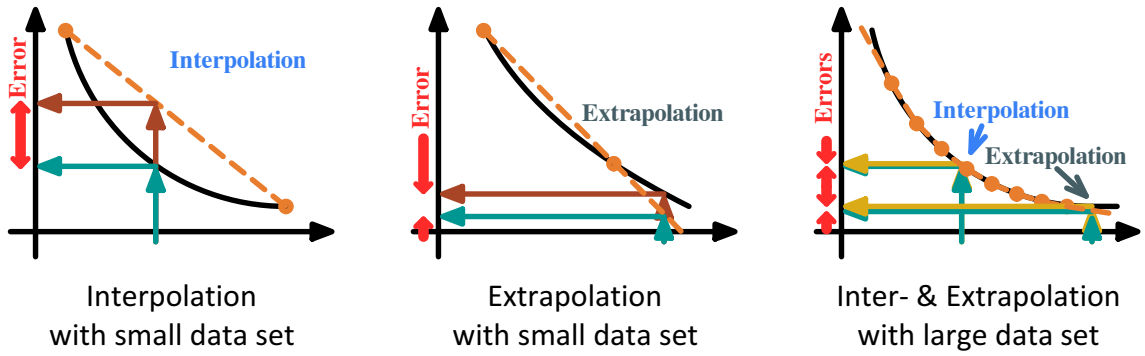

Figure 21. Interpolation and Extrapolation Errors with Small and Large Data Set

With a dense data set, interpolations made by PLECS to evaluate switching and conduction losses will be much more accurate. This in turn ensures accurate application analysis for losses, efficiency, and temperature.

Including Soft Switching in PLECS Model

One missing and critical information that is not obtained by the classical double pulse tester is the losses in case of soft switching operation. The classical double pulse tester is only valid in hard switching.

All designers familiar with soft switching techniques (either full resonant stage like LLC, CLLC, etc. or transition resonant stage like Full Bridge Phase Shifted or Dual Active Bridge) know that the soft switching is achieved if enough resonant energy is available before the switching event happens. If not, partial soft switching can be achieved if energy is lower than needed, and even hard switching in the case of the resonant tank has no resonant energy at all.

Here are the basic diagrams (See Figures 22 and 23) that show the current flow for a hard and a soft switching transition.

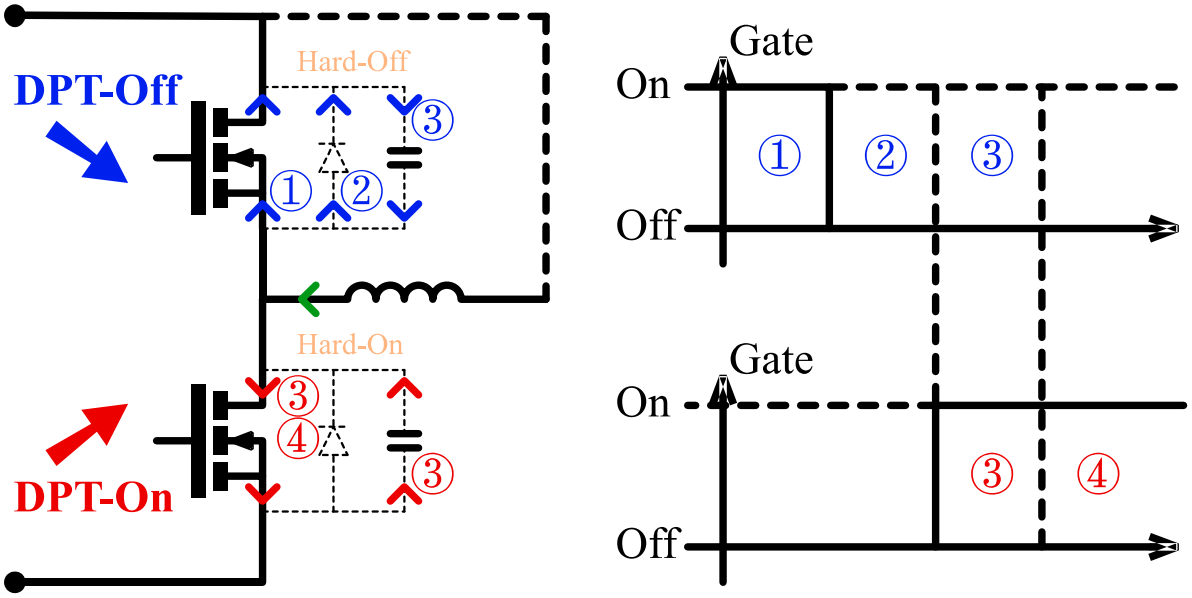

Figure 22. Hard Switching Transition

In Hard switching transition, the energy stored in the device that turns on is lost in the device that turns on. In soft switching this energy is transferred from the device that turns on to the one that turns off, as it can be seen in Figure 23 compared to Figure 22.

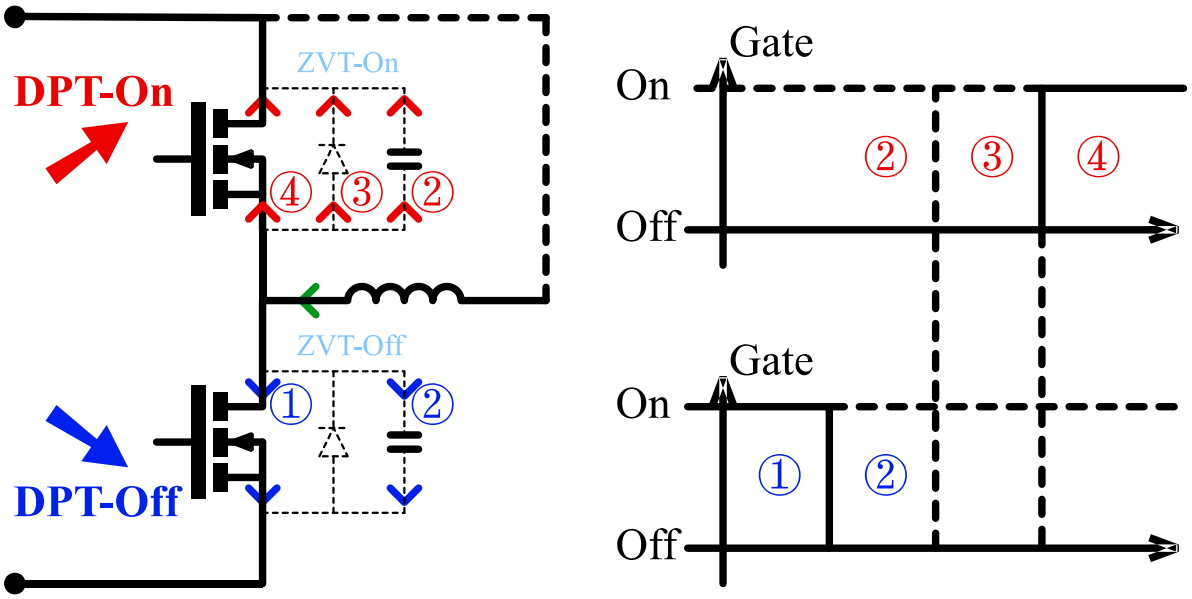

Figure 23. Soft Switching Transition

The switching events are resumed below the Figure 24. For the turn−off event, the switching current direction shown is the one before the switching event or turn−off. For the turn−on event, the switching current direction shown is the one after the switching event or turn−on.

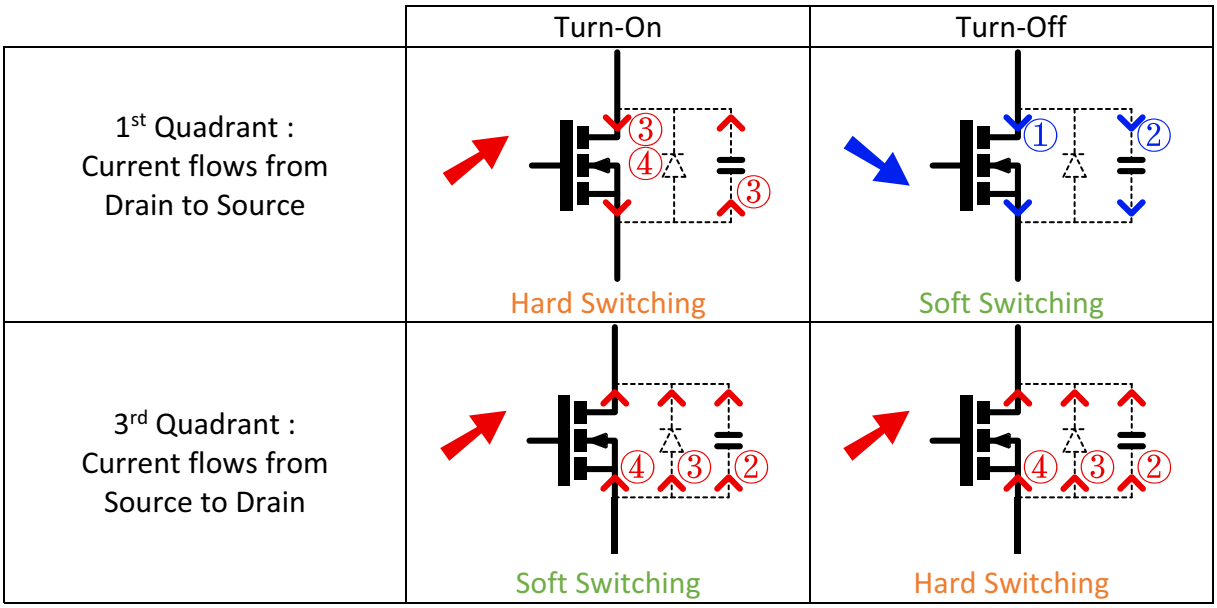

Figure 24. Switching Event Synthesis

To include PLECS models valid for soft switching in the new **onsemi** Elite Power Simulator and SSPMG, a small modification is introduced in the classical double pulse tester (see Figure 17) to operate in Soft Switching (See Figure 25). Additional parameters are included to capture the dI/dt in the resonant inductor when the switching event happens.

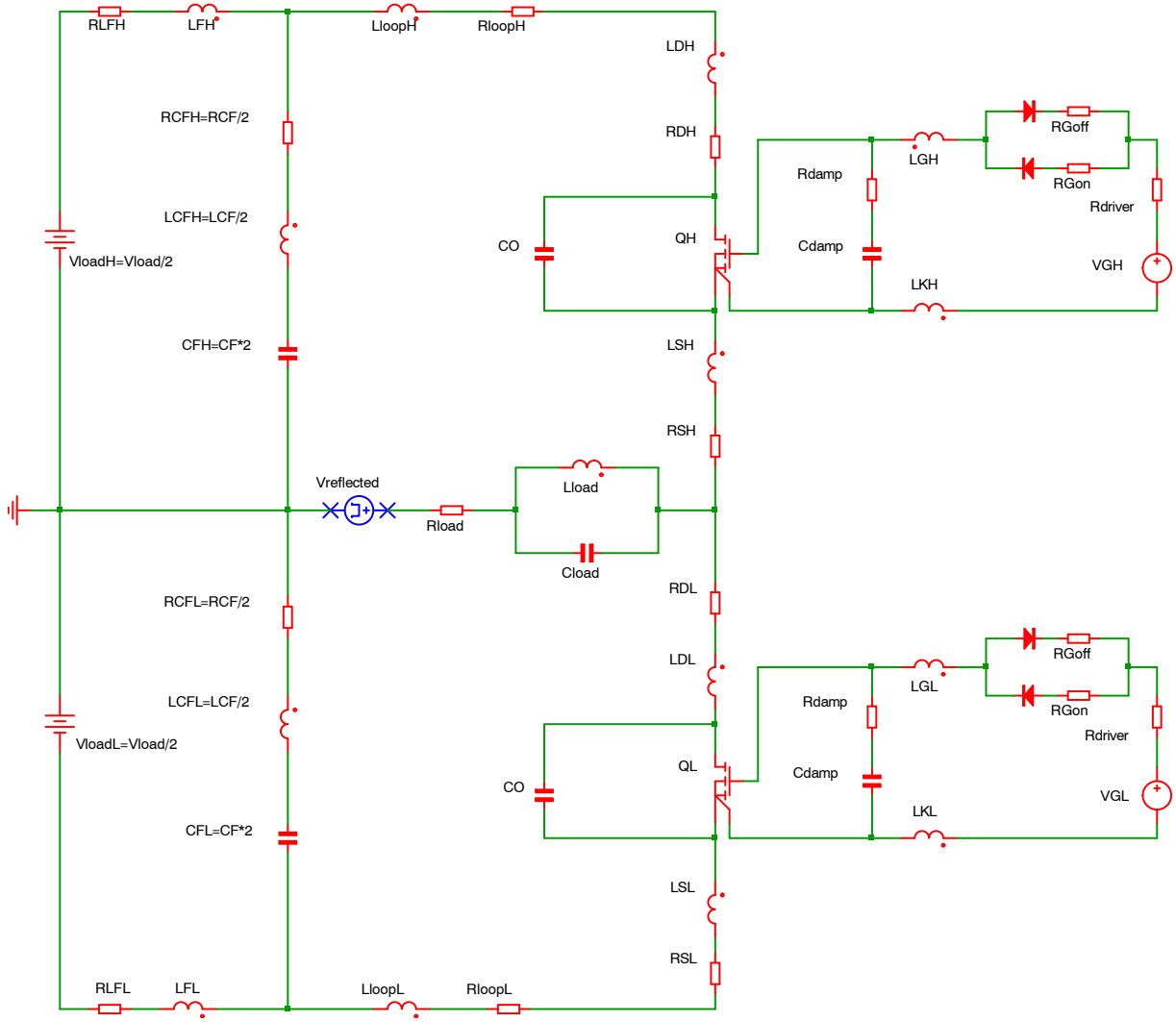

Figure 25. Discrete Product Soft Switching Double Pulse Tester Schematic with Parasistics Introduced to Reflect Real Applications

This dI/dt is directly link to the resonant inductor voltage by the Faraday's law of induction E=L*dI/dt. The "Reflected" voltage source represents the transformer voltage and helps to set the dI/dt in the resonant inductor.

The user also enters the maximum dead time allowed between high side and low side switches for the resonant transition to occur. The user can select Hard or Soft switching type in SSPMG. All the additional soft switching related parameters appear automatically when the user enters selects Soft Switching operation as shown in Figure 26.

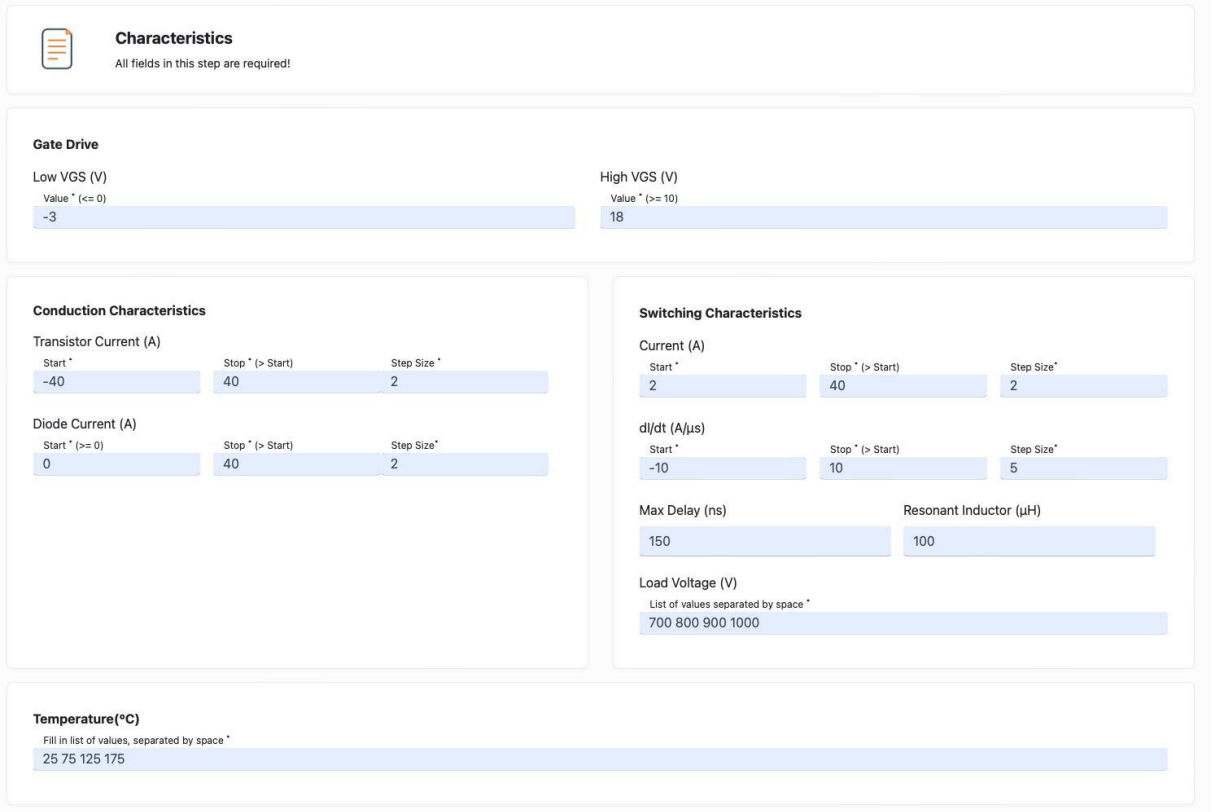

Figure 26. Operating Range Setting for Hard Switching and Soft Switching

With those extra parameters, **onsemi** enables customers to predict losses in any switching cases that are Hard, Soft, or Partial Soft switching.

Designers can now know the real performances or losses of their applications for a particular design or set of parameters. They can also see at which operating points the transition between modes happens and the impact on losses, efficiency, or temperature.

onsemi makes the evaluation of soft switching topologies performances easy in a very accessible and simple manner with SSPMG for loss model generation and the Elite Power Simulator for applications' simulation.

Corner PLECS Model Generation

Conventional PLECS models based on measurements are valid for the typical or nominal process case in manufacturing. **onsemi** has developed accurate corner and statistical SPICE models for SiC MOSFETs based on real manufacturing distribution. Leveraging these device level corner models, **onsemi** provides users of SSPMG and the Elite Power Simulator the capability to explore their application robustness to semiconductor process variation at the system level. The uncorrelated process parameters such as gate oxide thickness, electron mobility, and epitaxial region doping concentration (to name just a few), work together to produce correlated changes in the electrical parameters such as threshold voltage V_{th}, $R_{DS(on)}$, and capacitances. The variations of the electrical parameters in turn induce variations in the conduction and switching energy losses which are contained within the PLECS models. Table 1 captures the physically based correlation of the SiC MOSFET electrical parameters and PLECS models. Physics dictates that worst case conduction and worst−case switching losses do not happen simultaneously for example.

Table 1. PLECS CORNER MODELS

	Electrical Parameters			PLECS Model	
Corner Case	**V_{th}**	**$R_{DS(on)}$**	**Capacitance**	**Conduction Losses**	**Switching Energy Losses**
Nominal	Nominal	Nominal	Nominal	Nominal	Nominal
1	High	High	Low	Worst	Best
2	Low	Low	High	Best	Worst

Depending on the application, the influence of conduction and switching energy losses on the overall system performance will vary. The **onsemi** corner PLECS models provide the user the flexibility to investigate the entire correlated space.

When generating a custom PLECS model in SSPMG, the user can easily select the corner case as shown for Corner Case selection in Figure 27.

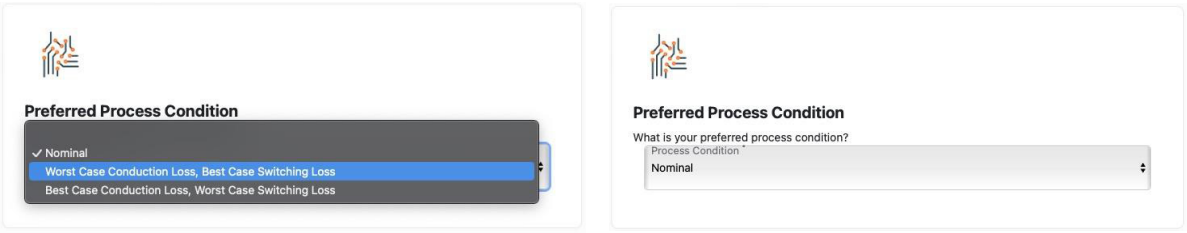

Figure 27. Selecting Process Corner Condition in SSPMG

In the Elite Power Simulator, the user can select corner cases for the default PLECS models in the Device Configuration step.

Conclusion

onsemi is enabling our customers to be successful in their system level simulation through advancing the state of the art in PLECS model generation and simulation. Through the breakthrough SSPMG platform, the influence of the customer application parasitic components, dense operating conditions, and semiconductor process variation are incorporated in the PLECS models. All these features are not possible through brute force measurement techniques. Further, customers are enabled for the first time to generate PLECS models accurate for Soft Switching. In many instances, the application designer can avoid huge redesigns due to bad estimations and longer design cycles than expected.

The new Elite Power Simulator provides a tool to quickly estimate losses in an accurate manner due to the high fidelity of the embedded PLECS models. The user can upload SSPMG based models directly into the Elite Power Simulator, all online. With that said, the Elite Power Simulator tool enables the user to anticipate design performances (Losses, Temperature, ZVT/ZVS, Efficiency) in combination with the fast speed of PLECS online. For a new design, the compromise between several Elite SiC MOSFETs or Modules can be analyzed quickly. Not only that, the trade−offs with other parasitic components in the design or schematic that interact with the switches can be evaluated.

References

1. An Introduction to Physical Scalable Models for Wide Bandgap Power Semiconductor − Part One (Blog article) https://www.onsemi.com/blog/industrial−cloud−power/wide−band−gap−ecosystem−part−i
2. Wide Bandgap Power Semiconductor: Silicon Carbide MOSFET Models − Part Two − (Blog Article) https://www.onsemi.com/blog/industrial−cloud−power/wide−band−gap−ecosystem−switches−disruptive−environments
3. Wide Bandgap Semiconductor Simulation Model Verification − Part Three − (Blog Article) https://www.onsemi.com/blog/industrial−cloud−power/wide−bandgap−semiconductor−simulation−model−verification
4. Physically Based, Scalable SPICE Modeling Methodologies for Modern Power Electronic Devices (White paper) − https://www.onsemi.com/pub/Collateral/TND6260−D.PDF
5. PLECS website : https://www.plexim.com/products/plecs
6. SiC Simulation − (White paper) https://www.onsemi.com/pub/collateral/tnd6395−d.pdf
7. Using Physical and Scalable Simulation Models to Evaluate Parameters and Application Results (White paper) − https://www.onsemi.com/pub/collateral/tnd6330−d.pdf
8. SiC MOSFET Corner and Statistical SPICE Model Generation − Proceeding of International Symposium on Power Semiconductor Devices and ICs (ISPSD)2020, pp. 154−147, September 2202 https://ieeexplore.ieee.org/document/9170091

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊