TSV791, TSV792

Datasheet

High bandwidth (50 MHz) low offset (200 µV) rail-to-rail 5 V op-amp

TSV791
SOT23-5

TSV792
DFN8 2x2 mm

TSV792
MiniSO8

TSV792
SO8

Features

- Gain bandwidth product 50 MHz, unity gain stable
- Slew rate 30 V/µs
- Low input offset voltage 50 µV typ., 200 µV max.
- Low input bias current: 2 pA typ.
- Low input voltage noise density 6.5 nV/√Hz @ 10 kHz
- Wide supply voltage range: 2.2 V to 5.5 V
- Rail-to-rail input and output
- Extended temperature range: - 40 °C to +125 °C
- Automotive grade version available
- Benefits:
  - Accuracy of measurement virtually unaffected by noise or input bias current
  - Signal conditioning for high frequencies

Applications

- High bandwidth low-side and high-side current sensing
- Photodiode transimpedance amplification
- A/D converters input buffers
- Power management in solar-powered systems
- Power management in automotive applications

Maturity status link
TSV791, TSV792

Related products	
TSZ181 TSZ182	Zero drift amplifiers with more power savings (3 MHz)
TSB712	36 V high-bandwidth amplifiers (6 MHz)
TSB7192	36 V high-bandwidth amplifiers (20 MHz)

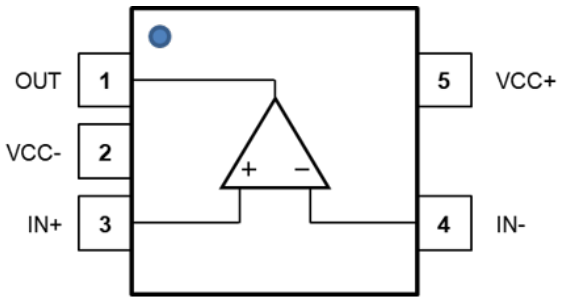
Description

The TSV791 and TSV792 are single and dual 50 MHz-bandwidth unity-gain-stable amplifiers. The rail-to-rail input stage and the slew rate of 30 V/µs make the TSV791 and TSV792 ideal for low-side current measurement. The excellent accuracy provided by maximum input voltage of 200 µV allows amplifying accurately small-amplitude input signal. The TSV792 can operate from a 2.2 V to 5.5 V single supply; it can typically handle an output capacitor up to 1 nF and is fully specified on a load of 22 pF, therefore allowing easy usage as A/D converters input buffer.

1 Pin description

1.1 TSV791 single operational amplifier

Figure 1. **Pin connections (top view)**



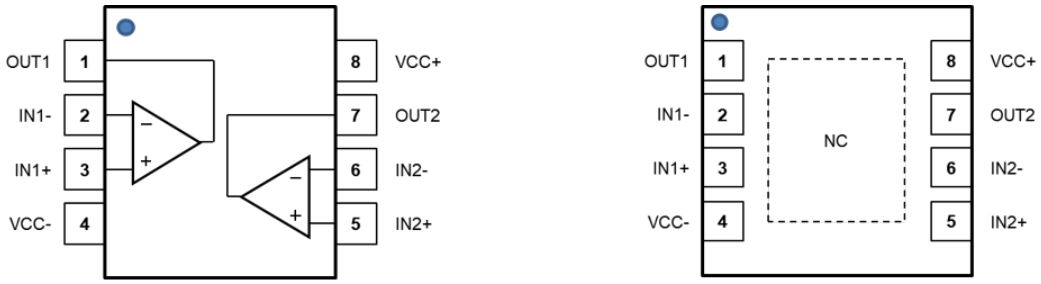
SOT23-5

Table 1. **Pin description**

Pin n°	Pin name	Description
1	OUT	Output channel
2	VCC-	Negative supply voltage
3	IN+	Non-inverting input channel
4	IN-	Inverting input channel
5	VCC+	Positive supply voltage

1.2 TSV792 dual operational amplifier

Figure 2. Pin connections (top view)



MiniSO8 and SO8

DFN8 2 x 2 mm (1)

1. The exposed pad of the DFN8 2x2 can be connected to VCC- or left floating.

Table 2. Pin description

Pin n°	Pin name	Description
1	OUT1	Output channel 1
2	IN1-	Inverting input channel 1
3	IN1+	Non-inverting input channel 1
4	VCC-	Negative supply voltage
5	IN2+	Non-inverting input channel 2
6	IN2-	Inverting input channel 2
7	OUT2	Output channel 2
8	VCC+	Positive supply voltage

2 Absolute maximum ratings and operating conditions

Table 3. Absolute maximum ratings

Symbol	Parameter (1)	Value	Unit
V_{CC}	Supply voltage	6	V
V_{id}	Input voltage differential (V_{IN+} - V_{IN-}) (2)	$\pm V_{CC}$	V
V_{in}	Input voltage	(V_{CC-}) - 0.2 to (V_{CC+}) + 0.2	V
I_{in}	Input current	±10	mA
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{th-ja} (3)	Thermal resistance junction-to-ambient		°C / W
	SOT23-5	250	
	DFN8 2x2	57	
	MiniSO8	127	
	SO8	125	
R_{th-jc} (4)	Thermal resistance junction-to-case		°C / W
	SOT23-5	TBD	
	DFN8 2x2	TBD	
	MiniSO8	51	
	SO8	TBD	
ESD	HBM: human body model (industrial grade) (5)	4	kV
	HBM: human body model (automotive grade) (6)	4	kV
	CDM: charged device model (7)	1	kV

1. *All voltage values are with respect to the VCC- pin, unless otherwise specified.*
2. *The maximum input voltage differential value may be extended to the condition that the input current is limited to ±10 mA.*
3. *R_{th-ja} is a typical value, obtained with PCB according to JEDEC 2s2p without vias.*
4. *R_{th-jc} is a typical value, obtained with PCB according to JEDEC 1s0p without vias.*
5. *Human body model: HBM test according to the standard ESDA-JS-001-2017.*
6. *Human body model: HBM test according to the standard AEC-Q100-002.*
7. *Charged device model: the CDM test is done according to the standard AEC-Q100-011.*

Table 4. Operating conditions

Symbol	Parameter	Value
V_{CC}	Supply voltage	2.2 V to 5.5 V
V_{icm}	Common mode input voltage range	V_{CC-} – 0.1 V to V_{CC+} + 0.1 V
T_{oper}	Operating free air temperature range	-40 °C to +125 °C

3 Electrical characteristics

Table 5. Electrical characteristics at V_{CC} = 5 V, V_{ICM} = V_{OUT} = V_{CC} / 2, T = 25 °C, R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 22 pF (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			± 200	µV
		-40 °C ≤ T ≤ 125 °C			± 700	
$\Delta V_{io}/\Delta T$	Input offset voltage temperature drift [1]	-40 °C ≤ T ≤ 125 °C			± 5	µV/°C
ΔV_{io} [2]	Input offset voltage long-term drift	T = 25 °C		750		nV/√month
I_{ib} [3]	Input bias current	T = 25 °C		2		pA
		-40 °C ≤ T ≤ 125 °C		75		
I_{io} [3]	Input offset current	T = 25 °C		1		pA
		-40 °C ≤ T ≤ 125 °C		20		
A_{VD}	Open loop gain	V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} - 200 mV, T = 25 °C	110	133		dB
		V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} - 200 mV, -40 °C ≤ T ≤ 125 °C	90	113		
		R_L = 600 Ω, T = 25 °C V_{CC-} + 300 mV ≤ V_{OUT} ≤ V_{CC+} - 300 mV,	105	132		
		R_L = 600 Ω, V_{CC-} + 300 mV ≤ V_{OUT} ≤ V_{CC+} - 300 mV -40 °C ≤ T ≤ 125 °C	85			
CMR1	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} ≤ V_{icm} ≤ V_{CC+} - 2 V, T = 25°C	100	120		dB
		V_{CC-} ≤ V_{icm} ≤ V_{CC+} - 2 V, -40 °C ≤ T ≤ 125 °C	90	120		
CMR2		V_{CC-} ≤ V_{icm} ≤ V_{CC+}, T = 25 °C	80	100		dB
		V_{CC-} ≤ V_{icm} ≤ VCC+, -40 °C ≤ T ≤ 125 °C	76	92		
SVR	Supply-voltage rejection ratio 20.log ($\Delta V_{io}/\Delta_{CC}V_{CC}$)	2.2 V ≤ V_{CC} ≤ 5.5 V, T = 25°C, V_{ICM} = 0 V	90	109		dB
		2.2 V ≤ V_{CC} ≤ 5.5 V, -40 °C ≤ T ≤ 125 °C, V_{ICM} = 0 V	90	108		
V_{OH}	High level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	T = 25°C			20	mV
		-40 °C ≤ T ≤ 125 °C			25	
V_{OL}	Low level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			15	
I_{OUT}	I_{SINK}	OUT connected to V_{CC+}, T = 25 °C	60	70		mA
		OUT connected to V_{CC+},	35			

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{OUT}	I_{SINK}	-40 °C ≤ T ≤ 125 °C				mA
	I_{SOURCE}	OUT connected to V_{CC-}, T = 25°C	50	60		
		OUT connected to V_{CC-}, -40 °C ≤ T ≤ 125 °C	40			
I_{CC}	Supply current (by operational amplifier)	T = 25 °C		5.5	6	mA
		-40 °C ≤ T ≤ 125 °C			6	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 22 pF	35	50		MHz
SR	Slew rate	R_L = 10 kΩ, C_L = 22 pF, A_V = 1 V/V, 10 % to 90 %		30		V/µs
CR	Cross talk	V_{OUT} = 4 V_{pp}, R_L = 10 kΩ, A_V = +101, f = 1 kHz		126		dB
Φm	Phase margin	R_L = 10 kΩ		53		degrees
en	Input voltage noise density	f = 10 Hz		140		nV/√Hz
		f = 100 Hz		43		
		f = 10 kHz		6.5		
en p-p	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		9		$µV_{pp}$
C_{in}	Input capacitance	Differential		6.3		pF
		Common mode		1.6		

1. *See Section 5.2 Input offset voltage drift overtemperature.*
2. *See Section 5.3 Long term input offset voltage drift.*
3. *Guaranteed by characterization.*

Table 6. Electrical characteristics at V_{CC} = 3.3 V, V_{ICM} = V_{OUT} = V_{CC} / 2, T = 25 °C, R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 22 pF (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			± 200	µV
		-40 °C ≤ T ≤ 125 °C			± 700	
$\Delta V_{io}/\Delta T$ [4]	Input offset voltage temperature drift	-40 °C ≤ T ≤ 125 °C			± 5	µV/°C
I_{ib} [5]	Input bias current	T = 25 °C		1.5		pA
		-40 °C ≤ T ≤ 125 °C		60		
I_{io} [5]	Input offset current	T = 25 °C		1		pA
		-40 °C ≤ T ≤ 125 °C		20		
A_{VD}	Open loop gain	V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} - 200 mV, T = 25 °C	105	130		dB
		V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} - 200 mV, -40 °C ≤ T ≤ 125 °C	90	113		
		R_L = 600 Ω, T = 25 °C V_{CC-} + 300 mV ≤ V_{OUT} ≤ V_{CC+} - 300 mV,	100	129		
		R_L = 600 Ω, V_{CC-} + 300 mV ≤ V_{OUT} ≤ V_{CC+} - 300 mV -40 °C ≤ T ≤ 125 °C	85	99		
CMR1	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} ≤ V_{icm} ≤ V_{CC+} - 2 V, T = 25°C	95	116		dB
		V_{CC-} ≤ V_{icm} ≤ V_{CC+} - 2 V, -40 °C ≤ T ≤ 125 °C	85	111		
CMR2		V_{CC-} ≤ V_{icm} ≤ V_{CC+}, T = 25 °C	77	97		dB
		V_{CC-} ≤ V_{icm} ≤ VCC+, -40 °C ≤ T ≤ 125 °C	70	90		
V_{OH}	High level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	T = 25 °C			25	mV
		-40 °C ≤ T ≤ 125 °C			40	
V_{OL}	Low level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			15	mV
		-40 °C ≤ T ≤ 125 °C			30	
I_{OUT}	I_{SINK}	OUT connected to V_{CC+}, T = 25 °C	55	63		mA
		OUT connected to V_{CC+}, -40 °C ≤ T ≤ 125 °C	35			
	I_{SOURCE}	OUT connected to V_{CC-}, T = 25 °C	50	63		
		OUT connected to V_{CC-}, -40 °C ≤ T ≤ 125 °C	35			
I_{CC}	Supply current (by operational amplifier)	T = 25 °C		5.3	5.8	mA
		-40 °C ≤ T ≤ 125 °C			5.8	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 22 pF	35	50		MHz
SR	Slew rate	R_L = 10 kΩ, C_L = 22 pF, A_V = 1 V/V, 10 % to 90 %		30		V/µs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
CR	Cross talk	V_{OUT} = 4 V_{pp}, R_L = 10 kΩ, A_V = +101, f = 1 kHz		126		dB
Φm	Phase margin	R_L = 10 kΩ		53		degrees
en	Input voltage noise density	f = 10 Hz		140		nV/√Hz
		f = 100 Hz		43		
		f = 10 kHz		6.5		
C_{in}	Input capacitance	Differential		6.3		pF
		Common mode		1.6		

1. *See Section 5.2 Input offset voltage drift overtemperature.*
2. *Guaranteed by characterization.*

Table 7. Electrical characteristics at V_{CC} = 2.2 V, V_{ICM} = V_{OUT} = V_{CC} / 2, T = 25 °C, R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 22 pF (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	V_{icm} = 0 V, T = 25 °C		± 50	± 200	µV
		V_{icm} = 0 V, -40 °C ≤ T ≤ 125 °C			± 700	
$\Delta V_{io}/\Delta T$ [6]	Input offset voltage temperature drift	-40 °C ≤ T ≤ 125 °C			± 5	µV/°C
I_{ib} [7]	Input bias current	T = 25 °C		1		pA
		-40 °C ≤ T ≤ 125 °C		45		
I_{io} [7]	Input offset current	T = 25 °C		1		pA
		-40 °C ≤ T ≤ 125 °C		13		
A_{VD}	Open loop gain	V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} - 200 mV, T = 25 °C	95	120		dB
		V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} - 200 mV, -40 °C ≤ T ≤ 125 °C	85	107		
		R_L = 600 Ω, V_{CC-} + 300 mV ≤ V_{OUT} ≤ V_{CC+} - 300 mV, T = 25 °C	90	119		
		R_L = 600 Ω, V_{CC-} + 300 mV ≤ V_{OUT} ≤ V_{CC+} - 300 mV -40 °C ≤ T ≤ 125 °C	80	99		
CMR	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} ≤ V_{icm} ≤ V_{CC+}, T = 25 °C	73	94		dB
		V_{CC-} ≤ V_{icm} ≤ V_{CC+}, -40 °C ≤ T ≤ 125 °C	67	85		
V_{OH}	High level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	T = 25 °C			25	mV
		-40 °C ≤ T ≤ 125 °C			40	
V_{OL}	Low level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			15	mV
		-40 °C ≤ T ≤ 125 °C			30	
I_{OUT}	I_{SINK}	OUT connected to V_{CC+}, T = 25 °C	55	62		mA
		OUT connected to V_{CC+}, -40 °C ≤ T ≤ 125 °C	35			
	I_{SOURCE}	OUT connected to V_{CC-}, T = 25 °C	50	62		
		OUT connected to V_{CC-}, -40 °C ≤ T ≤ 125 °C	35			
I_{CC}	Supply current (by operational amplifier)	V_{ICM} = 0 V, T = 25 °C		5	5.5	mA
		V_{ICM} = 0 V, -40 °C ≤ T ≤ 125 °C			5.5	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ	35	50		MHz
SR	Slew rate	R_L = 10 kΩ, A_V = 1 V/V, 10 % to 90 %		30		V/µs
CR	Cross talk	V_{OUT} = 4 V_{pp}, R_L = 10 kΩ, A_V = +101, f = 1 kHz		126		dB
Φm	Phase margin	R_L = 10 kΩ		69		degrees

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
en	Input voltage noise density	f = 10 Hz		250		nV/√Hz
		f = 100 Hz		94		
		f = 10 kHz		15		
C_{in}	Input capacitance	Differential		6.3		pF
		Common mode		1.6		

1. *See Section 5.2 Input offset voltage drift overtemperature.*
2. *Guaranteed by characterization.*

4 Typical performance characteristics

R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 22 pF, unless otherwise specified.

Figure 3. Supply current vs. supply voltage

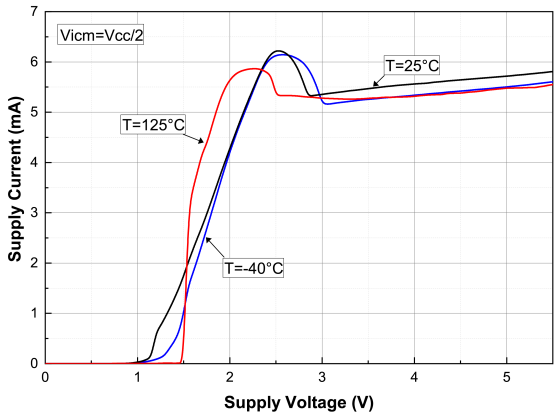


Figure 4. Input offset voltage distribution at V_{CC} = 5 V

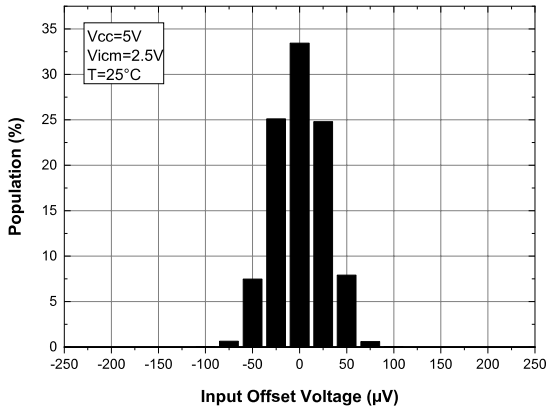


Figure 5. Input offset voltage distribution at V_{CC} = 2.2 V

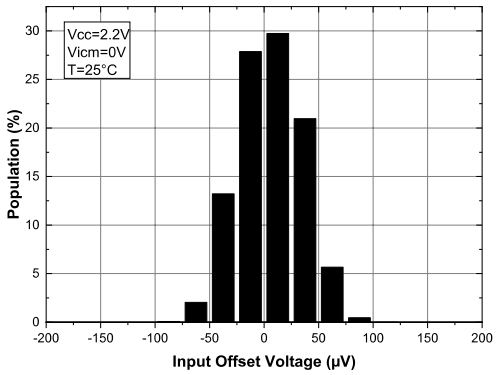


Figure 6. Input offset voltage vs. temperature at V_{CC} = 5 V

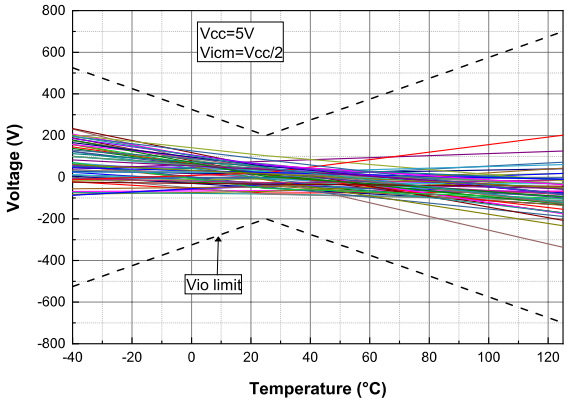


Figure 7. Input offset voltage vs. temperature at V_{CC} = 2.2 V

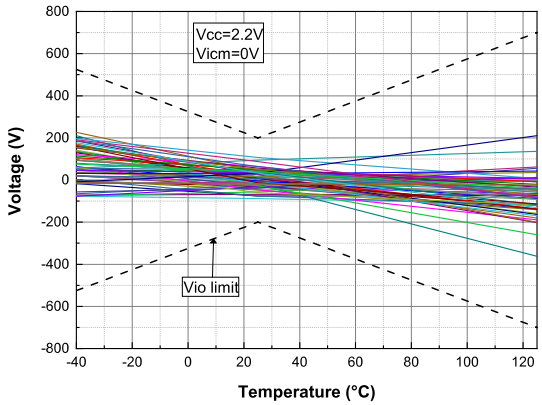


Figure 8. Input offset voltage thermal coefficient distribution at V_{CC} = 5 V

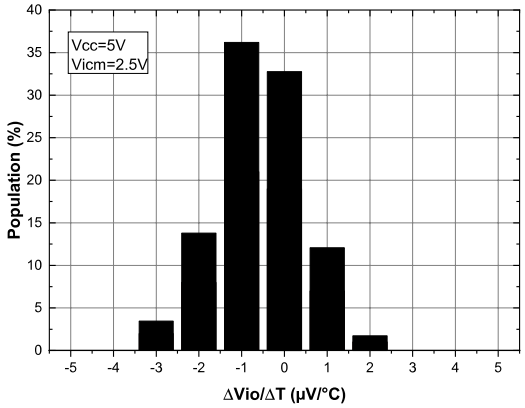


Figure 9. Input offset voltage thermal coefficient at V_{CC} = 2.2 V

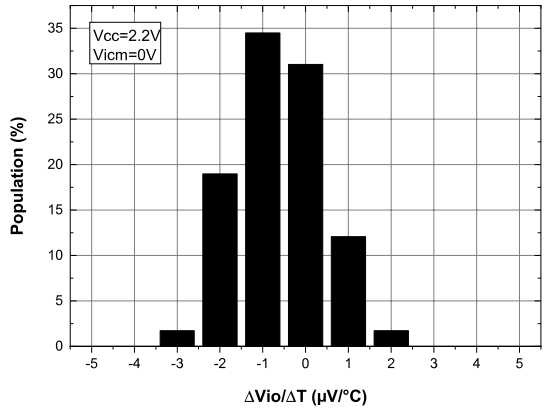


Figure 10. Input offset voltage vs. supply voltage

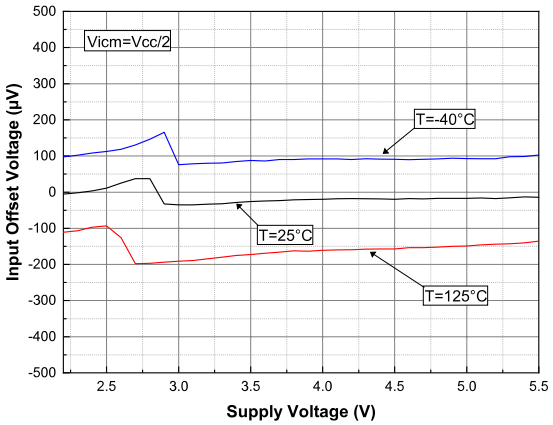


Figure 11. Input offset voltage vs. common mode voltage at V_{CC} = 5 V

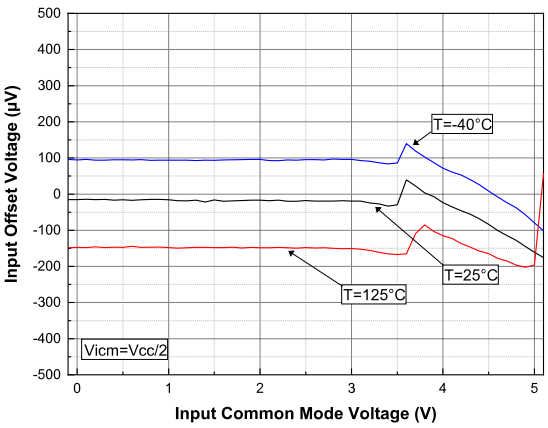


Figure 12. Input offset voltage vs. common mode voltage at V_{CC} = 2.2 V

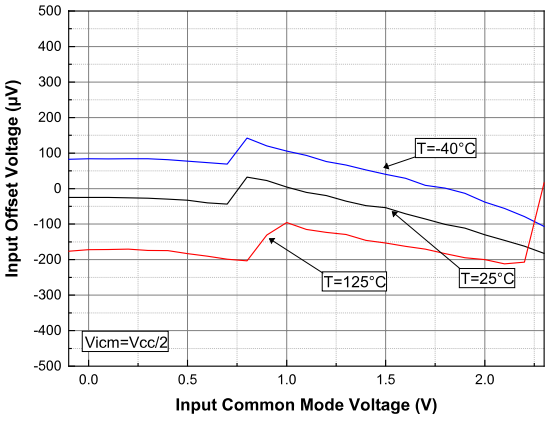


Figure 13. Input bias current vs. temperature at $V_{ICM} = V_{CC} / 2$

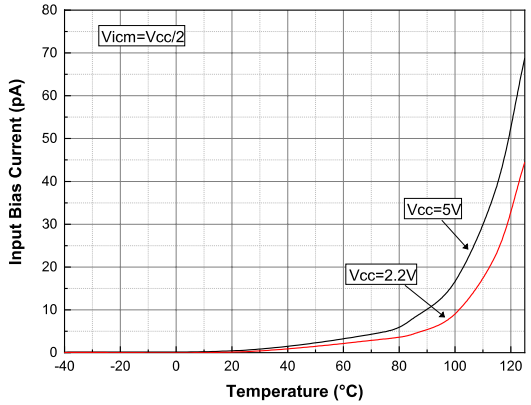


Figure 14. Input bias current vs. common mode voltage at V_{CC} = 5 V

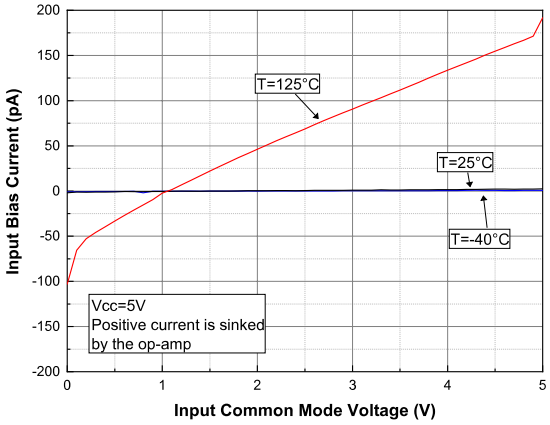


Figure 15. Output current vs. output voltage at V_{CC} = 5 V

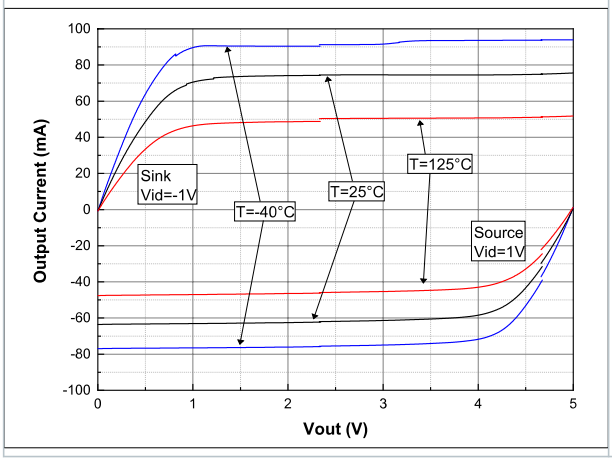


Figure 16. Output current vs. output voltage at V_{CC} = 2.2 V

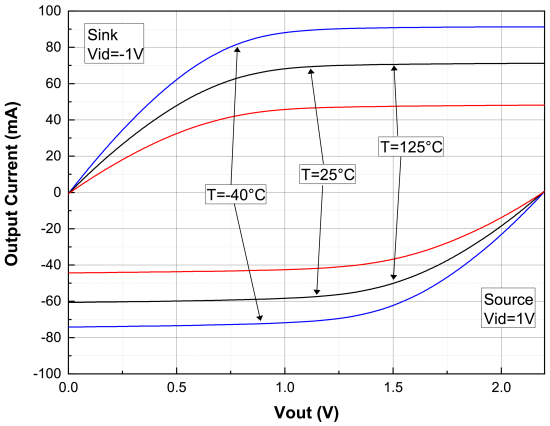


Figure 17. Output saturation voltage (V_{OL}) vs. supply voltage

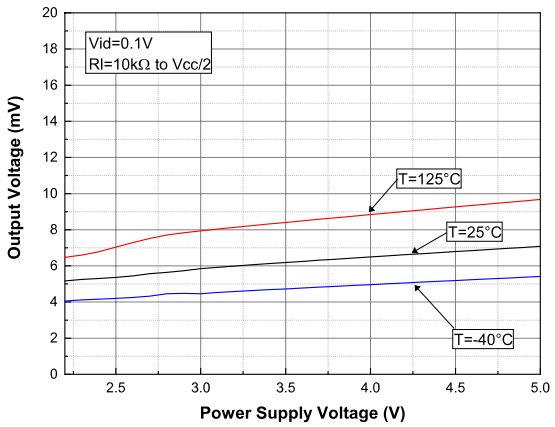


Figure 18. Output saturation voltage (V_{OH}) vs. supply voltage

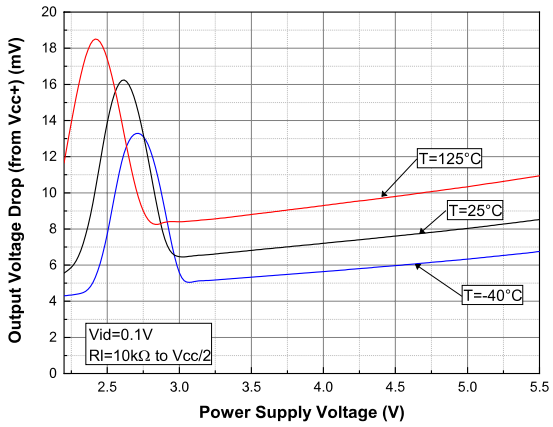


Figure 19. Positive slew rate at V_{CC} = 5 V

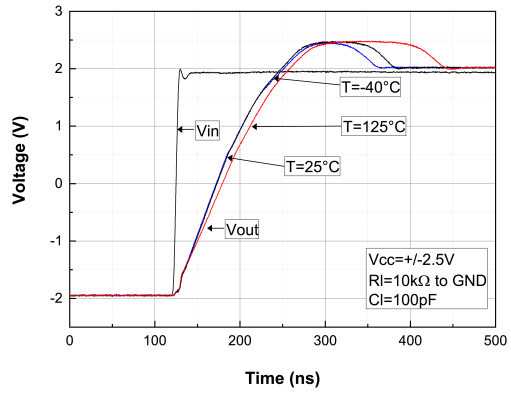


Figure 20. Negative slew rate at VCC = 5 V

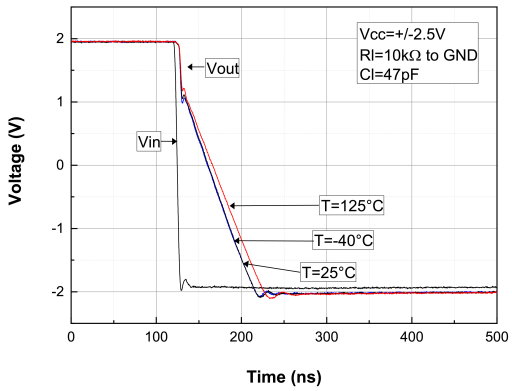


Figure 21. Slew rate vs. V_{CC}

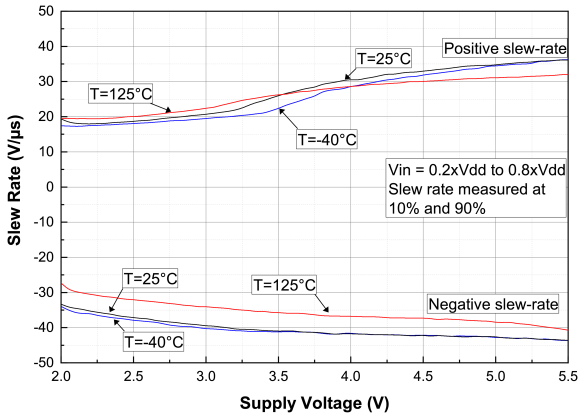


Figure 22. Open loop bode diagram at V_{CC} = 5 V

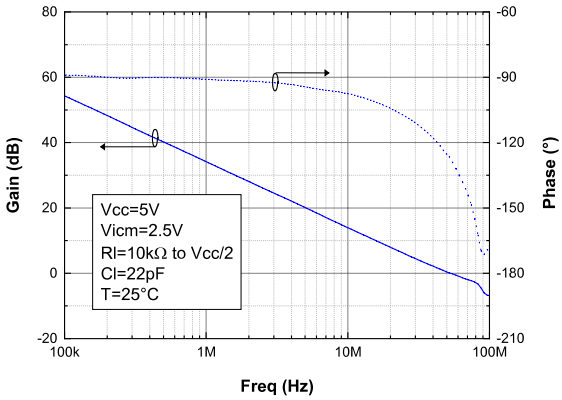


Figure 23. Open loop bode diagram at V_{CC} = 2.2 V

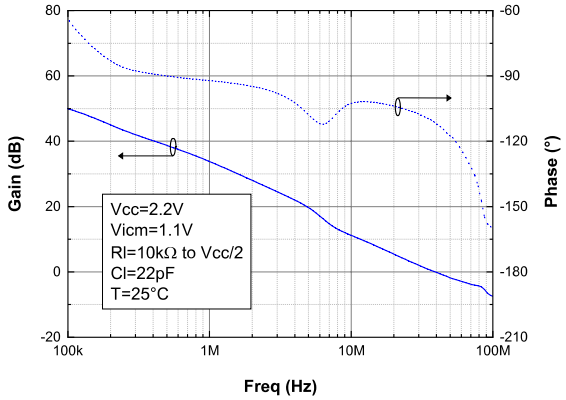


Figure 24. Closed loop bode diagram at V_{CC} = 5 V

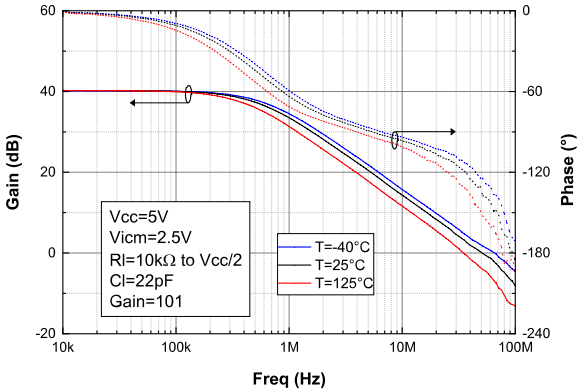


Figure 25. Closed loop bode diagram at V_{CC} = 2.2 V

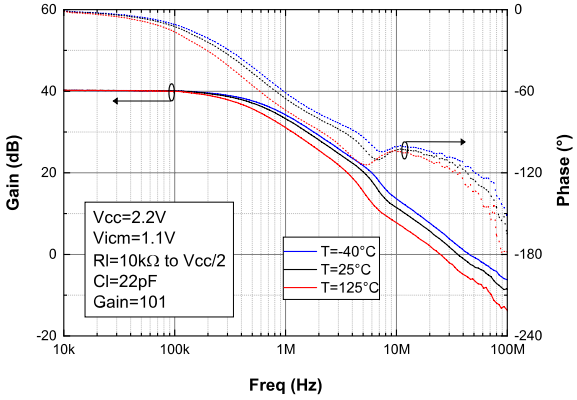


Figure 26. Phase margin vs. common mode voltage and load current at V_{CC} = 5 V

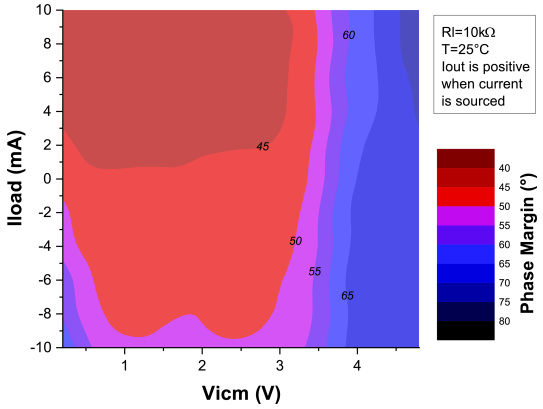


Figure 27. Phase margin vs. capacitive load

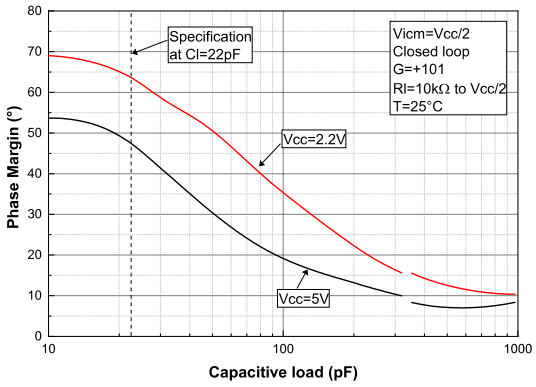


Figure 28. Small step response at V_{CC} = 5 V

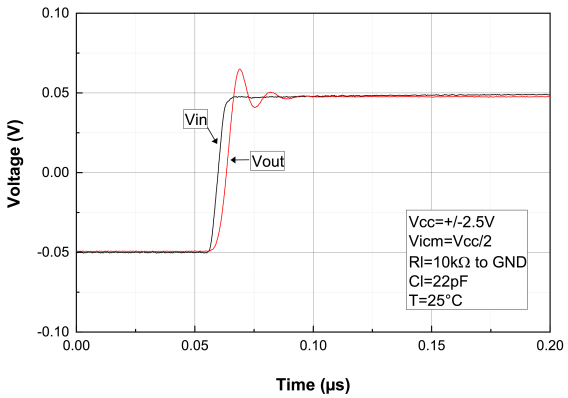


Figure 29. Small step response at V_{CC} = 2.2 V

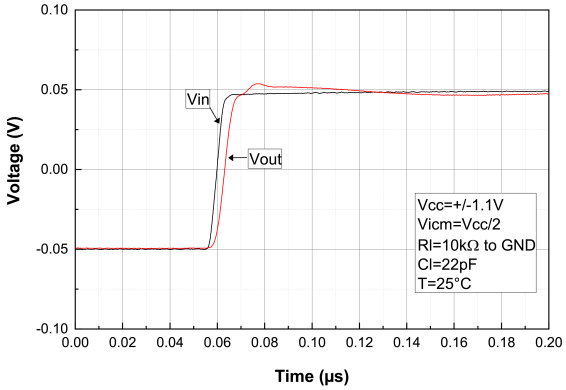


Figure 30. Desaturation from low rail at V_{CC} = 5 V

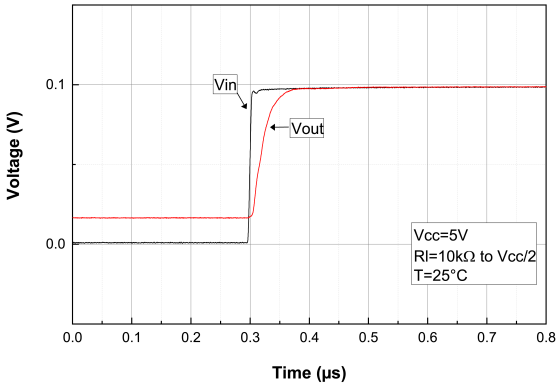


Figure 31. Desaturation from high rail at V_{CC} = 5 V

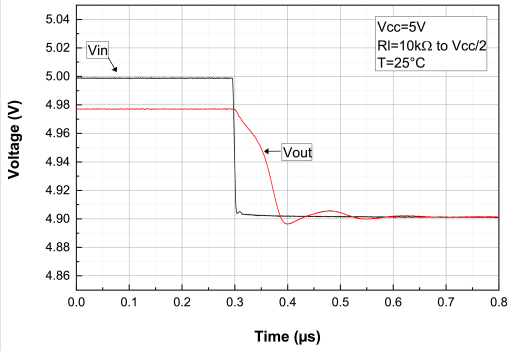


Figure 32. Settling time output high to low at V_{CC} = 5 V

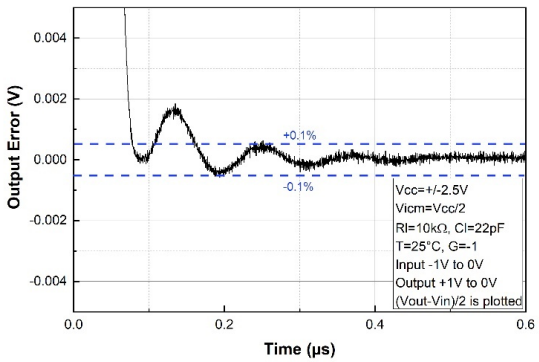


Figure 33. Settling time output low to high at V_{CC} = 5 V

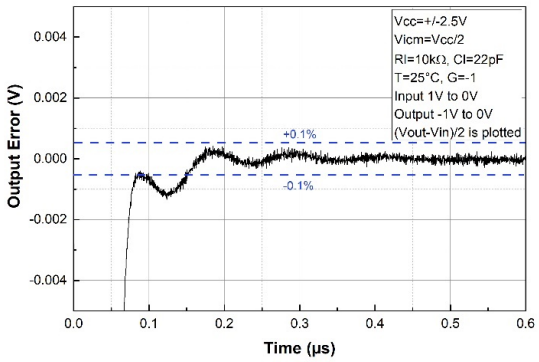


Figure 34. Settling time output high to low at V_{CC} = 2.2 V

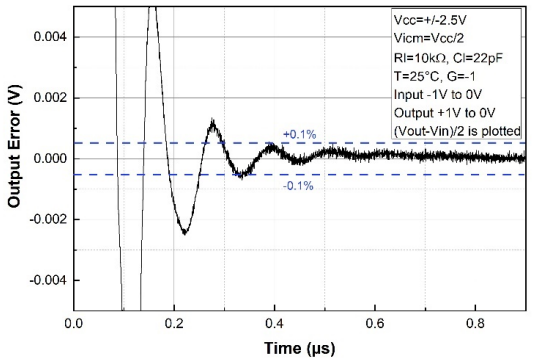


Figure 35. Settling time output low to high at V_{CC} = 2.2 V

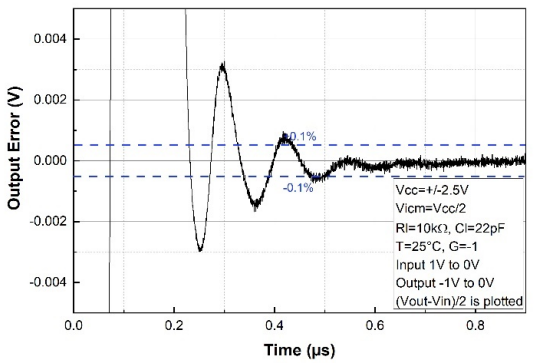


Figure 36. Small step overshoot vs. load capacitance

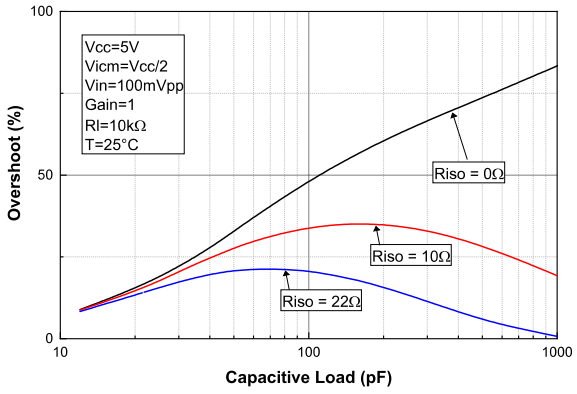


Figure 37. Linearity vs. load resistance at V_{CC} = 5 V

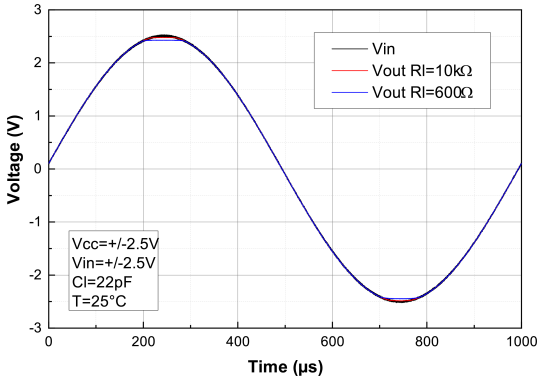


Figure 38. Noise vs. frequency

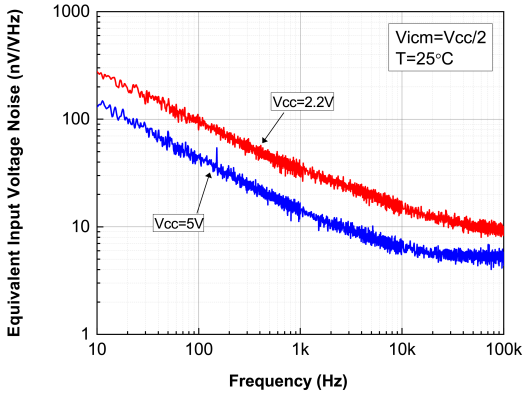


Figure 39. Noise vs. time at V_{CC} = 5 V

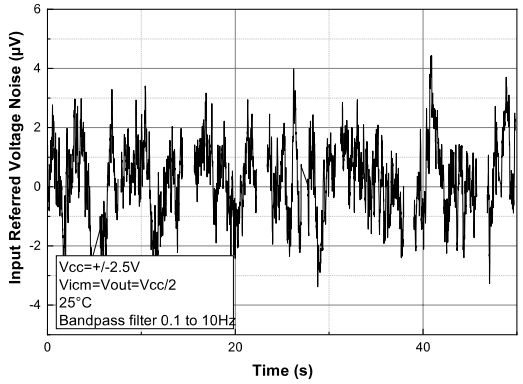


Figure 40. THD+N vs. frequency

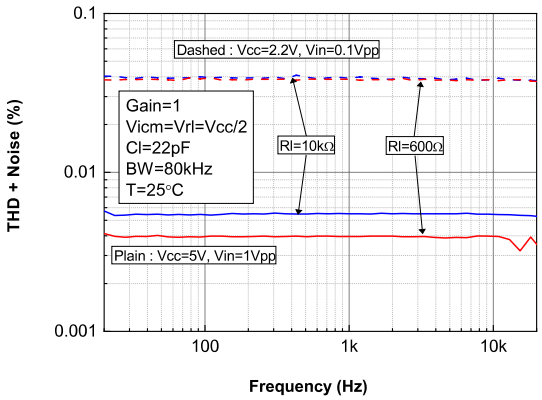


Figure 41. THD+N vs. output voltage

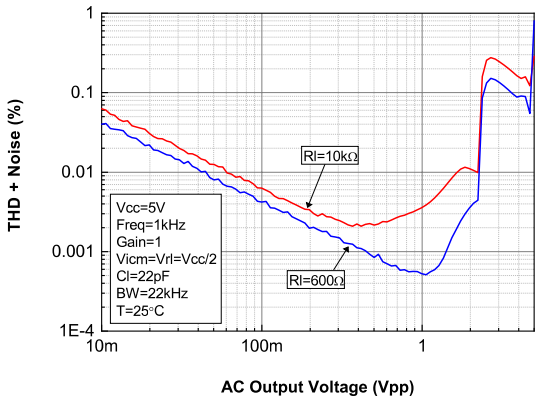


Figure 42. CMRR vs. frequency at V_{CC} = 5 V

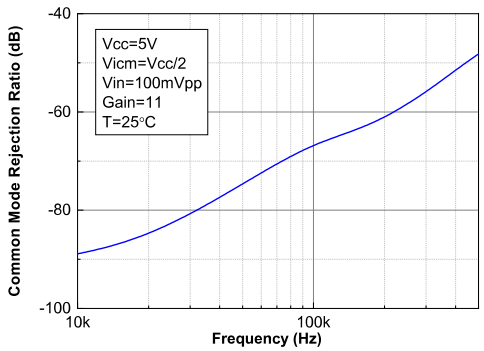


Figure 43. PSRR vs. frequency at V_{CC} = 5 V

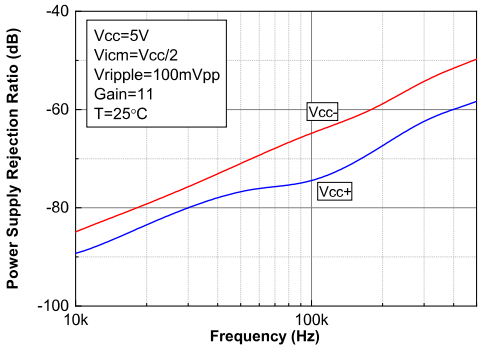
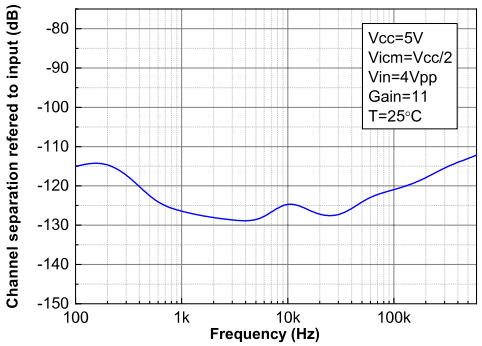


Figure 44. Crosstalk vs. frequency at V_{CC} = 5 V



5 Application information

5.1 Operating voltages

The TSV79x devices can operate from 2.2 to 5.5 V. The parameters are fully specified at 2.2 V, 3.3 V and 5 V power supplies. However, the parameters are very stable over the full V_{CC} range and several characterization curves show the TSV79x device characteristics over the full operating range. Additionally, the main specifications are guaranteed in extended temperature range from - 40 to 125 °C.

The TSV79X devices are rail-to-rail input and output, and feature two input transistor pairs, allowing the op-amp to operate over all the common mode range, from V_{cc-} - 0.1 V, to V_{cc+} + 0.1 V. The input pair transition typically occurs at V_{cc+} - 1.4 V, as seen in figures 11 and 12. The precision and dynamic performances are particularly optimized on the low pair, from V_{cc-} - 0.1 V to V_{cc+} - 2 V, and operating in this V_{icm} range is advised for best performance whenever possible. Also, operating near the pair transition should be avoided when precision is a concern, as CMRR can be lower in these conditions.

5.2 Input offset voltage drift overtemperature

The maximum input voltage drift variation overtemperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset (V_{io}) is a major contributor to the chain accuracy.

The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift overtemperature enables the system designer to anticipate the effect of temperature variations. The maximum input voltage drift overtemperature is computed using Equation 1.

$$\frac{\Delta V_{io}}{\Delta T} = max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right|_{T = -40°C \; and \; T = 125°C} \quad (1)$$

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.3 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)} \quad (2)$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in Equation 3.

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)} \quad (3)$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173 x 10^{-5} eV . K^{-1})

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (Equation 4).

$$A_F = A_{FT} . A_{FV} \quad (4)$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in Equation x to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Months = A_F × 1000 h × 12 months / (24 h × 365.25 days)

To evaluate the op-amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules). The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see Equation 5).

$$V_{CC} = max\left(V_{op}\right) \; with \; V_{icm} = \frac{V_{cc}}{2} \quad (5)$$

The long term drift parameter ΔV_{io} (in µV.month$^{-1/2}$), estimating the reliability performance of the product, is obtained using the ratio of the Vio (input offset voltage value) drift over the square root of the calculated number of months (Equation 6).

$$\Delta V_{io} = \frac{V_{io}drift}{\sqrt{months}} \quad (6)$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

The V_{io} final drift, in µV, to be measured on the device in real operation conditions can be computed from Equation 7.

$$V_{io\ final\ drift}\left(t_{op}, T_{op}, V_{CC}\right) = \Delta V_{io} \cdot \sqrt{t_{op} . e^{\beta . (V_{CC} - V_{CC\ nom})} . e^{\frac{E_a}{k} \cdot \left(\frac{1}{297} - \frac{1}{T_{op}}\right)}} \quad (7)$$

Where:

ΔV_{io} is the long term drift parameter in µV.√month

t_{op} is the operating time seen by the device, in months

T_{op} is the operating temperature

V_{CC} is the power supply during operating time

V_{CC} nom is the nominal V_{CC} at which the ΔV_{io} is computed (5 V for TSV79x)

E_a is the activation energy of the technology (here 0.7 eV).

5.4 Unused channel

When one of the two channels of the TSV792 is not used, it must be properly connected in order to avoid internal oscillations that can negatively impact the signal integrity on the other channel, as well as the current consumption. Two different configurations can be used:

Gain configuration: the channel can be set in gain, the input can be set to any voltage within the V_{icm} operating range.

Comparator configuration: the channel can be set to a comparator configuration (without negative feedback). In this case, positive and negative inputs can be set to any value provided these values are significantly different (100 mV or more, to avoid oscillation between positive and negative state).

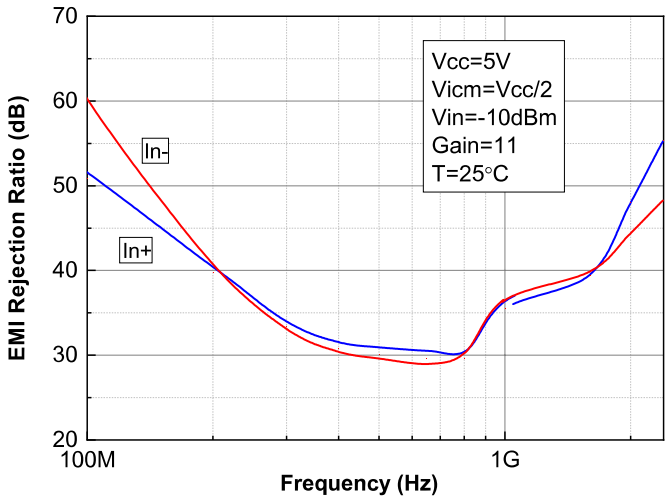
5.5 EMI rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op-amps is a change in the offset voltage as a result of RF signal rectification. EMIRR is defined in Equation 8:

$$EMIRR = 20 . log\left(\frac{V_{in\ pp}}{\Delta V_{io}}\right) \quad (8)$$

The TSV79x has been specially designed to minimize susceptibility to EMIRR and shows a low sensitivity. As seen in Figure 45, EMI rejection ratio has been measured on both inputs and output, from 400 MHz to 2.4 GHz.

Figure 45. EMIRR on IN+ and IN- pins



EMIRR performances might be improved by adding small capacitances (in the pF range) on the inputs, power supply and output pins. These capacitances help to minimize the impedance of these nodes at high frequencies.

5.6 Maximum power dissipation

The usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the TSV79x is 150 °C. The junction temperature can be estimated as follows:

$$T_J = P_D \times \theta_{JA} + T_A \quad (9)$$

T_J is the die junction temperature

P_D is the power dissipated in the package

θ_{JA} is the junction to ambient thermal resistance of the package.

T_A is the ambient temperature.

The power dissipated in the package P_D is the sum of the quiescent power dissipated and the power dissipated by the output stage transistor. It is calculated as follows:

$P_D = (V_{CC} \times I_{CC}) + (V_{CC+} - V_{OUT}) \times ILoad$ when the op-amp is sourcing the current.

$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} - V_{CC-}) \times ILoad$ when the op-amp is sinking the current.

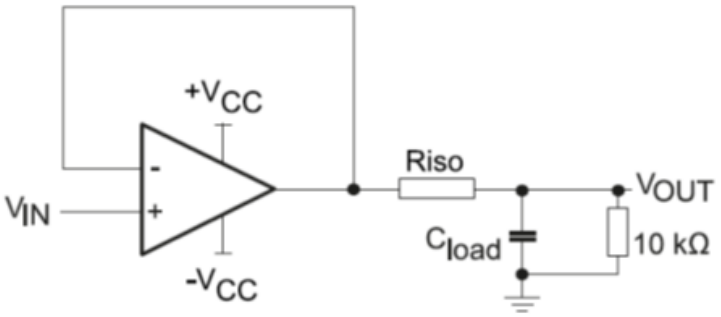
Do not exceed the 150 °C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device.

5.7 Capacitive load and stability

Stability analysis must be performed for large capacitive loads over 22 pF. Increasing the load capacitance to high values produces gain peaking in the frequency response, with overshoot and ringing in the step response.

Generally, unity gain configuration is the worst situation for stability and the ability to drive large capacitive loads. For additional capacitive load drive capability in unity-gain configuration, stability can be improved by inserting a small resistor R_{ISO} (10 Ω to 22 Ω) in series with the output (see Figure 36). This resistor significantly reduces ringing while maintaining DC performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L. R_{ISO} modifies the maximum capacitive load acceptable from a stability point-of-view as described in the figure below:

Figure 46. Test configuration for R_{ISO}



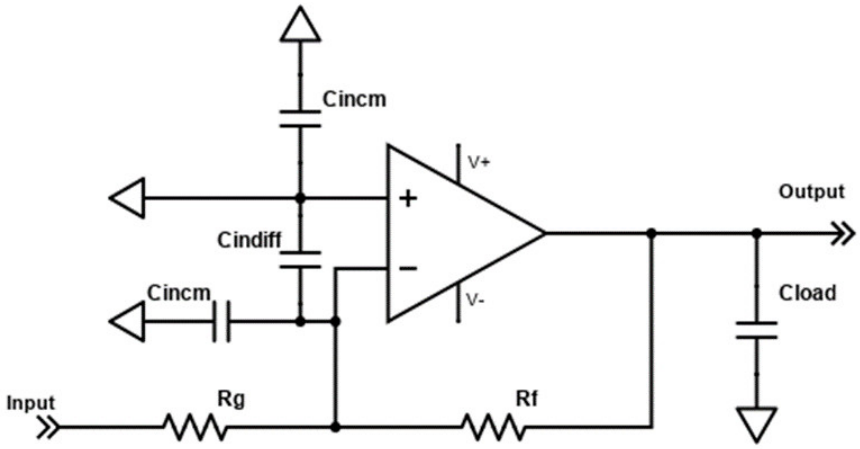
Please note that R_{ISO} = 22 Ω is sufficient to make the TSV79x stable whatever the capacitive load.

5.8 Resistor values for high speed op-amp design

Due to its high gain bandwidth product (GBP), this op-amp is particularly sensitive to parasitic impedances. Board parasitics should be taken into account in any sensitive design. Indeed, excessive parasitics (both capacitive and inductive) in the op-amp frequency range can alter performances and stability. These issues can often be mitigated by lowering the resistive impedances.

More specifically, the RC network created by the schematic resistors (R_f and R_g) and the parasitic capacitances of both the op-amp (as documented in Table 5 to Table 7 and illustrated in Figure 46) and the PCB can generate a pole below or in the same order of magnitude than the closed-loop bandwidth of the circuit. In this case, the feedback circuit is not able to fully play its role at high frequency, and the application can be unstable. This issue can happen when the schematic gain is low (typically < 5), or the device is used in follower mode with a resistor in the feedback. In these cases, it is advised to use a low value feedback resistor (R_f), typically 600 Ω.

Figure 47. Inverting amplifier configuration with parasitic input capacitances



Also, some designs use an input resistor on the positive input, generally of the same value than the input on the negative resistor. This resistor can be useful to balance the input currents on the positive and negative inputs, and reduce the impact of those input currents on precision. However, this is not useful on TSV79x as the input currents are very low. Furthermore, this resistor can also interact with the input capacitances to generate a pole. The frequency of this pole should be kept higher than the closed-loop bandwidth frequency.

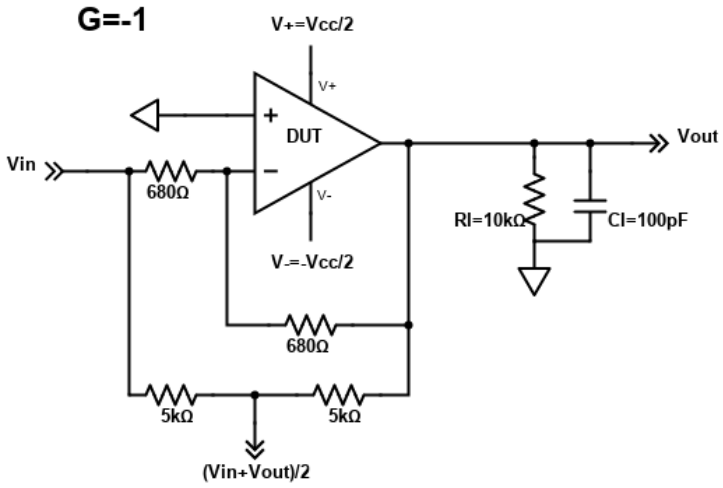
The macromodel provided takes into account the circuit parasitic capacitors. Thus, a transient SPICE simulation (100 mV step) is an easy way to evaluate the stability of the application. However, this cannot replace hardware evaluation of the application circuit.

5.9 Settling time

Settling time in an application can be defined as the amount of time between the input changes, and the output reaching its final value. It is usually defined with a given tolerance, so the output stability is reached when the output stays within the given range around the final value.

In Figure 32 to Figure 35, the settling time is measured in an inverting configuration, using the so-called “false summing node” circuit.

Figure 48. Settling time measurement configuration



This circuit is used with a step input voltage from a positive or negative value, to 0 V. The measurement point being (V_{in} - V_{out}) / 2, and V_{out} being in an ideal circuit equal to -V_{in}, the measurement point gives half of the error on V_{out}, comparatively to V_{in}. This error is compared to the tolerance, 0.1% for this circuit, to deduce the settling time.

This characteristic is particularly useful when driving an ADC. It is related to the slew rate, GBP and stability of the circuit. It also varies with the circuit gain, the circuit load, and the input voltage step value. However, computing the value of the settling time in a given configuration is not straightforward. The macromodel can give a good estimation, but prototyping can be needed for fine circuit optimization.

5.10 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

5.11 Decoupling capacitor

In order to ensure op-amp full functionality, it is mandatory to place a decoupling capacitor of at least 22 nF as close as possible to the op-amp supply pins. A good decoupling helps to reduce electromagnetic interference impact.

5.12 Macro model

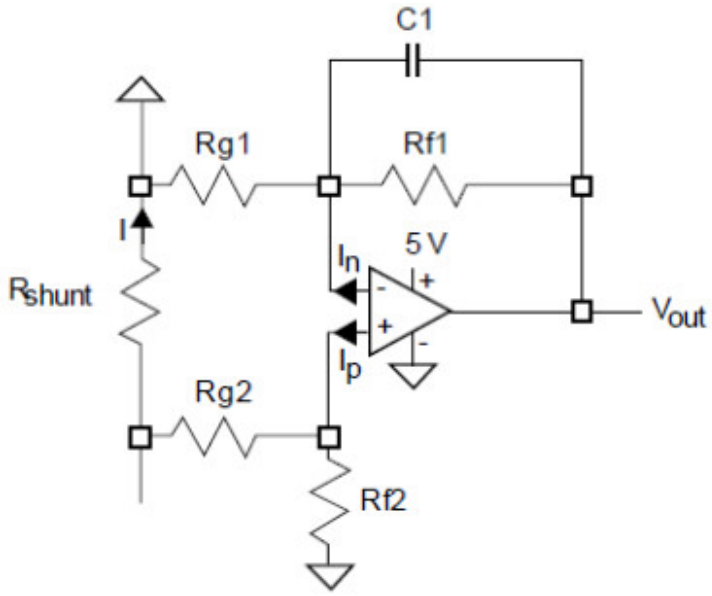
Accurate macro models of the TSV79x device are available on the STMicroelectronics' website at: www.st.com. These models are a trade-off between accuracy and complexity (that is, time simulation) of the TSV79x operational amplifier. They emulate the nominal performance of a typical device at 25 °C within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, but they do not replace onboard measurements.

6 Typical applications

6.1 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful for protecting applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSV79x (see Figure 48).

Figure 49. Low-side current sensing schematic



V_{out} can be expressed as follows:

$$V_{Out} = R_{shunt} \cdot I\left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right) \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) + I_p \cdot \frac{R_{g2} \cdot R_{f2}}{R_{g2} + R_{f2}} \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) - I_n \cdot R_{f1} - V_{io} \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) \quad (10)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, Equation 10 can be simplified as follows:

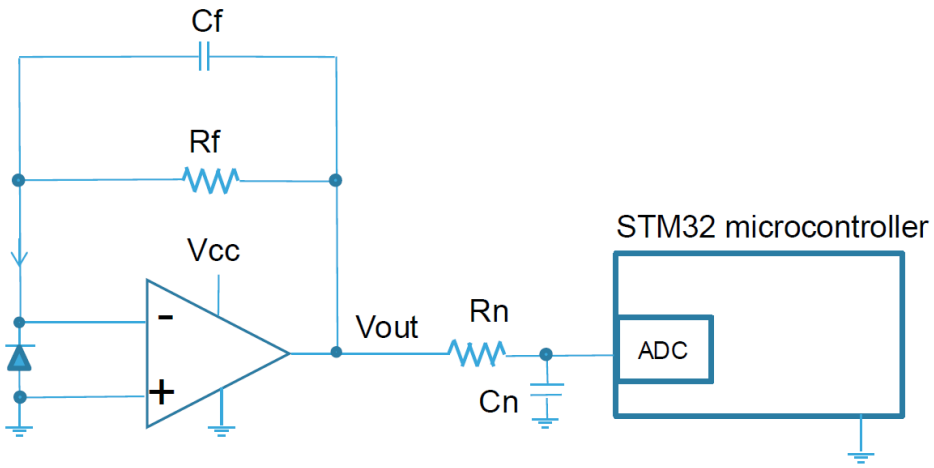
$$V_{Out} = R_{shunt} \cdot I \cdot \frac{R_f}{R_g} - V_{io} \cdot \left(1 + \frac{R_f}{R_g}\right) + R_f \cdot I_{io} \quad (11)$$

The main advantage of using the TSV79x for a low-side current sensing relies on its low Vio, compared to general purpose operational amplifiers. For the same current and targeted accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path, and lower cost. Particular attention must be paid to the matching and precision of R_{g1}, R_{g2}, R_{f1}, and R_{f2}, to maximize the accuracy of the measurement.

6.2 Photodiode transimpedance amplification

The TSV79x, with high bandwidth and slew rate, is well suited for photodiode signal conditioning in a transimpedance amplifier circuit. This application is useful in high performance UV sensors, smoke detectors or particle sensors.

Figure 50. Photodiode transimpedance amplifier circuit



The transimpedance amplifier circuit converts the small photodiode output current in the nA range, into a voltage signal readable by an ADC following Equation 12:

$$V_{Out} = R_f \cdot I_{photodiode} \quad (12)$$

The feedback resistance is usually in the MΩ range, in order to get a large enough voltage output range. However, together with the diode parasitic capacitance, the op-amp input capacitances and the PCB stray capacitance, this feedback network creates a pole that makes the circuit oscillate. Using a small (few pF) capacitor in parallel with the feedback resistor is mandatory to stabilize the circuit. The value of this capacitor can be tuned to optimize the application settling time with a spice simulation using the op-amp macromodel, or by prototyping.

For more details on tuning this circuit, please read the application note AN4451.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SOT23-5 package information

Figure 51. **SOT23-5 package outline**

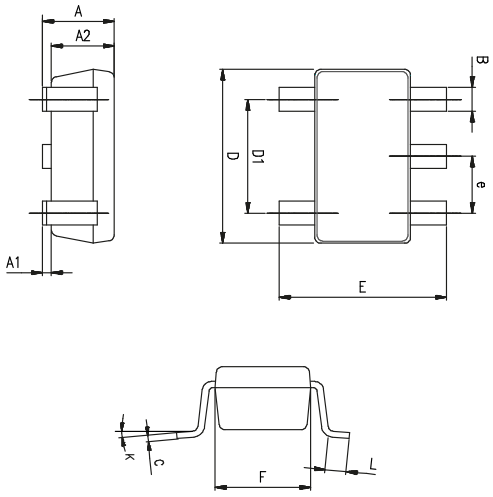


Table 8. **SOT23-5 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.020
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0°		10°	0°		10°

7.2 DFN8 2x2 package information

Figure 52. **DFN8 2x2 package outline**

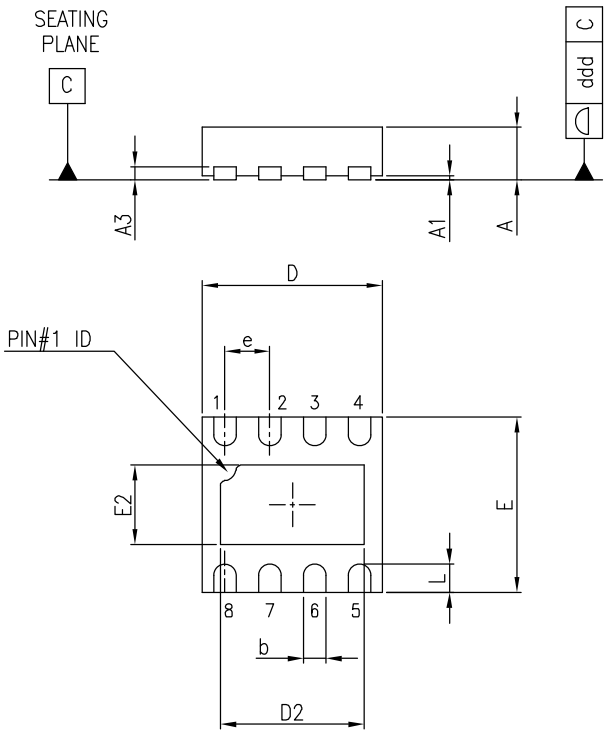
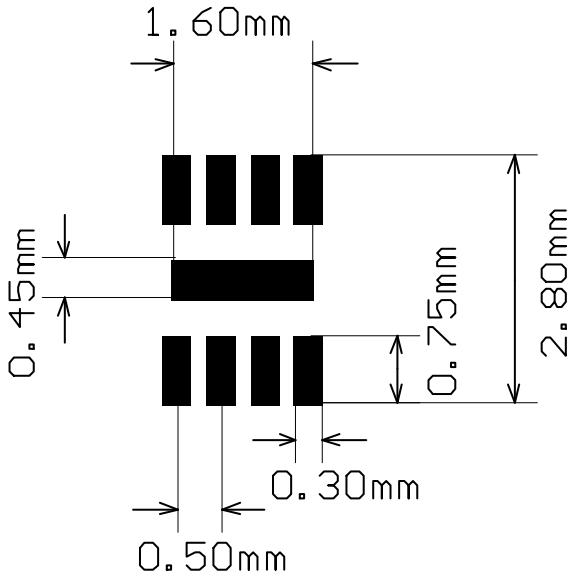


Table 9. **DFN8 2x2 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L	0.225	0.325	0.425	0.009	0.013	0.017
ddd			0.08			0.003

Figure 53. **DFN8 2x2 recommended footprint**



Note: The exposed pad of the DFN8 2x2 can be connected to VCC- or left floating.

7.3 MiniSO8 package information

Figure 54. MiniSO8 package outline

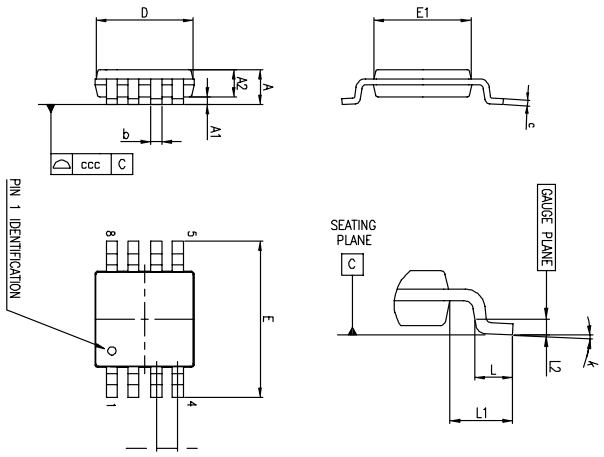


Table 10. MiniSO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

7.4 SO-8 package information

Figure 55. **SO-8 package outline**

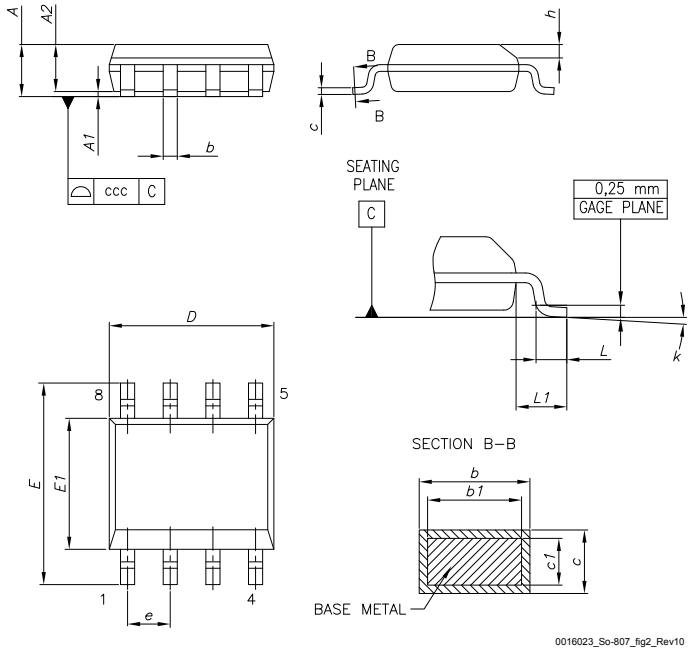


Table 11. **SO-8 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

8 Ordering information

Table 12. Order code

Order code	Channel	Temperature range	Package	Marking
TSV791ILT	1	-40 °C to 125 °C	SOT23-5	K2B
TSV792IQ2T	1		DFN8 2x2	K2B
TSV792IST	2		MiniSO8	K2B
TSV792IDT	2		SO8	TSV792I
TSV791IYLT	2	-40 °C to 125 °C automotive grade (1)	SOT23-5	K227
TSV792IYST	2		MiniSO8	K227
TSV792IYDT	2		SO8	TSV792Y

1. *Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.*

Revision history

Table 13. **Document revision history**

Date	Revision	Changes
11-Nov-2020	1	Initial release.
11-Jan-2021	2	Updated V_{io} and CMR condititions in Table 7.

Contents