Reference Manual

ACPL-P346

Panasonic X-GaN Transistor PGA26E07BA Half Bridge Evaluation Board

Introduction

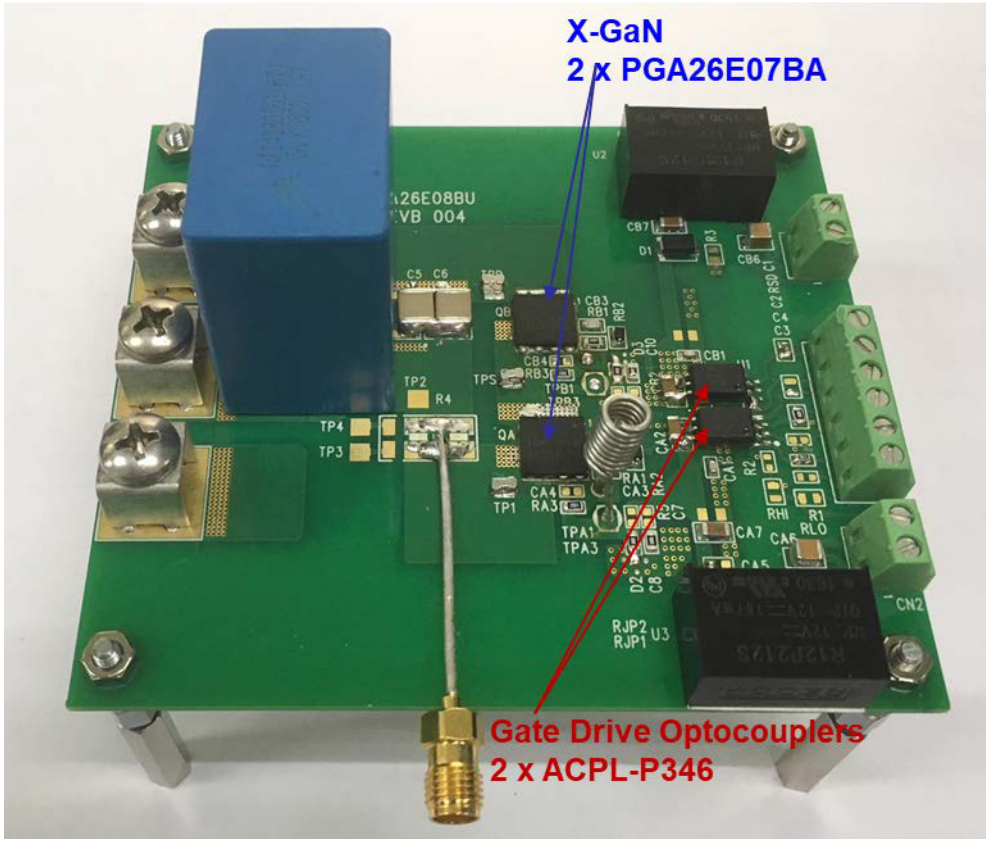
GaN Power Semiconductors

Gallium Nitride (GaN) power semiconductors are rapidly emerging into the commercial market delivering huge benefits over conventional Silicon-based power semiconductors. GaN can improve overall system efficiency with lower on-resistance and the higher switching capability can reduce the overall system size and costs. The technical benefits coupled with lower costs have increased the fast adoption of GaN power semiconductors in applications like industrial power supplies and renewable energy inverters.

Broadcom gate drive optocouplers have been used extensively in driving Silicon-based semiconductors like IGBT. This reference design will discuss how gate drive optocoupler, ACPL-P346 can also be used to drive GaN devices.

A half bridge evaluation board featuring Panasonic 600V 70mΩ X-GaN transistor, PGA26E07BA and 2.5A gate drive optocoupler, ACPL-P346 will be used to perform the slew rate, switching power loss and efficiency test.

Figure 1: Half Bridge Evaluation Board

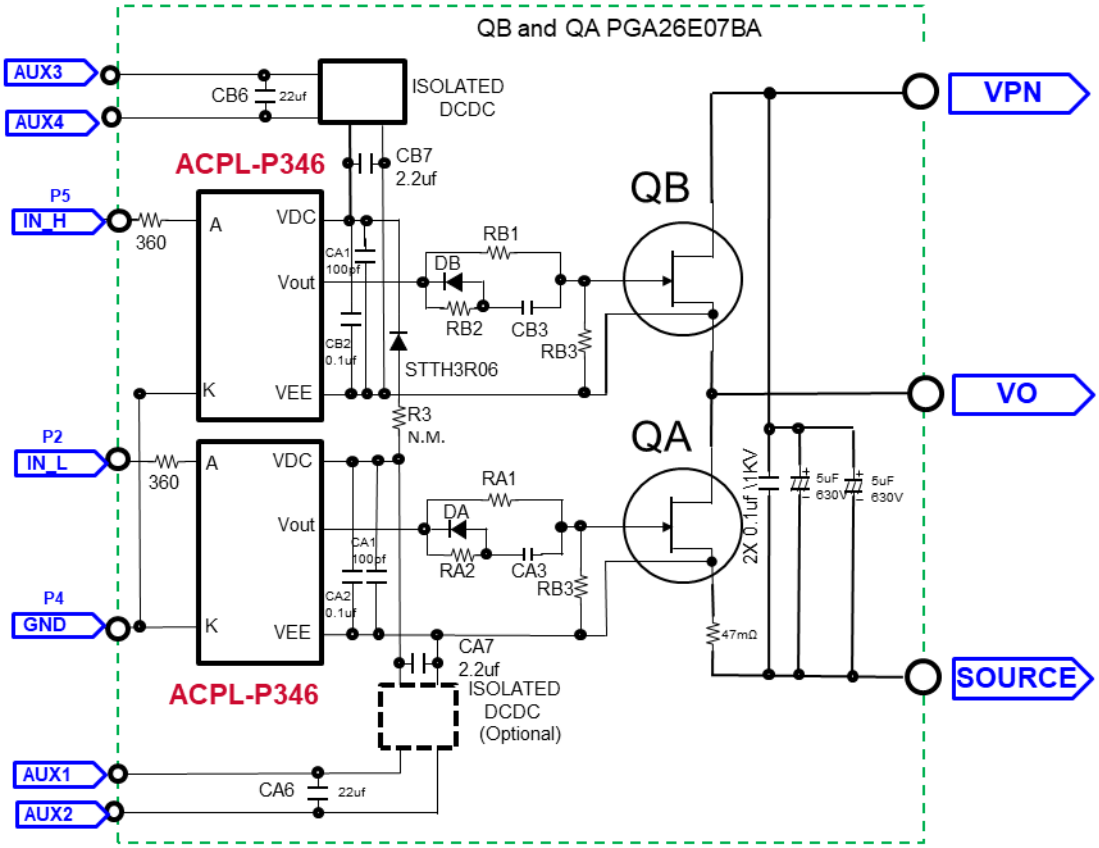


Description of the Half Bridge Evaluation Board

Figure 2 shows the schematic of the half bridge evaluation board. The isolated DCDC converters (RECOM R12P12S) are used to provide 12V (VDC) bias to the gate drivers for the high and low side. Alternatively, bootstrap power supply can be setup using bootstrap resistor R3 and diode D1.

The half bridge evaluation board uses 2 gate drive optocoupler ACPL-P346 to drive the GaN transistor directly. The ACPL-P346 is a basic gate driver optocoupler used to isolate and drive the GaN operating at high DC bus voltage. It has a rail-to-rail output with 2.5A maximum output current to provide fast switching high voltage and driving current to turn-on and off the GaN efficiently and reliably. The ACPL-P346 has a maximum propagation delay less than 110 ns and typical rise and fall times around 8 ns. The very high CMR, common mode rejection of 100 kV/µs (min.) is required to isolate high transient noise during the high frequency operation from causing erroneous outputs. It can provide isolation certified by UL1577 for up to V_{ISO} 3750V_{RMS}/min and IEC 60747-5-5 for working voltage, V_{IORM} up to 891 V_{PEAK}.

Figure 2: Half Bridge Evaulation Board Schematic



RB1,RA1	RB2,RA2	CB3,CA3	RB3,RA3	DB,DA
680Ω	22Ω	1500pF	10KΩ	BAV21WS

The GaN transistors, QB and QA would require about 12.5-mA on-state current to continuously bias the VGS at 3.5V to maintain the transistor in on-state. The value of RB1 and RA1 can be calculated:

Equation 1:

$RB1,RA1 = (VDC – V_{GSF}) / I_{G\_ONSTATE} = (12V – 3.5V) / 12.5mA = 680Ω$

where:

V_{GSF} = 3.5V (refer to the PGA26E07BA data sheet)

$I_{G\_ONSTATE}$ = 12.5 mA (recommended for 70mΩ GaN device)

The initial in-rush charging current to turn on the GaN quickly is provided by ACPL-P346 and the peak current limited by RB2 and RA2. CB3 and CA3 are used to turn on the GaN faster by increase the charging current momentarily. The required $_{IG\_CHARG}E$ can be calculated by the GaN's Qgd and turn on rate.

Equation 2:

$I_{G\_CHARGE} = (VDS / dt) \times (Qgd / VPN) = 70 \times 10^9 \times ((2.6 \times 10^9) / 400) = 0.455A$

where:

(VDS / dt) = (70V /1 ns) (turn on rate based on design)

Qgd = 2.6 nC (refer to the PGA26E07BA data sheet)

VPN = 400V (based on design)

Equation 3:

RB2, RA2 = ((VDC – Vpl)/ (I_{G_CHARGE} – (VDC / RA1))) = ((12 – 1.7) / (0.455 – (12 / 680))) = 23.3Ω (use 22Ω)

where:

Vpl = 1.7V (refer to the PGA26E07BA data sheet)

The "speed-up" capacitors, CA3 and CB3, can be calculated based on two conditions.

Equation 4:

(VDC – V_{GSF}) × CA3 > Qg

Equation 5:

(VDC – V_{GSF}) × CA3 < Qgmax

Equation 6:

(Qg / (VDC – V_{GSF})) < CA3 < (Qgmax / (VDC – V_{GSF})

(5 nC / (12V – 3.5V)) < CA3 < (32 nC / (12V – 3.5V))

588 nF < CA3 < 3765 pF

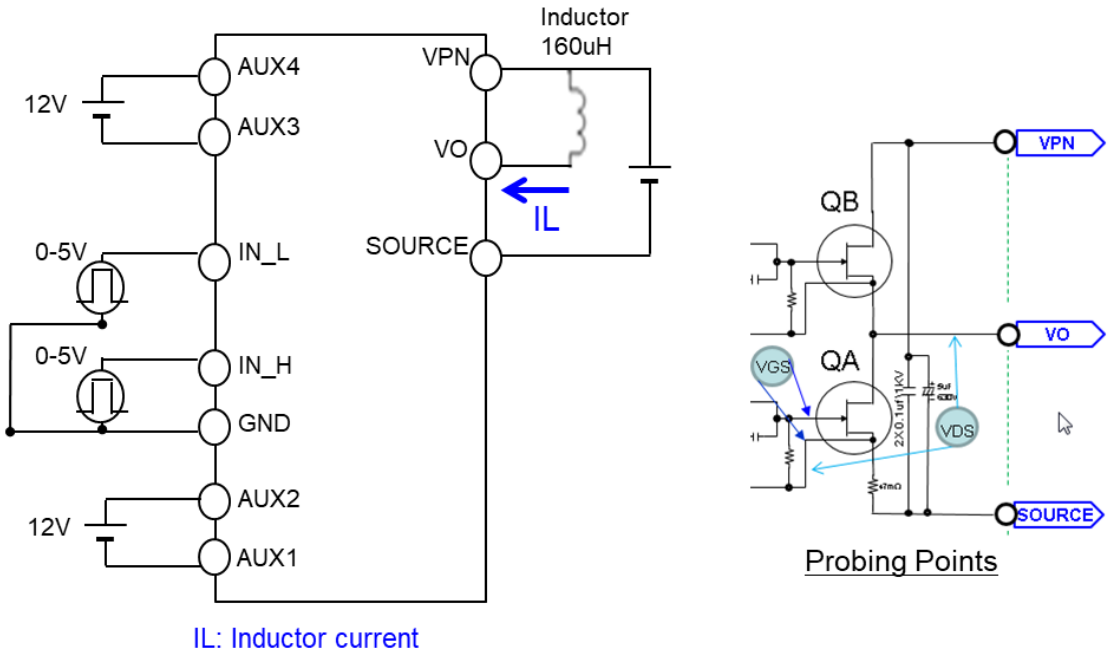
1500pF is chosen for CA3,CB3.

Test Circuits and Results

Slew Rate Test Circuit

A 160-µH inductor is connected between VPN and VO to form the boost configuration also known as low side test. The low side GaN transistor QA is active in boost mode. 400V Bus voltage is applied to VPN.

Figure 3: Low Side Slew Rate Test Circuit



5V double pulse signals, with a dead time of 100 ns are applied to IN_L and IN_H as shown in Figure 4.

Figure 4: Input Double Pulse Test Pattern and Timings

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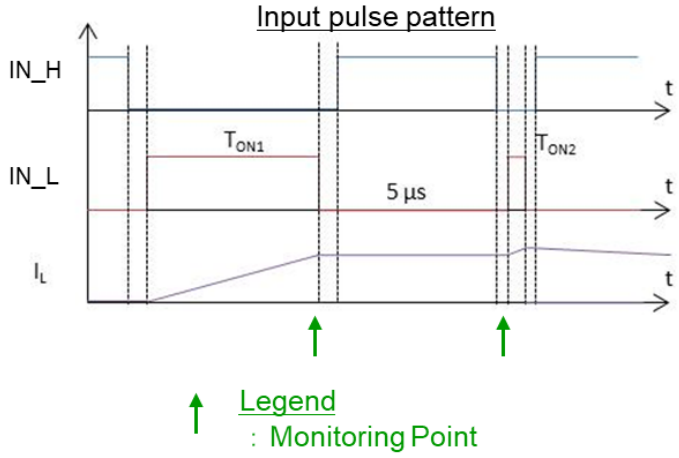


IDS	T_{ON1}	T_{ON2}
2A	1us	0.8us
6A	2.8us	0.8us
10A	4.8us	0.8us
14A	6.7us	0.8us
18A	8.4us	0.8us
22A	10.1us	0.8us
26A	11.7us	0.8us

NOTE: The double pulses are generated in burst mode. If the pulse is generated continuously, the transistor will be damaged by the high current flows.

Slew Rate Test Results

The slew rates (dVDS/dt) are measured at the second monitoring point for the GaN transistor turns on and off characteristics. The highest slew rate of 116kV/us was measured when the GaN transistor turned off at an inductor current of IL = 26A.

Figure 5: Turn Off Slew Rate versus Inductor Current

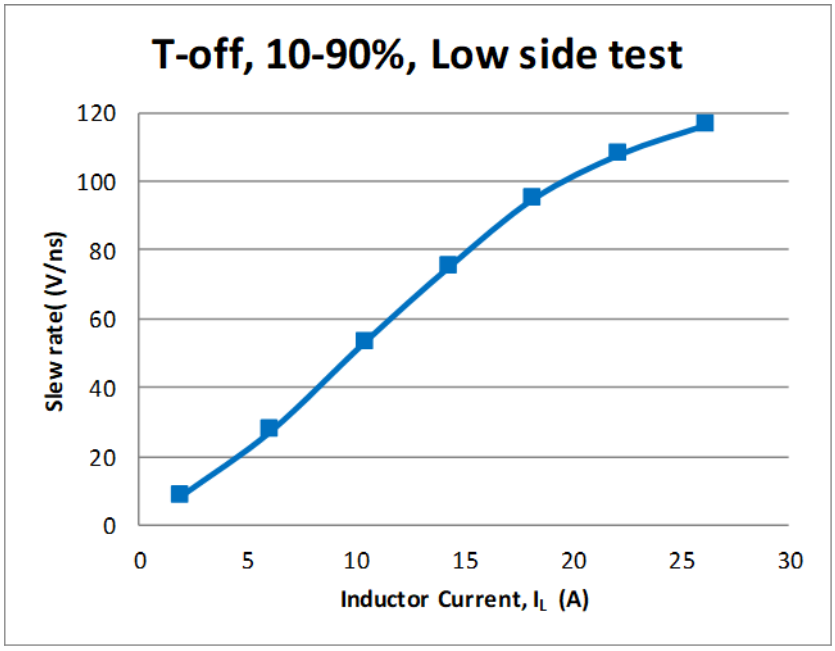


Figure 6: Turn On Slew Rate versus Inductor Current

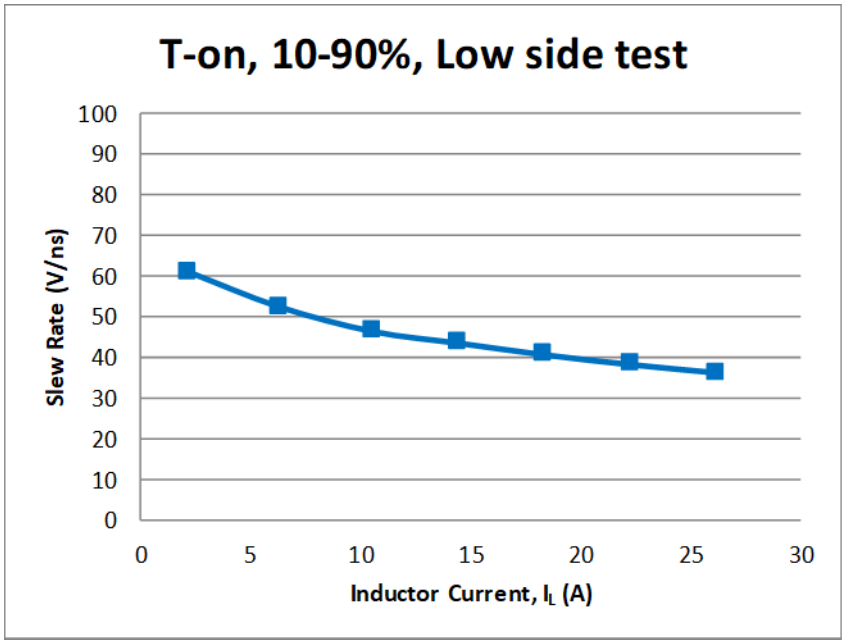
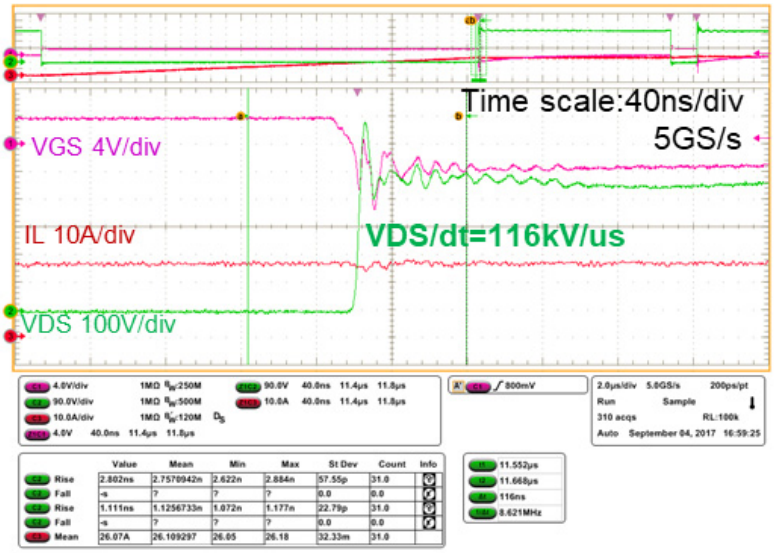


Figure 7: Turn Off Slew Rate at IL = 26A



Power Loss Test Circuit

The power loss test uses the same boost configuration or the low side test. The VDS of QA is measured and IDS is measured by the voltage across the 47mΩ sense resistor (see Figure 1) using a BNC cable to a 50Ω terminated channel of the oscilloscope. IDS is then derived by dividing the voltage measured over 47mΩ.

Figure 8: Low Side Power Loss Test Circuit

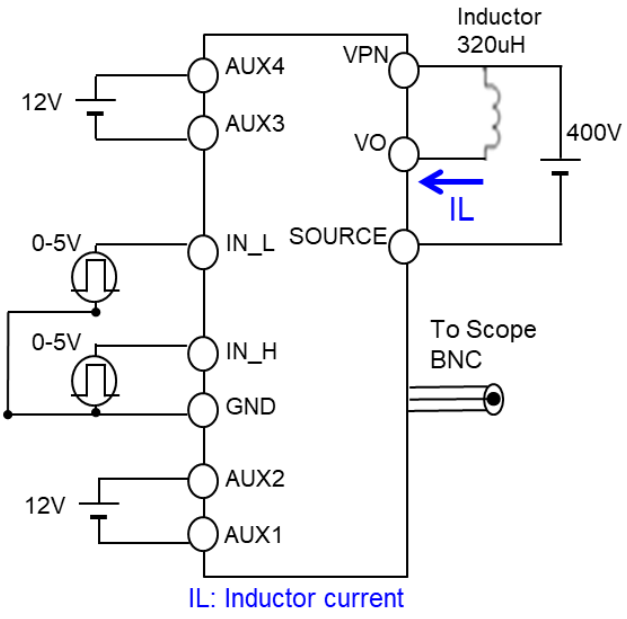
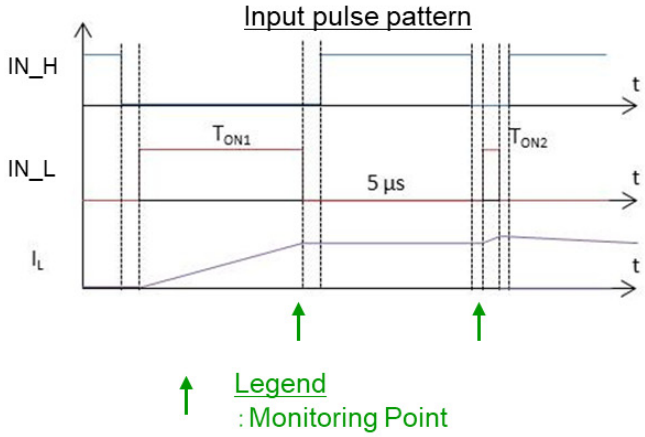


Figure 9: Input Double Pulse Test Pattern, Timings and Power Measurements



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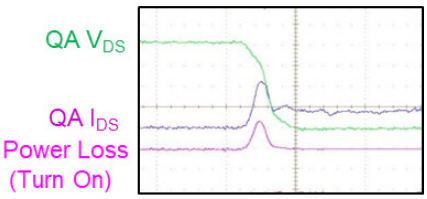
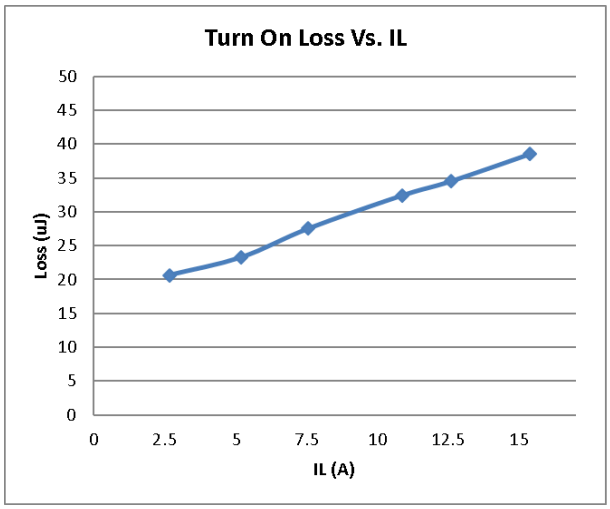


The same double pulse signals and timing of the slew rate test is used for the power loss measurement. The measurement is done at the monitoring points when the GaN transistor turns on or off at the target current level. The math function on oscilloscope is used to find the multiplication of VDS and IDS. The measure function on the oscilloscope is then used to find power loss which is the area under the curve.

Power Loss Test Results

The turn off power loss is kept at 10 µJ regardless of inductor load current. The turn of power loss is low at less than 40 µJ at a load current of 15A.

Figure 10: Turn On/Off Power Loss versus Inductor Current



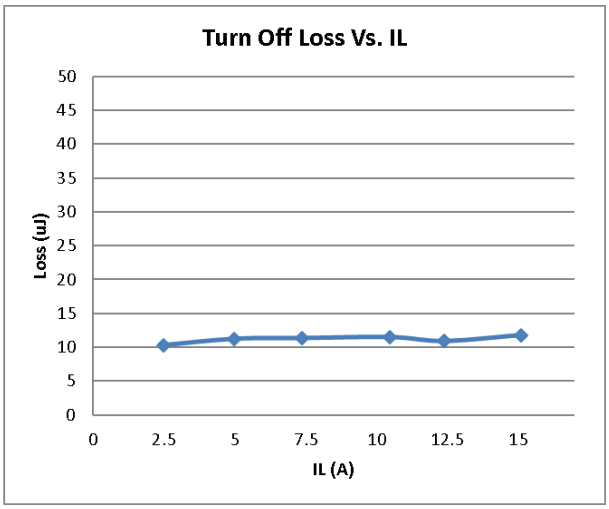


Figure 11: Turn On Power Loss at IL = 5A and 15A

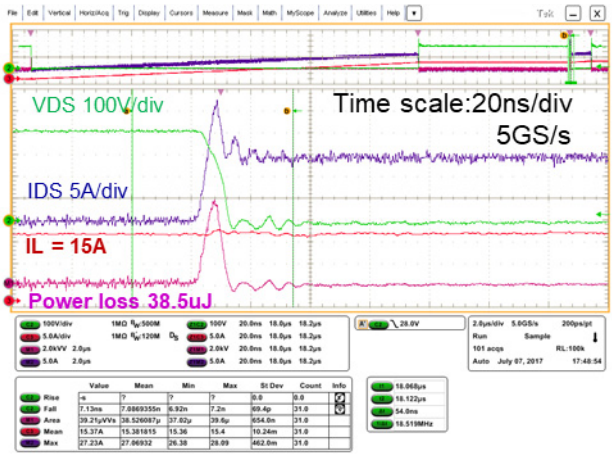
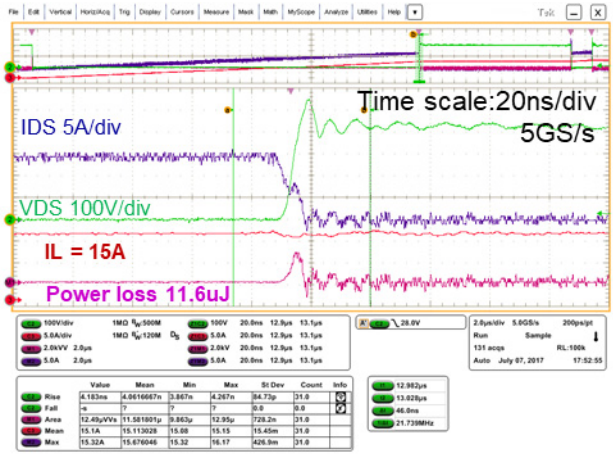


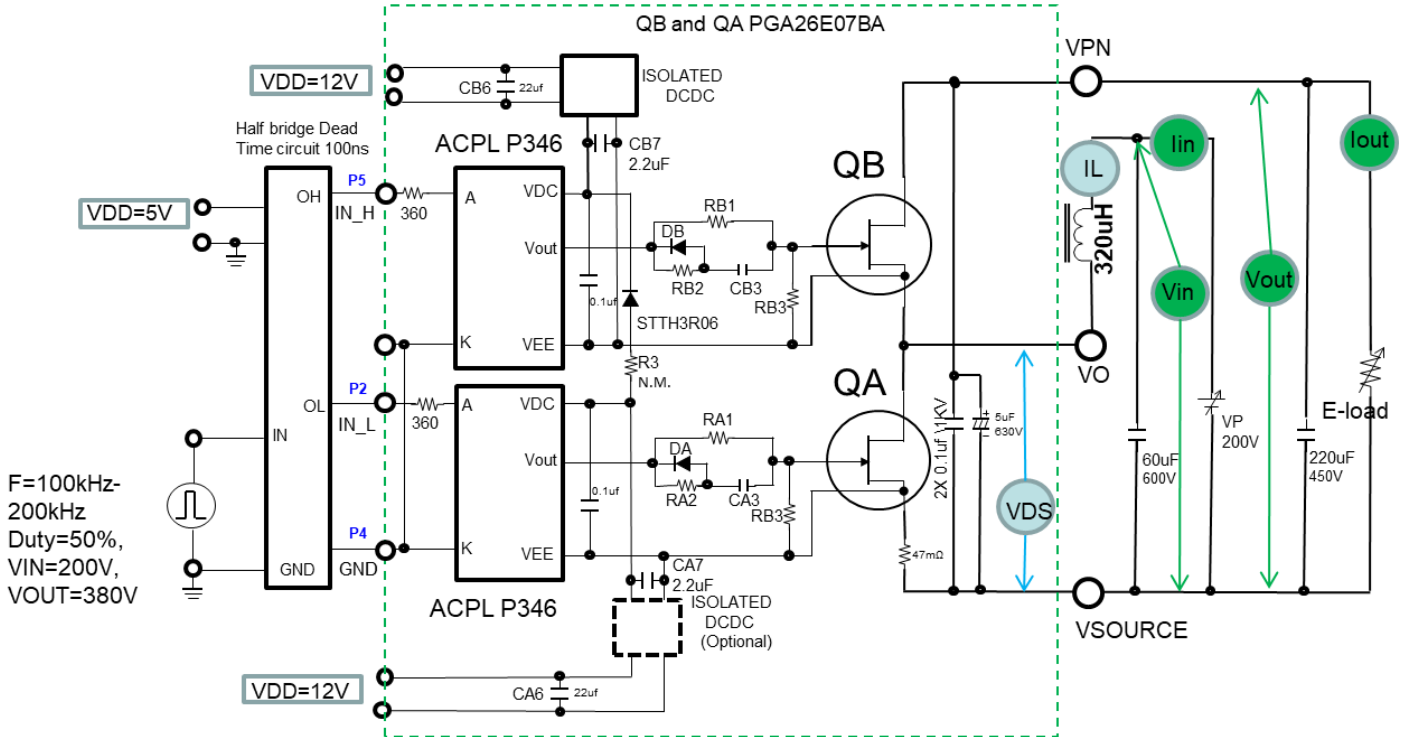
Figure 12: Turn Off Power Loss at IL = 5A and 15A



Efficiency Test Circuit

To test the efficiency of GaN transistor in hard switching operation, the board is connected as DC-DC converter in synchronous boost configuration. The converter is operated at high frequency 100 kHz and 200 kHz.

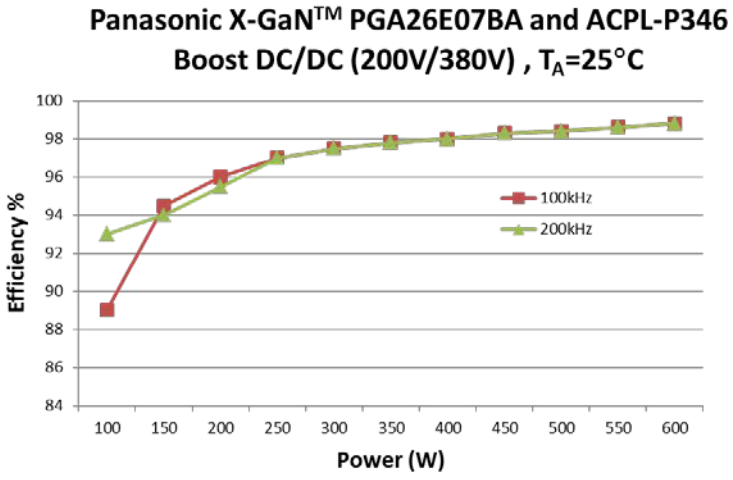
Figure 13: Efficiency Test Circuit



Efficiency Test Results

A very high DC-DC conversion efficiency of 99% is achieved using Panasonic X-GaN transistor, PGA26E07BA, and gate drive optocoupler, ACPL-P346 at both 100 kHz and 200 kHz.

Figure 14: Efficiency Test Results



Acknowledgement

Broadcom thanks the GaN Field Application Team, Panasonic Semiconductor Solutions Singapore for the technical support on the development of the half bridge evaluation board.