User's Manual

RZ/V2M

User's Manual: Hardware

VisionAI ASSP
RZ Family RZ/V Series

arm

Renesas Electronics
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Technology Name
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SD
H.264
H.265

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Objective and Target Users

This manual was written to explain the hardware functions and electrical characteristics of this LSI to the target users, i.e. those who will be using this LSI chip in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logic circuits, and microcomputers.

This manual is structured to cover the following items: an overview of the product, descriptions of the CPU, system control functions, and peripheral functions, electrical characteristics of the device, and usage notes.

When designing an application system that includes this LSI chip, take all points to note into account. Points to note are given in their contexts, at the final parts of each of the sections, and in the section giving usage notes.

The list of revisions is a summary of major points of revision or addition for this and earlier versions. It does not cover all revised items. For details on the revised points, see the actual locations in the manual.

This manual is a simplified version. Please contact a Renesas Electronics sales representative for the detailed version of the manual.

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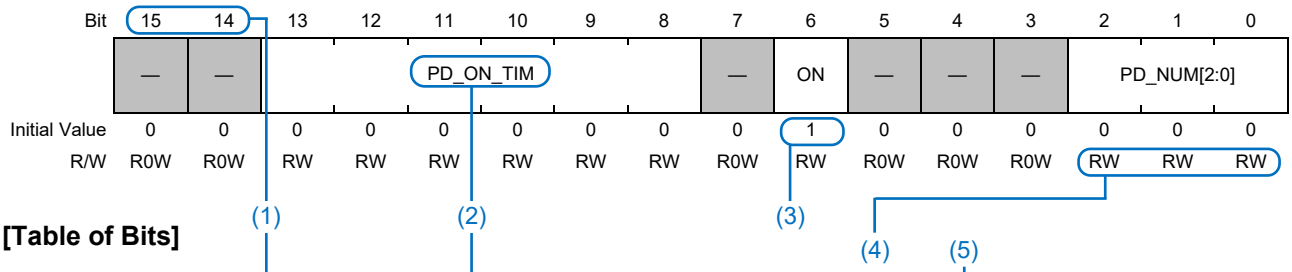
2. Description of Registers

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings. The standard format and notation for use with bit charts and tables are described below.

[Bit Chart]



[Table of Bits]

Bit Position	Bit Name	Description
15, 14	—	Reserved These bits are read as 0b. The write value should be always 0b.
13 to 8	PD_ON_TIM	Set the power-on time for power domain unit.
7	—	Reserved These bits are read as 0b. The write value should be always 0b.
6	ON	Writing to this register starts the process of turning on/off the power domain. 0b: Power off 1b: Power on
5 to 3	—	Reserved These bits are read as 0b. The write value should be always 0b.
2 to 0	PD_NUM[2:0]	Specify the power domain to be turned on/off. 000b: The power on/off process does not start. 001b: The processing target is PD_1. 010b: The processing target is PD_2. 100b: The processing target is PD_3. Settings other than the above are prohibited.

Note: The bit names and statements in the above figure and table are examples and have nothing to do with the main contents of this manual.

(1) Bit

Indicates the bit number or numbers.
In the case of a 64-bit register, the bits are arranged in order from 63 to 0.
In the case of a 32-bit register, the bits are arranged in order from 31 to 0.

(2) Bit name

Indicates the name of the bit or bit field.
When the number of bits must be clearly indicated for a bit field, appropriate notation is included (e.g., PD_NUM[2:0]).
Certain kinds of bits, such as those of timer counters, are not assigned bit names. In such cases, the entry under “Bit Name” is blank (e.g., PD_ON_TIM).
A reserved bit is indicated by “—”. Make sure to use the specified values when writing to such bits or fields. Otherwise, the correct operation of this LSI chip is not guaranteed.

(3) Initial value

Indicates the initial value of each bit.

0:	The initial value is 0.
1:	The initial value is 1.
x/—:	The initial value is undefined.

(4) R/W

For each bit and bit field, this entry indicates whether the bit or field is readable, writable, or both, and whether writing to and reading from the bit or field are impossible.

The notation is as follows:

RW:	The bit or field is readable and writable.
RW0:	The bit or field is readable and writable with 0. Writing 1 is invalid.
RW1:	The bit or field is readable and writable with 1. Writing 0 is invalid.
R0W:	The bit or field is readable as 0 and writable.
R1W:	The bit or field is readable as 1 and writable.
R:	The bit or field is readable. Writing is invalid.
R0W0:	The bit or field is readable as 0 and writable with 1. Writing 1 is invalid.
R0W1:	The bit or field is readable as 0 and writable with 1. Writing 0 is invalid.
R1W0:	The bit or field is readable as 1 and writable as 0. Writing 1 is invalid.
R1W1:	The bit or field is readable as and writable as 1. Writing 0 is invalid.
RCW0:	The bit or field is readable and writable with 0. Reading the bit initializes it. Writing 1 is invalid.
RCW1:	The bit or field is readable and writable with 1. Reading the bit initializes it. Writing 0 is invalid.

(5) Description

Describes the function of the bit or field and specifies the values for writing.

Note: Access to reserved addresses is prohibited.
Do not access these addresses. In case of access, correct operation of this LSI chip is not guaranteed.

3. Notation of Numbers and Symbols

Number notation: Binary numbers are given as XXXXb (or B'XXXX, b'XXXX), hexadecimal numbers are given as XXXXh (or H'XXXX, h'XXXX, 0xXXXX), and decimal numbers are given as XXXX.

Table of Contents

Section 1 Overview

This section describes the overview of this LSI.

1.1 Features

This LSI chip includes the AI dedicated accelerator (DRP-AI) and 4K-compatible image signal processor (ISP). This processor is vision-AI ASSP for real-time human and object recognition.

The AI dedicated hardware IP, DRP-AI, configured with the dynamic reconfigurable processor (DRP) and AI-MAC, combines both a high-speed AI inference and low power consumption and realizes 1TOPS/W class power performance. In addition, the image signal processor (ISP) is highly robust, producing a stable image independent of the environment, allowing for a high AI recognition accuracy. With these features, this LSI realizes low power consumption, which is a critical factor for embedded devices, making heat dissipation measures easier. The result is that it is ideal for vision AI applications in a wide range of embedded markets, including surveillance security, retail, office automation (OA), industrial automation, and robotics. In addition, this LSI also features abundant high-speed communication interfaces such as USB 3.1, PCI Express®, Gigabit Ethernet, and many CPU peripheral functions, so it can also be used in a variety of applications.

■ CPU and DDR Memory Interfaces

- Cortex®-A53 Dual (996 MHz maximum)
- 32-bit LPDDR4-3200

■ Vision and AI

- AI accelerator: DRP-AI (1.0 TOPS/W class)
- Image signal processor (ISP) with multi-stream capability
- Camera interface: 2× MIPI CSI
- Face and Human Detection Engine

■ Video and Graphics, Display

- H.265/H.264 Multi Codec
  Encoding: H.265 up to 2160p30, H.264 up to 1080p120
  Decoding: H.265 up to 2160p30, H.264 up to 1080p120
- 2D Graphics Engine: 200 MPixels/s
- Display: MIPI-DSI (4-lane), HDMI 1.4a

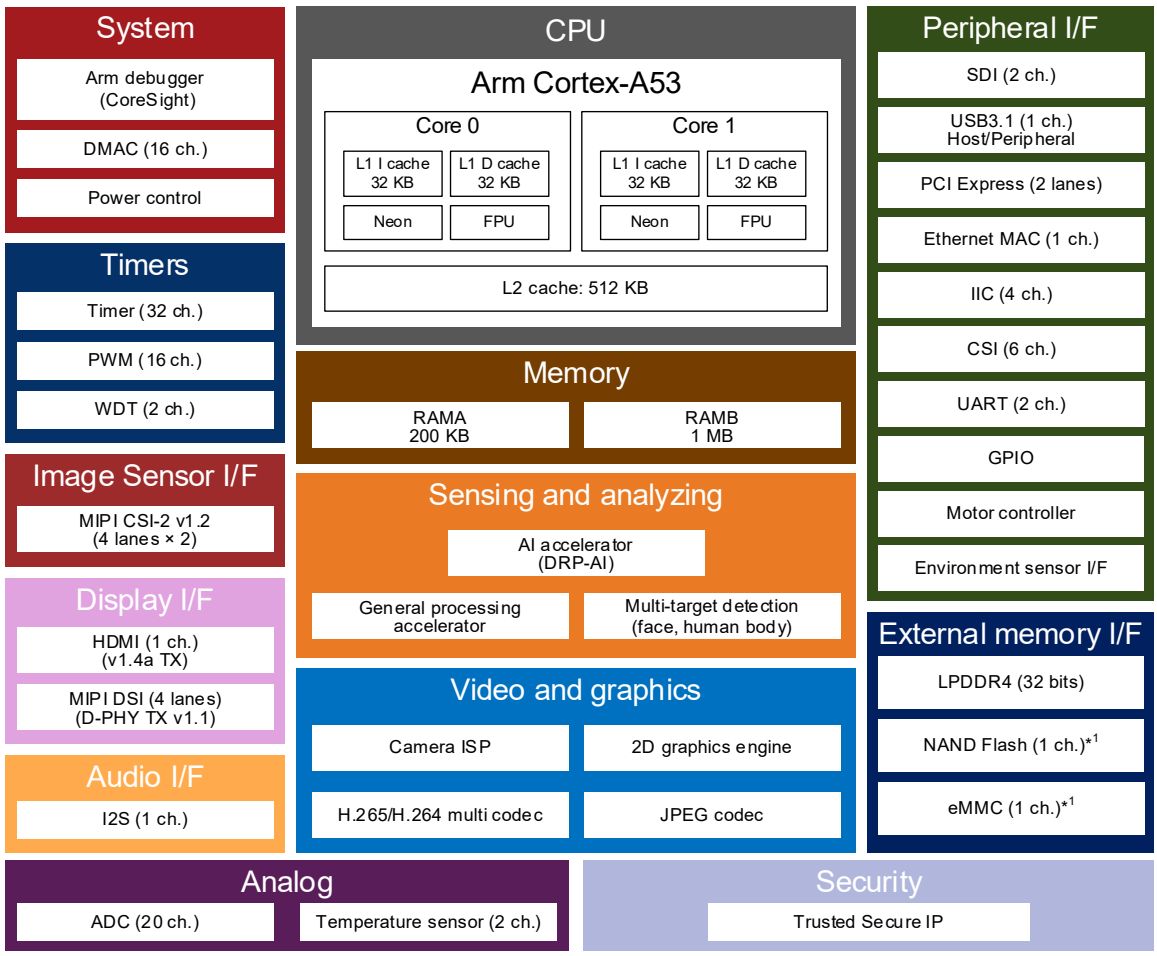
■ High Speed Interfaces

- 1× Gigabit Ethernet
- 1× USB3.1 Gen1 Host/Peripheral
- 1× PCIe® Gen 2 (2 lanes)
- 2× SDIO 3.0
- 1× NAND Flash Interface ONFI1.0
- 1× eMMC™ 4.5.1

■ Hardware Security Engine provided

■ Package

- FCBGA (15×15 mm, 0.5-mm pitch)



Note 1. The use of NAND flash memory and eMMC is exclusive of each other.

Figure 1.1-1 Diagram of Functional Overview

1.2 Product Lineup

The group currently consists of the following products.

Table 1.2-1 Product Lineup

Product Part Number	Part Number for Ordering	Package	Packing
R9A09G011GBG	R9A09G011GBG#ACC	PRBG0841KA-A	Individual tray
	R9A09G011GBG#BCC	PRBG0841KA-A	Full carton

1.3 Functions

Table 1.3-1 Overview of Functions (1/4)

Item	Function
CPU	• Arm® Cortex-A53 dual core (CA53): 996 MHz – L1 cache: 32 KB (for instructions) + 32 KB (for data) for each core – L2 cache: 512 KB – FPU, Neon™ extension – ECC supported • Debugger interface (JTAG/SWD) – CoreSight™ debugging components incorporated – ETF (64-Kbyte trace RAM), ETR, and STM incorporated – External trace output (16-bit width)
Memory	• RAM A (RAMA): 200 KB (with ECC) • RAM B (RAMB): 1 MB • ROM: 128 KB
Timers	• Watchdog timer (WDT): 2 channels (CA53 core 0, CA53 core 1) • Compare-match timer: 32 channels • Pulse-width modulation timer (PWM): 16 channels • Real-time clock (RTC)
DMA controller	DMA controller (16 channels)
CMOS image sensor interfaces	• MIPI CSI-2 Ver.1.2/ D-PHY Ver.1.2 4 lanes × 2, 2.5 Gbps per lane: Supports 2 sensor inputs • Formats: – RAW: 8/10/12 bits – YUV422: 8 bits*1 • Supports WDR extraction • Virtual channel
Audio interfaces	I2S interface for the external audio codec: 1 channel Audio sampling rate: 32 kHz, 44.1 kHz, 48 kHz
Sensing and analyzing	• AI accelerator (DRP-AI) • Multi-target detection (face, human body) • General-purpose accelerator

Note 1. The input of data in this format limits the available functions of the LSI chip. For details, contact a Renesas Electronics sales representative.

Table 1.3-1 Overview of Functions (2/4)

Item	Function
Video & graphics	• Camera ISP – 3840 × 2160 p × 30 fps / 1920 × 1080 p × 30 fps × 2 / 640 × 480 p × 800 fps supported – WDR processing – 3D noise reduction – Fisheye correction • H.265/H.264 multi codec – Supported functions H.265 encoding and H.265 decoding, or H.264 encoding and H.264 decoding – Support encoding/decoding standard H.265/HEVC main profile at level 5 H.264/AVC constrained baseline/main/high profile at level 5.1 – I-/P-slice supported for H.264/H.265 encoding and decoding – H.265 encoding and decoding performance 3840 × 2160 p × 30 fps encoding, 3840 × 2160 p × 30 fps decoding 1920 × 1080 p × 60 fps encoding, 1920 × 1080 p × 60 fps decoding 640 × 480 p × 800 fps encoding – H.264 encoding and decoding performance 1920 × 1080 p × 60 fps encoding, 1920 × 1080 p × 60 fps decoding 640 × 480 p × 800 fps encoding • JPEG codec – JPEG extended DCT-based process/baseline-process compliant – Color format: YUV – Image data rate: Max. 16 samples/clock cycle • 2D graphics engine – 200 Mpixels per second fill rate (200-MHz clock, single pipeline) – 4096 × 4096 texture size
External memory interfaces	• LPDDR4 interface – 3200 Mbps – 32-bit data width – Up to 4 GB supported • NAND flash interface – ONFI1.0 compliant – Supports KIOXIA's BENAND™ – EDO not supported – 8-bit data width – 128 MB and 256 MB are supported – 4-/8-bit ECC • eMMC interface conforming to eMMC version 4.51 – Supports HS200 (high-speed DDR and HS400 are not supported) – 1/4/8-bit data bus

Table 1.3-1 Overview of Functions (3/4)

Item	Function
Peripheral interfaces	• SD host interface (SDI): 2 channels (SD specification version 3.01 compliant) – SD memory / I/O card interface (1-bit/4-bit SD bus) – SD memory card access for SD, SDHC, and SDXC – Supports default, high-speed, UHS-I/SDR12, SDR25, SDR50, and SDR104 transfer modes (DDR50, not supported) – Supports card detection and write protection • USB interface: 1 channel – USB3.1 Gen1 standard compliant – Dual-role device function supported (static switching of the host controller function and the peripheral controller function) – Supports super-speed (5 Gbps), high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transfer (low-speed is only supported for the host controller) • PCI Express interface: Gen2 (5GT/s), 2 lanes – PCI Express base specification revision 4.0 compliant – Supports root complex/endpoint • Ethernet MAC interface: 1 channel – Supports transfer at 1000 Mbps, and 100 Mbps in full-duplex mode – Supports IEEE802.3 PHY GMII, MII compliant interface • IIC bus interface: 4 channels • Clocked serial interface: 6 channels • UART: 2 channels • Motor control Stepping motor control, serial interface dedicated to the motor driver • Environment sensor interface Acquisition of external device data and transfer to the DRAM by an internal timer • GPIO
Display interfaces	• Display control – Display control via HDMI and MIPI DSI interfaces – Resolution conversion, picture compositing, and image frame adjustment • HDMI Tx interface v1.4a: 1 channel – Supports DTV with 1280 × 720 p, 1920 × 1080 p resolution – YUV digital video output format, supported – HDCP, CEC, and HEAC, not supported • LCD control interface (MIPI DSI Ver.1.3.1/ D-PHY Ver.1.1), 4 lanes – Supports the video formats: 16-bit RGB 5-6-5 18-bit RGB 6-6-6 18-bit RGB 6-6-6 (loosely packed) 24-bit RGB 8-8-8 – Transmission and reception of command packets HS-TX: Max. 1024 bytes LP-TX: Max. 128 bytes LP-RX: Max. 128 bytes
Security engine	• AES and ARC4 encryption and decryption algorithms implemented • RSA2048 signature verification algorithm implemented • SHA-224/256 tamper proofing algorithms implemented • Hardware Random Number Generator
Analog	• A/D converter: 12 channels, A/D converter: 8 channels (12 bits, 600 ksamples /sec) • Temperature sensor: 2 channels
Power control	• External power supply sequence control • Internal power domain control

Table 1.3-1 Overview of Functions (4/4)

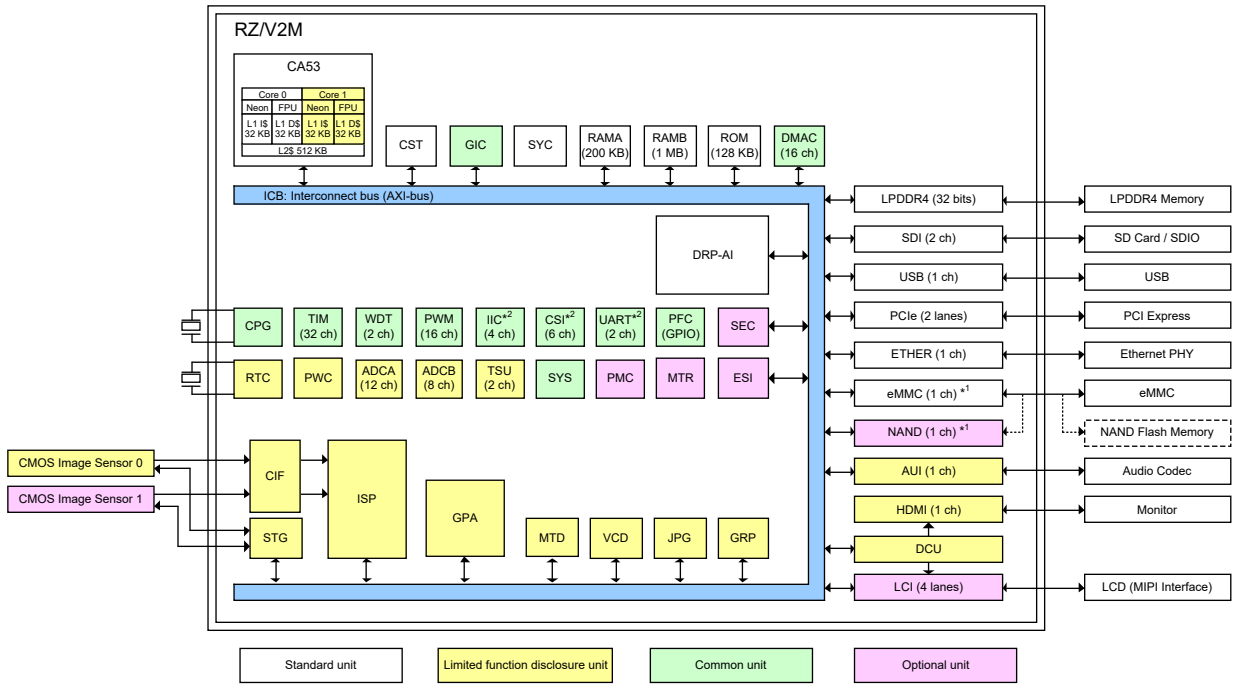
Item	Function
Power voltage	• 0.8-V power supply VDD08, RTVDD08, PWVDD08, LPVDD, PLDVDD08n (n = 1, 2, 3, 4, 6, 7), OTVDD08, TSnDVDD08A (n = 0, 1), LVRXAVDD, HDAVDD08, DSMSVDD0P8, PCVDD08, USDVDD, USVP, USVPTX • 1.1-V power supply LPVDDQ • 1.2-V power supply DSMVDD12 • 1.5-V power supply RTVDD • 1.8-V power supply PLVDDn (n = 1, 2, 3, 4, 6, 7), OTVDD18, TSnAVDD18 (n = 0, 1), ADnAVCCA (n = 0, 1), LVRXAVCC, LPVAA, HDAVDD18, DSMSVDD18, PCVDD18, USVDDH, PWVDD, VDD18, PAPREDVDD, PBPREDVDD, PCPREDVDD, IM0PREDVDD, IM1PREDVDD, NAPREDVDD, SD0PREDVDD, SD1FVDD,GEPREDVDD, PREDVDD33 • 3.3-V power supply USVD330, USVPH, VDD33 • 3.3-V/1.8-V switchable power supply PAMODVDD, PBMODVDD, PCMODVDD, IM0MODVDD, IM1MODVDD, NAMODVDD, SD0MODVDD, SD1FMODVDD,GEMODVDD
Operating temperature	Tj = 103ºC (max.) Tj: Junction temperature

1.4 Block Diagram

This LSI is equipped with the “standard unit”, “limited function disclosure unit”, and “optional unit”.

Unit Classification	Control	Disclosure of Register Specifications
Standard	User software	Disclosed
Limited function disclosure	Dedicated software: ISP support package (Controlled by the API in the unit of function and system operation)	Not disclosed
Common (standard/limited function disclosure)	Either of the followings within an unit is supported as the unit of function. • User software • Dedicated software: ISP support package	Disclosed
Optional	Contact a Renesas Electronics sales representative.	

Figure 1.4-1 shows the configuration.



ADCA:	A/D converter A	GRP:	2D graphics engine	RAMA:	RAM A
ADCB:	A/D converter B	HDMI:	HDMI Tx interface	RAMB:	RAM B
AUI:	Audio interface	ICB:	Interconnect bus	ROM:	ROM
CA53:	Arm Cortex-A53	IIC:	IIC Bus Interface	RTC:	Real-time clock
CIF:	CMOS image sensor interface	ISP:	Camera ISP	SDI:	SD host interface
CPG:	Clock pulse generator	JPG:	JPEG codec	SEC:	Trusted Secure IP
CSI:	Clocked serial interface	LCI:	LCD Control Interface (MIPI DSI)	STG:	Image sensor timing generator
CST:	Arm CoreSight	LPDDR4:	LPDDR4 interface	SYC:	System counter
DCU:	Display control unit	MTD:	Multi-target detection	SYS:	System configuration
DMAC:	DMA controller	MTR:	Motor controller	TIM:	Compare-match timer
DRP-AI:	AI accelerator	NAND:	NAND flash interface	TSU:	Temperature sensor
eMMC:	eMMC host interface	PCIe:	PCI Express 2.0 interface	UART:	Universal asynchronous receiver transmitter
ESI:	Environment sensor Interface	PFC:	Pin function controller	USB:	USB3.1 Gen1 interface
ETHER:	Ethernet MAC interface	PMC:	Internal power domain controller	VCD:	H.265/H.264 Multi Codec
GIC:	Generic interrupt controller	PWC:	External power sequence controller	WDT:	Watchdog timer
GPA:	General Processing Accelerator	PWM:	Pulse-width modulation timer		

Note 1. The use of NAND flash memory and eMMC is exclusive.

Note 2. The external pins of IIC, CSI, and UART are used exclusively. Depending on the combination, it may not be possible to use all other channels.

Figure 1.4-1 Block Diagram

1.5 List of Units

Table 1.5-1 List of Units (1/2)

Unit Name	Unit Abbreviation*1	Functional Overview
ADCA	ATGA	A/D converter A
ADCB	ATGB	A/D converter B
AUI	AUI	Audio interface
CA53	CA53	Arm Cortex-A53
CIF	CIF	CMOS image sensor interface
CPG	CPG	Clock pulse generator
CSI	CSI	Clocked serial interface
CST	CST	Arm CoreSight
DCU	DCI	Display control unit
DMAC	DMAA	DMA controller
DRP-AI	DRPA	AI accelerator (DRP-AI)
eMMC	EMM	eMMC host interface
ESI	SDT	Environment sensor interface
ETHER	ETH or ETH0	Ethernet MAC interface
GIC	GIC	Generic interrupt controller
GPA	GPA	General processing accelerator
GRP	GRP	2D graphics engine
HDMI	HMI	HDMI Tx interface
ICB	ICB	Interconnect bus
IIC	IIC	IIC bus interface
ISP	ISP	Camera ISP
JPG	JPG	JPEG codec
LCI	LCI	LCD control interface (MIPI DSI)
LPDDR4	DDR	LPDDR4 interface
MMC	MMC	LPDDR4 memory controller
DDI	DDI	LPDDR4 PHY interface
MTD	FCD	Multi-target detection
MTR	MTR	Motor controller
NAND	NFI	NAND flash interface
PCIe	PCI	PCI Express 2.0 interface
PFC	PFC	Pin function controller
PMC	PMC	Internal power domain controller
PWC	PWC	External power sequence controller
PWM	PWM	Pulse-width modulation timer
RAMA	RAMA	RAM A
RAMB	RAMB	RAM B
ROM	ROM	ROM
RTC	RTC	Real-time clock
SDI	SDI	SD host interface
SEC	SEC	Trusted secure IP
STG	STG	Image sensor timing generator
SYC	SYC	System counter

Table 1.5-1 List of Units (2/2)

Unit Name	Unit Abbreviation*1	Functional Overview
SYS	SYS	System configuration
TIM	TIM	Compare-match timer
TSU	TSU	Temperature sensor
UART	URT	Universal asynchronous receiver transmitter
USB	USB	USB3.1 Gen1 interface
VCD	VCD	H.265/H.264 multi codec
WDT	WDT	Watchdog timer

Note 1. Used as a prefix for the base address name of a register, terminal name, or signal name.

Section 2 Pin

This section describes the pins of this LSI.

2.1 Pin Assignment

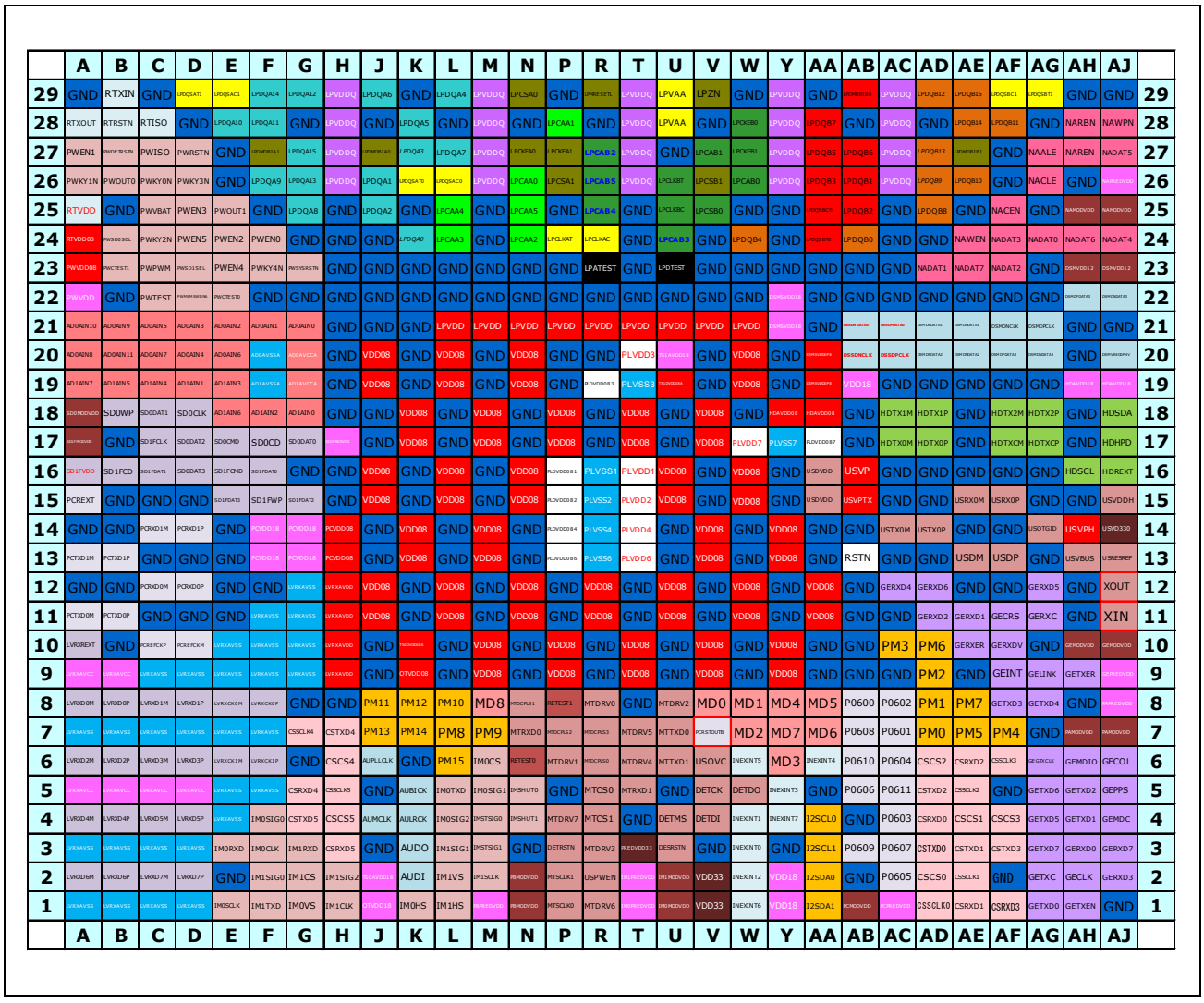


Figure 2.1-1 Pin Assignment (Top view)

Table 2.1-1 Ball Numbers and External Pin Names (1/5)

Ball Num.	External Pin Name
A1	LVRXAVSS
A2	LVRXD6M
A3	LVRXAVSS
A4	LVRXD4M
A5	LVRXAVCC
A6	LVRXD2M
A7	LVRXAVSS
A8	LVRXD0M
A9	LVRXAVCC
A10	LVRXREXT
A11	PCTXD0M
A12	GND
A13	PCTXD1M
A14	GND
A15	PCREXT
A16	SD1FVDD
A17	SD1FMODVDD
A18	SD0MODVDD
A19	AD1AIN7
A20	AD0AIN8
A21	AD0AIN10
A22	PWVDD
A23	PWVDD08
A24	RTVDD08
A25	RTVDD
A26	PWKY1N
A27	PWEN1
A28	RTXOUT
A29	GND
B1	LVRXAVSS
B2	LVRXD6P
B3	LVRXAVSS
B4	LVRXD4P
B5	LVRXAVCC
B6	LVRXD2P
B7	LVRXAVSS
B8	LVRXD0P
B9	LVRXAVCC
B10	GND
B11	PCTXD0P
B12	GND
B13	PCTXD1P
B14	GND
B15	GND
B16	SD1FCD

Ball Num.	External Pin Name
B17	GND
B18	SD0WP
B19	AD1AIN5
B20	AD0AIN11
B21	AD0AIN9
B22	GND
B23	PWCTEST1
B24	PWSD0SEL
B25	GND
B26	PWOUT0
B27	PWDETRSTN
B28	RTRSTN
B29	RTXIN
C1	LVRXAVSS
C2	LVRXD7M
C3	LVRXAVSS
C4	LVRXD5M
C5	LVRXAVCC
C6	LVRXD3M
C7	LVRXAVSS
C8	LVRXD1M
C9	LVRXAVSS
C10	PCREFCKP
C11	GND
C12	PCRXD0M
C13	GND
C14	PCRXD1M
C15	GND
C16	SD1FDAT1
C17	SD1FCLK
C18	SD0DAT1
C19	AD1AIN4
C20	AD0AIN7
C21	AD0AIN5
C22	PWTEST
C23	PWPWM
C24	PWKY2N
C25	PWVBAT
C26	PWKY0N
C27	PWISO
C28	RTISO
C29	GND
D1	LVRXAVSS
D2	LVRXD7P
D3	LVRXAVSS

Ball Num.	External Pin Name
D4	LVRXD5P
D5	LVRXAVCC
D6	LVRXD3P
D7	LVRXAVSS
D8	LVRXD1P
D9	LVRXAVSS
D10	PCREFCKM
D11	GND
D12	PCRXD0P
D13	GND
D14	PCRXD1P
D15	GND
D16	SD0DAT3
D17	SD0DAT2
D18	SD0CLK
D19	AD1AIN1
D20	AD0AIN4
D21	AD0AIN3
D22	PWMEMSWIENA
D23	PWSD1SEL
D24	PWEN5
D25	PWEN3
D26	PWKY3N
D27	PWRSTN
D28	GND
D29	LPDQSAT1
E1	IM0SCLK
E2	GND
E3	IM0RXD
E4	LVRXAVSS
E5	LVRXAVSS
E6	LVRXCK1M
E7	LVRXAVSS
E8	LVRXCK0M
E9	LVRXAVSS
E10	LVRXAVSS
E11	GND
E12	GND
E13	GND
E14	GND
E15	SD1FDAT3
E16	SD1FCMD
E17	SD0CMD
E18	AD1AIN6
E19	AD1AIN3

Ball Num.	External Pin Name
E20	AD0AIN6
E21	AD0AIN2
E22	PWCTEST0
E23	PWEN4
E24	PWEN2
E25	PWOUT1
E26	GND
E27	GND
E28	LPDQA10
E29	LPDQSAC1
F1	IM1TXD
F2	IM1SIG0
F3	IM0CLK
F4	IM0SIG0
F5	LVRXAVSS
F6	LVRXCK1P
F7	LVRXAVSS
F8	LVRXCK0P
F9	LVRXAVSS
F10	LVRXAVSS
F11	LVRXAVSS
F12	GND
F13	PCVDD18
F14	PCVDD18
F15	SD1FWP
F16	SD1FDAT0
F17	SD0CD
F18	AD1AIN2
F19	AD1AVSSA
F20	AD0AVSSA
F21	AD0AIN1
F22	GND
F23	PWKY4N
F24	PWEN0
F25	GND
F26	LPDQA9
F27	LPDMDBIA1
F28	LPDQA11
F29	LPDQA14
G1	IM0VS
G2	IM1CS
G3	IM1RXD
G4	CSTXD5
G5	CSRXD4
G6	GND

Table 2.1-1 Ball Numbers and External Pin Names (2/5)

Ball Num.	External Pin Name
G7	CSSCLK4
G8	GND
G9	LVRXAVSS
G10	LVRXAVSS
G11	LVRXAVSS
G12	LVRXAVSS
G13	PCVDD18
G14	PCVDD18
G15	SD1FDAT2
G16	GND
G17	SD0DAT0
G18	AD1AIN0
G19	AD1AVCCA
G20	AD0AVCCA
G21	AD0AIN0
G22	GND
G23	PWSYSRSTN
G24	GND
G25	LPDQA8
G26	LPDQA13
G27	LPDQA15
G28	GND
G29	LPDQA12
H1	IM1CLK
H2	IM1SIG2
H3	CSRXD5
H4	CSCS5
H5	CSSCLK5
H6	CSCS4
H7	CSTXD4
H8	GND
H9	LVRXAVDD
H10	LVRXAVDD
H11	LVRXAVDD
H12	LVRXAVDD
H13	PCVDD08
H14	PCVDD08
H15	GND
H16	GND
H17	SD0PREDVDD
H18	GND
H19	GND
H20	GND
H21	GND
H22	GND

Ball Num.	External Pin Name
H23	GND
H24	GND
H25	GND
H26	LPVDDQ
H27	LPVDDQ
H28	LPVDDQ
H29	LPVDDQ
J1	OTVDD18
J2	TS0AVDD18
J3	GND
J4	AUMCLK
J5	GND
J6	AUPLLCLK
J7	PM13
J8	PM11
J9	GND
J10	GND
J11	VDD08
J12	VDD08
J13	GND
J14	GND
J15	VDD08
J16	VDD08
J17	GND
J18	GND
J19	VDD08
J20	VDD08
J21	GND
J22	GND
J23	GND
J24	GND
J25	LPDQA2
J26	LPDQA1
J27	LPDMDBIA0
J28	GND
J29	LPDQA6
K1	IM0HS
K2	AUDI
K3	AUDO
K4	AULRCK
K5	AUBICK
K6	GND
K7	PM14
K8	PM12
K9	OTVDD08

Ball Num.	External Pin Name
K10	TS0DVDD08A
K11	GND
K12	GND
K13	VDD08
K14	VDD08
K15	GND
K16	GND
K17	VDD08
K18	VDD08
K19	GND
K20	GND
K21	GND
K22	GND
K23	GND
K24	LPDQA0
K25	GND
K26	LPDQSAT0
K27	LPDQA3
K28	LPDQA5
K29	GND
L1	IM1HS
L2	IM1VS
L3	IM1SIG1
L4	IM0SIG2
L5	IM0TXD
L6	PM15
L7	PM8
L8	PM10
L9	GND
L10	GND
L11	VDD08
L12	VDD08
L13	GND
L14	GND
L15	VDD08
L16	VDD08
L17	GND
L18	GND
L19	VDD08
L20	VDD08
L21	LPVDD
L22	GND
L23	GND
L24	LPCAA3
L25	LPCAA4

Ball Num.	External Pin Name
L26	LPDQSAC0
L27	LPDQA7
L28	GND
L29	LPDQA4
M1	PBPREDVDD
M2	IM1SCLK
M3	IMSTSIG1
M4	IMSTSIG0
M5	IM0SIG1
M6	IM0CS
M7	PM9
M8	MD8
M9	VDD08
M10	VDD08
M11	GND
M12	GND
M13	VDD08
M14	VDD08
M15	GND
M16	GND
M17	VDD08
M18	VDD08
M19	GND
M20	GND
M21	LPVDD
M22	GND
M23	GND
M24	GND
M25	GND
M26	LPVDDQ
M27	LPVDDQ
M28	LPVDDQ
M29	LPVDDQ
N1	PBMODVDD
N2	PBMODVDD
N3	GND
N4	IMSHUT1
N5	IMSHUT0
N6	RETEST0
N7	MTRXD0
N8	MTDCPLS1
N9	GND
N10	GND
N11	VDD08
N12	VDD08

Table 2.1-1 Ball Numbers and External Pin Names (3/5)

Ball Num.	External Pin Name
N13	GND
N14	GND
N15	VDD08
N16	VDD08
N17	GND
N18	GND
N19	VDD08
N20	VDD08
N21	LPVDD
N22	GND
N23	GND
N24	LPCAA2
N25	LPCAA5
N26	LPCAA0
N27	LPCKEA0
N28	GND
N29	LPCSA0
P1	MTSCLK0
P2	MTSCLK1
P3	DETRSTN
P4	MTDRV7
P5	GND
P6	MTDRV1
P7	MTDCPLS2
P8	RETEST1
P9	VDD08
P10	VDD08
P11	GND
P12	GND
P13	PLDVDD086
P14	PLDVDD084
P15	PLDVDD082
P16	PLDVDD081
P17	VDD08
P18	VDD08
P19	GND
P20	GND
P21	LPVDD
P22	GND
P23	GND
P24	LPCLKAT
P25	GND
P26	LPCSA1
P27	LPCKEA1
P28	LPCAA1

Ball Num.	External Pin Name
P29	GND
R1	MTDRV6
R2	USPWEN
R3	MTDRV3
R4	MTCS1
R5	MTCS0
R6	MTDCPLS0
R7	MTDCPLS3
R8	MTDRV0
R9	GND
R10	GND
R11	VDD08
R12	VDD08
R13	PLVSS6
R14	PLVSS4
R15	PLVSS2
R16	PLVSS1
R17	GND
R18	GND
R19	PLDVDD083
R20	GND
R21	LPVDD
R22	GND
R23	LPATEST
R24	LPCLKAC
R25	LPCAB4
R26	LPCAB5
R27	LPCAB2
R28	GND
R29	LPMRESETL
T1	IM0PREDVDD
T2	IM1PREDVDD
T3	PREDVDD33
T4	GND
T5	MTRXD1
T6	MTDRV4
T7	MTDRV5
T8	GND
T9	VDD08
T10	VDD08
T11	GND
T12	GND
T13	PLVDD6
T14	PLVDD4
T15	PLVDD2

Ball Num.	External Pin Name
T16	PLVDD1
T17	VDD08
T18	VDD08
T19	PLVSS3
T20	PLVDD3
T21	LPVDD
T22	GND
T23	GND
T24	GND
T25	GND
T26	LPVDDQ
T27	LPVDDQ
T28	LPVDDQ
T29	LPVDDQ
U1	IM0MODVDD
U2	IM1MODVDD
U3	DESRSTN
U4	DETMS
U5	GND
U6	MTTXD1
U7	MTTXD0
U8	MTDRV2
U9	GND
U10	GND
U11	VDD08
U12	VDD08
U13	GND
U14	GND
U15	VDD08
U16	VDD08
U17	GND
U18	GND
U19	TS1DVDD08A
U20	TS1AVDD18
U21	LPVDD
U22	GND
U23	LPDTEST
U24	LPCAB3
U25	LPCLKBC
U26	LPCLKBT
U27	GND
U28	LPVAA
U29	LPVAA
V1	VDD33
V2	VDD33

Ball Num.	External Pin Name
V3	GND
V4	DETDI
V5	DETCK
V6	USOVC
V7	PCRSTOUTB
V8	MD0
V9	VDD08
V10	VDD08
V11	GND
V12	GND
V13	VDD08
V14	VDD08
V15	GND
V16	GND
V17	VDD08
V18	VDD08
V19	GND
V20	GND
V21	LPVDD
V22	GND
V23	GND
V24	GND
V25	LPCSB0
V26	LPCSB1
V27	LPCAB1
V28	GND
V29	LPZN
W1	INEXINT6
W2	INEXINT2
W3	INEXINT0
W4	INEXINT1
W5	DETDO
W6	INEXINT5
W7	MD2
W8	MD1
W9	GND
W10	GND
W11	VDD08
W12	VDD08
W13	GND
W14	GND
W15	VDD08
W16	VDD08
W17	PLVDD7
W18	GND

Table 2.1-1 Ball Numbers and External Pin Names (4/5)

Ball Num.	External Pin Name
W19	VDD08
W20	VDD08
W21	LPVDD
W22	GND
W23	GND
W24	LPDQB4
W25	GND
W26	LPCAB0
W27	LPCKEB1
W28	LPCKEB0
W29	GND
Y1	VDD18
Y2	VDD18
Y3	GND
Y4	INEXINT7
Y5	INEXINT3
Y6	MD3
Y7	MD7
Y8	MD4
Y9	VDD08
Y10	VDD08
Y11	GND
Y12	GND
Y13	VDD08
Y14	VDD08
Y15	GND
Y16	GND
Y17	PLVSS7
Y18	HDAVDD08
Y19	GND
Y20	GND
Y21	DSMSVDD18
Y22	DSMSVDD18
Y23	GND
Y24	GND
Y25	GND
Y26	LPVDDQ
Y27	LPVDDQ
Y28	LPVDDQ
Y29	LPVDDQ
AA1	I2SDA1
AA2	I2SDA0
AA3	I2SCL1
AA4	I2SCL0
AA5	GND

Ball Num.	External Pin Name
AA6	INEXINT4
AA7	MD6
AA8	MD5
AA9	GND
AA10	GND
AA11	VDD08
AA12	VDD08
AA13	GND
AA14	GND
AA15	USDVDD
AA16	USDVDD
AA17	PLDVDD087
AA18	HDAVDD08
AA19	DSMSVDD0P8
AA20	DSMSVDD0P8
AA21	GND
AA22	GND
AA23	GND
AA24	LPDQSBT0
AA25	LPDQSBC0
AA26	LPDQB3
AA27	LPDQB5
AA28	LPDQB7
AA29	GND
AB1	PCMODVDD
AB2	GND
AB3	P0609
AB4	GND
AB5	P0606
AB6	P0610
AB7	P0608
AB8	P0600
AB9	GND
AB10	GND
AB11	GND
AB12	GND
AB13	RSTN
AB14	GND
AB15	USVPTX
AB16	USVP
AB17	GND
AB18	GND
AB19	VDD18
AB20	DSSDNCLK
AB21	DSSDNDATA0

Ball Num.	External Pin Name
AB22	GND
AB23	GND
AB24	LPDQB0
AB25	LPDQB2
AB26	LPDQB1
AB27	LPDQB6
AB28	GND
AB29	LPDMDBIB0
AC1	PCPREDVDD
AC2	P0605
AC3	P0607
AC4	P0603
AC5	P0611
AC6	P0604
AC7	P0601
AC8	P0602
AC9	GND
AC10	PM3
AC11	GND
AC12	GERXD4
AC13	GND
AC14	USTX0M
AC15	GND
AC16	GND
AC17	HDTX0M
AC18	HDTX1M
AC19	GND
AC20	DSSDPCLK
AC21	DSSDPDATA0
AC22	GND
AC23	GND
AC24	GND
AC25	GND
AC26	LPVDDQ
AC27	LPVDDQ
AC28	LPVDDQ
AC29	LPVDDQ
AD1	CSSCLK0
AD2	CSCS0
AD3	CSTXD0
AD4	CSRXD0
AD5	CSTXD2
AD6	CSCS2
AD7	PM0
AD8	PM1

Ball Num.	External Pin Name
AD9	PM2
AD10	PM6
AD11	GERXD2
AD12	GERXD6
AD13	GND
AD14	USTX0P
AD15	GND
AD16	GND
AD17	HDTX0P
AD18	HDTX1P
AD19	GND
AD20	DSMDPDATA2
AD21	DSMDPDATA1
AD22	GND
AD23	NADAT1
AD24	GND
AD25	LPDQB8
AD26	LPDQB9
AD27	LPDQB13
AD28	GND
AD29	LPDQB12
AE1	CSRXD1
AE2	CSSCLK1
AE3	CSTXD1
AE4	CSCS1
AE5	CSSCLK2
AE6	CSRXD2
AE7	PM5
AE8	PM7
AE9	GND
AE10	GERXER
AE11	GERXD1
AE12	GND
AE13	USDM
AE14	GND
AE15	USRX0M
AE16	GND
AE17	GND
AE18	GND
AE19	GND
AE20	DSMDNDATA2
AE21	DSMDNDATA1
AE22	GND
AE23	NADAT7
AE24	NAWEN

Table 2.1-1 Ball Numbers and External Pin Names (5/5)

Ball Num.	External Pin Name
AE25	GND
AE26	LPDQB10
AE27	LPDMDBIB1
AE28	LPDQB14
AE29	LPDQB15
AF1	CSRXD3
AF2	GND
AF3	CSTXD3
AF4	CSCS3
AF5	GND
AF6	CSSCLK3
AF7	PM4
AF8	GETXD3
AF9	GEINT
AF10	GERXDV
AF11	GECRS
AF12	GND
AF13	USDP
AF14	GND
AF15	USRX0P
AF16	GND
AF17	HDTXCM
AF18	HDTX2M
AF19	GND
AF20	DSMDPDATA3
AF21	DSMDNCLK
AF22	GND
AF23	NADAT2
AF24	NADAT3
AF25	NACEN
AF26	GND

Ball Num.	External Pin Name
AF27	GND
AF28	LPDQB11
AF29	LPDQSBC1
AG1	GETXD0
AG2	GETXC
AG3	GETXD7
AG4	GETXD5
AG5	GETXD6
AG6	GEGTXCLK
AG7	GND
AG8	GETXD4
AG9	GELINK
AG10	GND
AG11	GERXC
AG12	GERXD5
AG13	GND
AG14	USOTGID
AG15	GND
AG16	GND
AG17	HDTXCP
AG18	HDTX2P
AG19	GND
AG20	DSMDNDATA3
AG21	DSMDPCLK
AG22	GND
AG23	GND
AG24	NADAT0
AG25	GND
AG26	NACLE
AG27	NAALE
AG28	GND

Ball Num.	External Pin Name
AG29	LPDQSBT1
AH1	GETXEN
AH2	GECLK
AH3	GERXD0
AH4	GETXD1
AH5	GETXD2
AH6	GEMDIO
AH7	PAMODVDD
AH8	GND
AH9	GETXER
AH10	GEMODVDD
AH11	GND
AH12	GND
AH13	USVBUS
AH14	USVPH
AH15	GND
AH16	HDSCL
AH17	GND
AH18	GND
AH19	HDAVDD18
AH20	GND
AH21	GND
AH22	DSMDPDATA0
AH23	DSMVDD12
AH24	NADAT6
AH25	NAMODVDD
AH26	GND
AH27	NAREN
AH28	NARBN
AH29	GND
AJ1	GND

Ball Num.	External Pin Name
AJ2	GERXD3
AJ3	GERXD7
AJ4	GEMDC
AJ5	GEPPS
AJ6	GECOL
AJ7	PAMODVDD
AJ8	PAPREDVDD
AJ9	GEPREDVDD
AJ10	GEMODVDD
AJ11	XIN
AJ12	XOUT
AJ13	USRESREF
AJ14	USVD330
AJ15	USVDDH
AJ16	HDREXT
AJ17	HDHPD
AJ18	HDSDA
AJ19	HDAVDD18
AJ20	DSMVREG0P4V
AJ21	GND
AJ22	DSMDNDATA0
AJ23	DSMVDD12
AJ24	NADAT4
AJ25	NAMODVDD
AJ26	NAPREDVDD
AJ27	NADAT5
AJ28	NAWPN
AJ29	GND
—	—
—	—
—	—

2.2 External Pins

2.2.1 List of External Pins

Table 2.2-1 List of External Pins (1/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
RTXIN	I	1.5	1.5-V OSC	CLOCK	Pull down	—	—	—	—	—
RTXOUT	O	1.5	1.5-V OSC	CLOCK	Open	—	—	—	—	—
RTRSTN	I	1.5	RTC I/O	Don't care	Pull down	●	OFF	—	—	—
RTISO	I	1.5	RTC I/O	Hi-Z	Pull up	●	OFF	—	—	—
RTVDD	—	1.5	RTC I/O, 1.5-V OSC power supply	—	—	—	—	—	—	—
RTVDD08	—	0.8	RTC core power supply	—	—	—	—	—	—	—
PWRSTN	I	1.8	PWC I/O	Don't care	Pull down	●	OFF	—	—	—
PWTEST	I	1.8	PWC I/O	Don't care	Pull down	●	OFF	—	—	—
PWVBAT	I	1.8	PWC I/O	Don't care	Pull up	●	OFF	—	—	—
PWKY0N	I	1.8	PWC I/O	Don't care	Pull up	●	OFF	—	—	—
PWKY1N	I	1.8	PWC I/O	Don't care	Pull up	●	OFF	—	—	—
PWKY2N	I	1.8	PWC I/O	Don't care	Pull up	●	OFF	—	—	—
PWKY3N	I	1.8	PWC I/O	Don't care	Pull up	●	OFF	—	—	—
PWKY4N	I	1.8	PWC I/O	Don't care	Pull up	●	OFF	—	—	—
PWDETRSTN	I	1.8	PWC I/O	Don't care	Pull up	●	OFF	—	—	—
PWEN0	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN1	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN2	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN3	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN4	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWEN5	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWSYSRSTN	O	1.8	PWC I/O	L	Open	—	—	●	Fixed*2	—
PWOUT0	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWOUT1	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWPWM	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWSD0SEL	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWSD1SEL	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWCTEST0	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWCTEST1	I	1.8	PWC I/O	Don't care	Pull up	●	OFF	—	—	—
PWMEMSWIENA	O	1.8	PWC I/O	L	Open	—	—	—	Fixed*2	—
PWISO	O	1.8	PWC I/O	Hi-Z	Open	—	—	●	Fixed*2	—
PWVDD08	—	0.8	PWC core power supply	—	—	—	—	—	—	—
PWVDD	—	1.8	PWC I/O power supply	—	—	—	—	—	—	—
NADAT0	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NADAT1	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NADAT2	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)

Table 2.2-1 List of External Pins (2/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
NADAT3	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NADAT4	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NADAT5	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NADAT6	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NADAT7	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NACEN	IO	3.3/1.8	PORT00 I/O	PU	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NAREN	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NAWEN	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NACLE	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NAALE	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NARBN	IO	3.3/1.8	PORT00 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-3**)
NAWPN	O	3.3/1.8	PORT00 I/O	L	Open	—	—	—	Selectable*2	—
NAMODVDD	—	3.3/1.8	PORT00 I/O power supply	—	—	—	—	—	—	—
NAPREDVDD	—	1.8	PORT00 pre-driver power supply	—	—	—	—	—	—	—
PM0*3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM1*3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM2*3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM3*3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)

Table 2.2-1 List of External Pins (3/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
PM4*3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM5*3	IO	3.3/1.8	PORT01(A) I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM6*3	IO	3.3/1.8	PORT01(A) I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM7*3	IO	3.3/1.8	PORT01(A) I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PAMODVDD	—	3.3/1.8	PORT01(A), PORT03 I/O power supply	—	—	—	—	—	—	—
PAPREDVDD	—	1.8	PORT01(A), PORT03 pre-driver power supply	—	—	—	—	—	—	—
PM8	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM9	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM10	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM11	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM12	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM13	IO	3.3/1.8	PORT01(B) I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM14	IO	3.3/1.8	PORT01(B) I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PM15*3	IO	3.3/1.8	PORT01(B) I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-4**)
PBMODVDD	—	3.3/1.8	PORT01(B), PORT04, PORT07, PORT21 I/O power supply	—	—	—	—	—	—	—
PBPREDVDD	—	1.8	PORT01(B), PORT04, PORT07, PORT21 pre-driver power supply	—	—	—	—	—	—	—
INEXINT0*1 *3	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)

Table 2.2-1 List of External Pins (4/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
INEXINT1*1 *3	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
INEXINT2*1 *3	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
INEXINT3*1 *3	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
INEXINT4*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
INEXINT5*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
INEXINT6*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
INEXINT7*1	IO	1.8	PORT02 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-5**)
CSTXD0	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSRXD0	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSSCLK0	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSCS0	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSTXD1*3	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSRXD1*3	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSSCLK1*3	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSCS1*3	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSTXD2	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSRXD2	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)

Table 2.2-1 List of External Pins (5/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
CSSCLK2*3	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSCS2*3	IO	3.3/1.8	PORT03 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSTXD3*3	IO	3.3/1.8	PORT03 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSRXD3*3	IO	3.3/1.8	PORT03 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSSCLK3*3	IO	3.3/1.8	PORT03 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSCS3*3	IO	3.3/1.8	PORT03 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-6**)
CSTXD4	IO	3.3/1.8	PORT04 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSRXD4	IO	3.3/1.8	PORT04 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSSCLK4	IO	3.3/1.8	PORT04 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSCS4	IO	3.3/1.8	PORT04 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSTXD5*3	IO	3.3/1.8	PORT04 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSRXD5*3	IO	3.3/1.8	PORT04 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSSCLK5*3	IO	3.3/1.8	PORT04 I/O	PD	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
CSCS5*3	IO	3.3/1.8	PORT04 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-7**)
I2SDA0*1	IO	1.8	PORT05 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-8**)
I2SCL0*1	IO	1.8	PORT05 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-8**)
I2SDA1*1,*3	IO	1.8	PORT05 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-8**)

Table 2.2-1 List of External Pins (6/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
I2SCL1*1,*3	IO	1.8	PORT05 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-8**)
P0600*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0601*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0602*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0603*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0604*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0605*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0606*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0607*3	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0608	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0609	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0610	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
P0611	IO	3.3/1.8	PORT06 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-9**)
PCMODVDD	—	3.3/1.8	PORT06 I/O power supply	—	—	—	—	—	—	—
PCPREDVDD	—	1.8	PORT06 pre-driver power supply	—	—	—	—	—	—	—
AULRCK*3	IO	3.3/1.8	PORT07 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-10**)
AUBICK*3	IO	3.3/1.8	PORT07 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-10**)
AUDI*3	IO	3.3/1.8	PORT07 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-10**)

Table 2.2-1 List of External Pins (7/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
AUDO*3	IO	3.3/1.8	PORT07 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-10**)
AUMCLK*3	IO	3.3/1.8	PORT07 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-10**)
AUPLLCLK*3	IO	3.3/1.8	PORT07 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-10**)
SD0CMD	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0CLK	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0DAT0	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0DAT1	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0DAT2	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0DAT3	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0WP	IO	3.3/1.8	PORT08 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0CD	IO	3.3/1.8	PORT08 I/O	PU	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-11**)
SD0MODVDD	—	3.3/1.8	PORT08 I/O power supply	—	—	—	—	—	—	—
SD0PREDVDD	—	1.8	PORT08 pre-driver power supply	—	—	—	—	—	—	—
SD1FCMD	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FCLK	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FDAT0	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FDAT1	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FDAT2	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)

Table 2.2-1 List of External Pins (8/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
SD1FDAT3	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FWP	IO	3.3/1.8	PORT09 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FCD	IO	3.3/1.8	PORT09 I/O	PU	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-12**)
SD1FMODVDD	—	3.3/1.8	PORT09 I/O power supply	—	—	—	—	—	—	—
SD1FVDD	—	1.8	PORT09 pre-driver power supply	—	—	—	—	—	—	—
IM0VS*3	IO	3.3/1.8	PORT10 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
IM0HS*3	IO	3.3/1.8	PORT10 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
IM0CLK*3	O	3.3/1.8	PORT10 I/O	L	Open	—	PU/PD/OFF changeable	—	Selectable*2	—
IM0CS*3	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
IM0TXD*3	IO	3.3/1.8	PORT10 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
IM0RXD*3	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
IM0SCLK*3	IO	3.3/1.8	PORT10 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
IM0SIG0*3	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
IM0SIG1*3	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
IM0SIG2*3	IO	3.3/1.8	PORT10 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-13**)
IM0MODVDD	—	3.3/1.8	PORT10 I/O power supply	—	—	—	—	—	—	—
IM0PREDVDD	—	1.8	PORT10 pre-driver power supply	—	—	—	—	—	—	—
IM1VS*3	IO	3.3/1.8	PORT11 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
IM1HS*3	IO	3.3/1.8	PORT11 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)

Table 2.2-1 List of External Pins (9/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
IM1CLK*3	O	3.3/1.8	PORT11 I/O	L	Open	—	OFF	—	Selectable*2	—
IM1CS*3	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
IM1TXD*3	IO	3.3/1.8	PORT11 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
IM1RXD*3	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
IM1SCLK*3	IO	3.3/1.8	PORT11 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
IM1SIG0*3	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
IM1SIG1*3	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
IM1SIG2*3	IO	3.3/1.8	PORT11 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-14**)
IM1MODVDD	—	3.3/1.8	PORT11 I/O power supply	—	—	—	—	—	—	—
IM1PREDVDD	—	1.8	PORT11 pre-driver power supply	—	—	—	—	—	—	—
IMSHUT0*3	IO	3.3	PORT12 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-15**)
IMSHUT1*3	IO	3.3	PORT12 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-15**)
IMSTSIG0*3	IO	3.3	PORT12 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-15**)
IMSTSIG1*3	IO	3.3	PORT12 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-15**)
MTDRV0*3	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
MTDRV1*3	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
MTDRV2*3	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
MTDRV3*3	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)

Table 2.2-1 List of External Pins (10/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
MTDRV4*3	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
MTDRV5*3	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
MTDRV6*3	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
MTDRV7*3	IO	3.3	PORT13 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
MTDCPLS0*3	IO	3.3	PORT13 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
MTDCPLS1*3	IO	3.3	PORT13 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
MTDCPLS2*3	IO	3.3	PORT13 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
MTDCPLS3*3	IO	3.3	PORT13 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-16**)
MTCS0*3	IO	3.3	PORT14 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
MTTXD0*3	IO	3.3	PORT14 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
MTRXD0*3	IO	3.3	PORT14 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
MTSCLK0*3	IO	3.3	PORT14 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
MTCS1*3	IO	3.3	PORT14 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
MTTXD1*3	IO	3.3	PORT14 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
MTRXD1*3	IO	3.3	PORT14 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
MTSCLK1*3	IO	3.3	PORT14 I/O	PD	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-17**)
GETXC	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)

Table 2.2-1 List of External Pins (11/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
GETXEN	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXER	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD0	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD1	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD2	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD3	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD4	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD5	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD6	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GETXD7	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GERXC	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GERXDV	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GERXER	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GERXD0	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GERXD1	IO	3.3/1.8	PORT15 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-18**)
GERXD2	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GERXD3	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)

Table 2.2-1 List of External Pins (12/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
GERXD4	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GERXD5	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GERXD6	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GERXD7	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GECRS	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GECOL	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GEMDC	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GEMDIO	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GEGTXCLK	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GELINK	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GEINT	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	●	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GECLK	IO	3.3/1.8	PORT16 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-19**)
GEPPS	IO	3.3/1.8	PORT17 I/O	Hi-Z	Open	—	PU/PD/OFF changeable	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-20**)
GEMODVDD	—	3.3/1.8	PORT15, PORT16, PORT17 I/O power supply	—	—	—	—	—	—	—
GEPREDVDD	—	1.8	PORT15, PORT16, PORT17 pre-driver power supply	—	—	—	—	—	—	—
DETCK	I	1.8	Debugger I/O	PD	Open	—	PD	—	—	—
DETDI	I	1.8	Debugger I/O	PU	Open	—	PU	—	—	—
DETDO	O	1.8	Debugger I/O	Hi-Z	Open	—	OFF	—	Selectable*2	—
DETMS	IO	1.8	Debugger I/O	PU	Open	—	PU	—	Selectable*2	—
DETRSTN	I	1.8	Debugger I/O	PU	Open	—	PU	—	—	—
DESRSTN	I	1.8	Debugger I/O	PU	Open	—	PU	—	—	—
RETEST0	I	3.3	LSI test I/O	PD	Pull down	●	PD	—	—	—
RETEST1	I	3.3	LSI test I/O	PD	Pull down	●	PD	—	—	—

Table 2.2-1 List of External Pins (13/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
LPATEST	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA0	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA1	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA2	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA3	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA4	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAA5	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB0	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB1	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB2	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB3	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB4	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCAB5	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCKEA0	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPCKEA1	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPCKEB0	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPCKEB1	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPCLKAC	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCLKAT	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCLKBC	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCLKBT	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCSA0	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCSA1	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCSB0	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPCSB1	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDMDBIA0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDMDBIA1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDMDBIB0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDMDBIB1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA2	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA3	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA4	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA5	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA6	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA7	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA8	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA9	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA10	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA11	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA12	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA13	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA14	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQA15	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB2	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB3	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB4	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—

Table 2.2-1 List of External Pins (14/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
LPDQB5	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB6	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB7	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB8	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB9	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB10	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB11	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB12	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB13	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB14	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQB15	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSAC0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSAC1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSAT0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSAT1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSBC0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSBC1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSBT0	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPDQSBT1	IO	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPMRESETL	O	1.1	LPDDR4 PHY	L	Open	—	—	—	—	—
LPZN	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LPVAA	—	1.8	LPDDR4 PLL 1.8-V power supply	—	—	—	—	—	—	—
LPVDD	—	0.8	LPDDR4 core 0.8-V power supply	—	—	—	—	—	—	—
LPVDDQ	—	1.1	LPDDR4 PHY 1.1-V power supply	—	—	—	—	—	—	—
LPDTEST	O	1.1	LPDDR4 PHY	Hi-Z	Open	—	—	—	—	—
LVRXD0P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD0P
LVRXD0M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD0M
LVRXD1P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD1P
LVRXD1M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD1M
LVRXD2P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD2P
LVRXD2M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD2M
LVRXD3P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD3P
LVRXD3M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD3M
LVRXCK0P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXCK0P
LVRXCK0M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXCK0M
LVRXD4P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD4P
LVRXD4M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD4M
LVRXD5P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD5P
LVRXD5M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD5M
LVRXD6P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD6P
LVRXD6M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD6M
LVRXD7P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD7P
LVRXD7M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXD7M
LVRXCK1P	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXCK1P
LVRXCK1M	I	1.8	CIF PHY	Hi-Z	Pull down	—	—	—	—	MPRXCK1M
LVRXREXT	I	1.8	CIF PHY	Hi-Z	Pull down (10KΩ)	—	—	—	—	—
LVRXAVCC	—	1.8	CIF PHY 1.8-V power supply	—	—	—	—	—	—	—

Table 2.2-1 List of External Pins (15/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
LVRXAVDD	—	0.8	CIF PHY 0.8-V power supply	—	—	—	—	—	—	—
LVRXAVSS	—	0	CIF PHY GND	—	—	—	—	—	—	—
DSMDPDATA0	IO	1.8	MIPI DSI Tx PHY	L	Open	—	—	—	—	—
DSMDNDATA0	IO	1.8	MIPI DSI Tx PHY	L	Open	—	—	—	—	—
DSMDPDATA1	IO	1.8	MIPI DSI Tx PHY	L	Open	—	—	—	—	—
DSMDNDATA1	IO	1.8	MIPI DSI Tx PHY	L	Open	—	—	—	—	—
DSMDPDATA2	IO	1.8	MIPI DSI Tx PHY	L	Open	—	—	—	—	—
DSMDNDATA2	IO	1.8	MIPI DSI Tx PHY	L	Open	—	—	—	—	—
DSMDPDATA3	IO	1.8	MIPI DSI Tx PHY	L	Open	—	—	—	—	—
DSMDNDATA3	IO	1.8	MIPI DSI Tx PHY	L	Open	—	—	—	—	—
DSMDPCLK	IO	1.8	MIPI DSI Tx PHY	L	Open	—	—	—	—	—
DSMDNCLK	IO	1.8	MIPI DSI Tx PHY	L	Open	—	—	—	—	—
DSMVREG0P4V	IO	1.8	MIPI DSI Tx PHY	L	Open (external capacitor not required)	—	—	—	—	—
DSSDPDATA0	IO	1.8	MIPI DSI Tx PHY	Hi-Z	Pull down	—	—	—	—	—
DSSDNDATA0	IO	1.8	MIPI DSI Tx PHY	Hi-Z	Pull down	—	—	—	—	—
DSSDPCLK	IO	1.8	MIPI DSI Tx PHY	Hi-Z	Pull down	—	—	—	—	—
DSSDNCLK	IO	1.8	MIPI DSI Tx PHY	Hi-Z	Pull down	—	—	—	—	—
DSMSVDD18	—	1.8	MIPI DSI Tx PHY 1.8-V power supply	—	—	—	—	—	—	—
DSMVDD12	—	1.2	MIPI DSI Tx PHY 1.2-V power supply	—	—	—	—	—	—	—
DSMSVDD0P8	—	0.8	MIPI DSI Tx PHY 0.8-V power supply	—	—	—	—	—	—	—
PCRXD0P	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCRXD0M	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCTXD0P	O	1.8	PCIe PHY	X	Open	—	—	—	—	—
PCTXD0M	O	1.8	PCIe PHY	X	Open	—	—	—	—	—
PCREFCKP	I	1.8	PCIe PHY	CLOCK	Open	—	—	—	—	—
PCREFCKM	I	1.8	PCIe PHY	CLOCK	Open	—	—	—	—	—
PCREXT	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCRXD1P	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCRXD1M	I	1.8	PCIe PHY	—	Open	—	—	—	—	—
PCTXD1P	O	1.8	PCIe PHY	X	Open	—	—	—	—	—
PCTXD1M	O	1.8	PCIe PHY	X	Open	—	—	—	—	—
PCVDD08	—	0.8	PCIe PHY 0.8-V power supply	—	—	—	—	—	—	—
PCVDD18	—	1.8	PCIe PHY 1.8-V power supply	—	—	—	—	—	—	—
PCRSTOUTB	O	3.3	PCIe I/O	H	Open	—	OFF	—	Selectable*2	—
USDP	IO	3.3	USB PHY	L	Open	—	-	—	—	—
USDM	IO	3.3	USB PHY	L	Open	—	-	—	—	—
USRESREF	I	0.25	USB RESREF	—	Open	—	—	—	—	—
USVD330	—	3.3	USB PHY HS section 3.3-V power supply	—	—	—	—	—	—	—
USVDDH	—	1.8	USB PHY HS section 1.8-V power supply	—	—	—	—	—	—	—
USDVDD*4	—	0.8	USB PHY HS section 0.8-V power supply	—	—	—	—	—	—	—
USVBUS	I	3.3	USB PHY	Hi-Z	Open	—	—	—	—	—
USRX0M	I	0.8	USB PHY	—	Open	—	—	—	—	—
USRX0P	I	0.8	USB PHY	—	Open	—	—	—	—	—

Table 2.2-1 List of External Pins (16/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
USTX0M	O	0.8	USB PHY	—	Open	—	—	—	—	—
USTX0P	O	0.8	USB PHY	—	Open	—	—	—	—	—
USOTGID	I	1.8	USB PHY	—	Open	—	—	—	—	—
USVP	—	0.8	USB PHY SS section 0.8-V power supply	—	—	—	—	—	—	—
USVPH	—	3.3	USB PHY SS section 3.3-V power supply	—	—	—	—	—	—	—
USVPTX	—	0.8	USB PHY SS section transmitter power supply	—	—	—	—	—	—	—
USPWEN	O	3.3	USB I/O	L	Open	—	OFF	—	Selectable*2	—
USOVC	I	3.3	USB I/O	Hi-Z	Pull up	—	OFF	—	—	—
HDTXCP	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTXCM	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTX0P	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTX0M	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTX1P	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTX1M	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTX2P	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDTX2M	O	1.8	HDMI PHY	Hi-Z	Open	—	—	—	—	—
HDREXT	IO	1.8	HDMI PHY	—	Open	—	—	—	—	—
HDAVDD18	—	1.8	HDMI PHY 1.8-V power supply	—	—	—	—	—	—	—
HDAVDD08	—	0.8	HDMI PHY 0.8-V power supply	—	—	—	—	—	—	—
HDSCL*3	IO	1.8	PORT20 I/O	Hi-Z	Open	●	OFF	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-21**)
HDSDA*3	IO	1.8	PORT20 I/O	Hi-Z	Open	●	OFF	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-21**)
HDHPD*3	IO	1.8	PORT20 I/O	Hi-Z	Open	●	OFF	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-21**)
AD0AIN0	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN1	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN2	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN3	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN4	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN5	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN6	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN7	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN8	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN9	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN10	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AIN11	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD0AVCCA	—	1.8	ADCA 1.8-V power supply	—	—	—	—	—	—	—
AD0AVSSA	—	0	ADCA GND	—	—	—	—	—	—	—
AD1AIN0	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AIN1	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AIN2	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AIN3	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—

Table 2.2-1 List of External Pins (17/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
AD1AIN4	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AIN5	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AIN6	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AIN7	I	1.8	ADCA I/O	—	Pull down	—	—	—	—	—
AD1AVCCA	—	1.8	ADCA 1.8-V power supply	—	—	—	—	—	—	—
AD1AVSSA	—	0	ADCA GND	—	—	—	—	—	—	—
MD0	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	OFF	—	—	—
MD1	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	OFF	—	—	—
MD2	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	OFF	—	—	—
MD3	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	OFF	—	—	—
MD4	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	OFF	—	—	—
MD5	I	1.8	MD7-0 I/O	PD	Always in use	—	PD	—	—	—
MD6	I	1.8	MD7-0 I/O	PD	Always in use	—	PD	—	—	—
MD7	I	1.8	MD7-0 I/O	Hi-Z	Always in use	—	OFF	—	—	—
MD8*5	IO	3.3/1.8	PORT21 I/O	Hi-Z	Always in use	—	OFF	—	Selectable*2	Multiplexed pin (see **Table 2.2-2** and **Table 2.2-22**)
OTVDD18	—	1.8	OTP 1.8-V power supply	—	—	—	—	—	—	—
OTVDD08	—	0.8	OTP 0.8-V power supply	—	—	—	—	—	—	—
TS0AVDD18	—	1.8	TSU ch. 0 1.8-V power supply	—	—	—	—	—	—	—
TS0DVDD08A	—	0.8	TSU ch. 0 0.8-V power supply	—	—	—	—	—	—	—
TS1AVDD18	—	1.8	TSU ch. 1 1.8-V power supply	—	—	—	—	—	—	—
TS1DVDD08A	—	0.8	TSU ch. 1 0.8-V power supply	—	—	—	—	—	—	—
XIN	I	1.8	1.8-V OSC	CLOCK	Always in use	—	—	—	—	—
XOUT	O	1.8	1.8-V OSC	CLOCK	Always in use	—	—	—	—	—
RSTN	I	1.8	RSTN I/O	PU	Always in use	●	PU	—	—	—
PLVDD1	—	1.8	PLL ch. 1 1.8-V power supply	—	—	—	—	—	—	—
PLVSS1	—	0	PLL ch. 1 GND	—	—	—	—	—	—	—
PLVDD2	—	1.8	PLL ch. 2 1.8-V power supply	—	—	—	—	—	—	—
PLVSS2	—	0	PLL ch. 2 GND	—	—	—	—	—	—	—
PLVDD3	—	1.8	PLL ch. 3 1.8-V power supply	—	—	—	—	—	—	—
PLVSS3	—	0	PLL ch. 3 GND	—	—	—	—	—	—	—
PLVDD4	—	1.8	PLL ch. 4 1.8-V power supply	—	—	—	—	—	—	—
PLVSS4	—	0	PLL ch. 4 GND	—	—	—	—	—	—	—
PLVDD6	—	1.8	PLL ch. 6 1.8-V power supply	—	—	—	—	—	—	—

Table 2.2-1 List of External Pins (18/18)

Pin Name	I/O	Voltage (V)	I/O Group	Initial Value after Power-on Reset	Pin State when not in Use	Input		Output		Multiplexed Pin
						Schmitt Trigger	Pull-up/ Pull-down	N-ch Open-Drain	Drive Strength Selectable/Fixed	
PLVSS6	—	0	PLL ch. 6 GND	—	—	—	—	—	—	—
PLVDD7	—	1.8	PLL ch. 7 1.8-V power supply	—	—	—	—	—	—	—
PLVSS7	—	0	PLL ch. 7 GND	—	—	—	—	—	—	—
PLDVDD081	—	0.8	PLL ch. 1 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD082	—	0.8	PLL ch. 2 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD083	—	0.8	PLL ch. 3 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD084	—	0.8	PLL ch. 4 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD086	—	0.8	PLL ch. 6 0.8-V power supply	—	—	—	—	—	—	—
PLDVDD087	—	0.8	PLL ch. 7 0.8-V power supply	—	—	—	—	—	—	—
VDD08	—	0.8	VDD08 0.8-V power supply	—	—	—	—	—	—	—
VDD18	—	1.8	VDD18 group I/O power supply (PORT02 I/O, PORT05 I/O, PORT20 I/O, 1.8-V OSC, RSTN I/O, debugger I/O, MD0-7 I/O)	—	—	—	—	—	—	—
VDD33	—	3.3	VDD33 group I/O power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	—	—	—	—	—	—	—
PREDVDD33	—	1.8	VDD33 group pre-driver power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	—	—	—	—	—	—	—
GND	—	0	GND	—	—	—	—	—	—	—

Note 1. For 3.3-V input tolerant

Note 2. For the drive strength, see **Section 54.4.2, Standard I/O Characteristics**.

Note 3. These multiplexed pins are for use with the ISP support package, so do not change the multiplexed functional blocks.

Note 4. Connect an external resistor (1.1kΩ). For details, refer to *the RZ/V2M High-Speed Interface PCB Design Guidelines*.

Note 5. This pin is intended to be used for LED control during boot sequence. Therefore, do not use this pin for any other purpose.

Usage Note

In this LSI, supply power to all power pins.

It is necessary to supply power even if the power pin is an unused function and to connect the ground pin to the ground.

2.2.2 List of Multiplexed Functional Blocks

Table 2.2-2 List of Multiplexed Functional Blocks

I/O Group	Share Group 0	Share Group 1	Share Group 2	Share Group 3	Share Group 4	Share Group 5	Share Group 6	Share Group 7
PORT00	GPIO	NAND	eMMC	—	—	—	—	—
PORT01*1	GPIO	PWM	Ex. interrupt	Timer/ CLK out	—	—	—	ESI
PORT02*1	GPIO	—	Ex. interrupt	—	—	—	—	—
PORT03*1	GPIO	CSI0 CSI1 CSI2 CSI3	UART0 UART1 IIC2 IIC3 CSI3	CSI0 CSI1 CSI2	TRACE	—	—	ESI
PORT04*1	GPIO	CSI4 CSI5	CSI4 CSI5	—	TRACE	—	—	—
PORT05*1	GPIO	—	IIC0 IIC1	—	—	—	—	—
PORT06*1	GPIO	—	—	—	—	—	—	—
PORT07*1	GPIO	I2S	—	—	—	—	—	—
PORT08	GPIO	SDI0	—	—	—	—	—	—
PORT09	GPIO	SDI1	Ex. interrupt	—	—	—	—	—
PORT10*1	GPIO	STG0	Ex. interrupt	—	—	—	—	—
PORT11*1	GPIO	STG1	Ex. interrupt	—	—	—	—	—
PORT12*1	GPIO	Mechanical shutter	Ex. interrupt	—	—	—	—	—
PORT13*1	GPIO	—	Ex. interrupt	MTR	—	—	—	—
PORT14*1	GPIO	—	Ex. interrupt	MTR	—	—	—	—
PORT15	GPIO	ETHER	—	—	TRACE	—	—	—
PORT16	GPIO	ETHER	—	MTR	TRACE	—	—	—
PORT17	GPIO	ETHER	—	—	—	—	—	—
PORT20*1	GPIO	HDMI	—	—	—	—	—	—
PORT21	GPIO	—	—	—	—	—	—	—

Note 1. Some or all pins in the same I/O group are used by ISP support package. Therefore, do not change the function of those pins. For details, refer to the following pages.

Table 2.2-3 I/O Group PORT00 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	NAND	eMMC	—	—	—	—	—
NADAT0	P00_00	NADAT0	MMDAT0	—	—	—	—	—
NADAT1	P00_01	NADAT1	MMDAT1	—	—	—	—	—
NADAT2	P00_02	NADAT2	MMDAT2	—	—	—	—	—
NADAT3	P00_03	NADAT3	MMDAT3	—	—	—	—	—
NADAT4	P00_04	NADAT4	MMDAT4	—	—	—	—	—
NADAT5	P00_05	NADAT5	MMDAT5	—	—	—	—	—
NADAT6	P00_06	NADAT6	MMDAT6	—	—	—	—	—
NADAT7	P00_07	NADAT7	MMDAT7	—	—	—	—	—
NACEN	P00_08	NACEN	—	—	—	—	—	—
NAREN	P00_09	NAREN	—	—	—	—	—	—
NAWEN	P00_10	NAWEN	MMCMD	—	—	—	—	—
NACLE	P00_11	NACLE	MMCLK	—	—	—	—	—
NAALE	P00_12	NAALE	—	—	—	—	—	—
NARBN	P00_13	NARBN	—	—	—	—	—	—

Table 2.2-4 I/O Group PORT01 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	PWM	Ex. interrupt	Timer/ CLK out	—	—	—	ESI
PM0*1	P01_00	PM0	INEXINT8	—	—	—	—	—
PM1*1	P01_01	PM1	INEXINT9	—	—	—	—	—
PM2*1	P01_02	PM2	INEXINT10	—	—	—	—	—
PM3*1	P01_03	PM3	INEXINT11	—	—	—	—	—
PM4*1	P01_04	PM4	INEXINT12	—	—	—	—	SDTCS1
PM5*1	P01_05	PM5	INEXINT13	GFPLS0	—	—	—	SDTCS2
PM6*1	P01_06	PM6	INEXINT14	GMCLK0	—	—	—	SDTCS3
PM7*1	P01_07	PM7	INEXINT15	GMCLK1	—	—	—	—
PM8	P01_08	PM8	INEXINT16	—	—	—	—	—
PM9	P01_09	PM9	INEXINT17	—	—	—	—	—
PM10	P01_10	PM10	INEXINT18	—	—	—	—	—
PM11	P01_11	PM11	INEXINT19	—	—	—	—	—
PM12	P01_12	PM12	INEXINT20	—	—	—	—	—
PM13	P01_13	PM13	INEXINT21	GFPLS1	—	—	—	—
PM14	P01_14	PM14	INEXINT22	GMCLK0	—	—	—	—
PM15*1	P01_15	PM15	INEXINT23	GMCLK1	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-5 I/O Group PORT02 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	—	—	—	—	—
INEXINT0*1	P02_00	—	INEXINT0	—	—	—	—	—
INEXINT1*1	P02_01	—	INEXINT1	—	—	—	—	—
INEXINT2*1	P02_02	—	INEXINT2	—	—	—	—	—
INEXINT3*1	P02_03	—	INEXINT3	—	—	—	—	—
INEXINT4	P02_04	—	INEXINT4	—	—	—	—	—
INEXINT5	P02_05	—	INEXINT5	—	—	—	—	—
INEXINT6	P02_06	—	INEXINT6	—	—	—	—	—
INEXINT7	P02_07	—	INEXINT7	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-6 I/O Group PORT03 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	CSI0, CSI1, CSI2, CSI3	UART0, UART1, IIC2, IIC3, CSI3	CSI0, CSI1, CSI2	TRACE	—	—	ESI
CSTXD0	P03_00	CSTXD0	UATX0	CSRXD0	—	—	—	—
CSRXD0	P03_01	CSRXD0	UARX0	—	—	—	—	—
CSSCLK0	P03_02	CSSCLK0	UACTS0N	—	—	—	—	—
CSCS0	P03_03	CSCS0	UARTS0N	—	—	—	—	—
CSTXD1*1	P03_04	CSTXD1	UATX1	CSRXD1	—	—	—	—
CSRXD1*1	P03_05	CSRXD1	UARX1	—	—	—	—	—
CSSCLK1*1	P03_06	CSSCLK1	UACTS1N	—	TRDAT15	—	—	—
CSCS1*1	P03_07	CSCS1	UARTS1N	—	TRDAT14	—	—	—
CSTXD2	P03_08	CSTXD2	I2SDA2	CSRXD2	TRDAT13	—	—	—
CSRXD2	P03_09	CSRXD2	I2SCL2	—	TRDAT12	—	—	—
CSSCLK2*1	P03_10	CSSCLK2	I2SDA3	—	TRDAT11	—	—	—
CSCS2*1	P03_11	CSCS2	I2SCL3	—	TRDAT10	—	—	—
CSTXD3*1	P03_12	CSTXD3	CSRXD3	—	TRDAT9	—	—	SDTTXD
CSRXD3*1	P03_13	CSRXD3	—	—	TRDAT8	—	—	SDTRXD
CSSCLK3*1	P03_14	CSSCLK3	—	—	TRDAT7	—	—	SDTSCLK
CSCS3*1	P03_15	CSCS3	—	—	TRDAT6	—	—	SDTCS0

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-7 I/O Group PORT04 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	CSI4, CSI5	CSI4, CSI5	—	TRACE	—	—	—
CSTXD4	P04_00	CSTXD4	CSRXD4	—	TRDAT5	—	—	—
CSRXD4	P04_01	CSRXD4	—	—	TRDAT4	—	—	—
CSSCLK4	P04_02	CSSCLK4	—	—	TRDAT3	—	—	—
CSCS4	P04_03	CSCS4	—	—	TRDAT2	—	—	—
CSTXD5*1	P04_04	CSTXD5	CSRXD5	—	TRDAT1	—	—	—
CSRXD5*1	P04_05	CSRXD5	—	—	TRDAT0	—	—	—
CSSCLK5*1	P04_06	CSSCLK5	—	—	TRCLK	—	—	—
CSCS5*1	P04_07	CSCS5	—	—	TRCTL	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-8 I/O Group PORT05 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	IIC0, IIC1	—	—	—	—	—
I2SDA0	P05_00	—	I2SDA0	—	—	—	—	—
I2SCL0	P05_01	—	I2SCL0	—	—	—	—	—
I2SDA1*1	P05_02	—	I2SDA1	—	—	—	—	—
I2SCL1*1	P05_03	—	I2SCL1	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-9 I/O Group PORT06 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	—	—	—	—	—	—
P0600*1	P06_00	—	—	—	—	—	—	—
P0601*1	P06_01	—	—	—	—	—	—	—
P0602*1	P06_02	—	—	—	—	—	—	—
P0603*1	P06_03	—	—	—	—	—	—	—
P0604*1	P06_04	—	—	—	—	—	—	—
P0605*1	P06_05	—	—	—	—	—	—	—
P0606*1	P06_06	—	—	—	—	—	—	—
P0607*1	P06_07	—	—	—	—	—	—	—
P0608	P06_08	—	—	—	—	—	—	—
P0609	P06_09	—	—	—	—	—	—	—
P0610	P06_10	—	—	—	—	—	—	—
P0611	P06_11	—	—	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-10 I/O Group PORT07 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	AUI	—	—	—	—	—	—
AULRCK*1	P07_00	AULRCK	—	—	—	—	—	—
AUBICK*1	P07_01	AUBICK	—	—	—	—	—	—
AUDI*1	P07_02	AUDI	—	—	—	—	—	—
AUDO*1	P07_03	AUDO	—	—	—	—	—	—
AUMCLK*1	P07_04	AUMCLK	—	—	—	—	—	—
AUPLLCLK*1	P07_05	AUPLLCLK	—	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-11 I/O Group PORT08 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	SDI0	—	—	—	—	—	—
SD0CMD	P08_00	SD0CMD	—	—	—	—	—	—
SD0CLK	P08_01	SD0CLK	—	—	—	—	—	—
SD0DAT0	P08_02	SD0DAT0	—	—	—	—	—	—
SD0DAT1	P08_03	SD0DAT1	—	—	—	—	—	—
SD0DAT2	P08_04	SD0DAT2	—	—	—	—	—	—
SD0DAT3	P08_05	SD0DAT3	—	—	—	—	—	—
SD0WP	P08_06	SD0WP	—	—	—	—	—	—
SD0CD	P08_07	SD0CD	—	—	—	—	—	—

Table 2.2-12 I/O Group PORT09 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	SDI1	Ex. interrupt	—	—	—	—	—
SD1FCMD	P09_00	SD1FCMD	—	—	—	—	—	—
SD1FCLK	P09_01	SD1FCLK	—	—	—	—	—	—
SD1FDAT0	P09_02	SD1FDAT0	—	—	—	—	—	—
SD1FDAT1	P09_03	SD1FDAT1	—	—	—	—	—	—
SD1FDAT2	P09_04	SD1FDAT2	—	—	—	—	—	—
SD1FDAT3	P09_05	SD1FDAT3	—	—	—	—	—	—
SD1FWP	P09_06	SD1FWP	INEXINT24	—	—	—	—	—
SD1FCD	P09_07	SD1FCD	INEXINT25	—	—	—	—	—

Table 2.2-13 I/O Group PORT10 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	STG0	Ex. interrupt	—	—	—	—	—
IM0VS*1	P10_00	IM0VS	—	—	—	—	—	—
IM0HS*1	P10_01	IM0HS	—	—	—	—	—	—
IM0CS*1	P10_02	IM0CS	—	—	—	—	—	—
IM0TXD*1	P10_03	IM0TXD	—	—	—	—	—	—
IM0RXD*1	P10_04	IM0RXD	—	—	—	—	—	—
IM0SCLK*1	P10_05	IM0SCLK	—	—	—	—	—	—
IM0SIG0*1	P10_06	IM0SIG0	INEXINT26	—	—	—	—	—
IM0SIG1*1	P10_07	IM0SIG1	INEXINT27	—	—	—	—	—
IM0SIG2*1	P10_08	IM0SIG2	—	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-14 I/O Group PORT11 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	STG1	Ex. interrupt	—	—	—	—	—
IM1VS*1	P11_00	IM1VS	—	—	—	—	—	—
IM1HS*1	P11_01	IM1HS	—	—	—	—	—	—
IM1CS*1	P11_02	IM1CS	—	—	—	—	—	—
IM1TXD*1	P11_03	IM1TXD	—	—	—	—	—	—
IM1RXD*1	P11_04	IM1RXD	—	—	—	—	—	—
IM1SCLK*1	P11_05	IM1SCLK	—	—	—	—	—	—
IM1SIG0*1	P11_06	IM1SIG0	INEXINT28	—	—	—	—	—
IM1SIG1*1	P11_07	IM1SIG1	INEXINT29	—	—	—	—	—
IM1SIG2*1	P11_08	IM1SIG2	—	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-15 I/O Group PORT12 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	STG1	Ex. interrupt	—	—	—	—	—
IMSHUT0*1	P12_00	IMSHUT0	INEXINT30	—	—	—	—	—
IMSHUT1*1	P12_01	IMSHUT1	INEXINT31	—	—	—	—	—
IMSTSIG0*1	P12_02	IMSTSIG0	INEXINT32	—	—	—	—	—
IMSTSIG1*1	P12_03	IMSTSIG1	INEXINT33	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-16 I/O Group PORT13 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	MTR	—	—	—	—
MTDRV0*1	P13_00	—	—	MTDRV0	—	—	—	—
MTDRV1*1	P13_01	—	—	MTDRV1	—	—	—	—
MTDRV2*1	P13_02	—	—	MTDRV2	—	—	—	—
MTDRV3*1	P13_03	—	—	MTDRV3	—	—	—	—
MTDRV4*1	P13_04	—	—	MTDRV4	—	—	—	—
MTDRV5*1	P13_05	—	—	MTDRV5	—	—	—	—
MTDRV6*1	P13_06	—	—	MTDRV6	—	—	—	—
MTDRV7*1	P13_07	—	—	MTDRV7	—	—	—	—
MTDCPLS0*1	P13_08	—	—	MTDCPLS0	—	—	—	—
MTDCPLS1*1	P13_09	—	INEXINT34	MTDCPLS1	—	—	—	—
MTDCPLS2*1	P13_10	—	INEXINT35	MTDCPLS2	—	—	—	—
MTDCPLS3*1	P13_11	—	INEXINT36	MTDCPLS3	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-17 I/O Group PORT14 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	Ex. interrupt	MTR	—	—	—	—
MTCS0*1	P14_00	—	—	MTCS0	—	—	—	—
MTTXD0*1	P14_01	—	—	MTTXD0	—	—	—	—
MTRXD0*1	P14_02	—	INEXINT37	MTRXD0	—	—	—	—
MTSCLK0*1	P14_03	—	—	MTSCLK0	—	—	—	—
MTCS1*1	P14_04	—	—	MTCS1	—	—	—	—
MTTXD1*1	P14_05	—	—	MTTXD1	—	—	—	—
MTRXD1*1	P14_06	—	INEXINT38	MTRXD1	—	—	—	—
MTSCLK1*1	P14_07	—	—	MTSCLK1	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-18 I/O Group PORT15 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	ETHER	—	—	TRACE	—	—	—
GETXC	P15_00	GETXC	—	—	TRCLK	—	—	—
GETXEN	P15_01	GETXEN	—	—	TRCTL	—	—	—
GETXER	P15_02	GETXER	—	—	—	—	—	—
GETXD0	P15_03	GETXD0	—	—	—	—	—	—
GETXD1	P15_04	GETXD1	—	—	—	—	—	—
GETXD2	P15_05	GETXD2	—	—	—	—	—	—
GETXD3	P15_06	GETXD3	—	—	—	—	—	—
GETXD4	P15_07	GETXD4	—	—	—	—	—	—
GETXD5	P15_08	GETXD5	—	—	TRDAT0	—	—	—
GETXD6	P15_09	GETXD6	—	—	TRDAT1	—	—	—
GETXD7	P15_10	GETXD7	—	—	TRDAT2	—	—	—
GERXC	P15_11	GERXC	—	—	TRDAT3	—	—	—
GERXDV	P15_12	GERXDV	—	—	TRDAT4	—	—	—
GERXER	P15_13	GERXER	—	—	TRDAT5	—	—	—
GERXD0	P15_14	GERXD0	—	—	TRDAT6	—	—	—
GERXD1	P15_15	GERXD1	—	—	TRDAT7	—	—	—

Table 2.2-19 I/O Group PORT16 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	ETHER	—	MTR	TRACE	—	—	—
GERXD2	P16_00	GERXD2	—	MTDRV8	TRDAT8	—	—	—
GERXD3	P16_01	GERXD3	—	MTDRV9	TRDAT9	—	—	—
GERXD4	P16_02	GERXD4	—	MTDRV10	TRDAT10	—	—	—
GERXD5	P16_03	GERXD5	—	MTDRV11	TRDAT11	—	—	—
GERXD6	P16_04	GERXD6	—	MTDRV12	TRDAT12	—	—	—
GERXD7	P16_05	GERXD7	—	MTDRV13	TRDAT13	—	—	—
GECRS	P16_06	GECRS	—	MTDRV14	TRDAT14	—	—	—
GECOL	P16_07	GECOL	—	MTDRV15	TRDAT15	—	—	—
GEMDC	P16_08	GEMDC	—	—	—	—	—	—
GEMDIO	P16_09	GEMDIO	—	—	—	—	—	—
GEGTXCLK	P16_10	GEGTXCLK	—	—	—	—	—	—
GELINK	P16_11	GELINK	—	—	—	—	—	—
GEINT	P16_12	GEINT	—	—	—	—	—	—
GECLK	P16_13	GECLK	—	—	—	—	—	—

Table 2.2-20 I/O Group PORT17 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	ETHER	—	—	—	—	—	—
GEPPS	P17_00	GEPPS	—	—	—	—	—	—

Table 2.2-21 I/O Group PORT20 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	HDMI	—	—	—	—	—	—
HDSCL*1	P20_00	HDSCL	—	—	—	—	—	—
HDSDA*1	P20_01	HDSDA	—	—	—	—	—	—
HDHPD*1	P20_02	HDHPD	—	—	—	—	—	—

Note 1. This multiplexed pin is used by the ISP support package. Therefore, do not change the multiplexed mode.

Table 2.2-22 I/O Group PORT21 in the Multiplexed Mode

External Pin Name	Share Pin Name 0	Share Pin Name 1	Share Pin Name 2	Share Pin Name 3	Share Pin Name 4	Share Pin Name 5	Share Pin Name 6	Share Pin Name 7
	GPIO	—	—	—	—	—	—	—
MD8*1	P21_00	—	—	—	—	—	—	—

Note 1. This pin is intended to be used for LED control during boot sequence. Therefore, do not use this pin for any other purpose.

2.3 Pin Functions of Functional Blocks

Table 2.3-1 List of Pin Functions (1/7)

Classification	Pin Name	I/O	Function
Real time clock (RTC)	RTXIN	I	To connect a 32.768-kHz crystal resonator
	RTXOUT	O	To connect a 32.768-kHz crystal resonator
	RTRSTN	I	RTC reset input (active low)
	RTISO	I	RTC isolation input pin
Power control (PWC)	PWRSTN	I	PWC reset input (active low)
	PWTEST	I	LSI test pin, fixed to the low level
	PWVBAT	I	Battery voltage detection
	PWKY2N to PWKY0N	I	Input power key 2 to 0 (active low)
	PWKY4N, PWKY3N	I	Input power key 4, 3
	PWDETRSTN	I	Reserved, pulled up by a 1.8-V power supply
	PWEN5 to PWEN0	O	Power enable 5 to 0 (active high)
	PWSYSRSTN	O	System reset output, connected to the RSTN pin to use the power control function of PWC
	PWOUT1, PWOUT0	O	Reserved, leave these pins open-circuit
	PWPWM	O	Reserved, leave this pin open-circuit
	PWSD0SEL	O	PWC SDI0 interface power supply selection
	PWSD1SEL	O	PWC SDI1 interface power supply selection
	PWCTEST0	O	LSI test pin: leave this pin open-circuit
	PWCTEST1	I	LSI test pin: fixed to the high level (pulled up by the PWVDD)
	PWMEMSWIENA	O	Enable signal output pin for controlling the LPVDD power supply on/off
	PWISO	O	RTC separation output pin. Open drain output. Connected to the RTISO pin and pulled up (with 10kΩ to 100kΩ) to a 1.5-V power supply.*1
NAND flash interface (NAND)	NADAT7 to NADAT0	I/O	NAND flash I/O data [7:0]
	NACEN	O	NAND flash chip enable (active low)
	NAREN	O	NAND flash read enable (active low)
	NAWEN	O	NAND flash write enable (active low)
	NACLE	O	NAND flash command latch enable
	NAALE	O	NAND flash address latch enable
	NARBN	I	NAND flash ready/busy input
	NAWPN	O	NAND flash write protect
eMMC interface (eMMC)	MMDAT7 to MMDAT0	I/O	eMMC data [7:0]
	MMCMD	I/O	eMMC command
	MMCLK	O	eMMC clock
Pulse-width modulation timer (PWM)	PM15 to PM0	O	PWM output
External interrupt	INEXINT38 to INEXINT0	I	External interrupt

Table 2.3-1 List of Pin Functions (2/7)

Classification	Pin Name	I/O	Function
CSI ch. 0 (CSI0)	CSTXD0	O	CSI0 serial data output
	CSRXD0	I	CSI0 serial data input
	CSSCLK0	I/O	CSI0 serial clock
	CSCS0	I	CSI0 serial chip select
CSI ch. 1 (CSI1)	CSTXD1	O	CSI1 serial data output
	CSRXD1	I	CSI1 serial data input
	CSSCLK1	I/O	CSI1 serial clock
	CSCS1	I	CSI1 serial chip select
CSI ch. 2 (CSI2)	CSTXD2	O	CSI2 serial data output
	CSRXD2	I	CSI2 serial data input
	CSSCLK2	I/O	CSI2 serial clock
	CSCS2	I	CSI2 serial chip select
CSI ch. 3 (CSI3)	CSTXD3	O	CSI3 serial data output
	CSRXD3	I	CSI3 serial data input
	CSSCLK3	I/O	CSI3 serial clock
	CSCS3	I	CSI3 serial chip select
CSI ch. 4 (CSI4)	CSTXD4	O	CSI4 serial data output
	CSRXD4	I	CSI4 serial data input
	CSSCLK4	I/O	CSI4 serial clock
	CSCS4	I	CSI4 serial chip select
CSI ch. 5 (CSI5)	CSTXD5	O	CSI5 serial data output
	CSRXD5	I	CSI5 serial data input
	CSSCLK5	I/O	CSI5 serial clock
	CSCS5	I	CSI5 serial chip select
IIC ch. 0 (IIC0)	I2SDA0	I/O	IIC0 serial data
	I2SCL0	I/O	IIC0 serial clock
IIC ch. 1 (IIC1)	I2SDA1	I/O	IIC1 serial data
	I2SCL1	I/O	IIC1 serial clock
IIC ch. 2 (IIC2)	I2SDA2	I/O	IIC2 serial data
	I2SCL2	I/O	IIC2 serial clock
IIC ch. 3 (IIC3)	I2SDA3	I/O	IIC3 serial data
	I2SCL3	I/O	IIC3 serial clock
UART ch. 0 (UART0)	UATX0	O	UART0 transmission data
	UARX0	I	UART0 reception data
	UACTS0N	I	UART0 transmission enable signal (active low)
	UARTS0N	O	UART0 reception enable signal (active low)
UART ch. 1 (UART1)	UATX1	O	UART1 transmission data
	UARX1	I	UART1 reception data
	UACTS1N	I	UART1 transmission enable signal (active low)
	UARTS1N	O	UART1 reception enable signal (active low)

Table 2.3-1 List of Pin Functions (3/7)

Classification	Pin Name	I/O	Function
Audio interface (AUI)	AULRCK	I	Audio channel clock
	AUBICK	I	Audio serial clock
	AUDI	I	Audio serial data input
	AUDO	O	Audio serial data output
	AUMCLK	O	Audio master clock output
	AUPLLCLK	I	Audio master clock input
SD host interface ch. 0 (SDI0)	SD0CMD	I/O	SDI0 command/response signal
	SD0CLK	O	SDI0 clock
	SD0DAT3 to SD0DAT0	I/O	SDI0 data line bits [3:0]
	SD0WP	I	SDI0 write protect signal
	SD0CD	I	SDI0 card detection signal
SD host interface ch. 1 (SDI1)	SD1FCMD	I/O	SDI1 command/response signal
	SD1FCLK	O	SDI1 clock
	SD1FDAT3 to SD1FDAT0	I/O	SDI1 data line bits [3:0]
	SD1FWP	I	SDI1 write protect signal
	SD1FCD	I	SDI1 card detection signal
Image sensor timing generator ch. 0 (STG0)	IM0VS	I/O	Image sensor 0 vertical synchronization signal
	IM0HS	I/O	Image sensor 0 horizontal synchronization signal
	IM0CLK	O	Image sensor 0 clock supply port
	IM0CS	I/O	Image sensor 0 dedicated serial chip select output (or dedicated IIC clock)
	IM0TXD	O	Image sensor 0 dedicated serial transmission data output
	IM0RXD	I/O	Image sensor 0 dedicated serial reception data input (or dedicated IIC data)
	IM0SCLK	O	Image sensor 0 dedicated serial clock output
	IM0SIG2 to IM0SIG0	O	Image sensor 0 control pulse output
Image sensor timing generator ch. 1 (STG1)	IM1VS	I/O	Image sensor 1 vertical synchronization signal
	IM1HS	I/O	Image sensor 1 horizontal synchronization signal
	IM1CLK	O	Image sensor 1 clock supply port
	IM1CS	I/O	Image sensor 1 dedicated serial chip select output (or dedicated IIC clock)
	IM1TXD	O	Image sensor 1 dedicated serial transmission data output
	IM1RXD	I/O	Image sensor 1 dedicated serial reception data input (or dedicated IIC data)
	IM1SCLK	O	Image sensor 1 dedicated serial clock output
	IM1SIG2 to IM1SIG0	O	Image sensor 1 control pulse output
Mechanical shutter	IMSHUT0	O	Mechanical shutter control pin 0
	IMSHUT1	O	Mechanical shutter control pin 1
	IMSTSIG0	O	External flash control pin 0
	IMSTSIG1	O	External flash control pin 1

Table 2.3-1 List of Pin Functions (4/7)

Classification	Pin Name	I/O	Function
Motor controller (MTR)	MTDRV15 to MTDRV0	O	Motor drive signal
	MTDCPLS3 to MTDCPLS0	I	Reserved, leave these pins open-circuit
	MTCS0	O	Motor 0 serial chip select
	MTTXD0	O	Motor 0 serial transmission data
	MTRXD0	I	Motor 0 serial reception data
	MTSCLK0	O	Motor 0 serial clock
	MTCS1	O	Motor 1 serial chip select
	MTTXD1	O	Motor 1 serial transmission data
	MTRXD1	I	Motor 1 serial reception data
	MTSCLK1	O	Motor 1 serial clock
Gigabit Ethernet MAC interface (ETHER)	GETXC	I	Transmission clock for Ethernet 100-Mbps mode
	GETXEN	O	Transmission enable signal (active high)
	GETXER	O	Transmission error signal (active high)
	GETXD7 to GETXD0	O	Transmission data [7:0]
	GERXC	I	Ethernet reception clock
	GERXDV	I	Reception data valid signal (active high)
	GERXER	I	Reception error signal (active high)
	GERXD7 to GERXD0	I	Receive data [7:0]
	GECRS	I	Carrier detection signal (active high)
	GECOL	I	Transmission collision signal (active high)
	GEMDC	O	PHY management clock
	GEMDIO	I/O	PHY management I/O data
	GEGTXCLK	O	GMII transmission clock
	GELINK	I	PHY LINK signal
	GEINT	I	PHY interrupt signal
	GECLK*2	I	Clock input
	GEPPS	O	AVTP PPS (pulse per second) signal
Debugger interface	DETCK	I	JTAG TCK
	DETDI	I	JTAG TDI
	DETDO	O	JTAG TDO
	DETMS	I/O	JTAG TMS
	DETRSTN	I	JTAG TRST (active low)
	DESRSTN	I	System reset from debugger (active low)
For LSI test	RETEST0	I	LSI test enable, fixed to the low level
	RETEST1	I	LSI test enable, fixed to the low level

Table 2.3-1 List of Pin Functions (5/7)

Classification	Pin Name	I/O	Function
LPDDR4 interface	LPATEST	O	LSI test pin, leave this pin open-circuit
	LPCAA5 to LPCAA0	O	DRAM address and command bits: Ch-A command/address input
	LPCAB5 to LPCAB0	O	DRAM address and command bits: Ch-B command/address input
	LPCKEA1, LPCKEA0	O	DRAM address and command bits: Ch-A clock enable
	LPCKEB1, LPCKEB0	O	DRAM address and command bits: Ch-B clock enable
	LPCLKAC	O	DRAM address and command bits: Ch-A clock (negative)
	LPCLKAT	O	DRAM address and command bits: Ch-A clock (positive)
	LPCLKBC	O	DRAM address and command bits: Ch-B clock (negative)
	LPCLKBT	O	DRAM address and command bits: Ch-B clock (positive)
	LPCSA1, LPCSA0	O	DRAM address and command bits: Ch-A chip select
	LPCSB1, LPCSB0	O	DRAM address and command bits: Ch-B chip select
	LPDMDBIA1, LPDMDBIA0	I/O	DRAM data bits and strobes: Ch-A data mask inversion
	LPDMDBIB1, LPDMDBIB0	I/O	DRAM data bits and strobes: Ch-B data mask inversion
	LPDQA15 to LPDQA0	I/O	DRAM data bits and strobes: Ch-A data input/output
	LPDQB15 to LPDQB0	I/O	DRAM data bits and strobes: Ch-B data input/output
	LPDQSAC1, LPDQSAC0	I/O	DRAM data bits and strobes: Ch-A data strobe (negative)
	LPDQSAT1, LPDQSAT0	I/O	DRAM data bits and strobes: Ch-A data strobe (positive)
	LPDQSBC1, LPDQSBC0	I/O	DRAM data bits and strobes: Ch-B data strobe (negative)
	LPDQSBT1, LPDQSBT0	I/O	DRAM data bits and strobes: Ch-B data strobe (positive)
	LPMRESETL	O	DRAM reset. Note that this requires no external resistor.
	LPZN	O	External reference resistor connection pin for use in calibration. * To connect a pull-down resistor. Resistance: 240Ω±1%
	LPDTEST	O	LSI test pin, leave this pin open-circuit
MIPI CSI-2	LVRXREXT	I	External reference resistor connection pin * Resistance: 10kΩ ±1%
MIPI CSI-2 interface	MPRXD7P to MPRXD0P	I	MIPI CSI-2 differential serial data 7 to 0 (positive)
	MPRXD7M to MPRXD0M	I	MIPI CSI-2 differential serial data 7 to 0 (negative)
	MPRXCK1P, MPRXCK0P	I	MIPI CSI-2 differential serial clocks 1, 0 (positive)
	MPRXCK1M, MPRXCK0M	I	MIPI CSI-2 differential serial clocks 1, 0 (negative)
MIPI DSI Tx interface	DSMDPDATA3 to DSMDPDATA0	I/O	MIPI DSI Tx differential data lanes 3 to 0 (positive)
	DSMDNDATA3 to DSMDNDATA0	I/O	MIPI DSI Tx differential data lanes 3 to 0 (negative)
	DSMDPCLK	I/O	MIPI DSI Tx differential clock (positive)
	DSMDNCLK	I/O	MIPI DSI Tx differential clock (negative)
	DSMVREG0P4V	I/O	External capacitor connection pin for internal regulator * Connect the pin to GND via the capacitance. Recommended capacitance: 2.2 nF
	DSSDPCLK	I/O	LSI test pin, fixed to the low level
	DSSDNCLK	I/O	LSI test pin, fixed to the low level
	DSSDPDATA0	I/O	LSI test pin, fixed to the low level
	DSSDNDATA0	I/O	LSI test pin, fixed to the low level

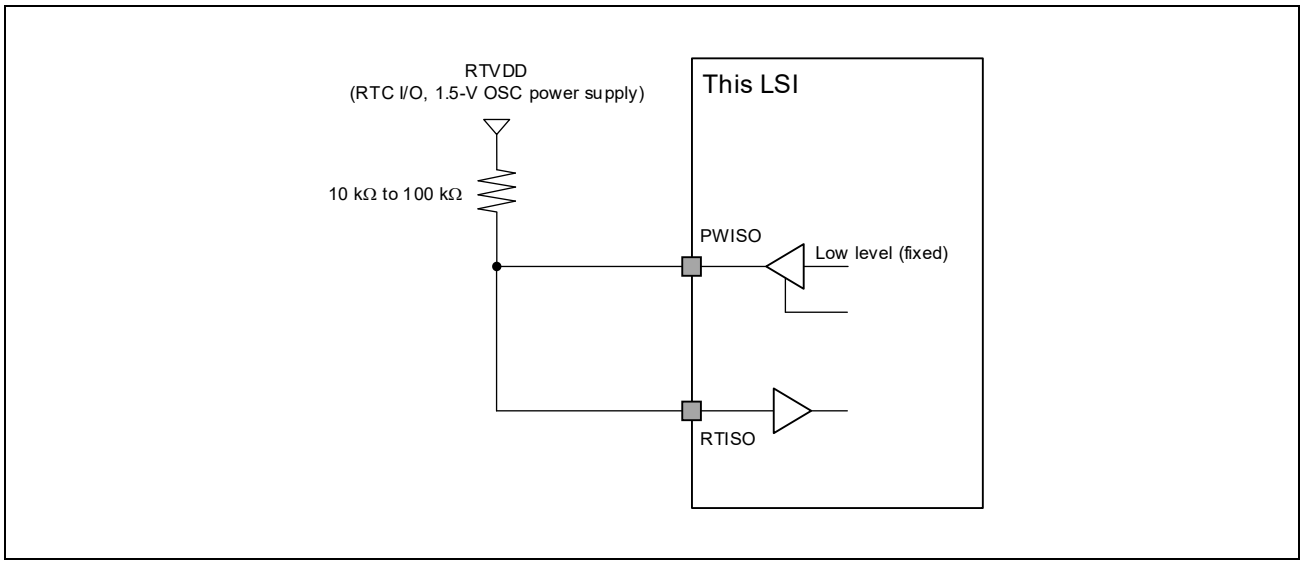
Table 2.3-1 List of Pin Functions (6/7)

Classification	Pin Name	I/O	Function
PCI Express interface	PCRXD1P, PCRXD0P	I	Rx serial data inputs 1, 0 (positive)
	PCRXD1M, PCRXD0M	I	Rx serial data inputs 1, 0 (negative)
	PCTXD1P, PCTXD0P	O	Tx serial data outputs 1, 0 (positive)
	PCTXD1M, PCTXD0M	O	Tx serial data outputs 1, 0 (negative)
	PCREFCKP	I	Differential reference clock (positive)
	PCREFCKM	I	Differential reference clock (negative)
	PCREXT	I	Reference resistor connection pin for band-gap reference (BGR) and bias generator * To connect a pull-down resistor. Resistance: 8.2kΩ ±1%
	PCRSTOUTB	O	Reset output (for other-party PCIe devices) (active low)
USB interface	USDP	I/O	USB2.0 USB D+ signal (positive)
	USDM	I/O	USB2.0 USB D− signal (negative)
	USRESREF	I	Reference resistor connection pin * To connect a pull-down resistor. Resistance: 200Ω ±1%
	USVBUS	I	USB 5-V signal detection pin * Resistance partial pressure outside the chip*3
	USRX0M	I	USB3.1 super-speed differential reception pair (negative)
	USRX0P	I	USB3.1 super-speed differential reception pair (positive)
	USTX0M	O	USB3.1 super-speed differential transmission pair (negative)
	USTX0P	O	USB3.1 super-speed differential transmission pair (positive)
	USOTGID	I	ID detection (OTG ID input, 0: Host, 1: Peripheral)
	USPWEN	O	VBUS control signal (active high)
	USOVC	I	Overcurrent detection (active low)
HDMI Tx interface (HDMI)	HDTXCP	O	TXPHY clock output (positive)
	HDTXCM	O	TXPHY clock output (negative)
	HDTX0P	O	Data channel 0 TXPHY output (positive)
	HDTX0M	O	Data channel 0 TXPHY output (negative)
	HDTX1P	O	Data channel 1 TXPHY output (positive)
	HDTX1M	O	Data channel 1 TXPHY output (negative)
	HDTX2P	O	Data channel 2 TXPHY output (positive)
	HDTX2M	O	Data channel 2 TXPHY output (negative)
	HDREXT	I/O	External reference resistor connection pin * To connect a pull-down resistor. Resistance: 8.2kΩ ±1%
	HDSCL	I/O	DDC IIC master SCL
	HDSDA	I/O	DDC IIC master SDA
	HDHPD	I/O	Hot plug detection (active high)
Environment sensor interface (ESI)	SDTTXD	O	ESI serial transmission data
	SDTRXD	I	ESI serial reception data
	SDTSCLK	O	ESI serial clock
	SDTCS3 to SDTCS0	O	ESI serial chip select
ADC unit A (ADCA)	AD0AIN11 to AD0AIN0	I	Analog input signal
ADC unit B (ADCB)	AD1AIN7 to AD1AIN0	I	Analog input signal

Table 2.3-1 List of Pin Functions (7/7)

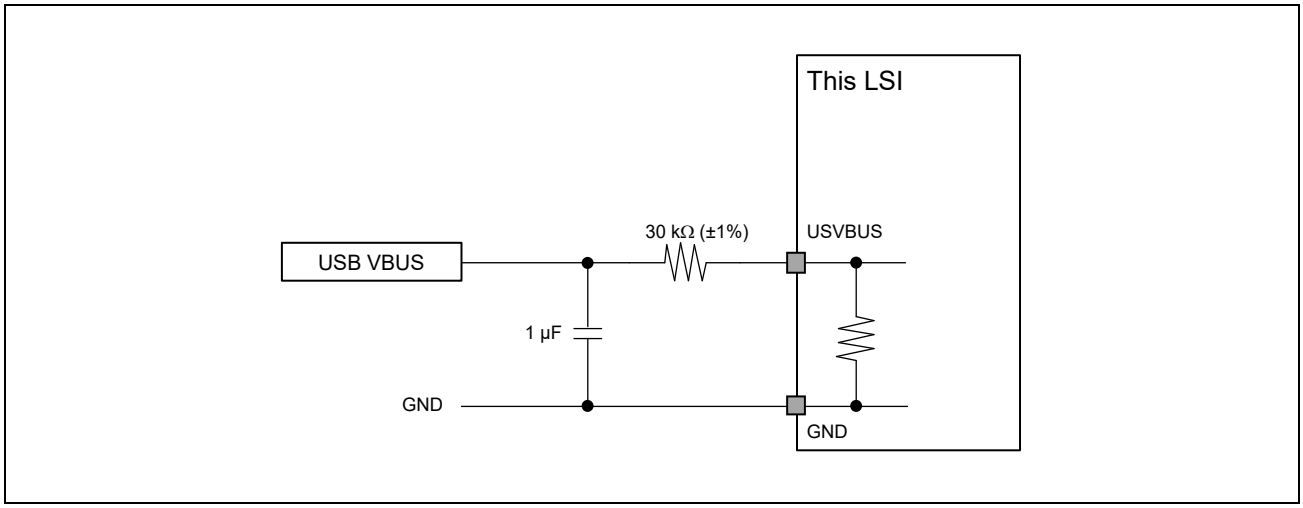
Classification	Pin Name	I/O	Function
Boot	MD2 to MD0	I	Boot device select [2:0]
	MD3	I	Boot device write interface select When not using security, fix the input level to low. When using security, prepare a circuit that is capable of switching the input level externally to low or high (pull up with VDD18).
	MD4	I	Boot mode select [0] (reserved) Fix the pin to the low level.
	MD6, MD5	I	Boot mode select [2:1]
	MD7	I	Boot mode select [3] (reserved) Fix the pin to the low level.
	MD8*4	I/O	Boot GPIO (LED control when booted)*4
Clock/reset	XIN	I	To connect a 48-MHz crystal resonator
	XOUT	O	To connect a 48-MHz crystal resonator
	RSTN	I	System reset (active low)
Timer pulse/ clock output	GFPLS0	I/O	Timer pulse I/O 0
	GFPLS1	I/O	Timer pulse I/O 1
	GMCLK0	O	Clock output 0
	GMCLK1	O	Clock output 1
Trace interface (TRACE)	TRDAT15 to TRDAT0	O	Trace data [15:0]
	TRCLK	O	Trace clock
	TRCTL	O	Trace control
General-purpose input/output ports (GPIO)	P00_13 to P00_00	I/O	GPIO port 00 [13:0]
	P01_15 to P01_00	I/O	GPIO port 01 [15:0]
	P02_07 to P02_00	I/O	GPIO port 02 [7:0]
	P03_15 to P03_00	I/O	GPIO port 03 [15:0]
	P04_07 to P04_00	I/O	GPIO port 04 [7:0]
	P05_03 to P05_00	I/O	GPIO port 05 [3:0]
	P06_11 to P06_00	I/O	GPIO port 06 [11:0]
	P07_05 to P07_00	I/O	GPIO port 07[5:0]
	P08_07 to P08_00	I/O	GPIO port 08[7:0]
	P09_07 to P09_00	I/O	GPIO port 09[7:0]
	P10_08 to P10_00	I/O	GPIO port 10[8:0]
	P11_08 to P11_00	I/O	GPIO port 11[8:0]
	P12_03 to P12_00	I/O	GPIO port 12[3:0]
	P13_11 to P13_00	I/O	GPIO port 13[11:0]
	P14_07 to P14_00	I/O	GPIO port 14[7:0]
	P15_15 to P15_00	I/O	GPIO port 15[15:0]
	P16_13 to P16_00	I/O	GPIO port 16[13:0]
	P17_00	I/O	GPIO port 17[0]
	P20_02 to P20_00	I/O	GPIO port 20[2:0]
	P21_00	I/O	GPIO port 21[0]*4

Note 1. The PWISO and RTISO pins are connected to this LSI, and these nodes should be pulled up with a 10kΩ to 100kΩ resistor. The schematic diagram is shown below.



Note 2. GECLK is the input clock for GEGTXCLK.

Note 3. Since this LSI has a resistor mounted between the USVBUS pin and GND, connect the pin to the USVBUS pin via a 30-kΩ (±1%) resistor. The schematic diagram is shown below.



Note 4. This pin is intended to be used for LED control during boot sequence. Therefore, do not use this pin for any other purpose.

Section 3 Clock

This section describes the clocks of this LSI.

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

3.1 Overview of Clocks

The clocks which are input to and output from this LSI are divided into the following two types.

- External clocks: Clocks which are externally input to this LSI and those which are externally output from this LSI
- Unit clocks: Clocks for use by the internal units of this LSI

3.1.1 External Clocks

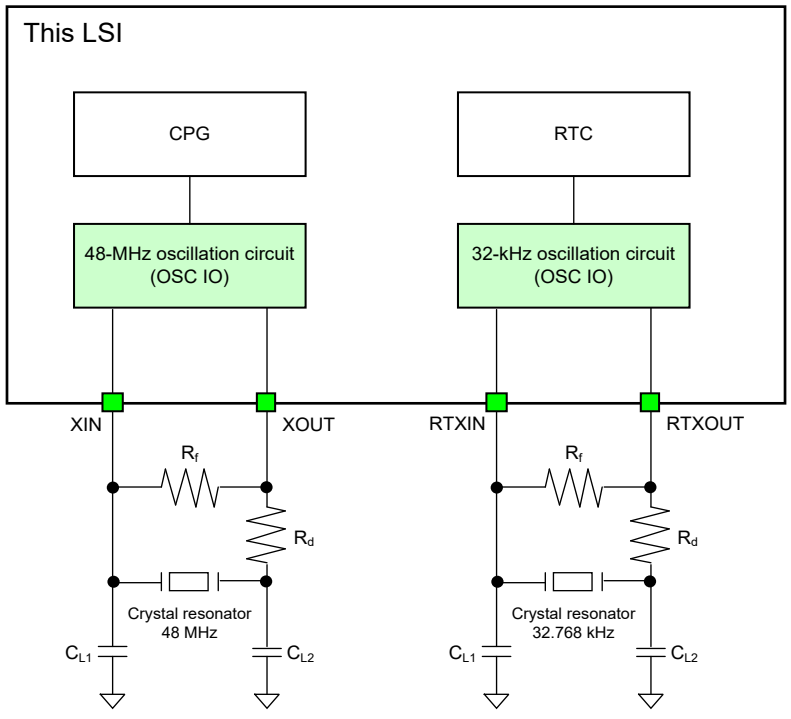
3.1.1.1 Clocks for the Oscillators Circuits (OSC)

This LSI includes two oscillation circuits (OSC) and they are respectively connected to 48 MHz and 32.768 kHz crystals.

Table 3.1-1 lists the clocks for oscillation circuits. **Figure 3.1-1** shows an example connection of this LSI and the crystals.

Table 3.1-1 List of the Clocks for the Oscillation Circuits (OSC)

External Pin Name (Multiplexed Pin Name)	I/O	Function	Frequency
Clocks for the 32.768 kHz OSC			
RTXIN	Input	OSC input clock. Connection of a 32.768-kHz crystal is required.	32.768 kHz
RTXOUT	Output	OSC output clock. Connection of a 32.768-kHz crystal is required.	32.768 kHz
Clocks for the 48 MHz OSC			
XIN	Input	OSC input clock. Connection of a 48-MHz crystal is required.	48 MHz
XOUT	Output	OSC output clock. Connection of a 48-MHz crystal is required.	48 MHz



Note: R_f: Feedback resistor
R_d: Dumping resistor
C_{load} (load capacitance of the crystal): See below for the formula.

$$C_{load} = \{C_{L1} \times C_{L2} / (C_{L1} + C_{L2})\} + \text{PCB's floating capacitance}$$

Figure 3.1-1 Example Connection of This LSI and the Crystals

3.1.1.2 Pin Functions

The clocks for various external interfaces to be connected to this LSI includes clocks which are externally input to this LSI and clocks which are externally output from this LSI. **Table 3.1-2** lists the clocks for external interfaces. The clocks which are externally output from this LSI are generated by the CPG and output via the units of each interface.

Table 3.1-2 List of External Pins (1/2)

Pin Name	I/O	Function	Frequency*1	Supply Source/ Destination Unit
CMOS Image Sensor Interfaces				
CMOS image sensor differential input clocks				
LVRXCK0P*2	—	—	—	CIF
LVRXCK0M*2	—	—	—	CIF
LVRXCK1P*2	—	—	—	CIF
LVRXCK1M*2	—	—	—	CIF
CMOS image sensor output clocks				
IM0CLK*2	—	—	—	STG
IM0SCLK*2	—	—	—	STG
IM1CLK*2	—	—	—	STG
IM1SCLK*2	—	—	—	STG
Control motor serial output clocks				
MTSCLK0*2	—	—	—	MTR
MTSCLK1*2	—	—	—	MTR
Display Interfaces				
MIPI LCD transmission differential output clocks				
DSMDPCLK*2	—	—	—	LCI
DSMDNCLK*2	—	—	—	LCI
HDMI interface output clocks				
HDTXCP*2	—	—	—	HDMI
HDTXCM*2	—	—	—	HDMI
HDSCL*2	—	—	—	HDMI
Audio Interfaces				
Audio interface clocks				
AUPLLCLK*2	—	—	—	AUI
AUBICK*2	—	—	—	AUI, HDMI
AUMCLK*2	—	—	—	CPG
External Memory Interfaces				
LPDDR4 differential output clocks				
LPCLKAT*2	—	—	—	DDI
LPCLKAC*2	—	—	—	DDI
LPCLKBT*2	—	—	—	DDI
LPCLKBC*2	—	—	—	DDI
eMMC interface output clock				
MMCLK*2	—	—	—	eMMC

Table 3.1-2 List of External Pins (2/2)

Pin Name	I/O	Function	Frequency*1	Supply Source/ Destination Unit
Peripheral Interfaces				
SDIO0 interface output clocks				
SD0CLK*2	—	—	—	SDI0
SDIO1 interface output clock				
SD1FCLK*2	—	—	—	SDI1
PCIe reference differential input clocks				
PCREFCKP*2	—	—	—	PCIe
PCREFCKM*2	—	—	—	PCIe
ETHER interface clocks				
GETXC*2	—	—	—	ETHER
GERXC*2	—	—	—	ETHER
GECLK*2	—	—	—	ETHER
GEMDC*2	—	—	—	ETHER
GEGTXCLK*2	—	—	—	ETHER
CSI interface clocks				
CSSCLKn (n: 0 to 5)	Input	CSI data transmission/reception input clock (slave mode)	24 MHz	CSIn (n: 0 to 5)
	Output	CSI data transmission/reception output clock (master mode)	24 MHz	CSIn (n: 0 to 5)
IIC interface clocks				
I2SCLn (n: 0 to 3)	IO	IIC data transmission/reception I/O clock	400 kHz	IICn (n: 0 to 3)
General-purpose output clocks				
GMCLK0	Output	General-purpose output clock 0	100 MHz	CPG
GMCLK1	Output	General-purpose output clock 1	100 MHz	CPG
Sensor device serial output clock				
SDTSCLK*2	—	—	—	ESI
Others				
Trace interface output clock				
TRCLK	Output	Trace interface output clock	50 MHz	CST
Debugger interface input clock				
DETCK	Input	Debugger interface input clock	50 MHz	CST

Note 1. The clock frequencies are either variable or fixed. In the case of the variable clocks, the maximum frequencies which can be output are listed for the output clocks and the maximum frequencies which can be input to this LSI are listed for the input clocks.

Note 2. For more information, contact a Renesas Electronics sales representative.

3.1.2 Unit Clocks

The internal units require three types of unit clock. **Table 3.1-3** gives an overview of the types of unit clock.

Table 3.1-3 Overview of the Types of Unit Clock

Clock Type	Supply Destination Unit	Overview
PLL clock	Other than RTC and PWC	These are high-speed clocks obtained through frequency-multiplication by the internal PLLs. Most of the clocks distributed to the units are also divided by frequency-dividers. These clocks include those generated by different dividers which are switched by selectors and distributed to the units and those generated by the different PLLs which are switched by selectors and distributed to the units.
48-MHz clock	Other than RTC and PWC	The 48-MHz clock which is input externally and signals derived from it by division. That is, these clocks include the 48-MHz-clock itself and those obtained by division by frequency-dividers for distribution and of those, clocks which are switched by selectors for distribution.
32.768-kHz clock	RTC, PWC	The 32.768-kHz clock which is input externally. This is the operating clock of the RTC. The PWC is supplied with clock signals which are obtained by division within the RTC.

Table 3.1-4 lists the clocks which are input to and output from each unit. This table lists the supply sources and destinations of the clocks which are input to and output from each unit. The clocks which are supplied to each unit include those supplied by the CPG and those supplied by the other units.

Table 3.1-4 List of Unit Clocks (1/10)

Unit Clock				Supply Source/Destination	
Unit	Clock Pin	I/O	Frequency [MHz]	Unit	Clock Pin
RTC*3	—	—	—	—	—
PWC*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
CPG	XINCLK	Input	48	External pin	XIN
	DETCK	Input	50	External pin	DETCK
	AUPLLCLK	Input	12.288	External pin	AUPLLCLK
	AUMCLK	Output	12	External pin	AUMCLK
	LCI_CLK_GP	Input	20 to 375	LCI	PLLQTCLK
	GMCLK0	Output	Max. 100	External pin	GMCLK0
	GMCLK1	Output	Max. 100	External pin	GMCLK1
CA53	CLKIN	Input	996/498/332/249/166/83/41.5	CPG	CA53_CLK
	APCLK_DBG	Input	400/200/100/50/48	CPG	CA53_APCLK_DBG
	ACLK	Input	400/200/100/50/48	CPG	CA53_ACLK
	ATCLK	Input	400/200/100/50/48	CPG	CA53_ATCLK
	TSCLK	Input	48	CPG	CA53_TSCLK
	APCLK_REG	Input	200/100/50/48	CPG	CA53_APCLK_REG
CIF*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
CSI0	PCLK	Input	100/50/48	CPG	CPERI_GRPG_PCLK
	CSICLK	Input	48/24	CPG	CSI_CLK[0]
	SCKI	Input	Max. 24	External pin	CSSCLK0
	SCKO	Output	24/12 (CSICLK/2)	External pin	

Table 3.1-4 List of Unit Clocks (2/10)

Unit Clock				Supply Source/Destination	
Unit	Clock Pin	I/O	Frequency [MHz]	Unit	Clock Pin
CSI1	PCLK	Input	100/50/48	CPG	CPERI_GRPG_PCLK
	CSICLK	Input	48/24	CPG	CSI_CLK[1]
	SCKI	Input	Max. 24	External pin	CSSCLK1
	SCKO	Output	24/12 (CSICLK/2)	External pin	
CSI2	PCLK	Input	100/50/48	CPG	CPERI_GRPG_PCLK
	CSICLK	Input	48/24	CPG	CSI_CLK[2]
	SCKI	Input	Max. 24	External pin	CSSCLK2
	SCKO	Output	24/12 (CSICLK/2)	External pin	
CSI3	PCLK	Input	100/50/48	CPG	CPERI_GRPG_PCLK
	CSICLK	Input	48/24	CPG	CSI_CLK[3]
	SCKI	Input	Max. 24	External pin	CSSCLK3
	SCKO	Output	24/12 (CSICLK/2)	External pin	
CSI4	PCLK	Input	100/50/48	CPG	CPERI_GRPH_PCLK
	CSICLK	Input	48/24	CPG	CSI_CLK[4]
	SCKI	Input	Max. 24	External pin	CSSCLK4
	SCKO	Output	24/12 (CSICLK/2)	External pin	
CSI5	PCLK	Input	100/50/48	CPG	CPERI_GRPH_PCLK
	CSICLK	Input	48/24	CPG	CSI_CLK[5]
	SCKI	Input	Max. 24	External pin	CSSCLK5
	SCKO	Output	24/12 (CSICLK/2)	External pin	
CST	cs_clk	Input	400/200/100/50/48	CPG	CST_CS_CLK
	ts_clk	Input	48	CPG	CST_TS_CLK
	traceclkin	Input	100/50/48	CPG	CST_TRACECLK
	swclktck	Input	50	CPG	TCK
	sb_clk	Input	200/100/50/48	CPG	CST_SB_CLK
	ahb_clk	Input	48	CPG	CST_AHB_CLK
	apb_ca53_clk	Input	400/200/100/50/48	CPG	CST_APB_CA53_CLK
	atb_sb_clk	Input	200/100/50/48	CPG	CST_ATB_SB_CLK
	ts_sb_clk	Input	200/100/50/48	CPG	CST_TS_SB_CLK
	traceclk_traceout	Output	50	External pin	TRCLK

Table 3.1-4 List of Unit Clocks (3/10)

Unit Clock				Supply Source/Destination	
Unit	Clock Pin	I/O	Frequency [MHz]	Unit	Clock Pin
LPDDR4*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
DMAC	ACLK	Input	200/100/50/48	CPG	DMAA_ACLK
DRP-AI	ACLK	Input	400/200/100/50/48	CPG	DRPA_ACLK
	DCLKIN	Input	1260	CPG	DRPA_DCLK
	INITCLK	Input	48	CPG	DRPA_INITCLK
	MCLK	Input	400/200/100/50/48	CPG	DRPA_ACLK
ETHER*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
GIC	CLK	Input	200/100/50/25/24	CPG	GIC_CLK
GRP	clk	Input	200/100/50/48	CPG	GRP_CLK
HDMI*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—

Table 3.1-4 List of Unit Clocks (4/10)

Unit Clock				Supply Source/Destination	
Unit	Clock Pin	I/O	Frequency [MHz]	Unit	Clock Pin
IIC0	PCLK	Input	100/50/48	CPG	IIC_PCLK[0]
	SCLI	Input	0.4	External pin	I2SCL0
	SCLO0	Output	0.4	External pin	
IIC1	PCLK	Input	100/50/48	CPG	IIC_PCLK[0]
	SCLI	Input	0.4	External pin	I2SCL1
	SCLO0	Output	0.4	External pin	
IIC2	PCLK	Input	100/50/48	CPG	IIC_PCLK[1]
	SCLI	Input	0.4	External pin	CSRXD2
	SCLO0	Output	0.4	External pin	
IIC3	PCLK	Input	100/50/48	CPG	IIC_PCLK[1]
	SCLI	Input	0.4	External pin	CSCS2
	SCLO0	Output	0.4	External pin	
LCI*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
NAND*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
PCIe*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
PFC	PCLK	Input	48	CPG	PFC_PCLK
PMC	PCLK	Input	48	CPG	PMC_CORE_CLOCK
PWM0	PCLK	Input	100/50/48	CPG	CPERI_GRPE_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[0]
PWM1	PCLK	Input	100/50/48	CPG	CPERI_GRPE_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[1]

Table 3.1-4 List of Unit Clocks (5/10)

Unit Clock				Supply Source/Destination	
Unit	Clock Pin	I/O	Frequency [MHz]	Unit	Clock Pin
PWM2	PCLK	Input	100/50/48	CPG	CPERI_GRPE_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[2]
PWM3	PCLK	Input	100/50/48	CPG	CPERI_GRPE_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[3]
PWM4	PCLK	Input	100/50/48	CPG	CPERI_GRPE_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[4]
PWM5	PCLK	Input	100/50/48	CPG	CPERI_GRPE_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[5]
PWM6	PCLK	Input	100/50/48	CPG	CPERI_GRPE_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[6]
PWM7	PCLK	Input	100/50/48	CPG	CPERI_GRPE_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[7]
PWM8	PCLK	Input	100/50/48	CPG	CPERI_GRPF_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[8]
PWM9	PCLK	Input	100/50/48	CPG	CPERI_GRPF_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[9]
PWM10	PCLK	Input	100/50/48	CPG	CPERI_GRPF_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[10]
PWM11	PCLK	Input	100/50/48	CPG	CPERI_GRPF_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[11]
PWM12	PCLK	Input	100/50/48	CPG	CPERI_GRPF_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[12]
PWM13	PCLK	Input	100/50/48	CPG	CPERI_GRPF_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[13]
PWM14	PCLK	Input	100/50/48	CPG	CPERI_GRPF_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[14]
PWM15	PCLK	Input	100/50/48	CPG	CPERI_GRPF_PCLK
	PWM_CLK	Input	48	CPG	PWM_CLK[15]
RAMA	ACLK	Input	400/200/100/50/48	CPG	RAMA_ACLK
RAMB0	ACLK	Input	400/200/100/50/48	CPG	RAMB_ACLK[0]
RAMB1	ACLK	Input	400/200/100/50/48	CPG	RAMB_ACLK[1]
RAMB2	ACLK	Input	400/200/100/50/48	CPG	RAMB_ACLK[2]
RAMB3	ACLK	Input	400/200/100/50/48	CPG	RAMB_ACLK[3]
ROM	ACLK	Input	200/100/50/48	CPG	ROM_ACLK
SDI0*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—

Table 3.1-4 List of Unit Clocks (6/10)

Unit Clock				Supply Source/Destination	
Unit	Clock Pin	I/O	Frequency [MHz]	Unit	Clock Pin
SDI1*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
eMMC*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
SEC	ACLK	Input	200/100/50/48	CPG	SEC_ACLK
	PCLK	Input	200/100/50/48	CPG	SEC_PCLK
	TCLK	Input	200/100/50/48	CPG	SEC_TCLK
	PCLK_TSIPG	Input	200/100/50/48	CPG	SEC_TCLK
SYC	CNT_CLK	Input	24	CPG	SYC_CNT_CLK
SYS	PCLK	Input	48	CPG	SYS_CLK
	PCI_ACLK	Input	200/100/50/48	CPG	PCI_ACLK
	IIC_PCLK1	Input	100/50/48	CPG	IIC_PCLK[1]
	IIC_PCLK0	Input	100/50/48	CPG	IIC_PCLK[0]
TIM0	PCLK	Input	100/50/48	CPG	CPERI_GRPA_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[0]
TIM1	PCLK	Input	100/50/48	CPG	CPERI_GRPA_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[1]
TIM2	PCLK	Input	100/50/48	CPG	CPERI_GRPA_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[2]
TIM3	PCLK	Input	100/50/48	CPG	CPERI_GRPA_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[3]
TIM4	PCLK	Input	100/50/48	CPG	CPERI_GRPA_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[4]
TIM5	PCLK	Input	100/50/48	CPG	CPERI_GRPA_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[5]
TIM6	PCLK	Input	100/50/48	CPG	CPERI_GRPA_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[6]
TIM7	PCLK	Input	100/50/48	CPG	CPERI_GRPA_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[7]
TIM8	PCLK	Input	100/50/48	CPG	CPERI_GRPB_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[8]
TIM9	PCLK	Input	100/50/48	CPG	CPERI_GRPB_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[9]
TIM10	PCLK	Input	100/50/48	CPG	CPERI_GRPB_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[10]
TIM11	PCLK	Input	100/50/48	CPG	CPERI_GRPB_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[11]

Table 3.1-4 List of Unit Clocks (7/10)

Unit Clock				Supply Source/Destination	
Unit	Clock Pin	I/O	Frequency [MHz]	Unit	Clock Pin
TIM12	PCLK	Input	100/50/48	CPG	CPERI_GRPB_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[12]
TIM13	PCLK	Input	100/50/48	CPG	CPERI_GRPB_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[13]
TIM14	PCLK	Input	100/50/48	CPG	CPERI_GRPB_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[14]
TIM15	PCLK	Input	100/50/48	CPG	CPERI_GRPB_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[15]
TIM16	PCLK	Input	100/50/48	CPG	CPERI_GRPC_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[16]
TIM17	PCLK	Input	100/50/48	CPG	CPERI_GRPC_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[17]
TIM18	PCLK	Input	100/50/48	CPG	CPERI_GRPC_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[18]
TIM19	PCLK	Input	100/50/48	CPG	CPERI_GRPC_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[19]
TIM20	PCLK	Input	100/50/48	CPG	CPERI_GRPC_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[20]
TIM21	PCLK	Input	100/50/48	CPG	CPERI_GRPC_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[21]
TIM22	PCLK	Input	100/50/48	CPG	CPERI_GRPC_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[22]
TIM23	PCLK	Input	100/50/48	CPG	CPERI_GRPC_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[23]
TIM24	PCLK	Input	100/50/48	CPG	CPERI_GRPD_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[24]
TIM25	PCLK	Input	100/50/48	CPG	CPERI_GRPD_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[25]
TIM26	PCLK	Input	100/50/48	CPG	CPERI_GRPD_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[26]
TIM27	PCLK	Input	100/50/48	CPG	CPERI_GRPD_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[27]
TIM28	PCLK	Input	100/50/48	CPG	CPERI_GRPD_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[28]
TIM29	PCLK	Input	100/50/48	CPG	CPERI_GRPD_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[29]
TIM30	PCLK	Input	100/50/48	CPG	CPERI_GRPD_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[30]
TIM31	PCLK	Input	100/50/48	CPG	CPERI_GRPD_PCLK
	INCLOCK	Input	2	CPG	TIM_CLK[31]
TSU0	PCLK	Input	48	CPG	TSU0_PCLK
TSU1	PCLK	Input	48	CPG	TSU1_PCLK
UART0	PCLK	Input	100/50/48	CPG	URT_PCLK
	SCLK	Input	Max. 108/48	CPG	URT_CLK[0]

Table 3.1-4 List of Unit Clocks (8/10)

Unit Clock				Supply Source/Destination	
Unit	Clock Pin	I/O	Frequency [MHz]	Unit	Clock Pin
UART1	PCLK	Input	100/50/48	CPG	URT_PCLK
	SCLK	Input	Max. 108/48	CPG	URT_CLK[1]
USB*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
VCD*3	—	—	—	—	—
	—	—	—	—	—
WDT0	PCLK	Input	100/50/48	CPG	WDT_PCLK[0]
	WDT_CLK	Input	48	CPG	WDT_CLK[0]
WDT1	PCLK	Input	100/50/48	CPG	WDT_PCLK[1]
	WDT_CLK	Input	48	CPG	WDT_CLK[1]
AUI*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
ADCA*3	—	—	—	—	—
	—	—	—	—	—
ADCB*3	—	—	—	—	—
	—	—	—	—	—
MTR*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
DCU*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
ESI*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—

Table 3.1-4 List of Unit Clocks (9/10)

Unit Clock				Supply Source/Destination	
Unit	Clock Pin	I/O	Frequency [MHz]	Unit	Clock Pin
STG*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
JPG*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
ISP*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
GPA*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
MTD*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—

Table 3.1-4 List of Unit Clocks (10/10)

Unit Clock				Supply Source/Destination	
Unit	Clock Pin	I/O	Frequency [MHz]	Unit	Clock Pin
ICB*3	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—		—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—
	—	—	—	—	—

Note 1. This pin functions as an output in actual operation.

Note 2. P0_CLK and P1_CLK of CIF are controlled and supplied by the Clock Gating cells within the CIF.

Note 3. For more information, contact a Renesas Electronics sales representative.

3.2 Clock System Diagram

For the clock system diagram, see the section of CPG.

3.3 Clock Configuration of CPG

All units excluding RTC*1 and PWC*2 of this LSI are configured to supply the clock signal from the CPG. The CPG has the following functionality to control the clock signal for supply to a given unit.

- Six PLLs
- Dividers
- Clock selectors
- Clock Gating cells

Note 1. The RTC runs on the 32.768-kHz clock which is input externally.
Note 2. The PWC runs on a frequency-divided clock supplied from the RTC.

Figure 3.3-1 shows a schematic view of the clock configuration of this LSI.

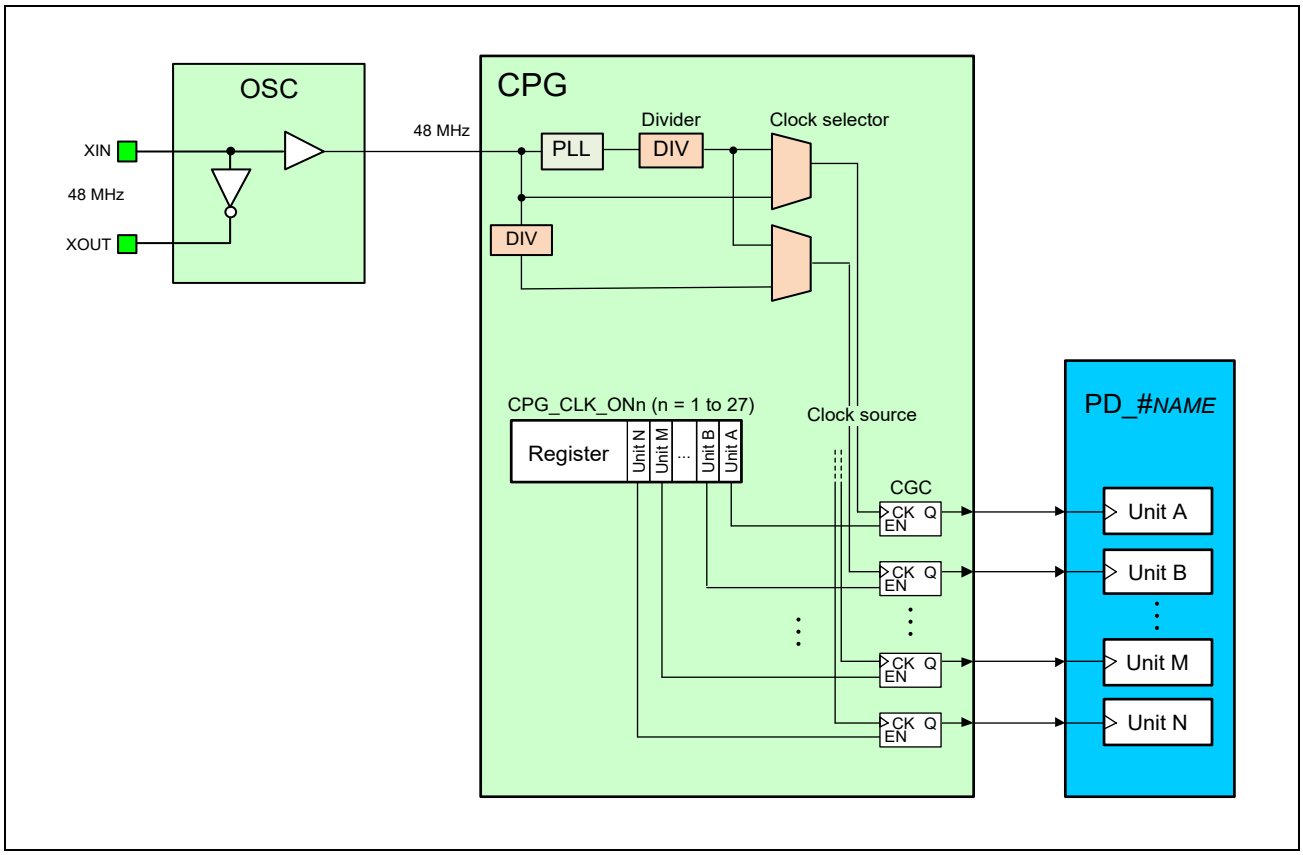


Figure 3.3-1 Schematic View of the Clock Configuration

3.4 Clock Function

3.4.1 PLLs

This LSI includes six PLLs. The PLLs multiply externally input 48-MHz clocks as reference signals to generate high-speed clocks. Each PLL can change the operating mode and the oscillation frequency.

Table 3.4-1 lists the types of PLLs of this LSI and their main usages.

Table 3.4-1 Types and Usages of PLLs

PLL Name	SSCG Setting	Main Usage
PLL1	SSCG is available (default SSCG included)	Dedicated for CA53
PLL2	SSCG is available (default SSCG included)	For SYSTEM BUS and ISP
PLL3	SSCG is available (default SSCG included)	Dedicated for LPDDR4
PLL4	SSCG is not available	For STG, MTR, and ADC
PLL6	SSCG is available (default SSCG not included)	Dedicated for DRP-AI
PLL7	SSCG is available (default SSCG included)	For display control

3.4.2 Dividers and Clock Selectors

Dividers and clock selectors are located in a later stage of the PLL.

There are two types of divider: a fixed divider where the frequency divisor is fixed and a variable divider which can change the frequency divisor.

3.4.3 Clock Gating Cells

Clock Gating cells are located on a part of the clock output paths, which can control supplying and stopping of the clock signal.

Section 4 Reset

This section describes resets of this LSI.

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

4.1 Overview of Resets

Classification of Resets

The reset functions of this LSI are classified into three categories: hardware resets, watchdog timer reset, and software resets. **Table 4.1-1** lists the classification of resets. For details, see the section of CPG.

Table 4.1-1 Classification of Resets

Category	Sub-Category	Reset Source	Scope
Hardware resets (External pin resets)	Single resets	RTRSTN pin	RTC
		PWRSTN pin	PWC
		DETRSTN pin*1 DESRSTN pin*1	TAP of CST
	System resets	RSTN pin	All units excluding RTC and PWC
		DETRSTN pin*1 DESRSTN pin*1	
Watchdog timer reset		Counter overflow	All units excluding RTC and PWC
Software resets (register control resets)	CPG register control reset	CPG register control	Target units set by registers
	CA53 register control reset	CA53 register control	CA53
	CST register control reset	CST register control	CST
	Resets within the units	Control of individual unit registers	Functions within the units

Note 1. The DESRSTN and DETRSTN pins are debugger-dedicated pins.

4.2 Configuration of Resets

4.2.1 Configuration of Hardware Resets (External Pin Resets)

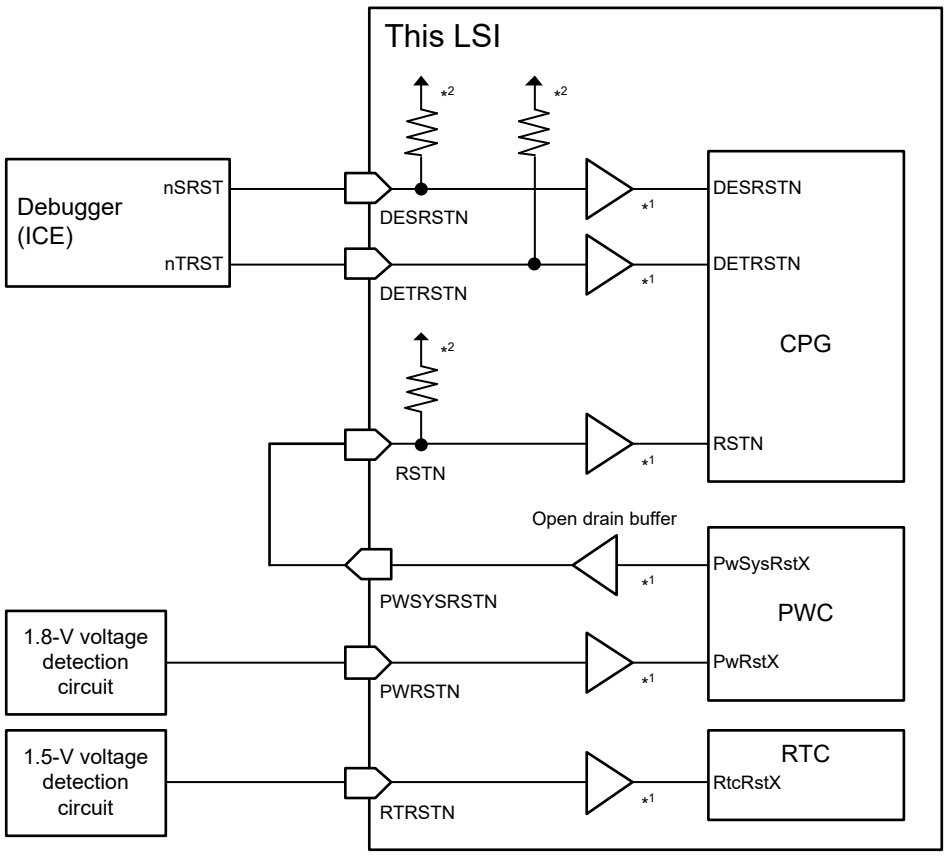
Table 4.2-1 lists the names and functions of the external pins for a hardware reset.

For the connection configuration (example of connection) of the external pin resets, see **Figure 4.2-1**.

Table 4.2-1 Hardware Reset Pin Functions

Pin Name	I/O	Function	Active Level	Connected Unit
Single reset for external pins: Reset range is RTC single reset and PWC single reset				
RTRSTN	Input	Input reset of the RTC section	Low	RTC
PWRSTN	Input	Input reset of the PWC section	Low	PWC
Reset for external RSTN pin: Reset range is system reset				
RSTN	Input	System input reset	Low	CPG
PWSYSRSTN	Output	System reset output. Connected to the RSTN pin to use the power control function of PWC.	—	PWC
Reset for external debugger: Reset range is system reset				
DETRSTN	Input	Input reset of the TAP section from the debugger	Low	CPG
DESRSTN	Input	System input reset from the debugger	Low	CPG

Figure 4.2-1 shows an example of connection of the external pin resets (while a debugger is connected).



Note 1. These are connected to the external pins via the externally connected units.

Note 2. A pull-up resistor in the I/O buffer is used.

Figure 4.2-1 Example Connection of the External Pin Resets (while a Debugger is Connected)

CAUTION

RSTN, DESRSTN, and DETRSTN should be asserted for no less than 10 µs. When a system reset is initiated by RSTN, DESRSTN, or DETRSTN, the external power switch of PD_MEM is also turned off. Accordingly, secure the period for assertion of RSTN, DESRSTN, and DETRSTN, so that the power supply voltage of PD_MEM falls below 0.1 V within 10 µs or to continue until the power supply voltage falls below 0.1 V. In addition, to switch the power supply for PD_MEM on or off by using the external power switch, make sure that the power supply voltage is cut off within the above period or secure enough time for the assertion of RSTN, DESRSTN, and DETRSTN so that the power supply voltage has been cut off.

4.2.2 Configuration of Watchdog Timer Reset

A reset request signal from the WDT (WDTRSTB) is connected to a WDT timeout reset pin (WDT_RST_N[n] (n = 0, 1) of the CPG. If WDTRSTB on either pin is asserted, this LSI is system-reset.

4.2.3 List of Unit Resets

Control over the resetting of individual units is possible by setting registers of the CPG by software. **Table 4.2-2** lists the correspondence between the reset pins of individual units and the sources for supply of the resets.

Table 4.2-2 List of Unit Resets (1/3)

Unit Reset		Supply Source	
Unit	Reset Pin	Unit	Reset Pin
CA53	ARESETn	CPG	CA53_NARESET
	nCPUPORESET[0]	CPG	CA53_NCPUPORESET[0]
	nCPUPORESET[1]	CPG	CA53_NCPUPORESET[1]
	nCORERESET[0]	CPG	CA53_NCORERESET[0]
	nCORERESET[1]	CPG	CA53_NCORERESET[1]
	nPRESETDBG	CPG	CA53_NPRESETDBG
	nL2RESET	CPG	CA53_L2RESET
	nMISCRESET_HM	CPG	CA53_NMISCRESET_HM
	nMISCRESET_SM	CPG	CA53_NMISCRESET_SM
CIF*1	—	—	—
CSI0	PRESETn	CPG	CSI_GPG_PRESETN
CSI1	PRESETn	CPG	CSI_GPG_PRESETN
CSI2	PRESETn	CPG	CSI_GPG_PRESETN
CSI3	PRESETn	CPG	CSI_GPG_PRESETN
CSI4	PRESETn	CPG	CSI_GPH_PRESETN
CSI5	PRESETn	CPG	CSI_GPH_PRESETN
CST	ntrst	CPG	CST_NTRST
	npotrst	CPG	CST_NPOTRST
	cs_resetn	CPG	CST_CS_RESETN
	ts_resetn	CPG	CST_TS_RESETN
	traceresetn	CPG	CST_TRESETN
	sb_resetn	CPG	CST_SB_RESETN
	ahb_resetn	CPG	CST_AHB_RESETN
	apb_ca53_resetn	CPG	CST_APB_CA53_RESETN
	atb_sb_resetn	CPG	CST_ATB_SB_RESETN
	ts_sb_resetn	CPG	CST_TS_SB_RESETN
LPDDR4*1	—	—	—
	—	—	—
	—	—	—
	—	—	—
	—	—	—
	—	—	—
DMAC	ARESETn	CPG	DMAA_ARESETN
DRP-AI	ARESETn	CPG	DRPA_ARESETN

Table 4.2-2 List of Unit Resets (2/3)

Unit Reset		Supply Source	
Unit	Reset Pin	Unit	Reset Pin
ETHER*1	—	—	—
GIC	nRESET	CPG	GIC_NRESET
GRP*1	—	—	—
HDMI*1	—	—	—
	—	—	—
IIC0	PRESETZ	CPG	IIC_GPA_PRESETN
IIC1	PRESETZ	CPG	IIC_GPA_PRESETN
IIC2	PRESETZ	CPG	IIC_GPB_PRESETN
IIC3	PRESETZ	CPG	IIC_GPB_PRESETN
LCI*1	—	—	—
	—	—	—
NAND*1	—	—	—
	—	—	—
PCIe*1	—	—	—
PFC	PRESETn	CPG	PFC_PRESETN
PMC	PRESETn	CPG	PMC_RESET_N
PWM0-7	PRESETn	CPG	PWM_GPE_PRESETN
PWM8-15	PRESETn	CPG	PWM_GPF_PRESETN
RAMA	ARESETn	CPG	RAMA_ARESETN
RAMB0	ARESETn	CPG	RAMB_ARESETN[0]
RAMB1	ARESETn	CPG	RAMB_ARESETN[1]
RAMB2	ARESETn	CPG	RAMB_ARESETN[2]
RAMB3	ARESETn	CPG	RAMB_ARESETN[3]
ROM	ARESETn	CPG	ROM_ARESETN
SDI0*1	—	—	—
SDI1*1	—	—	—
eMMC*1	—	—	—
SEC	ARESETn	CPG	SEC_ARESETN
	PRESETn	CPG	SEC_PRESETN
	RSTB	CPG	SEC_RSTB
SYC	RESETN	CPG	SYC_RST_N
SYS	PRESETn	CPG	SYS_RST_N
TIM0-7	PRESETn	CPG	TIM_GPA_PRESETN
TIM8-15	PRESETn	CPG	TIM_GPB_PRESETN
TIM16-23	PRESETn	CPG	TIM_GPC_PRESETN
TIM24-31	PRESETn	CPG	TIM_GPD_PRESETN
TSU0	PRESETn	CPG	TSU0_RESETN
TSU1	PRESETn	CPG	TSU1_RESETN
UART0	PRESETn	CPG	URT_PRESETN
UART1	PRESETn	CPG	URT_PRESETN
USB*1	—	—	—
	—	—	—
	—	—	—
	—	—	—

Table 4.2-2 List of Unit Resets (3/3)

Unit Reset		Supply Source	
Unit	Reset Pin	Unit	Reset Pin
VCD*1	—	—	—
WDT0	PRESETn	CPG	WDT_PRESETN[0]
WDT1	PRESETn	CPG	WDT_PRESETN[1]
AUI*1	—	—	—
ADCA*1	—	—	—
ADCB*1	—	—	—
MTR*1	—	—	—
DCU*1	—	—	—
ESI*1	—	—	—
STG*1	—	—	—
JPG*1	—	—	—
ISP*1	—	—	—
	—	—	—
	—	—	—
	—	—	—
	—	—	—
	—	—	—
	—	—	—
GPA*1	—	—	—
	—	—	—
MTD*1	—	—	—
ICB*1	—	—	—
	—	—	—
	—	—	—
	—	—	—
	—	—	—

Note 1. For more information, contact a Renesas Electronics sales representative.

4.3 Reset System Diagram

For the reset system diagram, see the section of CPG.

4.4 Reset Functions

4.4.1 Hardware Resets (External Pin Resets)

These resets are initiated by external pins of the LSI.

The units to be reset depend on the reset pin through which control is applied.

4.4.1.1 Single Resets

A few units can be individually reset. For details, refer to the description of CPG.

(1) RTC and PWC Resets

The RTRSTN and PWRSTN pins are dedicated for resetting of the RTC and PWC, respectively. These reset pins must be controlled by the external circuits of this LSI.

Table 4.4-1 lists the sources of the single resets and the respective timings for release from reset.

Table 4.4-1 Single Reset Control

Category	Source (Reset Pin State)	Reset Release Timing	Scope
RTC reset	RTRSTN pin = Low	After 1.5-V power is supplied to the I/O section of RTC and 0.8-V power is supplied to the RTC core	RTC
PWC reset	PWRSTN pin = Low	After 1.8-V power is supplied to the I/O section of RTC and 0.8-V power is supplied to the RTC core	PWC

(2) CST TAP Reset

If the input levels on the DESRSTN and DETRSTN pins are high and low, respectively, in debugging mode (i.e., the MD6 = low and the MD5 pin = high), the TAP section of the CST is reset. It is released from the reset state when both the DESRSTN and DETRSTN pins are at the high level.

Table 4.4-2 lists the source of a debugger reset by the DESRSTN and DETRSTN pins and the timing for release from reset.

Table 4.4-2 Debugger Reset Control

Category	Source (Reset Pin State)	Reset Release Timing	Scope
Debugger reset	DESRSTN = High and DETRSTN = Low	After the external power supplies of the LSI are turned on	TAP within the CST

4.4.1.2 System Reset

(1) System Reset in Normal Mode

The RSTN pin and the debugger-dedicated pins (DESRSTN and DETRSTN pins) control a system reset.

Table 4.4-3 lists the sources of a system reset by the pins and the timing for release from reset.

Table 4.4-3 System Reset: Control Pins

Category	Source (Reset Pin State)	Reset Release Timing	Scope
System reset	RSTN pin = Low	After the external power supplies of the LSI are turned on	All units of this LSI excluding PWC and RTC
	DESRSTN pin = Low DETRSTN pin = Low or High		

By connecting the output signal on the PWCSYSRSTN pin to the RSTN pin, the LSI can be released from the reset state in response to the completion of the external power supplies being turned on (the PWCSYSRSTN pin outputs the low level while the external power supplies are turned on and is placed in the Hi-Z state after the completion of the external power supplies being turned on). Note that the RSTN pin is provided with a pull-up resistor within the LSI.

4.4.2 Watchdog Timer Reset

A watchdog timer reset is automatically initiated by the hardware of this LSI when the counter of the watchdog timer of this LSI detects an overflow*[1]. After an interrupt request signal is generated, deassert the interrupt signal of the watchdog timer by software until the next time the counter overflows

Note 1. After an interrupt request signal is generated in every period set in the counter of the watchdog timer, the interrupt signal is not asserted and the counter overflows next time.

4.4.3 Software Resets

A software reset involves the initialization in response to a register setting.

There are four types of software reset listed below.

- Reset for initializing the target units by setting registers in the CPG.
- Reset for initializing CA53 by setting registers in CA53
- Reset for initializing the debugging function by setting registers in the CST
- Reset for initializing the functions within the units individually by setting registers in other units

Section 5 Interrupt

This section describes the interrupt function of this LSI.

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

5.1 Interrupt System Diagram

This LSI is equipped with a GIC (GIC-400) as an interrupt controller for CA53. Signals from respective units and external interrupts are input via a synchronization circuit and a GIC (GIC-400).

Figure 5.1-1 shows the interrupt system diagram of this LSI.

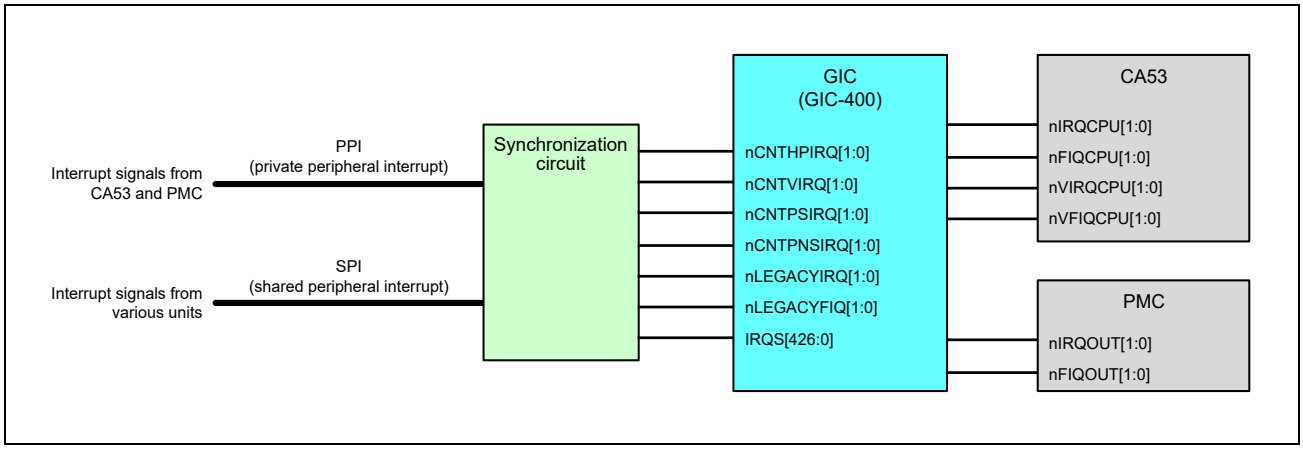


Figure 5.1-1 Interrupt System Diagram

NOTE

For details on the interrupt control (controlling the interrupt controller), see the GIC section.
However, as the following units are for use with the ISP support package, do not use the registers of the GIC related to the target channels.

Unit Name	Resource for Use with ISP Support Package
TIM	Total of 16 channels, ch. 0 to ch. 7 and ch. 23 to ch. 31
PWM	Total of 9 channels, ch. 0 to ch. 7 and ch. 15
DMAC	Total of 8 channels, DMAC1 ch. 0 to ch. 7
UART	Ch. 1
IIC	Total of 2 channels, ch. 1 and ch. 3
CSI	Total of 4 channels, ch. 1 to ch. 3 and ch. 5
WDT	Ch. 1
GRP	—
VCD	—
JPG	—
MTD	—

Unit Name	Resource for Use with ISP Support Package
ESI	—
AUI	—
MTR	—
ADCA	—
ADCB	—
DCU	—
LCI	—
HDMI	—
STG	—
ISP/GPA	—

5.2 Synchronization and Polarity of Interrupts

The input specifications of the GIC are shown below.

- PPI (private peripheral interrupt): Active-low level interrupt
- SPI (shared peripheral interrupt): Active-high level interrupt or rise-edge pulse interrupt

To satisfy this specification, the interrupt signals from the various units are polarity-matched and synchronized.

Figure 5.2-1 shows a functional overview of the synchronization circuit.

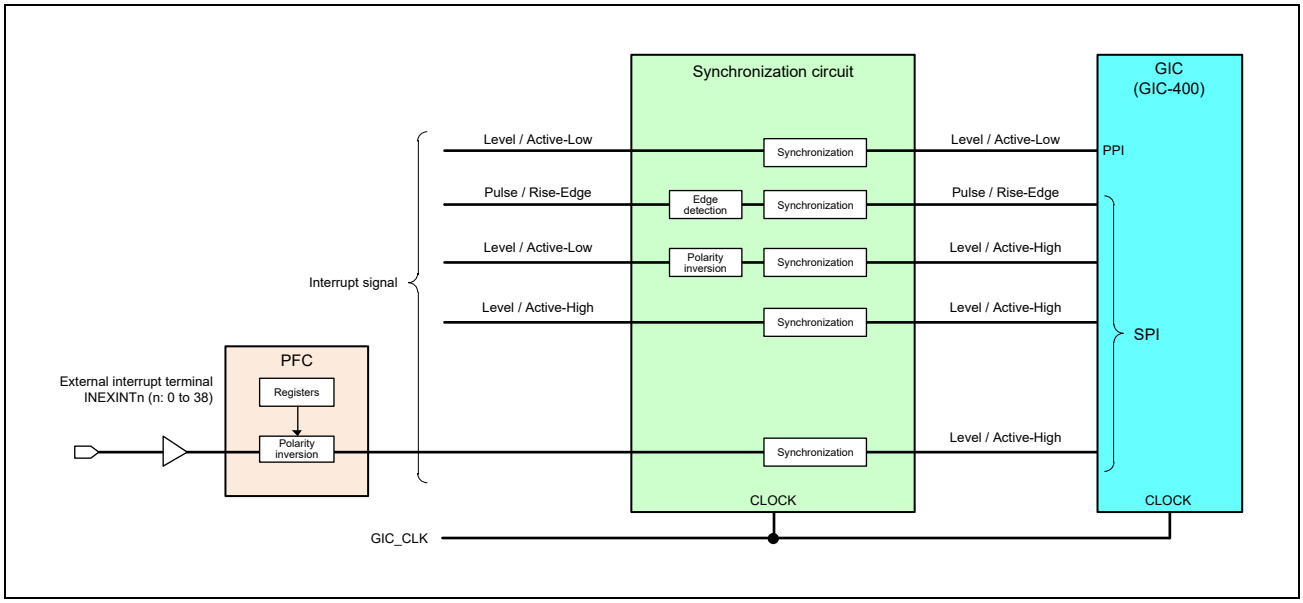


Figure 5.2-1 Functional Overview of the Synchronization Circuit

5.3 Interrupt Settings

Some units always require register settings for level or pulse mode and the active level of the interrupt.

5.3.1 Level/Pulse Mode Setting

The interrupt outputs of the units listed in **Table 5.3-1** require the selection of level or pulse mode by the register of the respective units.

This interrupt should be used with the settings listed in the table.

Table 5.3-1 Interrupt Signals with Switching Function between Level Mode and Pulse Mode

Unit Name	Interrupt Output Pin Name	Description
DMAC	DMAINT[15:0]	Set it to level mode for use.
	DMAERR	Set it to level mode for use.
TIM0-31	INTCMD	Set it to level mode for use.

NOTE

The interrupt output mode for units other than listed in **Table 5.3-1** is fixed. (Level or pulse mode cannot be selected.)
For details on register settings, see the DMAC section and TIM section.

5.3.2 Active Level Setting

For interrupts input from the external interrupt pin INEXINTn (n: 0 to 38), the active level can be selected by the register in the PFC unit.

The active level of the interrupt input pins should be set and used according to the interrupt specifications of the external device.

For details on the settings, see the PFC section.

5.4 List of Interrupts

Table 5.4-1 is the list of GIC interrupts.

Set the interrupts (level or pulse interrupts) for the interrupt controller as shown in the table.

5.4.1 List of CA53 Interrupts

Table 5.4-1 lists the interrupt ID assignment information for the GIC (GIC-400 for CA53).

The following table shows the correspondence between the interrupt input pins of the GIC and the interrupt outputs notified to the GIC from individual units.

Table 5.4-1 Interrupt list of GIC (GIC-400 for CA53) (1/10)

PPI/ SPI	ID	GIC Input Pin Name	Interrupt Request Source				
			Unit	Output Pin Name	Interrupt Description	Level/ Pulse	Active Level
PPI	26	nCNTHPIRQ[0]	CA53	nCNTHPIRQ[0]	Hypervisor physical timer interrupt [Core0/Core1]	Level	Low
		nCNTHPIRQ[1]		nCNTHPIRQ[1]			
	27	nCNTVIRQ[0]	CA53	nCNTVIRQ[0]	Virtual timer event [Core0/Core1]	Level	Low
		nCNTVIRQ[1]		nCNTVIRQ[1]			
	28	nLEGACTFIQ[0]	PMC	INT_CA53_LFIQ_N[0]	Cortex-A53 standby release signal [Core0/Core1] (Legacy FIQ)	Level	Low
		nLEGACTFIQ[1]		INT_CA53_LFIQ_N[1]			
	29	nCNTPSIRQ[0]	CA53	nCNTPSIRQ[0]	Secure physical timer event [Core0/Core1]	Level	Low
		nCNTPSIRQ[1]		nCNTPSIRQ[1]			
	30	nCNTPNSIRQ[0]	CA53	nCNTPNSIRQ[0]	Non-secure physical timer event [Core0/Core1]	Level	Low
		nCNTPNSIRQ[1]		nCNTPNSIRQ[1]			
	31	nLEGACYIRQ[0]	PMC	INT_CA53_LIRQ_N[0]	Cortex-A53 standby release signal [Core0/Core1] (Legacy IRQ)	Level	Low
		nLEGACYIRQ[1]		INT_CA53_LIRQ_N[1]			
SPI	32	IRQS[0]	—	Reserved	—	—	—
	33	IRQS[1]	—	Reserved	—	—	—
	34	IRQS[2]	CA53	CTIIRQ[0]	CTI interrupt request [Core0/Core1] **[For debugging]**	Level	High
	35	IRQS[3]		CTIIRQ[1]			
	36	IRQS[4]	CA53	DBGRSTREQ[0]	Debug reset request [Core0/Core1] **[For debugging]**	Level	High
	37	IRQS[5]		DBGRSTREQ[1]			
	38	IRQS[6]	—	Reserved	—	—	—
	39	IRQS[7]	—	Reserved	—	—	—
	40	IRQS[8]	—	Reserved	—	—	—
	41	IRQS[9]	—	Reserved	—	—	—
	42	IRQS[10]	CA53	WARMRSTREQ[0]	Warm reset request [Core0/Core1]	Level	High
	43	IRQS[11]		WARMRSTREQ[1]			
	44	IRQS[12]		STANDBYWFI[0]	Standby WFI state [Core0/Core1]	Level	High
	45	IRQS[13]		STANDBYWFI[1]			
	46	IRQS[14]		STANDBYWFE[0]	Standby WFE state [Core0/Core1]	Level	High
	47	IRQS[15]		STANDBYWFE[1]			
	48	IRQS[16]		STANDBYWFIL2	Standby WFIL2 state	Level	High
	49	IRQS[17]		L2FLUSHDONE	L2 flush completion	Level	High

Table 5.4-1 Interrupt list of GIC (GIC-400 for CA53) (2/10)

PPI/ SPI	ID	GIC Input Pin Name	Interrupt Request Source				
			Unit	Output Pin Name	Interrupt Description	Level/ Pulse	Active Level
SPI	50	IRQS[18]	—	Reserved	—	—	—
	51	IRQS[19]	—	Reserved	—	—	—
	52	IRQS[20]	—	Reserved	—	—	—
	53	IRQS[21]	—	Reserved	—	—	—
	54	IRQS[22]	—	Reserved	—	—	—
	55	IRQS[23]	—	Reserved	—	—	—
	56	IRQS[24]	—	Reserved	—	—	—
	57	IRQS[25]	—	Reserved	—	—	—
	58	IRQS[26]	—	Reserved	—	—	—
	59	IRQS[27]	—	Reserved	—	—	—
	60	IRQS[28]	—	Reserved	—	—	—
	61	IRQS[29]	—	Reserved	—	—	—
	62	IRQS[30]	—	Reserved	—	—	—
	63	IRQS[31]	—	Reserved	—	—	—
	64	IRQS[32]	—	Reserved	—	—	—
	65	IRQS[33]	—	Reserved	—	—	—
	66	IRQS[34]	—	Reserved	—	—	—
	67	IRQS[35]	—	Reserved	—	—	—
	68	IRQS[36]	—	Reserved	—	—	—
	69	IRQS[37]	—	Reserved	—	—	—
	70	IRQS[38]	—	Reserved	—	—	—
	71	IRQS[39]	CST	cdbgrstreq_cdbgrst	Debug reset request **[For debugging]**	Level	High
	72	IRQS[40]	ICB*3	—	—	—	—
	73	IRQS[41]		—	—	—	—
	74	IRQS[42]		—	—	—	—
	75	IRQS[43]	WDT0	WDTINT	WDT interrupt request output	Level	High
	76	IRQS[44]	WDT1*2				
	77	IRQS[45]	—	Reserved	—	—	—
	78	IRQS[46]	—	Reserved	—	—	—
	79	IRQS[47]	—	Reserved	—	—	—
	80	IRQS[48]	—	Reserved	—	—	—
	81	IRQS[49]	—	Reserved	—	—	—
	82	IRQS[50]	DMAC	DMAINT[0]*2	DMA transaction completion interrupt	Level*1	High
	83	IRQS[51]		DMAINT[1]*2			
	84	IRQS[52]		DMAINT[2]*2			
	85	IRQS[53]		DMAINT[3]*2			
	86	IRQS[54]		DMAINT[4]*2			
	87	IRQS[55]		DMAINT[5]*2			
	88	IRQS[56]		DMAINT[6]*2			
	89	IRQS[57]		DMAINT[7]*2			
	90	IRQS[58]		DMAINT[8]			
	91	IRQS[59]		DMAINT[9]			
	92	IRQS[60]		DMAINT[10]			

Table 5.4-1 Interrupt list of GIC (GIC-400 for CA53) (3/10)

PPI/ SPI	ID	GIC Input Pin Name	Interrupt Request Source				
			Unit	Output Pin Name	Interrupt Description	Level/ Pulse	Active Level
SPI	93	IRQS[61]	DMAC	DMAINT[11]	DMA transaction completion interrupt	Level*1	High
	94	IRQS[62]		DMAINT[12]			
	95	IRQS[63]		DMAINT[13]			
	96	IRQS[64]		DMAINT[14]			
	97	IRQS[65]		DMAINT[15]			
	98	IRQS[66]	—	Reserved	—	—	—
	99	IRQS[67]	—	Reserved	—	—	—
	100	IRQS[68]	PFC	INEXINT[0]*2	External interrupt	Level	High*1
	101	IRQS[69]		INEXINT[1]*2			
	102	IRQS[70]		INEXINT[2]*2			
	103	IRQS[71]		INEXINT[3]*2			
	104	IRQS[72]		INEXINT[4]			
	105	IRQS[73]		INEXINT[5]			
	106	IRQS[74]		INEXINT[6]			
	107	IRQS[75]		INEXINT[7]			
	108	IRQS[76]		INEXINT[8]*2			
	109	IRQS[77]		INEXINT[9]*2			
	110	IRQS[78]		INEXINT[10]*2			
	111	IRQS[79]		INEXINT[11]*2			
	112	IRQS[80]		INEXINT[12]*2			
	113	IRQS[81]		INEXINT[13]*2			
	114	IRQS[82]		INEXINT[14]*2			
	115	IRQS[83]		INEXINT[15]*2			
	116	IRQS[84]		INEXINT[16]			
	117	IRQS[85]		INEXINT[17]			
	118	IRQS[86]		INEXINT[18]			
	119	IRQS[87]		INEXINT[19]			
	120	IRQS[88]		INEXINT[20]			
	121	IRQS[89]		INEXINT[21]			
	122	IRQS[90]		INEXINT[22]			
	123	IRQS[91]		INEXINT[23]*2			
	124	IRQS[92]		INEXINT[24]			
	125	IRQS[93]		INEXINT[25]			
	126	IRQS[94]		INEXINT[26]*2			
	127	IRQS[95]		INEXINT[27]*2			
	128	IRQS[96]		INEXINT[28]*2			
	129	IRQS[97]		INEXINT[29]*2			
	130	IRQS[98]		INEXINT[30]*2			
	131	IRQS[99]		INEXINT[31]*2			
	132	IRQS[100]		INEXINT[32]*2			
	133	IRQS[101]		INEXINT[33]*2			
	134	IRQS[102]		INEXINT[34]*2			
	135	IRQS[103]		INEXINT[35]*2			
	136	IRQS[104]		INEXINT[36]*2			

Table 5.4-1 Interrupt list of GIC (GIC-400 for CA53) (4/10)

PPI/ SPI	ID	GIC Input Pin Name	Interrupt Request Source				
			Unit	Output Pin Name	Interrupt Description	Level/ Pulse	Active Level
SPI	137	IRQS[105]	PFC	INEXINT[37]	External interrupt	Level	High*1
	138	IRQS[106]		INEXINT[38]			
	139	IRQS[107]	TIM0*2	INTCMD	Timer match interrupt request signal	Level*1	High
	140	IRQS[108]	TIM1*2				
	141	IRQS[109]	TIM2*2				
	142	IRQS[110]	TIM3*2				
	143	IRQS[111]	TIM4*2				
	144	IRQS[112]	TIM5*2				
	145	IRQS[113]	TIM6*2				
	146	IRQS[114]	TIM7*2				
	147	IRQS[115]	TIM8				
	148	IRQS[116]	TIM9				
	149	IRQS[117]	TIM10				
	150	IRQS[118]	TIM11				
	151	IRQS[119]	TIM12				
	152	IRQS[120]	TIM13				
	153	IRQS[121]	TIM14				
	154	IRQS[122]	TIM15				
	155	IRQS[123]	TIM16				
	156	IRQS[124]	TIM17				
	157	IRQS[125]	TIM18				
	158	IRQS[126]	TIM19				
	159	IRQS[127]	TIM20				
	160	IRQS[128]	TIM21				
	161	IRQS[129]	TIM22				
	162	IRQS[130]	TIM23*2				
	163	IRQS[131]	TIM24*2				
	164	IRQS[132]	TIM25*2				
	165	IRQS[133]	TIM26*2				
	166	IRQS[134]	TIM27*2				
	167	IRQS[135]	TIM28*2				
	168	IRQS[136]	TIM29*2				
	169	IRQS[137]	TIM30*2				
	170	IRQS[138]	TIM31*2				
	171	IRQS[139]	ISP/ GPA*2,*3	—	—	—	—
	172	IRQS[140]	—	Reserved	—	—	—
	173	IRQS[141]	ADCA *2,*3	—	—	—	—
	174	IRQS[142]		—			
	175	IRQS[143]	ADCB *2,*3	—	—	—	—
	176	IRQS[144]		—			
	177	IRQS[145]	DCU*2,*3	—	—	—	—

Table 5.4-1 Interrupt list of GIC (GIC-400 for CA53) (5/10)

PPI/ SPI	ID	GIC Input Pin Name	Interrupt Request Source			Level/ Pulse	Active Level
			Unit	Output Pin Name	Interrupt Description		
SPI	178	IRQS[146]	GRP*2,*3	—	—	—	—
	179	IRQS[147]		—	—		
	180	IRQS[148]		—	—		
	181	IRQS[149]	LCI*2,*3	—	—	—	—
	182	IRQS[150]		—	—		
	183	IRQS[151]		—	—		
	184	IRQS[152]		—	—		
	185	IRQS[153]		—	—		
	186	IRQS[154]		—	—		
	187	IRQS[155]		—	—		
	188	IRQS[156]		—	—		
	189	IRQS[157]	—	Reserved	—	—	—
	190	IRQS[158]	—	Reserved	—	—	—
	191	IRQS[159]	HDMI *2,*3	—	—	—	—
	192	IRQS[160]	ISP/ GPA*2,*3	—	—		
	193	IRQS[161]		—	—		
	194	IRQS[162]		—	—		
	195	IRQS[163]		—	—		
	196	IRQS[164]	—	Reserved	—	—	—
	197	IRQS[165]	—	Reserved	—	—	—
	198	IRQS[166]	ISP/ GPA*2,*3	—	—	—	—
	199	IRQS[167]		—	—	—	—
	200	IRQS[168]		—	—	—	—
	201	IRQS[169]		—	—	—	—
	202	IRQS[170]		—	—	—	—
	203	IRQS[171]		—	—	—	—
	204	IRQS[172]		—	—	—	—
	205	IRQS[173]		—	—	—	—
	206	IRQS[174]		—	—	—	—
	207	IRQS[175]		—	—	—	—
	208	IRQS[176]	—	Reserved	—	—	—
	209	IRQS[177]	—	Reserved	—	—	—
	210	IRQS[178]	—	Reserved	—	—	—
	211	IRQS[179]	—	Reserved	—	—	—
	212	IRQS[180]	—	Reserved	—	—	—
	213	IRQS[181]	—	Reserved	—	—	—
	214	IRQS[182]	—	Reserved	—	—	—
	215	IRQS[183]	—	Reserved	—	—	—
	216	IRQS[184]	—	Reserved	—	—	—
	217	IRQS[185]	—	Reserved	—	—	—
	218	IRQS[186]	—	Reserved	—	—	—
	219	IRQS[187]	—	Reserved	—	—	—

Table 5.4-1 Interrupt list of GIC (GIC-400 for CA53) (6/10)

PPI/ SPI	ID	GIC Input Pin Name	Interrupt Request Source			Level/ Pulse	Active Level
			Unit	Output Pin Name	Interrupt Description		
SPI	220	IRQS[188]	STG*2,*3	—	—	—	—
	221	IRQS[189]		—			
	222	IRQS[190]		—			
	223	IRQS[191]		—			
	224	IRQS[192]		—			
	225	IRQS[193]		—			
	226	IRQS[194]		—			
	227	IRQS[195]		—			
	228	IRQS[196]		—			
	229	IRQS[197]		—			
	230	IRQS[198]		—			
	231	IRQS[199]		—			
	232	IRQS[200]		—			
	233	IRQS[201]		—			
	234	IRQS[202]		—			
	235	IRQS[203]		—			
	236	IRQS[204]		—			
	237	IRQS[205]		—			
	238	IRQS[206]		—			
	239	IRQS[207]		—			
	240	IRQS[208]	ESI*2,*3	—	—	—	—
	241	IRQS[209]		—			
	242	IRQS[210]		—			
	243	IRQS[211]		—			
	244	IRQS[212]		—			
	245	IRQS[213]		—			
	246	IRQS[214]		—			
	247	IRQS[215]	AUI*2,*3	—	—	—	—
	248	IRQS[216]	MTR*2,*3	—	—	—	—
	249	IRQS[217]		—			
	250	IRQS[218]		—			
	251	IRQS[219]		—			
	252	IRQS[220]		—			
	253	IRQS[221]		—			
	254	IRQS[222]		—			
	255	IRQS[223]		—			
	256	IRQS[224]		—			
	257	IRQS[225]		—			
	258	IRQS[226]	CSI0	CSIINT	CSI interrupt signal	Level	High
	259	IRQS[227]	CSI1*2				
	260	IRQS[228]	CSI2*2				
	261	IRQS[229]	CSI3*2				
	262	IRQS[230]	CSI4				
	263	IRQS[231]	CSI5*2				

Table 5.4-1 Interrupt list of GIC (GIC-400 for CA53) (7/10)

PPI/ SPI	ID	GIC Input Pin Name	Interrupt Request Source				
			Unit	Output Pin Name	Interrupt Description	Level/ Pulse	Active Level
SPI	264	IRQS[232]	IIC0	IICBTIA	Interrupt signal [Standard interrupt]	Pulse	Rise
	265	IRQS[233]	IIC1*2				
	266	IRQS[234]	IIC2				
	267	IRQS[235]	IIC3*2				
	268	IRQS[236]	IIC0	IICBTIS	Interrupt signal [NACK interrupt]	Pulse	Rise
	269	IRQS[237]	IIC1*2				
	270	IRQS[238]	IIC2				
	271	IRQS[239]	IIC3*2				
	272	IRQS[240]	UART0	INTR	URT interrupt signal	Level	High
	273	IRQS[241]	UART1 *2				
	274	IRQS[242]	USB*3	—	—	—	—
	275	IRQS[243]		—	—	—	—
	276	IRQS[244]		—	—	—	—
	277	IRQS[245]		—	—	—	—
	278	IRQS[246]		—	—	—	—
	279	IRQS[247]	—	Reserved	—	—	—
	280	IRQS[248]	—	Reserved	—	—	—
	281	IRQS[249]	—	Reserved	—	—	—
	282	IRQS[250]	—	Reserved	—	—	—
	283	IRQS[251]	ETHER *3	—	—	—	—
	284	IRQS[252]		—			
	285	IRQS[253]		—			
	286	IRQS[254]		—			
	287	IRQS[255]		—			
	288	IRQS[256]		—			
	289	IRQS[257]		—			
	290	IRQS[258]		—			
	291	IRQS[259]		—			
	292	IRQS[260]		—			
	293	IRQS[261]		—			
	294	IRQS[262]		—			
	295	IRQS[263]		—			
	296	IRQS[264]		—			
	297	IRQS[265]		—			
	298	IRQS[266]		—			
	299	IRQS[267]		—			
	300	IRQS[268]		—			
	301	IRQS[269]		—	—	—	—
	302	IRQS[270]		—			
	303	IRQS[271]		—			
	304	IRQS[272]		—			
	305	IRQS[273]		—	—	—	—
	306	IRQS[274]		—	—	—	—

Table 5.4-1 Interrupt list of GIC (GIC-400 for CA53) (8/10)

PPI/ SPI	ID	GIC Input Pin Name	Interrupt Request Source			Level/ Pulse	Active Level
			Unit	Output Pin Name	Interrupt Description		
SPI	307	IRQS[275]	ETHER *3	—	—	—	—
	308	IRQS[276]		—	—	—	—
	309	IRQS[277]		—	—	—	—
	310	IRQS[278]		—	—	—	—
	311	IRQS[279]		—	—	—	—
	312	IRQS[280]	—	Reserved	—	—	—
	313	IRQS[281]	—	Reserved	—	—	—
	314	IRQS[282]	—	Reserved	—	—	—
	315	IRQS[283]	—	Reserved	—	—	—
	316	IRQS[284]	—	Reserved	—	—	—
	317	IRQS[285]	—	Reserved	—	—	—
	318	IRQS[286]	—	Reserved	—	—	—
	319	IRQS[287]	—	Reserved	—	—	—
	320	IRQS[288]	—	Reserved	—	—	—
	321	IRQS[289]	—	Reserved	—	—	—
	322	IRQS[290]	—	Reserved	—	—	—
	323	IRQS[291]	—	Reserved	—	—	—
	324	IRQS[292]	—	Reserved	—	—	—
	325	IRQS[293]	—	Reserved	—	—	—
	326	IRQS[294]	—	Reserved	—	—	—
	327	IRQS[295]	—	Reserved	—	—	—
	328	IRQS[296]	—	Reserved	—	—	—
	329	IRQS[297]	—	Reserved	—	—	—
	330	IRQS[298]	—	Reserved	—	—	—
	331	IRQS[299]	—	Reserved	—	—	—
	332	IRQS[300]	—	Reserved	—	—	—
	333	IRQS[301]	—	Reserved	—	—	—
	334	IRQS[302]	—	Reserved	—	—	—
	335	IRQS[303]	—	Reserved	—	—	—
	336	IRQS[304]	—	Reserved	—	—	—
	337	IRQS[305]	—	Reserved	—	—	—
	338	IRQS[306]	—	Reserved	—	—	—
	339	IRQS[307]	—	Reserved	—	—	—
	340	IRQS[308]	—	Reserved	—	—	—
	341	IRQS[309]	PCIe*3	—	—	—	—
	342	IRQS[310]		—	—	—	—
	343	IRQS[311]		—	—	—	—
	344	IRQS[312]		—	—	—	—
	345	IRQS[313]		—	—	—	—
	346	IRQS[314]		—	—	—	—
	347	IRQS[315]		—	—	—	—
	348	IRQS[316]		—	—	—	—
	349	IRQS[317]		—	—	—	—
	350	IRQS[318]		—	—	—	—

Table 5.4-1 Interrupt list of GIC (GIC-400 for CA53) (9/10)

PPI/ SPI	ID	GIC Input Pin Name	Interrupt Request Source				
			Unit	Output Pin Name	Interrupt Description	Level/ Pulse	Active Level
SPI	351	IRQS[319]	PCIe*3	—	—	—	—
	352	IRQS[320]		—	—	—	—
	353	IRQS[321]		—	—	—	—
	354	IRQS[322]		—	—	—	—
	355	IRQS[323]		—	—	—	—
	356	IRQS[324]		—	—	—	—
	357	IRQS[325]		—	—	—	—
	358	IRQS[326]		—	—	—	—
	359	IRQS[327]		—	—	—	—
	360	IRQS[328]		—	—	—	—
	361	IRQS[329]		—	—	—	—
	362	IRQS[330]	—	Reserved	—	—	—
	363	IRQS[331]	—	Reserved	—	—	—
	364	IRQS[332]	ISP/ GPA*2,*3	—	—	—	—
	365	IRQS[333]	—	Reserved	—	—	—
	366	IRQS[334]	—	Reserved	—	—	—
	367	IRQS[335]	—	Reserved	—	—	—
	368	IRQS[336]	ISP/ GPA*2,*3	—	—	—	—
	369	IRQS[337]		—	—	—	—
	370	IRQS[338]		—	—	—	—
	371	IRQS[339]		—	—	—	—
	372	IRQS[340]		—	—	—	—
	373	IRQS[341]		—	—	—	—
	374	IRQS[342]		—	—	—	—
	375	IRQS[343]		—	—	—	—
	376	IRQS[344]	MTD*2,*3	—	—	—	—
	377	IRQS[345]	DRP-AI	NMLINT	Interrupt output signal	Level	High
	378	IRQS[346]		ERRINT	Error interrupt output signal	Level	High
	379	IRQS[347]		MAC_NMLINT	AI interrupt output signal	Level	High
	380	IRQS[348]		MAC_ERRINT	AI error interrupt output signal	Level	High
	381	IRQS[349]	JPG*2,*3	—	—	—	—
	382	IRQS[350]	—	Reserved	—	—	—
	383	IRQS[351]	VCD*2,*3	—	—	—	—
	384	IRQS[352]		—	—	—	—
	385	IRQS[353]	NAND*3	—	—	—	—
	386	IRQS[354]	eMMC*3	—	—	—	—
	387	IRQS[355]		—	—	—	—
	388	IRQS[356]	SDI0*3	—	—	—	—
	389	IRQS[357]		—	—	—	—
	390	IRQS[358]	SDI1*3	—	—	—	—
	391	IRQS[359]		—	—	—	—

Table 5.4-1 Interrupt list of GIC (GIC-400 for CA53) (10/10)

PPI/ SPI	ID	GIC Input Pin Name	Interrupt Request Source				
			Unit	Output Pin Name	Interrupt Description	Level/ Pulse	Active Level
SPI	392	IRQS[360]	—	Reserved	—	—	—
	393	IRQS[361]	—	Reserved	—	—	—
	394	IRQS[362]	—	Reserved	—	—	—
	395	IRQS[363]	—	Reserved	—	—	—
	396	IRQS[364]	—	Reserved	—	—	—
	397	IRQS[365]	—	Reserved	—	—	—
	398	IRQS[366]	—	Reserved	—	—	—
	399	IRQS[367]	—	Reserved	—	—	—
	400	IRQS[368]	PWM0*2	PWMINT	PWM interrupt request output signal	Level	High
	401	IRQS[369]	PWM1*2				
	402	IRQS[370]	PWM2*2				
	403	IRQS[371]	PWM3*2				
	404	IRQS[372]	PWM4*2				
	405	IRQS[373]	PWM5*2				
	406	IRQS[374]	PWM6*2				
	407	IRQS[375]	PWM7*2				
	408	IRQS[376]	PWM8				
	409	IRQS[377]	PWM9				
	410	IRQS[378]	PWM10				
	411	IRQS[379]	PWM11				
	412	IRQS[380]	PWM12				
	413	IRQS[381]	PWM13				
	414	IRQS[382]	PWM14				
	415	IRQS[383]	PWM15 *2				
	416	IRQS[384]	—	Reserved	—	—	—
	417	IRQS[385]	—	Reserved	—	—	—
	418	IRQS[386]	PMC	INT_PMC	PMC interrupt signal	Level	High
	419	IRQS[387]	—	Reserved	—	—	—
	420	IRQS[388]	DMAC*2	DMAERR	Error response (ERROR) interrupt	Level*1	High
	421	IRQS[389]	—	Reserved	—	—	—
	422	IRQS[390]	ISP/ GPA*2,*3	—	—	—	—
	423	IRQS[391]		—	—	—	—
	424	IRQS[392]	RAMA	EC7TIE1	ECC 1-bit error interrupt	Pulse	Rise
	425	IRQS[393]		EC7TIE2	ECC 2-bit error interrupt	Pulse	Rise
	426	IRQS[394]		EC7TIOVF	ECC error address capture overflow interrupt	Pulse	Rise

Note 1. Make sure to set the registers for the interrupt output mode and active level by referring to **Section 5.3, Interrupt Settings**.

Note 2. This register is for use with the ISP support package. Therefore, using this interrupt is prohibited.

Note 3. For more information, contact a Renesas Electronics sales representative.

Section 6 Address Map

This section describes the address space of this LSI.

6.1 Overall Address Map

Figure 6.1-1 shows the address map of this LSI, which has a 34-bit address space (16 GB).

Note that the upper 8 GB of the address space is a reserved area.

The address space contains the following areas.

- Slave area: 1-GB space from 00_8000_0000h to 00_BFFF_FFFFh
  The areas of the individual units are allocated.
  For details of the slave area, see **Section 6.2, Address Map Details**.
- PCIe area: 1-GB space from 00_C000_0000h to 00_FFFF_FFFFh
  (PCIe window access area)
- DDR area 1-S: 2-GB space from 00_0000_0000h to 00_7FFF_FFFFh*1
  (the lower 2 GB of addresses in the externally connected LPDDR4 memory)
- DDR area 1-M: 2-GB space from 01_0000_0000h to 01_7FFF_FFFFh*1
  (a mirrored area for DDR area 1-S, that is, for the lower 2 GB of addresses in the externally connected LPDDR4 memory)
- DDR area 2: 2-GB space from 01_8000_0000h to 01_FFFF_FFFFh*1
  (the upper 2 GB of addresses in the externally connected LPDDR4 memory)

Note 1. The following register must be set to suit the configuration of the externally connected LPDDR4 memory.
1) LPDDR4 memory size setting (set in the Sche_DeviceSize register of the ICB)
For details, see the section of ICB.

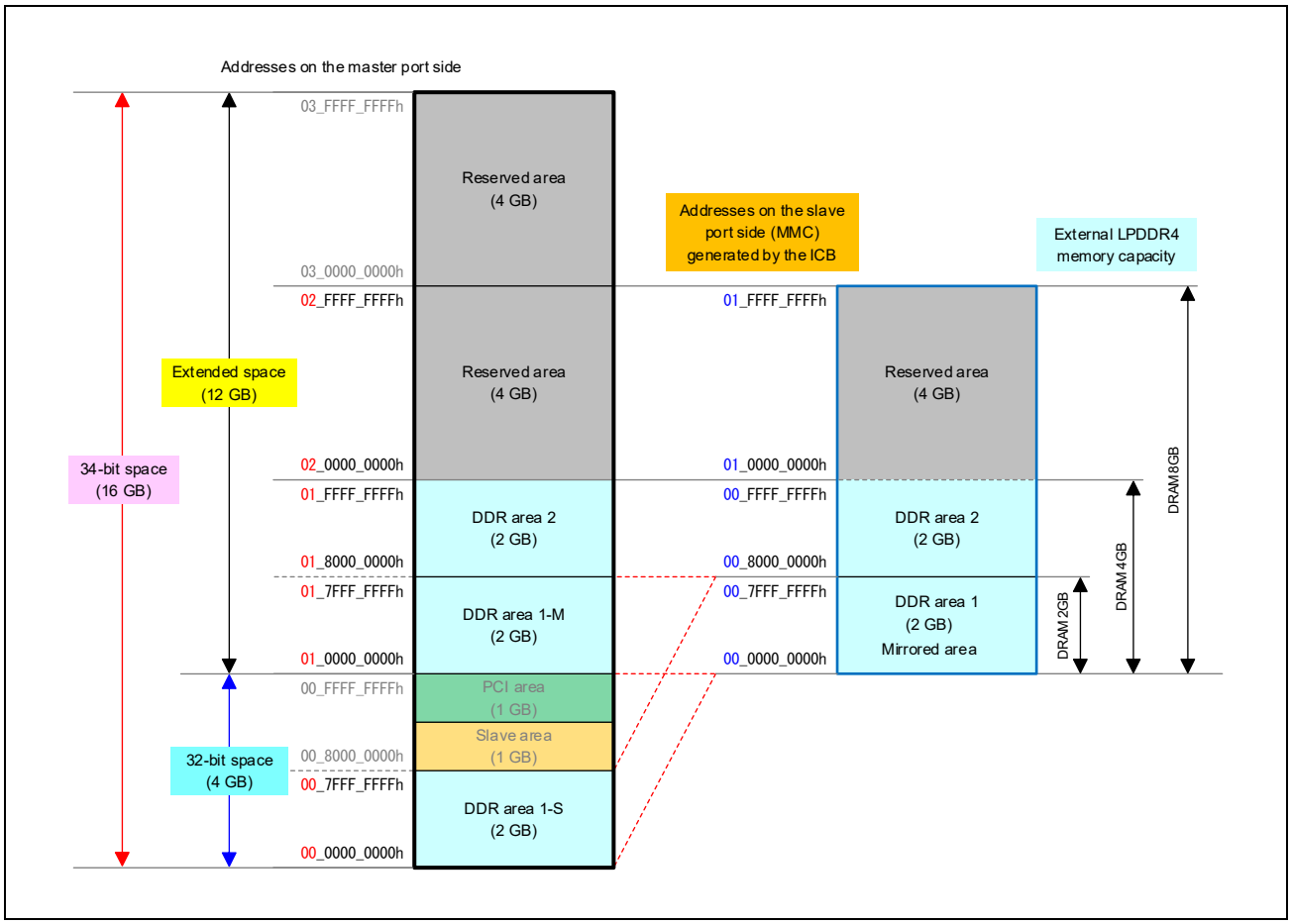


Figure 6.1-1 Overall Address Space

6.2 Address Map Details

Table 6.2-1 lists the allocation of the address spaces of this LSI to the units.

For those units which have multiple address spaces, the usage is indicated in the “Supplementary Note” column. The “Base Address Name” column indicates the correspondence with the port names of the AXI, AHB, and APB slaves allocated by the ICB.

Table 6.2-1 Address Allocation Details (1/5)

Base Address	Size*2		Unit	Base Address Name	Supplementary Note	Remarks
00_0000_0000h	2	Gbytes	MMC	—	LPDDR4 (less than 2 Gbytes)	—
00_8000_0000h	128	Kbytes	ROM	ROM_S0_base	ROM memory	—
00_8002_0000h	—	—	Reserved	—	—	*1
00_8010_0000h	200	Kbytes	RAMA	RAMA_S0_base	RAMA memory	—
00_8013_2000h	—	—	Reserved	—	—	*1
00_8020_0000h	64	Kbytes	NAND	NFI_S0_base	NAND DMA	—
00_8021_0000h	—	—	Reserved	—	—	*1
00_8200_0000h	512	Kbytes	GIC	GIC_S0_base	GIC register	—
00_8208_0000h	—	—	Reserved	—	—	*1
00_8210_0000h	2	Kbytes	DMAC	DMAA_S0_base	DMAC register	—
00_8210_0800h	—	—	Reserved	—	—	*1
00_8300_0000h	16	Mbytes	DRP-AI	DRPA_S0_base	DRP register	—
00_8400_0000h	4	Mbytes	DRP-AI	DRPA_S1_base	AI-MAC register	—
00_8440_0000h	—	—	Reserved	—	—	*1
00_8500_0000h	8	Kbytes	SDI0	SDI0_S0_base	SDI0 register	—
00_8500_2000h	—	—	Reserved	—	—	*1
00_8501_0000h	8	Kbytes	SDI1	SDI1_S0_base	SDI1 register	—
00_8501_2000h	—	—	Reserved	—	—	*1
00_8502_0000h	8	Kbytes	eMMC	EMM_S0_base	eMMC register	—
00_8502_2000h	—	—	Reserved	—	—	*1
00_8503_0000h	64	Kbytes	PCIe	PCI_S0_REG_base	PCIe link register	—
00_8504_0000h	—	—	Reserved	—	—	*1
00_8506_0000h	8	Kbytes	USB	USB_S0_base	USB host register	—
00_8506_2000h	—	—	Reserved	—	—	*1
00_8507_0000h	4	Kbytes	USB	USB_S1_base	USB peripheral register	—
00_8507_1000h	—	—	Reserved	—	—	*1
00_8600_0000h	16	Mbytes	CST	CST_S1_base	CoreSight STM-500	—
00_8700_0000h	—	—	Reserved	—	—	*1
00_9290_0000h	4	Kbytes	VCD	VCD_S0_base	VCD VLC register	—
00_9290_1000h	—	—	Reserved	—	—	*1
00_9294_0000h	4	Kbytes	VCD	VCD_S1_base	VCD CE register	—
00_9294_1000h	—	—	Reserved	—	—	*1
00_9298_0000h	4	Kbytes	VCD	VCD_S2_base	VCD FCP register	—
00_9298_1000h	—	—	Reserved	—	—	*1
00_92C0_0000h	16	Kbytes	GRP	GRP_S0_base	GRP register	—
00_92C0_4000h	—	—	Reserved	—	—	*1
00_92F4_0000h	256	Bytes	RAMA	RAMA_S1_base	RAMA register	—
00_92F4_0100h	—	—	Reserved	—	—	*1

Table 6.2-1 Address Allocation Details (2/5)

Base Address	Size*2		Unit	Base Address Name	Supplementary Note	Remarks
00_9800_0000h	128	Mbytes	ICB	ICB_S0_base	ICB register	—
00_A000_0000h	32	Mbytes	DDI	DDI_S0_base	DDI register	—
00_A200_0000h	32	Kbytes	MMC	MMC_S1_base	MMC register	—
00_A200_8000h	—	—	Reserved	—	—	*1
00_A300_0000h	64	Kbytes	NAND	NFI_S1_base	NAND register	—
00_A301_0000h	—	—	Reserved	—	—	*1
00_A330_0000h	2	Kbytes	ETHER	ETH_S0_base	ETHER register	—
00_A330_0800h	—	—	Reserved	—	—	*1
00_A350_0000h	4	Kbytes	CPG	CPG_S0_base	CPG register	—
00_A350_1000h	—	—	Reserved	—	—	*1
00_A360_0000h	4	Kbytes	PMC	PMC_S0_base	PMC register	—
00_A360_1000h	—	—	Reserved	—	—	*1
00_A3A0_0000h	4	Kbytes	LCI	LCI_S0_base	LCI Link register	—
00_A3A0_1000h	—	—	Reserved	—	—	*1
00_A3A8_0000h	1	Kbyte	LCI	LCI_S1_base	LCI PHY register	—
00_A3A8_0400h	—	—	Reserved	—	—	*1
00_A3B0_0000h	4	Kbytes	HDMI	HMI_S0_base	HDMI Link register	—
00_A3B0_1000h	—	—	Reserved	—	—	*1
00_A3B8_0000h	256	Bytes	HDMI	HMI_S1_base	HDMI PHY register	—
00_A3B8_0100h	—	—	Reserved	—	—	*1
00_A3D0_0000h	4	Kbytes	CIF	CIF_S0_base	CIF register	—
00_A3D0_1000h	—	—	Reserved	—	—	*1
00_A3F0_0000h	8	Kbytes	SYC	SYC_S0_base	SYC register	—
00_A3F0_2000h	4	Kbytes	CA53	CA53_S0_base	CA53 register	—
00_A3F0_3000h	1	Kbyte	SYS	SYS_S0_base	SYS register	—
00_A3F0_3400h	—	—	Reserved	—	—	*1
00_A3F3_0000h	64	Kbytes	DCU	DCU_S0_base	—	—
00_A3F4_0000h	—	—	Reserved	—	—	*1
00_A3F5_0000h	128	Bytes	TSU0	TSU0_S0_base	TSU0 register	—
00_A3F5_0080h	—	—	Reserved	—	—	*1
00_A3F6_0000h	128	Bytes	TSU1	TSU1_S0_base	TSU1 register	—
00_A3F6_0080h	—	—	Reserved	—	—	*1
00_A3F7_0000h	2	Kbytes	PCIe	PCI_S1_base	PCIe PHY (analog) register	—
00_A3F7_0800h	—	—	Reserved	—	—	*1
00_A3F8_0000h	2	Kbytes	PCIe	PCI_S2_base	PCIe PHY (logic) register	—
00_A3F8_0800h	—	—	Reserved	—	—	*1
00_A3F9_0000h	4	Kbytes	USB	USB_S2_base	USB test (phy) register	—
00_A3F9_1000h	—	—	Reserved	—	—	*1
00_A400_0000h	128	Bytes	TIM0	TIM0_S0_base	TIM0 register	—
00_A400_0080h	128	Bytes	TIM1	TIM1_S0_base	TIM1 register	—
00_A400_0100h	128	Bytes	TIM2	TIM2_S0_base	TIM2 register	—
00_A400_0180h	128	Bytes	TIM3	TIM3_S0_base	TIM3 register	—
00_A400_0200h	128	Bytes	TIM4	TIM4_S0_base	TIM4 register	—
00_A400_0280h	128	Bytes	TIM5	TIM5_S0_base	TIM5 register	—
00_A400_0300h	128	Bytes	TIM6	TIM6_S0_base	TIM6 register	—

Table 6.2-1 Address Allocation Details (3/5)

Base Address	Size*2		Unit	Base Address Name	Supplementary Note	Remarks
00_A400_0380h	128	Bytes	TIM7	TIM7_S0_base	TIM7 register	—
00_A400_0400h	128	Bytes	TIM8	TIM8_S0_base	TIM8 register	—
00_A400_0480h	128	Bytes	TIM9	TIM9_S0_base	TIM9 register	—
00_A400_0500h	128	Bytes	TIM10	TIM10_S0_base	TIM10 register	—
00_A400_0580h	128	Bytes	TIM11	TIM11_S0_base	TIM11 register	—
00_A400_0600h	128	Bytes	TIM12	TIM12_S0_base	TIM12 register	—
00_A400_0680h	128	Bytes	TIM13	TIM13_S0_base	TIM13 register	—
00_A400_0700h	128	Bytes	TIM14	TIM14_S0_base	TIM14 register	—
00_A400_0780h	128	Bytes	TIM15	TIM15_S0_base	TIM15 register	—
00_A400_0800h	128	Bytes	TIM16	TIM16_S0_base	TIM16 register	—
00_A400_0880h	128	Bytes	TIM17	TIM17_S0_base	TIM17 register	—
00_A400_0900h	128	Bytes	TIM18	TIM18_S0_base	TIM18 register	—
00_A400_0980h	128	Bytes	TIM19	TIM19_S0_base	TIM19 register	—
00_A400_0A00h	128	Bytes	TIM20	TIM20_S0_base	TIM20 register	—
00_A400_0A80h	128	Bytes	TIM21	TIM21_S0_base	TIM21 register	—
00_A400_0B00h	128	Bytes	TIM22	TIM22_S0_base	TIM22 register	—
00_A400_0B80h	128	Bytes	TIM23	TIM23_S0_base	TIM23 register	—
00_A400_0C00h	128	Bytes	TIM24	TIM24_S0_base	TIM24 register	—
00_A400_0C80h	128	Bytes	TIM25	TIM25_S0_base	TIM25 register	—
00_A400_0D00h	128	Bytes	TIM26	TIM26_S0_base	TIM26 register	—
00_A400_0D80h	128	Bytes	TIM27	TIM27_S0_base	TIM27 register	—
00_A400_0E00h	128	Bytes	TIM28	TIM28_S0_base	TIM28 register	—
00_A400_0E80h	128	Bytes	TIM29	TIM29_S0_base	TIM29 register	—
00_A400_0F00h	128	Bytes	TIM30	TIM30_S0_base	TIM30 register	—
00_A400_0F80h	128	Bytes	TIM31	TIM31_S0_base	TIM31 register	—
00_A400_1000h	—	—	Reserved	—	—	*1
00_A401_0000h	128	Bytes	PWM0	PWM0_S0_base	PWM0 register	—
00_A401_0080h	128	Bytes	PWM1	PWM1_S0_base	PWM1 register	—
00_A401_0100h	128	Bytes	PWM2	PWM2_S0_base	PWM2 register	—
00_A401_0180h	128	Bytes	PWM3	PWM3_S0_base	PWM3 register	—
00_A401_0200h	128	Bytes	PWM4	PWM4_S0_base	PWM4 register	—
00_A401_0280h	128	Bytes	PWM5	PWM5_S0_base	PWM5 register	—
00_A401_0300h	128	Bytes	PWM6	PWM6_S0_base	PWM6 register	—
00_A401_0380h	128	Bytes	PWM7	PWM7_S0_base	PWM7 register	—
00_A401_0400h	128	Bytes	PWM8	PWM8_S0_base	PWM8 register	—
00_A401_0480h	128	Bytes	PWM9	PWM9_S0_base	PWM9 register	—
00_A401_0500h	128	Bytes	PWM10	PWM10_S0_base	PWM10 register	—
00_A401_0580h	128	Bytes	PWM11	PWM11_S0_base	PWM11 register	—
00_A401_0600h	128	Bytes	PWM12	PWM12_S0_base	PWM12 register	—
00_A401_0680h	128	Bytes	PWM13	PWM13_S0_base	PWM13 register	—
00_A401_0700h	128	Bytes	PWM14	PWM14_S0_base	PWM14 register	—
00_A401_0780h	128	Bytes	PWM15	PWM15_S0_base	PWM15 register	—
00_A401_0800h	—	—	Reserved	—	—	*1
00_A402_0000h	128	Bytes	CSI0	CSI0_S0_base	CSI0 register	—
00_A402_0080h	128	Bytes	CSI1	CSI1_S0_base	CSI1 register	—

Table 6.2-1 Address Allocation Details (4/5)

Base Address	Size*2		Unit	Base Address Name	Supplementary Note	Remarks
00_A402_0100h	128	Bytes	CSI2	CSI2_S0_base	CSI2 register	—
00_A402_0180h	128	Bytes	CSI3	CSI3_S0_base	CSI3 register	—
00_A402_0200h	128	Bytes	CSI4	CSI4_S0_base	CSI4 register	—
00_A402_0280h	128	Bytes	CSI5	CSI5_S0_base	CSI5 register	—
00_A402_0300h	—	—	Reserved	—	—	*1
00_A403_0000h	128	Bytes	IIC0	IIC0_S0_base	IIC0 register	—
00_A403_0080h	128	Bytes	IIC1	IIC1_S0_base	IIC1 register	—
00_A403_0100h	128	Bytes	IIC2	IIC2_S0_base	IIC2 register	—
00_A403_0180h	128	Bytes	IIC3	IIC3_S0_base	IIC3 register	—
00_A403_0200h	—	—	Reserved	—	—	*1
00_A404_0000h	128	Bytes	UART0	URT0_S0_base	UART0 register	—
00_A404_0080h	128	Bytes	UART1	URT1_S0_base	UART1 register	—
00_A404_0100h	—	—	Reserved	—	—	*1
00_A405_0000h	128	Bytes	WDT0	WDT0_S0_base	WDT0 register	—
00_A405_0080h	128	Bytes	WDT1	WDT1_S0_base	WDT1 register	—
00_A405_0100h	—	—	Reserved	—	—	*1
00_A600_0000h	4	Mbytes	CST	CST_S0_base	CoreSight DebugAPB	—
00_A640_0000h	—	—	Reserved	—	—	*1
00_A702_0000h	64	Kbytes	AUI	AUI_S0_base	—	
00_A703_0000h	—	—	Reserved	—	—	*1
00_A705_0000h	64	Kbytes	MTR	MTR_S0_base	—	—
00_A706_0000h	64	Kbytes	ADCA	ADCA_S0_base	—	—
00_A707_0000h	64	Kbytes	ADCB	ADCB_S0_base	—	—
00_A708_0000h	—	—	Reserved	—	—	*1
00_A70A_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A70B_0000h	—	—	Reserved	—	—	*1
00_A800_0000h	64	Kbytes	JPG	JPG_S0_base	JPG register	—
00_A801_0000h	—	—	Reserved	—	—	*1
00_A803_0000h	64	Kbytes	STG	STG_S0_base	—	—
00_A804_0000h	—	—	Reserved	—	—	*1
00_A80B_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A80C_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A80D_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A80E_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A80F_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A810_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A811_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A812_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A813_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A814_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A815_0000h	—	—	Reserved	—	—	*1
00_A817_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A818_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A819_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A81A_0000h	64	Kbytes	ISP/GPA	—	—	—

Table 6.2-1 Address Allocation Details (5/5)

Base Address	Size*2		Unit	Base Address Name	Supplementary Note	Remarks
00_A81B_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A81C_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A81D_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A81E_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A81F_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A820_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A821_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A822_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A823_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A824_0000h	—	—	Reserved	—	—	*1
00_A825_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A826_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A827_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A828_0000h	—	—	Reserved	—	—	*1
00_A834_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A835_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A836_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A837_0000h	—	—	Reserved	—	—	*1
00_A838_0000h	64	Kbytes	ISP/GPA	—	—	—
00_A839_0000h	64	Kbytes	MTD	FCD_S0_base	—	—
00_A83A_0000h	—	—	Reserved	—	—	*1
00_B600_0000h	256	Kbytes	RAMB0	—	RAMB0 memory	—
00_B604_0000h	256	Kbytes	RAMB1	—	RAMB1 memory	—
00_B608_0000h	256	Kbytes	RAMB2	—	RAMB2 memory	—
00_B60C_0000h	256	Kbytes	RAMB3	—	RAMB3 memory	—
00_B610_0000h	—	—	Reserved	—	—	*1
00_B620_0000h	64	Kbytes	ISP/GPA	—	—	—
00_B621_0000h	64	Kbytes	ISP/GPA	—	—	—
00_B622_0000h	64	Kbytes	ISP/GPA	—	—	—
00_B623_0000h	64	Kbytes	ISP/GPA	—	—	—
00_B624_0000h	64	Kbytes	ISP/GPA	—	—	—
00_B625_0000h	2	Kbytes	PFC	PFC_S0_base	PFC register	—
00_B625_0800h	—	—	Reserved	—	—	*1
00_C000_0000h	1	Gbyte	PCIe	PCI_S0_base	PCIe window	—
01_0000_0000h	8	Gbytes	MMC	—	LPDDR4 (more than 2 Gbytes)	—
02_0000_0000h	—	—	Reserved	—	—	*1

Note 1. Access to the reserved address areas is prohibited.

Note 2. If a slave unit does not have an address range equivalent to the allocated size, the remainder of the area is viewed as a mirrored area. Access to the mirrored area is prohibited.

6.3 Access to 34-Bit Address Space

Table 6.3-1 lists the classification of the areas accessible by the units which have a master port.

The LCI unit can only access a 32-bit address space (from 0000_0000h to FFFF_FFFFh).

The units other than LCI can access a 34-bit address space (from 00_0000_0000h to 01_FFFF_FFFFh).

Note that bank switching will allow access to DRP-AI, eMMC, SDI0, SDI1, ETHER, PCIe, USB, VCD, GRP, and DMAC. The units which require bank switching must access the address space over 32 bits by setting the register of SYS (bank switching is described in the next section).

Table 6.3-1 Classification of Areas Accessible by the Units

Unit Category	Target Unit
Units which can access a 34-bit space (00_0000_0000h to 01_FFFF_FFFFh)	CA53, CST, NAND **[Units which require bank switching]** DRP-AI, eMMC, SDI0, SDI1, ETHER, PCIe, USB, VCD, GRP, DMAC
Units which can only access a 32-bit space (0000_0000h to FFFF_FFFFh)	LCI

6.4 Access by Bank Switching

The address width of the master port of the target units listed below is 32 bits (4-GB address spaces).

Therefore, in this LSI, to make the 34-bit address space (16-GB address space) accessible, extended addresses (bank addresses) are provided by using the two higher-order bits for access through bank switching.

The bank address is switched by using the bank address switching register in SYS.

Table 6.4-1 lists the correspondence between the bank addresses and the address spaces.

For the bank address switching register in SYS, see the section of SYS.

Target units: DRP-AI, eMMC, SDI0, SDI1, ETHER, PCIe, USB, VCD, GRP, DMAC

Table 6.4-1 Correspondence between the Bank Addresses and the Address Spaces

Bank Address (Two Extension Bits)	Address Space
11b	03_0000_0000h to 03_FFFF_FFFFh (4 GB) Setting prohibited
10b	02_0000_0000h to 02_FFFF_FFFFh (4 GB) Setting prohibited
01b	01_0000_0000h to 01_FFFF_FFFFh (4 GB)
00b	00_0000_0000h to 00_FFFF_FFFFh (4 GB)

CAUTION

Any access that spans 32-bit address boundaries is prohibited.

The usage of the value of the bank address switching register in SYS (the address extension method) differs between the DMAC and other units. **Figure 6.4-1** and **Table 6.4-2** give summaries of address extension.

Table 6.4-2 Summary of the 34-Bit Address Extension Method

Address Extension Method	Target Unit and Summary of the Address Extension Method
Address extension 1	DRP-AI, eMMC, SDI0, SDI1, ETHER, PCIe, USB, VCD, GRP ⇨ The address is extended by the output of two bank address bits from SYS to ICB.
Address extension 2	DMAC ⇨ The address is extended by the output of two bank address bits from SYS to DMAC.

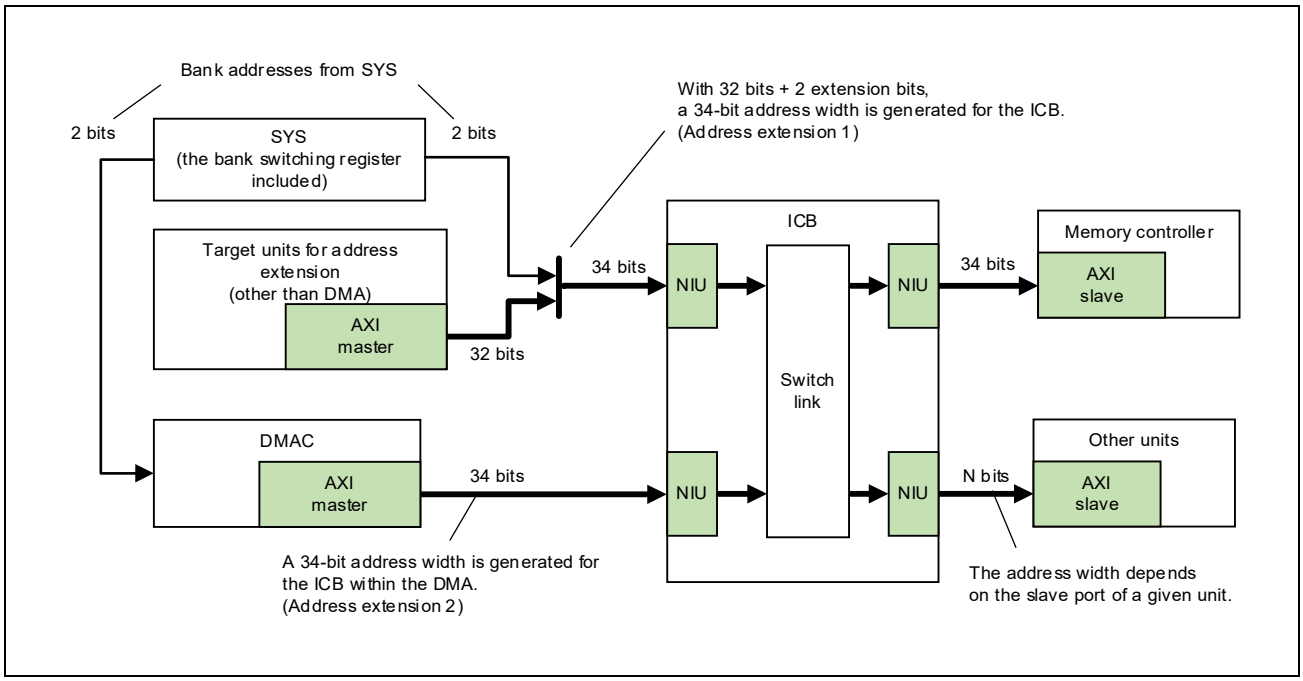


Figure 6.4-1 Schematic Diagram of the 34-Bit Address Extension Method

To switch the bank address, follow the procedure below before starting access by the master port.

For the bank address switching register in SYS, see the section of SYS.

[Bank Address Switching Procedure in Outline]

Step 1. Set the bank address switching register of SYS.*1

Step 2. Wait for at least 50 ns.*2

Step 3. Start access with the set bank address.

Note 1. If the target unit is DRP-AI, eMMC, SDI0, SDI1, ETHER, PCIe, USB, or VCD, or GRP, change the bank address while the target master port is stopped or idle, i.e., while it is not proceeding with access through buses. If the target unit is DMAC, change the bank address while operation of the target channels is stopped.

Note 2. The bank switching register requires 50 ns from writing until the setting is reflected.

6.4.1 Address Extension 1

For DRP-AI, eMMC, SDI0, SDI1, ETHER, PCIe, USB, and VCD, and GRP, the two bank address bits from SYS are extended by the higher-order bits [33:32] from the 32 address bits [31:0] of each master port to configure the address bus of the ICB. See **Figure 6.4-1** for the schematic diagram of address extension 1.

The following describes an example of the bank address switching procedure for the unit for address extension 1.

■ **For ETHER**

Step 1. Change the operating mode of ETHER to reset mode.

Step 2. Set the bank address in bits 1 and 0 of the PERI1_BANK register in SYS.

Step 3. Read the register value set in step 2 to check that the value has been reflected.

Step 4. Make initial settings for ETHER (“X” of register values should be specified by the user).

Poll the CSR register (00Ch) until it becomes 0000_0000h (reset mode).

Write 0000_0001h to the CCC register (set to config mode).

Poll the CSR register (00Ch) until it becomes 0000_0002h (config mode).

Write 0000_000Xh to the CXR2C register (52Ch).

Write 0000_2000h to the CXR2A register (508h) (set the maximum frame size to 8 KB).

Write 0000_XXXXh to the CXR71 register (554h).

Write XXXX_XXXXh to the CXR24 register (5C0h).

Write 0000_XXXXh to the CXR25 register (5C8h).

Write 0000_00XXh to the CXR22 register (518h).

Write 0000_000Xh to the CXR2D register (5B0h).

Write XXXX_XXXXh to the DBAT register (004h).

Write XXXX_00XXh to the RCR register (090h).

Write 0FFC_0FFCh to the RTC register (0B4h) (set the maximum reception frame size to 4092 bytes).

Write 000X_0X0Xh to the CIE register (384h).

Write 0000_XXXXh to the DIE register (450h).

Write 0000_0XXXh to the EIE register (458h).

Write 000X_XXXXh to the RIE0 register (460h).

Write X00X_XXXXh to the RIE1 register (468h).

Write X00X_XXXXh to the RIE2 register (470h).

Write 000X_0X0Xh to the TIE register (478h).

Write 000X_XXXXh to the RIE3 register (488h).

Write 0X0X_00X2h to the CCC register (000h) (set to operation mode).

Write 0XXX_XXXXh to the CXR20 register (500h).

Write 000X_0X03h to the TCCR register (304h).

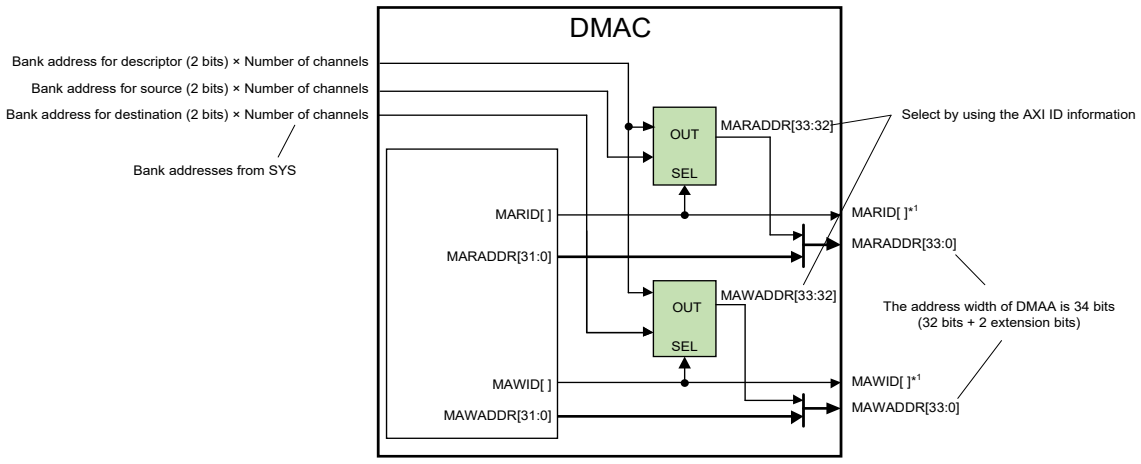
6.4.2 Address Extension 2

The DMAC is provided with an address width extension function within the unit by using the value of the bank address switching register of SYS, which realizes extension into the 34-bit space (16 GB).

The bank address from SYS is appended to the 32-bit addresses output by the general-purpose DMAC of DMA for output to the ICB in the 34-bit address width.

The bank address switching address register of SYS provides three types of bank address, respectively for the descriptor, source, and destination per DMAC number and channel. The descriptor, source, and destination areas can be set individually in each 4-GB space by selecting the required bank address of the two higher-order bits in utilizing the AXI ID information when a given channel proceeds with access through the AXI bus.

Figure 6.4-2 shows a schematic of the address extension function of the DMAC.



Note 1. The bit width of MARID and MAWID depends on the configuration of the on-chip DMAC.

Figure 6.4-2 Schematic of Address Bus Width Extension (Address Extension 2)

Table 6.4-3 lists the AXI ID information for access by the DMAC through the AXI bus.

Table 6.4-4 describes how a given channel selects the bank address by using the AXI ID information.

Table 6.4-3 AXI ID Information of DMAC

Unit Name	Marcro Name	AXI ID[4]	AXI ID[3]	AXI ID[2]	AXI ID[1]	AXI ID[0]
DMAC	DMAC0	Descriptor access/ DMA transfer	Channel number of DMAC0			0
	DMAC1	Descriptor access/ DMA transfer	Channel number of DMAC1			1

Note: The DMAC includes two units. DMAC0 and DMAC1 have eight channels respectively, 16 channels in total.

Table 6.4-4 DMAC Bank Address Selection Specification

Unit Name	Source Reading Descriptor Reading	Destination Writing Descriptor Write-Back
DMAC0, DMAC1	The two higher-order bits of MARADDR are selected by AXI ID[4:1]	The two higher-order bits of MAWADDR are selected by AXI ID[4:1]

The following describes the selection of bank addresses with the AXI ID information, taking DMAC0 as an example.

The bank addresses listed below are input from SYS to DMAC0 (the following are the internal pin names of DMAC0).

When a given channel proceeds with access through AXI, the one higher-order bits of MARADDR are selected by AXI ID[4:1] for source reading and descriptor reading, and the two higher-order bits of MAWADDR are selected by AXI ID[4:1] for destination writing and descriptor write-back.

Table 6.4-5 Selection of MARADDR and MAWADDR for DMAC0

AXI ID[4]	AXI ID[3:1]	Selected MARADDR Higher-Order Address	Selected MAWADDR Higher-Order Address
0b	000b	Channel 0 source address	Channel 0 destination address
0b	001b	Channel 1 source address	Channel 1 destination address
0b	010b	Channel 2 source address	Channel 2 destination address
0b	011b	Channel 3 source address	Channel 3 destination address
0b	100b	Channel 4 source address	Channel 4 destination address
0b	101b	Channel 5 source address	Channel 5 destination address
0b	110b	Channel 6 source address	Channel 6 destination address
0b	111b	Channel 7 source address	Channel 7 destination address
1b	000b	Channel 0 descriptor address	Channel 0 descriptor address
1b	001b	Channel 1 descriptor address	Channel 1 descriptor address
1b	010b	Channel 2 descriptor address	Channel 2 descriptor address
1b	011b	Channel 3 descriptor address	Channel 3 descriptor address
1b	100b	Channel 4 descriptor address	Channel 4 descriptor address
1b	101b	Channel 5 descriptor address	Channel 5 descriptor address
1b	110b	Channel 6 descriptor address	Channel 6 descriptor address
1b	111b	Channel 7 descriptor address	Channel 7 descriptor address

The following describes an example of the bank address switching procedure for DMAC.

Step 1. Check that bit 0 (EN) and bit 2 (TACT) in the CHSTAT_n register of DMAC are 0b.
(n = channel for which the bank address is to be changed)

Step 2. Set the bank address in the SYS_DMAAm_CHn_BANK register.
(m = 0, 1; n = 01, 23, 45, 67)

Step 3. Read the register value set in step 2 to check that the value has been reflected.

Step 4. Make transfer settings for the DMAC unit and channels for which the bank address has been changed and start DMA transfer.

For details of DMA transfer control, see the section of DMAC.

For details of the SYS registers, see the section of SYS.

Section 7 Bus Structure

This section describes the bus structure of this LSI.

For details on the functions of the interconnect bus (ICB), see the ICB section.

7.1 Bus Connection Configuration

Figure 7.1-1 shows the connection configuration of the ICB and various units.

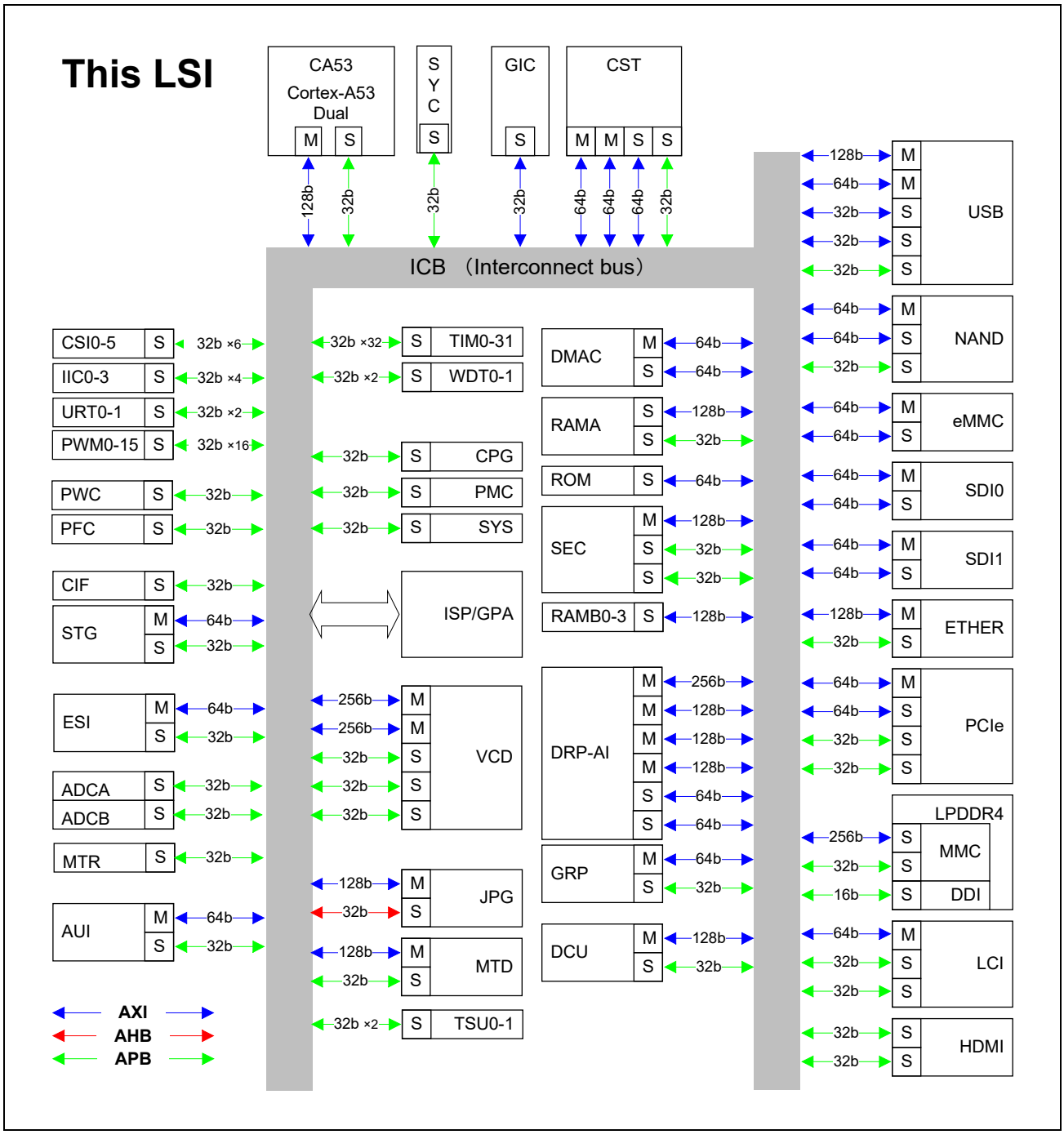


Figure 7.1-1 Bus Connection Configuration

7.2 Access Path

Figure 7.2-1 shows the access path between masters and slaves of the units included in this LSI.

Master/Slave Access Table

✓: Access path available
No mark: No access path

Unit Name	Slave Port Name	Unit Name	CA53	CST	CST	DMAC	PCIe	SDI0	SDI1	eMMC	NAND	USB	USB	ETHER	DRP-AI				VCD		GRP	LCI	JPG	DCU	AUI	STG	MTD	ESI	ISP/GPA
		Master Port Name	CA53_M0	CST_M0	CST_M1	DMAA_M0	PCI_M0	SDI0_M0	SDI1_M0	EMM_M0	NFI_M0	USB_M0	USB_M1	ETH_M0	DRPA_M0	DRPA_M1	DRPA_M2	DRPA_M3	VCD_M0R	VCD_M0W	GRP_M0	LCI_M0	JPG_M0	DCI_M0	AUI_M0	STG_M0	FCD_M0	SDT_M0	ISP/GPA related
						*4													*2	*2	*2	*2	*2	*2	*2	*2	*2	*2	*2
CA53	CA53_S0		✓	✓																									
SYC	SYC_S0		✓	✓																									
GIC	GIC_S0		✓	✓																									
CST	CST_S0		✓	✓																									
CST	CST_S1		✓																										
TIM0 to TIM31	TIM0_S0 to TIM31_S0	*3	✓	✓																									
PWM0 to PWM15	PWM0_S0 to PWM15_S0	*3	✓	✓																									
CSI0 to CSI5	CSI0_S0 to CSI5_S0	*3	✓	✓		✓																							
IIC0 to IIC3	IIC0_S0 to IIC3_S0	*3	✓	✓																									
URT0, URT1	URT0_S0 to URT1_S0	*3	✓	✓		✓																							
WDT0 to WDT1	WDT0_S0 to WDT1_S0		✓	✓																									
DMAC	DMAA_S0	*3	✓	✓																									
RAMA	RAMA_S0		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓												✓	✓	✓	✓
RAMA	RAMA_S1		✓	✓																									
ROM	ROM_S0		✓	✓		✓																							
RAMB0 to RAMB3	RAMB0_S0 to RAMB3_S0		✓	✓	✓	✓									✓	✓	✓	✓							✓	✓	✓	✓	✓
CPG	CPG_S0		✓	✓																									
PMC	PMC_S0		✓	✓																									
PFC	PFC_S0		✓	✓											✓														
SYS	SYS_S0		✓	✓																									
USB	USB_S0		✓	✓																									
USB	USB_S1		✓	✓																									
USB	USB_S2		✓	✓																									
NAND	NFI_S0		✓	✓		✓																							
NAND	NFI_S1		✓	✓																									
eMMC	EMM_S0		✓	✓																									
SDI0	SDI0_S0		✓	✓																									
SDI1	SDI1_S0		✓	✓																									
ETHER	ETH_S0		✓	✓																									
PCIe	PCI_S0 / PCI_S0:reg		✓	✓	✓																								
PCIe	PCI_S1		✓	✓																									
PCIe	PCI_S2		✓	✓																									
LPDDR4	MMC_S0		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LPDDR4	MMC_S1_REG		✓	✓																									
LPDDR4	DDI_S0_REG		✓	✓																									
ICB	ICB_S0		✓	✓																									
DRP-AI	DRPA_S0		✓	✓																									
DRP-AI	DRPA_S1		✓	✓																									
GRP	GRP_S0	*1	✓	✓																									
VCD	VCD_S0	*1	✓	✓																									
VCD	VCD_S1	*1	✓	✓																									
VCD	VCD_S2	*1	✓	✓																									
JPG	JPG_S0	*1	✓	✓																									
MTD	FCD_S0	*1	✓	✓																									
TSU0 to TSU1	TSU0_S0 to TSU1_S0	*1	✓	✓																									
ESI	SDT_S0	*1	✓	✓											✓														
AUI	AUI_S0	*1	✓	✓																									
MTR	MTR_S0	*1	✓	✓																									
ADCA	ATGA_S0	*1	✓	✓																									
ADCB	ATGB_S0	*1	✓	✓																									
DCU	DCI_S0	*1	✓	✓																									
LCI	LCI_S0	*1	✓	✓																									
LCI	LCI_S1	*1	✓	✓																									
HMI	HMI_S0	*1	✓	✓																									
HMI	HMI_S1	*1	✓	✓																									
CIF	CIF_S0	*1	✓	✓																									
STG	STG_S0	*1	✓	✓																									
ISP/GPA	ISP/GPA related	*1	✓	✓																									

(*Continuation of the previous page*)

Note 1. Access not listed in **Figure 7.2-1** is prohibited.

Note 2. The following accesses shown in **Figure 7.2-1** are for the ISP support package and should not be used.
- — Access to the slave port with *1
- — Access from the master port with *2
- — Access to the slave ports of the following channels with *3
  - TIM: Total of 16 channels, ch. 0 to ch. 7 and ch. 24 to ch. 31
  - PWM: Total of 8 channels, ch. 0 to ch. 7
  - WDT: Ch. 1
  - CSI: Total of 4 channels, ch. 1 to ch. 3, ch. 5
  - IIC: Total of 2 channels, ch. 1 and ch. 3
  - UART: Ch. 1
  - DMAC: Total of 8 channels, DMAC1 ch. 0 to ch. 7
- — Access from the master ports of the following channels with *4
  - DMAC: Total of 8 channels, DMAC1 ch. 0 to ch. 7

Figure 7.2-1 Bus Access Path

7.3 Master and Slave Port Specifications

For details on the master port and slave port specifications, see the section of ICB.

Section 8 Power Supply

This section describes the power supply of this LSI.

8.1 External Power Supply Pins

The external power supplies of this LSI are described below. The following five power supply systems require external power sources.

- RTC power supplies: Power supplies for the RTC (1.5 V, 0.8 V)
- PWC power supplies: Power supplies for the PWC (1.8 V, 0.8 V)
- Internal power supplies: Power supplies for the internal logic cells and SRAM and ROM (0.8 V)
- I/O power supplies: Power supplies for the I/O cells (1.8 V / 3.3 V)
- IP power supplies: Power supplies for the IP cores (0.8 V / 1.1 V / 1.2 V / 1.8 V / 3.3 V)

Note that the individual external power supplies of this LSI need to be turned on and off in specified sequences and these are controlled by the hardware of the PWC. **Figure 8.1-1** is a schematic view of the control of external power supplies by the PWC. For details, see the section of PWC.

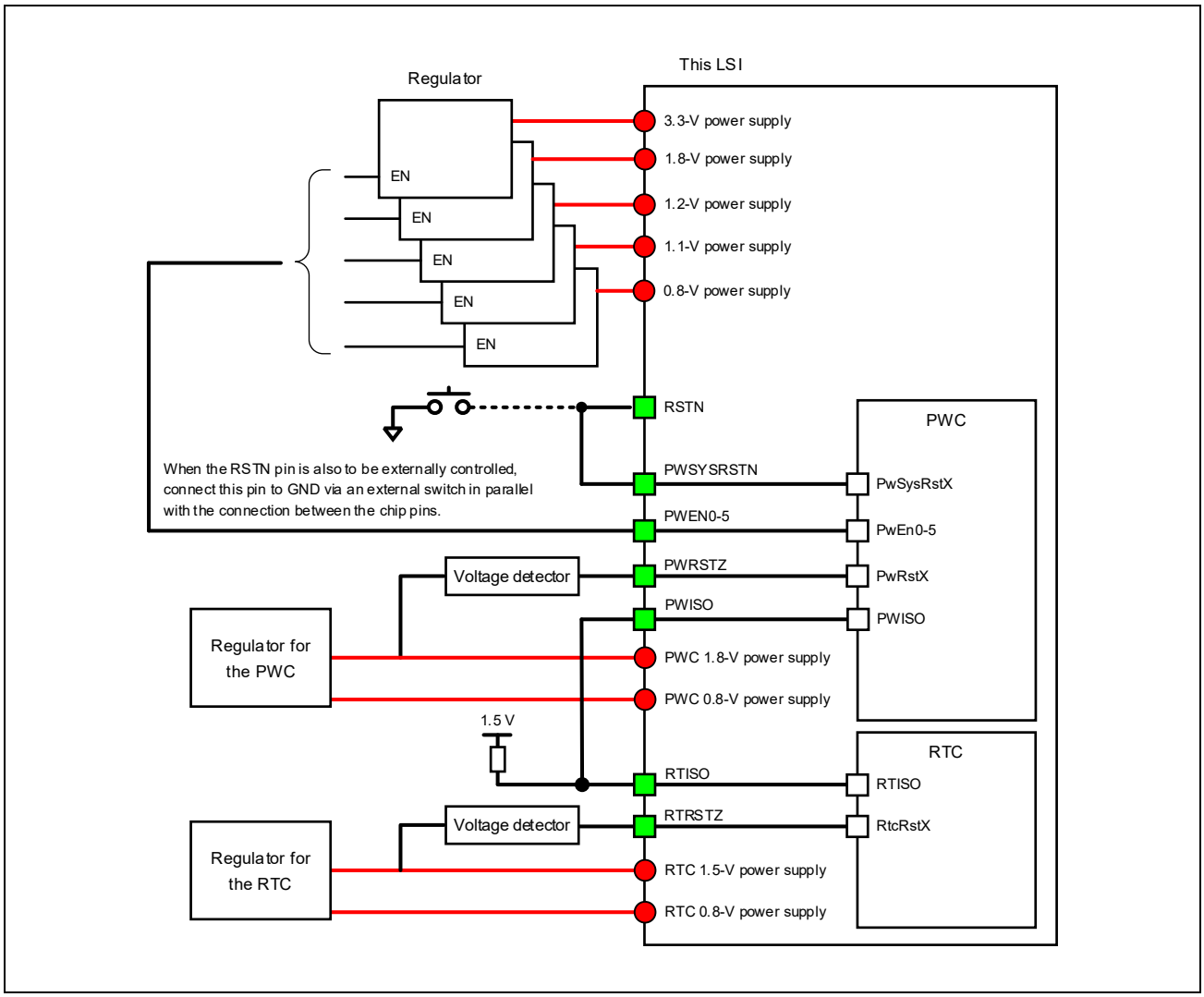


Figure 8.1-1 Schematic View of the Control of External Power Supplies by the PWC

NOTE

When the RSTN pin is to be controlled externally from the LSI, connect the PWSYSRSTN pin and the RSTN pin in parallel to GND via a switch.

Table 8.1-1 Definitions of the States of External Power Supplies

Power Supply State Definition	RTC Power Supply	PWC Power Supply	Internal Power Supply	I/O Power Supply	IP Power Supply
All power supplies off	OFF	OFF	OFF	OFF	OFF
Backup power supply on	ON	OFF	OFF	OFF	OFF
PWC supply on	ON	ON	OFF	OFF	OFF
All power supplies on	ON	ON	ON	ON	ON

Although the PWC unit is for controlling the external power supplies, an external PMIC (power management IC) and such can be used instead of the PWC to control the external power supplies to this LSI. **Figure 8.1-2** shows an example of external connections when the PWC is not to be used.

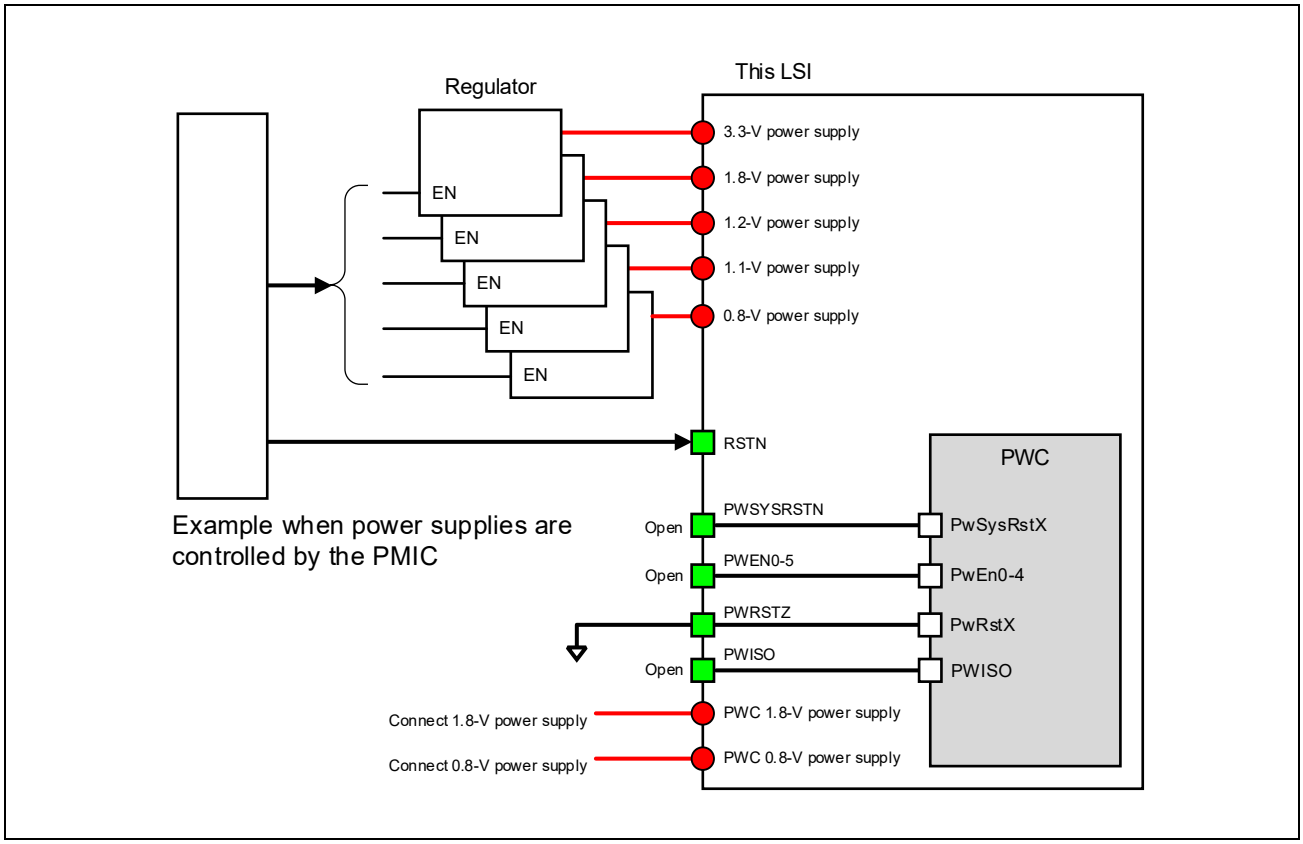


Figure 8.1-2 Example of External Connections when the PWC is not to be Used

Since the PWC of this LSI is recommended, the use of the PWC is assumed in subsequent descriptions of the power supply specifications.

8.2 Internal Power Domains

This section describes the specifications of the internal power supplies (power domains) of this LSI.

8.2.1 Definitions of the Power Domains

Table 8.2-1 lists the correspondence between the definitions of the internal power domains of the LSI and the units which belong to the respective power domains.

For PD_MEM, PD_VIDEO0, PD_VIDEO1, PD_RFX, PD_DRPA, and PD_CA53, control in the form of switching the power on or off is possible. Switching the power on or off is controlled by setting registers of the PMC.

For details, see the section of PMC.

Table 8.2-1 Definitions of the Power Domains and the Units which belong to the Respective Power Domains

Power Domain Control Unit	Power Domain Name	Target Unit*1	Remarks
—	PD_AWO	Units in the internal power supply area other than PD_MEM, PD_VIDEO0, PD_VIDEO1, PD_RFX, PD_DRPA, PD_CA53	Internal power supply (0.8-V) area
PMC	PD_MEM	LPDDR4 (MMC, DDI), ICB (Scheduler)	
	PD_VIDEO0	STG, ISP, GPA	
	PD_VIDEO1	VCD, JPG, ISP,GPA	
	PD_RFX	RAMB	
	PD_DRPA	DRP-AI	
	PD_CA53	CA53	
—	PD_RTC	RTC	RTC power supply (1.5-V, 0.8-V) area
—	PD_PWC	PWC	PWC power supply (1.8-V, 0.8-V) area

Note 1. For details of the target units which belong to the respective power domains, see **Table 8.2-2**.

8.2.2 Power Domain Diagram

Figure 8.2-1 shows the configuration of the power domains of this LSI.

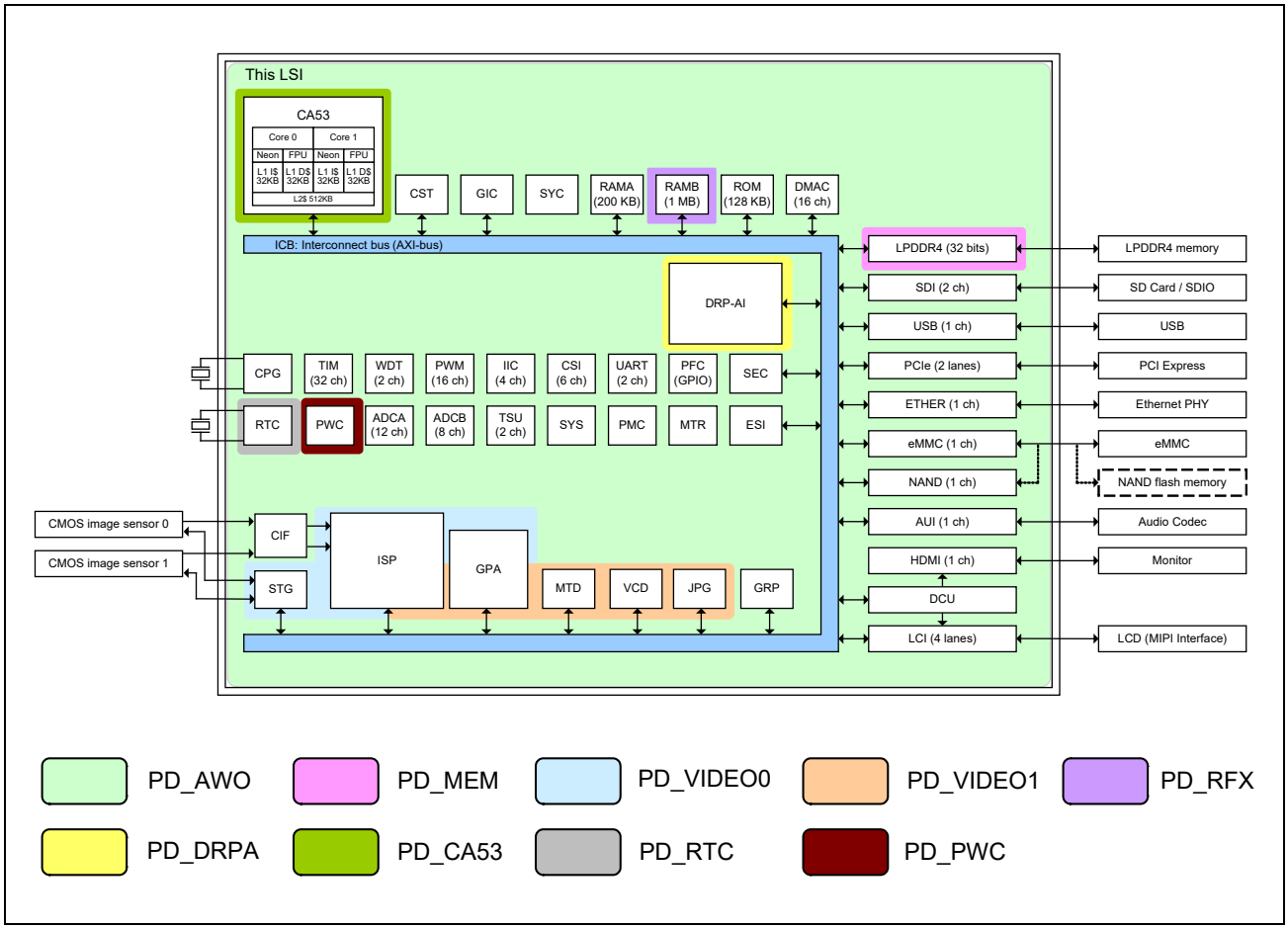


Figure 8.2-1 Power Domain Diagram

8.2.3 Correspondence between Power Domains and Units

Table 8.2-2 lists the correspondence between the power domains and the units.

Table 8.2-2 Correspondence between Power Domains and Units

Power Domain Name	Unit Name
PD_AWO	CST
	DMAC
	ETHER
	GRP
	HDMI
	LCI
	USB
	NAND
	PCIe
	PFC
	PMC
	RAMA
	ROM
	SDI0-1
	eMMC
	SEC
	SYC
	SYS
	CSI0-5
	I2C0-3
	PWM0-15
	TIM0-31
	UART0-1
	WDT0-1
	TSU0-1
	ADCA, ADCB
	AUI
	DCU
	ESI
	GIC
	CIF
	CPG(OTHER)
	CPG(PD_MEM)
	ICB(REG)
	ICB(PD_AWO)

Power Domain Name	Unit Name
PD_MEM	LPDDR4
	ICB (PD_MEM)
PD_VIDEO0	ISP
	GPA
	STG
	CPG (PD_VD0)
	ICB (PD_VD0)
PD_VIDEO1A	ISP
	GPA
	CPG (PD_VD1A)
	ICB (PD_VD1A)
PD_VIDEO1B	VCD
	JPG
	ISP
	CPG (PD_VD1B)
	ICB (PD_VD1B)
PD_RFX	RAMB0-3
	CPG (PD_RFX)
	ICB (PD_RFX)
PD_DRPA	DRP-AI
PD_CA53	CA53
PD_PWC	PWC
PD_RTC	RTC

8.2.4 Internal Power Domains

The internal cell areas which operate with internal power supplies (0.8 V) are in eight different power domains.

All but one of the power domains are configured so that power can be turned off by using an external switch (for one domain) and the internal power switches of the LSI to control the supply of 0.8-V power. **Table 8.2-3** lists the internal power domains and the power switches and **Figure 8.2-2** is a schematic view of the allocation of the internal power domains and the power switches.

Table 8.2-3 Power Switches Used for the Respective Power Domains

Power Domain Name	Power Switch	Remarks
PD_AWO	—	Always on when 0.8-V power is supplied.
PD_MEM	External power switch of the LSI	Switching the power off with an external power switch of the LSI is possible.
PD_VIDEO0	Internal power switch of the LSI	Switching the power off with an internal power switch of the LSI is possible.
PD_VIDEO1	Internal power switch of the LSI	
PD_RFX	Internal power switch of the LSI	
PD_DRPA	Internal power switch of the LSI	
PD_CA53	Internal power switch of the LSI	

Note: These switches are designed to allow turning power off to achieve lower power consumption for the chip while the external power is being supplied, reducing circuit leakage current in the specified power domains.

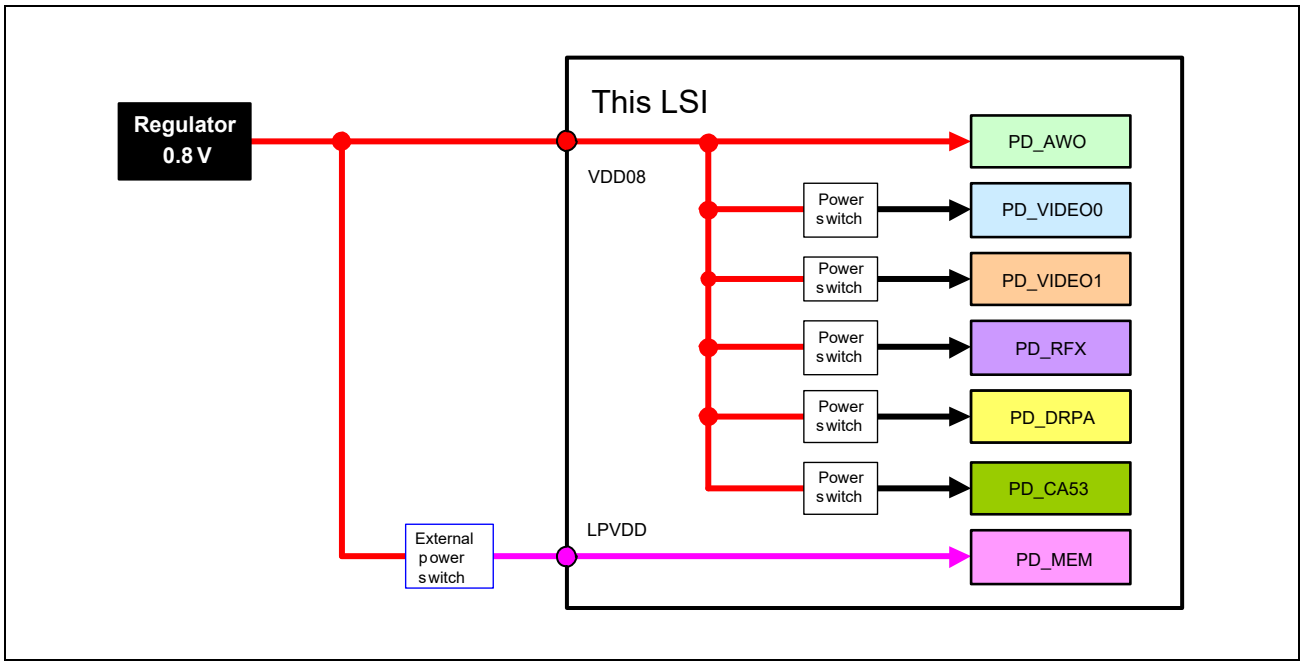


Figure 8.2-2 Schematic View of the Allocation of the Internal Power Domains and the Power Switches

Section 9 System Function

This section describes the system function.

9.1 System Startup/Shutdown

9.1.1 System Startup

This LSI starts the system boot process when the PWC power is turned on and the PWC reset is released.

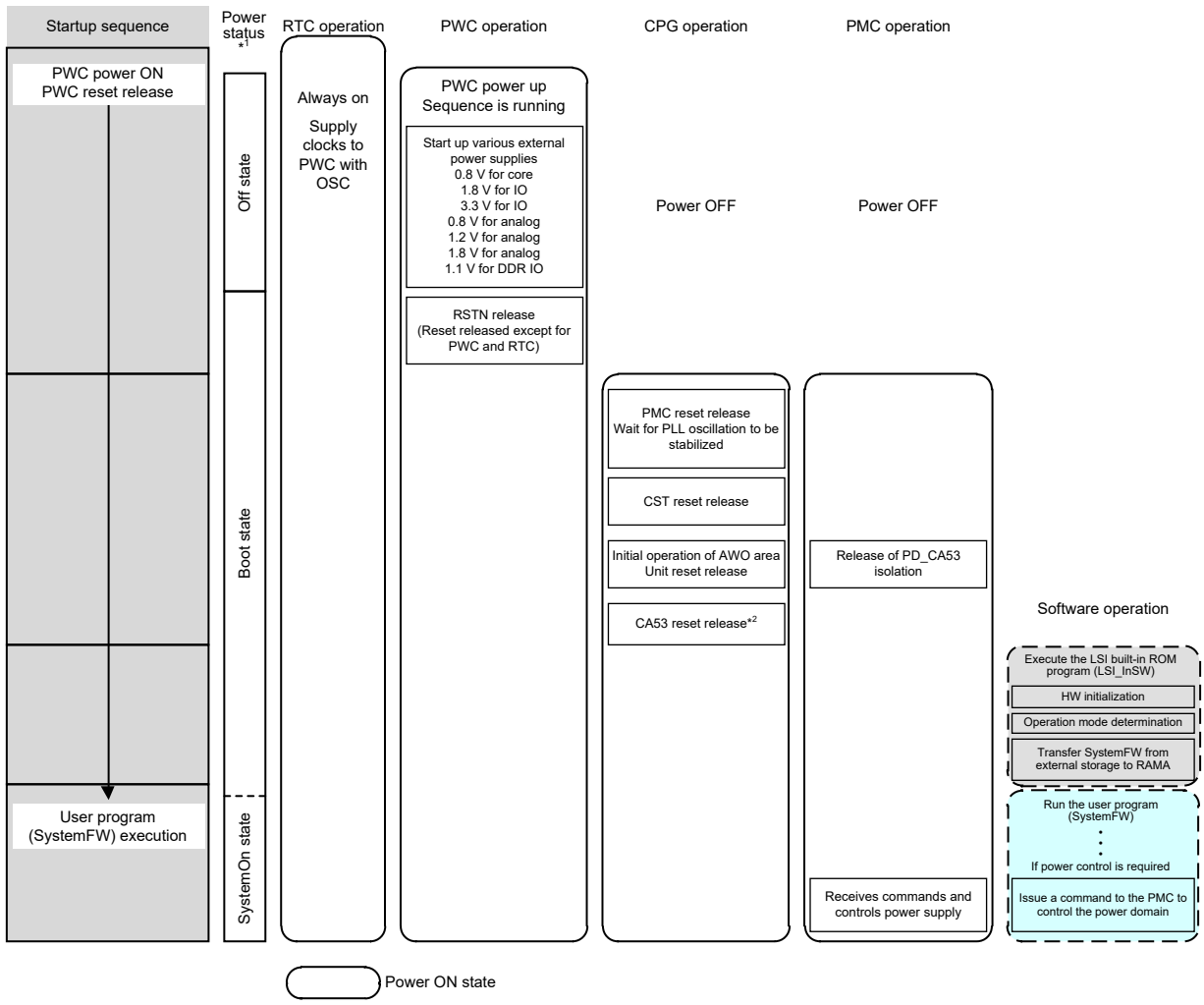
Figure 9.1-1 shows the operation of the individual units in the system startup process.

The RTC, PWC, and CPG are involved in the system startup process, and the startup process is performed by the hardware processing of the individual units without the interaction of the CA53.

RTC: Provides clocks for PWC

PWC: Generates timing for turning on the external power supply

CPG: Internal clock and reset control



Note 1. Definition of power state
Off state: Power is off for all power domains.
Boot state: Power supply domains PD_AWO and PD_CA53 are turned on.
SystemOn state: Power supply domains PD_AWO, PD_MEM, and PD_CA53 are turned on.

Note 2. Before releasing the CA53 reset (400 µs after releasing the system reset using RSTN), turn on the power of the external devices (NAND FLASH, eMMC) on the board where this LSI is mounted and make them ready for operation.

Figure 9.1-1 Startup Sequence Outline

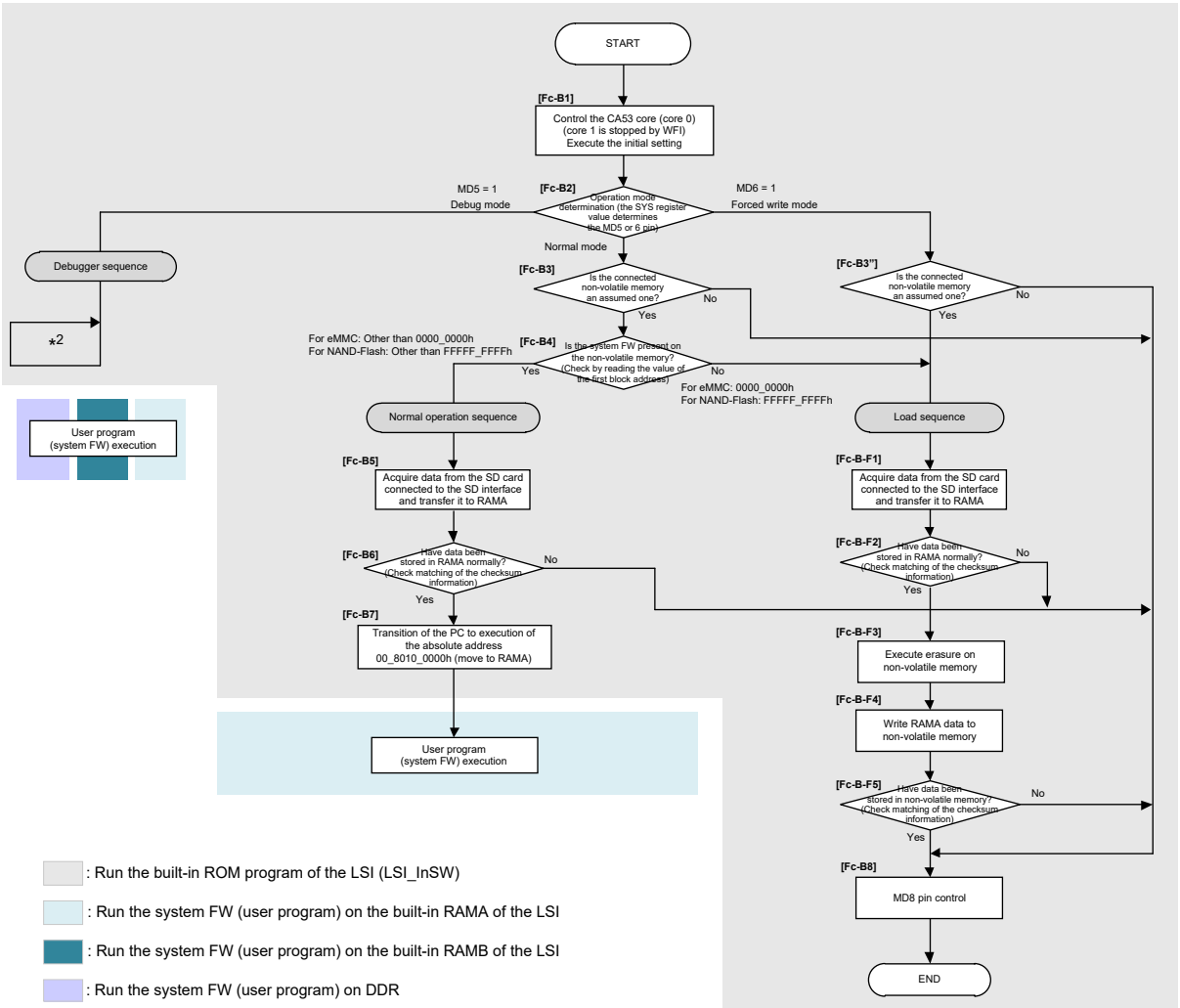
9.1.2 Boot Specifications

9.1.2.1 Overview

When this LSI is booted, the dual-core CA53 boots up and shifts core 1 to the WFI state at the initial setting, and then it operates/controls with core 0 only. After the CA53 is started up, the program stored in the built-in ROM of the LSI (hereafter referred to as LSI_InSW) operates, and the processing branches/executes according to the state of the MD6-5 pins. After the execution, if an error is detected, the MD8 pin is controlled to determine the cause of the error. The values of MD6-0 pins must be fixed before the reset (RSTN) is released.

Figure 9.1-2 shows the boot sequence of this LSI.

This section describes the execution of the built-in ROM of the LSI (hereafter referred to as LSI_InSW) shown in the figures.



Note 1. After the system operates on RAMA of the LSI, a transition to the destination for subsequent execution (RAMB of the LSI or DDR) is arbitrarily determined by the SystemFW processing (control over activation of each peripheral also follows the SystemFW).

Note 2. The PC (program counter) is locked (loop is repeated), and the control is transferred to the debugger.

Figure 9.1-2 Boot Sequence

9.1.2.2 Operation Specifications

In this section, execution of LSI_InSW in **Figure 9.1-2** is described.

(1) Switching the Operation Specifications

The operating mode (normal, debug, forced write) and boot device (non-volatile memory mounted on the board) are selected by the state of the MD6-0 pins.

Note that the status of the MD6-0 pins is output to bits MD6-0 in the SYS_MD_MON register (00_A3F0_3100h).

a) Operation mode

Table 9.1-1 Selection of Operation Mode

MD6	MD5	Operation Mode	Operation in Outline
0	0	Normal mode	Mode which acquires the SystemFW stored in a non-volatile memory and executes it on RAMA (this mode is for use in normal activation).
0	1	Debug mode	Mode which connects the debugger (ICE) to control the LSI.
1	x	Forced write mode	Mode for writing the following file specified by the MD3 pin to a non-volatile memory. • SD: A file which is stored in the SD card via the SD interface of this LSI.

Note: x: Don‘t care

b) Boot device (non-volatile memory mounted on the board)

Table 9.1-2 Selection of Boot Device

MD2	MD1	MD0	Boot Device
1	0	x	BENAND 1 Gbit (128 Mbytes) / 2 Gbits (256 Mbytes)
1	1	0	eMMC
Other than the above			Setting prohibited

Note: x: Don’t care

(2) Operation when Normal Mode is Activated

Normal mode is the mode used for normal activation.

When LSI_InSW is activated in normal mode, SystemFW*[1] stored in the non-volatile memory is extended to RAMA. After checking that it has been extended normally, the control is transferred to the SystemFW extended on RAMA.

- The address where the SystemFW (including the boot loader) starts is 00_0000_0000h (the absolute address: 00_8010_0000h).
  Write the SystemFW in that area beforehand.

Note 1. A 128-Kbyte firmware running on RAMA which performs expansion of the main SystemFW that is to run first following the system startup is defined as the boot loader.

9.1.2.3 Control Sequence in Each Operation Mode

This section describes the control sequence (flow of processing) in each operation mode.

In each mode, the following common processing is executed before the individual processing

NOTE

[FC-Bn] and [FC-B-Fm] at the end of the description of each processing in this section indicate the processing number of each flowchart in the figure below.
(n = 1 to 8, m = 1 to 5)

- **Figure 9.1-2, Boot Sequence**

■ Common Processing

(a) The built-in ROM of the LSI is started up and initialization (CA53 initialization and initialization of other required hardware) is executed. [Fc-B1]

(b) Acquire the state of the MD6-0 pins from the MD6-0 bits of the SYS_MD_MON register. [Fc-B2]

Brach to a given operation mode by the value of MD6-5.

When MD6-5 = 00b ⇨ Move to normal mode.
When MD6-5 = 01b ⇨ Move to debug mode.
When MD6-5 = 1xb ⇨ Move to forced write mode.
x: Don’t care

(1) Normal Mode

The following describes the flow of processing in normal mode.

■ Example of transition: In the case of a boot device (non-volatile memory mounted on the board): eMMC / NAND flash

(c) Determine the non-volatile memory mounted on the board with the value of MD2-0 acquired in step (b) above. [Fc-B3]

Determine the interface voltage or non-volatile memory from the value of MD2-0 and execute the settings (pins, EMM or NFI, etc.) in the selected memory.

After that, acquire the ID information of the non-volatile memory and execute reading of the first data on the memory and determine whether acquisition of that value is possible or not (the acquired value itself is not determined at this time).

When acquisition is possible ⇨ Move to (d).
When acquisition is not possible ⇨ LED lighting control: Proceed with error detection (Fc-B8) and end processing.

(d) Acquire data in the specific area of eMMC or NAND flash via the EMM or NFI and determine whether the SystemFW*[1] is or is not present. [Fc-B4]

[For eMMC]

When the acquired value is not 0000_0000h ⇨ Move to (e): Proceed to the normal operation sequence.
When the acquired value is 0000_0000h ⇨ Proceed to the load sequence.

[For NAND flash]

When the acquired value is not FFFF_FFFFh ⇨ Move to (e): Proceed to the normal operation sequence.
When the acquired value is FFFF_FFFFh ⇨ Proceed to the load sequence.

(e) Acquire the SystemFW from the start of the non-volatile memory and copy it to the start of RAMA (capacity: 125 Kbytes). [Fc-B5]

(f) Check the checksum information to confirm that the SystemFW has been normally transferred to RAMA. [Fc-B6]

Calculate the checksum for data which have been transferred to RAMA to compare whether it matches the checksum read from eMMC or NAND flash via the EMM or NFI.

When the result is a match ⇨ Move to (g).
When the result is a mismatch ⇨ LED lighting control: Proceed with error detection (Fc-B8) and end processing.

(g) Jump to the address where RAMA starts (00_8010_0000h). [Fc-B7]

~~ After the above steps, control of the user program (SystemFW)*[1] is to proceed. ~~

Note 1. "SystemFW" defined here is assumed as a boot loader.

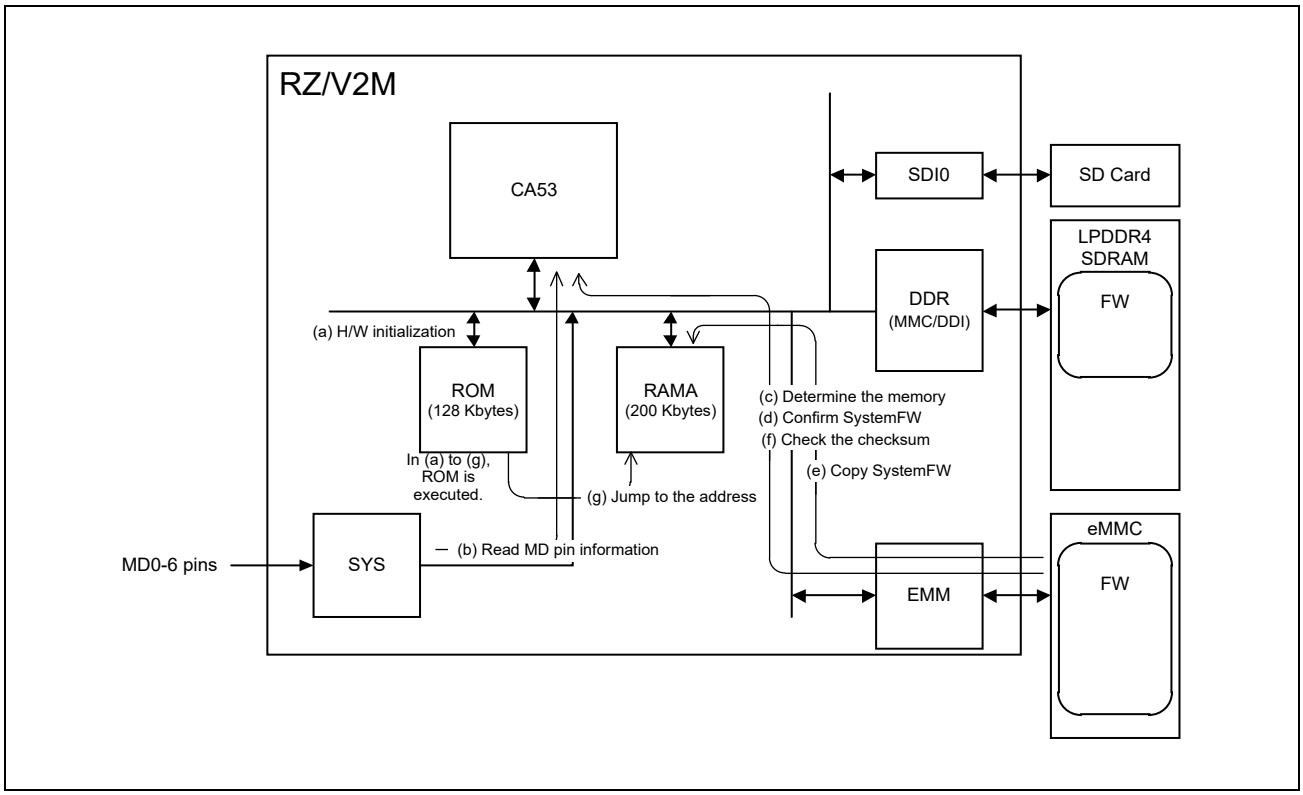


Figure 9.1-3 Normal Mode

(2) Forced Write Mode

The following describes the flow of processing in forced write mode.

This mode operates on the assumption that the SD card is connected to the SD interface (the SD card is inserted to the SD card connector).

The data specifications obtained with an other-party device (SD card) in the load sequence are as follows:

- Max. data capacity: 128 Kbytes
- Checksum value: 2 bytes (16 bits), little endian
- Address range: from 801F_FFFEh to 801F_FFFFh
- File name: B2_INTSW.bin

■ Example of transition

(c) Determine the non-volatile memory mounted on the board with the value of MD2-0 acquired in step (b) above. [Fc-B3”]

Determine the interface voltage or non-volatile memory from the value of MD2-0 and set the registers to suit the selected memory (for pins and eMMC: EMM; for NAND: NFI).

After that, acquire the ID information of the non-volatile memory and execute reading of the first data and determine whether acquisition of that value is possible or not (the acquired value itself is not determined at this time).

When acquisition is possible ⇒ Move to (d).
When acquisition is not possible ⇒ LED lighting control: Proceed with error detection (Fc-B8) and end processing.

~~ After the above steps, the load sequence is to proceed. ~~

(d) Access the SD card via SDI0, acquire the file format information, and transfer data (SystemFW) with the corresponding file name to RAMA. [Fc-B-F1]

When acquisition is possible ⇒ Move to (e).
When acquisition is not possible ⇒ LED lighting control: Proceed with error detection (Fc-B8) and end processing.

(e) Check the checksum information to confirm that the SystemFW has been normally transferred to RAMA. [Fc-B-F2]

Calculate the checksum value from the data which have been transferred to RAMA to compare whether it matches the expected value (the value stored within the SystemFW).

When the result is a match ⇒ Move to (f).
When the result is a mismatch ⇒ Proceed with LED lighting control (Fc-B8) and end processing.

(f) Control the unit that suits the non-volatile memory and erase the start area of that memory (the area to which the SystemFW is written). [Fc-B-F3]

(g) Control the unit that suits the non-volatile memory and write the SystemFW stored in RAMA to the non-volatile memory). [Fc-B-F4]

(h) Check the checksum information to confirm that the SystemFW has been normally transferred to the non-volatile memory. [Fc-B-F5]

Calculate the checksum value from the data which have been expanded in the non-volatile memory to compare whether it matches the expected checksum value acquired in step (e).

When the result is a match ⇒ Proceed with LED lighting control (Fc-B8) and end processing.
When the result is a mismatch ⇒ Proceed with LED lighting control (Fc-B8) and end processing.

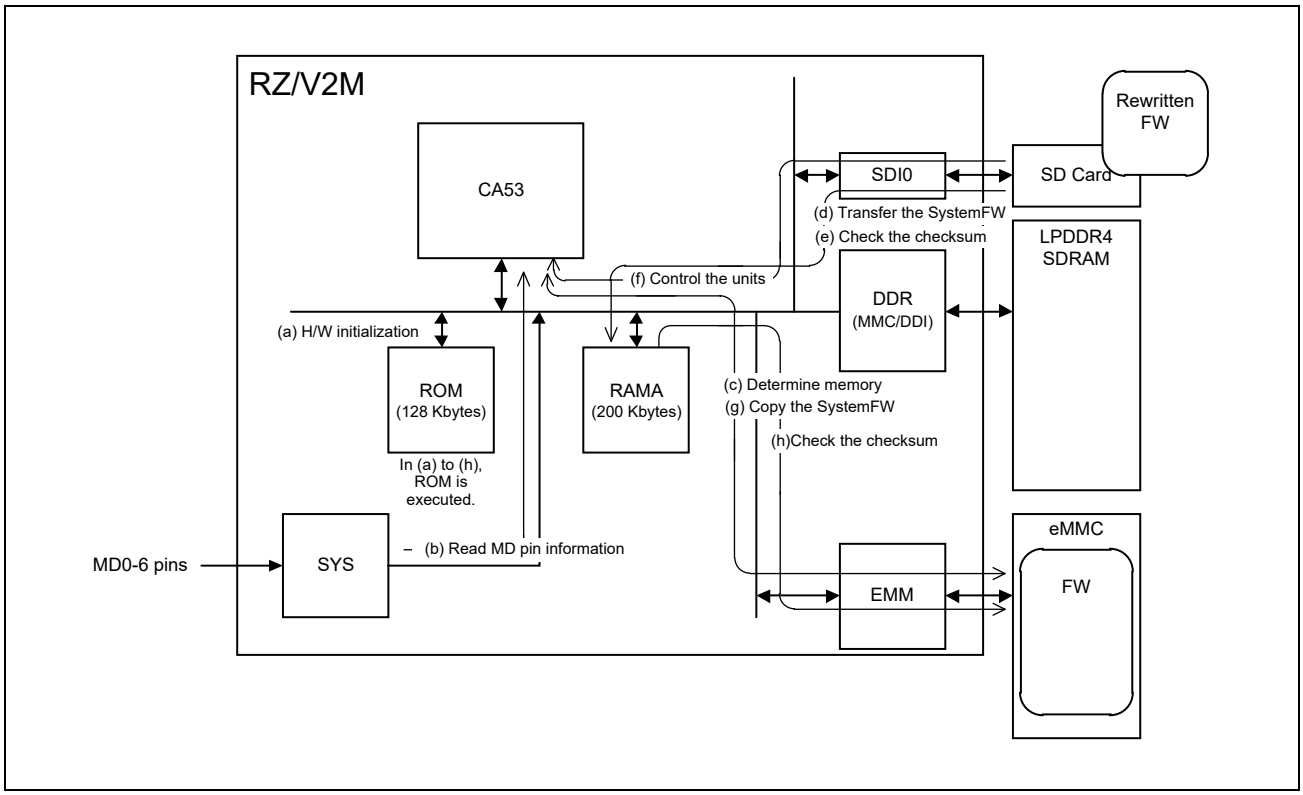


Figure 9.1-4 Forced Write Mode (SD Card)

(3) Debug Mode

The following describes the flow of processing in debug mode.

(c) When the mode for transition is judged to be debug mode in step (b), an endless loop is entered (access from the debugger is possible after that).

~~ After the above step, processing from the debugger is to proceed. ~~

(d) A software reset from the debugger is input externally, and the ICE specifies the address where execution is to start and copies data, and execution of the SystemFW starts.

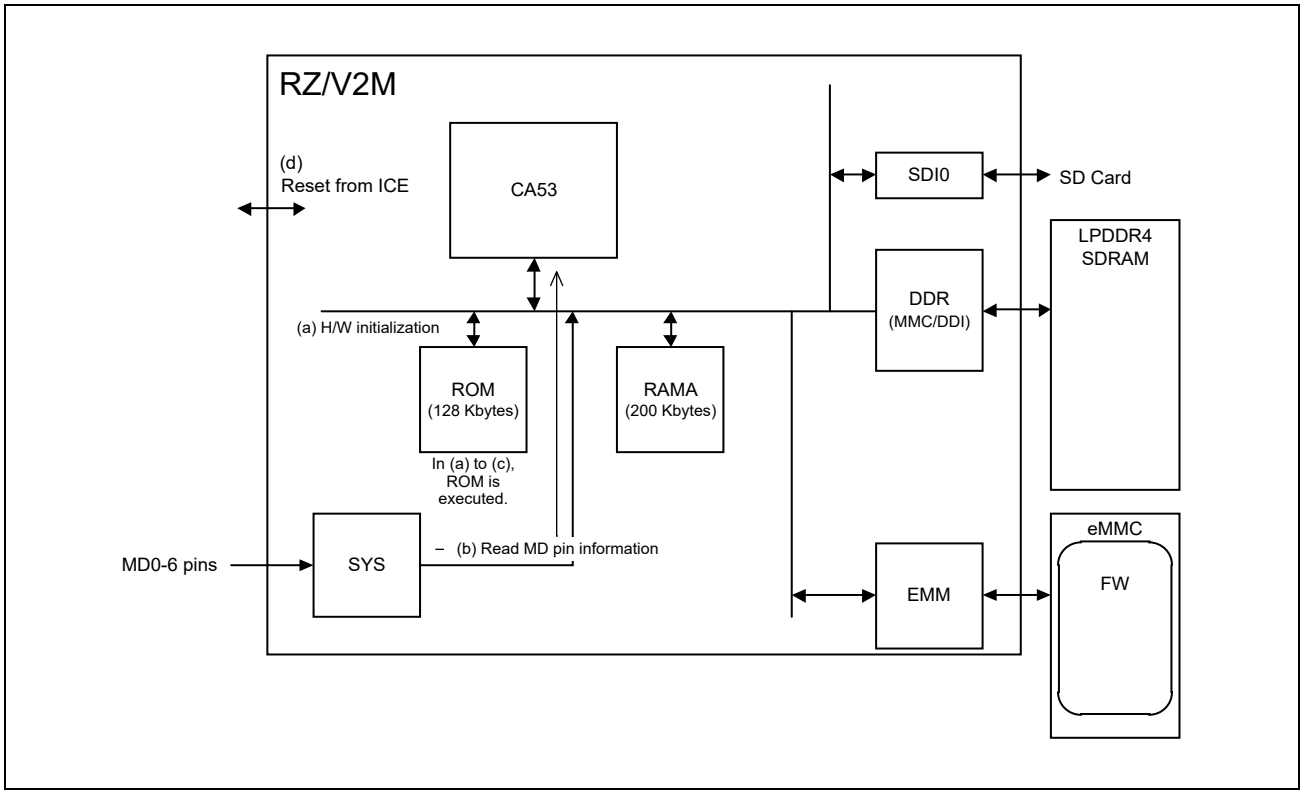


Figure 9.1-5 Debug Mode

9.1.2.4 Error Detection and MD8 Pin Control

When an error in execution of LSI_InSW is detected, the MD8 pin is controlled.

The detected error conditions and the MD8 pin control patterns for the errors are listed below.

By connecting an LED to this MD8 pin, whether the error has occurred can be judged by LED lighting. For the flow number, see **Figure 9.1-2**.

Table 9.1-3 List of Error Operation Modes

Sequence	Item	Detected Error	Flow Number	Control Pattern
Normal operation/load	MD switch	MD0-2 = 111b	Fc-B1	Pattern1. Pin error
	NAND, eMMC	Failure in device ID acquisition*1	Fc-B3, Fc-B3”	Pattern2. Boot device error
		Failure in reading of the first data*1	Fc-B3, Fc-B3”	Pattern2. Boot device error
		Failure in checksum judgment (The data stored in NAND or eMMC are expanded in RAMA, and the checksum value calculated from the expanded data and the expected value to be added to the last of the data are compared to check whether they match.)	Fc-B6	Pattern3. LSI error
Load	—	None	—	Pattern0. Normal operation
	SD card	Failure in data reading*2	Fc-B-F1	Pattern4. Other-party device error
	NAND, eMMC	Failure in checksum judgment Checksum is performed twice at the following times. 1) After expansion from the SD interface to RAMA 2) After expansion from RAM to the boot device	Fc-B-F2, Fc-B-F5	Pattern3. LSI error
		Failure in data erasure*1	Fc-B-F3	Pattern2. Boot device error
		Failure in data writing*1	Fc-B-F4	Pattern2. Boot device error
		Failure in data reading*1	Fc-B-F5	Pattern2. Boot device error

Note 1. A timeout of the execution command is detected, or an error is detected in the result of command execution.

Note 2. The SD interface is not connected, or an error is detected in the command response through the SD interface.

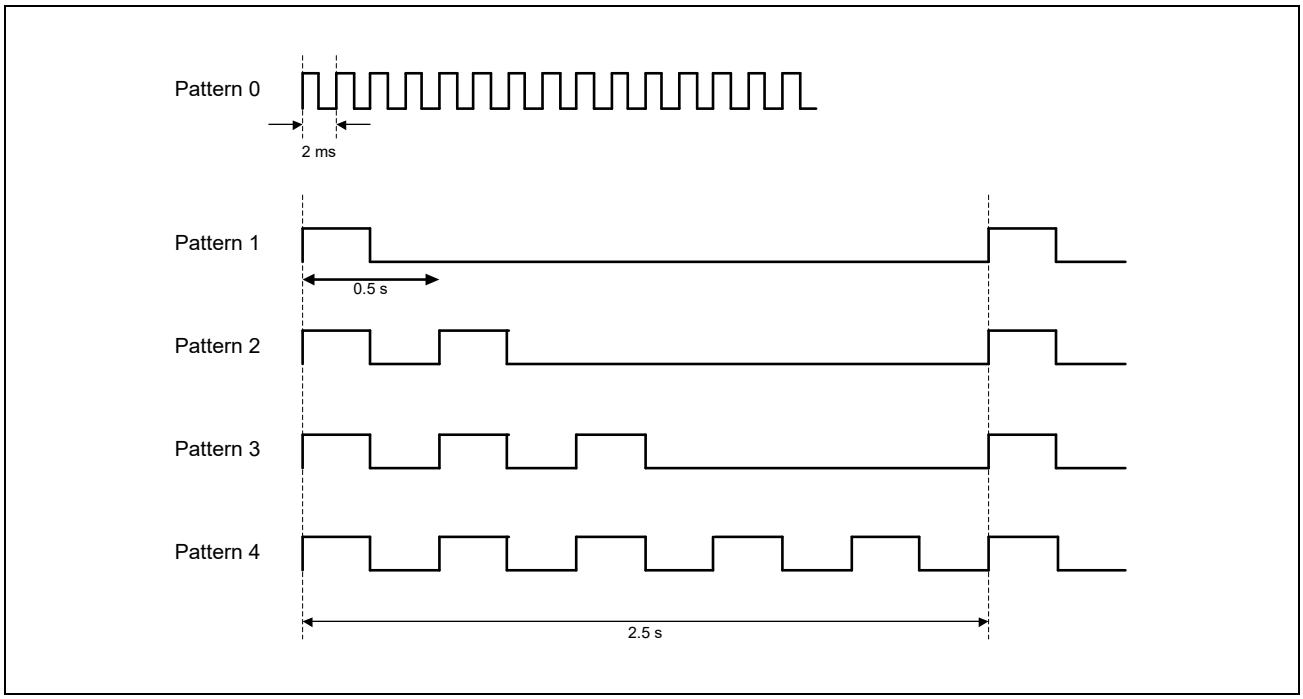


Figure 9.1-6 Control Patterns

9.1.2.5 Specifications of Register Settings

(1) Operating Clock Settings

The operating clocks to be set by LSI_InSW are listed below.

Table 9.1-4 Operating Frequency Settings

Category	Specified Clock	Control Register			Frequency Setting (MHz)
		Register Name	Offset Address	Setting Value	
MAIN	System clock	CPG_SYS_DDIV	204h	0000_0001h	ICB_ACLK: 200 GIC_CLK: 100 CPG_MPCLK: 200
	Source clock specification	CPG_CLK48_DSEL	214h	0000_0003h	Specified by CPG_CA53_DDIV
	CA53 core clock	CPG_CA53_DDIV	200h	0000_0003h	249
Flash (NFI)	NFI clock (NF_CLK, BCH_CLK: DIV NFI)	CPG_NFI_DDIV	20Ch	0000_0000h	400
eMMC, SD	Main clock	CPG_SDIEMM_SSEL	300h	0000_0001h	200
	SD clock (SDCLK)	SD_CLK_CTRL	90h	0000_0104h	12.5

(2) Initial Settings

The settings for register processing in LSI_InSW are listed below. [Fc-B1]

Table 9.1-5 Initial Settings (RAMA)

Unit	Register Name	Address	Setting Value	Setting in Outline
RAMA	RAMA_ECC_CNT	00_A3F0_3110h	0000_0001h	Enable RAMA ECC.
	RAMA_INIT	00_A3F0_3114h	0000_0001h	Change the enabled setting for initialization of the RAMA ECC code area to the disabled setting.
	W0_EC710CTL	00_92F4_0000h	0000_4050h	Set the recommended value in the ECC control register.
	W1_EC710CTL	00_92F4_0040h	0000_4050h	Set the recommended value in the ECC control register.
	W2_EC710CTL	00_92F4_0080h	0000_4050h	Set the recommended value in the ECC control register.
	W3_EC710CTL	00_92F4_00C0h	0000_4050h	Set the recommended value in the ECC control register.

9.1.2.6 Supplementary Notes on Specifications

The specifications of LSI_InSW operations are as follows.

(a) Bootloader area (information of allocation on RAMA)

Item	Address (Range)	Size
Bootloader body	8010_0000h to 8011_FFF7h	128 Kbytes
Bootloader body size	801F_FFF8h to 801F_FFFDh	4 bytes
Checksum value	801F_FFFEh to 801F_FFFFh	2 bytes (16 bits)

(b) Checksum calculation specifications

- Addition width: 16 bits
- Bit width for comparison after addition: 16 bits
- Addition in little-endian representation

(c) Judging the validity of non-volatile memory

The target non-volatile memory is judged as a usable device when the device ID and the data at the start address can be obtained (i.e., judged when a command response can be executed without an error, instead of judging the obtained value).

(d) Supplementary notes on the specifications of the load sequence

- When using this mode, be sure to insert an SD card into the SD card connector before supplying power to the board on which this LSI is mounted.
- The write file to be stored in the SD card must meet the following specifications.

Item	Description
File name	B2_INTSW
Format	One partition, FAT32 (SD-HC)
Supplementary note	• Only one target write file name must exist. • Files other than the target one can be stored up to ten files in the same partition. • Size judgement on the target write file name is not performed in the on-chip ROM. Detection of errors in the target write file is performed by using the checksum calculation results.

(e) Specifications of load sequence erase processing

- Range of erasure

  Flash: Erase only the storage range of the bootloader (128 Kbytes).

  eMMC: Erase the boot partition.

- If a problem occurs during the load sequence, erase processing, etc. is not performed on the non-volatile memory (flash or eMMC).

(f) Setting the timing of access to NAND flash

The settings for NAND flash access timing are as follows.

Table 9.1-6 Boot Device Timing Settings

NFI Register	Address	Setting Value	Part to be Adjusted	Setting Value
ASYNC	101Ch	0610_0607h	t_{RH}	06
			t_{RP}	10
			t_{WH}	06
			t_{WP}	07
TIMINGS0	1024h	1E1B_1B1Bh	t_{ADL}	1E
			t_{CCS}	1B
			t_{WHR}	1B
			t_{RHW}	1B
TIMINGS0	1028h	1A38_0DFFh	t_{RHZ}	1A
			t_{WB}	38
			t_{CWAW}	0D
			t_{VDLY}	FF
TIMINGS2	102Ch	0038_050Bh	t_{FEAT}	38
			CS_hold	05
			CS_setup	0B

9.1.3 CA53 Core1 Startup Setting

The following describes the startup procedure of CA53 core 1 following the bootloader after executing LSI_InSW.

[Startup control method]

(1) Specification of the storage address of the software to be executed by CA53 core 1

CA53_RVA1CRL register (A3F0_0028h), CA53_RVA1CRH register (A3F0_002Ch)

(2) Deployment of the software to be executed by CA53 core 1

Deployment of the software to the area (memory: RAMA/B, LPDDR4) specified in (1)

(3) Reset execution

CPG_RST8 register (A350_061Ch): UNIT3_RSTB bit = 0b, UNIT1_RSTB bit = 0b

(4) Wakeup

CA53_PSCR register (A3F0_003Ch): CA53_DBGPWRDUP[1] bit = 1b

(5) Reset release

CPG_RST8 register (A350_061Ch): UNIT3_RSTB bit = 1b, UNIT1_RSTB bit = 1b

9.1.4 Power Off Processing

While the internal power supply state is the system-on state, the external power supply turn-off sequence is activated and the system shifts to the off state.

9.2 Power Management

This section describes the power management function of this LSI.

This LSI is equipped with the following power management functions to achieve low power consumption.

- Clock stop control
- Power switch control

9.2.1 Clock Stop Control

This function reduces the operating power by stopping the clock of units that do not need to operate as a system.

The desired clock can be stopped by setting the CPG clock ON/OFF control register CPG (CPG_CLK_ON1 to CPG_CLK_ON27). For details, see the CPG section.

9.2.2 Power Switch Control

This function reduces the leakage power by turning off the power of power domains that do not need to be operate as a system.

By setting the PMC power supply enable register (PMC: PMC_SPLY_ENA), the power supplied to the power supply domains of PD_MEM, PD_VIDEO0, PD_VIDEO1, PD_RFX, PD_DRPA, and PD_CA53 can be turned off. For details, see the PMC section.

9.3 Debugger Connection

9.3.1 Debug Mode

The debug mode of this LSI is switched by the state of the MD5 and MD6 pins. For the pin status and the selected debug mode, see **Table 9.1-1**.

Fix the values of MD5 and MD6 pins before the reset (RSTN) is released.

9.3.2 Reset and Clock in Debug Mode

Resetting in debug mode is controlled by the DESRSTN and DETRSTN pins.

The schematic configuration of the debugger reset is shown in **Figure 9.3-1** and the status of SRSTN, TRSTN, and TCK in the respective modes is shown in **Table 9.3-1**.

In debug mode, SYS generates the SYS_DBGMD signal from the state of the MD5 and MD6 pins. CPG identifies whether the mode is normal mode or debug mode by the SYS_DBGMD signal and controls SRSTN, TRSTN, and TCK. In normal mode, the clock of the debug circuit is stopped and initialized.

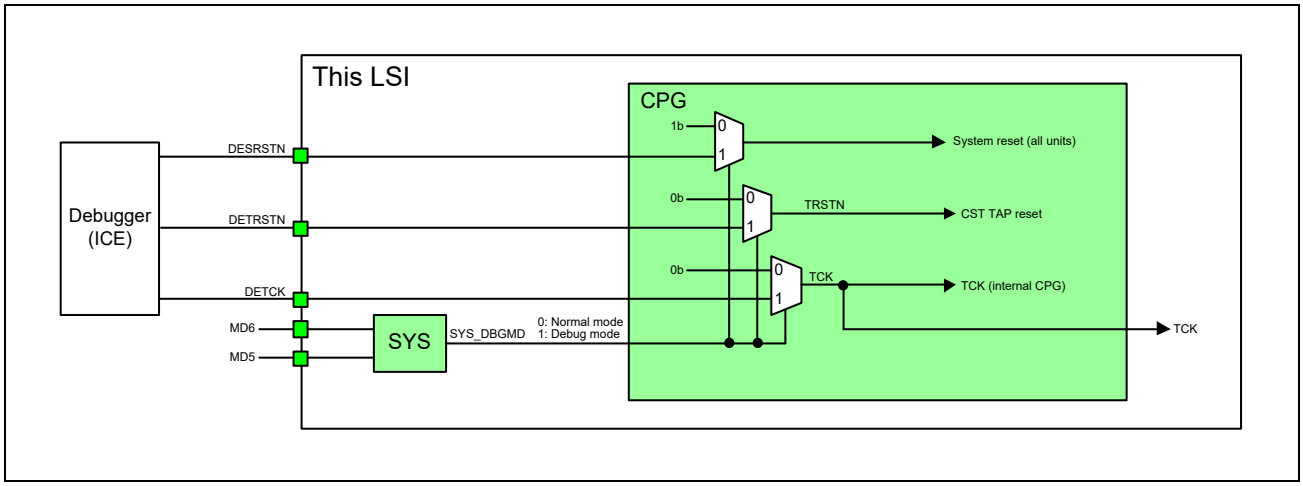


Figure 9.3-1 Debugger Reset Schematic Configuration

Table 9.3-1 Status of SRSTN, TRSTN, and TCK

Operation Mode	SYS_DBGMD	SRSTN	TRSTN	TCK
Normal mode	0	Fixed to 1	Fixed to 0	Fixed to 0
Debug mode	1	DESRSTN	DETRSTN	DETCK

Section 10 CPU

This section describes the functions of the Cortex-A53 subsystem (CA53).

10.1 Functional Overview

The CA53 is a subsystem with an Arm® Cortex®-A53 processor (r0p4). For details on the Cortex-A53, see *the ARM Cortex-A53 MPCore Processor Technical Reference Manual* and *the ARM Cortex-A53 MPCore Processor Advanced SIMD and Floating-point Extension Technical Reference Manual*.

In this section, the subsystems will be referred to as “CA53”, Arm’s CPU (hierarchy including SCU) as “Cortex-A53”, and Cortex-A53’s internal processing-elements as “Core”. If these are not specified, the subsystem is indicated.

10.1.1 CA53 Subsystem Functions

Table 10.1-1 lists the subsystem functions.

Table 10.1-1 Subsystem Functions

Item	Function
Equipped CPU	Cortex-A53 r0p4 (ARMv8-A) Number of cores installed: 2 L1$(I/D) = 32 Kbytes/ 32 Kbytes L2$ = 512 Kbytes
Internal register	Status monitoring of Cortex-A53

10.1.2 Cortex-A53 Configuration

Table 10.1-2 lists the configuration (embedded specification) of the Cortex-A53.

Table 10.1-2 Cortex-A53 Configuration

Item	Setting
Number of Cortex A53 cores	2
Arm® Neon™/FPU Engine	Available
Cryptography Engine	Not available
L1 cache size (instruction)	32 Kbytes
L1 cache size (data)	32 Kbytes
ECC for the L1 cache	Available
L2 cache	Available
L2 cache size	512 Kbytes
ECC for the L2 cache	Available
Setting the data input latency for L2 cache	1 cycle
Setting the data output latency for L2 cache	2 cycles
Architecture execution mode	64-bit mode (AArch64)
Byte order	Little endian
Core 0 reset vector position	00_8000_0000h
Core 1 reset vector position	00_8000_0000h

10.2 Register Description

This section describes the registers that have been added as the Cortex-A53 subsystem. For details on the Cortex-A53 registers, see *the ARM Cortex-A53 MPCore Processor Technical Reference Manual* and *the ARM Cortex-A53 MPCore Processor Advanced SIMD and Floating -point Extension Technical Reference Manual*.

For the base address of the registers (<CA53_S0_base>), see “Address Map Details” in the Address Map section.

10.2.1 List of Registers

Table 10.2-1 is a list of registers.

Table 10.2-1 List of Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)*1
Cortex-A53 pin control register				
000h to 024h	Reserved	—	—	—
028h	CA53 Core1 Reset Vector Address Configuration Register L	CA53_RVA1CRL	8000_0000h	32 bits
02Ch	CA53 Core1 Reset Vector Address Configuration Register H	CA53_RVA1CRH	0000_0000h	32 bits
030h to 038h	Reserved	—	—	—
03Ch	CA53 Processor Power Status Configuration Register	CA53_PSCR	0000_0003h	32 bits
040h to 3FCh	Reserved	—	—	—
Cortex-A53 monitor register				
400h	CA53 Warm Reset Request Monitor Register	CA53_WRIRMR	0000_000xh*2	32 bits
404h to 40Ch	Reserved	—	—	—
410h	CA53 L2cache Hardware Flush Complete Monitor Register	CA53_L2HFMR	0000_000xh*2	32 bits
414h	CA53 CPUECTLR.SMPEN Bit Monitor Register	CA53_SMPENMR	0000_000xh*2	32 bits
418h to FFCh	Reserved	—	—	—

Note 1. Access other than 32 bits and access to the reserved registers are prohibited. The operation is not guaranteed if accessed.

Note 2. bit[0] is undefined.

10.2.2 Register Descriptions

10.2.2.1 CA53 Core1 Reset Vector Address Configuration Register L (CA53_RVA1CRL)

This register sets the lower-order side [31:2] of the reset vector base address in the AArch64 state of core 1.

This register setting is sampled while each processor power-up reset or each core reset is asserted.

Access Size: 32 bits

Address(es): <CA53_S0_base> + 0028h

Initial Value: 8000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CA53_RVBARADDR1[31:16]															
Initial Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CA53_RVBARADDR1[15:2]														—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R

Table 10.2-2 CA53_RVA1CRL Register Contents

Bit Position	Bit Name	Description
31 to 2	CA53_RVBARADDR1[31:2]	Set the reset vector base address [31:2] in the AArch64 state of core 1.
1, 0	—	Reserved. These bits are read as 0b. The write value should always be 0b.

10.2.2.2 CA53 Core1 Reset Vector Address Configuration Register H (CA53_RVA1CRH)

This register sets the higher-order side [39:32] of the reset vector base address in the AArch64 state of core 1.

This register setting is sampled while each processor power-up reset or each core reset is asserted.

Access Size: 32 bits

Address(es): <CA53_S0_base> + 002Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CA53_RVBARADDR1[39:32]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 10.2-3 CA53_RVA1CRH Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	CA53_RVBARADDR1[39:32]	Set the reset vector base address [39:32] in the AArch64 state of core 1.

10.2.2.3 CA53 Processor Power Status Configuration Register (CA53_PSCR)

This register is used to set the power status of each core.

Access Size: 32 bits

Address(es): <CA53_S0_base> + 003Ch

Initial Value: 0000_0003h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CA53_DBGPWRDUP[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Table 10.2-4 CA53_PSCR Register Contents

Bit Position	Bit Name	Description
31 to 2	—	Reserved. These bits are read as 0b. The write value should always be 0b.
1, 0	CA53_DBGPWRDUP[1:0]	Sets the power status of the processor. Bit 1 = Core1, Bit 0 = Core0 0b: Processor power down 1b: Processor power up (initial value)

10.2.2.4 CA53 Warm Reset Request Monitor Register (CA53_WRIRMR)

This register is used to monitor the warm reset request for respective cores.

Access Size: 32 bits

Address(es): <CA53_S0_base> + 0400h

Initial Value: 0000_000xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CA53_WARMRSTREQ[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 10.2-5 CA53_WRIRMR Register Contents

Bit Position	Bit Name	Description
31 to 2	—	Reserved. These bits are read as 0b.
1, 0	CA53_WARMRSTREQ[1:0]	Monitor the value of warm reset request signal for respective cores. Bit 1 = Core 1, Bit 0 = Core 0 0b: No warm reset requested 1b: Warm reset requested

10.2.2.5 CA53 L2 Cache Hardware Flush Complete Monitor Register (CA53_L2HFMR)

This register is used to monitor the L2 cache HW flush completion status.

Access Size: 32 bits

Address(es): <CA53_S0_base> + 0410h

Initial Value: 0000_000xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CA53_L2FLUSHDONE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 10.2-6 CA53_L2HFMR Register Contents

Bit Position	Bit Name	Description
31 to 1	—	Reserved. These bits are read as 0b.
0	CA53_L2FLUSHDONE	Monitor the value of L2 cache HW flush completion signal. 0b: L2 cache HW flush not completed 1b: L2 cache HW flush completed

10.2.2.6 CA53 CPUECTLR.SMPEN bit Monitor Register (CA53_SMPENMR)

This register is used to monitor the state of the SMPEN bit in the CPU extended control register (CPUECTLR) for respective cores.

Access Size: 32 bits

Address(es): <CA53_S0_base> + 0414h

Initial Value: 0000_000xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CA53_SMPEN [1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 10.2-7 CA53_SMPENMR Register Contents

Bit Position	Bit Name	Description
31 to 2	—	Reserved. These bits are read as 0b.
1, 0	CA53_SMPEN[1:0]	Monitor the value of SMPEN output signal in the CPU extended control register (CPUECTLR) for respective cores. Bit 1 = Core 1, Bit 0 = Core 0 0b: Power OFF is possible. 1b: Retention is possible. Power OFF is not possible.

10.3 Functional Description

For details on the Cortex-A53 functions, see *the ARM Cortex-A53 MPCore Processor Technical Reference Manual* and *the ARM Cortex-A53 MPCore Processor Advanced SIMD and Floating-point Extension Technical Reference Manual*.

10.4 Operating Procedure

For details on the operating procedures of the Cortex-A53, see *the ARM Cortex-A53 MPCore Processor Technical Reference Manual* and *the ARM Cortex-A53 MPCore Processor Advanced SIMD and Floating-point Extension Technical Reference Manual*.

Section 11 System Counter (SYC)

This section describes the functions of the system counter (SYC).

The SYC is the unit used to generate the count values used by the generic timer in the CA53. It uses a timestamp generator, one of the components of the Arm® CoreSight™ SoC-400, to generate a 64-bit count value. For details on the timestamp generator, see *the ARM CoreSight SoC-400 Technical Reference Manual*.

11.1 Functional Overview

Table 11.1-1 is an overview of functions.

Table 11.1-1 Overview of Functions

Item	Function
Equipped functions	• Generates 64-bit gray code count values – Convert the value generated by the timestamp generator to gray code and output it. • Halt-on-debug function – Halt/resume of the count value in debug mode is possible according to the request from CST.
Operating frequency	24 MHz

11.2 Block Diagram

Figure 11.2-1 shows a block diagram of the SYC.

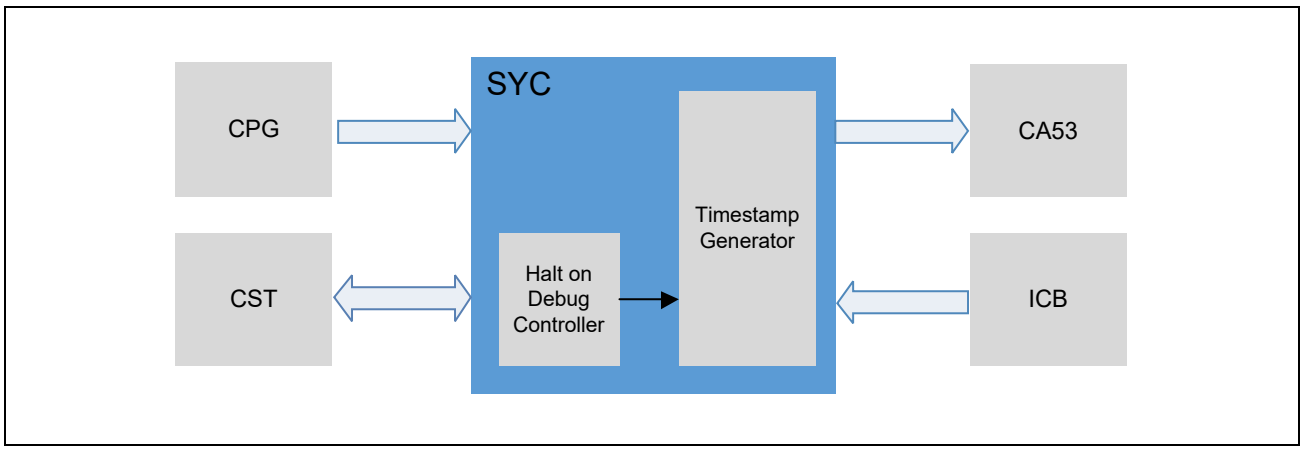


Figure 11.2-1 Block Diagram

11.3 Address Space

Table 11.3-1 lists the APB address space (SYC_S0_base). The SYC has an APB address space of 8 Kbytes.

For details on the APB address space (SYC_S0_base), see “Address Map Details” in the Address Map section.

Table 11.3-1 Address Space (SYC_S0)

Offset Address	Access Target
0000h to 0FFFh	PSELCTRL region & PSELCTRL region Management registers
1000h to 1FFFh	PSELREAD region & PSELREAD region Management registers

11.4 Register Description

For details on respective registers, see *the ARM CoreSight SoC-400 Technical Reference Manual 3.10 Timestamp generator*.

11.5 Functional Description

Access control is performed from one APB interface of this unit to two APB interfaces of the timestamp generator. The access to the first 4 Kbytes of the 8-Kbyte address area of the SYC is controlled to the PSELCTRL area, while the access to the second 4 Kbytes is controlled to the PSELREAD area. Only the secure access to the PSELCTRL area is allowed. In case of non-secure access, a slave error response is made.

11.5.1 Halt-on-Debug Function

This unit supports the halt-on-debug function of the timestamp generator.

Section 12 RAM A (RAMA)

This section describes functions of the RAM A (RAMA).

12.1 Functional Overview

This unit is a RAM with ECC error detection and correction functions. This unit has a function to detect and correct errors by ECC of data recorded in the internal RAM. It also has a FIFO function that retains transactions when accesses from various channels to the RAM are in conflict and access is not possible.

Figure 12.1-1 shows the connection diagram of the RAMA.

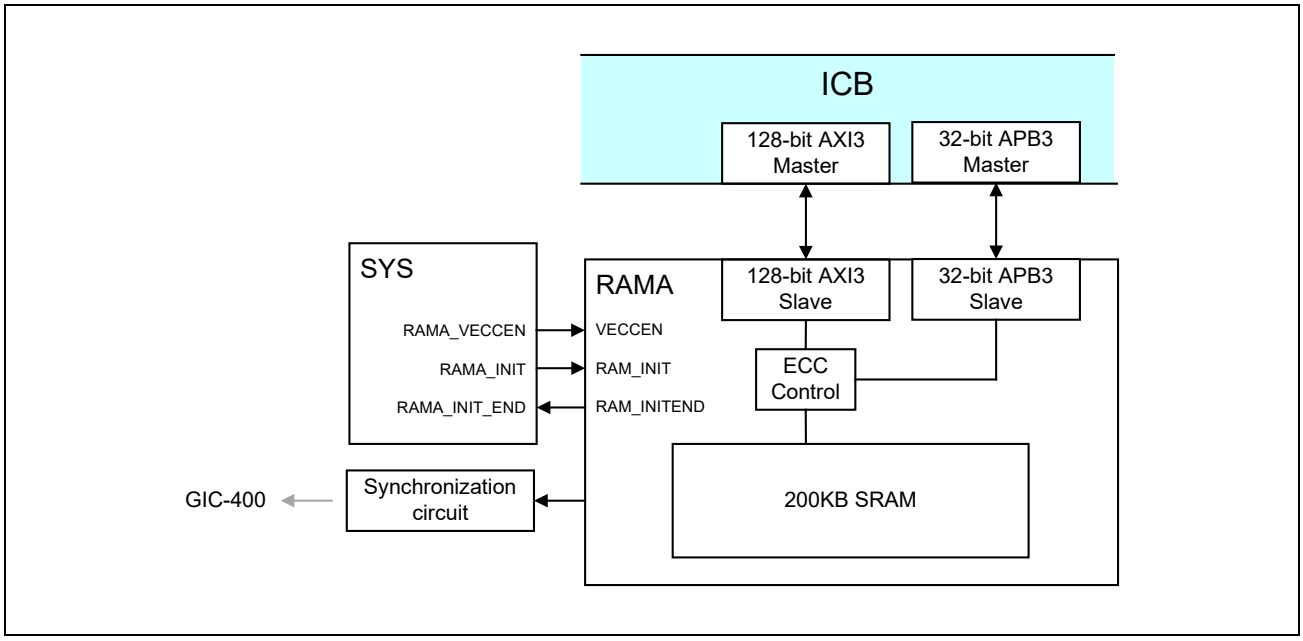


Figure 12.1-1 Connection Diagram

12.2 Pin Functions

12.2.1 List of Internal Pins

Table 12.2-1 lists the internal pins.

Table 12.2-1 List of Internal Pins

Pin name	I/O	Function
RAM Access		
VECCEN	Input	Pin for switching enabling and disabling of error correction by the ECC
ECC Control		
RAM_INIT	Input	Controlling initialization of the RAM ECC code area
RAM_INITEND	Output	Ending initialization of the RAM ECC code area

The following describes the internal pin functions of the RAMA unit.

12.2.1.1 RAM Access

The pin of this category is mainly for controlling the method for RAM access and the restrictions on access.

VECCEN (Input)

This pin is for switching enabling and disabling of error correction by the ECC. The ECC is enabled when the pin is fixed to the high level and disabled when it is fixed to the low level. For details of the functions of this pin, see **Section 12.5.1.2, VECCEN Pin Functions**. Note that this signal is synchronized through a two-2-FF synchronizer with which it goes to the high level at the time of a reset.

12.2.1.2 ECC Control

The pins of this category are related to the ECC macro and ECC control. Three interrupt outputs are the signals bundled with multiple interrupt output signals of the ECC macro. For details of the connection, see **Section 12.5.1.4, Error Detection and Correction Function**.

RAM_INIT (Input), RAM_INITEND (Output)

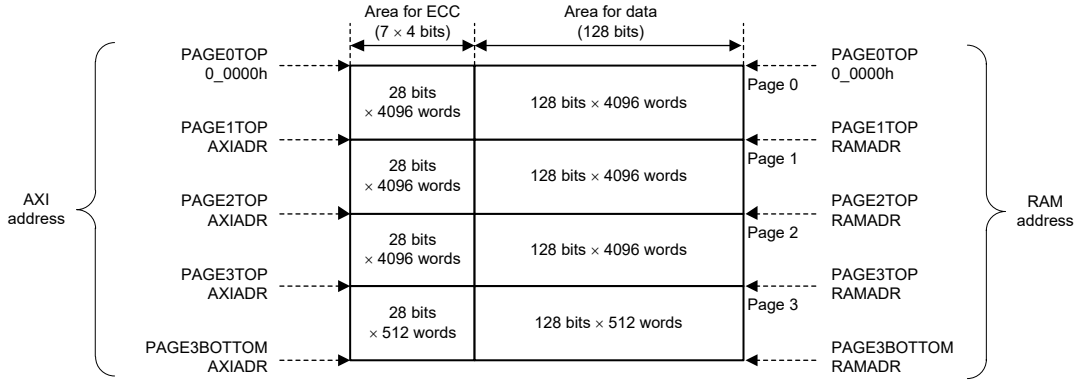
When RAM_INIT is changed from the low to the high level and the clock is input, RAM_INITEND changes from the low to the high level after certain clock cycles, and the internal RAM data and the whole area of the ECC code are initialized.

12.3 Address Space

This unit has a retention RAM area and a register area separately.

Figure 12.3-1 shows the retention RAM area. **Figure 12.3-2** shows the register area.

For the base address of the register (<RAMA_S1_base>), see “Address Map Details” in the Address Map section.



	RAM area (200-KB)	
Mapping position	AXIADR	RAMADR
PAGE1TOP	1_0000h	0_1000h
PAGE2TOP	2_0000h	0_2000h
PAGE3TOP	3_0000h	0_3000h
PAGE3BOTTOM	3_1FFFh	0_31FFh

Figure 12.3-1 Memory Map of RAM

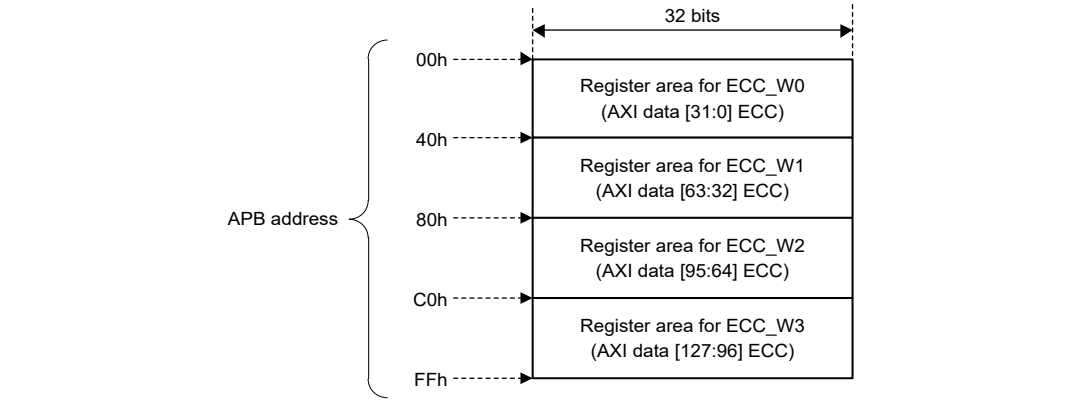


Figure 12.3-2 Memory Map of Register

12.4 Register Description

For the base address of the register (<RAMA_S1_base>), see the Address Map section.

12.4.1 List of Registers

Table 12.4-1 is the list of registers.

Table 12.4-1 List of Registers (1/2)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
ECC_W0				
00h	ECC Control Register	RAMA_Wm_EC710CTL	0000_001xh*1	32
04h to 0Ch	Reserved (When reading, 0 is always read.)	—	0000_0000h	32
10h	ECC Error Address Register 0	RAMA_Wm_EC710EAD0	0000_0000h	32
14h	ECC Error Address Register 1	RAMA_Wm_EC710EAD1	0000_0000h	32
18h	ECC Error Address Register 2	RAMA_Wm_EC710EAD2	0000_0000h	32
1Ch	ECC Error Address Register 3	RAMA_Wm_EC710EAD3	0000_0000h	32
20h	ECC Error Address Register 4	RAMA_Wm_EC710EAD4	0000_0000h	32
24h	ECC Error Address Register 5	RAMA_Wm_EC710EAD5	0000_0000h	32
28h	ECC Error Address Register 6	RAMA_Wm_EC710EAD6	0000_0000h	32
2Ch	ECC Error Address Register 7	RAMA_Wm_EC710EAD7	0000_0000h	32
30h to 3Ch	Reserved (When reading, 0 is always read.)	—	0000_0000h	32
ECC_W1				
40h	ECC Control Register	RAMA_Wm_EC710CTL	0000_001xh*1	32
44h to 4Ch	Reserved (When reading, 0 is always read.)	—	0000_0000h	32
50h	ECC Error Address Register 0	RAMA_Wm_EC710EAD0	0000_0000h	32
54h	ECC Error Address Register 1	RAMA_Wm_EC710EAD1	0000_0000h	32
58h	ECC Error Address Register 2	RAMA_Wm_EC710EAD2	0000_0000h	32
5Ch	ECC Error Address Register 3	RAMA_Wm_EC710EAD3	0000_0000h	32
60h	ECC Error Address Register 4	RAMA_Wm_EC710EAD4	0000_0000h	32
64h	ECC Error Address Register 5	RAMA_Wm_EC710EAD5	0000_0000h	32
68h	ECC Error Address Register 6	RAMA_Wm_EC710EAD6	0000_0000h	32
6Ch	ECC Error Address Register 7	RAMA_Wm_EC710EAD7	0000_0000h	32
70h to 7Ch	Reserved (When reading, 0 is always read.)	—	0000_0000h	32

Table 12.4-1 List of Registers (2/2)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
ECC_W2				
80h	ECC Control Register	RAMA_Wm_EC710CTL	0000_001xh*1	32
84h to 8Ch	Reserved (When reading, 0 is always read.)	—	0000_0000h	32
90h	ECC Error Address Register 0	RAMA_Wm_EC710EAD0	0000_0000h	32
94h	ECC Error Address Register 1	RAMA_Wm_EC710EAD1	0000_0000h	32
98h	ECC Error Address Register 2	RAMA_Wm_EC710EAD2	0000_0000h	32
9Ch	ECC Error Address Register 3	RAMA_Wm_EC710EAD3	0000_0000h	32
A0h	ECC Error Address Register 4	RAMA_Wm_EC710EAD4	0000_0000h	32
A4h	ECC Error Address Register 5	RAMA_Wm_EC710EAD5	0000_0000h	32
A8h	ECC Error Address Register 6	RAMA_Wm_EC710EAD6	0000_0000h	32
ACh	ECC Error Address Register 7	RAMA_Wm_EC710EAD7	0000_0000h	32
B0h to BCh	Reserved (When reading, 0 is always read.)	—	0000_0000h	32
ECC_W3				
C0h	ECC Control Register	RAMA_Wm_EC710CTL	0000_001xh*1	32
C4h to CCh	Reserved (When reading, 0 is always read.)	—	0000_0000h	32
D0h	ECC Error Address Register 0	RAMA_Wm_EC710EAD0	0000_0000h	32
D4h	ECC Error Address Register 1	RAMA_Wm_EC710EAD1	0000_0000h	32
D8h	ECC Error Address Register 2	RAMA_Wm_EC710EAD2	0000_0000h	32
DCh	ECC Error Address Register 3	RAMA_Wm_EC710EAD3	0000_0000h	32
E0h	ECC Error Address Register 4	RAMA_Wm_EC710EAD4	0000_0000h	32
E4h	ECC Error Address Register 5	RAMA_Wm_EC710EAD5	0000_0000h	32
E8h	ECC Error Address Register 6	RAMA_Wm_EC710EAD6	0000_0000h	32
ECh	ECC Error Address Register 7	RAMA_Wm_EC710EAD7	0000_0000h	32
F0h to FCh	Reserved (When reading, 0 is always read.)	—	0000_0000h	32

Note 1. Bit 0 is undefined.

12.4.2 Register Descriptions

The function description of each register is given below.

12.4.2.1 ECC Control Register (RAMA_Wm_EC710CTL) (m = 0 to 3)

This register controls the status and mode of the ECC macro.

Note: Write to the control bits (bits 7 to 3) of this register when AXI access is not performed.

Access Size: 32 bits

Address(es): <RAMA_S1_base> + 0000h
<RAMA_S1_base> + 0040h
<RAMA_S1_base> + 0080h
<RAMA_S1_base> + 00C0h

Initial Value: 0000_001xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ECDEDF7	ECSEDF7	ECDEDF6	ECSEDF6	ECDEDF5	ECSEDF5	ECDEDF4	ECSEDF4	ECDEDF3	ECSEDF3	ECDEDF2	ECSEDF2	ECDEDF1	ECSEDF1	ECDEDF0	ECSEDF0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EMCA[1:0]		—	—	ECOVFF	ECER2C	ECER1C	—	ECTHM	ECERVF	EC1ECP	EC2EDIC	EC1EDIC	ECER2F	ECER1F	ECEMF
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	x
R/W	RW	RW	R	R	R	RW	RW	R	RW	RW	RW	RW	RW	R	R	R

Table 12.4-2 RAMA_Wm_EC710CTL Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 16	ECDEDF[7:0] ECSEDF[7:0]	ECDEDF[7:0]: 2-bit error detection flag ECSE1F[7:0]: 1-bit error detection flag This bit is a flag indicating an error if stored in the error address register when error detection is enabled. 1b is set to ECSEDF[7:0] for a 1-bit error and to ECDEDF[7:0] for a 2-bit error. Since this bit is read-only, writing a value does not reflect it. This bit is cleared by writing 1b to ECER2C and ECER1C of bits 10 and 9, respectively.
15, 14	EMCA[1:0]	Access control bit to ECC mode selection bit These bits are the write trigger bits for bits 7 and 6 and the value of these bits is always 0b at normal times. Writing 01b to these bits enables write to bits 7 and 6.
13, 12	—	Reserved. The write value should be always 0b.
11	ECOVFF	ECC overflow detection flag If a new error address is detected with all error address registers holding an error address, this bit sets a flag and an overflow interrupt is output. This bit is read-only and should be cleared with bits 10 and 9. 0b: No overflow has occurred after resetting or after clearing this bit by bits 10 and 9. 1b: Indicates that the error address register has overflowed.
10	ECER2C	2-bit ECC error detection flag clear bit The read value is always 0, and the 2-bit error flag bit ECER2F is cleared by writing 1b. The overflow detection flag ECOVFF, ECC 2-bit error detection flag ECDEDF[7:0], and ECC 1-bit error detection flag ECSEDF[7:0] are also cleared. Clearing this bit has priority in the case of a conflict with the 2-bit ECC error detection flag factor. The internal state does not change when 0b is written to this bit.

Table 12.4-2 RAMA_Wm_EC710CTL Register Contents (2/2)

Bit Position	Bit Name	Description
9	ECER1C	1-bit ECC error detection flag clear bit The read value is always 0, and the 1-bit error flag bit ECER1F is cleared by writing 1b. The overflow detection flag ECOVFF, ECC 2-bit error detection flag ECDEDF[7:0], and ECC 1-bit error detection flag ECSEDF[7:0] are also cleared. Clearing this bit has priority in the case of a conflict with the 1-bit ECC error detection flag factor. The internal state does not change when 0b is written to this bit.
8	—	Reserved. The write value should be always 0b.
7	ECTHM	ECC function bypass mode selection bit This bit selects the ECC decoding operation and does not affect the encoding side. To change this bit, it is necessary to permit writing by simultaneously writing 01 to bits 15 and 14. 0b: Prohibit bypass mode (normal mode, initial value) 1b: Permit bypass mode. It does not affect the encode side, and error detection and error correction is not operated in the decode side.
6	ECERVF	ECC error judgement permission flag bit Set 1b to enable error judgement. The operation set to EC1ECP of bit 5 and error detection interrupts of bits 4 and 3 will be performed. To change this bit, simultaneously write 01b to bits 15 and 14 for write permission.
5	EC1ECP	1-bit error correction permission bit This bit allows 1-bit error correction when ECC error detection is enabled. 0b: Correct error if 1-bit error is detected. 1b: Not correct error if 1-bit error is detected.
4	EC2EDIC	2-bit error detection interrupt control bit This bit controls the output of 2-bit error interrupt when 2-bit error is detected. 2-bit error interrupt EC7TIE2 is output by setting 1b. 0b: Not output 2-bit error detection interrupt 1b: Output 2-bit error detection interrupt. (initial value)
3	EC1EDIC	1-bit error detection interrupt control bit This bit controls the output of 1-bit error interrupt when 1-bit error is detected. 1-bit error interrupt EC7TIE1 is output by setting 1b. 0b: Not output 1-bit error detection interrupt. (initial value) 1b: Output 1-bit error detection interrupt.
2	ECER2F	2-bit error detection / correction flag bit This bit is flagged when a 2-bit error is detected in the 39-bit macro input data with error judgment enabled. At this time, if output of 2-bit error interrupt is enabled, EC7TIE2 interrupt is output. 0b: 2-bit error does not occur after reset or after the bit is cleared. 1b: 2-bit error occurs after reset or after the bit is cleared.
1	ECER1F	1-bit error detection / correction flag bit This bit is flagged when a 1-bit error is detected in the 39-bit macro input data with error judgment enabled. At this time, if output of 1-bit error interrupt is enabled, EC7TIE1 interrupt is output. 0b: 1-bit error does not occur after reset or after the bit is cleared. 1b: 1-bit error occurs after reset or after the bit is cleared.
0	ECEMF	ECC error indication flag This bit indicates that there is an error in the current read data. This data is updated for each output of RAM output data. 0b: No error is detected in the data input to the decoding circuit. 1b: The current data is detected error. *This bit is not set to 1b when error judgment is prohibited or ECC bypass mode is set.

12.4.2.2 ECC Error Address Register 0 (RAMA_Wm_EC710EAD0) (m = 3 to 0)

This register is a read-only register that holds the ECC error occurrence address.

Access Size: 32 bits

Address(es): <RAMA_S1_base> + 0010h
<RAMA_S1_base> + 0050h
<RAMA_S1_base> + 0090h
<RAMA_S1_base> + 00D0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ECEAD0[13:0]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 12.4-3 RAMA_Wm_EC710EAD0 Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved
13 to 0	ECEAD0[13:0]	ECC error address register This is a read-only register that captures the RAM address using the detection signal as a trigger and stores it as the ECC error occurrence address from the ECEADn=0th position when an ECC error is detected with error judgment enabled. The bit width of this register changes depending on the RAM mounting area. The read value is always 0b for the other bits. This address register is cleared to 0b together with the flag by clearing the status flag of ECE R2F or ECE R1F.

NOTE

- **Correspondence between AXI address and ECEAD address**

The address stored is a RAM address and is stored as a 128-bit aligned address, it is different from an AXI address that is byte aligned (8 bits). The correspondence between the two is as follows.

The address stored in ECEAD = AXI address >> 4 (4-bit shift right)

- The address indicated by the register of ECC W0 indicates that there was an error in data [31:0] in the corresponding address area of RAM.
- The address indicated by the register of ECC W1 indicates that there was an error in data [63:32] in the corresponding address area of RAM.
- The address indicated by the register of ECC W2 indicates that there was an error in data [95:64] in the corresponding address area of RAM.
- The address indicated by the register of ECC W3 indicates that there was an error in data [127:96] in the corresponding address area of RAM.

For details on AXI addresses and register areas, see the Address Space section.

12.4.2.3 ECC Error Address Register 1 (RAMA_Wm_EC710EAD1) (m = 3 to 0)

This register is a read-only register that holds the ECC error occurrence address.

Access Size: 32 bits

Address(es): <RAMA_S1_base> + 0014h
<RAMA_S1_base> + 0054h
<RAMA_S1_base> + 0094h
<RAMA_S1_base> + 00D4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ECEAD1[13:0]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 12.4-4 RAMA_Wm_EC710EAD1 Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved.
13 to 0	ECEAD1[13:0]	ECC error address register This is a read-only register that captures the RAM address using the detection signal as a trigger and stores it as the ECC error occurrence address from the ECEADn=0th position when an ECC error is detected with error judgment enabled. The bit width of this register changes depending on the RAM mounting area. The read value is always 0b for the other bits. This address register is cleared to 0b together with the flag by clearing the status flag of ECE R2F or ECE R1F.

NOTE

- **Correspondence between AXI address and ECEAD address**

The address stored is a RAM address and is stored as a 128-bit aligned address, it is different from an AXI address that is byte aligned (8 bits). The correspondence between the two is as follows.

The address stored in ECEAD = AXI address >> 4 (4-bit shift right)

- The address indicated by the register of ECC W0 indicates that there was an error in data [31:0] in the corresponding address area of RAM.
- The address indicated by the register of ECC W1 indicates that there was an error in data [63:32] in the corresponding address area of RAM.
- The address indicated by the register of ECC W2 indicates that there was an error in data [95:64] in the corresponding address area of RAM.
- The address indicated by the register of ECC W3 indicates that there was an error in data [127:96] in the corresponding address area of RAM.

For details on AXI addresses and register areas, see the Address Space section.

12.4.2.4 ECC Error Address Register 2 (RAMA_Wm_EC710EAD2) (m = 3 to 0)

This register is a read-only register that holds the ECC error occurrence address.

Access Size: 32 bits

Address(es): <RAMA_S1_base> + 0018h
<RAMA_S1_base> + 0058h
<RAMA_S1_base> + 0098h
<RAMA_S1_base> + 00D8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ECEAD2[13:0]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 12.4-5 RAMA_Wm_EC710EAD2 Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved.
13 to 0	ECEAD2[13:0]	ECC error address register This is a read-only register that captures the RAM address using the detection signal as a trigger and stores it as the ECC error occurrence address from the ECEADn=0th position when an ECC error is detected with error judgment enabled. The bit width of this register changes depending on the RAM mounting area. The read value is always 0b for the other bits. This address register is cleared to 0b together with the flag by clearing the status flag of ECE R2F or ECE R1F.

NOTE

- **Correspondence between AXI address and ECEAD address**

The address stored is a RAM address and is stored as a 128-bit aligned address, it is different from an AXI address that is byte aligned (8 bits). The correspondence between the two is as follows.

The address stored in ECEAD = AXI address >> 4 (4-bit shift right)

- The address indicated by the register of ECC W0 indicates that there was an error in data [31:0] in the corresponding address area of RAM.
- The address indicated by the register of ECC W1 indicates that there was an error in data [63:32] in the corresponding address area of RAM.
- The address indicated by the register of ECC W2 indicates that there was an error in data [95:64] in the corresponding address area of RAM.
- The address indicated by the register of ECC W3 indicates that there was an error in data [127:96] in the corresponding address area of RAM

For details on AXI addresses and register areas, see the Address Space section.

12.4.2.5 ECC Error Address Register 3 (RAMA_Wm_EC710EAD3) (m = 3 to 0)

This register is a read-only register that holds the ECC error occurrence address.

Access Size: 32 bits

Address(es): <RAMA_S1_base> + 001Ch
<RAMA_S1_base> + 005Ch
<RAMA_S1_base> + 009Ch
<RAMA_S1_base> + 00DCh

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ECEAD3[13:0]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 12.4-6 RAMA_Wm_EC710EAD3 Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved.
13 to 0	ECEAD3[13:0]	ECC error address register This is a read-only register that captures the RAM address using the detection signal as a trigger and stores it as the ECC error occurrence address from the ECEADn=0th position when an ECC error is detected with error judgment enabled. The bit width of this register changes depending on the RAM mounting area. The read value is always 0b for the other bits. This address register is cleared to 0b together with the flag by clearing the status flag of ECE R2F or ECE R1F.

NOTE

- **Correspondence between AXI address and ECEAD address**

The address stored is a RAM address and is stored as a 128-bit aligned address, it is different from an AXI address that is byte aligned (8 bits). The correspondence between the two is as follows.

The address stored in ECEAD = AXI address >> 4 (4-bit shift right)

- The address indicated by the register of ECC W0 indicates that there was an error in data [31:0] in the corresponding address area of RAM.
- The address indicated by the register of ECC W1 indicates that there was an error in data [63:32] in the corresponding address area of RAM.
- The address indicated by the register of ECC W2 indicates that there was an error in data [95:64] in the corresponding address area of RAM.
- The address indicated by the register of ECC W3 indicates that there was an error in data [127:96] in the corresponding address area of RAM.

For details on AXI addresses and register areas, see the Address Space section.

12.4.2.6 ECC Error Address Register 4 (RAMA_Wm_EC710EAD4) (m = 3 to 0)

This register is a read-only register that holds the ECC error occurrence address.

Access Size: 32 bits

Address(es): <RAMA_S1_base> + 0020h
<RAMA_S1_base> + 0060h
<RAMA_S1_base> + 00A0h
<RAMA_S1_base> + 00E0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ECEAD4[13:0]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 12.4-7 RAMA_Wm_EC710EAD4 Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved.
13 to 0	ECEAD4[13:0]	ECC error address register This is a read-only register that captures the RAM address using the detection signal as a trigger and stores it as the ECC error occurrence address from the ECEADn=0th position when an ECC error is detected with error judgment enabled. The bit width of this register changes depending on the RAM mounting area. The read value is always 0b for the other bits. This address register is cleared to 0b together with the flag by clearing the status flag of ECE R2F or ECE R1F.

NOTE

- **Correspondence between AXI address and ECEAD address**

The address stored is a RAM address and is stored as a 128-bit aligned address, it is different from an AXI address that is byte aligned (8 bits). The correspondence between the two is as follows.

The address stored in ECEAD = AXI address >> 4 (4-bit shift right)

- The address indicated by the register of ECC W0 indicates that there was an error in data [31:0] in the corresponding address area of RAM.
- The address indicated by the register of ECC W1 indicates that there was an error in data [63:32] in the corresponding address area of RAM.
- The address indicated by the register of ECC W2 indicates that there was an error in data [95:64] in the corresponding address area of RAM.
- The address indicated by the register of ECC W3 indicates that there was an error in data [127:96] in the corresponding address area of RAM.

For details on AXI addresses and register areas, see the Address Space section.

12.4.2.7 ECC Error Address Register 5 (RAMA_Wm_EC710EAD5) (m = 3 to 0)

This register is a read-only register that holds the ECC error occurrence address.

Access Size: 32 bits

Address(es): <RAMA_S1_base> + 0024h
<RAMA_S1_base> + 0064h
<RAMA_S1_base> + 00A4h
<RAMA_S1_base> + 00E4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ECEAD5[13:0]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 12.4-8 RAMA_Wm_EC710EAD5 Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved.
13 to 0	ECEAD5[13:0]	ECC error address register This is a read-only register that captures the RAM address using the detection signal as a trigger and stores it as the ECC error occurrence address from the ECEADn=0th position when an ECC error is detected with error judgment enabled. The bit width of this register changes depending on the RAM mounting area. The read value is always 0b for the other bits. This address register is cleared to 0b together with the flag by clearing the status flag of ECE R2F or ECE R1F.

NOTE

- **Correspondence between AXI address and ECEAD address**

The address stored is a RAM address and is stored as a 128-bit aligned address, it is different from an AXI address that is byte aligned (8 bits). The correspondence between the two is as follows.

The address stored in ECEAD = AXI address >> 4 (4-bit shift right)

- The address indicated by the register of ECC W0 indicates that there was an error in data [31:0] in the corresponding address area of RAM.
- The address indicated by the register of ECC W1 indicates that there was an error in data [63:32] in the corresponding address area of RAM.
- The address indicated by the register of ECC W2 indicates that there was an error in data [95:64] in the corresponding address area of RAM.
- The address indicated by the register of ECC W3 indicates that there was an error in data [127:96] in the corresponding address area of RAM.

For details on AXI addresses and register areas, see the Address Space section.

12.4.2.8 ECC Error Address Register 6 (RAMA_Wm_EC710EAD6) (m = 3 to 0)

This register is a read-only register that holds the ECC error occurrence address.

Access Size: 32 bits

Address(es): <RAMA_S1_base> + 0028h
<RAMA_S1_base> + 0068h
<RAMA_S1_base> + 00A8h
<RAMA_S1_base> + 00E8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ECEAD6[13:0]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 12.4-9 RAMA_Wm_EC710EAD6 Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved.
13 to 0	ECEAD6[13:0]	ECC error address register This is a read-only register that captures the RAM address using the detection signal as a trigger and stores it as the ECC error occurrence address from the ECEADn=0th position when an ECC error is detected with error judgment enabled. The bit width of this register changes depending on the RAM mounting area. The read value is always 0b for the other bits. This address register is cleared to 0b together with the flag by clearing the status flag of ECE R2F or ECE R1F.

NOTE

- **Correspondence between AXI address and ECEAD address**

The address stored is a RAM address and is stored as a 128-bit aligned address, it is different from an AXI address that is byte aligned (8 bits). The correspondence between the two is as follows.

The address stored in ECEAD = AXI address >> 4 (4-bit shift right)

- The address indicated by the register of ECC W0 indicates that there was an error in data [31:0] in the corresponding address area of RAM.
- The address indicated by the register of ECC W1 indicates that there was an error in data [63:32] in the corresponding address area of RAM.
- The address indicated by the register of ECC W2 indicates that there was an error in data [95:64] in the corresponding address area of RAM.
- The address indicated by the register of ECC W3 indicates that there was an error in data [127:96] in the corresponding address area of RAM.

For details on AXI addresses and register areas, see the Address Space section.

12.4.2.9 ECC Error Address Register 7 (RAMA_Wm_EC710EAD7) (m = 3 to 0)

This register is a read-only register that holds the ECC error occurrence address.

Access Size: 32 bits

Address(es): <RAMA_S1_base> + 002Ch
<RAMA_S1_base> + 006Ch
<RAMA_S1_base> + 00Ach
<RAMA_S1_base> + 00ECh

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ECEAD7[13:0]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 12.4-10 RAMA_Wm_EC710EAD7 Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved.
13 to 0	ECEAD7[13:0]	ECC error address register This is a read-only register that captures the RAM address using the detection signal as a trigger and stores it as the ECC error occurrence address from the ECEADn=0th position when an ECC error is detected with error judgment enabled. The bit width of this register changes depending on the RAM mounting area. The read value is always 0b for the other bits. This address register is cleared to 0b together with the flag by clearing the status flag of ECE R2F or ECE R1F.

NOTE

- **Correspondence between AXI address and ECEAD address**

The address stored is a RAM address and is stored as a 128-bit aligned address, it is different from an AXI address that is byte aligned (8 bits). The correspondence between the two is as follows.

The address stored in ECEAD = AXI address >> 4 (4-bit shift right)

- The address indicated by the register of ECC W0 indicates that there was an error in data [31:0] in the corresponding address area of RAM.
- The address indicated by the register of ECC W1 indicates that there was an error in data [63:32] in the corresponding address area of RAM.
- The address indicated by the register of ECC W2 indicates that there was an error in data [95:64] in the corresponding address area of RAM.
- The address indicated by the register of ECC W3 indicates that there was an error in data [127:96] in the corresponding address area of RAM.

For details on AXI addresses and register areas, see the Address Space section.

12.5 Functional Description

In subsequent sections, the register name prefix (RAMA_) is omitted.

12.5.1 ECC Control Function

12.5.1.1 ECC Macro

This unit generates 7-bit ECC code for 32-bit data during encoding, and can detect and correct errors by inputting these data and ECC data during decoding.

For this unit, error detection and correction is performed for 128-bit data by generating 7-bit ECC codes using ECC macros for every 32 bits, for a total of 28 bits. The ECC macro function can store up to eight addresses where errors have occurred in registers, which can be read from the APB. Various interrupts (1-bit error detection, 2-bit error detection, and error address overflow) can be generated at this time.

12.5.1.2 VECCEN Pin Functions

The operations are as follows when VECCEN = 1.

- Controls so that the ECC code is written to the redundant bit RAM.
- Control by the ECC control circuit is applied to perform read-modify-write operation at the time of partial writing other than 32-, 64-, 96-, or 128-bit access.

The operations are as follows when VECCEN = 0.

- Controls so that the ECC code is not written to the redundant bit RAM.
- The results of ECC calculation are not reflected in input/output data.

Note that, if error detection of the ECC macro and interrupt output are enabled, an unintended interrupt may occur, so be sure to set masking.

12.5.1.3 Procedure for Switching VECCEN

For the flow of switching VECCEN, see **Section 12.5.2, Initialization Flow**.

12.5.1.4 Error Detection and Correction Function

(1) ECC Error Correction and Detection Function

The following functions are realized by the ECC macro in this unit. The following functions can be controlled by the registers in the ECC macro.

- Encoding of ECC codes for data stored in RAM
- Decoding from data stored in RAM and ECC code
- 1-bit error correction by the above decoding
- 2-bit error detection by the above decoding
- Interrupt control and flag retention for 1-bit error correction and 2-bit error detection

The error judgment and overflow interrupt output from this unit is connected to the internal ECC macro as shown below, and is output one clk later than the ECC macro interrupt output.

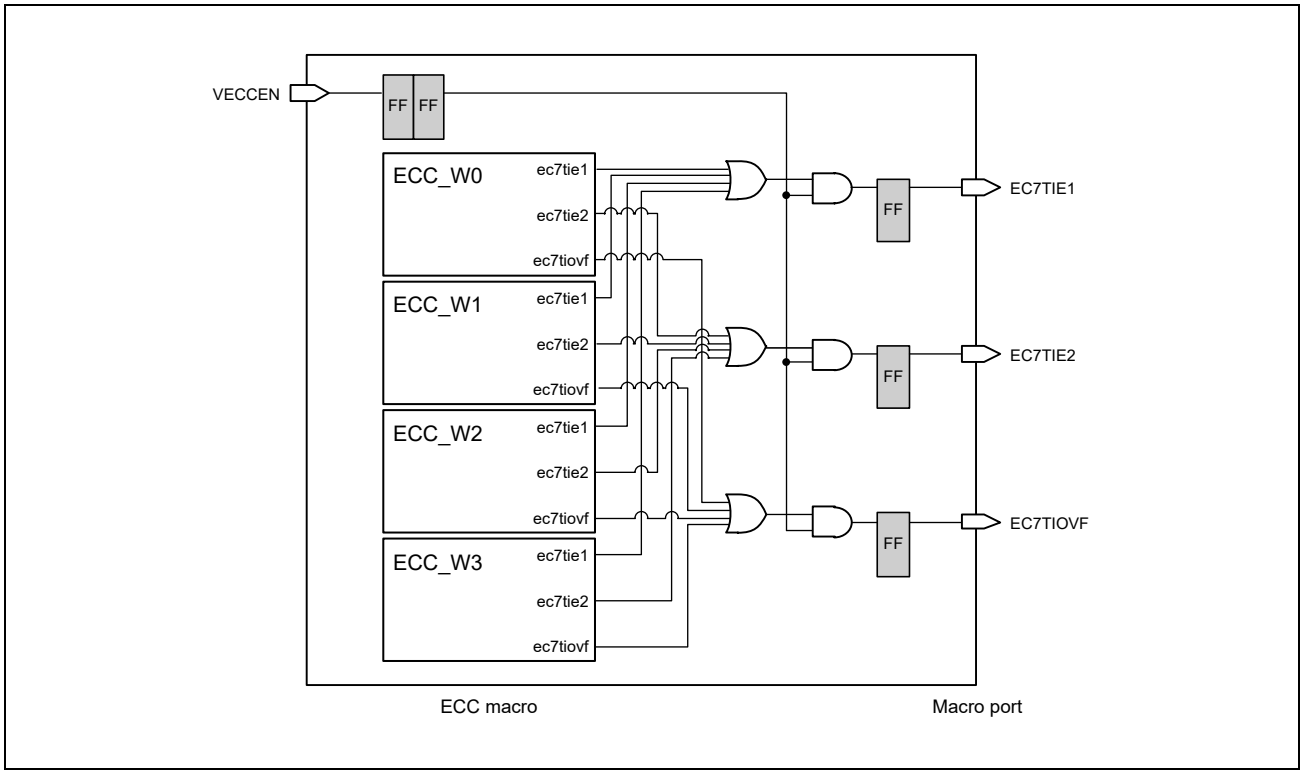


Figure 12.5-1 Connection between ECC Macro Interrupt Output and Macro Interrupt

12.5.1.5 ECC Error Address Retention and Address Register Overflow

(1) ECC Error Address Retention Register

The ECC macro in this unit has a function to capture addresses by triggering an error detection. The captured address is stored in the error address register in the ECC macro, and eight such address registers are included. Each time a different address or error factor occurs, the address at that time is stored in the error address register in the next stage.The flag indicating the error factor of the captured address is held in the upper 16 bits of the EC710CTL register.

When a 2-bit ECC error or 1-bit ECC error is detected with ECC error judgment enabled, the detection signal is used as a trigger to capture the address of the factor and hold it in the error address register (Wx_EC710EADn). In this case, set the ECDEDFm and ECSEDFm of the upper 16 bits of the Wx_EC710CTL register to indicate the applicable error. "m" in ECDEDFm and ECSEDFm refers to Wx_EC710EADn.

(*Example*)

If the error that occurred at the address stored in the error address register Wx_EC710EAD2 is a 2-bit error, ECDEDF2 is set to 1; if it is a 1-bit error, ECSEDF2 is set to 1.

(2) Address Holding Register Overflow

An interrupt is output when a new error address is detected while the error address has already been stored in all the error address holding registers. (A new error address here refers to an address other than the one stored in the error address register, or an error address with a different error factor in an already stored address.)

CAUTION

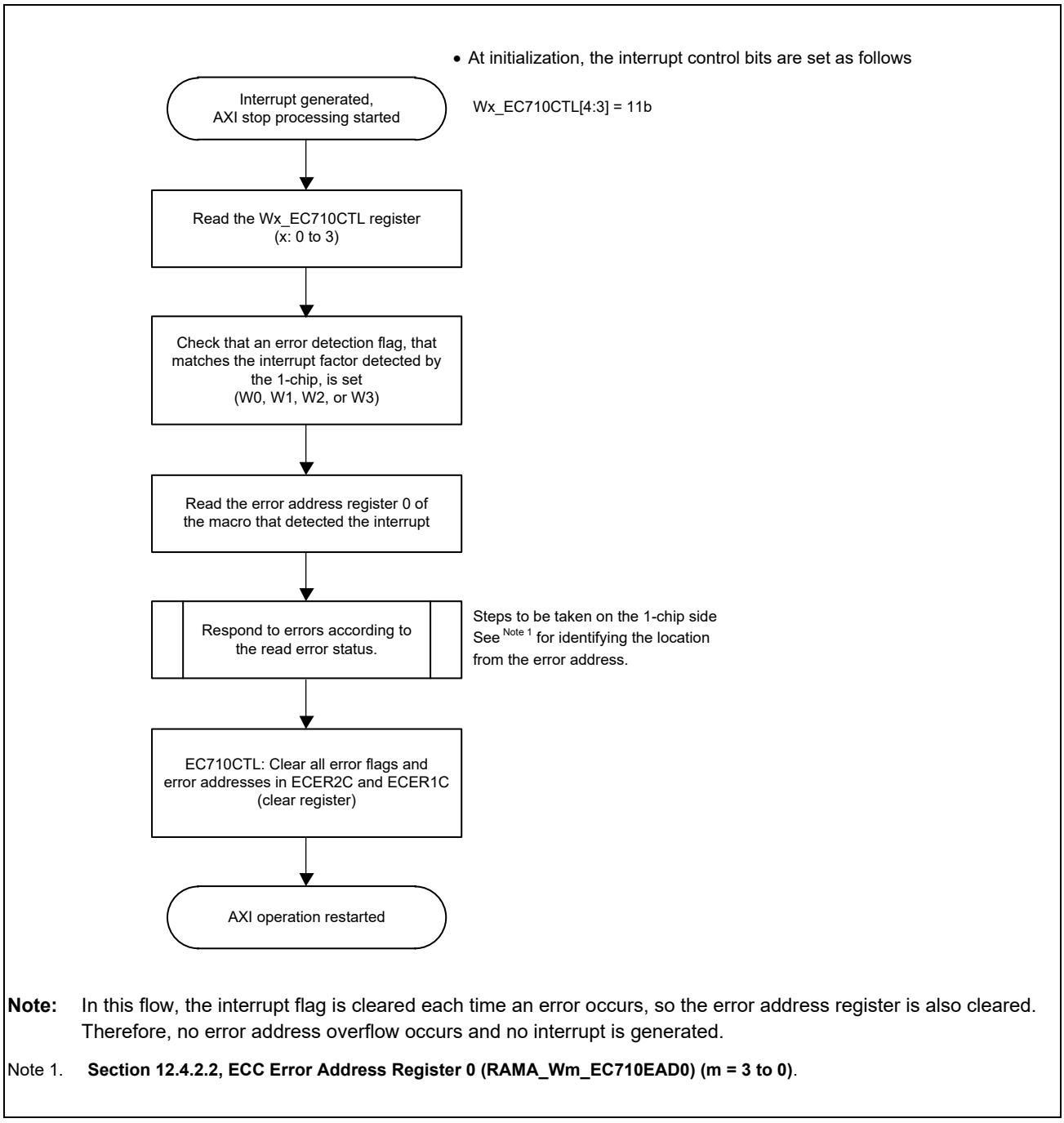
Normally, the error address will not be overwritten by the error address when the error address register overflows. Only when a 2-bit error occurs with all 8 registers filled with 1-bit error addresses (when the error address register detection flags are all 1-bit errors), ECC error address register 7 will be overwritten with the overflowed 2-bit error address. At this time, if 2-bit error interrupt is enabled, 2-bit error interrupt and overflow interrupt will be output. If 2-bit error interrupt is disabled, only overflow interrupt will be output.

12.5.1.6 Interrupt Processing Flow

The following are two examples of the processing flow after various error interruptions.

(1) Flow for Processing Every Error Interrupt

In this flow, all error interrupts are unmasked, and processing is performed for every error that occurs. Stop AXI access before starting the flow.



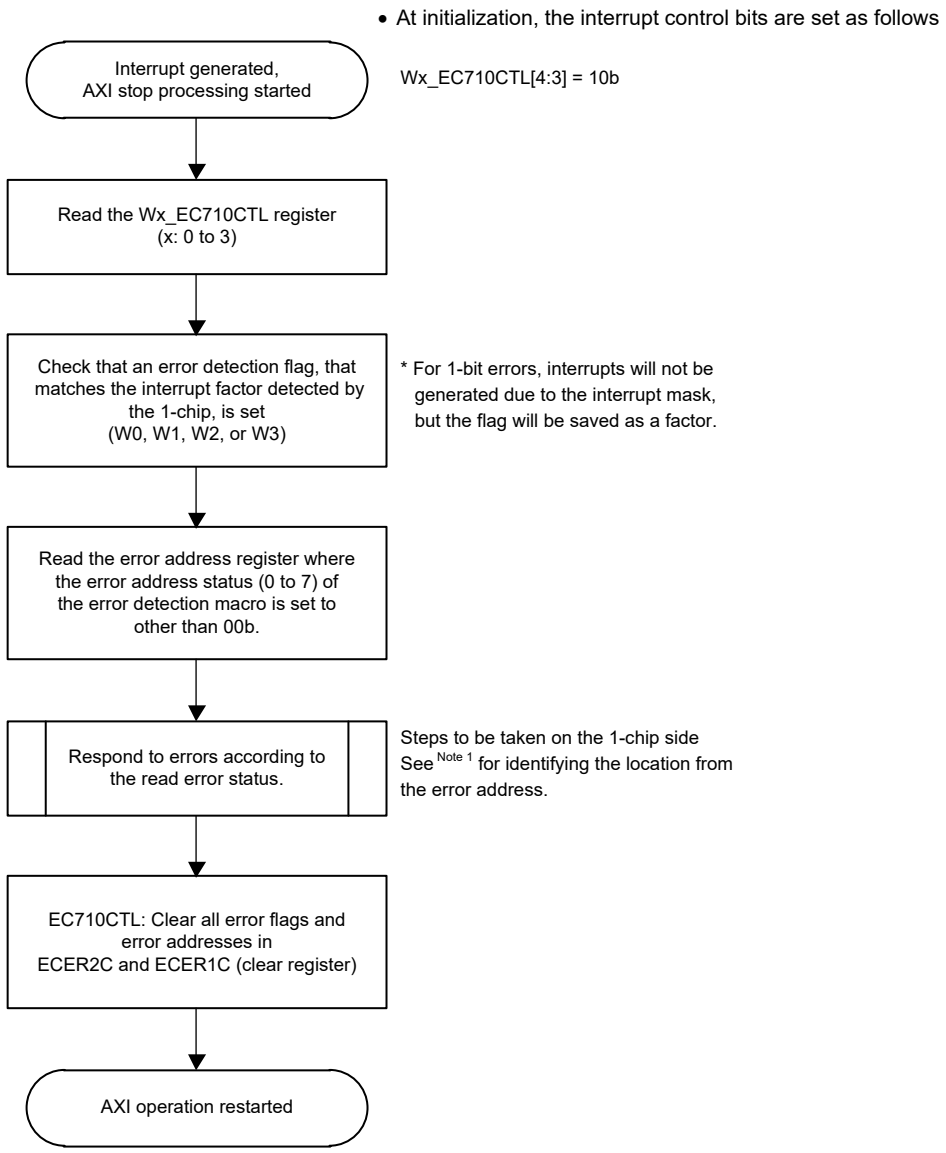
Note: In this flow, the interrupt flag is cleared each time an error occurs, so the error address register is also cleared. Therefore, no error address overflow occurs and no interrupt is generated.

Note 1. **Section 12.4.2.2, ECC Error Address Register 0 (RAMA_Wm_EC710EAD0) (m = 3 to 0)**.

Fiugure 12.5-2 Flow for Processing Every Error Interrupt (Release All Interrupt Masks)

(2) Flow for Processing 2-bit Error and Overflow Interrupt

This flow assumes that 1-bit errors will be corrected, and that 1-bit error interrupts will be masked, and 2-bit errors and overflows will be handled. As in the flow described in **Section 12.5.1.6(1), Flow for Processing Every Error Interrupt**, stop AXI access before starting the flow.



Note: In this flow, when an overflow interrupt occurs, if the error address status EC710CTL[31:16] of the generated macro is 5555h and EC710CTL[2] is 1, an overflow has occurred due to a 2-bit error, and the error address register 7 is overwritten by the 2-bit error address.

Note 1. **Section 12.4.2.2, ECC Error Address Register 0 (RAMA_Wm_EC710EAD0) (m = 3 to 0)** and **Section 12.5.1.5, ECC Error Address Retention and Address Register Overflow**.

Figure 12.5-3 Flow to be Processed at 2-bit Error and Overflow Interrupt (1-bit Error Interrupt Masked)

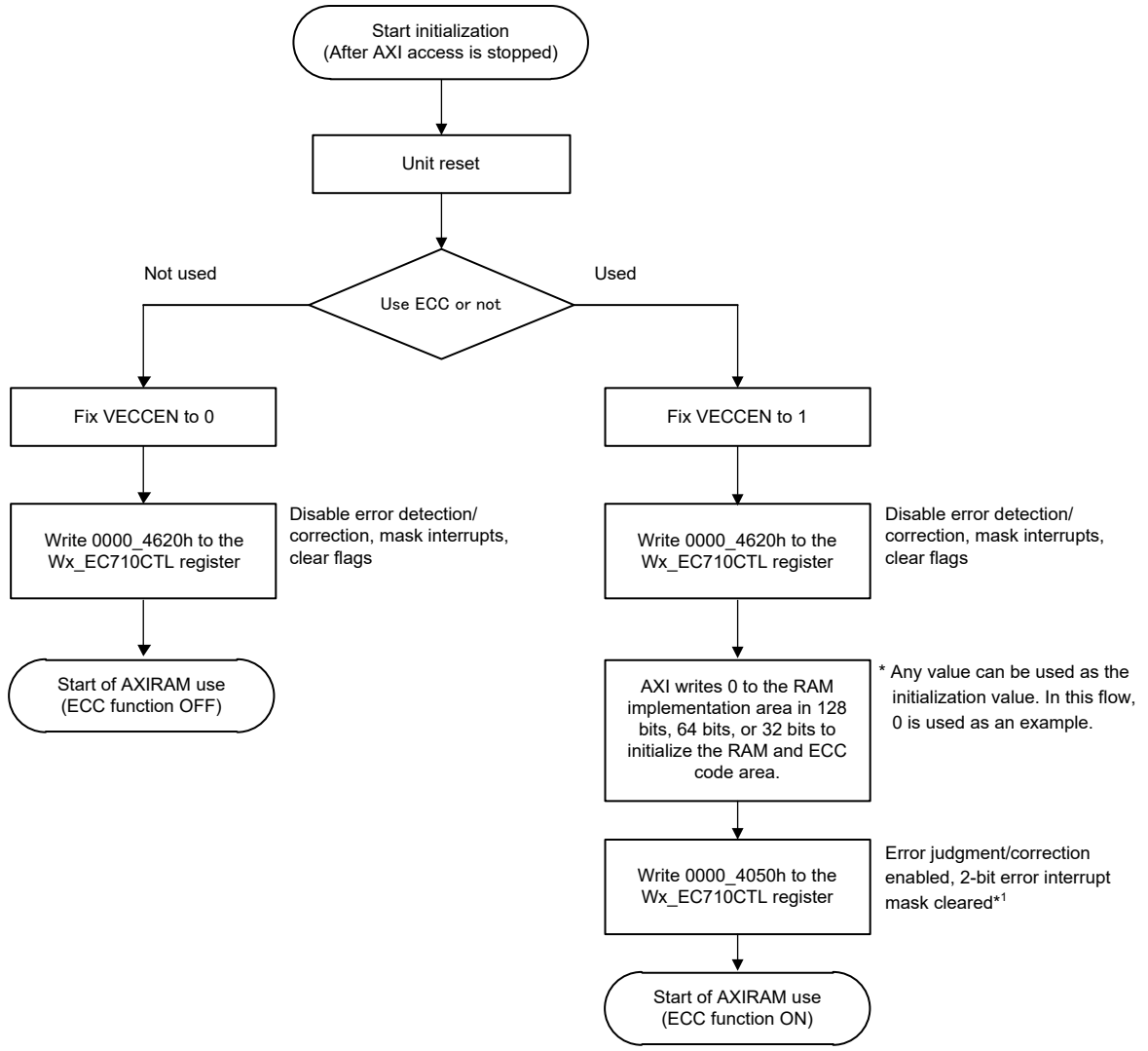
12.5.2 Initialization Flow

The procedure for initializing the unit is shown below. When initializing, stop normal access from AXI and reset the unit before doing so.

The initialization flow is shown below. There are two different flows depending on whether the RAM is initialized by S/W or H/W.

In this product, VECCEN, RAM_INIT, and RAM_INITEND are connected to the SYS unit and have control/monitoring registers (SYS_RAMA_ECC_CNT, SYS_RAMA_INIT, SYS_RAMA_INIT_END) for the corresponding signals.

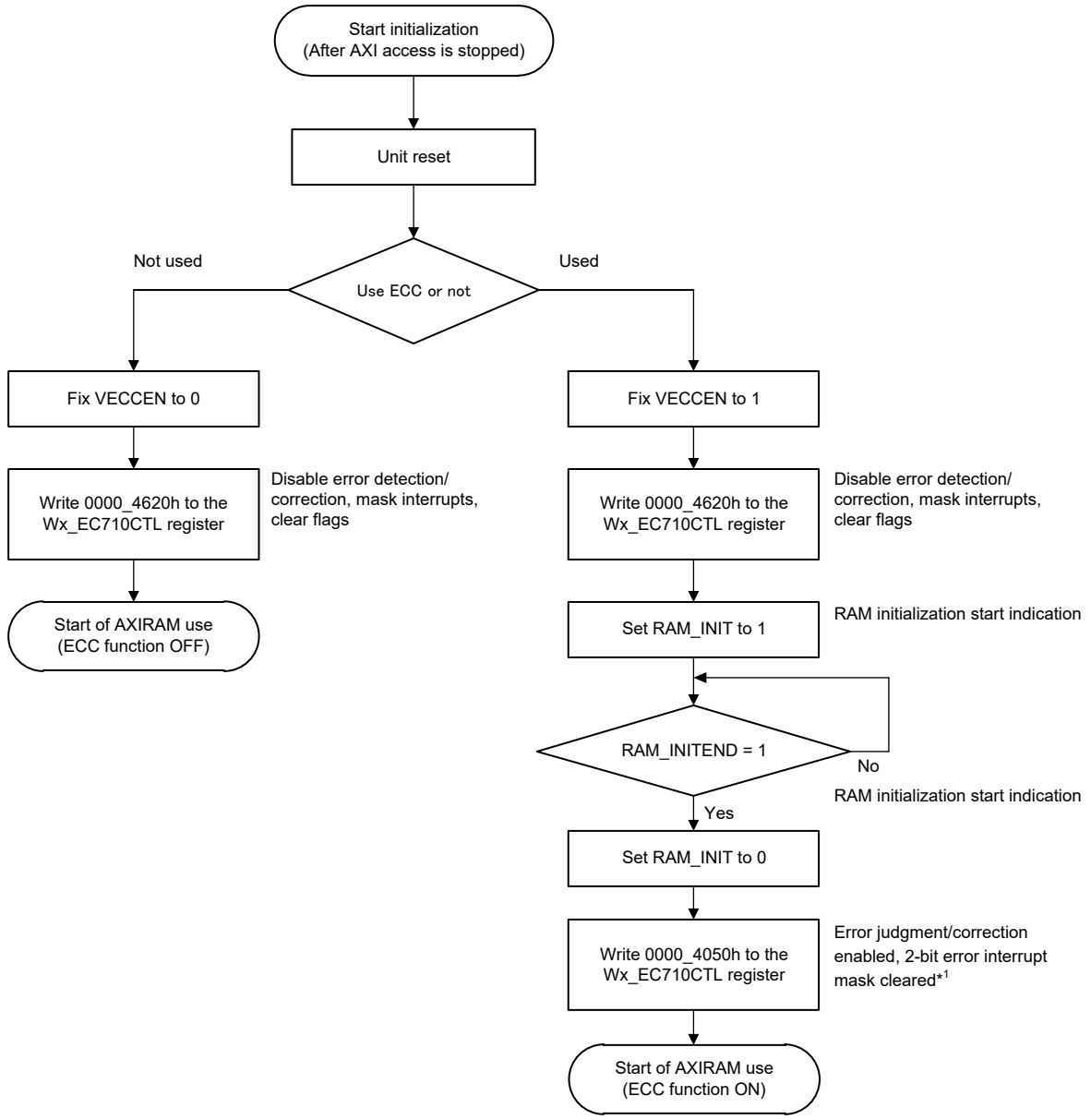
12.5.2.1 When Initializing RAM with S/W



Note 1. For the value of the interrupt control bits, change the write value depending on the usage conditions.

Figure 12.5-4 Initialization Flow by S/W

12.5.2.2 When Initializing RAM with H/W



Note 1. For the value of the interrupt control bits, change the write value depending on the usage conditions.

Figure 12.5-5 Initialization Flow by H/W

12.6 Usage Notes

12.6.1 Priority for Simultaneous Write and Read Access

Since AXI has separate write and read channels, it may receive write and read requests at the same time. The priority of simultaneous requests is as follows.

- When there is no access, Read has priority.
- If simultaneous accesses occur after a Read access, Write has priority.
- When simultaneous accesses occur after a Read access, Read has priority.

If it continues to accept requests at the same time, Write and Read will be processed alternately after Read is executed. Therefore, if Read and Write are performed to the same address at the same time, the order in which they are reflected in RAM will change with each access. To keep the order of Write and Read accesses to the same address, wait for one of the Read or Write cycles to finish on the master side before generating the other cycle.

12.6.2 Exclusive Access

When an exclusive read is performed for the same access information with different AxIDs (AXI bus IDs), the portion of the exclusive read that can be monitored succeeds, and the AxID and address information are monitored separately. After this, when an exclusive write is performed, the exclusive access succeeds only for the first exclusive write that has occurred, and the exclusive access monitor for the same AxID, including its own and others, which was set in the same access information, is cleared, and subsequent exclusive writes fail.

12.6.3 ECC Error Address Retention and Address Register Overflow

Normally, the error address will not be overwritten by the error address when the error address register overflows. Only when a 2-bit error occurs with all 8 registers filled with 1-bit error addresses (when the error address register detection flags are all 1-bit errors), ECC error address register 7 will be overwritten with the overflowed 2-bit error address. At this time, if 2-bit error interrupt is enabled, 2-bit error interrupt and overflow interrupt will be output. If 2-bit error interrupt is disabled, only overflow interrupt will be output.

Section 13 RAM B (RAMB)

This section describes the functions of RAM B (RAMB).

13.1 Functional Overview

The RAMB is mainly used by the CA53 for boot and work areas.

The RAMB has a capacity of 1 MB and consists of four 256-KB SRAMs.

Figure 13.1-1 shows the connection diagram of the RAMB.

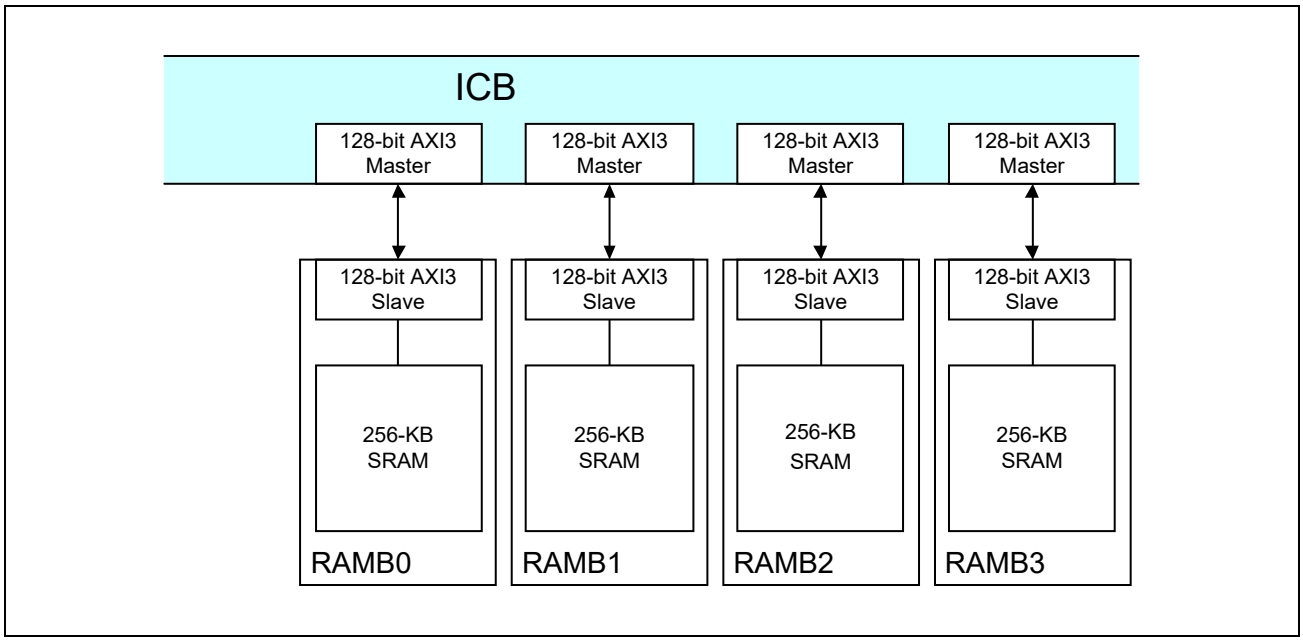


Figure 13.1-1 Schematic of RAMB Connection

13.2 Address Space

For the RAMB address allocation details, see “Address Map Details” in the Address Map section.

Section 14 ROM

This section describes the functions of the ROM.

14.1 Functional Overview

This ROM is a boot ROM, which stores the boot F/W for CA53 (LSI_InSW).

The ROM has a capacity of 128 KB.

Figure 14.1-1 shows the connection diagram of the ROM.

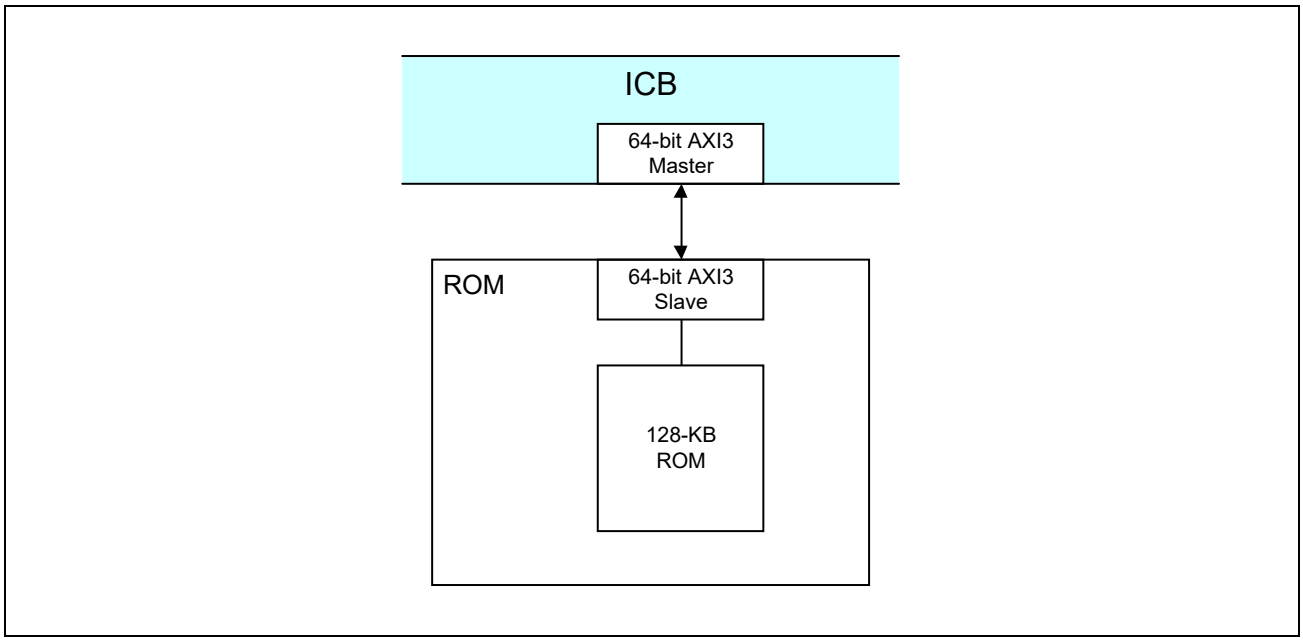


Figure 14.1-1 Schematic of ROM Connection

14.2 Address Space

For the ROM address allocation details, see “Address Map Details” in the Address Map section.

Section 15 Watchdog Timer (WDT)

This section describes the functions of the watchdog timer (WDT).

15.1 Functional Overview

The WDT has two channels, ch. 0 and ch. 1, which are respectively for CA53 core 0 and core 1.

Of those, ch. 1 is for use with the ISP support package, so do not use registers related to this channel.

15.1.1 Features

- Consists of a 32-bit counter driven by WDT_CLK (48 MHz)
- The period counter can be set to values from 21.8453 msec to 89.4785 sec in 21.8453 msec units.
- Generates an interrupt request signal every cycle set in the WDT counter.
- If the software does not clear the interrupt factor by the time the next counter overflows after the interrupt request signal is generated, a reset request signal, WDTRSTB, is asserted.
- The settings of each register and WDT elapsed time (in cycles of WDT_CLK) can be read.
- The counter operation and bus interface are asynchronous so operation does not depend on the lengths of the periods of the two clocks.
- Counting by the watchdog timer can be suspended by the CST and SYS (for debugging).

  For details, see the section of SYS.

15.2 Pin Functions

15.2.1 List of Internal Pins

Table 15.2-1 lists the internal pins.

Table 15.2-1 List of Internal Pins

Classification	Pin Name	I/O	Function
WDT pin	WDT_CLK	Input	WDT operating clock
	WDTRSTB	Output	WDT reset output (level output)
	WDTINT	Output	WDT interrupt request output (level output)
Count control pin	CNTSTOP	Input	When an ICE is in use in debugging the device, this terminal is used to stop the WDT in response to a break.

15.2.2 Pin Reset Timing

15.2.2.1 Reset Control

PRESETn supports asynchronous inputs and internally uses a reset desynchronization circuit for each clock domain.

Do not access this circuit over the time 2 × PCLK + 2 × WDT_CLK after deassertion of PRESETn, as the reset desynchronization circuit will retain the reset for this time.

The PRDATA[31:0] pins are reset to the low level in synchronization with the PCLK clock. When a low level signal is input as the PRESETn signal as shown in **Figure 15.2-1**, low level signals (initial value) are output in synchronization with the rising edge of PCLK after the clock cycle in which the low-level PRESETn signal was input. PCLK is required to reset these pins.

The WDTINT pin is reset to the low level in synchronization with the WDT_CL clock. WDT_CLK is required to reset this pin.

The WDTRSTB pin is asynchronously reset to the high level.

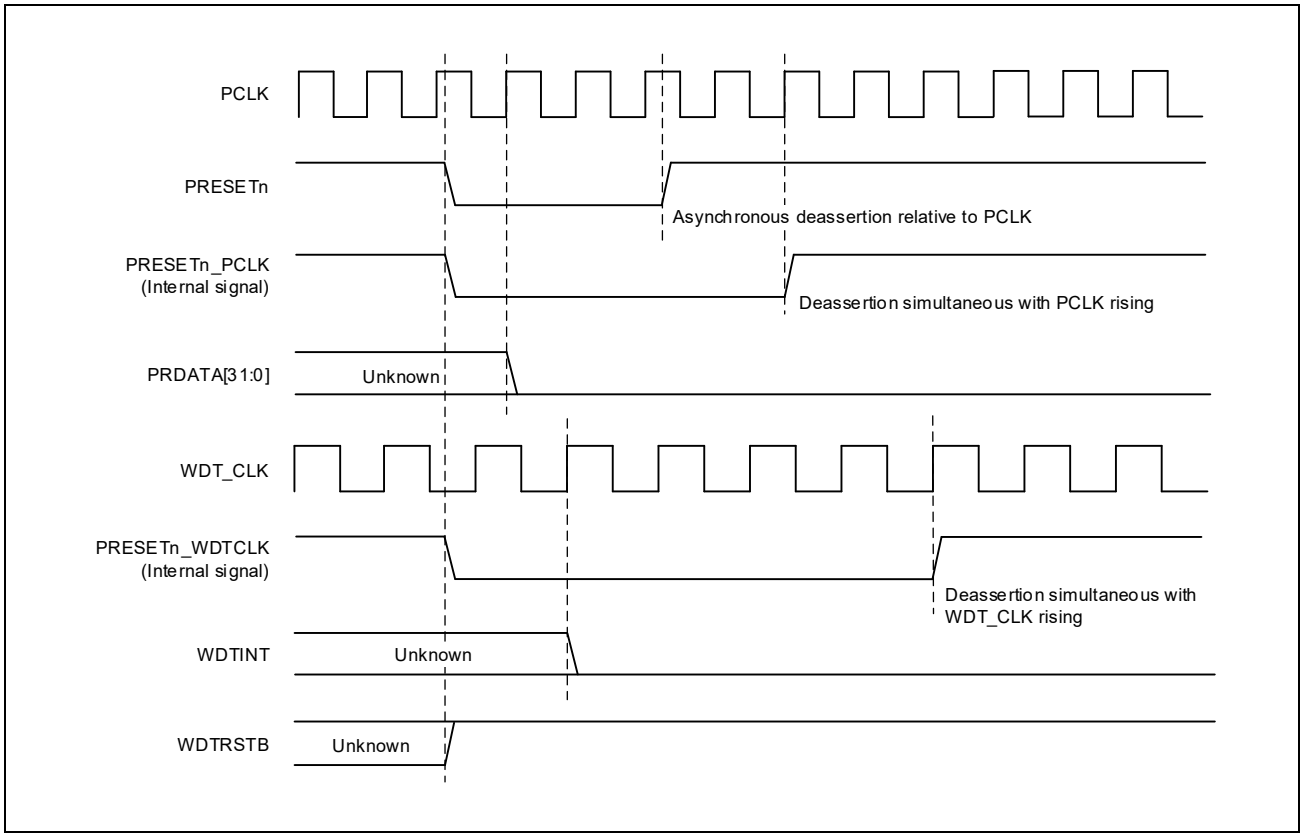


Figure 15.2-1 Reset Timing

15.2.3 Block Diagram

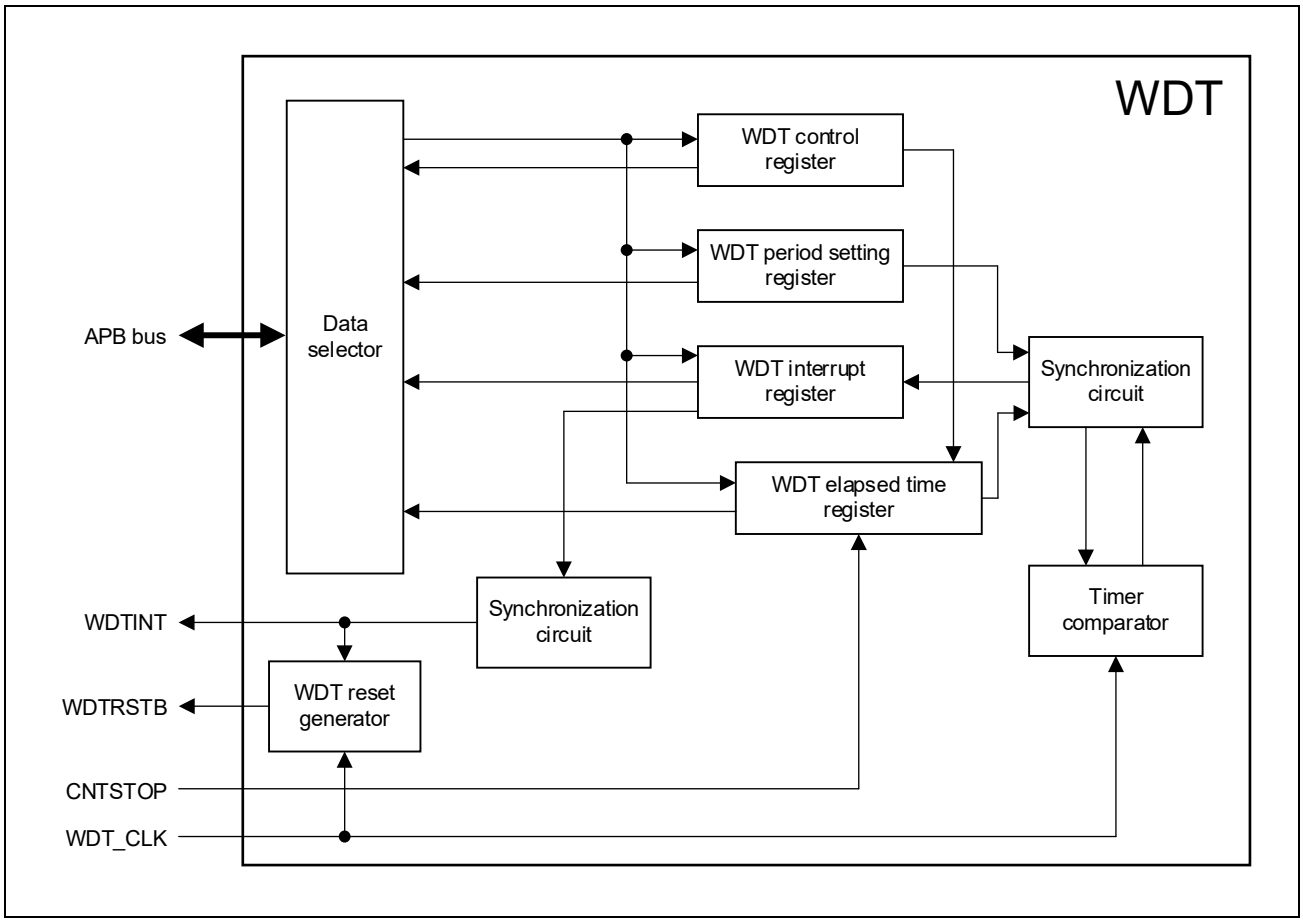


Figure 15.2-2 Block Diagram

15.2.4 Connection Configuration

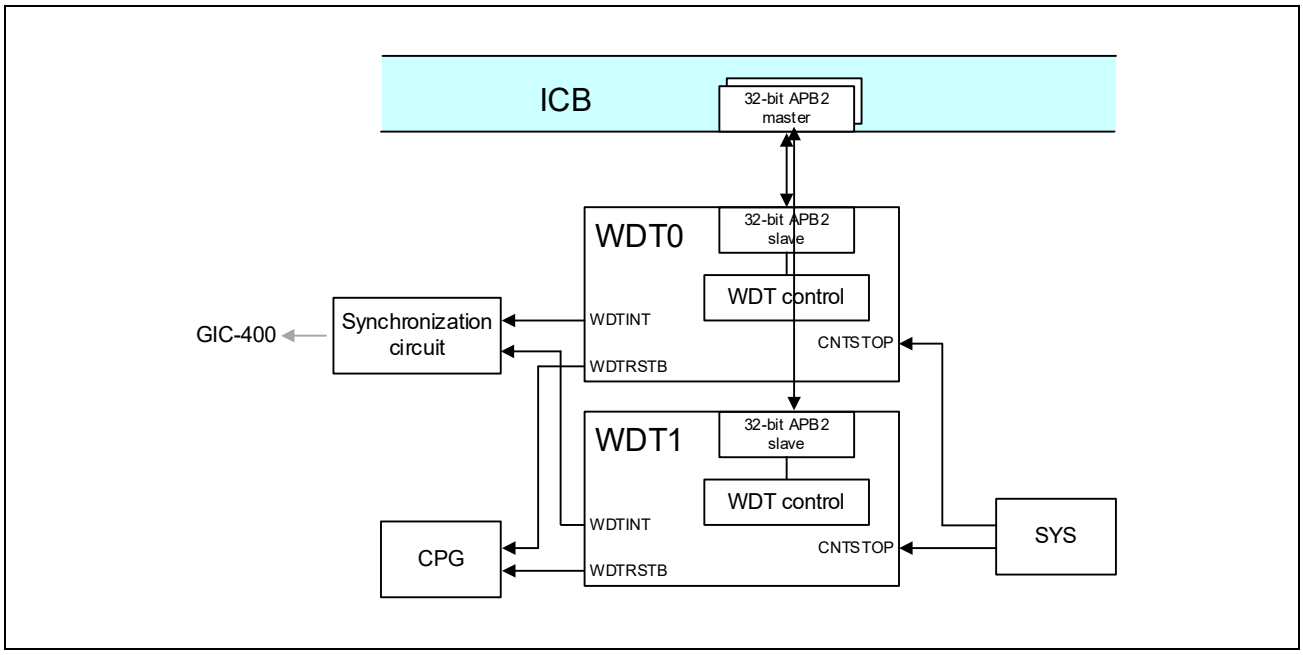


Figure 15.2-3 Schematic of WDT Connection

15.3 Register Description

For the base addresses of the registers (<WDT0_base> and <WDT1_base>), see the section of Address Map.

15.3.1 List of Registers

The following is a list of the WDT registers. They can be read and written in 32-bit units.

Table 15.3-1 List of Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
000h	WDT Control Register 0	WDT0_WDTCNT	0000_0000h	32
004h	WDT Period Setting Register 0	WDT0_WDTSET	FFF0_0000h	32
008h	WDT Elapsed Time Register 0	WDT0_WDTTIM	0000_0000h	32
00Ch	WDT Interrupt Control Register 0	WDT0_WDTINT	0000_0000h	32
080h	WDT Control Register 1	WDT1_WDTCNT	0000_0000h	32
084h	WDT Period Setting Register 1	WDT1_WDTSET	FFF0_0000h	32
088h	WDT Elapsed Time Register 1	WDT1_WDTTIM	0000_0000h	32
08Ch	WDT Interrupt Control Register 1	WDT1_WDTINT	0000_0000h	32

15.3.2 Register Descriptions

The function description of each register is given below.

The prefix (WDTm_) of the register names is omitted in the register descriptions and the field descriptions in this section.

15.3.2.1 WDT Control Register (WDTm_WDTCNT) (m = 0, 1)

This register is used to permit operation of the WDT function. Once software starts WDT, WDT does not stop*1 until it is reset by the PRESETn signal. Also, the WDT setting registers*2 cannot be changed. Setting the WDT setting register should be completed before permitting WDT operation*3.

Note 1. The CNTSTOP signal may stop the internal counter temporarily.

Note 2. The WDT period setting register (WDTSET) and the WDT elapsed time register (WDTTIM).

Note 3. When the setting register is changed, wait until the setting register write data value is reflected before permitting WDT operation. The reflection time of the setting register is 6 × PCLK + 9 × WDT_CLK or more. If this reflection time is not kept, the value of the setting register is not reflected, and is ignored.

Access Size: 32 bits

Address(es): <WDT0_S0_base> + 0000h
<WDT1_S0_base> + 0080h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WDTEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 15.3-2 WDTm_WDTCNT Register Contents

Bit Position	Bit Name	Description
31 to 1	—	Reserved. The write value should alwalys be 0b.
0	WDTEN	WDT enable bit 0b: Invalid (nothing changes) 1b: WDT operation is permitted.

15.3.2.2 WDT Period Setting Register (WDTm_WDTSET) (m = 0, 1)

This register sets the period of a 32-bit counter that composes WDT. Writing is not possible during WDT operation. If written continuously, the data written later is valid. Use the following formula to calculate the WDT period.

WDT period = WDT_CLK period × 1024 ×1024 × (the setting value of WDTTIME + 1)

Therefore,

the setting value of WDTTIME = WDT period / (WDT_CLK period ×1024 ×1024) – 1

Access Size: 32 bits

Address(es): <WDT0_S0_base> + 0004h
<WDT1_S0_base> + 0084h

Initial Value: FFF0_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WDTTIME[11:0]												—	—	—	—
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 15.3-3 WDTm_WDTSET Register Contents

Bit Position	Bit Name	Description
31 to 20	WDTTIME[11:0]	WDT period setting value Writing is not possible during WDT operation.
19 to 0	—	Reserved. The write value should always be 0b.

Note: When an interrupt occurs the value that WDT compares is WDTSET[31:0] + 000F_FFFFh. Therefore, if the setting value of this register is 0010_0000h, the interrupt occurrence count is 001F_FFFFh (not 0010_0000h).

15.3.2.3 WDT Elapsed Time Register (WDTm_WDTTIM) (m = 0, 1)

This register indicates the 32-bit count value that composes WDT. If reading is performed during WDT operation, the elapsed time from clear to read may be read.

By writing to this register when the WDT is stopped, the value at the start of counting may be set to the 32-bit counter configuring the WDT. Writing is used for logic testing of the circuit. If WDT operation is started by writing a value greater than the counter period that is set in WDT period setting register (cleared value), after the 32-bit counter overflows and the value returns to 0b, WDT operates at the set correct period. Writing is not possible during WDT operation. If written continuously, the data written later is valid.

Access Size: 32 bits

Address(es): <WDT0_S0_base> + 0008h
<WDT1_S0_base> + 0088h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CRTTIME[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CRTTIME[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 15.3-4 WDTm_WDTTIM Register Contents

Bit Position	Bit Name	Description
31 to 0	CRTTIME[31:0]	WDT count value Writing is not possible during WDT operation.

Note: When setting a value in the WDTTIM register, do not set a value that is WDTSET[31:0] register + F_FFFFh.

15.3.2.4 WDT Interrupt Control Register (WDTm_WDTINT) (m = 0, 1)

This register reads the WDT interrupt status, clears interrupt, and clears the counter that composes WDT. Set the INTDISP bit of this register to 1b within the time set by WDTSET. If not set, the WDTIT pin is asserted. After that, if the INTDISP bit is not further set to 1b within the time set by WDTSET, the WDTRSTB pin is asserted.

When the WDTINT register is accessed for consecutive writing, set a write interval of 5 × PCLK + 5 × WDT_CLK or more. If the write interval is not kept, the register is not written.

Access Size: 32 bits

Address(es): <WDT0_S0_base> + 000Ch
<WDT1_S0_base> + 008Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INTDISP
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 15.3-5 WDTm_WDTINT Register Contents

Bit Position	Bit Name	Description
31 to 1	—	Reserved. The write value should always be 0b.
0	INTDISP	Read and clear interrupt status [Read] Interrupt status 0b: No interrupt 1b: With interrupt [Write] Interrupt clear 0b: Invalid (nothing changes) 1b: Interrupt clear

15.4 Operations

The first time the counter overflows, the WDT outputs an interrupt signal, and when the counter overflows for a second time without having been cleared, the WDT outputs a reset request signal.

The prefix (WDTm_) of the register names is omitted in this and subsequent sections.

15.4.1 Operation Timing

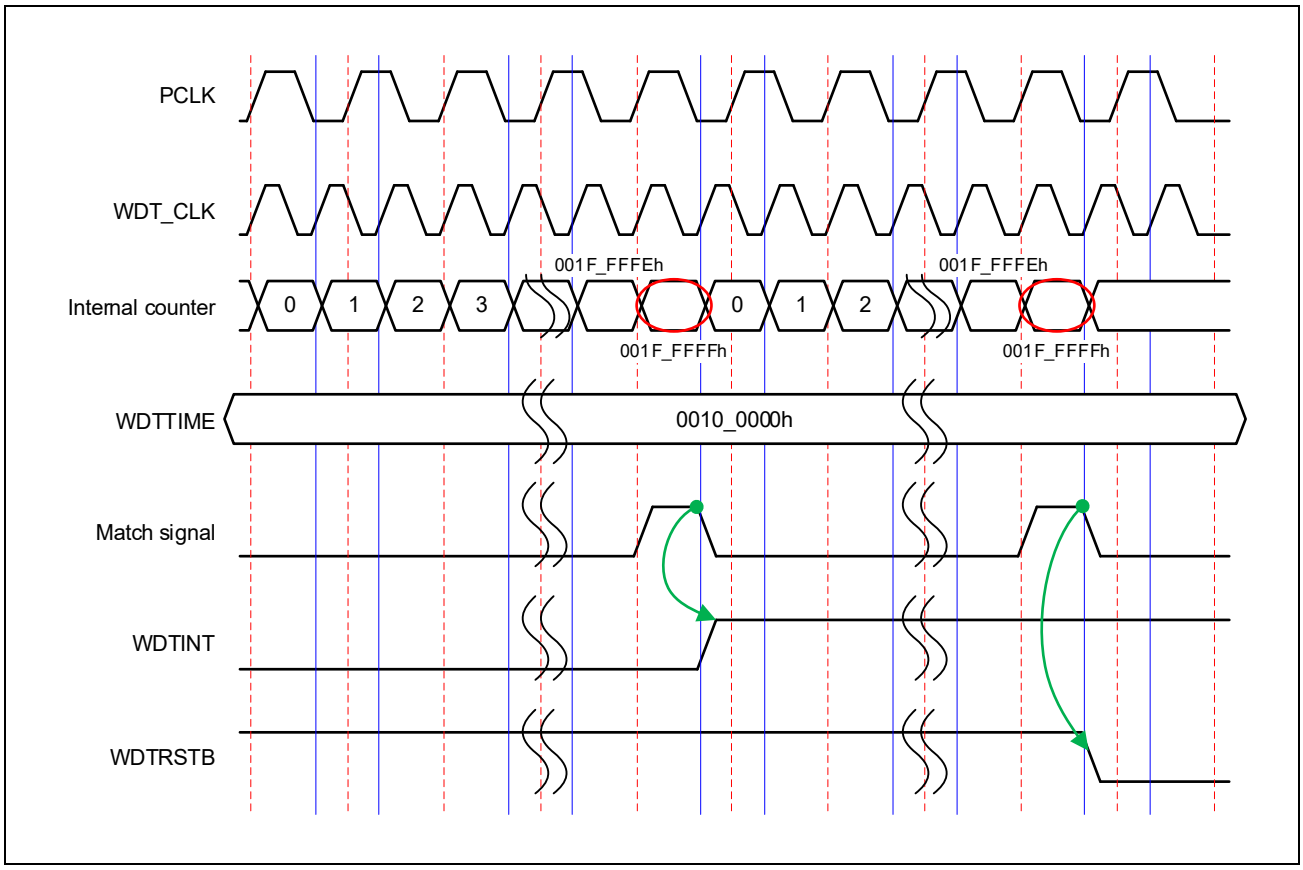


Figure 15.4-1 WDT Output Signal Operation Timing

15.4.2 Provisions for the Write Access Interval of a WDT Interrupt Control Register (WDTINT)

On completion of write access to a WDT interrupt control register, a synchronization period is required for synchronization of the written data with WDT_CLK. Consecutive writing to a WDTINT register requires a write interval*[1] of at least 5 × PCLK + 5 × WDT_CLK before a next write access.

Note 1. If condition for the write interval is not satisfied, the interrupt request may not be cleared. In this case, make sure that the interrupt factor has been cleared after write access before proceeding with a next write access.

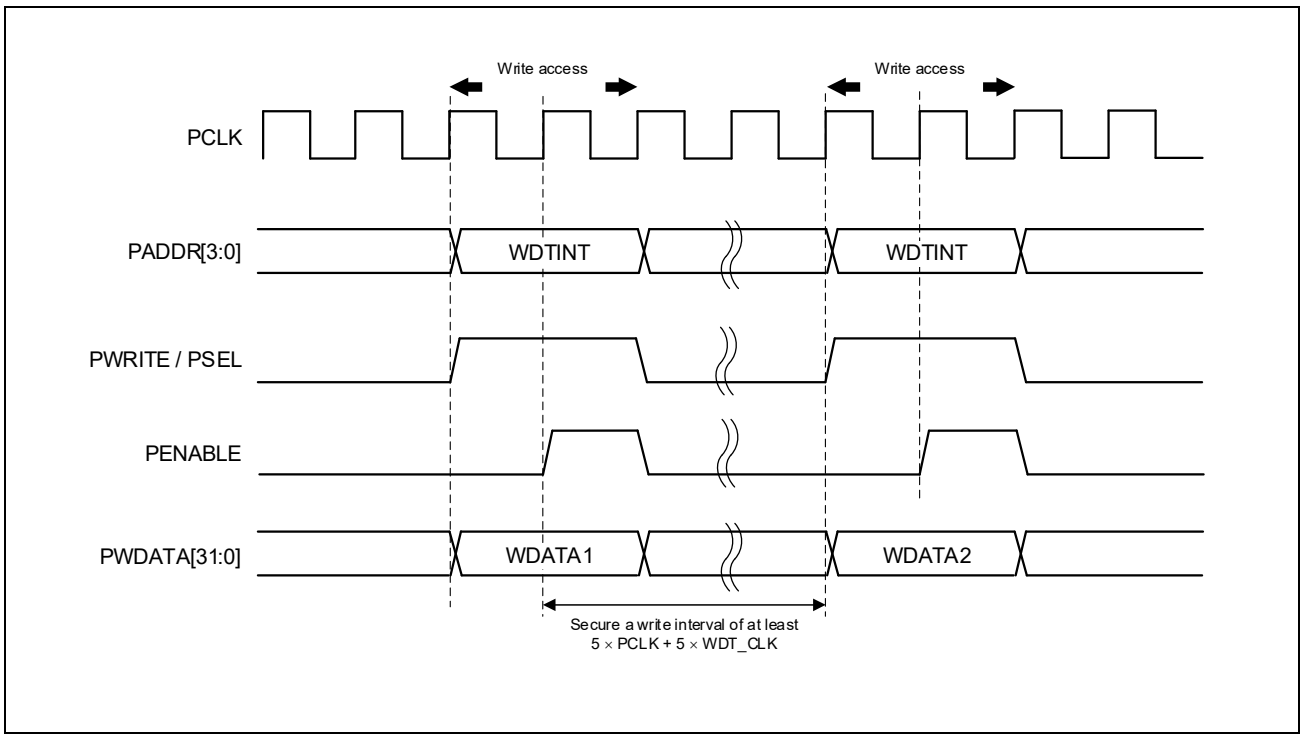


Figure 15.4-2 Provisions for the Write Access Interval of WDTINT

15.4.3 Timing of Reflection of Register Settings in WDT Operation

The registers other than the WDT interrupt control register (WDTINT) are always synchronized with WDT_CLK running at a fixed period.

Depending on the specifications of the synchronization circuit, the time taken until written data are reflected in the WDT operation is in the range from 2 × PCLK + 4 × WDT_CLK (minimum) to 6 × PCLK + 9 × WDT_CLK (maximum). **Figure 15.4-3** shows the minimum synchronization interval for written data. **Figure 15.4-4** shows the maximum synchronization interval for written data.

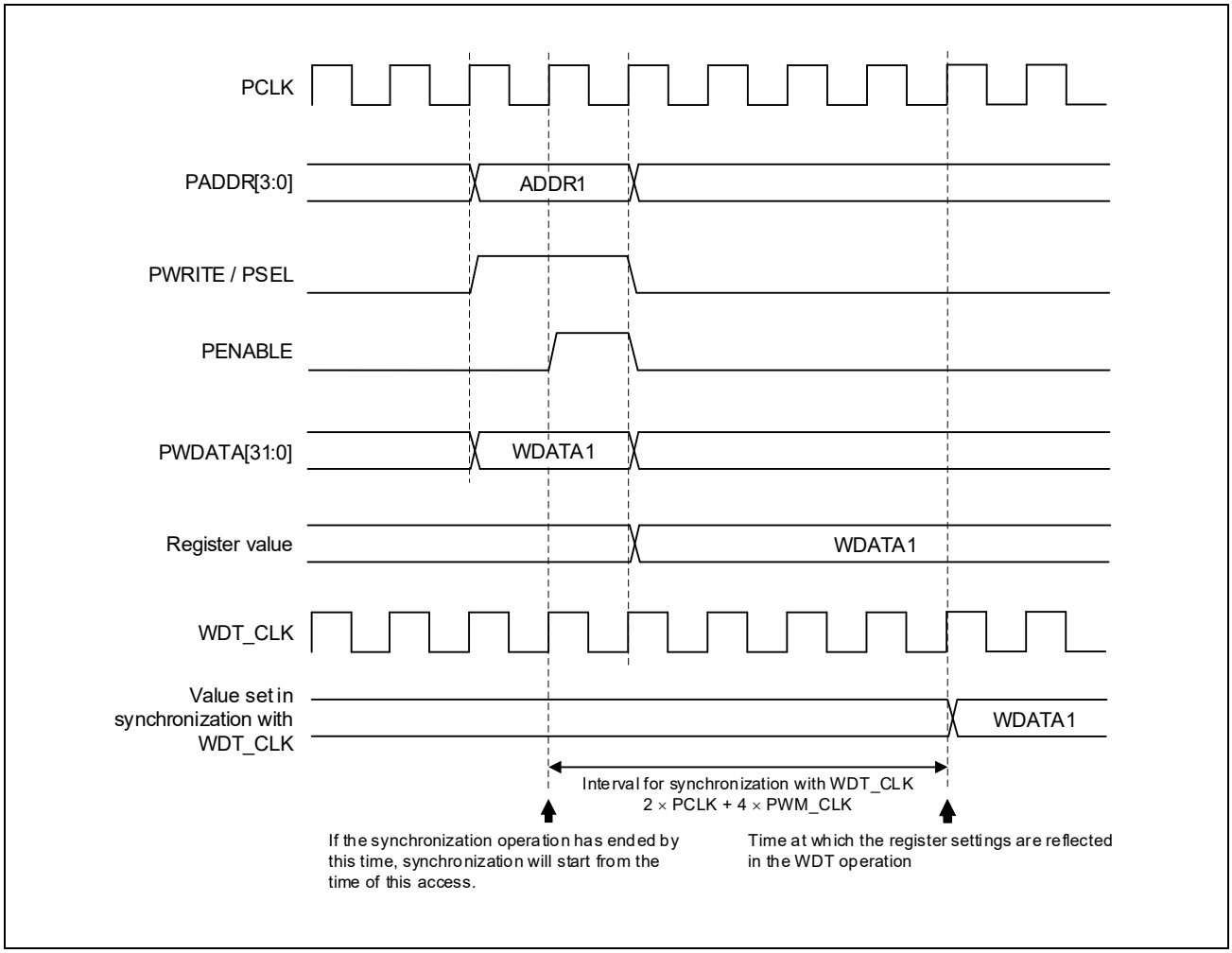


Figure 15.4-3 Timing 1 of Reflection of Register Settings in WDT Operation

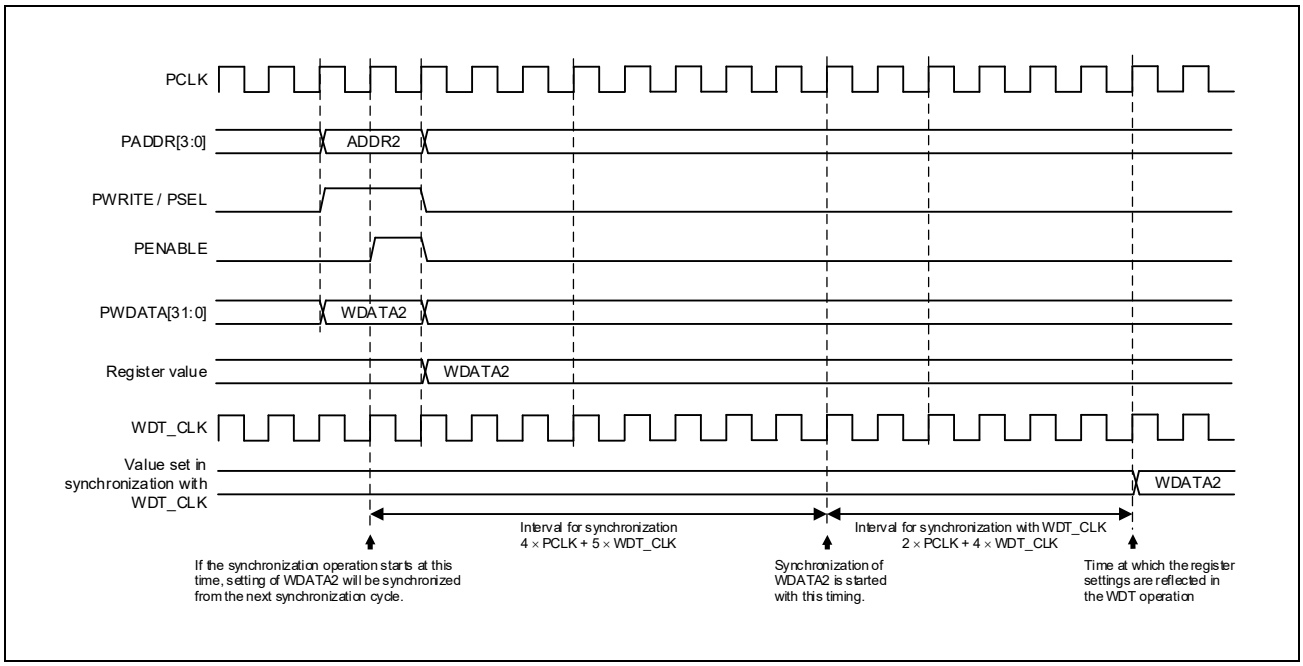


Figure 15.4-4 Timing 2 of Reflection of Register Settings in WDT Operation

15.4.4 Timing of Reflection of the WDT Counter Value in the WDTTIM Register

The storage of values in the WDTTIM register is of counter values in synchronization with PCLK. Therefore, the interval after which a value is updated in the WDTTIM register is up to 5 × WDT_CLK + 5 × PCLK, which means that the value prior to the actual counter value may be read during this interval.

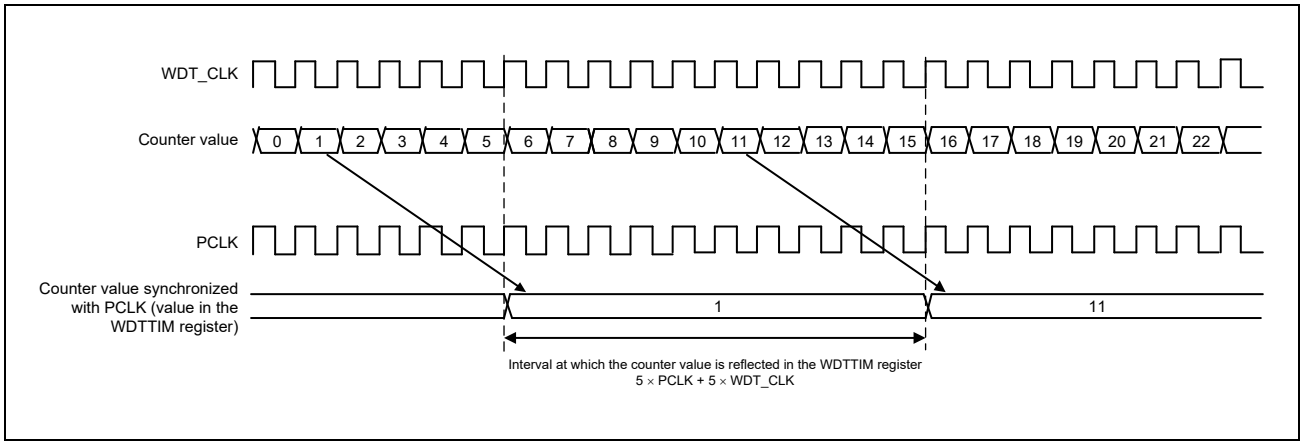


Figure 15.4-5 Timing of Reflection of the Counter Value in the WDTTIM Register

15.5 Usage Notes

- When setting values in the WDTTIM register, do not set the value of the WDTSET[31:0] register + F_FFFFh.
- The reset request signal, WDTRSTB, and the WDT interrupt signal, WDTINT, cannot be masked.

Section 16 Compare-Match Timer (TIM)

This section describes the functions of the compare match timer (TIM).

16.1 Functional Overview

The TIM has an internal 32-bit counter that can be used as an interval timer.

This LSI has a total of 32 channels of TIM from ch. 0 to ch. 31.

Among these channels, ch. 0 to ch. 7 and ch. 24 to ch. 31 are used by the ISP support package. Therefore, do not use the registers related to the target channels.

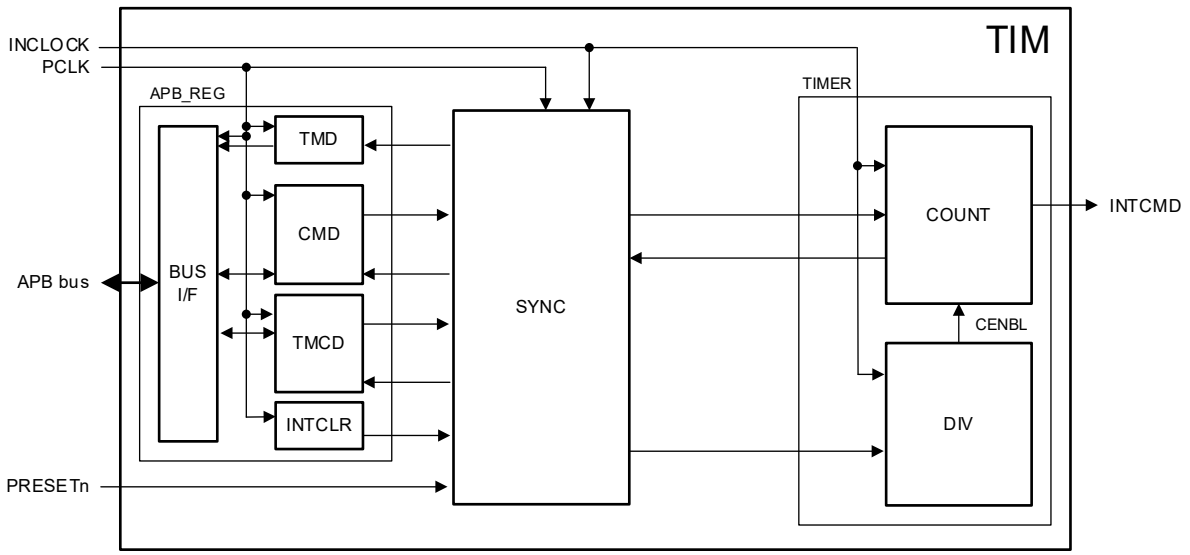
16.1.1 Features

- Configured with a 32-bit counter operating at INCLOCK (2 MHz)
- The clock input from the count clock input pin can be divided by 2, 4, 8, 16, 32, 64, 128, or 256, and one of these divided clocks can be used as the count clock.
- The counter period can be set in the range of 1 to 4294967296 (32-bit timer) using the selected divider clock as the count clock.
- Generates an interrupt request signal every cycle set in the TIM counter.
- The counter operation and the bus interface are asynchronous and can operate independently regardless of the size of the respective clock cycles.

CAUTION

The interrupt request signal should be used in level output mode (the INTMODE field in the TIMm_TMCD register should be set to 1b).

16.1.2 Block Diagram



Note:

- APB_REG block:
  An internal register to be allocated on the APB bus
- SYNC block:
  Synchronizes the PCLK-synchronized signal to INCLOCK or the INCLOCK-synchronized signal to PCLK.
  The INCLOCK synchronization of PRESETn is also performed internally by SYNC.
- TIMER block:
  Includes a divide-by-clock generation block (DIV) and a counter block (COUNT).
- DIV block:
  Generates the enable signal for count-up with the selected signal synchronized with CS[2:0] by INCLOCK.
  Clears the frequency divider with CE = 0b. Stops counting operation when CAE = 0b.
- COUNT block:
  Counts up on the rising edge of INCLOCK.
  When the counter value (TMD) matches the compare value (CMD), INTCMD is output.
  Clears the counter with CE = 0b.

Figure 16.1-1 Block Diagram

16.2 Pin Functions

16.2.1 List of Internal Pins

Table 16.2-1 lists the internal pins of the TIM.

Table 16.2-1 List of Internal Pins

Classification	Pin Name	I/O	Function
Count Clock	INCLOCK	Input	Counting clock
Interrupt	INTCMD	Output	Match interrupt request signal

16.3 Register Description

For the base addresses of the registers (<TIM0_S0_base> to <TIM31_S0_base>), see the section of Address Map.

16.3.1 List of Registers

The following is a list of the timer registers.

Table 16.3-1 List of Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
000h	Timer Counter Register	TIMm_TMD	0000_0000h	32
004h	Timer Compare Register	TIMm_CMD	0000_0000h	32
008h	Timer Control Register	TIMm_TMCD	0000_0000h	32
00Ch	Timer Interrupt Clear Register	TIMm_INTCLR	0000_0000h	32

Note: m = 0 to 31

16.3.2 Register Descriptions

The function description of each register is described below.

16.3.2.1 Timer Counter Register (TIMm_TMD) (m = 0 to 31)

This register is a 32-bit up counter, and starting and stopping are controlled by the CE bit of the control register (TIMm_TMCD).

For the count clock, the INCLOCK input is divided by the built-in frequency divider. INCLOCK /2, INCLOCK /4, INCLOCK /8, INCLOCK /16, INCLOCK /32, INCLOCK /64, INCLOCK /128, INCLOCK /256 can be selected from CS0-CS2 of TIMm_TMCD. This register can only be read.

Note: The TMD value is read out synchronized with PCLK. Therefore, a value before the actual count value may be read.

Access Size:	32 bits	
Address(es):	<TIM0_S0_base> + 0000h	<TIM16_S0_base> + 0000h
	<TIM1_S0_base> + 0000h	<TIM17_S0_base> + 0000h
	<TIM2_S0_base> + 0000h	<TIM18_S0_base> + 0000h
	<TIM3_S0_base> + 0000h	<TIM19_S0_base> + 0000h
	<TIM4_S0_base> + 0000h	<TIM20_S0_base> + 0000h
	<TIM5_S0_base> + 0000h	<TIM21_S0_base> + 0000h
	<TIM6_S0_base> + 0000h	<TIM22_S0_base> + 0000h
	<TIM7_S0_base> + 0000h	<TIM23_S0_base> + 0000h
	<TIM8_S0_base> + 0000h	<TIM24_S0_base> + 0000h
	<TIM9_S0_base> + 0000h	<TIM25_S0_base> + 0000h
	<TIM10_S0_base> + 0000h	<TIM26_S0_base> + 0000h
	<TIM11_S0_base> + 0000h	<TIM27_S0_base> + 0000h
	<TIM12_S0_base> + 0000h	<TIM28_S0_base> + 0000h
	<TIM13_S0_base> + 0000h	<TIM29_S0_base> + 0000h
	<TIM14_S0_base> + 0000h	<TIM30_S0_base> + 0000h
	<TIM15_S0_base> + 0000h	<TIM31_S0_base> + 0000h
Initial Value:	0000_0000h	

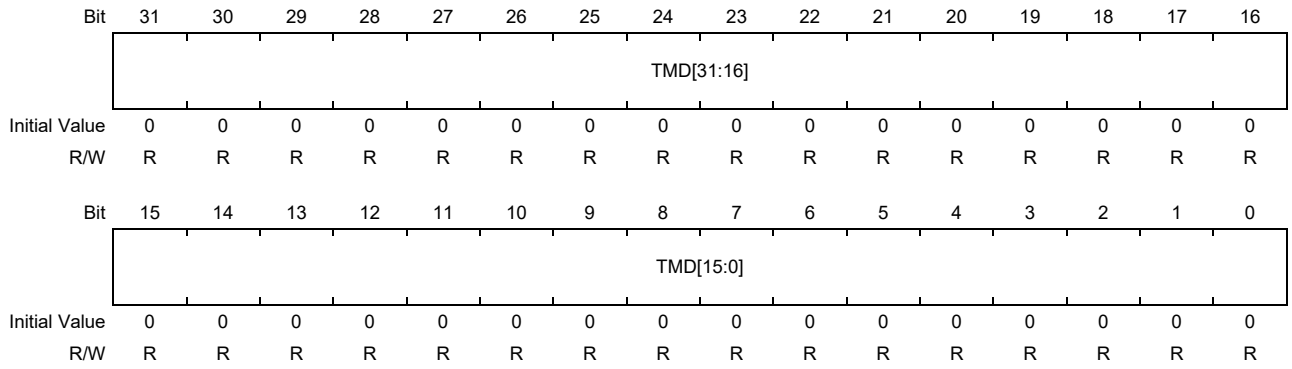


Table 16.3-2 TIMm_TMD Register Contents

Bit Position	Bit Name	Description
31 to 0	TMD[31:0]	Count value TMD = 0000_0000h under any of the following conditions. – Timing when a low is input to the PRESETn pin – Timing when the CE bit of TIMm_TMCD register is set to 0b – Timing when TMD and CMD values match

CAUTIONS

1. Do not change the divided clock setting while the timer is operating.
2. When changing the divided clock setting, set CE = 0b before executing.
3. The CE bit is synchronized with INCLOCK after being written from the APB bus, there is a time lag between the time CE = 1b is written and TMD is activated.
4. This is a read-only register, writing is prohibited.

16.3.2.2 Timer Compare Register (TIMm_CMD) (m = 0 to 31)

This register compares the count value of the TIMm_TMD register and generates an interrupt request signal (INTCMD) if they match. TIMm_TMD is cleared in synchronization with this match. The set value of this register is used as the counter comparison value after synchronizing with INCLOCK.

The INTCMD occurrence cycle can be calculated using the following formula.

$$\text{INTCMD generation cycle (sec)} = \frac{1}{\text{INCLOCK frequency (Hz)}} \times 2^{(N+1)} \times (\text{CMD} + 1)$$

N: CS[2:0] set value for TIMm_TMCD register
CMD: Set the value for TIMm_CMD register*1

Note 1. (CMD + 1) when CMD is set to 0b is as follows and 4294967296 + 1 for the 32-bit timer.

Access Size: 32 bits

Address(es):

<TIM0_S0_base> + 0004h	<TIM16_S0_base> + 0004h
<TIM1_S0_base> + 0004h	<TIM17_S0_base> + 0004h
<TIM2_S0_base> + 0004h	<TIM18_S0_base> + 0004h
<TIM3_S0_base> + 0004h	<TIM19_S0_base> + 0004h
<TIM4_S0_base> + 0004h	<TIM20_S0_base> + 0004h
<TIM5_S0_base> + 0004h	<TIM21_S0_base> + 0004h
<TIM6_S0_base> + 0004h	<TIM22_S0_base> + 0004h
<TIM7_S0_base> + 0004h	<TIM23_S0_base> + 0004h
<TIM8_S0_base> + 0004h	<TIM24_S0_base> + 0004h
<TIM9_S0_base> + 0004h	<TIM25_S0_base> + 0004h
<TIM10_S0_base> + 0004h	<TIM26_S0_base> + 0004h
<TIM11_S0_base> + 0004h	<TIM27_S0_base> + 0004h
<TIM12_S0_base> + 0004h	<TIM28_S0_base> + 0004h
<TIM13_S0_base> + 0004h	<TIM29_S0_base> + 0004h
<TIM14_S0_base> + 0004h	<TIM30_S0_base> + 0004h
<TIM15_S0_base> + 0004h	<TIM31_S0_base> + 0004h

Initial Value: 0000_0000h

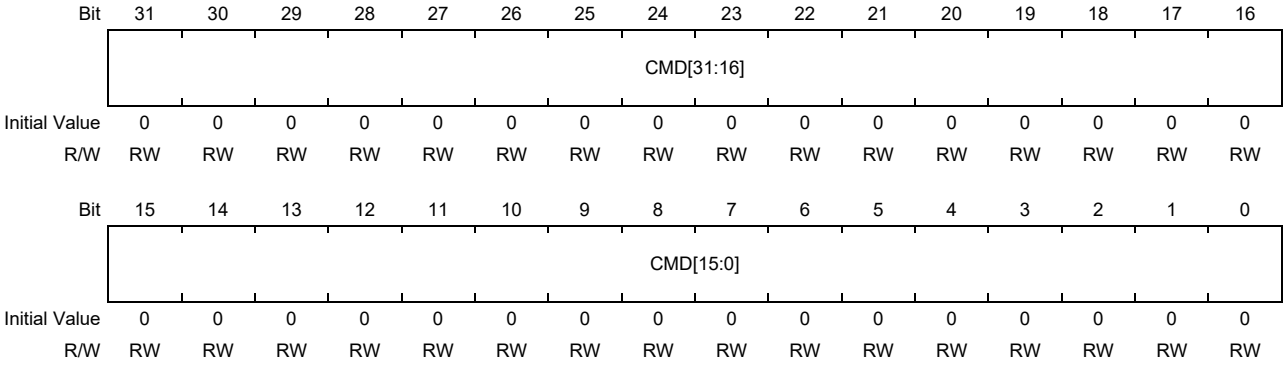


Table 16.3-3 TIMm_CMD Register Contents

Bit Position	Bit Name	Description
31 to 0	CMD[31:0]	Count comparison value

Note:

- The written value will be reflected after INCLOCK synchronization. There will be a time lag (refer to **Table 16.3 3a** below) for the maximum (latest) timing from when the write to the register is completed until the write value is reflected in the timer operation.

Table 16.3-3a Operation Reflection Timing of Register Setting Value

Register Name	Software Operation	Timer Stopped	Timer Running
TIMm_CMD	Compare value setting	1 × PCLK + 3 × INCLOCK	Counter clear timing after compare matches after 1 × PCLK + 3 × INCLOCK
TIMm_TMCD	Count start	Same as above	Same as above
	Count pause	Same as above	Same as above
	Resume from counting pause	Same as above	Same as above
	Count stop	Same as above	Same as above
TIMm_INTCLR	Clear interrupt	Same as above	Same as above

- The read value will be the value after INCLOCK synchronization. Since synchronization takes time, there will be a time lag before the set value can be read. Refer to **Table 16.3 3b** below for the maximum (latest) timing from when the write to the register is complete until the written value can be read.

Table 16.3-3b Register Read Enable Timing

Register Name	Software Operation	Timer Stopped	Timer Running
TIM_CMD	Compare value setting	5 × PCLK + 5 × INCLOCK	5 × PCLK + 5 × INCLOCK
TIM_TMCD	Count start	Same as above	Same as above
	Count pause	Same as above	Same as above
	Resume from counting pause	Same as above	Same as above
	Count stop	Same as above	Same as above

- If the CMD value is rewritten during the timer operation, the new CMD value is reflected when the counter (TMD) matches the previous CMD setting value.
- When writing to CMD, follow the rules for the writing interval. Write will be igonored if not followed.
- The relationship between the CMD setting value and the count number is shown in **Table 16.3 3c** below (as the 32-bit configuration).

Table 16.3-3c Relationship between CMD Setting Value and Count Number (32-bit Configuration)

CMD Setting Value (32-bit Timer)	Count Value	Description
0h	1_0000_0000h times	Maximum setting 0->1->2…FFFF_FFFFh->1_0000_0000h->0->1…
1h	0000_0001h times	Minimum setting 0->1->0->1…
2h	0000_0002h times	0->1->2->0->1->2…
:	:	—
FFFF_FFFEh	FFFF_FFFEh times	0->1->2…FFFF_FFFEh->0->1…
FFFF_FFFFh	FFFF_FFFFh times	0->1->2…FFFF_FFFEh->FFFF_FFFFh->0->1…

16.3.2.3 Timer Control Register (TIMm_TMCD) (m = 0 to 31)

This register sets the timer operation.

Note: Follow the rules regarding the write interval when writing to TIMm_TMCD. Write will be igonored if not followed.

Access Size: 32 bits

Address(es):

<TIM0_S0_base> + 0008h	<TIM16_S0_base> + 0008h
<TIM1_S0_base> + 0008h	<TIM17_S0_base> + 0008h
<TIM2_S0_base> + 0008h	<TIM18_S0_base> + 0008h
<TIM3_S0_base> + 0008h	<TIM19_S0_base> + 0008h
<TIM4_S0_base> + 0008h	<TIM20_S0_base> + 0008h
<TIM5_S0_base> + 0008h	<TIM21_S0_base> + 0008h
<TIM6_S0_base> + 0008h	<TIM22_S0_base> + 0008h
<TIM7_S0_base> + 0008h	<TIM23_S0_base> + 0008h
<TIM8_S0_base> + 0008h	<TIM24_S0_base> + 0008h
<TIM9_S0_base> + 0008h	<TIM25_S0_base> + 0008h
<TIM10_S0_base> + 0008h	<TIM26_S0_base> + 0008h
<TIM11_S0_base> + 0008h	<TIM27_S0_base> + 0008h
<TIM12_S0_base> + 0008h	<TIM28_S0_base> + 0008h
<TIM13_S0_base> + 0008h	<TIM29_S0_base> + 0008h
<TIM14_S0_base> + 0008h	<TIM30_S0_base> + 0008h
<TIM15_S0_base> + 0008h	<TIM31_S0_base> + 0008h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TEST	CS[2:0]			—	INTMODE	CE	CAE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	R0W	RW	RW	RW

Table 16.3-4 TIMm_TMCD Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 8	—	Reserved. The write value should always be 0b.
7	TEST	Reserved. The write value should always be 0b.
6 to 4	CS[2:0]	Select the divided clock of INCLOCK to determine the timer count clock.*1,*2
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2	INTMODE	Select whether to set the interrupt request signal to pulse mode or level mode. 0b: Selects the interrupt request signal in pulse mode. (Setting prohibited) 1b: Selects the interrupt request signal in level mode.
1	CE	The counter enable (CE) bit controls the operation of the divider and timer counter. When CE = 0b is set, the divider and timer counters are initialized. 0b: The frequency divider and counter are initialized to 0b and stopped. 1b: The divider and counter operate.

Table 16.3-4 TIMm_TMCD Register Contents (2/2)

Bit Position	Bit Name	Description
0	CAE	The clock action enable (CAE) bit controls the operation of the count clock (INCLOCK) divider. The purpose of this function is to pause the counter during a break when debugging with ICE. Set to 1b for normal use. 0b: Pauses the count clock (INCLOCK) divider. 1b: Return from the pause of the divider.

Note 1. Do not change CS[2:0] while the timer is operating. To change it, set CE to 0b before executing. If CS[2:0] is rewritten during operation, the operation cannot be guaranteed.

Note 2. The timer/counter count cycle selection is shown below.

Table 16.3-5 Selection of Timer/Counter Count Cycle

CS2	CS1	CS0	Count Enable Select
0b	0b	0b	Select INCLOCK divide-by-2 signal as count clock
0b	0b	1b	Select INCLOCK divide-by-4 signal as count clock
0b	1b	0b	Select INCLOCK divide-by-8 signal as count clock
0b	1b	1b	Select INCLOCK divide-by-16 signal as count clock
1b	0b	0b	Select INCLOCK divide-by-32 signal as count clock
1b	0b	1b	Select INCLOCK divide-by-64 signal as count clock
1b	1b	0b	Select INCLOCK divide-by-128 signal as count clock
1b	1b	1b	Select INCLOCK divide-by-256 signal as count clock

16.3.2.4 Timer Interrupt Clear Register (TIMm_INTCLR) (m = 0 to 31)

This register clears the interrupt request signal (INTCMD). When reading for writing only, 0b can be read.

Note: When writing to the TIMm_INTCLR register, be sure to observe the write interval rules. Write will be igonored if not followed. Clear is prioritized if write to the TIMm_INTCLR register and timer interrupt occurs simultaneously.

Access Size: 32 bits

Address(es):

<TIM0_S0_base> + 000Ch	<TIM16_S0_base> + 000Ch
<TIM1_S0_base> + 000Ch	<TIM17_S0_base> + 000Ch
<TIM2_S0_base> + 000Ch	<TIM18_S0_base> + 000Ch
<TIM3_S0_base> + 000Ch	<TIM19_S0_base> + 000Ch
<TIM4_S0_base> + 000Ch	<TIM20_S0_base> + 000Ch
<TIM5_S0_base> + 000Ch	<TIM21_S0_base> + 000Ch
<TIM6_S0_base> + 000Ch	<TIM22_S0_base> + 000Ch
<TIM7_S0_base> + 000Ch	<TIM23_S0_base> + 000Ch
<TIM8_S0_base> + 000Ch	<TIM24_S0_base> + 000Ch
<TIM9_S0_base> + 000Ch	<TIM25_S0_base> + 000Ch
<TIM10_S0_base> + 000Ch	<TIM26_S0_base> + 000Ch
<TIM11_S0_base> + 000Ch	<TIM27_S0_base> + 000Ch
<TIM12_S0_base> + 000Ch	<TIM28_S0_base> + 000Ch
<TIM13_S0_base> + 000Ch	<TIM29_S0_base> + 000Ch
<TIM14_S0_base> + 000Ch	<TIM30_S0_base> + 000Ch
<TIM15_S0_base> + 000Ch	<TIM31_S0_base> + 000Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INTCLR
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 16.3-6 TIMm_INTCLR Register Contents

Bit Position	Bit Name	Description
31 to 1	—	Reserved. These bits are read as 0b. The write value should be always 0b.
0	INTCLR	Clears the interrupt. 0b: No action 1b: Clears interrupt request signal

16.4 Operation

The prefix (TIMm_) of the register names is omitted in this and subsequent sections.

16.4.1 Notes on Write Interval

When the software writes to the same register of the timer, some precautions should be taken regarding the write interval. Follow the precautions when using this product. If the precautions are not followed, writing to the registers will be ignored.

<Write interval>

Clock notation: 5 × PCLK + 5 × INCLOCK
Time notation: 5 × (1/PCLK frequency (Hz)) + 5 × (1/INCLOCK frequency (Hz))
Allow an interval of at least the number described above for writing.

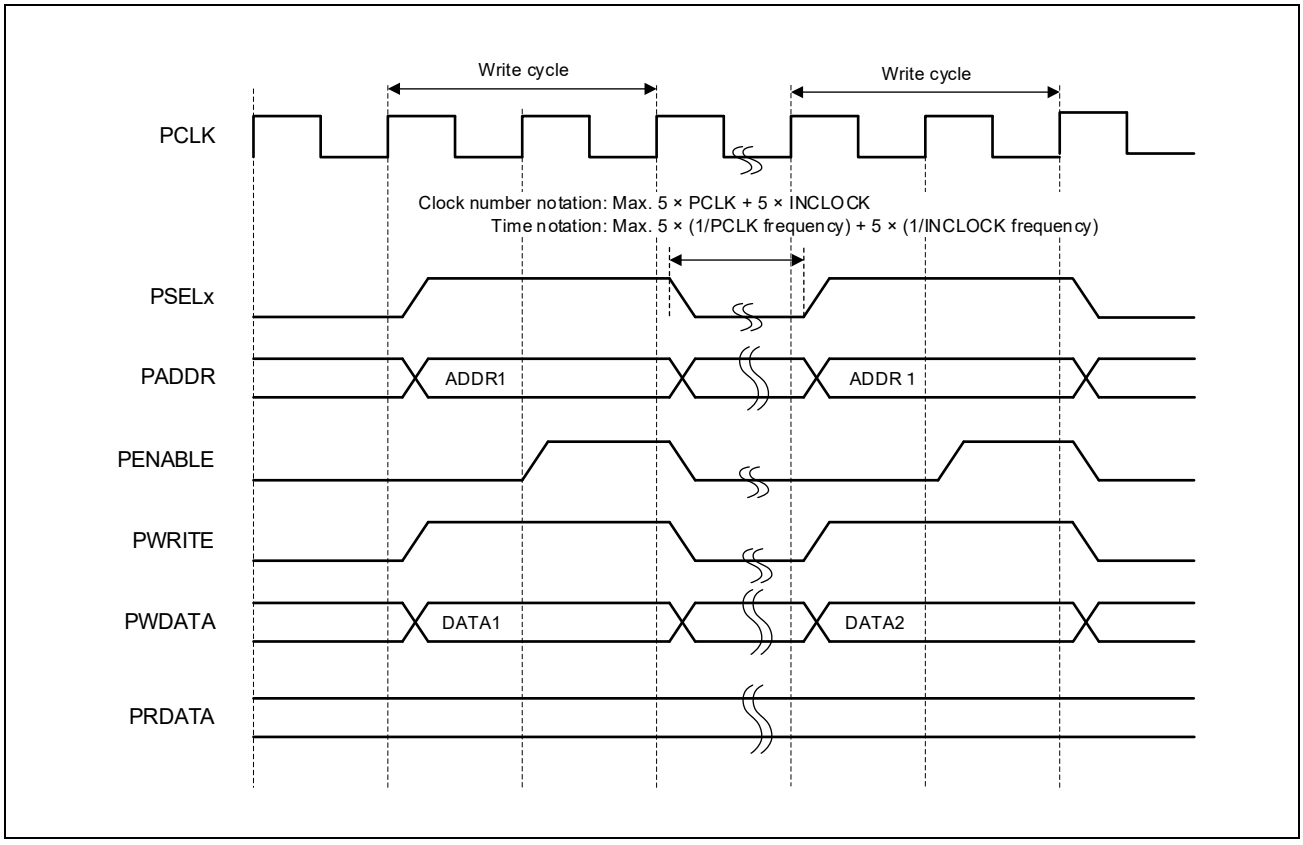


Figure 16.4-1 Notes on Write Interval

16.4.2 Clock and Reset Supply Procedure

As the reset is released synchronously with PCLK, supply it according to the following procedure.

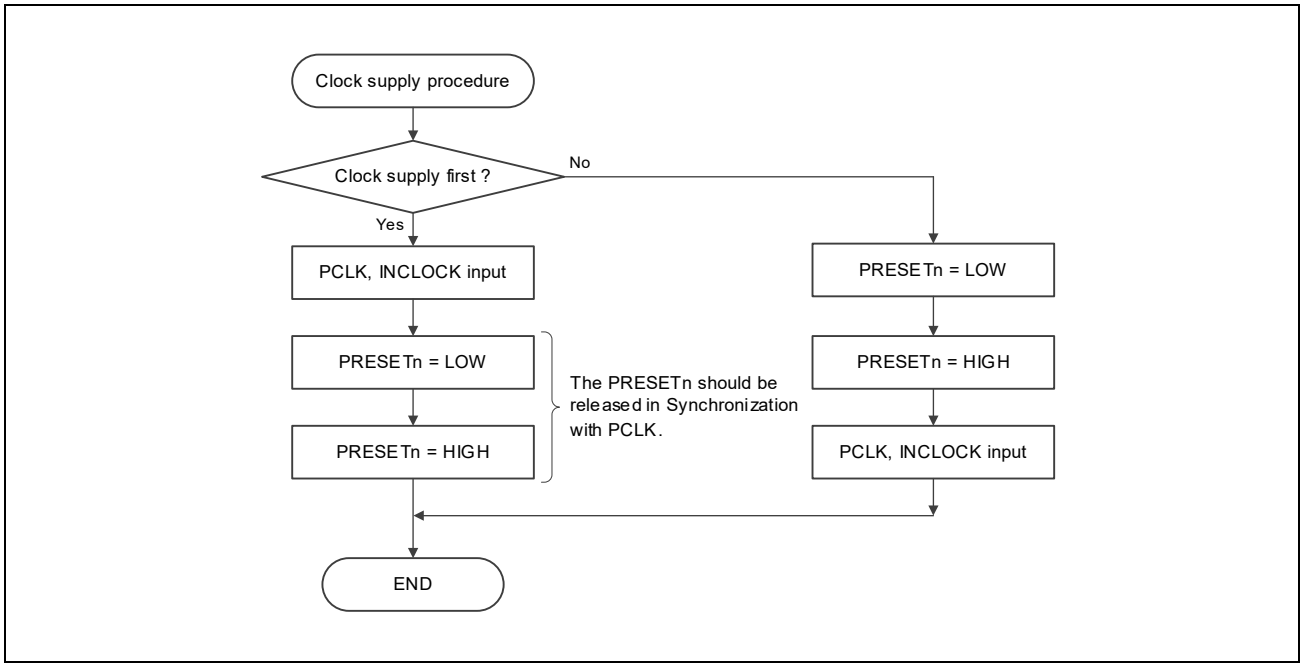


Figure 16.4-2 Clock Supply Procedure

16.4.3 Timer Startup Procedure

This section describes the procedure for starting the timer. Make sure to use the product according to this procedure.

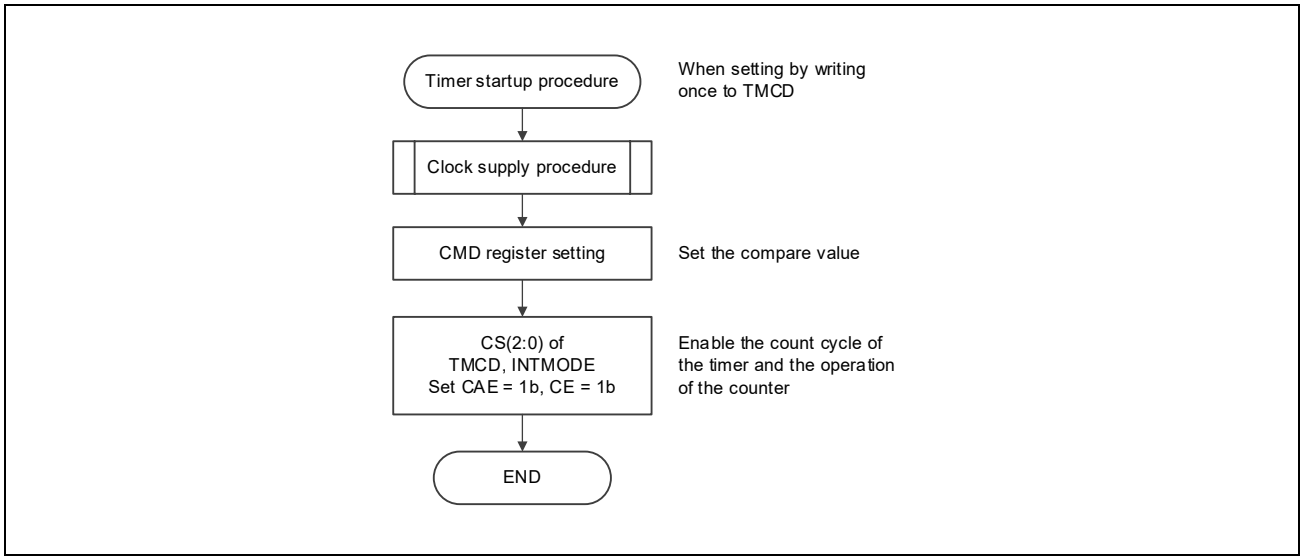


Figure 16.4-3 Timer Startup Procedure (for Writing One Time to TMCD)

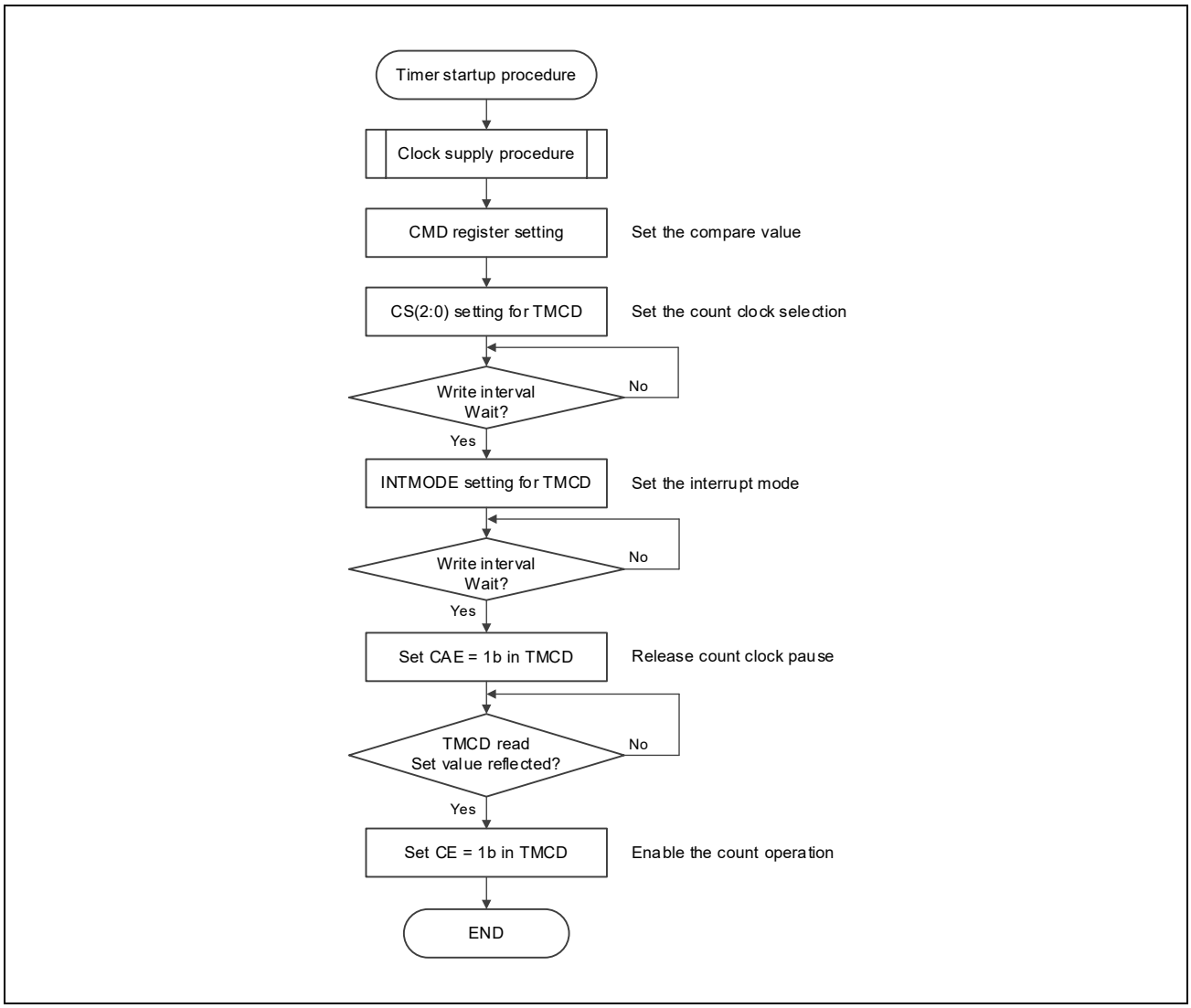
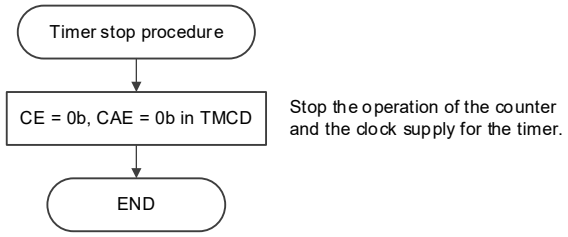


Figure 16.4-4 Timer Startup Procedure (When Writing to TMCD in Multiple Times)

16.4.4 Procedure for Stopping the Timer

This section describes the procedure for stopping the timer.

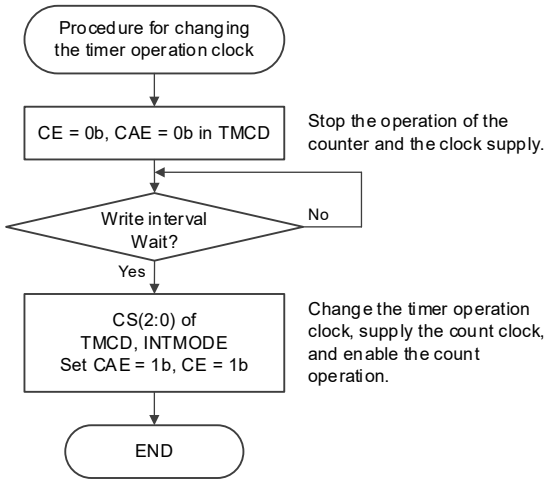


Note: When CE = 0b is set, the counter value and clock divider are initialized.

Figure 16.4-5 Procedure for Stopping the Timer

16.4.5 Procedure for Changing the Operation Clock of the Timer

The following is the procedure for changing the operation clock of the timer.



Note: When CE = 0b is set, the counter value and clock divider are initialized.

Figure 16.4-6 Procedure for Changing the Timer Operation Clock (Counter Operation and Clock Supply Stop)

16.4.6 Procedure for Changing the Compare Value of a Timer

This section describes the procedure for changing the compare value of a timer. If the value is changed while the timer is running, the change will be reflected when the timer interrupt is issued.

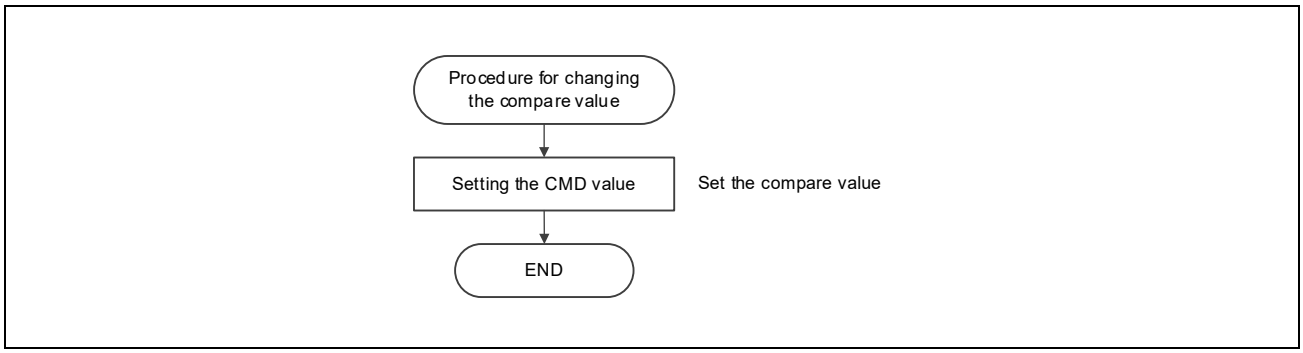
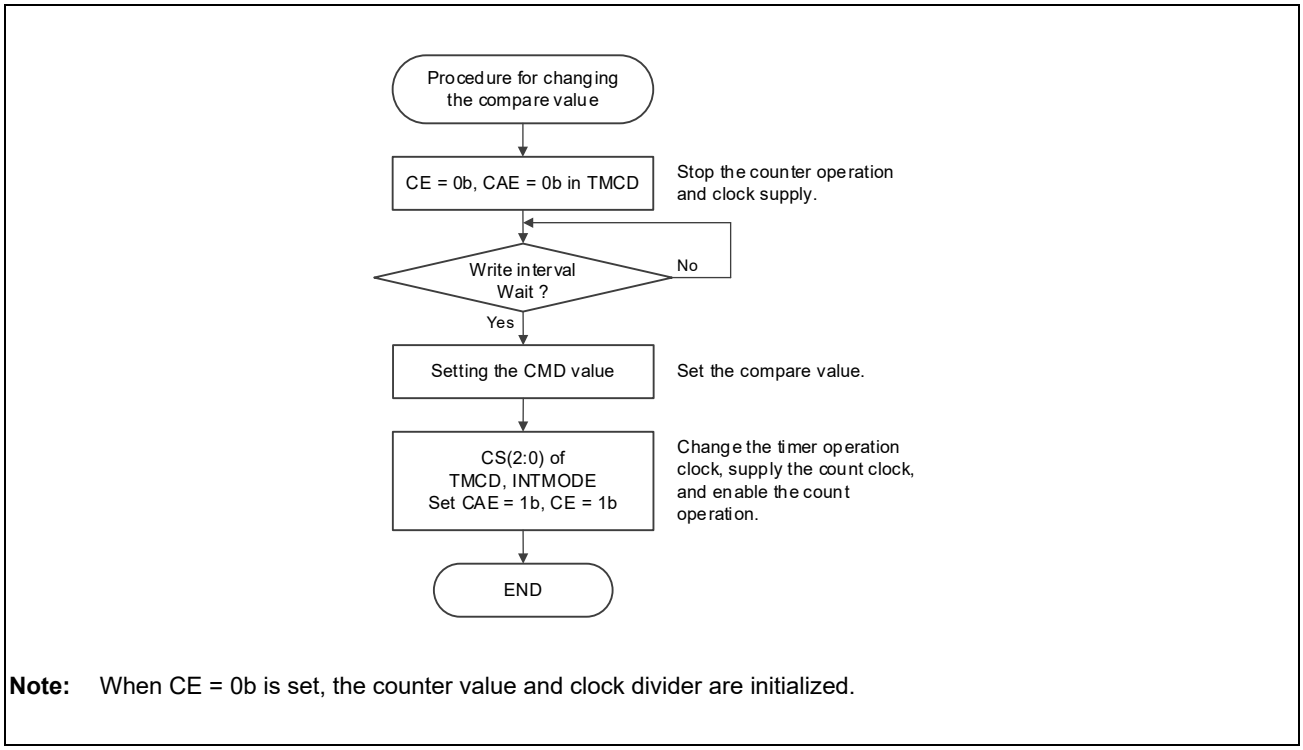


Figure 16.4-7 Procedure for Changing the Compare Value of a Timer (Changing While the Timer is Running)



Note: When CE = 0b is set, the counter value and clock divider are initialized.

Figure 16.4-8 Procedure for Changing the Compare Value of a Timer (After the Timer is Stopped)

16.4.7 Timer Operation

A time lag occurs when writing registers and capturing timer count values, due to the passing of signals between asynchronous clocks.

16.4.7.1 Operation Reflection Timing of Register Setting Values

The following indicates the maximum (slowest) timing between the completion of a write to the register and the time when the write value is reflected in the timer operation.

Table 16.4-1 Operation Reflection Timing of Register Setting Values

Register Name	Software Operation	Timer is Stopped	Timer is Running
CMD	Compare value setting	1 × PCLK + 3 × INCLOCK	Counter clear timing after a compare match following 1 × PCLK + 3 × INCLOCK
TCMD	Count start	Same as above	Same as above
	Count pause	Same as above	Same as above
	Resume from count pause	Same as above	Same as above
	Count stop	Same as above	Same as above
INTCLR	Interrupt clear	Same as above	Same as above

16.4.7.2 Readable Timing of Register Set Value

The folloing indicates the maximum (slowest) timing between the completion of a write to the register and the time when the written value can be read.

Table 16.4-2 Readable Timing of Register

Register Name	Software Operation	Timer is Stopped	Timer is Running
CMD	Compare value setting	5 × PCLK + 5 × INCLOCK	5 × PCLK + 5 × INCLOCK
TCMD	Count start	Same as above	Same as above
	Count pause	Same as above	Same as above
	Resume from count pause	Same as above	Same as above
	Count stop	Same as above	Same as above

16.4.7.3 Count Start Timing

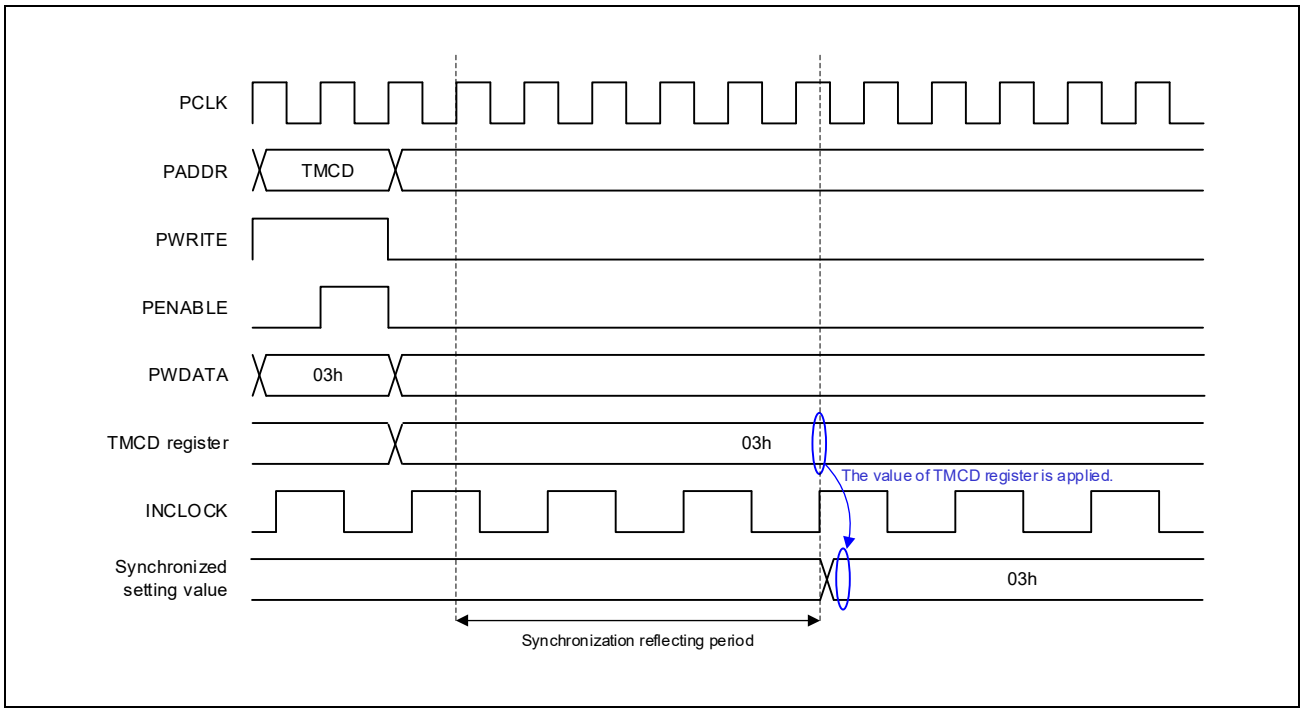


Figure 16.4-9 Count Start Timing

16.4.7.4 Count Stop Timing

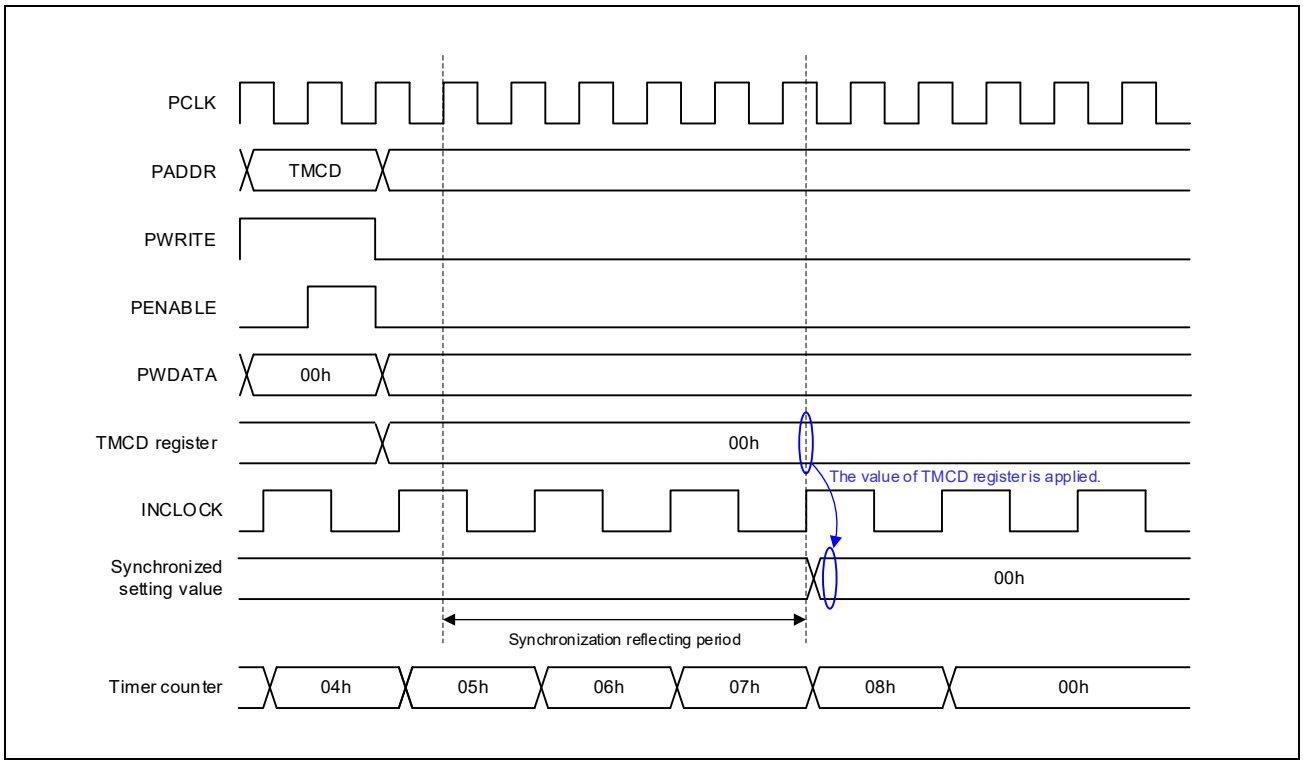


Figure 16.4-10 Count Stop Timing

16.4.7.5 Clear signal (INTCLR) Synchronization Reflection Timing

The clear signal is a 1-bit pulse signal.

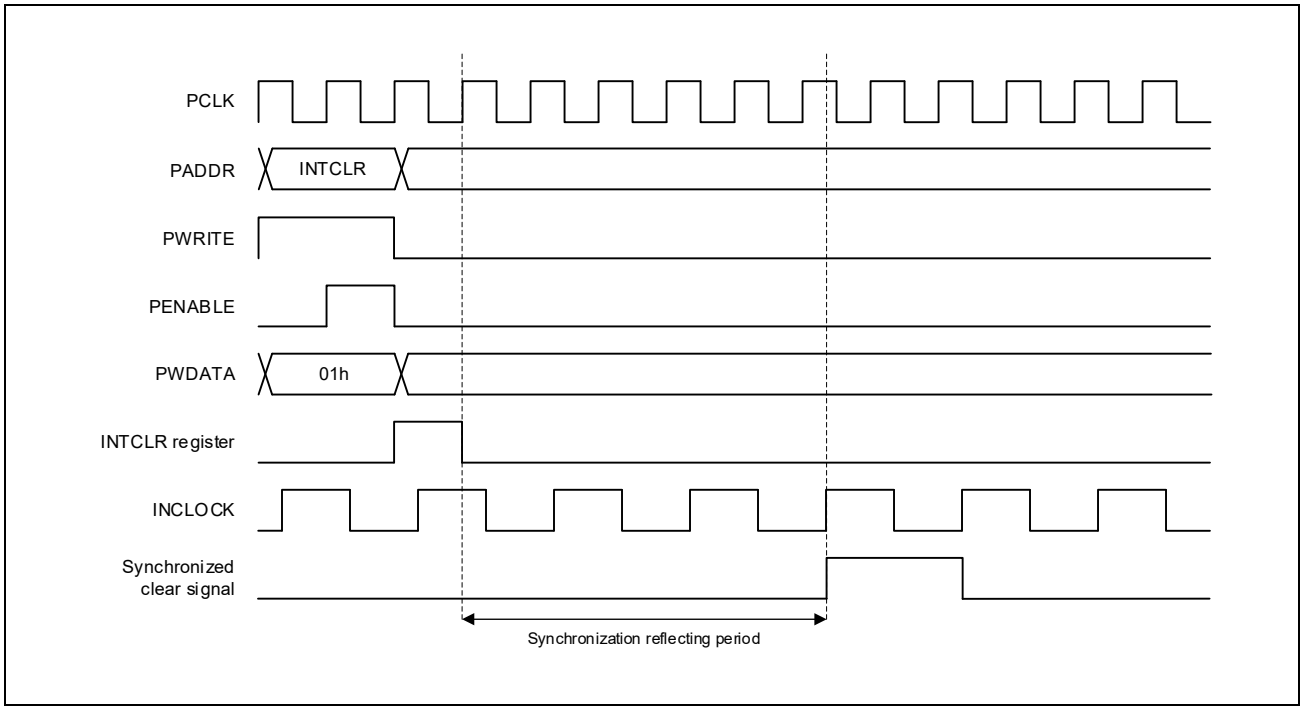


Figure 16.4-11 Reflection Timing of Clear Signal (INTCLR) to INCLOCK Synchronization Register

16.4.7.6 Reflection Timing of Count Value (TMD) to PCLK Synchronization Register

This register has a copy of the count value (TMD) of a timer running with the synchronization of INCLOCK, synchronizes the value of the copy with PCLK, and holds it in a register for reading. When a read is received from the APB bus, the register value for the read is returned. During the period when the count value operating with the synchronization of INCLOCK is synchronized with PCLK, the count value is held. Therefore, the value differs from the actual count value (TMD).

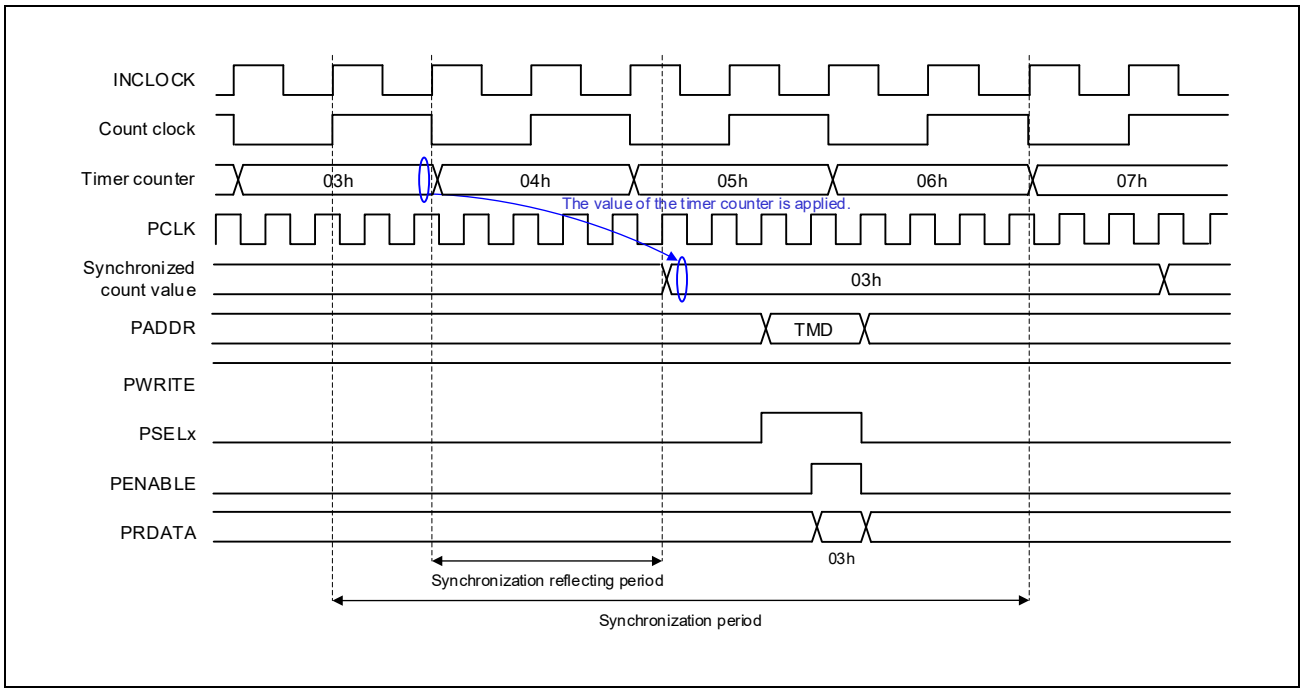


Figure 16.4-12 Reflection Timing of TMD Value to PCLK Synchronization Register

16.4.7.7 Operation Start Condition

The operation is started by writing TMCD:CE = 1b and CAE = 1b. The set values of CE and CAE and the operation of the counter are as follows.

Table 16.4-3 CE, CAE Setting Values and Internal Counter Operation

CE	CAE	Operation
1b	1b	Executes counting operation at rising edge of INCLOCK
1b	0b	Counter pauses (for debugging with ICE)
0b	1b	Counting operation stopped (the counter value is 0)
0b	0b	Counting operation stopped (the counter value is 0)

- INTCMD output timing

  INTCMD can be set pulse mode and level mode by the register. In pulse mode, it is active for one INCLOCK period starting from the rising edge of the next INCLOCK after the TMD and CMD slaves are matched. In level mode, it will remain active until it is cleared.

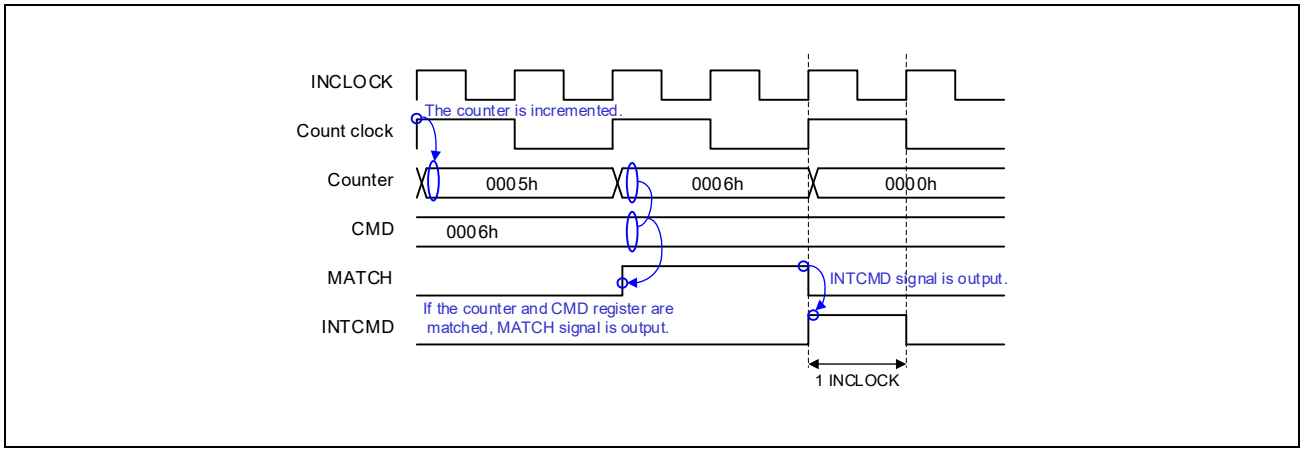


Figure 16.4-13 INTCMD Operation Timing (Pulse Mode)

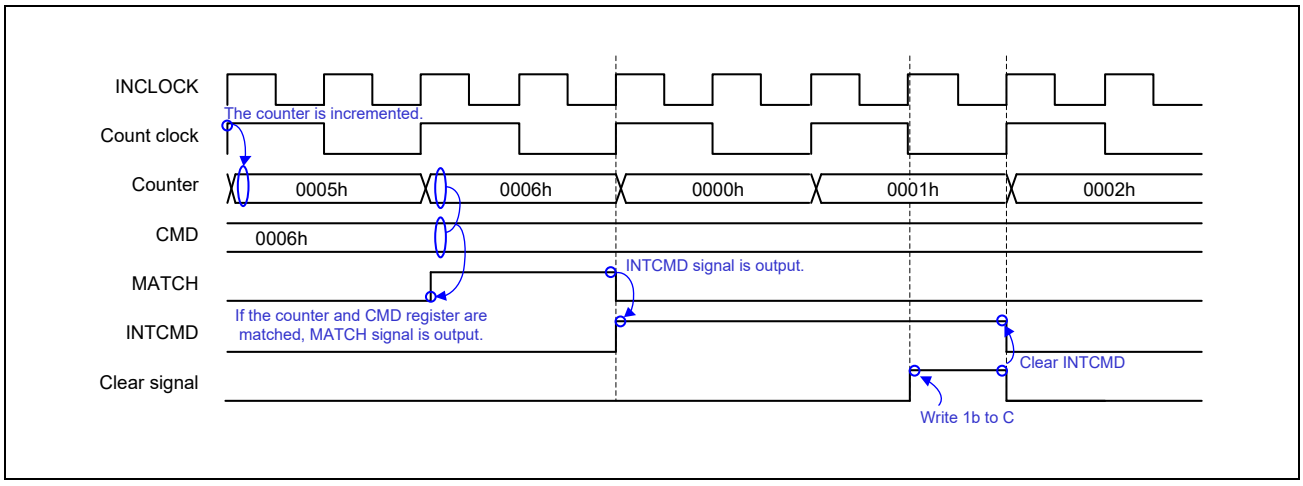


Figure 16.4-14 INTCMD Operation Timing (Level Mode)

Section 17 Pulse-Width Modulation Timer (PWM)

This section describes the functions of the pulse-width modulation timer (PWM).

17.1 Functional Overview

The PWM has a total of 16 channels from ch. 0 to ch. 15. Of those, ch. 0 to ch. 7 and ch. 15 are for use with the ISP support package, so do not use registers related to those channels.

17.1.1 Features

- The PWM has 32-bit counters which operate at PWM_CLK (48 MHz).
- The frequency division ratio for internal counter operation is selectable as PWM_CLK divided by 1, 16, 256, or 2048.
- The period as well as the duty cycle is adjustable.
- The low-level and high-level order of the PWM signals can be inverted.
- The duty cycle of the PWM signal is selectable in the range from 0 to 100%.
- The period of the PWM signal is selectable in the range from 2.4 Hz to 480 kHz.
- The minimum resolution is 20.83 ns.
- Three interrupt sources: Rising and falling edges of the PWM signal and clearing of the counter
- Counter operation and the bus interface are asynchronous and both can operate independently of the magnitude relationship of the respective clock periods.

17.1.2 Block Diagram

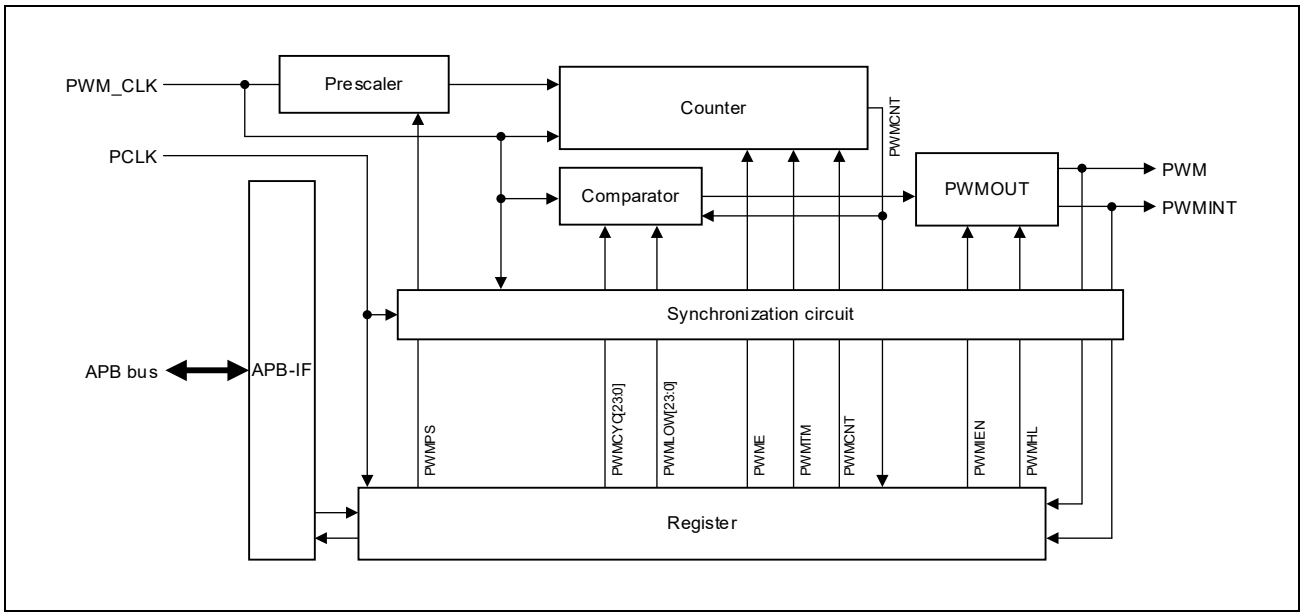


Figure 17.1-1 Block Diagram

17.1.3 Connection Configuration

Figure 17.1-2 shows the connection diagram of the PWM.

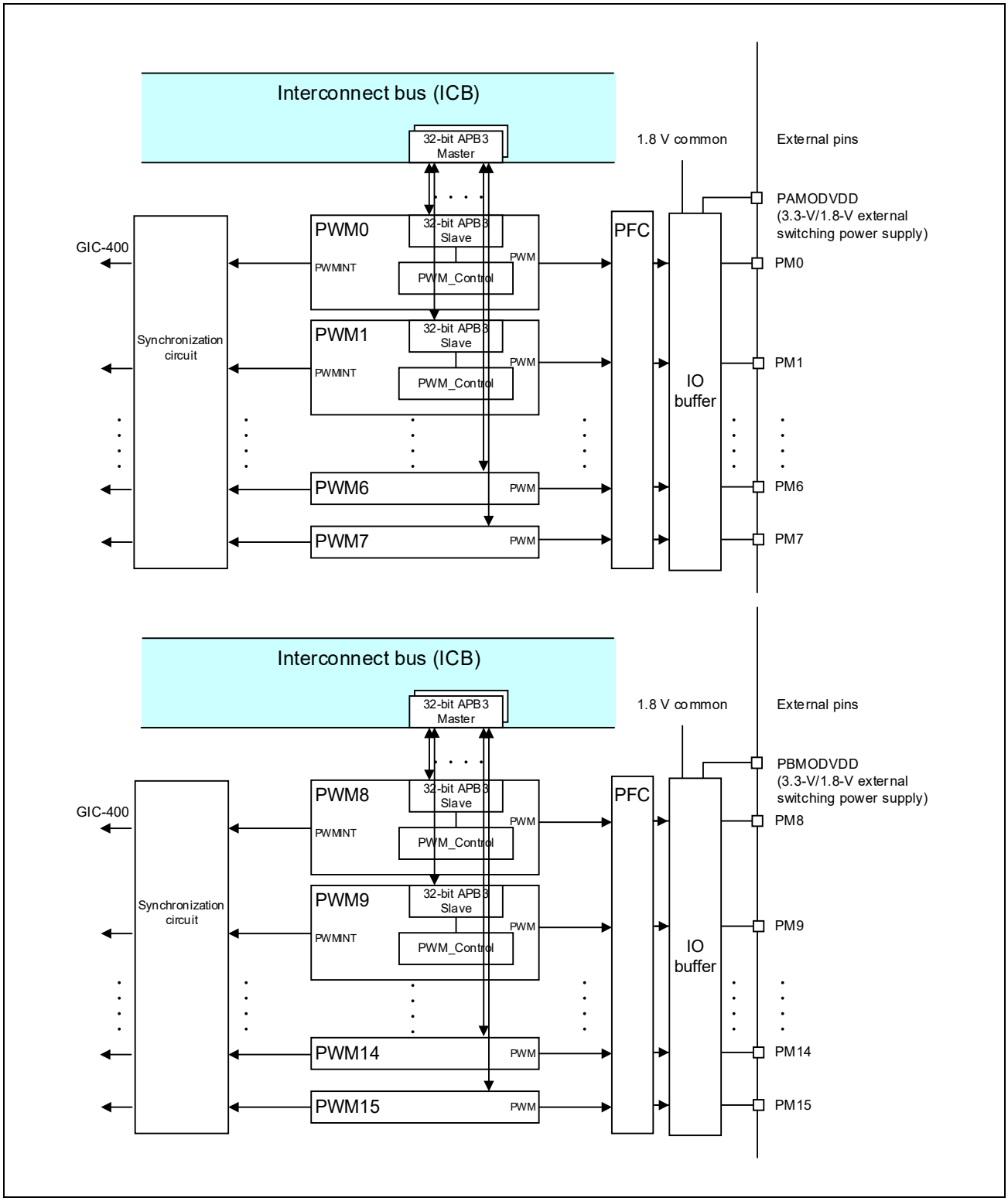


Figure 17.1-2 Schematic of the PWM Connection

17.2 Pin Functions

17.2.1 List of Internal Pins

Table 17.2-1 lists the internal pins of the PWM.

Table 17.2-1 List of Internal Pins

Classification	Pin Name	I/O	Function
PWM Related Pins	PWM_CLK	Input	PWM Counter Operating Clock
	PWM	Output	PWM Output Signal
Debugging Pin	PWMINT	Output	PWM Interrupt Request Output Signal This signal is connected to the interrupt controller as a level interrupt signal.

17.2.1.1 How to Control Resetting

PRESETn is an asynchronous input and internally works with the synchronous reset release circuits per clock domain. After the de-assertion of PRESETn, do not attempt access during the period 2 × PCLK + 2 × PWM_CLK as the synchronous reset release circuit leaves the reset retained over this period.

The PRDATA[31:0] pins are reset to the low level in synchronization with the PCLK clock. As shown in **Figure 17.2-1**, when the low level is input to the PRESETn signal, the low level (the initial value) is output after one clock cycle in synchronization with the rising edge of PCLK. Resetting these pins requires PCLK.

The PWMINT pin is reset to the low level in synchronization the WM_CLK clock. Resetting this pin requires PWM_CLK.

The PWM pin is reset to the low level asynchronously with the clock.

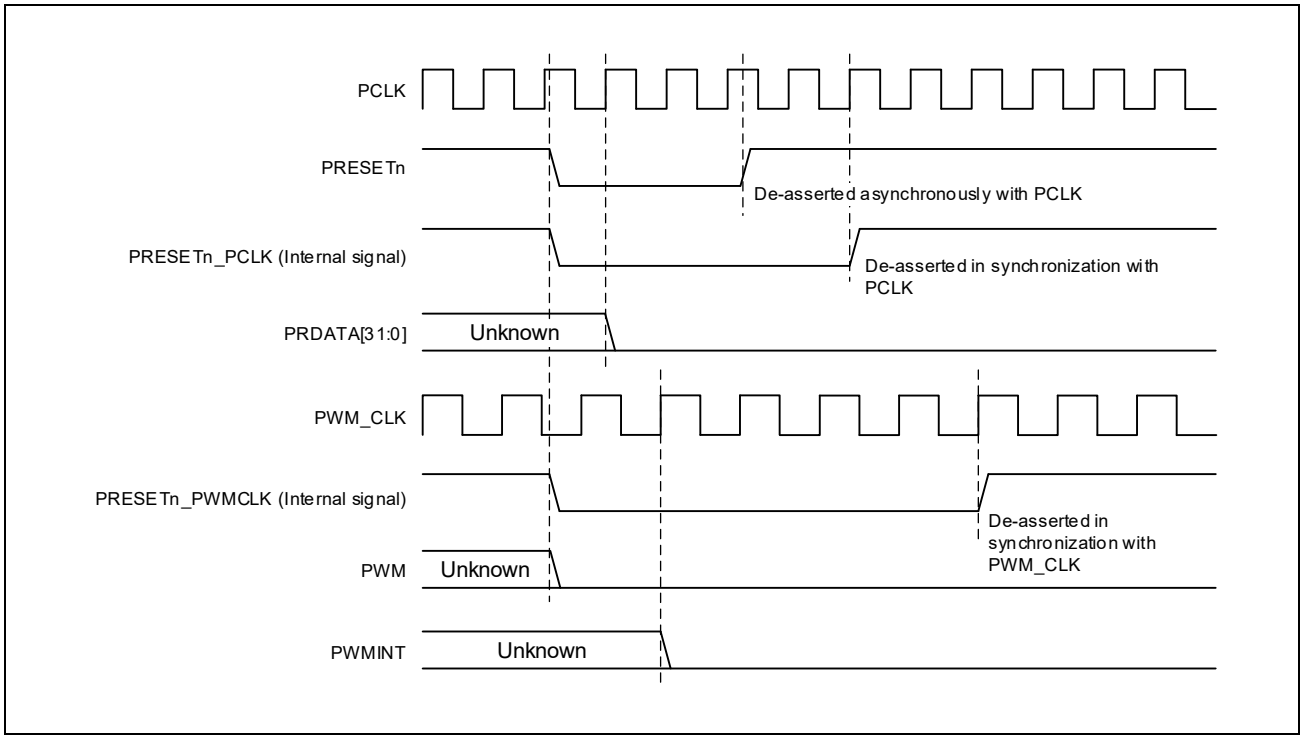


Figure 17.2-1 Reset Timing

17.2.1.2 Interrupt Timing

The figure below shows the timings of output of the three types of interrupt, rising and falling edges of the PWM signal and clearing of the counter.

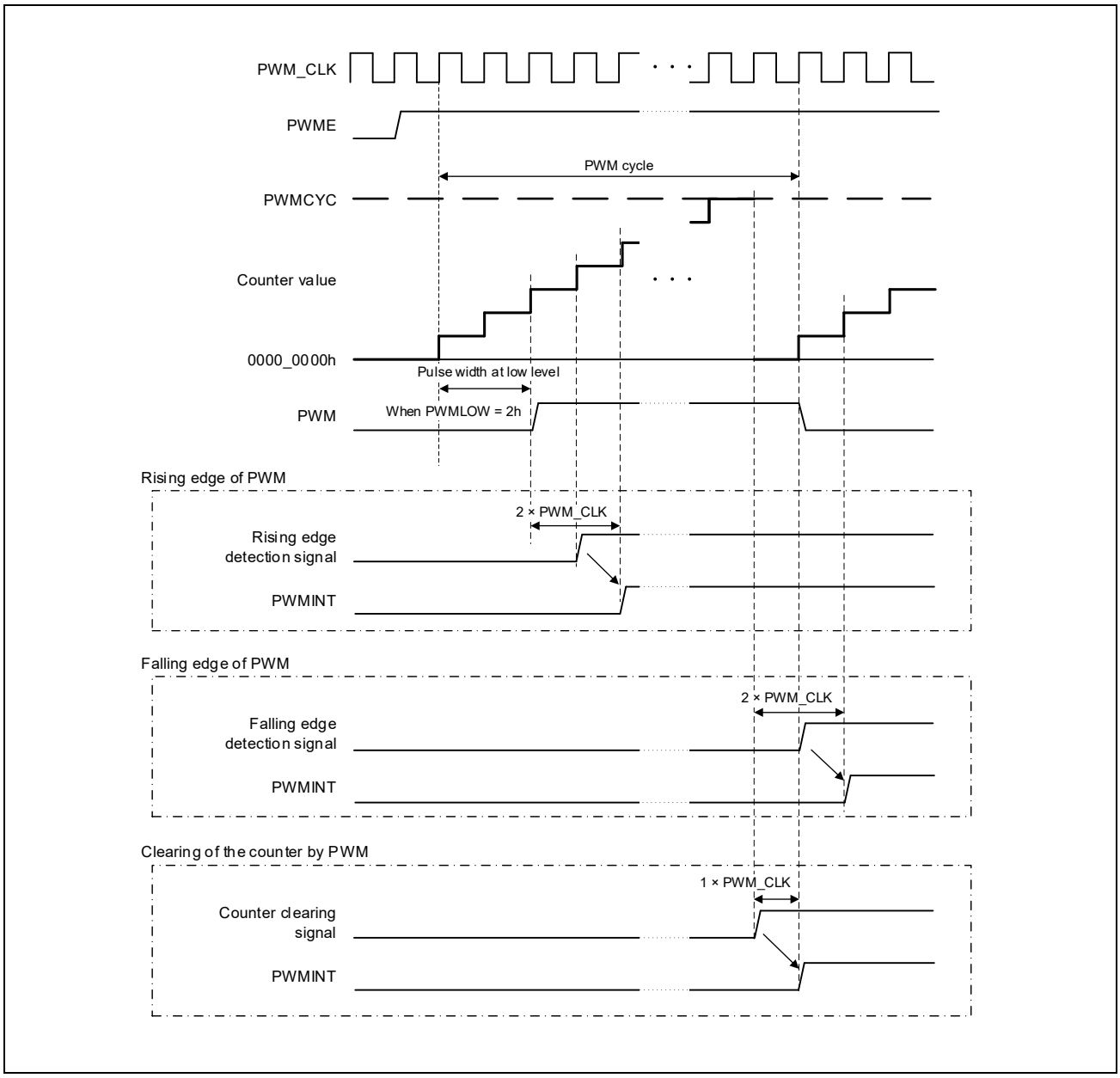


Figure 17.2-2 Interrupt Output Timing

17.3 Register Descriptions

For the register base addresses (<PWM0_S0_base> to <PWM15_S0_base>), see the section of Address Map.

17.3.1 List of Registers

Table 17.3-1 lists the registers.

Table 17.3-1 List of Registers

Offset Address	Register Name	Abbreviation*1	Initial Value	Access Unit (bits)
000h	PWM control register	PWMm_PWMCTR	0000_0000h	32
004h	PWM cycle setting register	PWMm_PWMCYC	0000_0000h	32
008h	PWM low-level width setting register	PWMm_PWMLOW	0000_0000h	32
00Ch	PWM counter register	PWMm_PWMCNT	0000_0000h	32
010h	PWM interrupt enable register	PWMm_PWMIEN	0000_0000h	32
014h	PWM interrupt register	PWMm_PWMINT	0000_0000h	32
018h to 01Ch	Reserved area	Reserved	Undefined	32

Note 1. m = 0 to 15

17.3.2 Register Descriptions

The function of each register is given below.

17.3.2.1 PWM Control Register (PWMm_PWMCTR) (m = 0 to 15)

This register controls the PWM operation.

Access Size: 32 bits

Address(es):

<PWM0_S0_base> + 0000h	<PWM8_S0_base> + 0000h
<PWM1_S0_base> + 0000h	<PWM9_S0_base> + 0000h
<PWM2_S0_base> + 0000h	<PWM10_S0_base> + 0000h
<PWM3_S0_base> + 0000h	<PWM11_S0_base> + 0000h
<PWM4_S0_base> + 0000h	<PWM12_S0_base> + 0000h
<PWM5_S0_base> + 0000h	<PWM13_S0_base> + 0000h
<PWM6_S0_base> + 0000h	<PWM14_S0_base> + 0000h
<PWM7_S0_base> + 0000h	<PWM15_S0_base> + 0000h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWMPS[17:16]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	PWMHL	PWMTM	PWME	PWMS
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	R

Table 17.3-2 PWMm_PWMCTR Register Contents

Bit Position	Bit Name	Description
31 to 18	—	Reserved. These bits are read as 0b. The write value should always be 0b.
17, 16	PWMPS[17:16]	PWM operation clock frequency division setting (PWM_CLK frequency division). 00b: Frequency division by 1 (no frequency division) 01b: Frequency division by 16 10b: Frequency division by 256 11b: Frequency division by 2048
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3	PWMHL	PWM signal output level setting 0b: The PWM signal is output as it is. 1b: The PWM signal is inverted and output.
2	PWMTM	PWM counter setting (PMW counter initial value setting) When this bit is set to 1b, any count value can be set in the PWMm_PWMCNT register, which is a PWM counter. Set this bit to 0b when operating the PWM.
1	PWME	Enable counter operation 0b: Disable 1b: Enable
0	PWMS	The PWM output value can be read.

Note: The relationship between PWMTM bit and PWME bit is shown in **Table 17.3-2a**.

Table 17.3-2a

PWMTM	PWME	Description
1	X	Any count value can be set in the PWMm_PWMCNT register, which is a PWM counter.
0	0	Counter is stopped and cleared.
0	1	Counter is counting up.

Note: x = Don’t care

17.3.2.2 PWM Cycle Setting Register (PWMm_PWMCYC) (m = 0 to 15)

This register is a 24-bit register that sets the cycle of the counter that generates PWM output. The setting value to the PWMm_PWMCYC register is obtained by the following formula.

PWMm_PWMCYC register setting value = (PWM period (ns) / (PWM_CLK period (ns) × Division ratio)) − 1

(*Ex*) When the period of the counter that generates PWM is 100,000,000 ns (10 Hz), the period of PWM_CLK is 20.8333 ns (48 MHz), and the PWM_CLK division setting is 1, the setting value of the PWMm_PWMCYC register is as follows.

PWMm_PWMCYC register setting value = (100,000,000ns / (20.8333 ns × 1)) − 1
= 4,800,000
= 493E00h

Note: To change the setting value of the PWM cycle setting register (PWMm_PWMCYC), set the PWME bit of the PWM control register (PWMm_PWMCTR) to 0b and stop the counter operation. If it is changed during counter operation, PWM output may not be performed correctly.

Access Size: 32 bits

Address(es):

<PWM0_S0_base> + 0004h	<PWM8_S0_base> + 0004h
<PWM1_S0_base> + 0004h	<PWM9_S0_base> + 0004h
<PWM2_S0_base> + 0004h	<PWM10_S0_base> + 0004h
<PWM3_S0_base> + 0004h	<PWM11_S0_base> + 0004h
<PWM4_S0_base> + 0004h	<PWM12_S0_base> + 0004h
<PWM5_S0_base> + 0004h	<PWM13_S0_base> + 0004h
<PWM6_S0_base> + 0004h	<PWM14_S0_base> + 0004h
<PWM7_S0_base> + 0004h	<PWM15_S0_base> + 0004h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	PWMCYC[23:16]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PWMCYC[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 17.3-3 PWMm_PWMCYC Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 0	PWMCYC[23:0]	Counter cycle value

17.3.2.3 PWM Low Width Setting Register (PWMm_PWMLOW) (m = 0 to 15)

This is a 24-bit register that sets the low pulse width of the PWM signal.

When the count clock source PWM_CLK = 100 [MHz], the low pulse width with a resolution of 10 [ns] can be registered. When the counter value matches the value set in the PWMLOW register, the PWM output goes high at the next clock rise. If the counter value is less than or equal to the value set in the PWMLOW register, the PWM output goes low at the next clock rise. If the PWMLOW register is changed during counter operation, the set value becomes valid after the current PWM cycle ends.

The setting value of the PWMm_PWMLOW register is obtained by the following formula.

Setting value of PWMm_PWMLOW register = PWMm_PWMCYC register setting value (decimal) × Low pulse width ratio (%)

(*Ex*) When the setting value of the PWMm_PWMCYC register 9,999,999 (counter frequency to generate PWM 10 [Hz]) and the low pulse width ratio is 90%, the setting value of the PWMm_PWMLOW register is as follows.

PWMm_PWMLOW register setting value = 9,999,999 × 0.90
= 8,999,999.1
= 89543Fh

The same calculation is performed as follows.

When PWMm_PWMLOW register = 000000h, low : high = 0 : 100 (low width 0%)
When PWMm_PWMLOW register = 4C4B3Fh, low : high = 50 : 50 (low width 50%)
When PWMm_PWMLOW register = 89543Fh, low : high = 90 : 10 (low width 90%)
When PWMm_PWMLOW register > 98967Fh, low : high = 100 : 0 (low width 100%)

Access Size: 32 bits

Address(es):

<PWM0_S0_base> + 0008h	<PWM8_S0_base> + 0008h
<PWM1_S0_base> + 0008h	<PWM9_S0_base> + 0008h
<PWM2_S0_base> + 0008h	<PWM10_S0_base> + 0008h
<PWM3_S0_base> + 0008h	<PWM11_S0_base> + 0008h
<PWM4_S0_base> + 0008h	<PWM12_S0_base> + 0008h
<PWM5_S0_base> + 0008h	<PWM13_S0_base> + 0008h
<PWM6_S0_base> + 0008h	<PWM14_S0_base> + 0008h
<PWM7_S0_base> + 0008h	<PWM15_S0_base> + 0008h

Initial Value: 0000_0000h

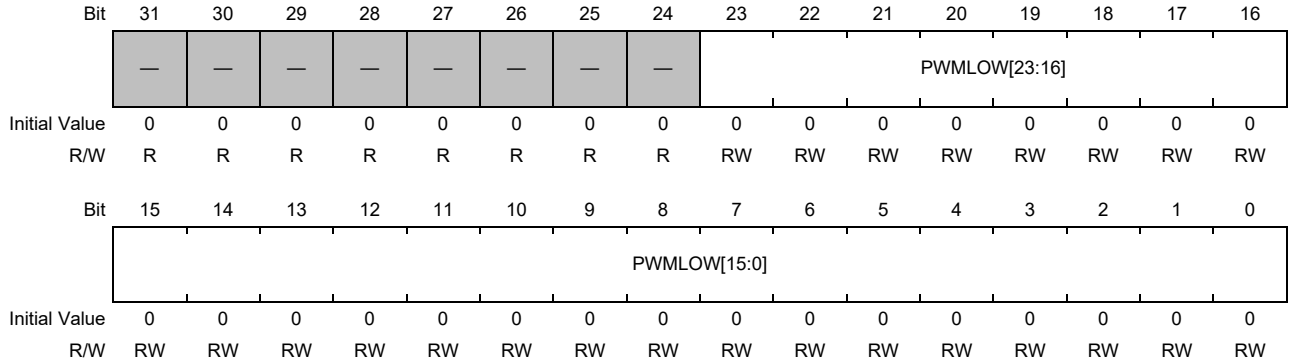


Table 17.3-4 PWMm_PWMLOW Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 0	PWMLOW[23:0]	Sets the low level pulse width of the PWM signal.

17.3.2.4 PWM Counter Register (PWMm_PWMCNT) (m = 0 to 15)

When the PWMm_PWMCNT register is read, the PWM counter value can be read.

The counter counts up when the PWMTM bit in the PWMCTR register = 0 and the PWME bit in the PWMm_PWMCTR register = 1, and continues to count up within the range set by the PWMm_PWMCYC register. When the PWMTM bit in the PWMm_PWMCTR register is 0b and the PWME bit in the PWMm_PWMCTR register is 0b, the count is stopped and the count value is 0b.

Since the PWMm_PWMCNT register stores the count value synchronized with PCLK, the value before the actual count value is read.

This register can be written only when PWMTM bit = 1 (PWM counter setting) in the PWMm_PWMCTR register is set. Note that when the PWMCNT bit is set to 0b with the PWMTM bit = 1 (PWM counter setting) or the count value is set to 0b and the counter is stopped (PWME bit = 0 in the PWMm_PWMCTR register), the counter clear interrupt is not generated.

Access Size: 32 bits

Address(es):

<PWM0_S0_base> + 000Ch	<PWM8_S0_base> + 000Ch
<PWM1_S0_base> + 000Ch	<PWM9_S0_base> + 000Ch
<PWM2_S0_base> + 000Ch	<PWM10_S0_base> + 000Ch
<PWM3_S0_base> + 000Ch	<PWM11_S0_base> + 000Ch
<PWM4_S0_base> + 000Ch	<PWM12_S0_base> + 000Ch
<PWM5_S0_base> + 000Ch	<PWM13_S0_base> + 000Ch
<PWM6_S0_base> + 000Ch	<PWM14_S0_base> + 000Ch
<PWM7_S0_base> + 000Ch	<PWM15_S0_base> + 000Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	PWMCNT[23:16]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W	R0W	R0W	R0W	R0W	R0W	R0W	R0W	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PWMCNT[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 17.3-5 PWMm_PWMCNT Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 0	PWMCNT[23:0]	The counter value of PWM can be read. It counts up with PWM_CLK.

17.3.2.5 PWM Interrupt Enable Register (PWMm_PWMIEN) (m = 0 to 15)

This register enables or disables output to the interrupt request output signal (PWMINT) for three interrupt factors. Multiple bits can be set at the same time.

Access Size: 32 bits

Address(es):

<PWM0_S0_base> + 0010h	<PWM8_S0_base> + 0010h
<PWM1_S0_base> + 0010h	<PWM9_S0_base> + 0010h
<PWM2_S0_base> + 0010h	<PWM10_S0_base> + 0010h
<PWM3_S0_base> + 0010h	<PWM11_S0_base> + 0010h
<PWM4_S0_base> + 0010h	<PWM12_S0_base> + 0010h
<PWM5_S0_base> + 0010h	<PWM13_S0_base> + 0010h
<PWM6_S0_base> + 0010h	<PWM14_S0_base> + 0010h
<PWM7_S0_base> + 0010h	<PWM15_S0_base> + 0010h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	PWMER	PWMEF	PWMEC
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 17.3-6 PWMm_PWMIEN Register Contents

Bit Position	Bit Name	Description
31 to 3	—	Reserved. These bits are read as 0b. The write value should always be 0b.
2	PWMER	Enables interrupt output at the rising edge of PWM. 0b: Disable 1b: Enable
1	PWMEF	Enables interrupts at the falling edge of PWM. 0b: Disable 1b: Enable
0	PWMEC	Enables interrupts when the counter is cleared. 0b: Disable 1b: Enable

17.3.2.6 PWM Interrupt Register (PWMm_PWMINT) (m = 0 to 15)

This register monitors and clears the interrupt status.

When reading, the interrupt status can be monitored. When writing, the interrupt is cleared by writing 1b. When 0b is written, the interrupt will not be cleared.

Access Size: 32 bits

Address(es):

<PWM0_S0_base> + 0014h	<PWM8_S0_base> + 0014h
<PWM1_S0_base> + 0014h	<PWM9_S0_base> + 0014h
<PWM2_S0_base> + 0014h	<PWM10_S0_base> + 0014h
<PWM3_S0_base> + 0014h	<PWM11_S0_base> + 0014h
<PWM4_S0_base> + 0014h	<PWM12_S0_base> + 0014h
<PWM5_S0_base> + 0014h	<PWM13_S0_base> + 0014h
<PWM6_S0_base> + 0014h	<PWM14_S0_base> + 0014h
<PWM7_S0_base> + 0014h	<PWM15_S0_base> + 0014h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	PWMIR	PWMIF	PWMIC
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 17.3-7 PWMm_PWMINT Register Contents

Bit Position	Bit Name	Description
31 to 3	—	Reserved. These bits are read as 0b. The write value should always be 0b.
2	PWMIR	Interrupts generated at the rising edge of PWM can be monitored. Read 0: No interrupt occurred Read 1: Interrupt generated Write 0: Retention Write 1: Clear interrupt
1	PWMIF	Interrupts generated at the falling edge of PWM can be monitored. Read 0: No interrupt occurred Read 1: Interrupt generated Write 0: Retention Write 1: Clear interrupt
0	PWMIC	Interrupts generated by counter clear can be monitored. Read 0: No interrupt occurred Read 1: Interrupt generated Write 0: Retention Write 1: Clear interrupt

17.4 Function Details

The prefix (PWMm_) of the register names is omitted in this and subsequent sections.

17.4.1 PWM Signal Output

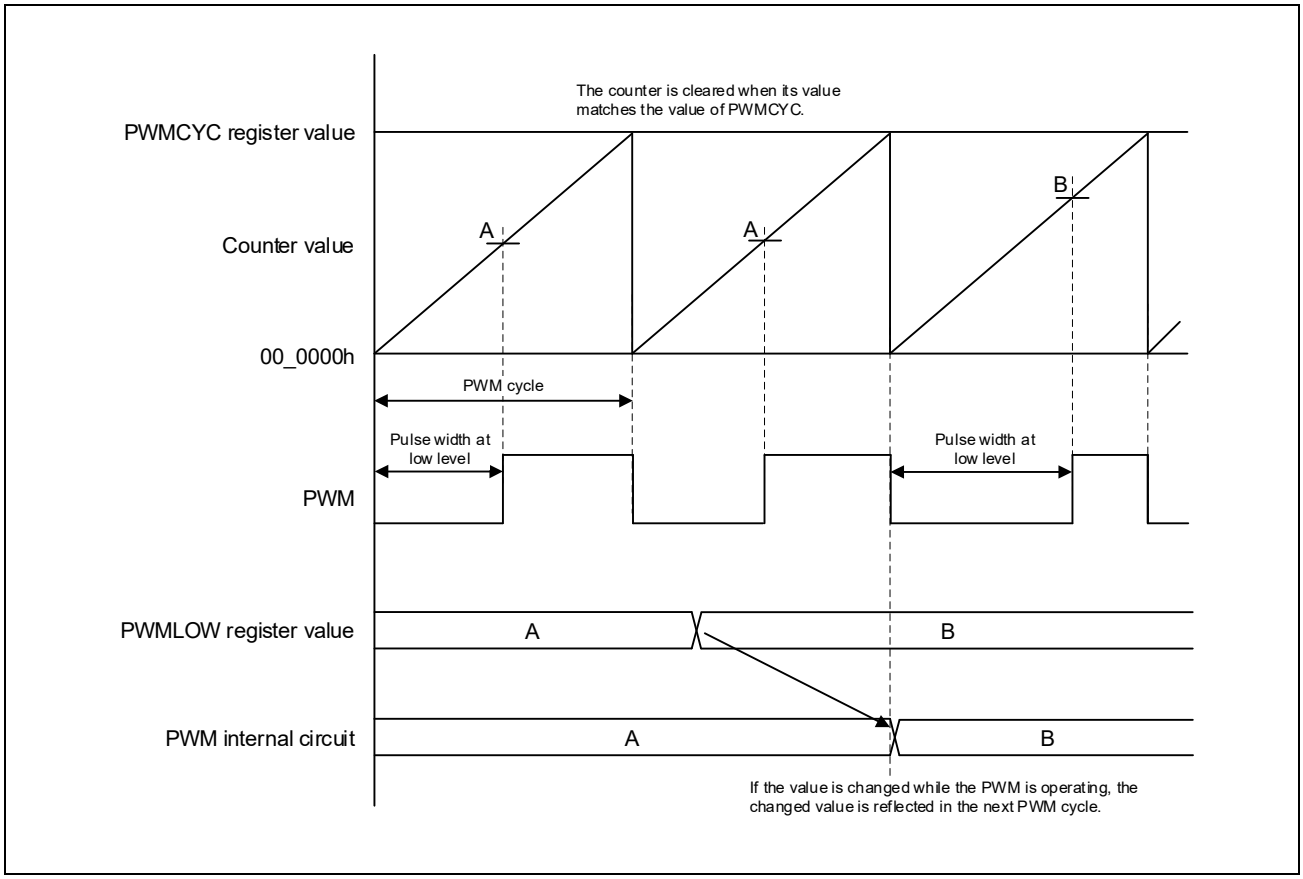


Figure 17.4-1 PWM Pin Operation Timing

The counter counts up from 0000_0000h on the rising edge of PWM_CLK. It is cleared when its value matches the value of the PWMCYC register and counts up again from 0000_0000h until its value matches that of the PWMCYC register. After that, the counter repeats this operation.

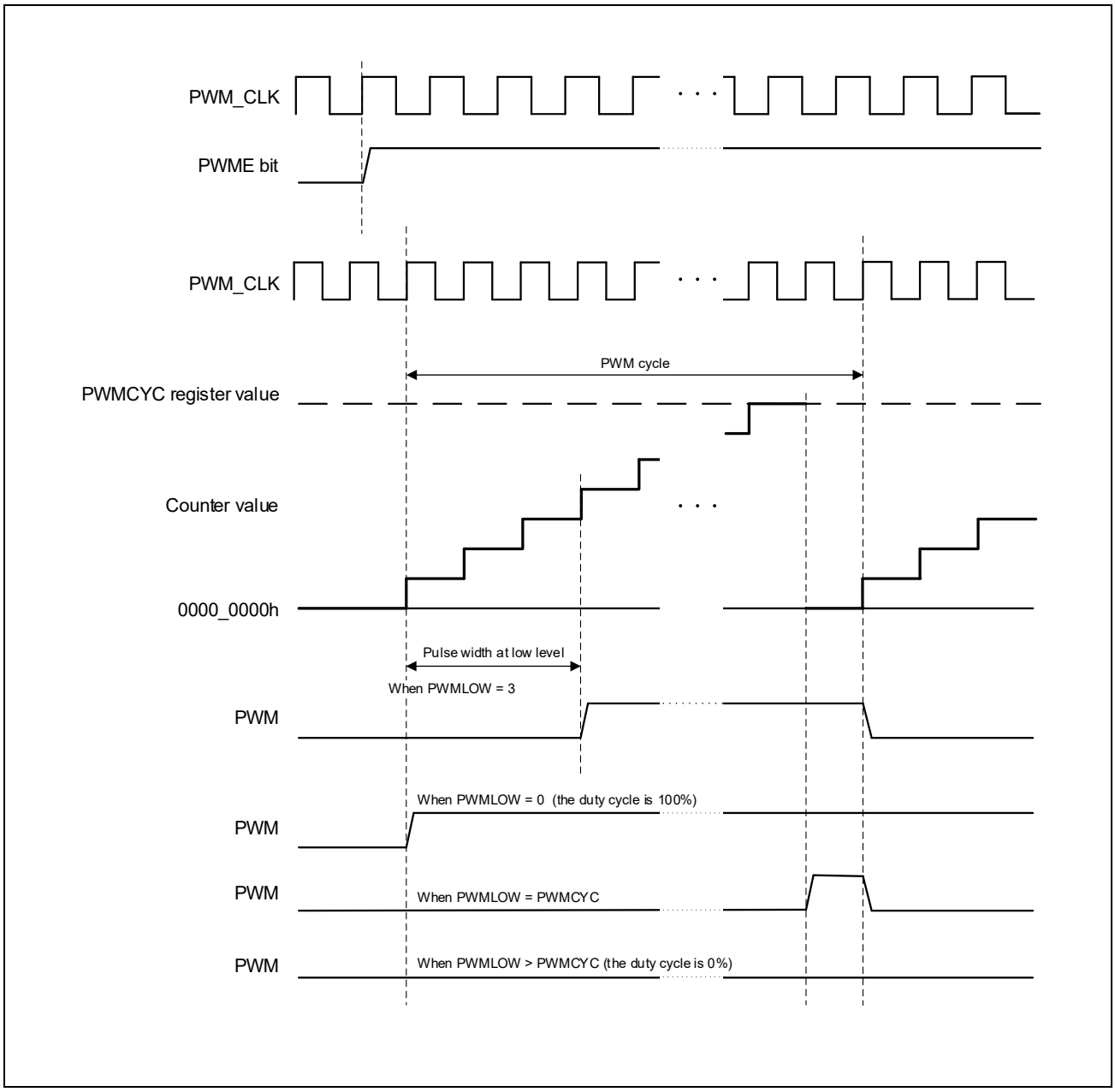


Figure 17.4-2 PWM Output Timing Details

The counter starts counting up on the rising edge of PWM_CLK when the PWME bit of the PWM control register (PWMCTR) is set to 1. The PWM signal remains at the low level until counting starts. When the counter value matches the value of the PWMLOW register, the PWM output is driven to high on the next rising edge of the clock.

The output level (low or high) setting of the PWM signal can be set by using the PWMHL bit of the PWM control register (PWMCTR) and the PWM signal is inverted and output if the output level setting of the PWM signal is 1 (i.e., the PWMHL bit = 1).

Figure 17.4-2 shows the respective timings of the PWM signal when the output level setting of the PWM signal is 0 (PWMHL = 0b), the PWMLOW register values are 3 and 0 (the duty cycle is 100%), when the PWMLOW register value is equal to that of the PWMCYC register, and when the PWMLOW register value is greater than the PWMCYC register value (the duty cycle is 0%).

17.4.2 Changing the Duty Cycle

Changing the duty cycle is possible by modifying the PWMLOW register value and changing the pulse width at low level. The duty cycle becomes 0% for the low width when the value of the PWMLOW register is 0000_0000h and 100% for the low width when the value of the PWMLOW register value is greater than that of the PWM cycle setting register (PWMCYC).

The PWMLOW register value can be changed even while the PWM is operating. The changed PWMLOW register value is reflected in the pulse width at low level of the next PWM cycle as shown in **Figure 17.4-1**. If the PWMLOW register is read immediately after it has been set, the new value may be read even before the PWM is operating in the way which reflects the changed value.

17.4.3 Stipulation on the Interval of Writing to the PWM Interrupt Register (PWMINT)

Following the completion of write access to the PWM interrupt register (PWMINT), a period for synchronization is required to synchronize the written data with PWM_CLK. In write access to the PWMINT register, an interval*1 of at least 5 × PCLK + 5 × PWM_CLK is required between writing once access and writing the next time.

Note 1. If the interval of writing is not secured, the interrupt request signal may not be de-asserted. In such cases, confirm that the interrupt source has been de-asserted after writing before proceeding with the next writing.

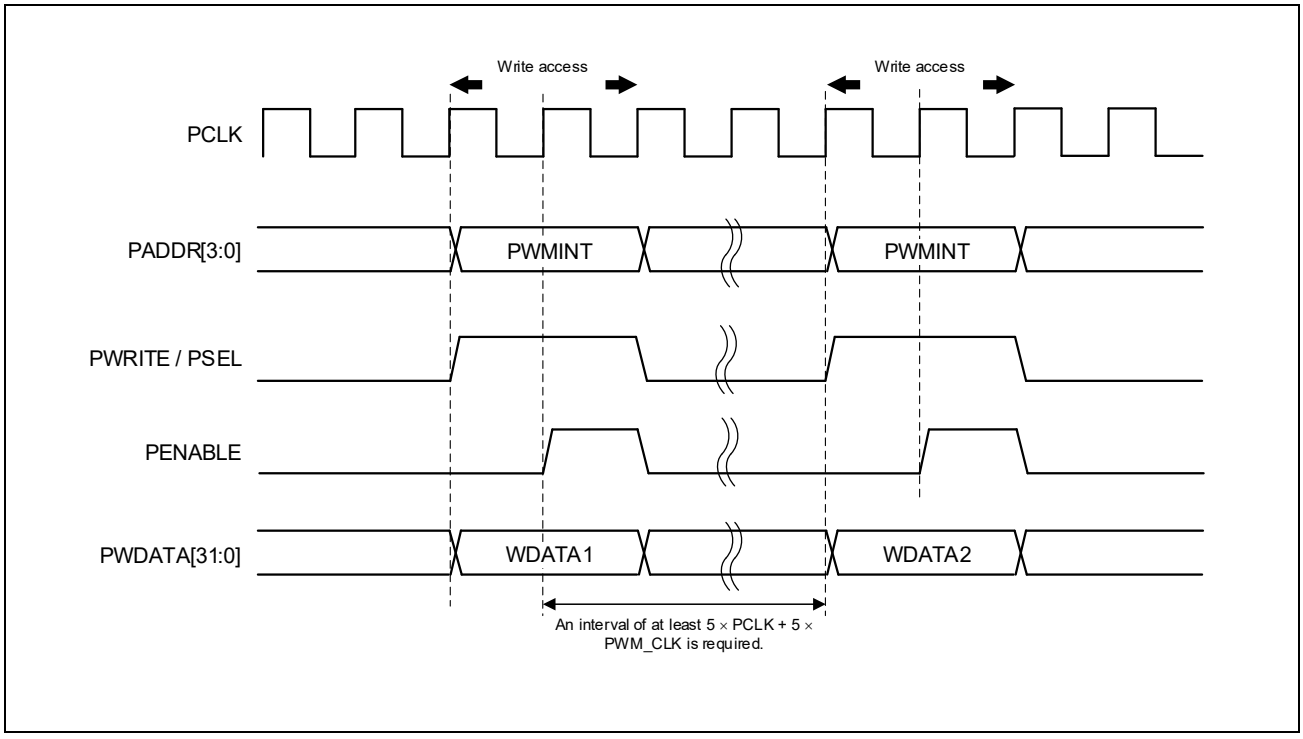


Figure 17.4-3 Stipulation on the Interval of Writing to the PWMINT Register

17.4.4 Timing at which Register Values are Reflected in PWM Operation

The registers other than the PWM interrupt register (PWMINT) are always synchronized with PWM_CLK at regular intervals.

It takes some time (Min: 2 × PCLK + 4 × PWM_CLK to Max: 6 × PCLK + 9 × PWM_CLK) for the value set in the register to be reflected in the PWM circuit because there is a synchronizer between the register and the PWM circuit.

Figure 17.4-4 shows how the written data are synchronized at the minimum period. **Figure 17.4-5** shows how the written data are synchronized at the maximum period.

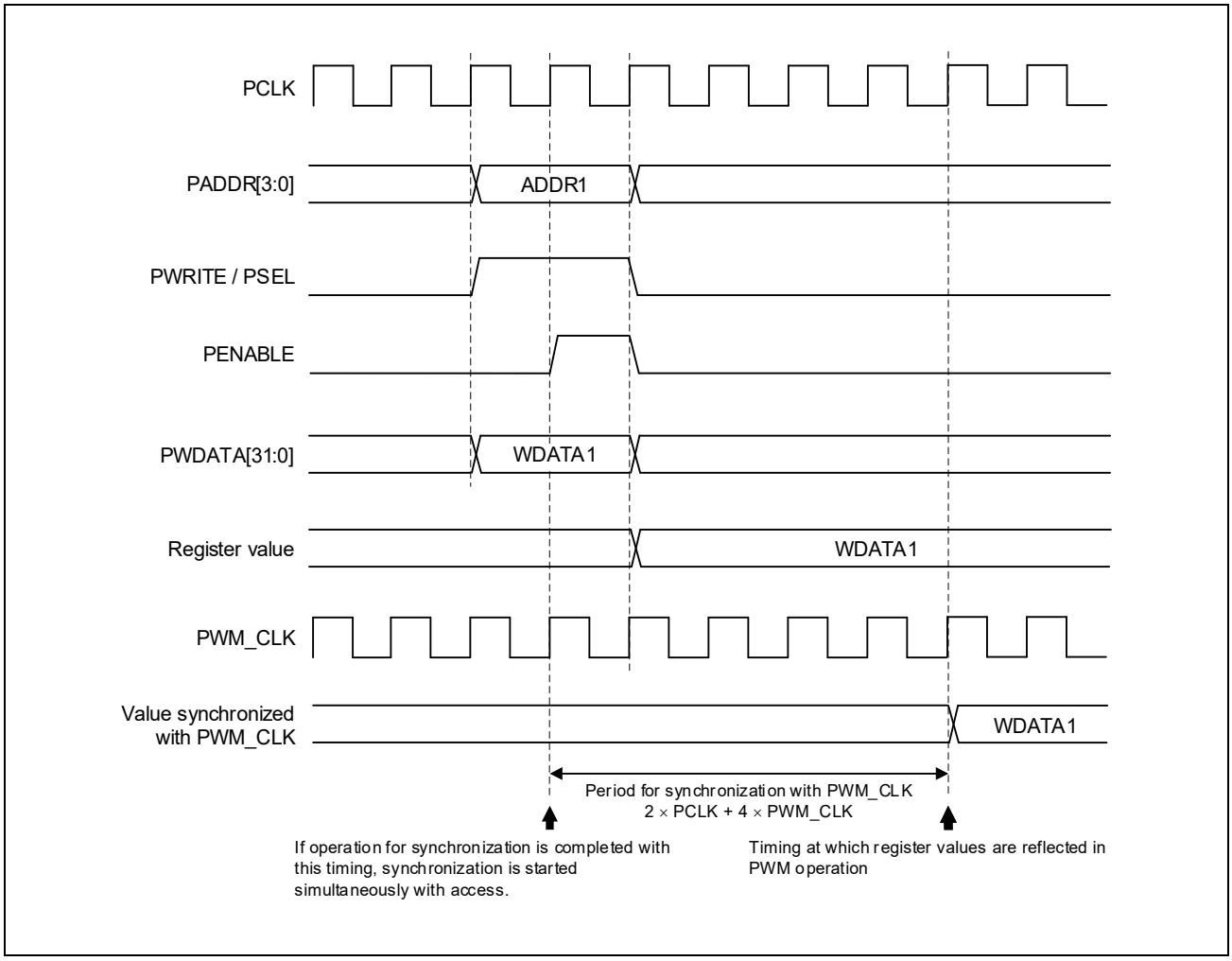


Figure 17.4-4 Timing 1 at which Register Values are Reflected in PWM Operation

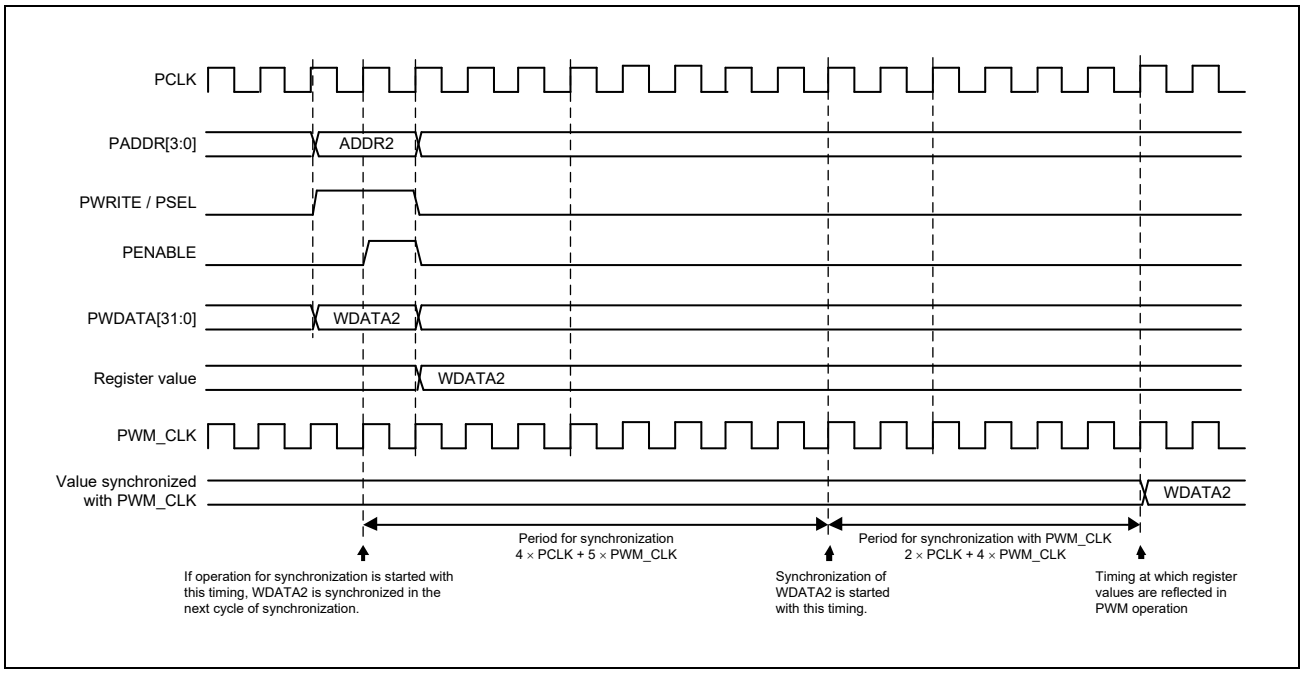


Figure 17.4-5 Timing 2 at which Register Values are Reflected in PWM Operation

17.4.5 Timing at which the PWM Operating Status Value is Reflected in a Register

The values to be stored in the PWMS bit of the PWMCTR register, in the PWMCNT register, and in the PWMINT register are stored in synchronization with PCLK. Accordingly, the interval at which the value is updated in each register is up to 5 × PWM_CLK + 5 × PCLK, and until this has elapsed the previous value may be read as the actual PWM operating status value.

17.5 Points for Caution

(1) When the setting of the PWM cycle setting register (PWMCYC) is to be changed, do so after setting the PWME bit of the PWM control register (PWMCTR) to 0 to stop counter operation. If the setting is changed during counter operation, PWM output may not proceed correctly.

(2) In the case of write access to the output level setting register for the PWM signal (the PWMHL bit of the PWMCTR register) to change its setting, the changed setting is reflected in the output level of the PWM signal at the time when the written data are synchronized with PWM_CLK, which is derived from PCLK.

Section 18 Real-Time Clock (RTC)

This section describes the functions of the real-time clock (RTC).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

18.1 Functional Overview

The RTC unit is a real-time clock module which runs with the backup power supply.

This LSI chip includes an oscillation circuit for a real-time clock (use of the RTC requires the external connection of a 32.768-kHz crystal resonator).

- The RTC has a 32-bit seconds counter and a 23-bit startup timer (seconds counter).
- The RTC has an interface with the external power supply sequence controller (PWC) so that it can be used as the startup timer.*1
- The clock function is available.

Note 1. If the external power supply sequence is controlled by the PWC, the system can be restarted after the specified time by operating the startup timer of the RTC before turning the system power supply off.

Section 19 DMA Controller (DMAC)

This section describes the functions of the DMA controller (DMAC).

19.1 Functional Overview

The DMAC controller (DMAC) is made up of DMAC0 and DMAC1 (each having eight channels).

It supports hardware activation, software activation, and link transfer with the use of descriptors. Of the two units, eight channels of DMAC1 are for use with the ISP support package, so do not use registers related to those channels.

19.1.1 Features

- The bank switching setting in SYS allows access to the address space over 4 Gbytes.
- DMA transaction setting modes

  Register mode and link mode are supported.

  - Register mode
    In this mode, DMA transfer proceeds with the use of settings from the CPU. Up to two register sets (Next0 and Next1 register sets) can be set and alternating consecutive transfer according to the respective settings can proceed.
  - Link mode
    In this mode, the settings (descriptors) are allocated to the external memory and captured by the DMAC, after which DMA transfer proceeds in accord with the values. By preparing multiple settings which specify the addresses of the descriptors to control next transfers, sequential execution of transfers is possible.
    Additionally, suspension and resumption of the next DMA transfer can be specified by the header of the descriptor.

- Triggering modes

  The following two types are supported to start DMA transfer.

  - Software activation
    DMA transfer is started by writing to an internal register.
  - Hardware activation
    DMA transfer is started according to the state of the DMAREQ input. The detection mode is selectable from those listed below. Masking is also possible.
    - Rising-edge detection
    - Falling-edge detection
    - Change-point detection
    - High-level detection
    - Low-level detection

- Interrupt

  Level and pulse interrupts are supported. In this LSI, use interrupts in level mode.

- Method of transfer

  Transfer sizes for the source and the destination are individually selectable as values from among 1 to 128 bytes. For transfer addresses, increment mode and fixed mode are supported.

- Buffer flushing

  Data already captured in the buffer can be forcibly flushed.

- Suspension

  DMA transfer in progress can be suspended.

- Interval function

  The interval between DMA transfers is specifiable to adjust the bus occupancy ratio.

19.1.2 DMA Transfer Specifications

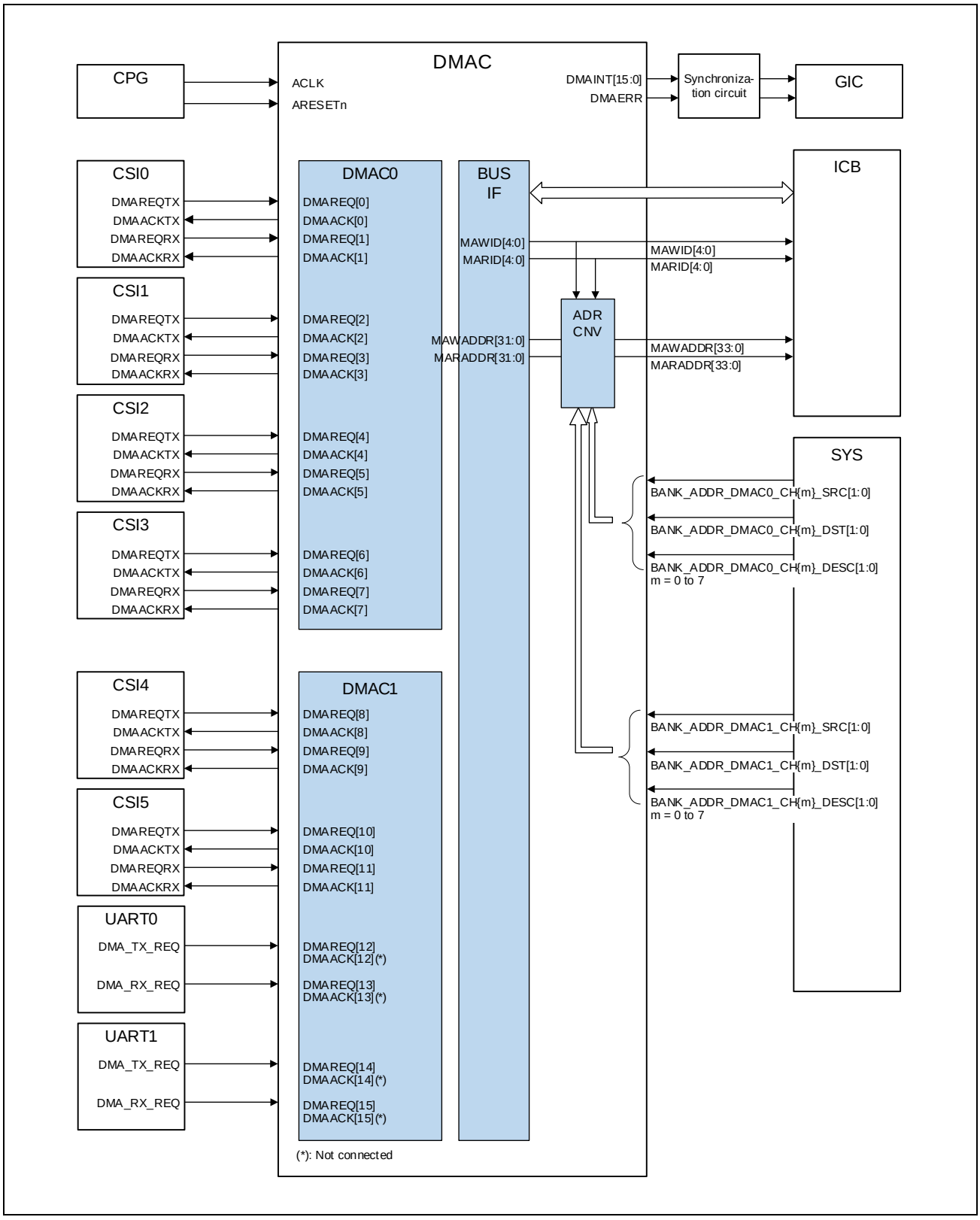
- Maximum number of bytes for DMA transfer

  Byte counting is specifiable per channel. The maximum number is $(2^{32} - 1)$ bytes = (4G − 1) bytes.

19.1.3 Restrictions

If transfer proceeds with the use of this unit in such a way that the data source and destination areas are the same or parts of these areas overlap, data consistency cannot be guaranteed. Accordingly, make settings such that the data source and destination address areas do not overlap.

19.2 Connection Configuration



(*Continuation of the previous page*)

[DMAC]

DMAC — The DMA controller is made up of two main units.

DMAC0:
DMA Controller Main Unit 0 (eight channels are included and the number of buffer stages per channel is 16).
DMA transfer control, arbitration control, DMA control registers, and DMA-dedicated interfaces are provided.

DMAC1:
DMA Controller Main Unit 1 (eight channels are included and the number of buffer stages per channel is 16).
DMA transfer control, arbitration control, DMA control registers, and DMA-dedicated interfaces are provided.

BUSIF:
Interface section with the external bus.
The AXI master address width is 32 bits and the data bus width is 64 bits.

ADRCNV —Master address conversion section

Two bank switching address bits input by SYS are appended to the higher-order bits of the master address (MARADDR[31:0], MAWADDR[31:0]) for extension to a 34-bit address (MARADDR[33:0], MAWADDR[33:0]).

Figure 19.2-1 Connection Configuration

19.3 Pin Functions

19.3.1 List of Internal Pins

Table 19.3-1 lists the internal pins of the DMAC.

Table 19.3-1 List of Internal Pins

Pin Name	I/O	Functions
DMA interfaces		
DMAREQ[15:0]	Input	DMA transfer request input * If DMAREQ is generated with the clock which is not synchronized with ACLK, use level-detection mode.
DMAACK[15:0]	Output	DMA acknowledge output * If the DMAACK signal is to be fetched with the clock which is not synchronized with ACLK, use level-output mode.
Interrupt interfaces		
DMAINT[15:0]	Output	DMA transaction completed interrupt
DMAERR	Output	Error response (ERROR) interrupt
Bank switching addresses		
BANK_ADDR_DMAC{0,1}_CH{0-7}_SRC[1:0]	Input	DMAC{0,1}, CH{0-7} bank switching address (for the source)
BANK_ADDR_DMAC{0,1}_CH{0-7}_DST[1:0]	Input	DMAC{0,1}, CH{0-7} bank switching address (for the destination)
BANK_ADDR_DMAC{0,1}_CH{0-7}_DESC[1:0]	Input	DMAC{0,1}, CH{0-7} bank switching address (for the descriptor)

19.3.1.1 DMA Interfaces

Each DMAC can be set to select one request from among eight transfer requests by software.

The DMAREQ and DMAACK signals are referred to as the DMA signals and are on pins for use in hardware activation.

Eight DMAREQ and DMAACK signals are assigned to each DMAC unit. The bit positions to be used are switchable by using the SEL field of the DMAA_DMACn_CHCFG_m register.

Table 19.3-2 lists the destinations to which the DMAREQ and DMAACK pins of the DMAC unit are connected.

Table 19.3-2 DMAREQ and DMAACK Pin Assignment

DMAC		Connect To	
DMAC Unit Name	Pin Name	Unit Name	Unit Pin Name
DMAC0	DMAREQ[0]	CSI0	DMAREQTX
	DMAACK[0]	CSI0	DMAACKTX
	DMAREQ[1]	CSI0	DMAREQRX
	DMAACK[1]	CSI0	DMAACKRX
	DMAREQ[2]	CSI1	DMAREQTX
	DMAACK[2]	CSI1	DMAACKTX
	DMAREQ[3]	CSI1	DMAREQRX
	DMAACK[3]	CSI1	DMAACKRX
	DMAREQ[4]	CSI2	DMAREQTX
	DMAACK[4]	CSI2	DMAACKTX
	DMAREQ[5]	CSI2	DMAREQRX
	DMAACK[5]	CSI2	DMAACKRX
	DMAREQ[6]	CSI3	DMAREQTX
	DMAACK[6]	CSI3	DMAACKTX
	DMAREQ[7]	CSI3	DMAREQRX
	DMAACK[7]	CSI3	DMAACKRX
DMAC1	DMAREQ[8]	CSI4	DMAREQTX
	DMAACK[8]	CSI4	DMAACKTX
	DMAREQ[9]	CSI4	DMAREQRX
	DMAACK[9]	CSI4	DMAACKRX
	DMAREQ[10]	CSI5	DMAREQTX
	DMAACK[10]	CSI5	DMAACKTX
	DMAREQ[11]	CSI5	DMAREQRX
	DMAACK[11]	CSI5	DMAACKRX
	DMAREQ[12]	UART0	DMA_TX_REQ
	DMAACK[12]	No destination for connection (the output is open)	—
	DMAREQ[13]	UART0	DMA_RX_REQ
	DMAACK[13]	No destination for connection (the output is open)	—
	DMAREQ[14]	UART1	DMA_TX_REQ
	DMAACK[14]	No destination for connection (the output is open)	—
	DMAREQ[15]	UART1	DMA_RX_REQ
	DMAACK[15]	No destination for connection (the output is open)	—

DMAREQ (Input)

This is a request input signal for DMA transfer.

Edge detection (rising-edge detection, falling-edge detection, and change-point detection) and level detection (high-level detection and low-level detection) are supported (masking requests is also possible).

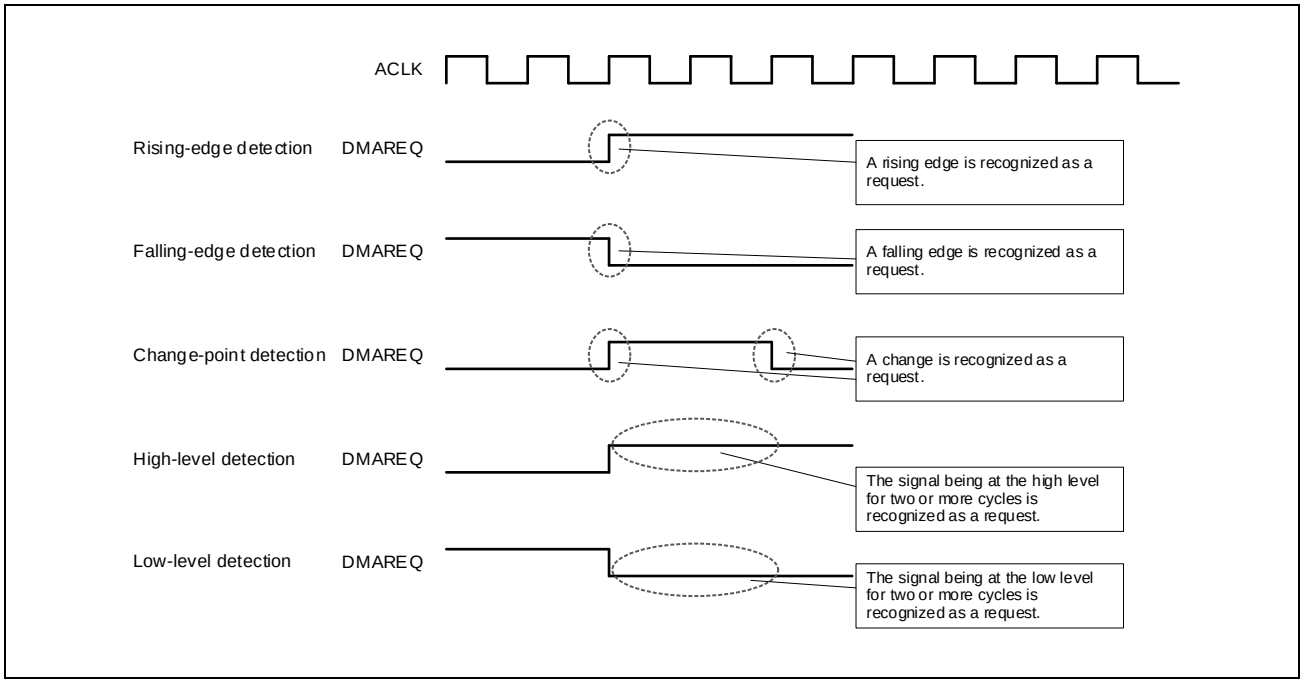


Figure 19.3-1 DMAREQ Detection Mode

DMAACK (Output)

This is an acknowledge output signal for the DMAREQ signal.

This signal is activated in response to the start of transfer corresponding to the DMAREQ signal.

It supports pulse mode, level mode, and bus cycle mode (masking the output is also possible).

If the DMAACK signal is in level mode, it remains at the high level until the DMAREQ signal is deactivated.

A next DMA request is not accepted while the DMAACK signal is at the high level. Use this signal for handshaking with the DMAREQ signal.

The figure below shows the output modes of the respective DMAACK signals and the example timing charts.

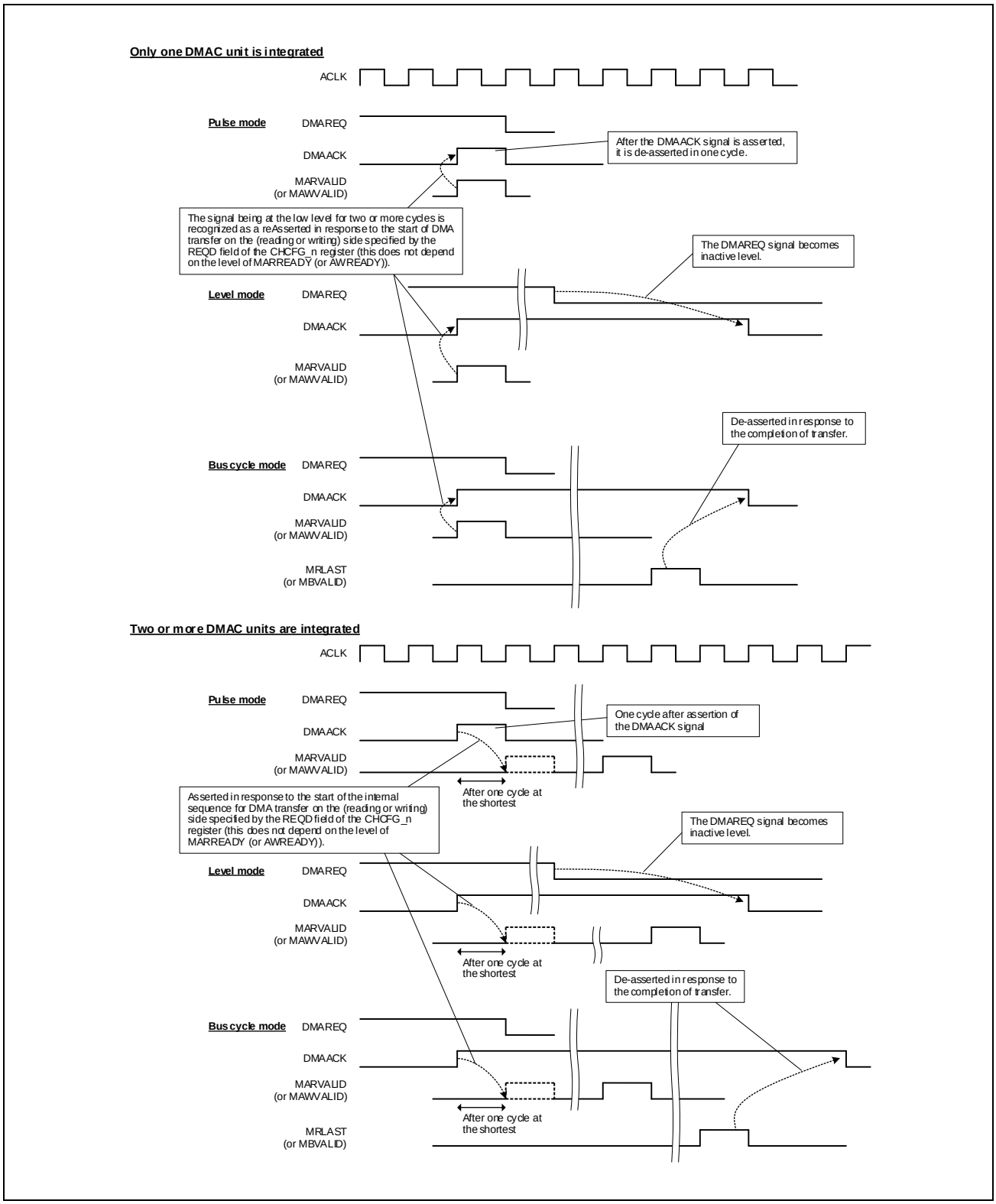


Figure 19.3-2 DMAACK Signal Output

19.3.1.2 Interrupt Interfaces

DMAINT (Output)

This is a DMA transaction completed interrupt signal. This signal is asserted on the completion of the DMA transaction. It is also asserted when an invalid descriptor is read in link mode.

The DMAINT pins correspond to the DMAEND pins of the internal DMAC. **Table 19.3-3** shows the assignment of the channels of the DMAC units to the DMAINT pins.

Table 19.3-3 DMAINT Pin Assignment

DMAINT pin	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DMAC unit	DMAC1								DMAC0							
Channel	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

DMAERR (Output)

This is an error response (ERROR) interrupt signal. This signal is asserted when an error response is returned to the transfer request issued by the master interface. This pin is one bit and is common to all channels.

The format of this interrupt output is switchable between pulse output and level output through the setting of the register. After a reset, pulse output is selected.

CAUTION

Select level output in this product.

19.3.1.3 Bank Switching Addresses

There are three bank switching addresses for the source, destination, and descriptor per DMAC number and channel number.

These pins are associated with the AXI address conversion function. For details, see **Section 19.6.3, AXI Address Conversion**.

In this product, the SYS unit controls the corresponding pin by a register.

BANK_ADDR_DMAC{0,1}_CH{0-7}_SRC[1:0] (Input)

Bank switching address for CH{0-7} of DMAC{0,1} (for the source).

BANK_ADDR_DMAC{0,1}_CH{0-7}_DST[1:0] (Input)

Bank switching address for CH{0-7} of DMAC{0,1} (for the destination).

BANK_ADDR_DMAC{0,1}_CH{0-7}_DESC[1:0] (Input)

Bank switching address for CH{0-7} of DMAC{0,1} (for the descriptor).

19.4 Address Space

Table 19.4-1 lists the allocation of the registers for DMAC0 and DMAC1.

Table 19.4-1 Address Space

Address	Group
000h	Registers for DMAC0
:	
3FCh	
400h	Registers for DMAC1
:	
7FCh	

19.5 Register Descriptions

For the register base address (<DMAA_S0_base>), see the section of Address Map.

The following lists the registers of one DMAC unit.

19.5.1 List of Registers

Table 19.5-1 lists the registers of the DMAC unit.

Table 19.5-1 List of Registers (1/7)

Offset Address	Group	Register Name	Abbreviation	Initial Value	Access Unit (bits)
DMAC0 Channel 0					
000h	Next0	Next0 Source Address Register 0	DMAA_DMAC0_N0SA_0	0000_0000h	32
004h		Next0 Destination Address Register 0	DMAA_DMAC0_N0DA_0	0000_0000h	32
008h		Next0 Transaction Byte Register 0	DMAA_DMAC0_N0TB_0	0000_0000h	32
00Ch	Next1	Next1 Source Address Register 0	DMAA_DMAC0_N1SA_0	0000_0000h	32
010h		Next1 Destination Address Resister 0	DMAA_DMAC0_N1DA_0	0000_0000h	32
014h		Next1 Transaction Byte Register 0	DMAA_DMAC0_N1TB_0	0000_0000h	32
018h	Current	Current Source Address Register 0	DMAA_DMAC0_CRSA_0	0000_0000h	32
01Ch		Current Destination Address Register 0	DMAA_DMAC0_CRDA_0	0000_0000h	32
020h		Current Transaction Byte Register 0	DMAA_DMAC0_CRTB_0	0000_0000h	32
024h	Channel	Channel Status Register 0	DMAA_DMAC0_CHSTAT_0	0000_0000h	32
028h		Channel Control Register 0	DMAA_DMAC0_CHCTRL_0	0000_0000h	32
02Ch		Channel Configuration Register 0	DMAA_DMAC0_CHCFG_0	0000_0000h	32
030h		Channel Interval Register 0	DMAA_DMAC0_CHITVL_0	0000_0000h	32
034h		Channel Extension Register 0	DMAA_DMAC0_CHEXT_0	0000_0000h	32
038h	Link	Next Link Address Resister 0	DMAA_DMAC0_NXLA_0	0000_0000h	32
03Ch		Current Link Address Resister 0	DMAA_DMAC0_CRLA_0	0000_0000h	32
DMAC0 Channel 1					
040h	Next0	Next0 Source Address Register 1	DMAA_DMAC0_N0SA_1	0000_0000h	32
044h		Next0 Destination Address Register 1	DMAA_DMAC0_N0DA_1	0000_0000h	32
048h		Next0 Transaction Byte Register 1	DMAA_DMAC0_N0TB_1	0000_0000h	32
04Ch	Next1	Next1 Source Address Register 1	DMAA_DMAC0_N1SA_1	0000_0000h	32
050h		Next1 Destination Address Register 1	DMAA_DMAC0_N1DA_1	0000_0000h	32
054h		Next1 Transaction Byte Register 1	DMAA_DMAC0_N1TB_1	0000_0000h	32
058h	Current	Current Source Address Register	DMAA_DMAC0_CRSA_1	0000_0000h	32
05Ch		Current Destination Address Register 1	DMAA_DMAC0_CRDA_1	0000_0000h	32
060h		Current Transaction Byte Register 1	DMAA_DMAC0_CRTB_1	0000_0000h	32
064h	Channel	Channel Status Register 1	DMAA_DMAC0_CHSTAT_1	0000_0000h	32
068h		Channel Control Register 1	DMAA_DMAC0_CHCTRL_1	0000_0000h	32
06Ch		Channel Configuration Register 1	DMAA_DMAC0_CHCFG_1	0000_0000h	32
070h		Channel Interval Register 1	DMAA_DMAC0_CHITVL_1	0000_0000h	32
074h		Channel Extension Register 1	DMAA_DMAC0_CHEXT_1	0000_0000h	32
078h	Link	Next Link Address Resister 1	DMAA_DMAC0_NXLA_1	0000_0000h	32
07Ch		Current Link Address Resister 1	DMAA_DMAC0_CRLA_1	0000_0000h	32

Table 19.5-1 List of Registers (2/7)

Offset Address	Group	Register Name	Abbreviation	Initial Value	Access Unit (bits)
DMAC0 Channel 2					
080h	Next0	Next0 Source Address Register 2	DMAA_DMAC0_N0SA_2	0000_0000h	32
084h		Next0 Destination Address Register 2	DMAA_DMAC0_N0DA_2	0000_0000h	32
088h		Next0 Transaction Byte Register 2	DMAA_DMAC0_N0TB_2	0000_0000h	32
08Ch	Next1	Next1 Source Address Register 2	DMAA_DMAC0_N1SA_2	0000_0000h	32
090h		Next1 Destination Address Register 2	DMAA_DMAC0_N1DA_2	0000_0000h	32
094h		Next1 Transaction Byte Register 2	DMAA_DMAC0_N1TB_2	0000_0000h	32
098h	Current	Current Source Address Register 2	DMAA_DMAC0_CRSA_2	0000_0000h	32
09Ch		Current Destination Address Register 2	DMAA_DMAC0_CRDA_2	0000_0000h	32
0A0h		Current Transaction Byte Register 2	DMAA_DMAC0_CRTB_2	0000_0000h	32
0A4h	Channel	Channel Status Register 2	DMAA_DMAC0_CHSTAT_2	0000_0000h	32
0A8h		Channel Control Register 2	DMAA_DMAC0_CHCTRL_2	0000_0000h	32
0ACh		Channel Configuration Register 2	DMAA_DMAC0_CHCFG_2	0000_0000h	32
0B0h		Channel Interval Register 2	DMAA_DMAC0_CHITVL_2	0000_0000h	32
0B4h		Channel Extension Register 2	DMAA_DMAC0_CHEXT_2	0000_0000h	32
0B8h	Link	Next Link Address Resister 2	DMAA_DMAC0_NXLA_2	0000_0000h	32
0BCh		Current Link Address Resister 2	DMAA_DMAC0_CRLA_2	0000_0000h	32
DMAC0 Channel 3					
0C0h	Next0	Next0 Source Address Register 3	DMAA_DMAC0_N0SA_3	0000_0000h	32
0C4h		Next0 Destination Address Register 3	DMAA_DMAC0_N0DA_3	0000_0000h	32
0C8h		Next0 Transaction Byte Register 3	DMAA_DMAC0_N0TB_3	0000_0000h	32
0CCh	Next1	Next1 Source Address Register 3	DMAA_DMAC0_N1SA_3	0000_0000h	32
0D0h		Next1 Destination Address Register 3	DMAA_DMAC0_N1DA_3	0000_0000h	32
0D4h		Next1 Transaction Byte Register 3	DMAA_DMAC0_N1TB_3	0000_0000h	32
0D8h	Current	Current Source Address Register 3	DMAA_DMAC0_CRSA_3	0000_0000h	32
0DCh		Current Destination Address Register 3	DMAA_DMAC0_CRDA_3	0000_0000h	32
0E0h		Current Transaction Byte Register 3	DMAA_DMAC0_CRTB_3	0000_0000h	32
0E4h	Channel	Channel Status Register 3	DMAA_DMAC0_CHSTAT_3	0000_0000h	32
0E8h		Channel Control Register 3	DMAA_DMAC0_CHCTRL_3	0000_0000h	32
0ECh		Channel Configuration Register 3	DMAA_DMAC0_CHCFG_3	0000_0000h	32
0F0h		Channel Interval Register 3	DMAA_DMAC0_CHITVL_3	0000_0000h	32
0F4h		Channel Extension Register 3	DMAA_DMAC0_CHEXT_3	0000_0000h	32
0F8h	Link	Next Link Address Resister 3	DMAA_DMAC0_NXLA_3	0000_0000h	32
0FCh		Current Link Address Resister 3	DMAA_DMAC0_CRLA_3	0000_0000h	32
DMAC0 Channel 4					
100h	Next0	Next0 Source Address Register 4	DMAA_DMAC0_N0SA_4	0000_0000h	32
104h		Next0 Destination Address Register 4	DMAA_DMAC0_N0DA_4	0000_0000h	32
108h		Next0 Transaction Byte Register 4	DMAA_DMAC0_N0TB_4	0000_0000h	32
10Ch	Next1	Next1 Source Address Register 4	DMAA_DMAC0_N1SA_4	0000_0000h	32
110h		Next1 Destination Address Register 4	DMAA_DMAC0_N1DA_4	0000_0000h	32
114h		Next1 Transaction Byte Register 4	DMAA_DMAC0_N1TB_4	0000_0000h	32
118h	Current	Current Source Address Register 4	DMAA_DMAC0_CRSA_4	0000_0000h	32
11Ch		Current Destination Address Register 4	DMAA_DMAC0_CRDA_4	0000_0000h	32
120h		Current Transaction Byte Register 4	DMAA_DMAC0_CRTB_4	0000_0000h	32

Table 19.5-1 List of Registers (3/7)

Offset Address	Group	Register Name	Abbreviation	Initial Value	Access Unit (bits)
124h	Channel	Channel Status Register 4	DMAA_DMAC0_CHSTAT_4	0000_0000h	32
128h		Channel Control Register 4	DMAA_DMAC0_CHCTRL_4	0000_0000h	32
12Ch		Channel Configuration Register 4	DMAA_DMAC0_CHCFG_4	0000_0000h	32
130h		Channel Interval Register 4	DMAA_DMAC0_CHITVL_4	0000_0000h	32
134h		Channel Extension Register 4	DMAA_DMAC0_CHEXT_4	0000_0000h	32
138h	Link	Next Link Address Resister 4	DMAA_DMAC0_NXLA_4	0000_0000h	32
13Ch		Current Link Address Resister 4	DMAA_DMAC0_CRLA_4	0000_0000h	32
DMAC0 Channel 5					
140h	Next0	Next0 Source Address Register 5	DMAA_DMAC0_N0SA_5	0000_0000h	32
144h		Next0 Destination Address Register 5	DMAA_DMAC0_N0DA_5	0000_0000h	32
148h		Next0 Transaction Byte Register 5	DMAA_DMAC0_N0TB_5	0000_0000h	32
14Ch	Next1	Next1 Source Address Register 5	DMAA_DMAC0_N1SA_5	0000_0000h	32
150h		Next1 Destination Address Register 5	DMAA_DMAC0_N1DA_5	0000_0000h	32
154h		Next1 Transaction Byte Register 5	DMAA_DMAC0_N1TB_5	0000_0000h	32
158h	Current	Current Source Address Register 5	DMAA_DMAC0_CRSA_5	0000_0000h	32
15Ch		Current Destination Address Register 5	DMAA_DMAC0_CRDA_5	0000_0000h	32
160h		Current Transaction Byte Register 5	DMAA_DMAC0_CRTB_5	0000_0000h	32
164h	Channel	Channel Status Register 5	DMAA_DMAC0_CHSTAT_5	0000_0000h	32
168h		Channel Control Register 5	DMAA_DMAC0_CHCTRL_5	0000_0000h	32
16Ch		Channel Configuration Register 5	DMAA_DMAC0_CHCFG_5	0000_0000h	32
170h		Channel Interval Register 5	DMAA_DMAC0_CHITVL_5	0000_0000h	32
174h		Channel Extension Register 5	DMAA_DMAC0_CHEXT_5	0000_0000h	32
178h	Link	Next Link Address Resister 5	DMAA_DMAC0_NXLA_5	0000_0000h	32
17Ch		Current Link Address Resister 5	DMAA_DMAC0_CRLA_5	0000_0000h	32
DMAC0 Channel 6					
180h	Next0	Next0 Source Address Register 6	DMAA_DMAC0_N0SA_6	0000_0000h	32
184h		Next0 Destination Address Register 6	DMAA_DMAC0_N0DA_6	0000_0000h	32
188h		Next0 Transaction Byte Register 6	DMAA_DMAC0_N0TB_6	0000_0000h	32
18Ch	Next1	Next1 Source Address Register 6	DMAA_DMAC0_N1SA_6	0000_0000h	32
190h		Next1 Destination Address Register 6	DMAA_DMAC0_N1DA_6	0000_0000h	32
194h		Next1 Transaction Byte Register 6	DMAA_DMAC0_N1TB_6	0000_0000h	32
198h	Current	Current Source Address Register 6	DMAA_DMAC0_CRSA_6	0000_0000h	32
19Ch		Current Destination Address Register 6	DMAA_DMAC0_CRDA_6	0000_0000h	32
1A0h		Current Transaction Byte Register 6	DMAA_DMAC0_CRTB_6	0000_0000h	32
1A4h	Channel	Channel Status Register 6	DMAA_DMAC0_CHSTAT_6	0000_0000h	32
1A8h		Channel Control Register 6	DMAA_DMAC0_CHCTRL_6	0000_0000h	32
1ACh		Channel Configuration Register 6	DMAA_DMAC0_CHCFG_6	0000_0000h	32
1B0h		Channel Interval Register 6	DMAA_DMAC0_CHITVL_6	0000_0000h	32
1B4h		Channel Extension Register 6	DMAA_DMAC0_CHEXT_6	0000_0000h	32
1B8h	Link	Next Link Address Resister 6	DMAA_DMAC0_NXLA_6	0000_0000h	32
1BCh		Current Link Address Resister 6	DMAA_DMAC0_CRLA_6	0000_0000h	32
DMAC0 Channel 7					
1C0h	Next0	Next0 Source Address Register 7	DMAA_DMAC0_N0SA_7	0000_0000h	32
1C4h		Next0 Destination Address Register 7	DMAA_DMAC0_N0DA_7	0000_0000h	32
1C8h		Next0 Transaction Byte Register 7	DMAA_DMAC0_N0TB_7	0000_0000h	32

Table 19.5-1 List of Registers (4/7)

Offset Address	Group	Register Name	Abbreviation	Initial Value	Access Unit (bits)
1CCh	Next1	Next1 Source Address Register 7	DMAA_DMAC0_N1SA_7	0000_0000h	32
1D0h		Next1 Destination Address Register 7	DMAA_DMAC0_N1DA_7	0000_0000h	32
1D4h		Next1 Transaction Byte Register 7	DMAA_DMAC0_N1TB_7	0000_0000h	32
1D8h	Current	Current Source Address Register 7	DMAA_DMAC0_CRSA_7	0000_0000h	32
1DCh		Current Destination Address Register 7	DMAA_DMAC0_CRDA_7	0000_0000h	32
1E0h		Current Transaction Byte Register 7	DMAA_DMAC0_CRTB_7	0000_0000h	32
1E4h	Channel	Channel Status Register 7	DMAA_DMAC0_CHSTAT_7	0000_0000h	32
1E8h		Channel Control Register 7	DMAA_DMAC0_CHCTRL_7	0000_0000h	32
1ECh		Channel Configuration Register 7	DMAA_DMAC0_CHCFG_7	0000_0000h	32
1F0h		Channel Interval Register 7	DMAA_DMAC0_CHITVL_7	0000_0000h	32
1F4h		Channel Extension Register 7	DMAA_DMAC0_CHEXT_7	0000_0000h	32
1F8h	Link	Next Link Address Resister 7	DMAA_DMAC0_NXLA_7	0000_0000h	32
1FCh		Current Link Address Resister 7	DMAA_DMAC0_CRLA_7	0000_0000h	32
DMAC0 Common					
200h to 2FFh		Reserved	—	—	—
300h		DMA Control Register	DMAA_DMAC0_DCTRL	0000_0000h	32
304h to 30Fh		Reserved	—	—	—
310h		DMA Status EN Register	DMAA_DMAC0_DST_EN	0000_0000h	32
314h		DMA Status ER Register	DMAA_DMAC0_DST_ER	0000_0000h	32
318h		DMA Status END Register	DMAA_DMAC0_DST_END	0000_0000h	32
31Ch		DMA Status TC Register	DMAA_DMAC0_DST_TC	0000_0000h	32
320h		DMA Status SUS Register	DMAA_DMAC0_DST_SUS	0000_0000h	32
324h to 3FFh		Undefined	—	—	—
DMAC1 Channel 0					
400h	Next0	Next0 Source Address Register 0	DMAA_DMAC1_N0SA_0	0000_0000h	32
404h		Next0 Destination Address Register 0	DMAA_DMAC1_N0DA_0	0000_0000h	32
408h		Next0 Transaction Byte Register 0	DMAA_DMAC1_N0TB_0	0000_0000h	32
40Ch	Next1	Next1 Source Address Register 0	DMAA_DMAC1_N1SA_0	0000_0000h	32
410h		Next1 Destination Address Resister 0	DMAA_DMAC1_N1DA_0	0000_0000h	32
414h		Next1 Transaction Byte Register 0	DMAA_DMAC1_N1TB_0	0000_0000h	32
418h	Current	Current Source Address Register 0	DMAA_DMAC1_CRSA_0	0000_0000h	32
41Ch		Current Destination Address Register 0	DMAA_DMAC1_CRDA_0	0000_0000h	32
420h		Current Transaction Byte Register 0	DMAA_DMAC1_CRTB_0	0000_0000h	32
424h	Channel	Channel Status Register 0	DMAA_DMAC1_CHSTAT_0	0000_0000h	32
428h		Channel Control Register 0	DMAA_DMAC1_CHCTRL_0	0000_0000h	32
42Ch		Channel Configuration Register 0	DMAA_DMAC1_CHCFG_0	0000_0000h	32
430h		Channel Interval Register 0	DMAA_DMAC1_CHITVL_0	0000_0000h	32
434h		Channel Extension Register 0	DMAA_DMAC1_CHEXT_0	0000_0000h	32
438h	Link	Next Link Address Resister 0	DMAA_DMAC1_NXLA_0	0000_0000h	32
43Ch		Current Link Address Resister 0	DMAA_DMAC1_CRLA_0	0000_0000h	32
DMAC1 Channel 1					
440h	Next0	Next0 Source Address Register 1	DMAA_DMAC1_N0SA_1	0000_0000h	32
444h		Next0 Destination Address Register 1	DMAA_DMAC1_N0DA_1	0000_0000h	32
448h		Next0 Transaction Byte Register 1	DMAA_DMAC1_N0TB_1	0000_0000h	32

Table 19.5-1 List of Registers (5/7)

Offset Address	Group	Register Name	Abbreviation	Initial Value	Access Unit (bits)
44Ch	Next1	Next1 Source Address Register 1	DMAA_DMAC1_N1SA_1	0000_0000h	32
450h		Next1 Destination Address Register 1	DMAA_DMAC1_N1DA_1	0000_0000h	32
454h		Next1 Transaction Byte Register 1	DMAA_DMAC1_N1TB_1	0000_0000h	32
458h	Current	Current Source Address Register	DMAA_DMAC1_CRSA_1	0000_0000h	32
45Ch		Current Destination Address Register 1	DMAA_DMAC1_CRDA_1	0000_0000h	32
460h		Current Transaction Byte Register 1	DMAA_DMAC1_CRTB_1	0000_0000h	32
464h	Channel	Channel Status Register 1	DMAA_DMAC1_CHSTAT_1	0000_0000h	32
468h		Channel Control Register 1	DMAA_DMAC1_CHCTRL_1	0000_0000h	32
46Ch		Channel Configuration Register 1	DMAA_DMAC1_CHCFG_1	0000_0000h	32
470h		Channel Interval Register 1	DMAA_DMAC1_CHITVL_1	0000_0000h	32
474h		Channel Extension Register 1	DMAA_DMAC1_CHEXT_1	0000_0000h	32
478h	Link	Next Link Address Resister 1	DMAA_DMAC1_NXLA_1	0000_0000h	32
47Ch		Current Link Address Resister 1	DMAA_DMAC1_CRLA_1	0000_0000h	32
DMAC1 Channel 2					
480h	Next0	Next0 Source Address Register 2	DMAA_DMAC1_N0SA_2	0000_0000h	32
484h		Next0 Destination Address Register 2	DMAA_DMAC1_N0DA_2	0000_0000h	32
488h		Next0 Transaction Byte Register 2	DMAA_DMAC1_N0TB_2	0000_0000h	32
48Ch	Next1	Next1 Source Address Register 2	DMAA_DMAC1_N1SA_2	0000_0000h	32
490h		Next1 Destination Address Register 2	DMAA_DMAC1_N1DA_2	0000_0000h	32
494h		Next1 Transaction Byte Register 2	DMAA_DMAC1_N1TB_2	0000_0000h	32
498h	Current	Current Source Address Register 2	DMAA_DMAC1_CRSA_2	0000_0000h	32
49Ch		Current Destination Address Register 2	DMAA_DMAC1_CRDA_2	0000_0000h	32
4A0h		Current Transaction Byte Register 2	DMAA_DMAC1_CRTB_2	0000_0000h	32
4A4h	Channel	Channel Status Register 2	DMAA_DMAC1_CHSTAT_2	0000_0000h	32
4A8h		Channel Control Register 2	DMAA_DMAC1_CHCTRL_2	0000_0000h	32
4ACh		Channel Configuration Register 2	DMAA_DMAC1_CHCFG_2	0000_0000h	32
4B0h		Channel Interval Register 2	DMAA_DMAC1_CHITVL_2	0000_0000h	32
4B4h		Channel Extension Register 2	DMAA_DMAC1_CHEXT_2	0000_0000h	32
4B8h	Link	Next Link Address Resister 2	DMAA_DMAC1_NXLA_2	0000_0000h	32
4BCh		Current Link Address Resister 2	DMAA_DMAC1_CRLA_2	0000_0000h	32
DMAC1 Channel 3					
4C0h	Next0	Next0 Source Address Register 3	DMAA_DMAC1_N0SA_3	0000_0000h	32
4C4h		Next0 Destination Address Register 3	DMAA_DMAC1_N0DA_3	0000_0000h	32
4C8h		Next0 Transaction Byte Register 3	DMAA_DMAC1_N0TB_3	0000_0000h	32
4CCh	Next1	Next1 Source Address Register 3	DMAA_DMAC1_N1SA_3	0000_0000h	32
4D0h		Next1 Destination Address Register 3	DMAA_DMAC1_N1DA_3	0000_0000h	32
4D4h		Next1 Transaction Byte Register 3	DMAA_DMAC1_N1TB_3	0000_0000h	32
4D8h	Current	Current Source Address Register 3	DMAA_DMAC1_CRSA_3	0000_0000h	32
4DCh		Current Destination Address Register 3	DMAA_DMAC1_CRDA_3	0000_0000h	32
4E0h		Current Transaction Byte Register 3	DMAA_DMAC1_CRTB_3	0000_0000h	32
4E4h	Channel	Channel Status Register 3	DMAA_DMAC1_CHSTAT_3	0000_0000h	32
4E8h		Channel Control Register 3	DMAA_DMAC1_CHCTRL_3	0000_0000h	32
4ECh		Channel Configuration Register 3	DMAA_DMAC1_CHCFG_3	0000_0000h	32
4F0h		Channel Interval Register 3	DMAA_DMAC1_CHITVL_3	0000_0000h	32
4F4h		Channel Extension Register 3	DMAA_DMAC1_CHEXT_3	0000_0000h	32

Table 19.5-1 List of Registers (6/7)

Offset Address	Group	Register Name	Abbreviation	Initial Value	Access Unit (bits)
4F8h	Link	Next Link Address Resister 3	DMAA_DMAC1_NXLA_3	0000_0000h	32
4FCh		Current Link Address Resister 3	DMAA_DMAC1_CRLA_3	0000_0000h	32
DMAC1 Channel 4					
500h	Next0	Next0 Source Address Register 4	DMAA_DMAC1_N0SA_4	0000_0000h	32
504h		Next0 Destination Address Register 4	DMAA_DMAC1_N0DA_4	0000_0000h	32
508h		Next0 Transaction Byte Register 4	DMAA_DMAC1_N0TB_4	0000_0000h	32
50Ch	Next1	Next1 Source Address Register 4	DMAA_DMAC1_N1SA_4	0000_0000h	32
510h		Next1 Destination Address Register 4	DMAA_DMAC1_N1DA_4	0000_0000h	32
514h		Next1 Transaction Byte Register 4	DMAA_DMAC1_N1TB_4	0000_0000h	32
518h	Current	Current Source Address Register 4	DMAA_DMAC1_CRSA_4	0000_0000h	32
51Ch		Current Destination Address Register 4	DMAA_DMAC1_CRDA_4	0000_0000h	32
520h		Current Transaction Byte Register 4	DMAA_DMAC1_CRTB_4	0000_0000h	32
524h	Channel	Channel Status Register 4	DMAA_DMAC1_CHSTAT_4	0000_0000h	32
528h		Channel Control Register 4	DMAA_DMAC1_CHCTRL_4	0000_0000h	32
52Ch		Channel Configuration Register 4	DMAA_DMAC1_CHCFG_4	0000_0000h	32
530h		Channel Interval Register 4	DMAA_DMAC1_CHITVL_4	0000_0000h	32
534h		Channel Extension Register 4	DMAA_DMAC1_CHEXT_4	0000_0000h	32
538h	Link	Next Link Address Resister 4	DMAA_DMAC1_NXLA_4	0000_0000h	32
53Ch		Current Link Address Resister 4	DMAA_DMAC1_CRLA_4	0000_0000h	32
DMAC1 Channel 5					
540h	Next0	Next0 Source Address Register 5	DMAA_DMAC1_N0SA_5	0000_0000h	32
544h		Next0 Destination Address Register 5	DMAA_DMAC1_N0DA_5	0000_0000h	32
548h		Next0 Transaction Byte Register 5	DMAA_DMAC1_N0TB_5	0000_0000h	32
54Ch	Next1	Next1 Source Address Register 5	DMAA_DMAC1_N1SA_5	0000_0000h	32
550h		Next1 Destination Address Register 5	DMAA_DMAC1_N1DA_5	0000_0000h	32
554h		Next1 Transaction Byte Register 5	DMAA_DMAC1_N1TB_5	0000_0000h	32
558h	Current	Current Source Address Register 5	DMAA_DMAC1_CRSA_5	0000_0000h	32
55Ch		Current Destination Address Register 5	DMAA_DMAC1_CRDA_5	0000_0000h	32
560h		Current Transaction Byte Register 5	DMAA_DMAC1_CRTB_5	0000_0000h	32
564h	Channel	Channel Status Register 5	DMAA_DMAC1_CHSTAT_5	0000_0000h	32
568h		Channel Control Register 5	DMAA_DMAC1_CHCTRL_5	0000_0000h	32
56Ch		Channel Configuration Register 5	DMAA_DMAC1_CHCFG_5	0000_0000h	32
570h		Channel Interval Register 5	DMAA_DMAC1_CHITVL_5	0000_0000h	32
574h		Channel Extension Register 5	DMAA_DMAC1_CHEXT_5	0000_0000h	32
578h	Link	Next Link Address Resister 5	DMAA_DMAC1_NXLA_5	0000_0000h	32
57Ch		Current Link Address Resister 5	DMAA_DMAC1_CRLA_5	0000_0000h	32
DMAC1 Channel 6					
580h	Next0	Next0 Source Address Register 6	DMAA_DMAC1_N0SA_6	0000_0000h	32
584h		Next0 Destination Address Register 6	DMAA_DMAC1_N0DA_6	0000_0000h	32
588h		Next0 Transaction Byte Register 6	DMAA_DMAC1_N0TB_6	0000_0000h	32
58Ch	Next1	Next1 Source Address Register 6	DMAA_DMAC1_N1SA_6	0000_0000h	32
590h		Next1 Destination Address Register 6	DMAA_DMAC1_N1DA_6	0000_0000h	32
594h		Next1 Transaction Byte Register 6	DMAA_DMAC1_N1TB_6	0000_0000h	32

Table 19.5-1 List of Registers (7/7)

Offset Address	Group	Register Name	Abbreviation	Initial Value	Access Unit (bits)
598h	Current	Current Source Address Register 6	DMAA_DMAC1_CRSA_6	0000_0000h	32
59Ch		Current Destination Address Register 6	DMAA_DMAC1_CRDA_6	0000_0000h	32
5A0h		Current Transaction Byte Register 6	DMAA_DMAC1_CRTB_6	0000_0000h	32
5A4h	Channel	Channel Status Register 6	DMAA_DMAC1_CHSTAT_6	0000_0000h	32
5A8h		Channel Control Register 6	DMAA_DMAC1_CHCTRL_6	0000_0000h	32
5ACh		Channel Configuration Register 6	DMAA_DMAC1_CHCFG_6	0000_0000h	32
5B0h		Channel Interval Register 6	DMAA_DMAC1_CHITVL_6	0000_0000h	32
5B4h		Channel Extension Register 6	DMAA_DMAC1_CHEXT_6	0000_0000h	32
5B8h	Link	Next Link Address Resister 6	DMAA_DMAC1_NXLA_6	0000_0000h	32
5BCh		Current Link Address Resister 6	DMAA_DMAC1_CRLA_6	0000_0000h	32
DMAC1 Channel 7					
5C0h	Next0	Next0 Source Address Register 7	DMAA_DMAC1_N0SA_7	0000_0000h	32
5C4h		Next0 Destination Address Register 7	DMAA_DMAC1_N0DA_7	0000_0000h	32
5C8h		Next0 Transaction Byte Register 7	DMAA_DMAC1_N0TB_7	0000_0000h	32
5CCh	Next1	Next1 Source Address Register 7	DMAA_DMAC1_N1SA_7	0000_0000h	32
5D0h		Next1 Destination Address Register 7	DMAA_DMAC1_N1DA_7	0000_0000h	32
5D4h		Next1 Transaction Byte Register 7	DMAA_DMAC1_N1TB_7	0000_0000h	32
5D8h	Current	Current Source Address Register 7	DMAA_DMAC1_CRSA_7	0000_0000h	32
5DCh		Current Destination Address Register 7	DMAA_DMAC1_CRDA_7	0000_0000h	32
5E0h		Current Transaction Byte Register 7	DMAA_DMAC1_CRTB_7	0000_0000h	32
5E4h	Channel	Channel Status Register 7	DMAA_DMAC1_CHSTAT_7	0000_0000h	32
5E8h		Channel Control Register 7	DMAA_DMAC1_CHCTRL_7	0000_0000h	32
5ECh		Channel Configuration Register 7	DMAA_DMAC1_CHCFG_7	0000_0000h	32
5F0h		Channel Interval Register 7	DMAA_DMAC1_CHITVL_7	0000_0000h	32
5F4h		Channel Extension Register 7	DMAA_DMAC1_CHEXT_7	0000_0000h	32
5F8h	Link	Next Link Address Resister 7	DMAA_DMAC1_NXLA_7	0000_0000h	32
5FCh		Current Link Address Resister 7	DMAA_DMAC1_CRLA_7	0000_0000h	32
DMAC1 Common					
600h to 6FFh		Reserved	—	—	—
700h		DMA Control Register	DMAA_DMAC1_DCTRL	0000_0000h	32
704h to 70Fh		Reserved	—	—	—
710h		DMA Status EN Register	DMAA_DMAC1_DST_EN	0000_0000h	32
714h		DMA Status ER Register	DMAA_DMAC1_DST_ER	0000_0000h	32
718h		DMA Status END Register	DMAA_DMAC1_DST_END	0000_0000h	32
71Ch		DMA Status TC Register	DMAA_DMAC1_DST_TC	0000_0000h	32
720h		DMA Status SUS Register	DMAA_DMAC1_DST_SUS	0000_0000h	32
724h to 7FFh		Undefined	—	—	—

CAUTION

1. If the reserved area is accessed, an OK response is returned. The initial value and the read/write attribute of this area may be changed by the functional extension in the future. Do not write the code which expects that the value read from this area is 0b by software. When writing to it, write 0b.
2. If the undefined area is accessed, an error response is returned. The control registers will not be changed.
3. Do not modify the registers by software while DMA transfer is in progress (EN = 1b), with the exception of the following registers.
   - Register set on the side that has not transferred data in register mode
   - DMAA_DMACn_CHCTRL_m

19.5.2 Register Descriptions

The functional description of each register is given below.

The prefix (DMAA_DMACn_) of the register names is omitted in the register descriptions and the field descriptions in this section.

The figure below shows the register configuration.

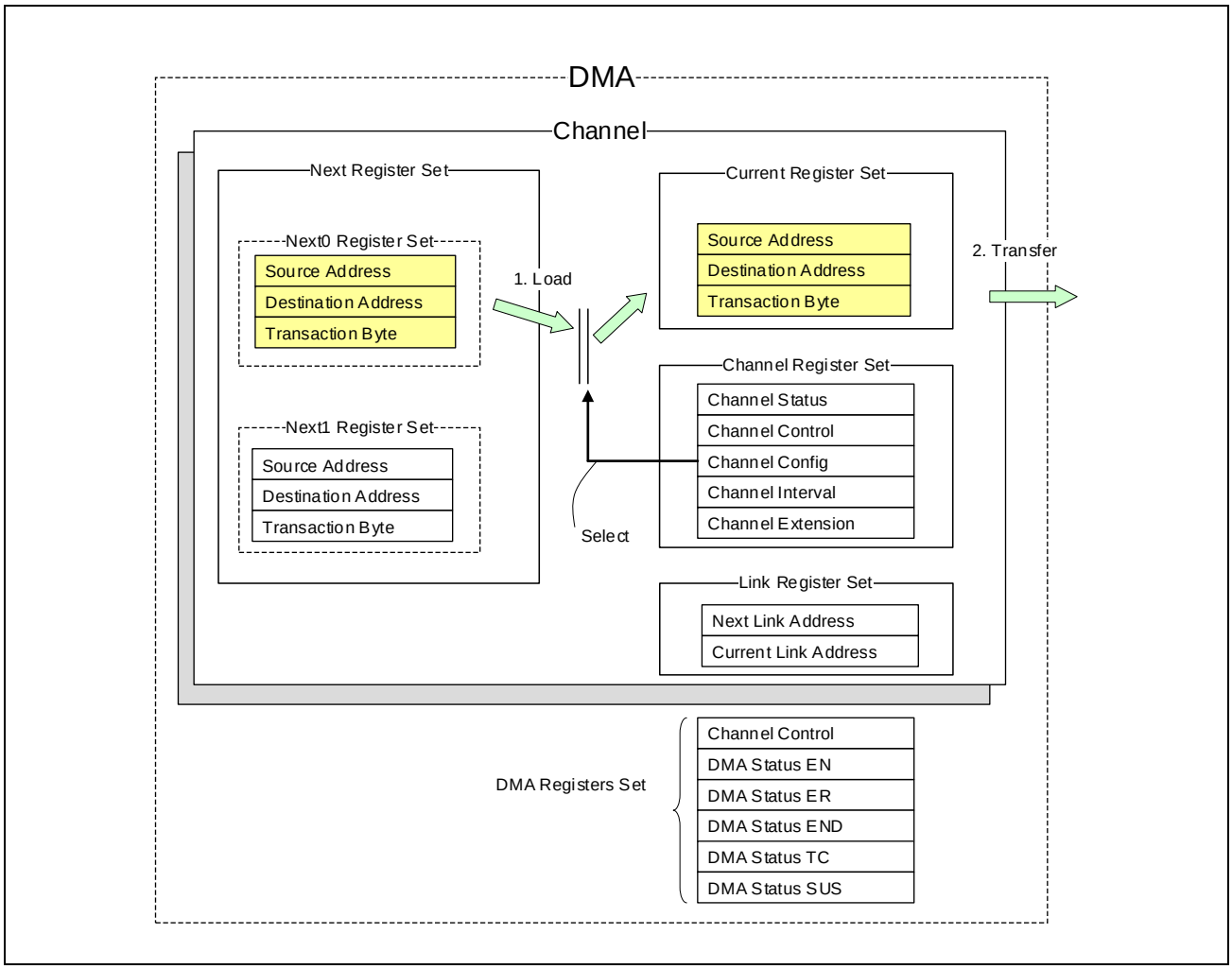


Figure 19.5-1 Register Configuration

Next Register Set

This register set sets the transfer source address, transfer destination address, and number of bytes to be transferred in the next DMA transaction to be executed.

It is composed of the Next0 and Next1 register sets.
In register mode, it is set by software. In link mode, the descriptor read data are automatically set in the Next0 register set.

The values of these register sets are loaded to the current register set and used for DMA transfer.

Current Register Set

This register set indicates the transfer source address, transfer destination address, and number of bytes being transferred in the DMA transaction that is currently in progress.

It is loaded from the Next0/1 register set (in register mode) or the descriptor read data (in link mode). It cannot be directly written by the user.

It is automatically updated every time the DMA transaction is executed.

Channel Register Set

This register set is used to make settings for DMA transfer.

It indicates the channel state, controls the channels, sets up DMA transactions, sets the interval between DMA transactions, and so on.

Link Register Set

This register set is composed of a register for setting the next descriptor address to be loaded (Next Link Address Register) and a register that indicates the descriptor address currently being executed (Current Link Address Register).

The Current Link Address Register is automatically updated by reading the descriptor and cannot be directly written by the user.

DMA Register Set

This register set is composed of a register that controls the entire DMAC and a register that indicates the state of the given channel. It is used to control the priority of channels, check the state of EN, ER, END, TCO, and SUS of the given channel, and so on.

19.5.2.1 Next0 Source Address Register m (DMAA_DMACn_N0SA_m) (n = 1, 0, m = 7 to 0)

This register sets the DMA transfer source address (32 bits) of the DMAC channel m.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0000h (n = 0, m = 0)
<DMAA_S0_base> + 0040h (n = 0, m = 1)
<DMAA_S0_base> + 0080h (n = 0, m = 2)
<DMAA_S0_base> + 00C0h (n = 0, m = 3)
<DMAA_S0_base> + 0100h (n = 0, m = 4)
<DMAA_S0_base> + 0140h (n = 0, m = 5)
<DMAA_S0_base> + 0180h (n = 0, m = 6)
<DMAA_S0_base> + 01C0h (n = 0, m = 7)
<DMAA_S0_base> + 0400h (n = 1, m = 0)
<DMAA_S0_base> + 0440h (n = 1, m = 1)
<DMAA_S0_base> + 0480h (n = 1, m = 2)
<DMAA_S0_base> + 04C0h (n = 1, m = 3)
<DMAA_S0_base> + 0500h (n = 1, m = 4)
<DMAA_S0_base> + 0540h (n = 1, m = 5)
<DMAA_S0_base> + 0580h (n = 1, m = 6)
<DMAA_S0_base> + 05C0h (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SA[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 19.5-2 DMAA_DMACn_N0SA_m Register Contents

Bit Position	Bit Name	Description
31 to 0	SA[31:0]	Source Address Sets the start address of the DMA transfer source.

19.5.2.2 Next0 Destination Address Register m (DMAA_DMACn_N0DA_m) (n = 1, 0, m = 7 to 0)

This register sets the DMA transfer destination address (32 bits) of the DMAC channel m.

Access Size: 32 bits

Address(es):
<DMAA_S0_base> + 0004h (n = 0, m = 0)
<DMAA_S0_base> + 0044h (n = 0, m = 1)
<DMAA_S0_base> + 0084h (n = 0, m = 2)
<DMAA_S0_base> + 00C4h (n = 0, m = 3)
<DMAA_S0_base> + 0104h (n = 0, m = 4)
<DMAA_S0_base> + 0144h (n = 0, m = 5)
<DMAA_S0_base> + 0184h (n = 0, m = 6)
<DMAA_S0_base> + 01C4h (n = 0, m = 7)
<DMAA_S0_base> + 0404h (n = 1, m = 0)
<DMAA_S0_base> + 0444h (n = 1, m = 1)
<DMAA_S0_base> + 0484h (n = 1, m = 2)
<DMAA_S0_base> + 04C4h (n = 1, m = 3)
<DMAA_S0_base> + 0504h (n = 1, m = 4)
<DMAA_S0_base> + 0544h (n = 1, m = 5)
<DMAA_S0_base> + 0584h (n = 1, m = 6)
<DMAA_S0_base> + 05C4h (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DA[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DA[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 19.5-3 DMAA_DMACn_N0DA_m Register Contents

Bit Position	Bit Name	Description
31 to 0	DA[31:0]	Destination Address Sets the start address of the DMA transfer destination.

19.5.2.3 Next0 Transaction Byte Register m (DMAA_DMACn_N0TB_m) (n = 1, 0, m = 7 to 0)

This register sets the total number of bytes transferred to the DMA channel m.

Access Size: 32 bits

Address(es):
<DMAA_S0_base> + 0008h (n = 0, m = 0)
<DMAA_S0_base> + 0048h (n = 0, m = 1)
<DMAA_S0_base> + 0088h (n = 0, m = 2)
<DMAA_S0_base> + 00C8h (n = 0, m = 3)
<DMAA_S0_base> + 0108h (n = 0, m = 4)
<DMAA_S0_base> + 0148h (n = 0, m = 5)
<DMAA_S0_base> + 0188h (n = 0, m = 6)
<DMAA_S0_base> + 01C8h (n = 0, m = 7)
<DMAA_S0_base> + 0408h (n = 1, m = 0)
<DMAA_S0_base> + 0448h (n = 1, m = 1)
<DMAA_S0_base> + 0488h (n = 1, m = 2)
<DMAA_S0_base> + 04C8h (n = 1, m = 3)
<DMAA_S0_base> + 0508h (n = 1, m = 4)
<DMAA_S0_base> + 0548h (n = 1, m = 5)
<DMAA_S0_base> + 0588h (n = 1, m = 6)
<DMAA_S0_base> + 05C8h (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TB[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TB[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 19.5-4 DMAA_DMACn_N0TB_m Register Contents

Bit Position	Bit Name	Description
31 to 0	TB[31:0]	Transaction Byte Sets the total number of transfer bytes. *Note*: Sets a non-zero value when starting a DMA transaction.

19.5.2.4 Next1 Source Address Register m (DMAA_DMACn_N1SA_m) (n = 1, 0, m = 7 to 0)

This register sets the DMA transfer source address (32 bits) of the DMAC channel m.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 000Ch (n = 0, m = 0)
<DMAA_S0_base> + 004Ch (n = 0, m = 1)
<DMAA_S0_base> + 008Ch (n = 0, m = 2)
<DMAA_S0_base> + 00CCh (n = 0, m = 3)
<DMAA_S0_base> + 010Ch (n = 0, m = 4)
<DMAA_S0_base> + 014Ch (n = 0, m = 5)
<DMAA_S0_base> + 018Ch (n = 0, m = 6)
<DMAA_S0_base> + 01CCh (n = 0, m = 7)
<DMAA_S0_base> + 040Ch (n = 1, m = 0)
<DMAA_S0_base> + 044Ch (n = 1, m = 1)
<DMAA_S0_base> + 048Ch (n = 1, m = 2)
<DMAA_S0_base> + 04CCh (n = 1, m = 3)
<DMAA_S0_base> + 050Ch (n = 1, m = 4)
<DMAA_S0_base> + 054Ch (n = 1, m = 5)
<DMAA_S0_base> + 058Ch (n = 1, m = 6)
<DMAA_S0_base> + 05CCh (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SA[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SA[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 19.5-5 DMAA_DMACn_N1SA_m Register Contents

Bit Position	Bit Name	Description
31 to 0	SA[31:0]	Source Address Sets the start address of the DMA transfer source.

19.5.2.5 Next1 Destination Address Register m (DMAA_DMACn_N1DA_m) (n = 1, 0, m = 7 to 0)

This register sets the DMA transfer destination address (32 bits) of the DMA channel m.

Access Size: 32 bits

Address(es):
<DMAA_S0_base> + 0010h (n = 0, m = 0)
<DMAA_S0_base> + 0050h (n = 0, m = 1)
<DMAA_S0_base> + 0090h (n = 0, m = 2)
<DMAA_S0_base> + 00D0h (n = 0, m = 3)
<DMAA_S0_base> + 0110h (n = 0, m = 4)
<DMAA_S0_base> + 0150h (n = 0, m = 5)
<DMAA_S0_base> + 0190h (n = 0, m = 6)
<DMAA_S0_base> + 01D0h (n = 0, m = 7)
<DMAA_S0_base> + 0410h (n = 1, m = 0)
<DMAA_S0_base> + 0450h (n = 1, m = 1)
<DMAA_S0_base> + 0490h (n = 1, m = 2)
<DMAA_S0_base> + 04D0h (n = 1, m = 3)
<DMAA_S0_base> + 0510h (n = 1, m = 4)
<DMAA_S0_base> + 0550h (n = 1, m = 5)
<DMAA_S0_base> + 0590h (n = 1, m = 6)
<DMAA_S0_base> + 05D0h (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DA[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DA[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 19.5-6 DMAA_DMACn_N1DA_m Register Contents

Bit Position	Bit Name	Description
31 to 0	DA[31:0]	Destination Address Sets the start address of the DMA transfer destination.

19.5.2.6 Next1 Transaction Byte Register m (DMAA_DMACn_N1TB_m) (n = 1, 0, m = 7 to 0)

This register sets the total number of bytes transferred to the DMA channel m.

Access Size: 32 bits

Address(es):
<DMAA_S0_base> + 0014h (n = 0, m = 0)
<DMAA_S0_base> + 0054h (n = 0, m = 1)
<DMAA_S0_base> + 0094h (n = 0, m = 2)
<DMAA_S0_base> + 00D4h (n = 0, m = 3)
<DMAA_S0_base> + 0114h (n = 0, m = 4)
<DMAA_S0_base> + 0154h (n = 0, m = 5)
<DMAA_S0_base> + 0194h (n = 0, m = 6)
<DMAA_S0_base> + 01D4h (n = 0, m = 7)
<DMAA_S0_base> + 0414h (n = 1, m = 0)
<DMAA_S0_base> + 0454h (n = 1, m = 1)
<DMAA_S0_base> + 0494h (n = 1, m = 2)
<DMAA_S0_base> + 04D4h (n = 1, m = 3)
<DMAA_S0_base> + 0514h (n = 1, m = 4)
<DMAA_S0_base> + 0554h (n = 1, m = 5)
<DMAA_S0_base> + 0594h (n = 1, m = 6)
<DMAA_S0_base> + 05D4h (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TB[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TB[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 19.5-7 DMAA_DMACn_N1TB_m Register Contents

Bit Position	Bit Name	Description
31 to 0	TB[31:0]	Transaction Byte Sets the total number of transfer bytes. *Note*: Set a non-zero value when starting a DMA transaction.

19.5.2.7 Current Source Address Register m (DMAA_DMACn_CRSA_m) (n = 1, 0, m = 7 to 0)

This register displays the DMA transfer source address of DMAC channel m.

Note: Indicates the Next 0/1 register value in register mode and the descriptor value in link mode. Cannot be written by software.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0018h (n = 0, m = 0)
<DMAA_S0_base> + 0058h (n = 0, m = 1)
<DMAA_S0_base> + 0098h (n = 0, m = 2)
<DMAA_S0_base> + 00D8h (n = 0, m = 3)
<DMAA_S0_base> + 0118h (n = 0, m = 4)
<DMAA_S0_base> + 0158h (n = 0, m = 5)
<DMAA_S0_base> + 0198h (n = 0, m = 6)
<DMAA_S0_base> + 01D8h (n = 0, m = 7)
<DMAA_S0_base> + 0418h (n = 1, m = 0)
<DMAA_S0_base> + 0458h (n = 1, m = 1)
<DMAA_S0_base> + 0498h (n = 1, m = 2)
<DMAA_S0_base> + 04D8h (n = 1, m = 3)
<DMAA_S0_base> + 0518h (n = 1, m = 4)
<DMAA_S0_base> + 0558h (n = 1, m = 5)
<DMAA_S0_base> + 0598h (n = 1, m = 6)
<DMAA_S0_base> + 05D8h (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CRSA[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CRSA[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 19.5-8 DMAA_DMACn_CRSA_m Register Contents

Bit Position	Bit Name	Description
31 to 0	CRSA[31:0]	Current Source Address Register Indicates the read address of the next DMA transaction. During a DMA transaction, increment is performed automatically. (Fixed when CHCFG_m.SAD = 1b.) The initial value is loaded from the following register. • Register mode: Load source address from Next 0/1. • Link mode: Load source address from the descriptor. Increment is performed at the start of read transfer. Read this register after the DMAC stops (CHSTAT_m.EN = 0b). (Treat the value during DMA operation as a reference value.)

19.5.2.8 Current Destination Address Register m (DMAA_DMACn_CRDA_m) (n = 1, 0, m = 7 to 0)

This register displays the DMA transfer destination address of DMAC channel m.

Note: Indicates the Next 0/1 register value in register mode and the descriptor value in link mode. Cannot be written by software.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 001Ch (n = 0, m = 0)
<DMAA_S0_base> + 005Ch (n = 0, m = 1)
<DMAA_S0_base> + 009Ch (n = 0, m = 2)
<DMAA_S0_base> + 00DCh (n = 0, m = 3)
<DMAA_S0_base> + 011Ch (n = 0, m = 4)
<DMAA_S0_base> + 015Ch (n = 0, m = 5)
<DMAA_S0_base> + 019Ch (n = 0, m = 6)
<DMAA_S0_base> + 01DCh (n = 0, m = 7)
<DMAA_S0_base> + 041Ch (n = 1, m = 0)
<DMAA_S0_base> + 045Ch (n = 1, m = 1)
<DMAA_S0_base> + 049Ch (n = 1, m = 2)
<DMAA_S0_base> + 04DCh (n = 1, m = 3)
<DMAA_S0_base> + 051Ch (n = 1, m = 4)
<DMAA_S0_base> + 055Ch (n = 1, m = 5)
<DMAA_S0_base> + 059Ch (n = 1, m = 6)
<DMAA_S0_base> + 05DCh (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CRDA[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CRDA[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 19.5-9 DMAA_DMACn_CRDA_m Register Contents

Bit Position	Bit Name	Description
31 to 0	CRDA[31:0]	Current Destination Address Register Indicates the write address of the next DMA transaction. During a DMA transaction, increment is performed automatically.(Fixed when CHCFG_m.DAD = 1b.) The initial value is loaded from the following register. • Register mode: Load forwarding destination address from Next 0/1. • Link mode: Load forwarding destination address from the descriptor. Increment is performed at the start of write transfer. Read this register after the DMAC stops (CHSTAT_m.EN = 0b). (Teat the value during DMA operation as a reference value.)

19.5.2.9 Current Transaction Byte Register m (DMAA_DMACn_CRTB_m) (n = 1, 0, m = 7 to 0)

This register displays the total number of bytes transferred for DMAC channel m.

Note: Indicates the Next 0/1 register value in register mode and the descriptor value in link mode. Cannot be written by software.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0020h (n = 0, m = 0)
<DMAA_S0_base> + 0060h (n = 0, m = 1)
<DMAA_S0_base> + 00A0h (n = 0, m = 2)
<DMAA_S0_base> + 00E0h (n = 0, m = 3)
<DMAA_S0_base> + 0120h (n = 0, m = 4)
<DMAA_S0_base> + 0160h (n = 0, m = 5)
<DMAA_S0_base> + 01A0h (n = 0, m = 6)
<DMAA_S0_base> + 01E0h (n = 0, m = 7)
<DMAA_S0_base> + 0420h (n = 1, m = 0)
<DMAA_S0_base> + 0460h (n = 1, m = 1)
<DMAA_S0_base> + 04A0h (n = 1, m = 2)
<DMAA_S0_base> + 04E0h (n = 1, m = 3)
<DMAA_S0_base> + 0520h (n = 1, m = 4)
<DMAA_S0_base> + 0560h (n = 1, m = 5)
<DMAA_S0_base> + 05A0h (n = 1, m = 6)
<DMAA_S0_base> + 05E0h (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CRTB[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CRTB[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 19.5-10 DMAA_DMACn_CRTB_m Register Contents

Bit Position	Bit Name	Description
31 to 0	CRTB[31:0]	Current Transaction Byte Register Indicates the number of bytes remaining in the current DMA transaction. During a DMA transaction, it is automatically decremented. The initial value is loaded from the following register. • Register mode: Load transfer byte count from Next 0/1 • Link mode: Loads transfer byte from the descriptor. Decrements when write transfer is completed. Read this register after the DMAC stops (CHSTAT_m.EN = 0b). (Treat the value during DMA operation as a reference value.)

19.5.2.10 Channel Status Register m (DMAA_DMACn_CHSTAT_m) (n = 1, 0, m = 7 to 0)

This register indicates the status of DMAC channel m.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0024h (n = 0, m = 0)
<DMAA_S0_base> + 0064h (n = 0, m = 1)
<DMAA_S0_base> + 00A4h (n = 0, m = 2)
<DMAA_S0_base> + 00E4h (n = 0, m = 3)
<DMAA_S0_base> + 0124h (n = 0, m = 4)
<DMAA_S0_base> + 0164h (n = 0, m = 5)
<DMAA_S0_base> + 01A4h (n = 0, m = 6)
<DMAA_S0_base> + 01E4h (n = 0, m = 7)
<DMAA_S0_base> + 0424h (n = 1, m = 0)
<DMAA_S0_base> + 0464h (n = 1, m = 1)
<DMAA_S0_base> + 04A4h (n = 1, m = 2)
<DMAA_S0_base> + 04E4h (n = 1, m = 3)
<DMAA_S0_base> + 0524h (n = 1, m = 4)
<DMAA_S0_base> + 0564h (n = 1, m = 5)
<DMAA_S0_base> + 05A4h (n = 1, m = 6)
<DMAA_S0_base> + 05E4h (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INTMSK
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	MODE	DER	DW	DL	SR	TC	END	ER	SUS	TACT	RQST	EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 19.5-11 DMAA_DMACn_CHSTAT_m Register Contents (1/4)

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b.
16	INTMSK	Displays the temporary mask status of DMAENDm interrupt pin output. 1b: Temporary mask state 0b: Temporary mask release state • Setting condition: When SETINTMSK is set 1b. • Clear condition: When CLRINTMSK or SWRST is set to 1b.
15 to 12	—	Reserved. These bits are read as 0b.
11	MODE	DMA Mode Indicates the DMA mode. Displays the setting value of the DMS bit in the CHCFG_m register. 0b: Register mode 1b: Link mode

Table 19.5-11 DMAA_DMACn_CHSTAT_m Register Contents (2/4)

Bit Position	Bit Name	Description
10	DER	Descriptor Error Indicates that the read register was invalid (LV = 0b). (It does not depend on the DIM level of the CHCFG_m register.) 0b: Descriptor Error has not occurred 1b: Descriptor Error has occurred • Set condition: Link mode descriptor load LV is 0b. • Clear condition: When SWRST is set to 1b.
9	DW	Descriptor Write-back Indicates descriptor write-back status. If a bus error is received during descriptor write-back, 1b is retained. 0b: Header in link mode is not written back. 1b: (ER = 0b) Link mode header is being written back. (ER = 1b) A bus error occurred while writing back the link mode header. • Set condition: At start of write-back of header in link mode. • Clear condition: Header write-back in link mode ends with an OK response. Or set 1b SWRST (CHCTRL_m).
8	DL	Descriptor Load Indicates that the descriptor is loaded. If a bus error is received during descriptor loading, 1b is held. 0b: No descriptor is loaded. 1b: (ER = 0b) Link mode descriptor is being loaded (ER = 1b) Bus error occurred while loading descriptor in link mode. • Set condition: At the start of descriptor loading in link mode. • Clear condition: Descriptor load in link mode ends with OK response. Or set 1b SWRST (CHCTRL_m).
7	SR	Selected Register Set Indicates the selected register set in register mode. 0b: Next0 Register Set 1b: Next1 Register Set • Setting condition: When RSEL is set to 1b. • Clear condition: When RSEL is set to 0b.
6	TC	Terminal Count Status bit indicates that the DMAC transaction is completed. It is set only when TCM = 0b in the CHCFG_m register. 0b: DMA transfer is incomplete 1b: DMA transfer is complete • Set conditions: – When transfer for the total number of transfer bytes set in the CRTB register is completed in register mode. – When transfer of the total number of transfer bytes set in the CRTB register is completed with WBD = 1b in the header of the descriptor in link mode. – Descriptor write-back ends with WBD = 0b in descriptor header in link mode. • Clear conditions: – CLRTC (CHCTRL_m) is set to 1b. – SWRST (CHCTRL_m) is set to 1b.

Table 19.5-11 DMAA_DMACn_CHSTAT_m Register Contents (3/4)

Bit Position	Bit Name	Description
5	END	DMAEND Interrupted This bit indicates that a DMA transaction has been completed and a DMAEND interrupt has occurred. 0b: DMA transfer is incomplete 1b: DMA transfer is complete • Set conditions: – When TC bit is set and DEM = 0b of CHCFG_m register – When LV = 0b of header and DIM = 0b at descriptor READ in link mode • Clear conditions: – CLREND (CHCTRL_m) is set to 1b. – SWRST (CHCTRL_m) is set to 1b.
4	ER	Error Bit Indicates that a DMAERR interrupt has been generated in response to an ERROR response during DMA transfer. 0b: ERROR response not received 1b: ERROR response received • Set condition: When an error response is received in the bus cycle • Clear condition: SWRST (CHCTRL_m) is set to 1b.
3	SUS	Suspend This bit indicates that the channel is paused. 0b: Channel_m is not paused 1b: Channel_m is paused • Set condition: SETSUS is set 1b during DMA transfer of Channel_m, and the internal status becomes SUSPEND. • Clear conditions: CLRSUS is set to 1b. CLREN is set to 1b.
2	TACT	Transaction Active This bit indicates that the DMAC is operating. This bit is used to confirm that the channel is completely stopped. 0b: Channel_m DMAC is stopped 1b: Channel_m DMAC is operating • Set condition: At the start of DMA transaction of Channel_m. • Clear condition: When DMA transaction is completed.

Table 19.5-11 DMAA_DMACn_CHSTAT_m Register Contents (4/4)

Bit Position	Bit Name	Description
1	RQST	Request This bit indicates that a transfer request is accepted. 0b: DMA transfer request is not received. 1b: DMA transfer request is received. • Set conditions: – Set STG-bit to 1b. – When a transfer request is accepted from the DMAREQ pin set by the CHCFG_m register. • Clear conditions: – SWRST (CHCTRL_m) is set to 1b. – CLRRQ (CHCTRL_m) is set to 1b. – When executing transfer on the side specified by REQD in single transfer (TM = 0b) mode – When all DMA transactions are completed in register mode (Transaction completed with REN = 0b). – When DMA transfer of the last descriptor (LE = 1b) is completed in link mode. – When stopped in descriptor mode (LV = 0b) in link mode – When the DMA transaction is terminated with DEM = 0b in link mode. – When the master interface receives a bus error.
0	EN	Enable Displays whether DMAC channel n is enabled or stopped. 0b: Operation stopped state 1b: Operation enabled state • Set condition: SETEN (CHCTRL_m) is set to 1b. • Clear conditions: – SWRST (CHCTRL_m) is set to 1b. – CLREN(CHCTRL_m) is set to 1b. – When an error response is received during transfer. – When all DMA transactions are completed in register mode (transaction complete when REN = 0b). – When DMA transfer (writeback if WBD = 0b) of the last descriptor (LE = 1b) is completed in link mode. – When stopping (LV = 0b) when reading descriptor in link mode

CAUTION

Treat transfers with the ER bit set as if the series of transfers is invalid. To interrupt a DMA transaction, mask and clear the transfer request or clear the enable. If a transfer request by DMA transfer request pin (DMAREQm) input and a transfer request by software (Set STG bit) are used together for the same channel, the activated activation factor cannot be specified. Use only one of the transfer requests in the system. When performing a transfer request by software, perform the next STG bit operation after completion(Check with Current Register etc.) of the previously requested DMA transfer operation.

19.5.2.11 Channel Control Register m (DMAA_DMACn_CHCTRL_m) (n = 1, 0, m = 7 to 0)

This register controls the DMA transfer operation of DMA channel m.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0028h (n = 0, m = 0)
<DMAA_S0_base> + 0068h (n = 0, m = 1)
<DMAA_S0_base> + 00A8h (n = 0, m = 2)
<DMAA_S0_base> + 00E8h (n = 0, m = 3)
<DMAA_S0_base> + 0128h (n = 0, m = 4)
<DMAA_S0_base> + 0168h (n = 0, m = 5)
<DMAA_S0_base> + 01A8h (n = 0, m = 6)
<DMAA_S0_base> + 01E8h (n = 0, m = 7)
<DMAA_S0_base> + 0428h (n = 1, m = 0)
<DMAA_S0_base> + 0468h (n = 1, m = 1)
<DMAA_S0_base> + 04A8h (n = 1, m = 2)
<DMAA_S0_base> + 04E8h (n = 1, m = 3)
<DMAA_S0_base> + 0528h (n = 1, m = 4)
<DMAA_S0_base> + 0568h (n = 1, m = 5)
<DMAA_S0_base> + 05A8h (n = 1, m = 6)
<DMAA_S0_base> + 05E8h (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLRINTMSK	SETINTMSK
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CLRSUS	SETSUS	—	CLRTC	CLRENDD	CLRRQ	SWRST	STG	SLREN	SETEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	R	RW	RW	RW	RW	RW	RW	RW

Table 19.5-12 DMAA_DMACn_CHCTRL_m Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 18	—	Reserved. These bits are read as 0b.The write value should always be 0b.
17	CLRINTMSK	Setting this bit cancels the state of masking the DMAENDm pin output. Also, the INTMSK bit of the CHSTATm register is 0b. If the mask is released while LVINT = 1b in the DCTRL register and END = 1b in the CHSTAT_m register, the DMAENDm pin output becomes active. (It is not active when LVINT = 0b.) When reading, 0b can be read. 1b: Cancels the mask set with SETINTMSK. 0b: Does not affect the operation.
16	SETINTMSK	Setting this bit temporarily masks the DMAENDm pin output. Also, the INTMSK bit of the CHSTATm register is set to 1b. When reading, 0b can be read. 1b: Masks DMAENDm. 0b: Does not affect the operation.
15 to 10	—	Reserved. These bits are read as 0b.The write value should always be 0b.
9	CLRSUS	Clear suspend Releases the pause state. When this bit is set to 1b when SUS of the CHSTAT_m register is 1b, the suspended state can be released. When this bit is read, 0b can be read. 1b: Cancel suspension of DMA transfer in progress. 0b: Does not affect operation.

Table 19.5-12 DMAA_DMACn_CHCTRL_m Register Contents (2/2)

Bit Position	Bit Name	Description
8	SETSUS	Set Suspend Suspends the ongoing DMA transfer. When this bit is set to 1b when EN of the CHSTAT_m register is 1b, DMA transfer in progress can be paused. When this bit is read, 0b can be read. 1b: Suspend DMA transfer in progress. 0b: Does not affect operation.
7	—	Reserved. This bit is read as 0b.The write value should always be 0b.
6	CLRTC	Clear TC Bit By setting this bit, the TC bit of the CHSTAT_m register can be cleared. When this bit is read, 0b can be read. 1b: Clear TC bit. 0b: Does not affect operation.
5	CLREND	Clear End Bit By setting this bit, the END bit of the CHSTAT_m register can be cleared. It also clears the DMAEND interrupt pin to low level. When this bit is read, 0b can be read. 1b: Clear END bit. 0b: Does not affect operation.
4	CLRRQ	Clear Request Bit By setting this bit, the RQST bit of the CHSTAT_m register can be cleared. When this bit is read, 0b can be read. 1b: Clear RQST bit. 0b: Does not affect operation.
3	SWRST	Software Reset The status register can be cleared by setting this bit. Set this bit when the EN bit is 0b and the TACT bit is 0b. When this bit is read, 0b can be read. 1b: Channel status register reset. 0b: Does not affect operation.
2	STG	Software Trigger Setting this bit sets an internal transfer request (software activation). If it is set at the same time as the SWRST bit, clearing by the SWRST bit has priority. When this bit is read, 0b can be read. 1b: Set transfer request by software (set RQST bit). 0b: Does not affect operation.
1	CLREN	Clear Enable The EN bit can be cleared by setting this bit. When this bit is read, 0b can be read. 1b: DMA transfer stopped (EN bit cleared). 0b: Does not affect operation.
0	SETEN	Set Enable Sets DMA transfer permission for DMAC channel m. If it is set at the same time as the SWRST bit, clearing by the SWRST bit has priority and transfer does not start. When this bit is read, 0b can be read. 1b: DMA transfer enabled (EN bit set). 0b: Does not affect operation.

19.5.2.12 Channel Configuration Register m (DMAA_DMACn_CHCFG_m) (n = 1, 0, m = 7 to 0)

This register controls the DMA transfer operation of DMA channel m.

Access Size: 32 bits

Address(es):
<DMAA_S0_base> + 002Ch (n = 0, m = 0)
<DMAA_S0_base> + 006Ch (n = 0, m = 1)
<DMAA_S0_base> + 00ACh (n = 0, m = 2)
<DMAA_S0_base> + 00ECh (n = 0, m = 3)
<DMAA_S0_base> + 012Ch (n = 0, m = 4)
<DMAA_S0_base> + 016Ch (n = 0, m = 5)
<DMAA_S0_base> + 01ACh (n = 0, m = 6)
<DMAA_S0_base> + 01ECh (n = 0, m = 7)
<DMAA_S0_base> + 042Ch (n = 1, m = 0)
<DMAA_S0_base> + 046Ch (n = 1, m = 1)
<DMAA_S0_base> + 04ACh (n = 1, m = 2)
<DMAA_S0_base> + 04ECh (n = 1, m = 3)
<DMAA_S0_base> + 052Ch (n = 1, m = 4)
<DMAA_S0_base> + 056Ch (n = 1, m = 5)
<DMAA_S0_base> + 05ACh (n = 1, m = 6)
<DMAA_S0_base> + 05ECh (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DMS	REN	RSW	RSEL	SBE	—	TCM	DEM	—	TM	DAD	SAD	DDS[3:0]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	R	RW	RW	R	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SDS[3:0]				—	AM[2:0]			—	LVL	HIEN	LOEN	REQD	SEL[2:0]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW

Table 19.5-13 DMAA_DMACn_CHCFG_m Register Contents (1/4)

Bit Position	Bit Name	Description
31	DMS	DMA Mode Select Sets the DMA mode. 0b: Register mode (initial value) 1b: Link mode
30	REN	Register Set Enable After the completion of the DMA transaction, DMA transfer is performed using the Next register set selected by RSEL. This bit is valid only in register mode. 0b: Do not continue. 1b: Continue execution. • Set condition: Write 1b to this bit. • Clear condition: Write 0b to this bit, or when DMA transaction is completed with REN = 1b.
29	RSW	Register Select Switch After the DMA transaction ends, RSEL is automatically inverted. This bit is valid only in register mode. 0b: Do not reverse RSEL after completion of DMA transaction. 1b: Reverse RSEL after completion of DMA transaction.

Table 19.5-13 DMAA_DMACn_CHCFG_m Register Contents (2/4)

Bit Position	Bit Name	Description
28	RSEL	Register Set Select Select the next register set to be executed next. This bit is valid only in register mode. When RSW = 1b, it is automatically reversed when the DMA transaction is completed. 0b: Execute Next0 Register Set. 1b: Execute Next1 Register Set. • Transition conditions: When RSW = 1b and DMA transaction completes.
27	SBE	Sweep Buffer Enable If the enable is cleared to 0b during a DMA transaction, select whether to sweep (by writing) the data that has already been read and captured in the buffer and stop it, or stop without sweeping. The sweep mode can be used only when REQD = 0b. 0b: Cancels transfer without sweeping buffer. 1b: Transfer is canceled by sweeping out the buffer.
26	—	Reserved. This bit is read as 0b.The write value should always be 0b.
25	TCM	Reserved. This bit is read as 0b.The write value should always be 0b.
24	DEM	DMAEND Mask Masks DMAEND [s] (s: pin selected by SEL) interrupt pin output during register mode transfer. If this bit is 1b at the DMAEND interrupt output timing, DMAEND [s] is not asserted. At this time, DEM is automatically cleared to 0b. 0b: Do not mask. 1b: Mask. • Clear condition: When DEM = 1b and DMA transaction completes
23	—	Reserved. This bit is read as 0b.The write value should always be 0b.
22	TM	Transfer Mode Sets the DMA transfer mode. 0b: Single transfer mode 1b: Block transfer mode
21	DAD	Sets the count direction of the transfer destination address of DMAC channel m. 0b: Increment 1b: Fixed If the destination address is beat unaligned, specify DAD = 0b (increment). If the destination address is beat aligned, both DAD = 0b and 1b can be set.
20	SAD	Sets the count direction of the transfer source address of DMAC channel m. 0b: Increment 1b: Fixed If the source address is beat unaligned, specify SAD = 0b (increment). If the source address is beat aligned, both SAD = 0b and 1b can be set.
19 to 16	DDS[3:0]	Destination Data Size Set the destination transfer size.

Set	Transfer Size	Remarks
0000b	8 bits	Initial value
0001b	16 bits	
0010b	32 bits	
0011b	64 bits	
0100b	128 bits	
0101b	256 bits	
0110b	512 bits	This can be set only when the number of buffer stages is 8 or 16. Setting is prohibited when the number of buffer stages is 4.
0111b	1024 bits	This can be set only when the number of buffer stages is 16. Setting is prohibited when the number of buffer stages is 4 or 8.
Others	—	Setting prohibited

Table 19.5-13 DMAA_DMACn_CHCFG_m Register Contents (3/4)

<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>15 to 12</td><td>SDS[3:0]</td><td>Source Data Size
Set the source transfer size.
<table>
<tr><th>Set</th><th>Transfer Size</th><th>Remarks</th></tr>
<tr><td>0000b</td><td>8 bits</td><td>Initial value</td></tr>
<tr><td>0001b</td><td>16 bits</td><td></td></tr>
<tr><td>0010b</td><td>32 bits</td><td></td></tr>
<tr><td>0011b</td><td>64 bits</td><td></td></tr>
<tr><td>0100b</td><td>128 bits</td><td></td></tr>
<tr><td>0101b</td><td>256 bits</td><td></td></tr>
<tr><td>0110b</td><td>512 bits</td><td>This can be set only when the number of buffer stages is 8 or 16.
Setting is prohibited when the number of buffer stages is 4.</td></tr>
<tr><td>0111b</td><td>1024 bits</td><td>This can be set only when the number of buffer stages is 16.
Setting is prohibited when the number of buffer stages is 4 or 8.</td></tr>
<tr><td>Others</td><td>—</td><td>Setting prohibited</td></tr>
</table></td></tr>
<tr><td>11</td><td>—</td><td>Reserved. This bit is read as 0b.The write value should always be 0b.</td></tr>
<tr><td>10 to 8</td><td>AM[2:0]</td><td>ACK Mode
Sets the DMAACKm output mode.
000b: Pulse mode (active for 1 clock)
001b: Level mode (active until the selected DMAREQ input becomes inactive)
01xb: Bus cycle mode (DMA transfer is active during bus cycle)
1xxb: Do not output DMAACKm</td></tr>
<tr><td>7</td><td>—</td><td>Reserved. These bits are read as 0b.The write value should always be 0b.</td></tr>
<tr><td>6</td><td>LVL</td><td>Level
Select whether to detect the DMA request at the signal level or at the edge.
0b: Detect at edge (Initial value)
1b: Detect by level</td></tr>
<tr><td>5</td><td>HIEN</td><td>High Enable
Select to detect the DMA request at the high level or rising edge of the signal.
If LVL = 0b:
HIEN = 1b: Recognizes that there was a request when the signal rises
HIEN = 0b: Does not recognize the request even when the signal rises
If LVL = 1b:
HIEN = 1b: Recognizes that there was a request when the signal is High
HIEN = 0b: Does not recognize the request even if the signal is High</td></tr>
<tr><td>4</td><td>LOEN</td><td>Low Enable
Select to detect the DMA request at the low level or falling edge of the signal.
If LVL = 0b:
LOEN = 1b: Recognizes that there was a request when the signal falls
LOEN = 0b: Does not recognize the request even if the signal falls
If LVL = 1b:
LOEN = 1b: Recognizes that there was a request when the signal is Low
LOEN = 0b: Does not recognize the request even if the signal is Low</td></tr>
<tr><td>3</td><td>REQD</td><td>Request Direction
Selects whether the DMAREQ selected by the SEL bit is on the source side or the destination side. This bit also selects the timing at which DMAACK becomes active.
0b: Source side, DMAACK is active when reading
1b: Destination side, DMAACK is active when writing</td></tr>
</table>

Table 19.5-13 DMAA_DMACn_CHCFG_m Register Contents (4/4)

Bit Position	Bit Name	Description
2 to 0	SEL[2:0]	Terminal Select Select one from eight DMAREQ / DMAACK signals.

SEL[2:0]	Select Signal	Remarks
000b	DMAREQ[0], DMAACK[0]	Initial value
001b	DMAREQ[1], DMAACK[1]	
010b	DMAREQ[2], DMAACK[2]	
011b	DMAREQ[3], DMAACK[3]	
100b	DMAREQ[4], DMAACK[4]	
101b	DMAREQ[5], DMAACK[5]	
110b	DMAREQ[6], DMAACK[6]	
111b	DMAREQ[7], DMAACK[7]	

NOTE

If units with different clocks are DMA transfer targets and require DMAACK, the DMAACK signal may not be received successfully due to the synchronization clock. In such a case, set AM[2:0] to 001b or 010b so that DMAACK becomes active for a long time.

19.5.2.13 Channel Interval Register m (DMAA_DMACn_CHITVL_m) (n = 1, 0, m = 7 to 0)

This register sets the transfer interval for DMAC channel m.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0030h (n = 0, m = 0)
<DMAA_S0_base> + 0070h (n = 0, m = 1)
<DMAA_S0_base> + 00B0h (n = 0, m = 2)
<DMAA_S0_base> + 00F0h (n = 0, m = 3)
<DMAA_S0_base> + 0130h (n = 0, m = 4)
<DMAA_S0_base> + 0170h (n = 0, m = 5)
<DMAA_S0_base> + 01B0h (n = 0, m = 6)
<DMAA_S0_base> + 01F0h (n = 0, m = 7)
<DMAA_S0_base> + 0430h (n = 1, m = 0)
<DMAA_S0_base> + 0470h (n = 1, m = 1)
<DMAA_S0_base> + 04B0h (n = 1, m = 2)
<DMAA_S0_base> + 04F0h (n = 1, m = 3)
<DMAA_S0_base> + 0530h (n = 1, m = 4)
<DMAA_S0_base> + 0570h (n = 1, m = 5)
<DMAA_S0_base> + 05B0h (n = 1, m = 6)
<DMAA_S0_base> + 05F0h (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ITVL[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 19.5-14 DMAA_DMACn_CHITVL_m Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.The write value should always be 0b.
15 to 0	ITVL[15:0]	Sets the channel transfer interval.

19.5.2.14 Channel Extension Register m (DMAA_DMACn_CHEXT_m) (n = 1, 0, m = 7 to 0)

This register functions as the DMAC channel m expansion register.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0034h (n = 0, m = 0)
<DMAA_S0_base> + 0074h (n = 0, m = 1)
<DMAA_S0_base> + 00B4h (n = 0, m = 2)
<DMAA_S0_base> + 00F4h (n = 0, m = 3)
<DMAA_S0_base> + 0134h (n = 0, m = 4)
<DMAA_S0_base> + 0174h (n = 0, m = 5)
<DMAA_S0_base> + 01B4h (n = 0, m = 6)
<DMAA_S0_base> + 01F4h (n = 0, m = 7)
<DMAA_S0_base> + 0434h (n = 1, m = 0)
<DMAA_S0_base> + 0474h (n = 1, m = 1)
<DMAA_S0_base> + 04B4h (n = 1, m = 2)
<DMAA_S0_base> + 04F4h (n = 1, m = 3)
<DMAA_S0_base> + 0534h (n = 1, m = 4)
<DMAA_S0_base> + 0574h (n = 1, m = 5)
<DMAA_S0_base> + 05B4h (n = 1, m = 6)
<DMAA_S0_base> + 05F4h (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCA[3:0]				—	DPR[2:0]			SCA[3:0]				—	SPR[2:0]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 19.5-15 DMAA_DMACn_CHEXT_m Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.The write value should always be 0b.
15 to 12	DCA[3:0]	Destination CACHE Sets the output value to CACHE[3:0] of DMA write transfer. The initial value is 0000b.
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.
10 to 8	DPR[2:0]	Destination PROT Sets the output value to PROT[2:0] of DMA write transfer. The initial value is 000b.
7 to 4	SCA[3:0]	Destination CACHE Sets the output value to CACHE[3:0] of DMA read transfer. The initial value is 0000b.
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	SPR[2:0]	Destination PROT Sets the output value to PROT[2:0] of DMA read transfer. The initial value is 000b.

19.5.2.15 Next Link Address Resister m (DMAA_DMACn_NXLA_m) (n = 1, 0, m = 7 to 0)

This register sets the descripter address to load next in link mode.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0038h (n = 0, m = 0)
<DMAA_S0_base> + 0078h (n = 0, m = 1)
<DMAA_S0_base> + 00B8h (n = 0, m = 2)
<DMAA_S0_base> + 00F8h (n = 0, m = 3)
<DMAA_S0_base> + 0138h (n = 0, m = 4)
<DMAA_S0_base> + 0178h (n = 0, m = 5)
<DMAA_S0_base> + 01B8h (n = 0, m = 6)
<DMAA_S0_base> + 01F8h (n = 0, m = 7)
<DMAA_S0_base> + 0438h (n = 1, m = 0)
<DMAA_S0_base> + 0478h (n = 1, m = 1)
<DMAA_S0_base> + 04B8h (n = 1, m = 2)
<DMAA_S0_base> + 04F8h (n = 1, m = 3)
<DMAA_S0_base> + 0538h (n = 1, m = 4)
<DMAA_S0_base> + 0578h (n = 1, m = 5)
<DMAA_S0_base> + 05B8h (n = 1, m = 6)
<DMAA_S0_base> + 05F8h (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	NXLA[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NXLA[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R

Table 19.5-16 DMAA_DMACn_NXLA_m Register Contents

Bit Position	Bit Name	Description
31 to 0	NXLA[31:0]	Set the link destination address. The lower 2 bits are masked with 0b. Only word-aligned addresses can be set.

19.5.2.16 Current Link Address Resister m (DMAA_DMACn_CRLA_m) (n = 1, 0, m = 7 to 0)

This is a 32-bit register that displays the address of the currently executing descriptor.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 003Ch (n = 0, m = 0)
<DMAA_S0_base> + 007Ch (n = 0, m = 1)
<DMAA_S0_base> + 00BCh (n = 0, m = 2)
<DMAA_S0_base> + 00FCh (n = 0, m = 3)
<DMAA_S0_base> + 013Ch (n = 0, m = 4)
<DMAA_S0_base> + 017Ch (n = 0, m = 5)
<DMAA_S0_base> + 01BCh (n = 0, m = 6)
<DMAA_S0_base> + 01FCh (n = 0, m = 7)
<DMAA_S0_base> + 043Ch (n = 1, m = 0)
<DMAA_S0_base> + 047Ch (n = 1, m = 1)
<DMAA_S0_base> + 04BCh (n = 1, m = 2)
<DMAA_S0_base> + 04FCh (n = 1, m = 3)
<DMAA_S0_base> + 053Ch (n = 1, m = 4)
<DMAA_S0_base> + 057Ch (n = 1, m = 5)
<DMAA_S0_base> + 05BCh (n = 1, m = 6)
<DMAA_S0_base> + 05FCh (n = 1, m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CRLA[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CRLA[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 19.5-17 DMAA_DMACn_CRLA_m Register Contents

Bit Position	Bit Name	Description
31 to 0	CRLA[31:0]	The address of the currently executing descriptor is displayed.

19.5.2.17 DMA Control Register (DMAA_DMACn_DCTRL) (n = 1, 0)

This register sets the transfer type for descriptor access and arbitration between channels.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0300h (n = 0)
<DMAA_S0_base> + 0700h (n = 1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	LWCA[3:0]				—	LWPR[2:0]			LDCA[3:0]				—	LDPR[2:0]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LVINT	PR
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Table 19.5-18 DMAA_DMACn_DCTRL Register Contents

Bit Position	Bit Name	Description
31 to 28	LWCA[3:0]	Link Writeback CACHE Sets the value to be output to CACHE[3:0] during descriptor write back in link mode.
27	—	Reserved. These bits are read as 0b. The write value should always be 0b.
26 to 24	LWPR[2:0]	Link Writeback PROT Sets the value to be output to MHPROT[2:0] during descriptor write-back in link mode.
23 to 20	LDCA[3:0]	Link Descriptor CACHE Sets the value to be output to CACHE[3:0] when loading a descriptor in link mode.
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	LDPR[2:0]	Link Descriptor PROT Sets the value to be output to MHPROT[2:0] when loading a descriptor in link mode.
15 to 2	—	Reserved. This bit is read as 0b.The write value should always be 0b.
1	LVINT	Sets whether to output DMAEND[7:0], DMAERR as a pulse or level. 0b: Pulse output (initial value) 1b: Level output *Note*: Pulse output setting is prohibited
0	PR	Sets the transfer priority control mode between channels 0b: Fixed priority mode (initial value) 1b: Round robin mode

19.5.2.18 DMA Status EN Register (DMAA_DMACn_DST_EN) (n = 1, 0)

This register displays the EN bit status of all channels.

Writing to this register does not change the value of each bit.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0310h (n = 0)
<DMAA_S0_base> + 0710h (n = 1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 19.5-19 DMAA_DMACn_DST_EN Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7	EN7	Displays the state of the DMAC channel 7 EN bit.
6	EN6	Displays the state of the DMAC channel 6 EN bit.
5	EN5	Displays the state of the DMAC channel 5 EN bit.
4	EN4	Displays the state of the DMAC channel 4 EN bit.
3	EN3	Displays the state of the DMAC channel 3 EN bit.
2	EN2	Displays the state of the DMAC channel 2 EN bit.
1	EN1	Displays the state of the DMAC channel 1 EN bit.
0	EN0	Displays the state of the DMAC channel 0 EN bit.

NOTE

Channels that do not exist in the channel configuration are set to 0b.

19.5.2.19 DMA Status ER Register (DMAA_DMACn_DST_ER) (n = 1, 0)

Displays the ER bit status of all channels.

Writing to this register does not change the value of each bit.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0314h (n = 0)
<DMAA_S0_base> + 0714h (n = 1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 19.5-20 DMAA_DMACn_DST_ER Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7	ER7	Displays the state of the DMAC channel 7 ER bit.
6	ER6	Displays the state of the DMAC channel 6 ER bit.
5	ER5	Displays the state of the DMAC channel 5 ER bit.
4	ER4	Displays the state of the DMAC channel 4 ER bit.
3	ER3	Displays the state of the DMAC channel 3 ER bit.
2	ER2	Displays the state of the DMAC channel 2 ER bit.
1	ER1	Displays the state of the DMAC channel 1 ER bit.
0	ER0	Displays the state of the DMAC channel 0 ER bit.

NOTE

Channels that do not exist in the channel configuration are set to 0b.

19.5.2.20 DMA Status END Register (DMAA_DMACn_DST_END) (n = 1, 0)

This register displays the END bit status of all channels.

Writing to this register does not change the value of each bit.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0318h (n = 0)
<DMAA_S0_base> + 0718h (n = 1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	END7	END6	END5	END4	END3	END2	END1	END0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 19.5-21 DMAA_DMACn_DST_END Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7	END7	Displays the state of the DMAC channel 7 END bit.
6	END6	Displays the state of the DMAC channel 6 END bit.
5	END5	Displays the state of the DMAC channel 5 END bit.
4	END4	Displays the state of the DMAC channel 4 END bit.
3	END3	Displays the state of the DMAC channel 3 END bit.
2	END2	Displays the state of the DMAC channel 2 END bit.
1	END1	Displays the state of the DMAC channel 1 END bit.
0	END0	Displays the state of the DMAC channel 0 END bit.

NOTE

Channels that do not exist in the channel configuration are set to 0b.

19.5.2.21 DMA Status TC Register (DMAA_DMACn_DST_TC) (n = 1, 0)

This register displays the TC bit status of all channels.

Writing to this register does not change the value of each bit.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 031Ch (n = 0)
<DMAA_S0_base> + 071Ch (n = 1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 19.5-22 DMAA_DMACn_DST_TC Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7	TC7	Displays the state of the DMAC channel 7 TC bit.
6	TC6	Displays the state of the DMAC channel 6 TC bit.
5	TC5	Displays the state of the DMAC channel 5 TC bit.
4	TC4	Displays the state of the DMAC channel 4 TC bit.
3	TC3	Displays the state of the DMAC channel 3 TC bit.
2	TC2	Displays the state of the DMAC channel 2 TC bit.
1	TC1	Displays the state of the DMAC channel 1 TC bit.
0	TC0	Displays the state of the DMAC channel 0 TC bit.

NOTE

Channels that do not exist in the channel configuration are set to 0b.

19.5.2.22 DMA Status SUS Register (DMAA_DMACn_DST_SUS) (n = 1, 0)

This register displays the SUS bit status of all channels.

Writing to this register does not change the value of each bit.

Access Size: 32 bits

Address(es): <DMAA_S0_base> + 0320h (n = 0)
<DMAA_S0_base> + 0720h (n = 1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SUS7	SUS6	SUS5	SUS4	SUS3	SUS2	SUS1	SUS0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 19.5-23 DMAA_DMACn_DST_SUS Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7	SUS7	Displays the state of the DMAC channel 7 SUS bit.
6	SUS6	Displays the state of the DMAC channel 6 SUS bit.
5	SUS5	Displays the state of the DMAC channel 5 SUS bit.
4	SUS4	Displays the state of the DMAC channel 4 SUS bit.
3	SUS3	Displays the state of the DMAC channel 3 SUS bit.
2	SUS2	Displays the state of the DMAC channel 2 SUS bit.
1	SUS1	Displays the state of the DMAC channel 1 SUS bit.
0	SUS0	Displays the state of the DMAC channel 0 SUS bit.

NOTE

Channels that do not exist in the channel configuration are set to 0b.

19.6 Functional Description

The prefix (DMAA_DMACn_) of the register names is omitted in this and subsequent sections.

19.6.1 DMA Mode

This section describes the DMAC mode specifications of the DMAC unit.

19.6.1.1 Mode Setting

The DMA mode can be switched between register mode and link mode according to the value of the DMS field in the CHCFG_m register.

Table 19.6-1 DMA Mode Setting

DMS (CHCFG_m)	Mode	Description
0b	Register mode	The values set in the next register set are used to proceed with DMA transfer.
1b	Link mode	The descriptor is set in the current register to proceed with DMA transfer. Loading of the descriptor and DMA transfer are repeated unless these are stopped with the setting by the descriptor or by the control register.

19.6.1.2 Register Mode

In register mode, the values set in the internal registers are used for DMA transfer.

Two types (Next0 Register Set and Next1 Register Set) of transfer source address, transfer destination address, and number of transfer bytes can be set. The Next register set to be used can be selected and transferred, or two Next register sets can be transferred consecutively.

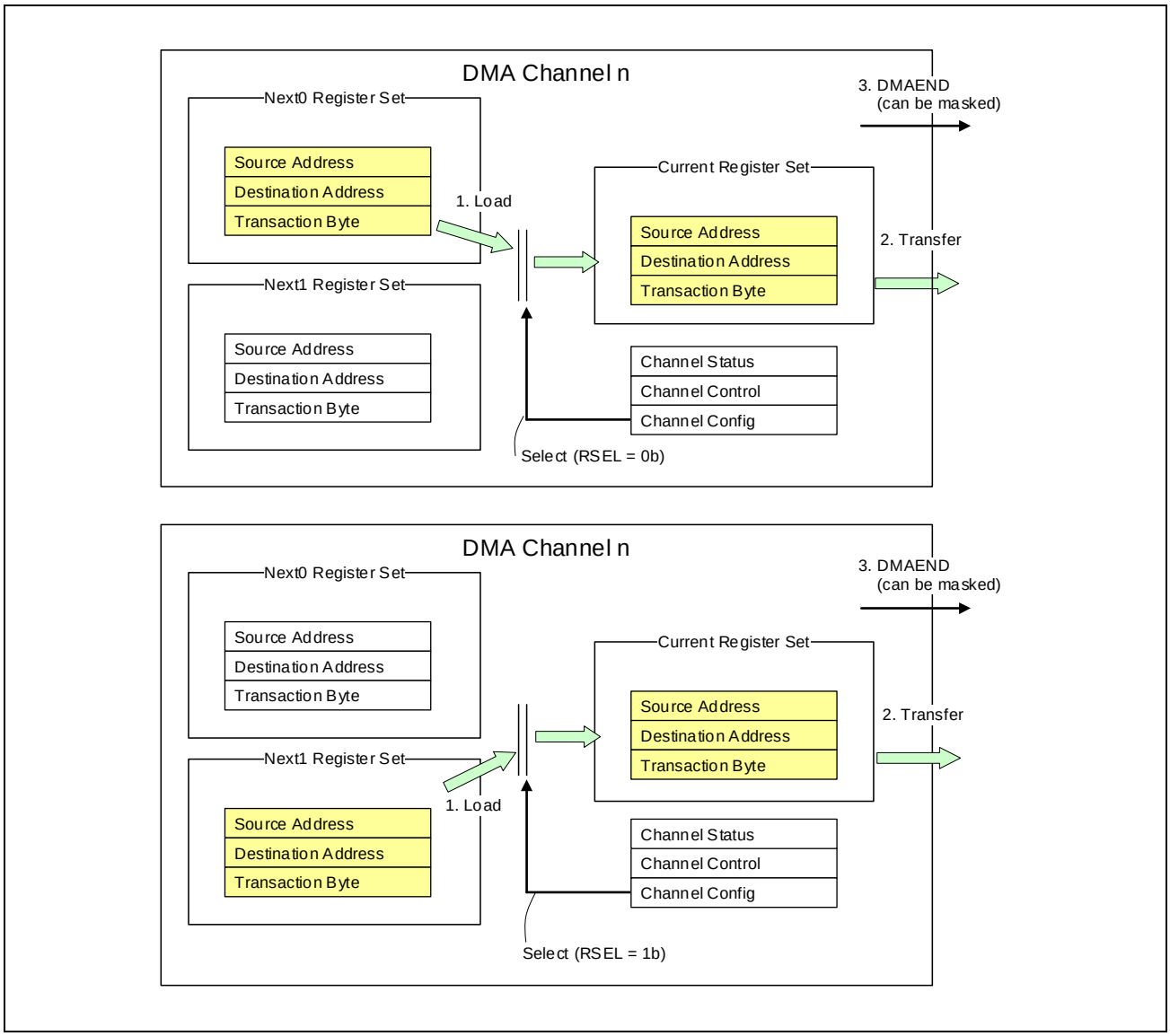


Figure 19.6-1 Overview of Register Normal Mode

The above figure illustrates operations when Next0 is executed (upper part of the figure) and when Next1 is executed (lower part of the figure).

(1) Flow of Operations

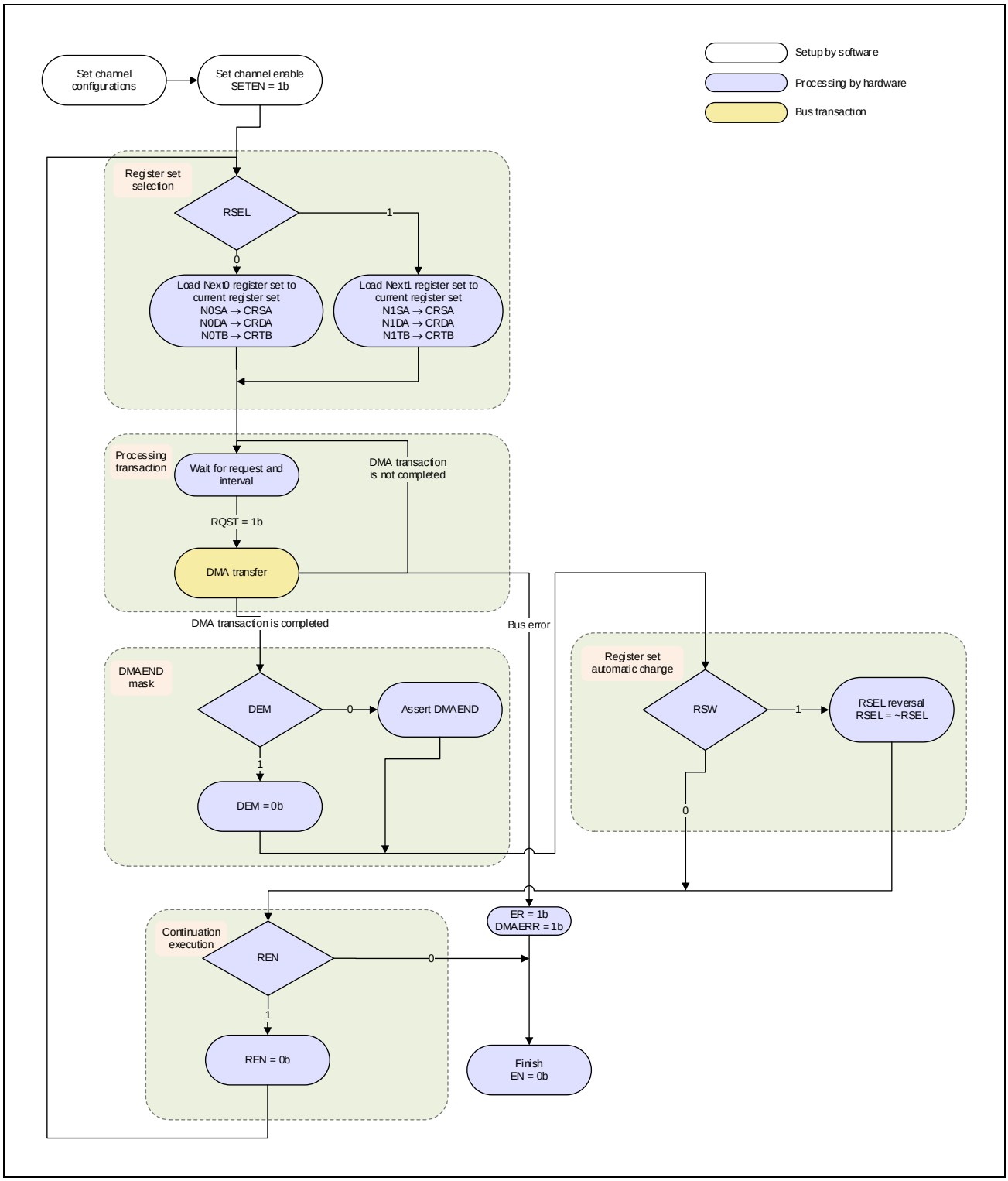


Figure 19.6-2 Register Mode Flow

<Description of the Register Mode Flow>

1. Set channel configuration

In addition, set the DMA register set (REQ, DMAACK, the amount of data for transfer, etc.) in the channel register set (See **Section 19.6.2, DMA Transfer**).

2. Register set selection

When the EN bit is set to 1b, the setting of the next register set selected by RSEL is loaded to the current register set.

3. Processing DMA transaction

DMA transfer proceeds in accord with the set value. For details of transfer, see **Section 19.6.2, DMA Transfer**.

4. Masking DMAEND

DMAEND is masked in accord with the value set in the DEM bit of CHCFG_m. DMAEND is not output if DEM = 1b. After that, DEM is automatically cleared to 0b.

5. Register set automatic change

Whether or not the other next register set is to be used is determined by the value set in the RSW bit of CHCFG_m.

6. Continuous execution

Whether or not DMA transfer is to be consecutively executed is determined by the value set in the REN bit of CHCFG_m. Transfer is executed consecutively if REN = 1b. After that, REN is automatically cleared to 0b.

(2) Register Settings

(a) Register Mode Setting

Select the register set to be executed.

Table 19.6-2 Register Mode Setting

DMS (CHCFG_m)	RSEL (CHCFG_m)	Description
0b	0b	Execute the Next0 register set.
	1b	Execute the Next1 register set.

(b) DMAEND Mask Setting

DMAEND can be masked for each register set.

Table 19.6-3 DMAEND Mask Setting

DEM (CHCFG_m)	Operation	Remarks
0b	DMAEND is issued on completion of the DMA transaction.	
1b	DMAEND is not issued even if the DMA transaction has completed. DEM is cleared to 0b by hardware following the completion of the DMA transaction.	

(c) Automatic Register Set Execution Setting

After DMA transfer, a DMA transaction of the selected register set is automatically executed.

Table 19.6-4 Automatic Register Set Execution Setting

REN (CHCFG_m)	Operation	Remarks
0b	When the DMA transaction of the register set that is set in the RSEL bit is completed, the EN bit is cleared to end DMA operation.	Set this to execute the DMA transaction once.
1b	After the completion of the DMA transaction, DMA transfer of the contents of the selected register set follows. When continuous transfer is established, REN is cleared to 0b.	Set this to execute the contents of the register set consecutively.

(d) Automatic Register Set Execution Setting

When REN = 1b, the next register set to be automatically executed can be switched following the completion of the DMA transaction.

Table 19.6-5 Automatic Register Set Execution Setting

RSW (CHCFG_m)	Operation	Remarks
0b	When REN = 1b and the DMA transaction is completed, the register set is not switched.	Set this when using one register set only.
1b	When REN = 1b and the DMA transaction is completed, RSEL is automatically inverted and the other register set is selected.	Set this when switching the register set.

(3) Example Settings

(a) When Using the Next0 Register Set Only

Table 19.6-6 Example Register Mode Setting 1

DMS (CHCFG_m)	RSEL (CHCFG_m)	DEM (CHCFG_m)	TCM (CHCFG_m)	RSW (CHCFG_m)	REN (CHCFG_m)
0b (Register mode)	0b (Next0)	0b (No masking)	0b (No masking)	0b (No switching)	0b (No continuous execution)

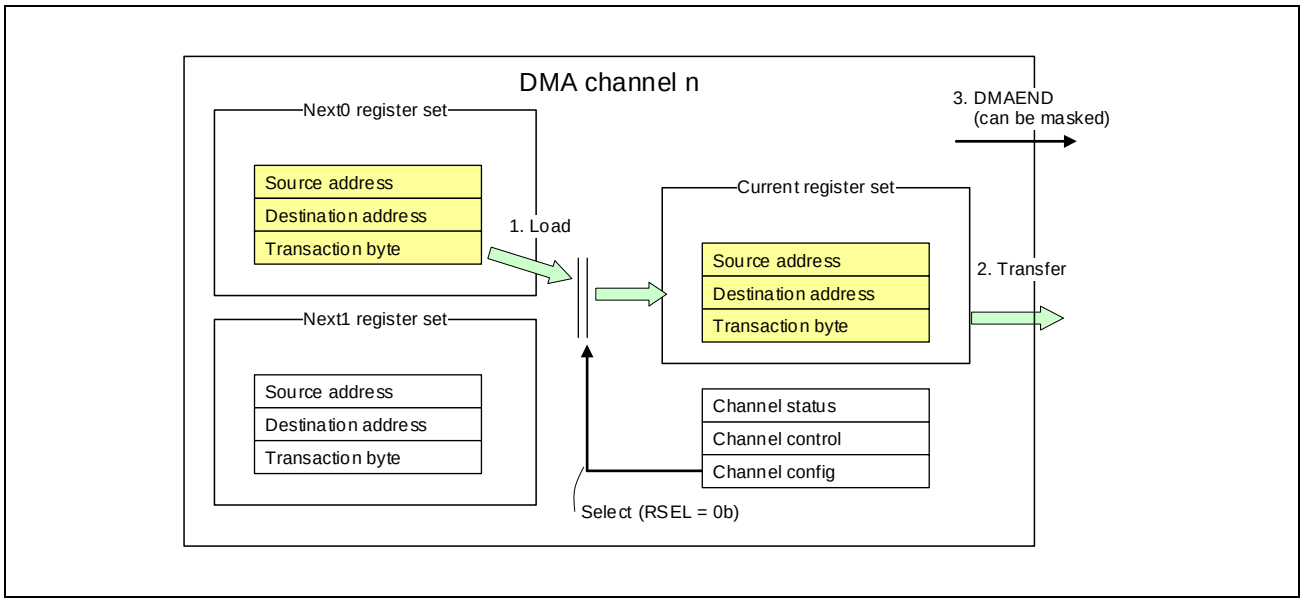


Figure 19.6-3 Example Register Mode Setting 1

1. Set EN = 1b (SETEN = 1b) to load the Next0 register set to the current register set.
2. Execute a DMA transaction according to the values of the current register set and channel register set.
3. DMAEND is issued following the completion of the DMA transaction.
4. Since REN is 0b, clear EN to 0b to end the operation.

(b) When Using Two Register Sets Consecutively

Table 19.6-7 Automatic Register Set Execution Setting

DMS (CHCFG_m)	RSEL (CHCFG_m)	DEM (CHCFG_m)	TCM (CHCFG_m)	RSW (CHCFG_m)	REN (CHCFG_m)
0b (Register mode)	0b (Next0)	1b (Masking)	0b (No masking)	1b (Switching)	1b (Continuous execution)

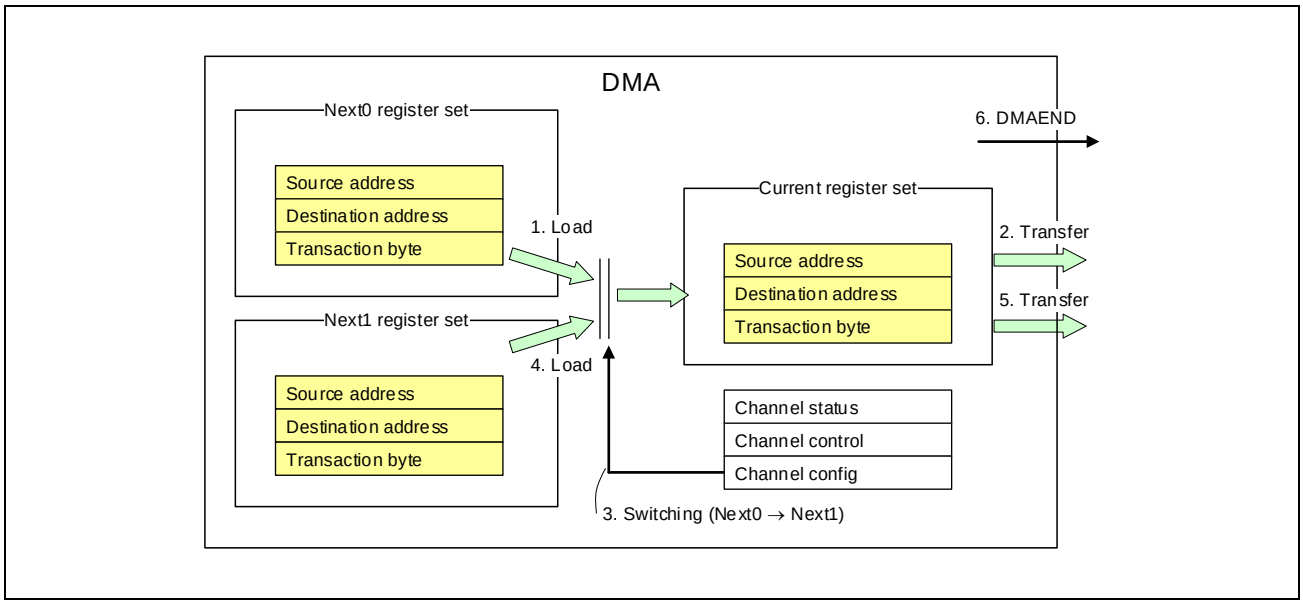


Figure 19.6-4 Example Register Mode Setting 2

1. Set EN = 1b (SETEN = 1b) to load the Next0 register set to the current register set.
2. Execute a DMA transaction according to the values of the current register set and channel register set.
3. Since DEM is 1b, DMAEND is not output following the completion of the DMA transaction. DEM is automatically cleared to 0.
4. Since REN is 1b, the operation is executed continuously. REN is automatically cleared to 0b.
5. Since RSW is 1b, the next register set to be executed is switched (RSEL = 0b → 1b).
6. Load the Next1 register set to the current register set.
7. Execute a DMA transaction according to the values of the current register set and channel register set.
8. Since DEM is 0b, DMAEND is issued following the completion of the DMA transaction.
9. Since REN is 0b, clear EN to 0b to end the operation.

19.6.1.3 Link Mode

In link mode, a DMA transaction is executed by loading descriptors in the external memory area as the settings. The DMAC has a next link address and current link address per channel and these are used to set the address of a next descriptor to be executed and to indicate the address of a descriptor for the DMA transaction that is currently in progress, respectively.

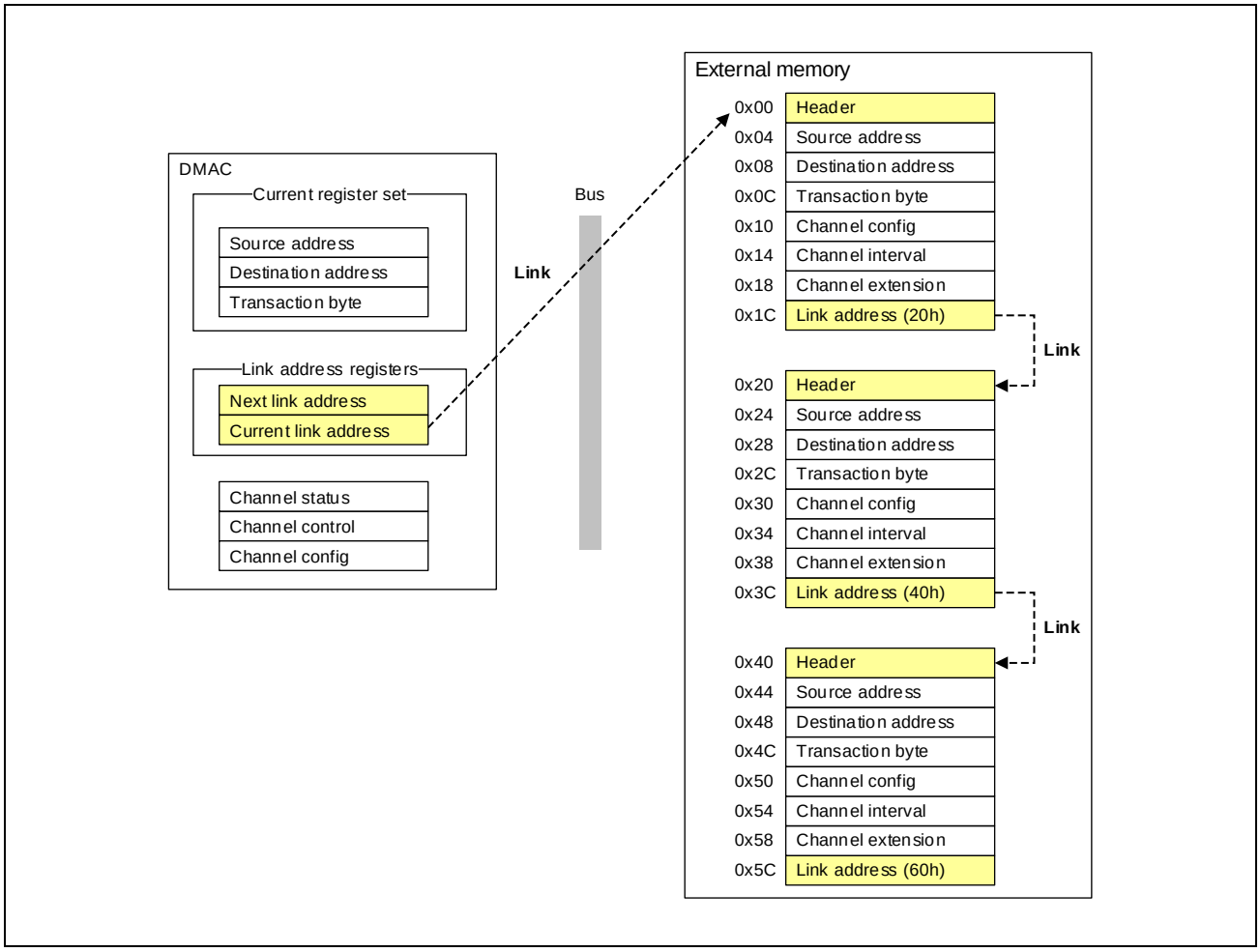


Figure 19.6-5 Overview of Link Mode

(1) Flow of Operations

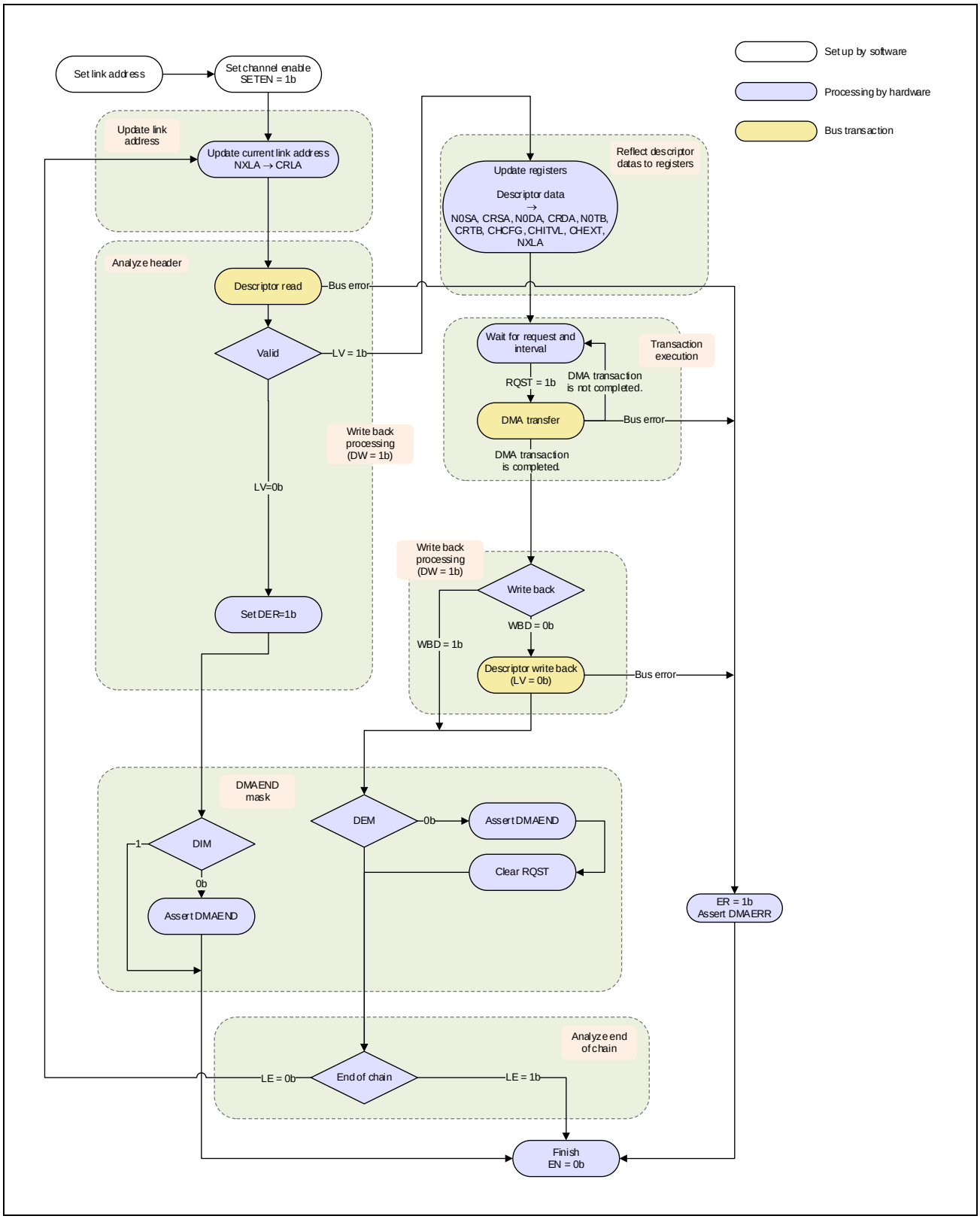


Figure 19.6-6 Flow of Link Mode

<Description of the Link Mode Flow>

1. Set channel configuration

   Set the address where the link destination is to start in NXLA_m.

2. Link address update

   Setting EN = 1b (setting SETEN to 1b) loads the link address set in NXLA_m to CRLA_n.

3. Reading the descriptor and judging the header

   The DMAC starts to load the descriptor and checks the header contents. If LV = 0b, the descriptor is discarded and DER is set to 1b indicating the end state (EN = 0b). If DIM within the header is 0b at this time, DMAEND is issued.

4. Descriptor setting

   Set the loaded descriptor in the current register set and channel register set. Also, set the next link destination in NXLA_m.

5. Processing DMA transaction

   Execute a DMA transaction according to the set values.

6. Header write-back

   If WBD in the header = 0b, the DMAC writes back 0b to the LV bit in the header.

7. Masking DMAEND

   If the DEM bit in CHCFG_m is 0b, DMAEND is issued.

8. Judging the end of the link

   If LE in the header = 1b, after the transfer according to the descriptor settings, TCO is issued (enabling masking by CHCFG_m) and EN is cleared to 0b to stop the operation. If LE = 0b, the current register set is updated and the DMAC starts to load the next descriptor.

(2) Register Settings

(a) Link Mode Setting

To use link mode, set the DMS bit in the CHCFG_m register to 1b.

Table 19.6-8 Link Mode Setting

DMS (CHCFG_m)	Description
1b	Operation is in link mode. The value of this bit cannot be changed by the descriptor.

(b) LINK Address Setting

There are the next link address register and the current link address register as registers which indicate the link destination.

When starting link mode, set the link destination in the next link address register.

The next link address indicates the next link destination after loading of the descriptor. The current link address indicates the address of the link currently being executed.

Table 19.6-9 Link Address Register Set

Register	Description
Next Link Address Register (NXLA_m)	Sets and indicates the next link destination. Before starting link mode, set the address of the link destination in this register.
Current Link Address Register (CRLA_n)	Indicates the link destination currently being executed. This register is only readable.

CAUTION

In link mode, the setting can be changed by reading the descriptor; however the timing of the change to the setting and a hardware request cannot be synchronized. Therefore, when using hardware requests, set AM, LVL, HIEN, LOEN, and SEL of the CHCFG_m register before enabling hardware requests and also make sure that these setting bits have the same values in the descriptor.

(3) Descriptor Settings

From the link destination address, prepare the parts of each descriptor in the following order.

The DMAC reads the descriptors in bursts.

(a) Descriptor Arrangement

Table 19.6-10 Descriptor Setting Arrangement

Address	Data	Remark
LinkAddress + 00h	Header	
LinkAddress + 04h	Source address	
LinkAddress + 08h	Destination address	
LinkAddress + 0Ch	Transaction byte	
LinkAddress + 10h	Config	Register mode cannot be set.
LinkAddress + 14h	Interval	
LinkAddress + 18h	Extension	
LinkAddress + 1Ch	Next link address	

Note: For the link destination, set the addresses aligned in 32-bit boundaries.

(b) Header

The header indicates the descriptor state as shown below.

This area is automatically read by the DMAC before starting DMA transfer in link mode. After the completion of the DMA transaction, the DMAC writes back the header and sets the LV bit to 0b to indicate the state of transfer.

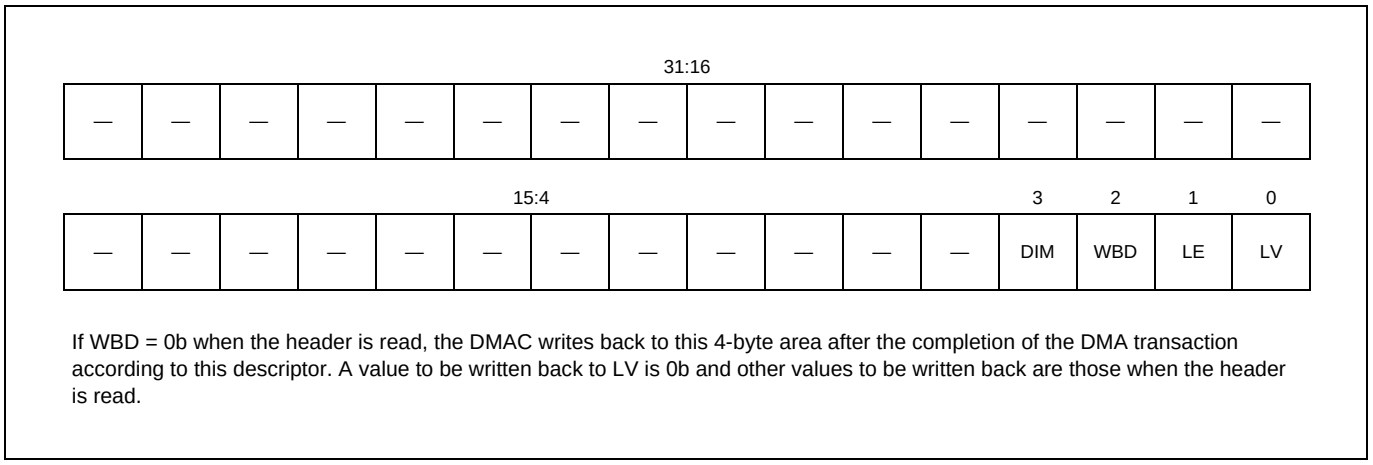


Figure 19.6-7 Header Area

Table 19.6-11 Header Area

Bit Position	Bit Name	Function
31:4	—	—
3	DIM	Descriptor Interrupt Mask If LV = 0b when the header is loaded, this bit sets whether or not to mask DMAEND. 0b: DMAEND is issued. 1b: DMAEND is not issued.
2	WBD	Write Back Disable This bit masks execution of write-back to the LV bit. When the setting of this bit is 1b, the DMAC does not proceed with write-back operation. 0b: The LV bit is written back to 0. 1b: The LV bit is not written back.
1	LE	Link End This bit indicates that the link ends in the DMA transaction of this descriptor. Set this bit to 1b to indicate the end of the link. 0b: The link continues. 1b: The link ends.
0	LV	Link Valid This bit indicates that this descriptor is enabled. When WBD = 0b, the DMAC writes 0b to this bit following the execution of the DMA transaction written in the descriptor. When setting the header, set this bit to 1b. 0b: The descriptor is disabled. 1b: The descriptor is enabled

(c) Setting the Descriptors Other than the Header

The values in the descriptors other than the header have the same specifications as those of the internal registers (however, the DMS bit of the CHCFG_m register cannot be modified by the descriptor). For the specifications of the internal registers, see **Section 19.5, Register Descriptions**.

For example settings of the descriptors, see **Section 19.7.1.4, Example Setting 4 (Link Mode)**.

(d) PROT and CACHE Settings at the Time of Access to the Descriptors

The PROT and CACHE settings at the time of access to the descriptors can be set in LWCA, LWPR, LDCA, and LDPR described in **Section 19.5.2.17, DMA Control Register (DMAA_DMACn_DCTRL) (n = 1, 0)**. Make the settings according to the destination for access in which the descriptors are prepared.

(a) Descriptor Areas and DMA Transfer Areas

The figure below shows an overview of the descriptor areas and DMA transfer areas, which are accessed by the DMAC.

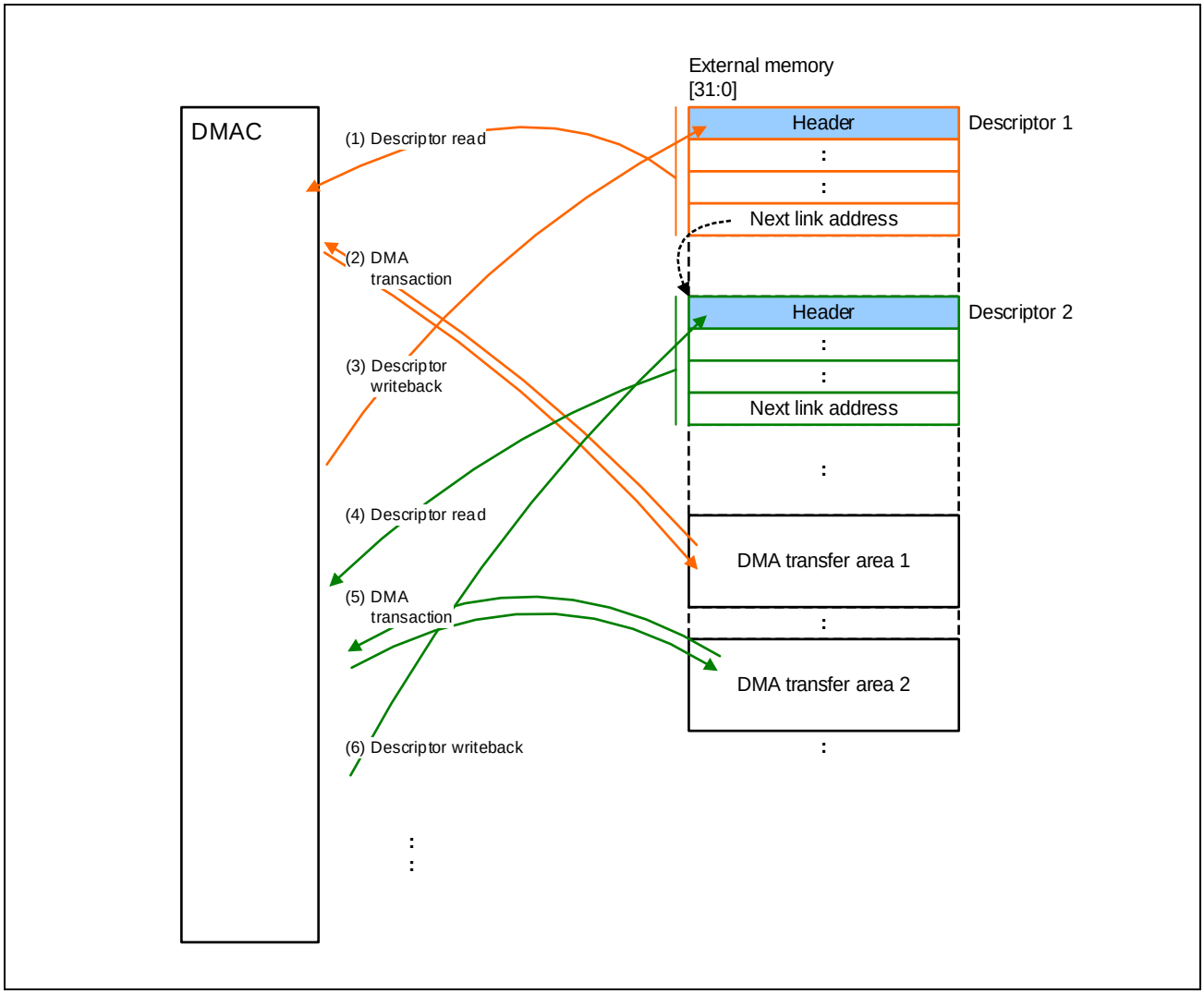


Figure 19.6-8 Overview of the Descriptor Areas and DMA Transfer Areas

(1) Descriptor read

Load the value set in the internal next link address register to the current link address register, and then read the descriptor from the external memory space (descriptor 1) indicated by the current link address register.

(2) DMA transfer

If LV in the header of the descriptor = 1b, execute DMA transfer according to the descriptor information.

(3) Descriptor write-back

After the DMA transfer for the specified number of bytes, if WBD in the header = 0b, write-back is executed on the header of descriptor 1 in the burst size of 32 bits with 0b for LV and the value read in step 1 for the other fields as data.

(4) Descriptor read

If LE in the header of the descriptor which has been previously read (in step 1) = 0b, read the next descriptor from the address (descriptor 2) indicated by the next link address in the descriptor.

(5) DMA transfer

If LV in the header of the descriptor = 1b, execute DMA transfer according to the descriptor information.

(6) Descriptor write-back

After the DMA transfer for the specified number of bytes, if WBD in the header = 0b, write-back is executed on the header of descriptor 2 in the burst size of 32 bits with 0 for LV and the value read in step 4 for the other fields as data.

After that, repeat steps (4) to (6).

If LE in the header = 1b and WBD = 0b, DMA transfer proceeds in accord with the descriptor settings, and 0 is written back to the LV bit of the header, after which the operation ends.

If LE in the header = 1b and WBD = 1b, DMA transfer proceeds in accord with the descriptor settings, after which the operation ends (write-back does not proceed).

If LV in the header = 0b, the operation stops (DMA transfer does not proceed).

(4) Example Descriptor Configuration

In link mode, descriptors can be configured as shown in the figure below.

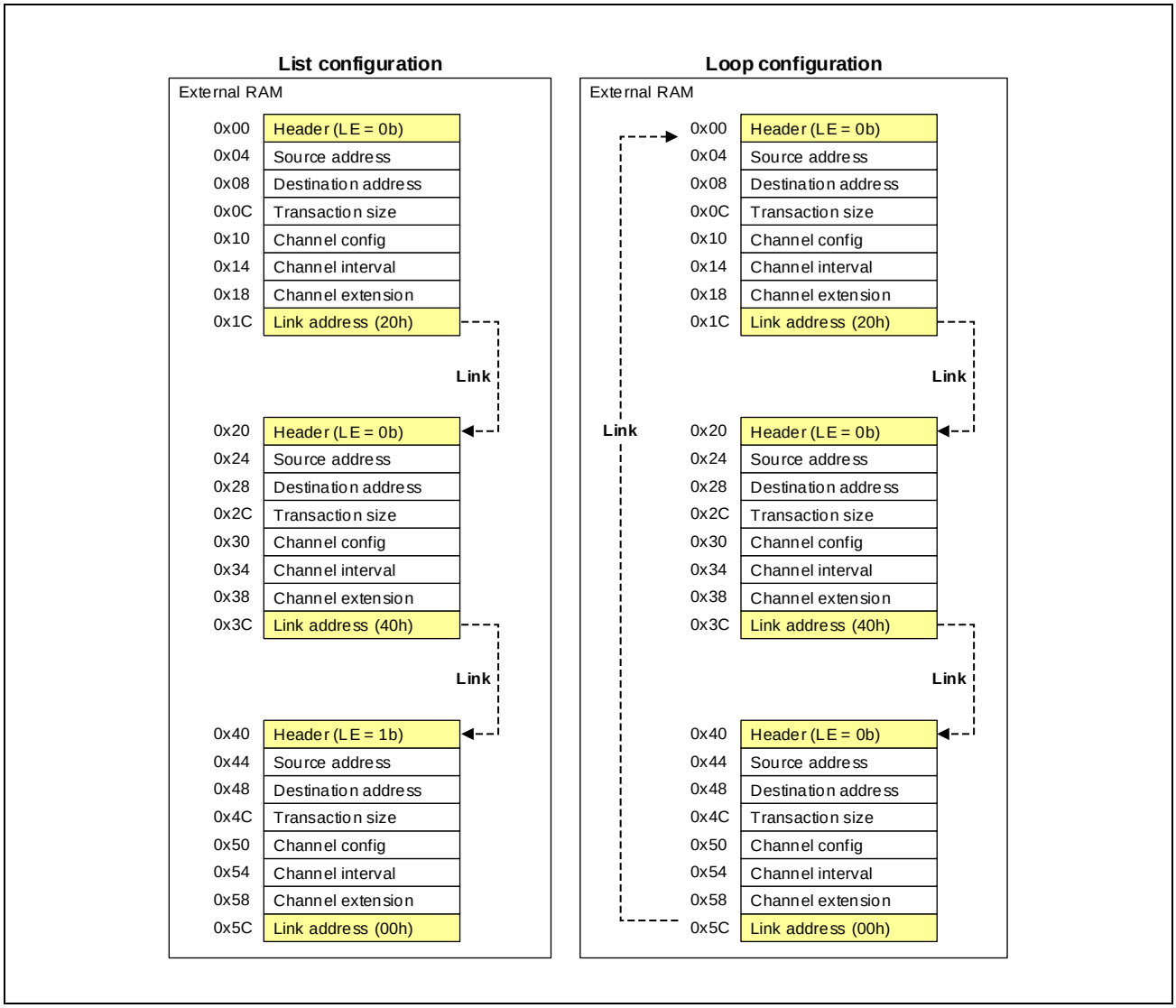


Figure 19.6-9 Example Descriptor Configuration

- List configuration

  Setting the LE bit in the header of the last descriptor to 1b ends the link.

- Loop configuration

  Setting the address of the first descriptor as the link address for the last descriptor configures the descriptors in a loop. To end the loop, either overwrite the LE bit of the header with 1b before the DMAC reads the descriptor or stop the DMAC according to the transfer suspension procedure.

19.6.2 DMA Transfer

This section describes basic operations of DMA transfer by the DMAC unit.

19.6.2.1 Transfer Mode

As the transfer mode, single-transfer mode and block-transfer mode are supported.

Select the mode by using the TM bit of CHCFG_m per channel.

Use single-transfer mode for normal DMA transfer with the use of the DMAREQm input and block-transfer mode for memory-to-memory transfer, etc., with the use of software activation.

Table 19.6-12 Basic Transfer Setting

Transfer Mode	TM (CHCFG_m)	Function	Usage
Single transfer	0b	A single round of DMA transfer proceeds in response to a single DMAREQ.	Use this mode for DMA transfer with the use of the DMAREQ input.
Block transfer	1b	Transfer proceeds in response to a single software activation until the completion of the DMA transaction.	Use this mode for memory-to-memory transfer with the use of software activation.

(1) Single-Transfer Mode

When a DMA transfer request is received, DMA transfer is executed once in the direction (source or destination) indicated by REQD and DMAACK is asserted. A single round of transfer proceeds every time a transfer request is received and this operation is repeated for the number of bytes loaded to CRTB_m (arbitration between channels proceeds per DMA transfer).

The timing of DMAACK and the timing of counting CRTB vary with the setting of REQD and the transfer size (DDS, SDS). For details, see **Section 19.6.2.8, Differences in Operation with the Transfer Size**.

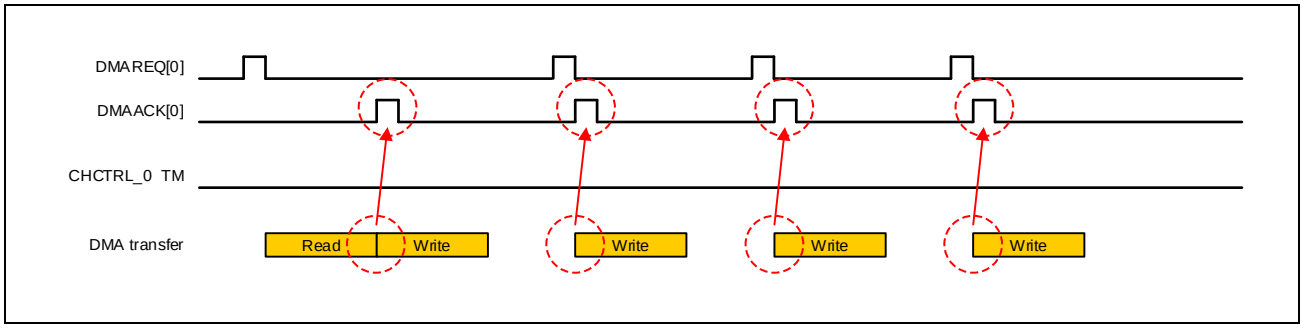


Figure 19.6-10 Single-Transfer Mode (REQD = 1b, SDS > DDS)

(2) Block-Transfer Mode

Once a DMA transfer request is received, transfer continues until a transfer for the number of bytes loaded to the DMA transfer byte register (CRTB_m register) is completed (the completion of the DMA transaction) (arbitration between channels proceeds per DMA transfer).

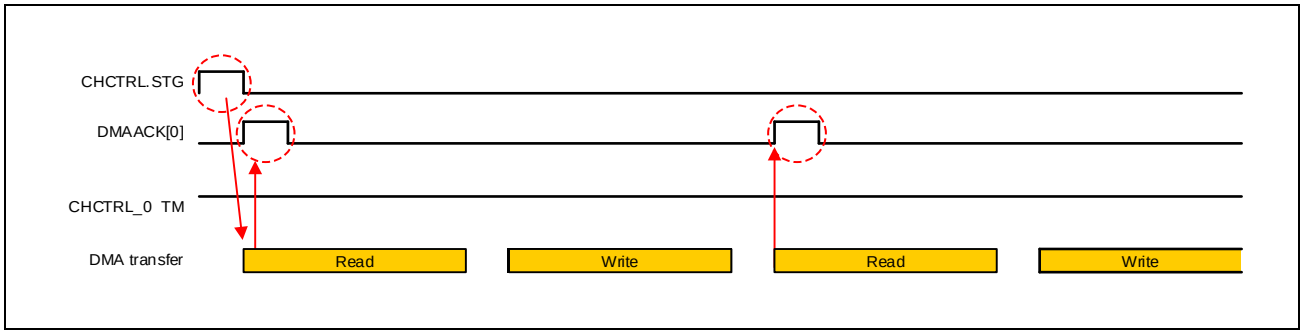


Figure 19.6-11 Block-Transfer Mode (REQD = 0b, SDS < DDS)

19.6.2.2 Control Over the Priority of DMAC Channels

Fixed priority mode and round-robin mode are supported as the order of priority among channels 0 to 7 of DMAC0 and among channels 0 to 7 of DMAC1. The mode is selected by using the PR bit of the DMA control register (DCTRL). When the setting of the PR bit is 0b, operation is in fixed priority mode; when it is 1b, operation is in round-robin mode.

Table 19.6-13 Priority Control Setting

Mode	PR (DCTRL)	Function	Usage
Fixed priority	0b	Controls requests in the fixed priority order (high: CH0 > CH1.> CH2 > CH3 > CH4 > CH5 > CH6 > CH7: low).	Use this mode when channels have the priority order.
Round-robin	1b	Controls requests in round-robin fashion.	Use this mode to execute each request evenly.

Round-robin mode is only supported as the order of priority between DMAC0 and DMAC1. In round-robin mode, the DMAC of DMAC no (which is currently executing transfer) + 1 has the highest priority. After a reset, DMAC0 is given the highest priority.

Table 19.6-14 Priority of Transfer Requests for DMAC during Transfer

Current DMAC \ Next DMAC	DMAC0	DMAC1
DMAC0	2	1
DMAC1	1	2

Note: Priority: 1 (high) ⇔ 2 (low)

The priority of reading and that of writing are controlled independently.

The DMAC issues transfer requests to the individual channels concurrently without waiting for the completion of transfer and handles them in the order the responses are returned. Therefore, the orders in which transactions start and end do not necessarily match.

(1) Fixed Priority Mode

In fixed priority mode, the order of priority among channels 0 to 7 of DMAC0 and among channels 0 to 7 of DMAC1 is fixed. The order of priority between DMAC0 and DMAC1 is round-robin. The order of priority after a reset is as follows.

High D0_CH0 > D1_CH0 > D0_CH1 > D1_CH1 > D0_CH2 > D1_CH2 > D0_CH3 > D1_CH3 > D0_CH4 > D1_CH4 > D0_CH5 > D1_CH5 > D0_CH6 > D1_CH6 > D0_CH7 > D1_CH7 Low

Note: D0 and D1 refer to DMAC0 and DMAC1, respectively.

If a transfer request for channel 0 of DMAC0 is output in this state, transfer by channel 0 of DMAC0 proceeds. The order of priority after the end of transfer is as follows.

High D1_CH1 > D0_CH0 > D1_CH1 > D0_CH1 > D1_CH2 > D0_CH2 > D1_CH3 > D0_CH3 > D1_CH4 > D0_CH4 > D1_CH5 > D0_CH5 > D1_CH6 >D0_CH6 > D1_CH7 > D0_CH7 Low

Note: D0 and D1 refer to DMAC0 and DMAC1, respectively.

If DMA transfer requests are generated on multiple channels simultaneously, the request for a smaller number channel is given priority. The figure below shows an example when another DMA transfer request with higher priority is generated while DMA transfer proceeds in fixed priority mode.

(2) Round-Robin Mode

In round-robin mode, the order of priority is changed so that the channel which has proceeded with the immediately preceding transfer is given the lowest priority every time a transfer among channels 0 to 7 of DMAC0 and among channels 0 to 7 of DMAC1 is accepted.

The order of priority between DMAC0 and DMAC1 is also determined in round-robin.

As with fixed priority mode, the order or priority after a reset is as follows.

High D0_CH0 > D1_CH0 > D0_CH1 > D1_CH1 > D0_CH2 > D1_CH2 > D0_CH3 > D1_CH3 > D0_CH4 > D1_CH4 > D0_CH5 > D1_CH5 > D0_CH6 >D1_CH6 > D0_CH7 > D1_CH7 Low

Note: D0 and D1 refer to DMAC0 and DMAC1, respectively.

If a transfer request for channel 2 of DMAC0 is output in this state, transfer by channel 2 of DMAC0 proceeds. The order of priority after the end of transfer is as follows.

High D1_CH0 > D0_CH3 > D1_CH1 > D0_CH4 > D1_CH2 > D0_CH5 > D1_CH3 > D0_CH6 > D1_CH4 > D0_CH7 > D1_CH5 > D0_CH0 > D1_CH6> D0_CH1 > D1_CH7 > D0_CH2 Low

Note: D0 and D1 refer to DMAC0 and DMAC1, respectively.

19.6.2.3 DMA Transfer Request

Edge detection or level detection is selectable by using the LVL bit of the CHCFG_m register.

The HIEN and LOEN bits of the CHCFG_m register are used to select rising or falling edge for edge detection and the high or low level for level detection.

Table 19.6-15 DMAREQ Pin Selection Setting

SEL[2:0] (CHCFG_m)	Request Pin	Acknowledge Pin	Usage
000b	DMAREQ[0]	DMAACK[0]	Set the DMAC pin to be used for channel n.
001b	DMAREQ[1]	DMAACK[1]	
010b	DMAREQ[2]	DMAACK[2]	
011b	DMAREQ[3]	DMAACK[3]	
100b	DMAREQ[4]	DMAACK[4]	
101b	DMAREQ[5]	DMAACK[5]	
110b	DMAREQ[6]	DMAACK[6]	
111b	DMAREQ[7]	DMAACK[7]	

Table 19.6-16 DMAREQ Detection Setting

Mode	LVL (CHCFG_m)	HIEN (CHCFG_m)	LOEN (CHCFG_m)	Function	Usage
Edge detection	0b	0b	0b	Edge detection cannot be performed in this setting. Select this setting when not using a hardware request.	Set the mode of DMAREQ and the method for detecting rising and falling edges.
			1b	Detection of falling edges of DMAREQm.	
		1b	0b	Detection of rising edges of DMAREQm.	
			1b	Detection of rising and falling edges of DMAREQm.	
Level detection	1b	0b	0b	Level detection cannot be performed in this setting.	
			1b	DMAREQm is detected in the low-level mode.	
		1b	0b	DMAREQm is detected in high-level mode.	
			1b	Transfer starts in response to the SETEN bit of the CHCTRL_m register being set to 1b regardless of the input level of DMAREQm. In this setting, set DMAACK to the mode other than level mode. If level mode is set, the operation will be deadlocked.	

CAUTION

- For the setting for detection of DMAREQ, make the setting to suit the system.
- Make the setting for DMAREQ independently of the setting for DMAACK.

(1) Edge Detection

Edge detection is selected by setting the LVL bit in the CHCFG_m register.

Setting the HIEN bit of the CHCFG_m register to 1 selects rising-edge detection and setting the LOEN bit to 1 selects falling-edge detection.

Make sure that the unit to be connected issues a next DMA transfer request after waiting for detection of DMAACK.

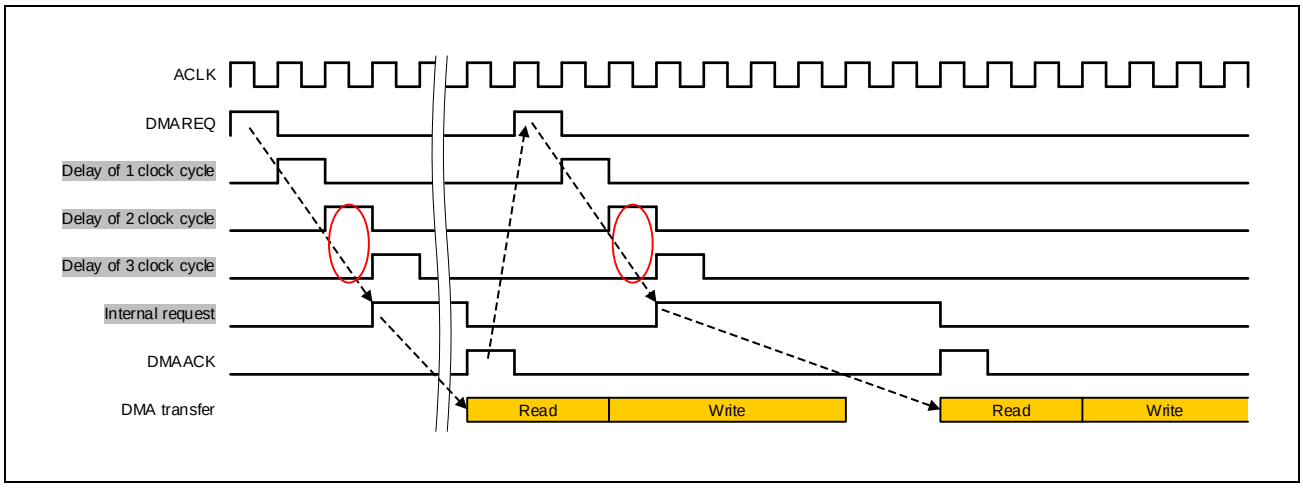


Figure 19.6-12 Edge Detection Timing (HIEN = 1b, REQD = 0b)

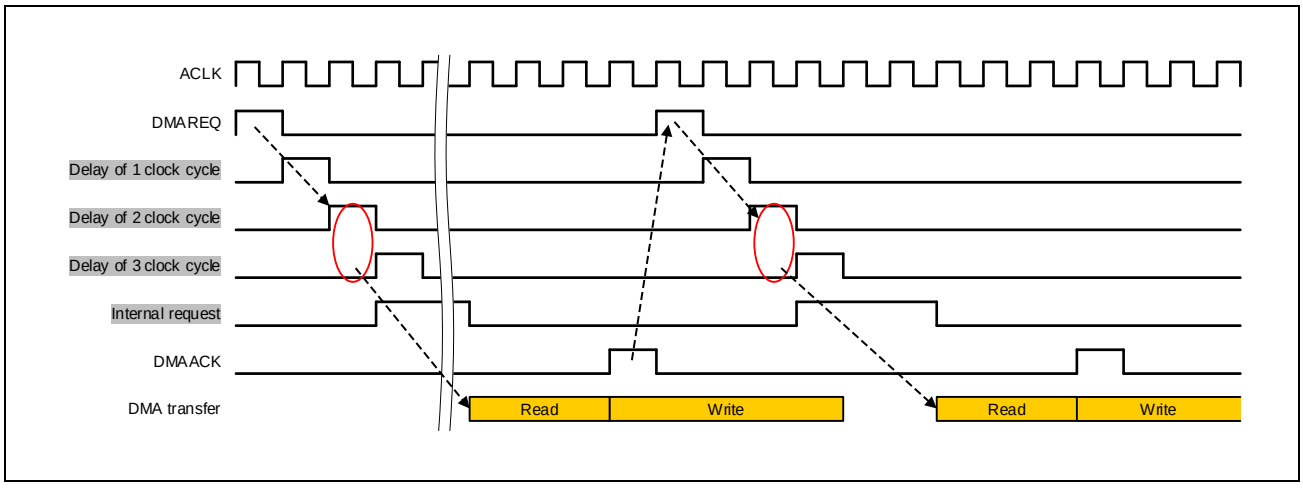


Figure 19.6-13 Edge Detection Timing (HIEN = 1b, REQD = 1b)

(2) Level Detection

Setting the LVL bit of the CHCFG_m register to 1 selects level detection.

If DMAREQ is at the active level (by the setting of HIEN or LOEN) for at least two consecutive clock cycles, it is recognized as a correct DMAREQ.

If DMAACK is set to level mode, DMAACK is at the high level until DMAREQ is de-asserted, so when a next DMA transfer request is to be output, assert DMAREQ after waiting for DMAACK to be de-asserted.

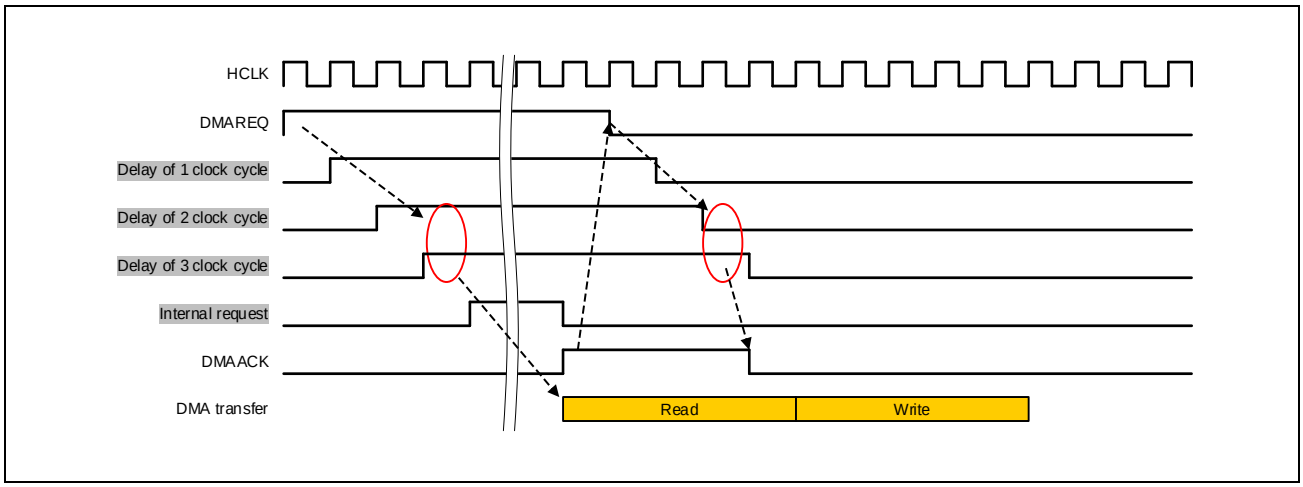


Figure 19.6-14 Level Detection Timing (HIEN = 1b, REQD = 0b, AM[2:0] = 001b)

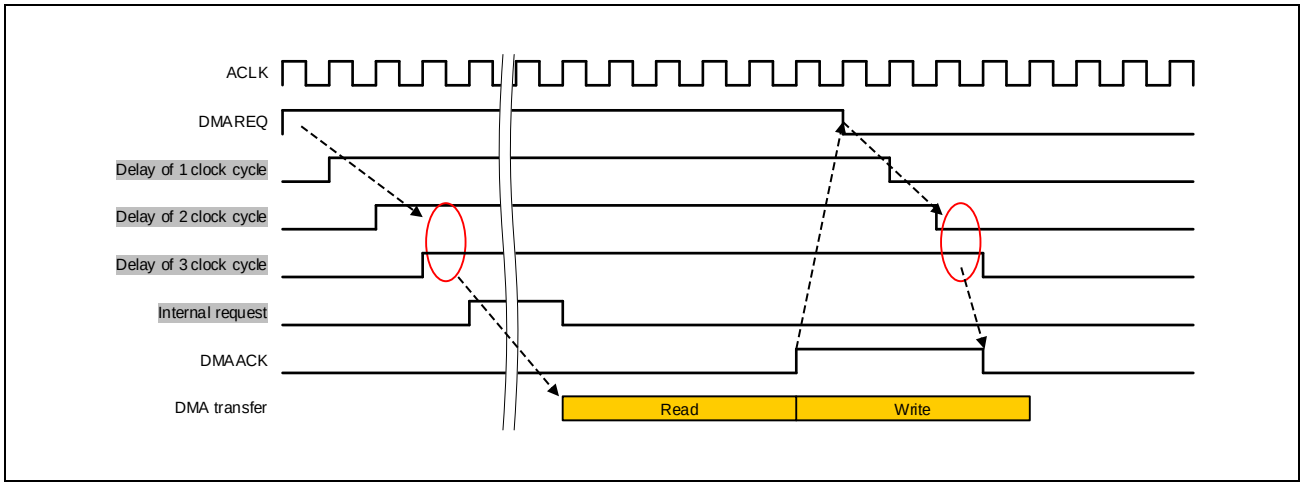


Figure 19.6-15 Level Detection Timing (HIEN = 1b, REQD = 1b, AM[2:0] = 001b)

19.6.2.4 DMA Acknowledge Output

DMAACK[7:0] is an acknowledge signal for the request source that outputs a DMA transfer request. This unit supports pulse output, level output, and bus cycle output to output DMAACK.

The SEL bit of the CHCFG_m register is used to select one from among the eight DMAACK[7:0] outputs per channel (See **Table 19.6-15**).

(1) DMA Acknowledge Signal Output Timing Setting

When the DMA transfer request is accepted, the acknowledge signal becomes active level (high level output). The REQD and AM[2:0] bits of the CHCFG_m register can be used to make the settings as follows.

Table 19.6-17 DMAACK Output Timing Setting

Mode	AM[2] (CHCFG_m)	AM[1:0] (CHCFG_m)	REQD (CHCFG_m)	Usage
Pulse	0b	00b	0b (Active at the time of reading)	DMAACK is output with a pulse. Use this mode when the unit to which DMAACK is connected can receive DMAACK with a pulse.
			1b (Active at the time of writing)	
Level	0b	01b	0b (Active at the time of reading)	DMAACK is output with a level. DMAACK continues to be asserted until DMAREQ is de-asserted. Use this mode when this output is asynchronous with the destination to which DMAACK is connected
			1b (Active at the time of writing)	
Bus cycle	0b	10b 11b	0b (Active at the time of reading)	DMAACK is output during the bus cycle period. Use this mode when DMAACK is to be asserted until the completion of a bus cycle.
			1b (Active at the time of writing)	
Masking	1b	—	—	DMAACK is fixed at the low level. Use this mode when DMAACK is not to be issued to the destination for connection.

(2) Pulse Output

Setting the AM bits of the CHCFG_m register to 000 selects pulse output.

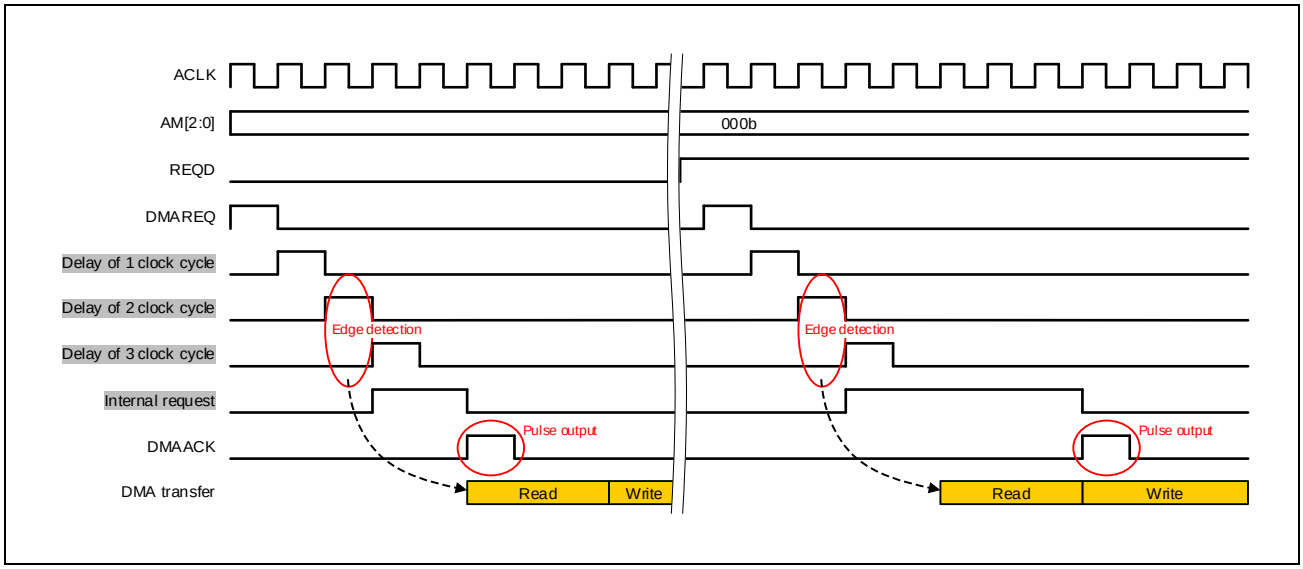


Figure 19.6-16 DMAACK Output Timing (AM[2:0] = 000b, LVL = 0b)

When REQD = 0b, DMAACK is asserted when a bus cycle for reading starts.

When REQD = 1b, DMAACK is asserted when a bus cycle for writing starts.

(3) Level Output

Setting the AM bits of the CHCFG_m register to 001 selects level output. DMAACK continues to be asserted until DMAREQ is de-asserted.

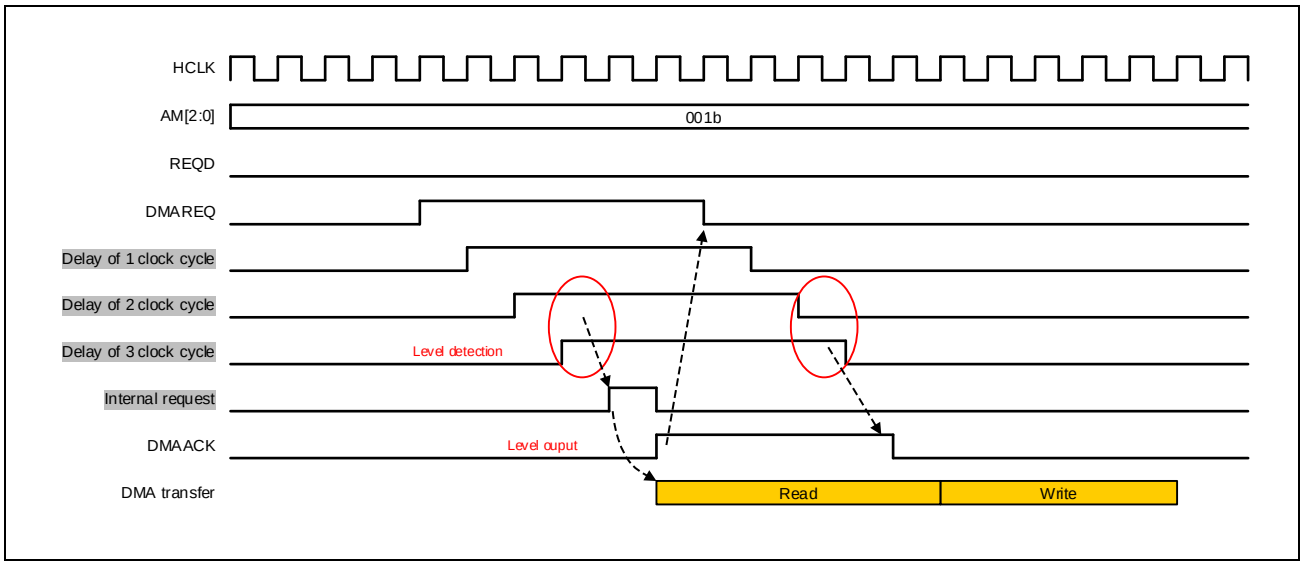


Figure 19.6-17 DMAACK Output Timing (AM[2:0] = 001b, LVL = 1b, REQD = 0b)

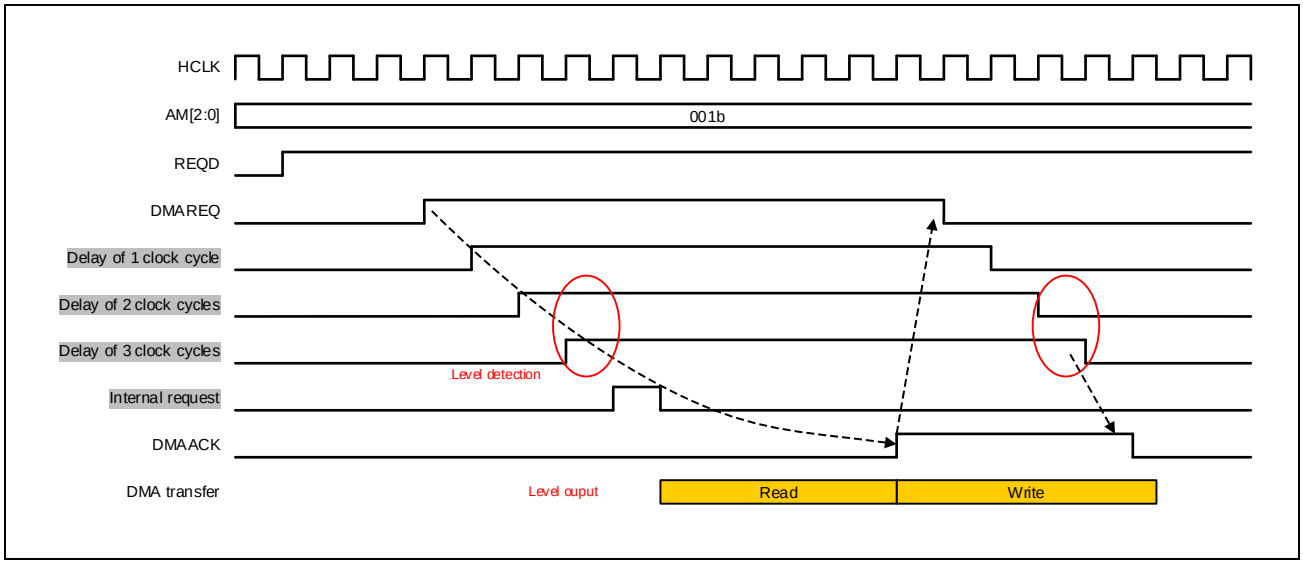


Figure 19.6-18 DMAACK Output Timing (AM[2:0] = 001b, LVL = 1b, REQD = 1b)

(4) Bus Cycle Output

Setting the AM bits of the CHCTRL_m register to 010 selects bus cycle output. DMAACK is at the active level during the bus cycle period.

DMAREQ is masked within this unit while DMAACK is at the active level. Accordingly, even if DMAREQ is set for level detection, the output side does not need to de-assert it once.

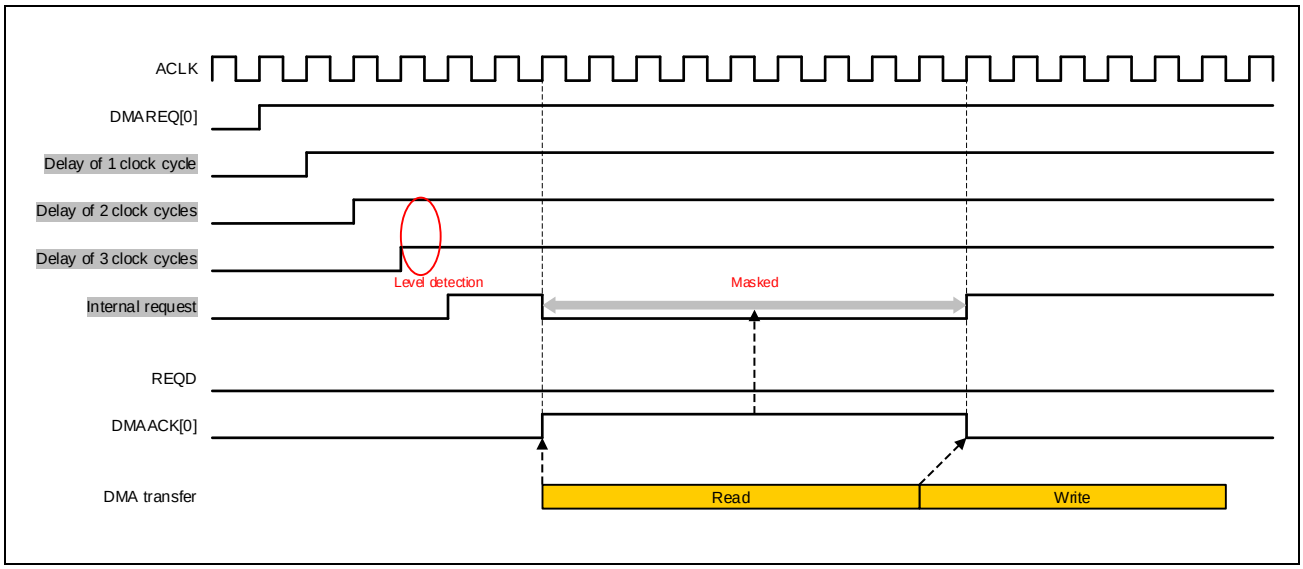


Figure 19.6-19 Bus Cycle Output Timing (AM[2:1] = 01b, LVL = 1b, REQD = 0b)

- When the signal is at the active level at the time of reading (REQD = 0b), DMAACK is at the active level during the period from the start of the read cycle to one cycle after the end of the read cycle.
  - Start of the read cycle: MARVALID = 1b
  - End of the read cycle: MRVALID & MRLAST & MRREADY = 1b

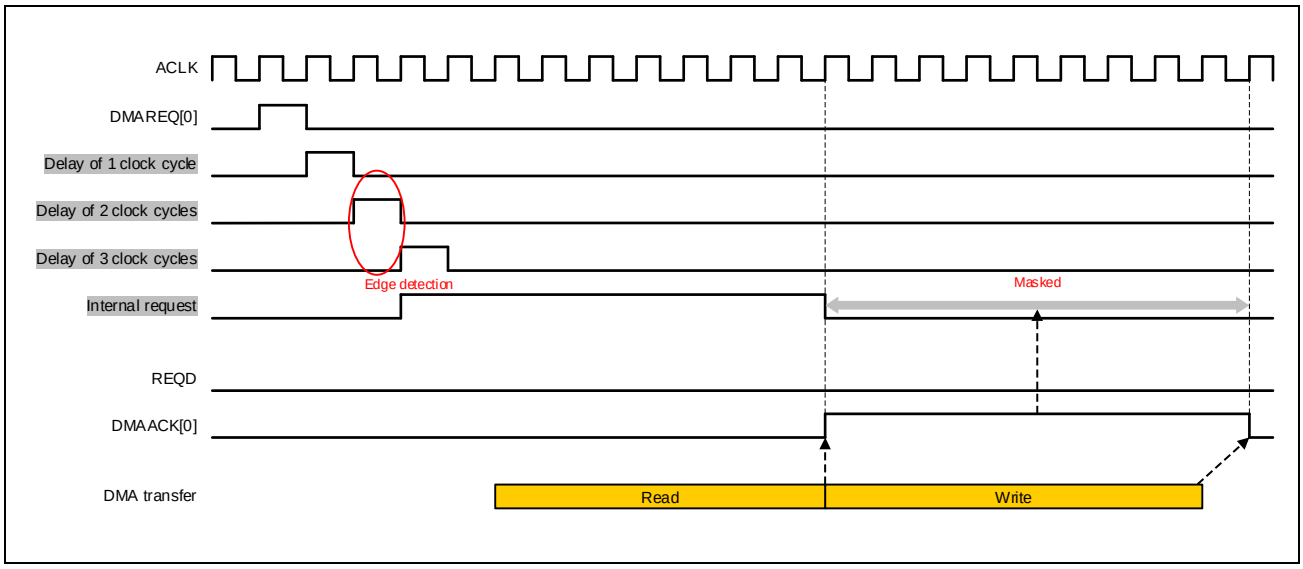


Figure 19.6-20 Bus Cycle Output Timing (AM[2:1] = 01b, LVL = 0b, REQD = 1b)

- When the signal is at the active level at the time of writing (REQD = 1b), DMAACK is at the active level during the period from the start of the write cycle to one cycle after the end of the write cycle.
  - Start of the write cycle: MAWVALID = 1b
  - End of the write cycle: MBVALID & MBREADY = 1b

19.6.2.5 DMA Transfer Completed Interrupt

DMAEND[7:0] are interrupt request signals that indicate the completion of a DMA transaction.

Each bit of DMAEND[7:0] corresponds to a respective channel.

If a transfer for the total number of transfer bytes loaded to CRTB (Current Transaction Byte) is completed with an OKAY response, END of the CHSTAT_m register is set to 1b. If DEM of the CHCFG_m register = 0b at this time, the high level is output from the DMAEND[n] pin (n = 7 to 0) (when write-back proceeds in link mode, the high level is output after the completion of write-back).

In link mode, if LV = 0b in the header of the descriptor that has been read, DER of the CHSTAT_m register is set to 1b. If DIM of the header = 0 at this time, the high level is output from the DMAEND[n] pin.

Use this signal for detection of a transfer completed interrupt by the interrupt controller.

Table 19.6-18 DMAEND Assertion Conditions

Source	Condition	DMAEND[n] Mask Signal
Completion of the DMAC transaction	A transfer for the total number of transfer bytes loaded to CRTB (current transaction byte) being completed with an OKAY response (after the completion of write-back if write-back proceeds in link mode).	DEM bit of the CHCFG_m register
Descriptor invalid	In link mode, LV = 0b in the header of the descriptor that has been read while DIM of the header = 0b.	DIM bit of the header

19.6.2.6 DMA Error Interrupt (DMAERR)

If an error response is received in DMA transfer and descriptor access, this unit judges this to be an error and stops transfer. If an error response is received, the EN bit of the CHSTAT_m register for channel n during transfer is cleared to 0 and the ER bit is set to 1b (n = 0 to 7). Also, the high level is output from the DMAERR pin (on the other hand, DMAERR is not output if an error occurs in access to a slave of this unit).

The DMAERR signal cannot be masked.

The series of transfers which causes the error does not guarantee that data. Be sure to start transfer over again from the beginning by following the procedure below.

1. Set the SWRST bit of the CHCTRL_m register to 1b.
2. Re-set each register.

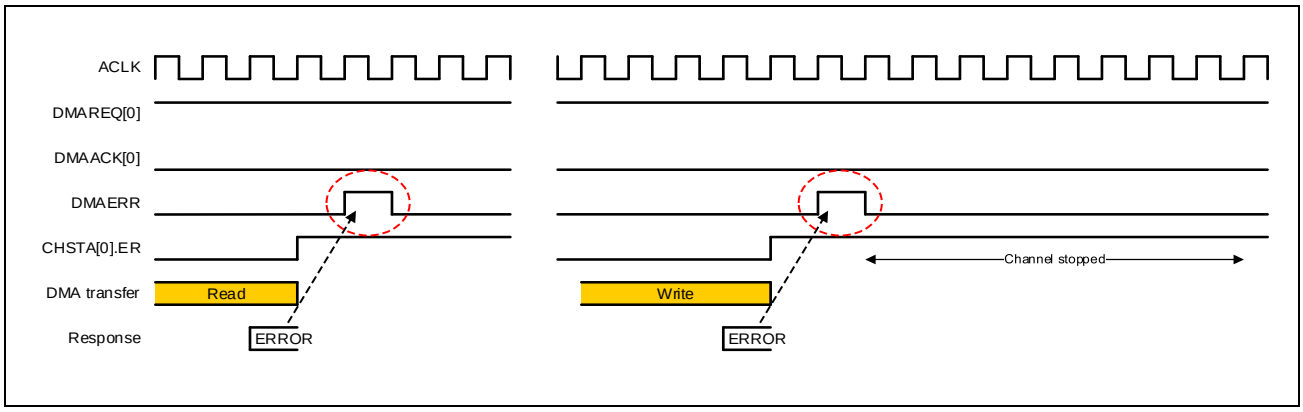


Figure 19.6-21 Timing of Stopping Transfer by an Error Response (ERROR)

19.6.2.7 Interval Counting

The interval between the execution of DMA transfers can be adjusted by the setting of the ITVL bit of the channel interval register (CHITVL_m). This functionality is intended to make sure that the DMA controller does not occupy the bus.

When one round of reading or writing is completed, counting down starts from the value set in CHITVL_m. A next internal request is not executed until the value counted reaches to 0.

The figure below shows an example of operations.

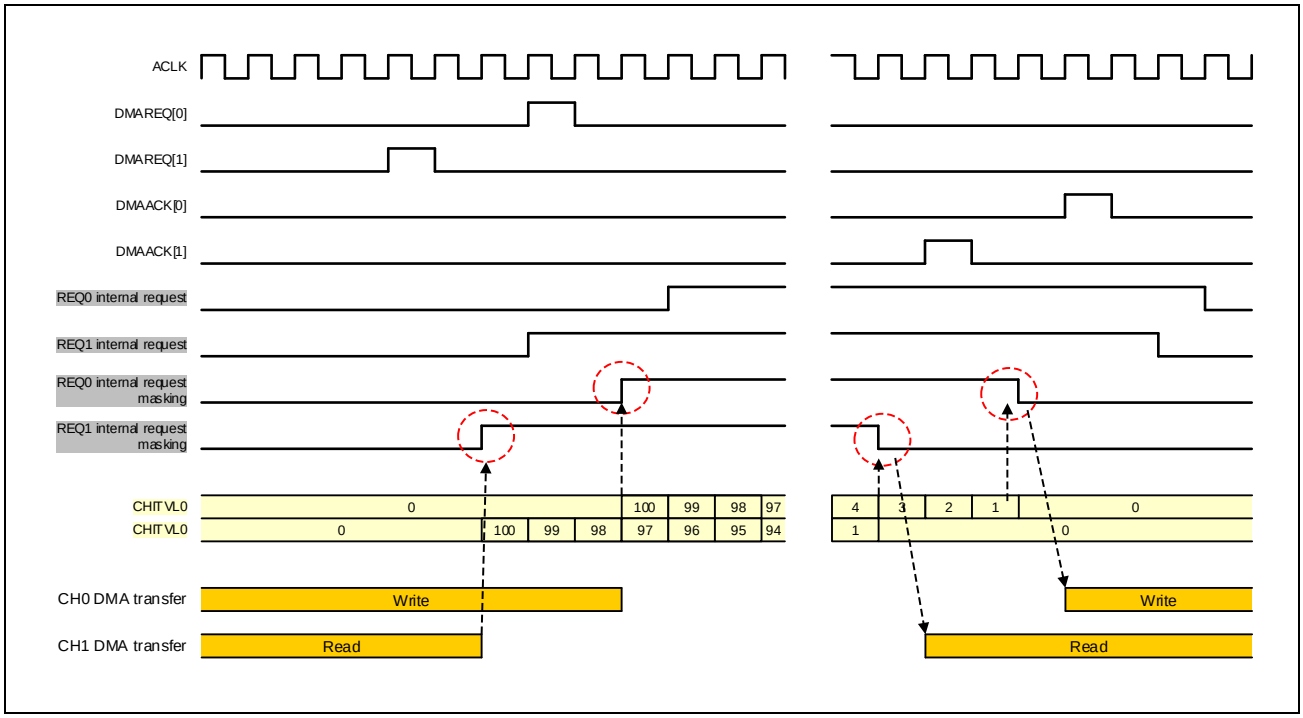


Figure 19.6-22 Interval Counting

19.6.2.8 Differences in Operation with the Transfer Size

(1) When the Transfer Size of the Source is Small

When reading of data corresponding to the destination transfer size is completed, writing to the destination proceeds.

The figure below is a timing chart when the transfer size of the source is 8 bits and that of the destination is 32 bits (in the case of rising-edge detection).

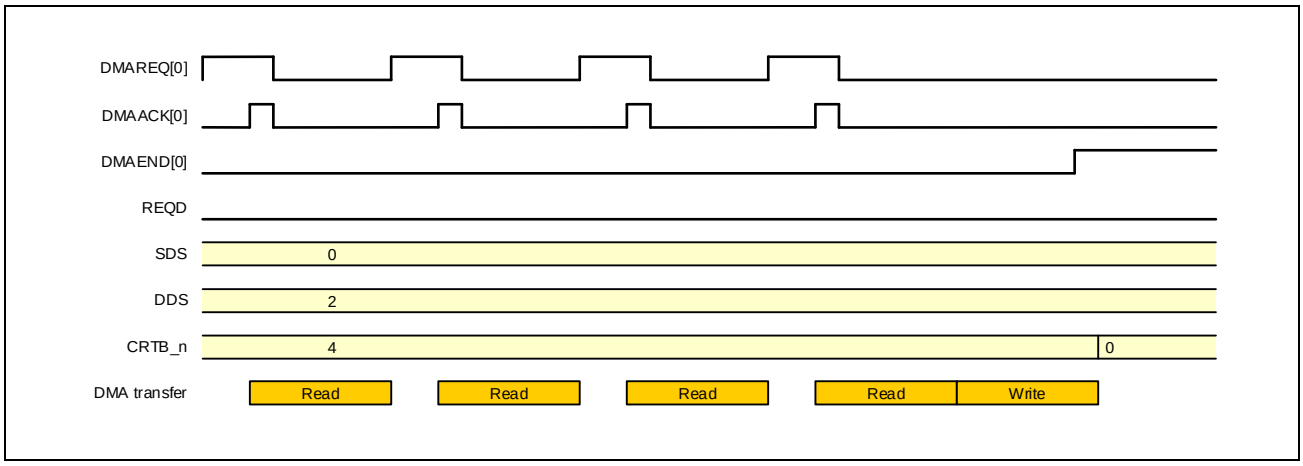


Figure 19.6-23 When the Transfer Size of the Source is Small (LVL of CHCFG_m = 0b, HIEN = 1b, REQD = 0b, SDS < DDS)

(2) When the Transfer Size of the Destination is Small

Since the transfer size of the source is larger than that of the destination, after reading from the source once, writing to the destination proceeds several times. The figure below is a timing chart when the transfer size of the source is 64 bits and that of the destination is 16 bits (in the case of rising-edge detection and (REQD of the CHCFG_m register is set to 1).

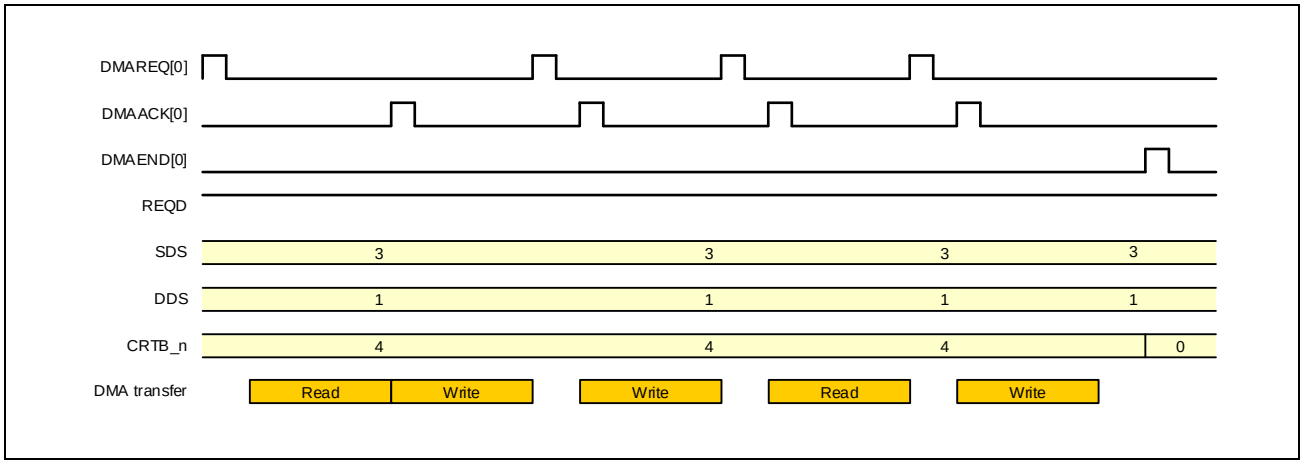


Figure 19.6-24 When the Transfer Size of the Destination is Small (LVL of CHCFG_m = 0b, HIEN = 1b, REQD = 1b, SDS > DDS)

(3) When the Transfer Sizes of the Source and Dstination are the Same

Reading from the source and writing to the source proceed every time a DMA transfer request is detected.

The figure below is a timing chart when the transfer sizes of the source and destination are 8 bits (in the case of rising-edge detection and when REQD of the CHCFG_m register is set to 1b).

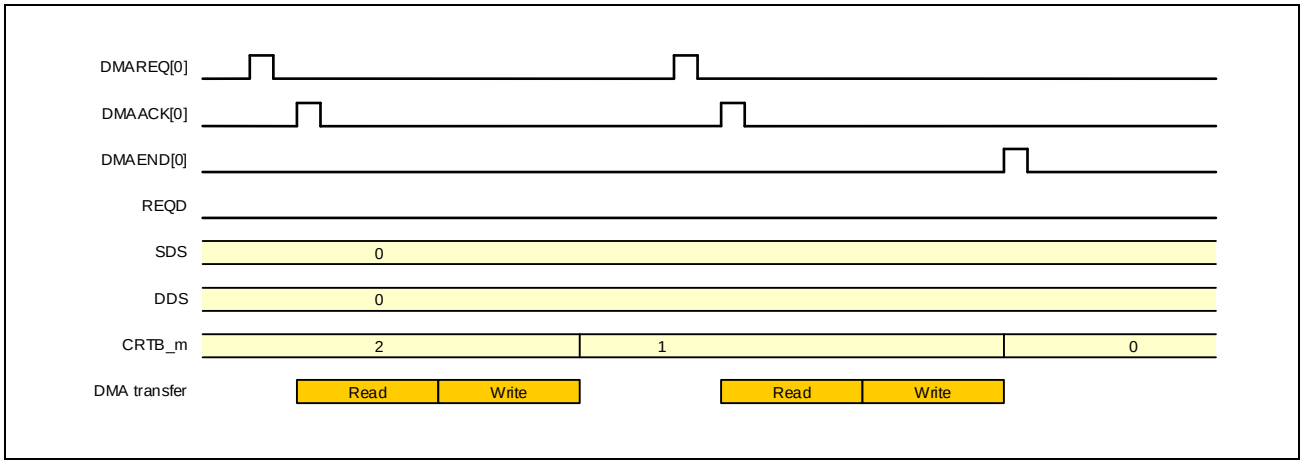


Figure 19.6-25 When the Transfer Sizes of the Source and Destination are the Same (LVL of CHCFG_m = 0b, HIEN = 1b, REQD = 0b, SDS = DDS)

19.6.2.9 Transfer State

The channel status register indicates the DMA transfer state of the channel.

(1) Transfer State

The transfer state is indicated by TACT as shown below.

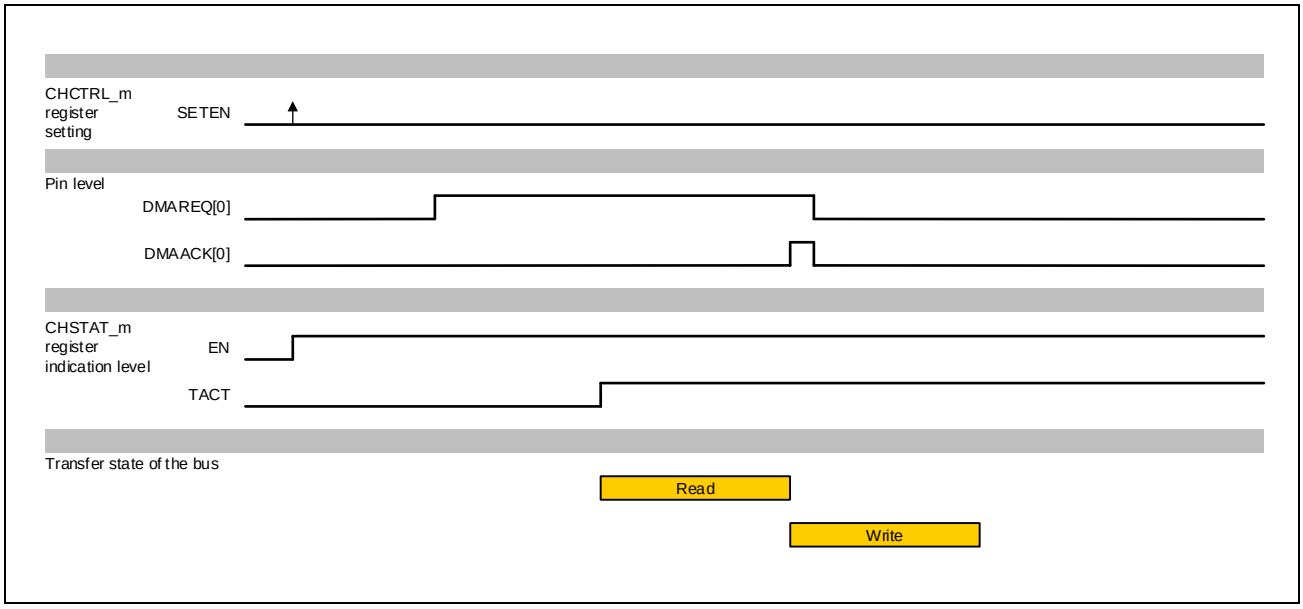


Figure 19.6-26 DMAC State Example 1 (Hardware Request)

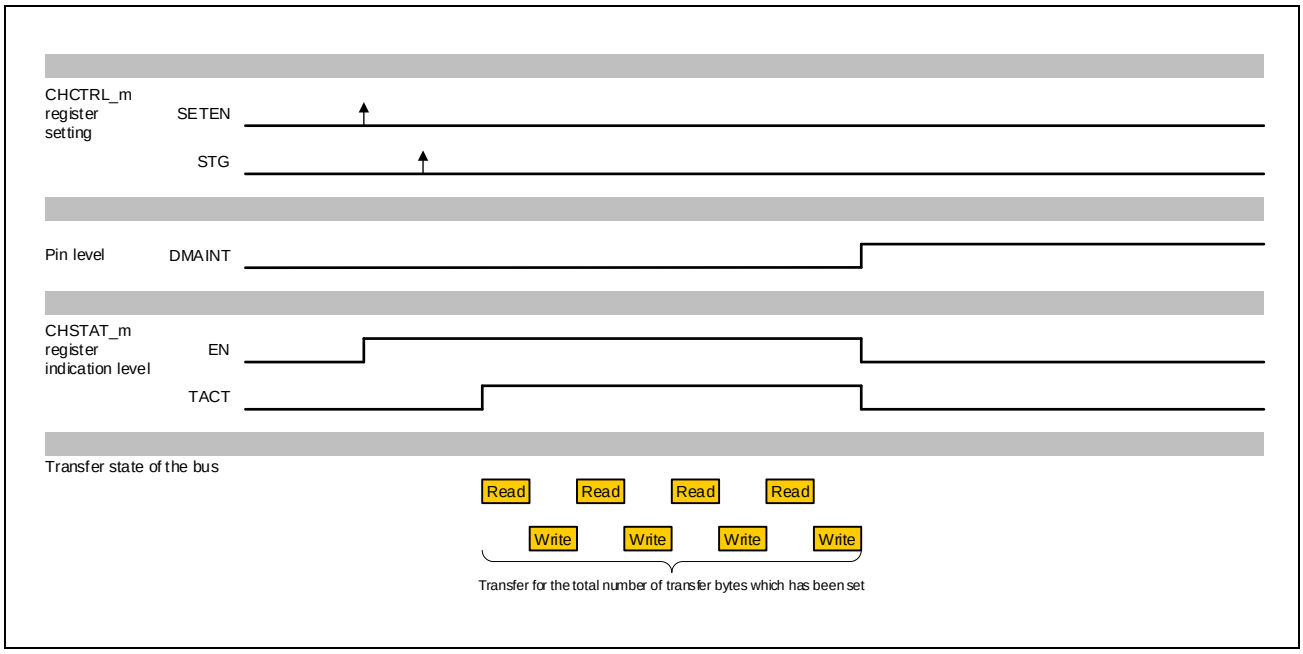


Figure 19.6-27 DMAC State Example 2 (Software Request)

(2) Suspension

The SETSUS bit of CHCTRL_m can be used to suspend DMA transfer. At that time, if the bus cycle is already is in progress, the DMAC is suspended after waiting for the completion of the cycle. It can be resumed from the suspended state by writing 1b to the CLRSUS bit.

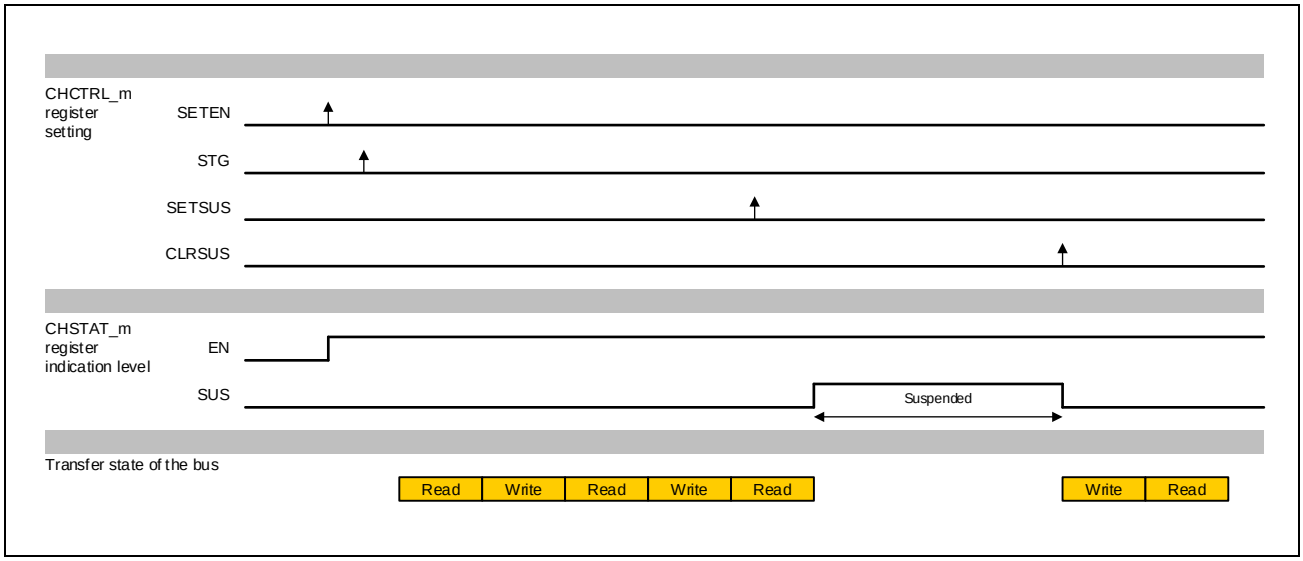


Figure 19.6-28 DMAC Suspended State (Block Transfer by Software Request)

In the above case, the DMAC is suspended at the time read transfer is completed.

If the DMAC has already executed transfer, it is suspended at the time that transfer is completed. To confirm that the transfer is suspended, set SETSUS and then check that the SUS bit for the corresponding channel is 1b by reading the CHSTAT or DST_SUS register.

(3) Aborting Transfer

Writing 1 to CLREN during the DMA transaction aborts the DMA transaction by the corresponding channel. As processing after the transaction has been aborted, select either of the following modes by using the SBE bit in the CHCFG_m register: the mode where the data remaining in the buffer are flushed at the time the transaction is aborted (SBE = 1b) and the mode where the data are not flushed (SBE = 0b). By default, SBE = 0b.

When the transfer in progress is aborted by setting CLREN to 1b while this flushing mode is enabled, if data remain in the buffer of the DMAC, that data are flushed before the transaction is completed.

(a) Aborting Transfer (No Buffer Flushing: SBE = 0b)

When CLREN is set during DMA transfer, the DMA transfer is aborted and then stopped. The timing of stopping the transfer depends on the value set in REQD. After the transfer has been stopped, be sure to clear the internal state of the DMAC before making the settings for next transfer.

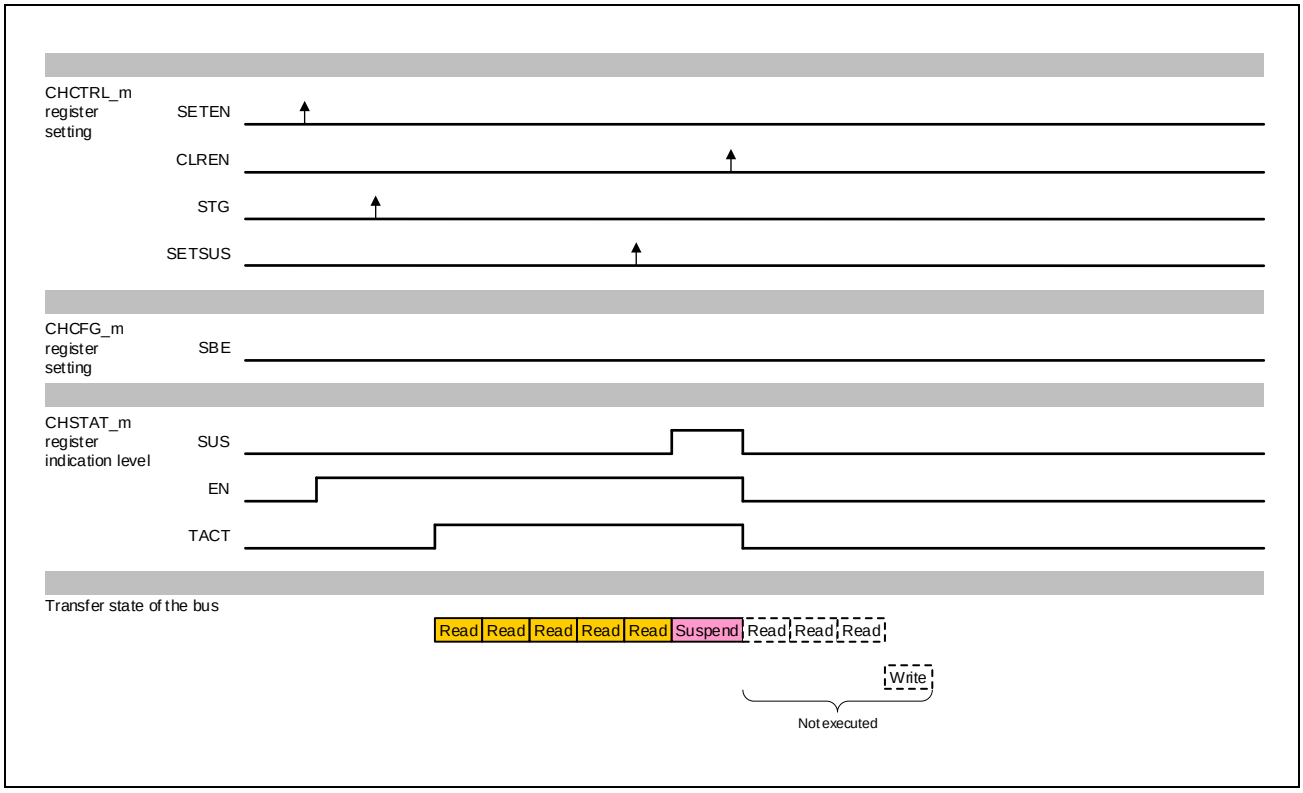


Figure 19.6-29 Aborting DMA Transfer

- Complete stopping of the channel can be confirmed at the time the TACT bit is cleared.
- If the DMA transfer in progress is aborted, the DMAEND pin is not asserted.
- If REQD = 0b, the transfer is stopped at the time next reading is completed. Note that if the buffer contains data that can be written, the transfer is stopped after the data are written.
- If REQD = 1b, the transfer is stopped at the time next writing is completed.

(b) Aborting Transfer (with Buffer Flushing: SBE = 1b)

Setting CLREN during DMA transfer aborts the DMA transfer. If REQD = 0b, data that have already been read are flushed (written) and then the DMA transfer is stopped. After the transfer has been stopped, set SWRST and clear the internal state of the DMAC before making the settings for next transfer.

If flushing mode is used when a hardware request is in use while REQD = 1b, data that have been read in advance may be written, so only use this mode while REQD = 0b.

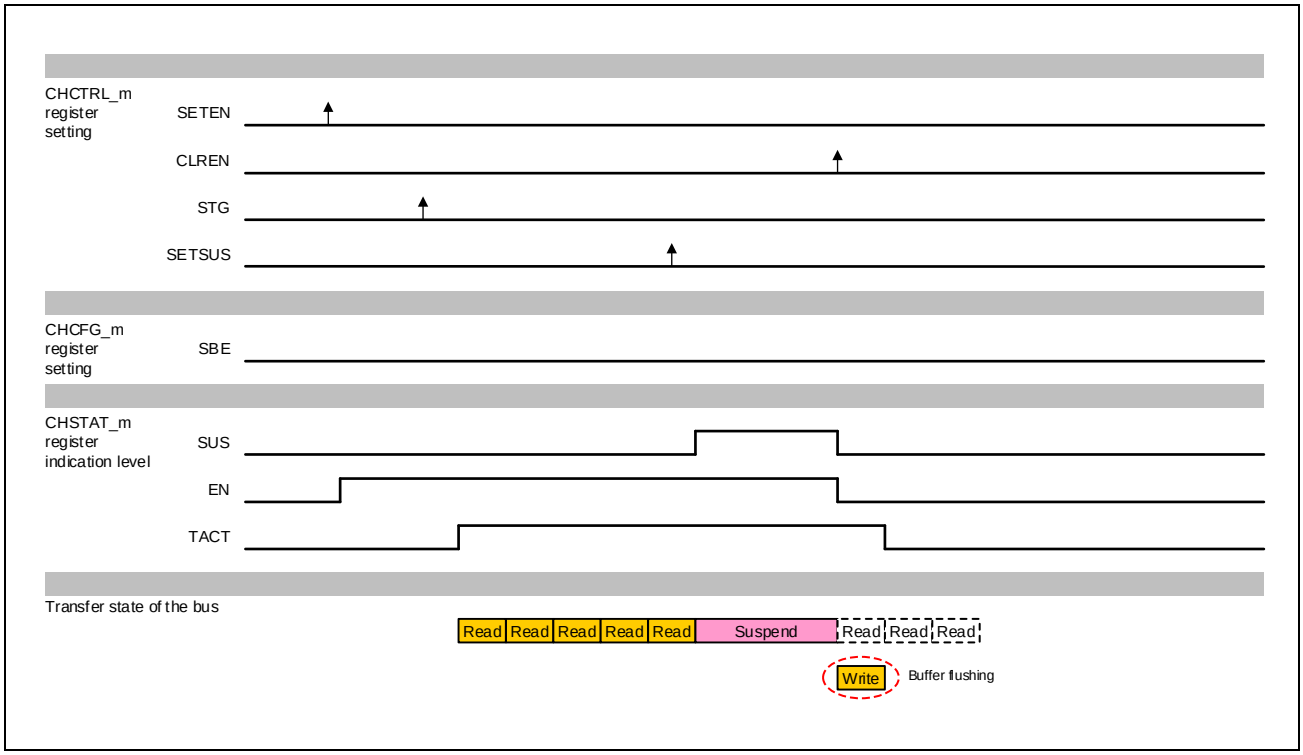


Figure 19.6-30 Aborting DMA Transfer (Buffer Flushing Mode)

- Complete stopping of the channel can be confirmed at the time the TACT bit is cleared.
- If the transfer is aborted during the fifth read transfer in flushing mode (SBE = 1b), the DMAC is stopped after writing the data that have been read.

(c) Checking stopping of the channel

Even if the EN bit is cleared to 0, the DMAC cannot be stopped immediately if transfer has already been executed on the bus. Accordingly, to confirm that the DMAC has been stopped completely, check that both the EN and TACT bits are 0b.

(d) Procedure for aborting transfer

The following describes the procedure for stopping transfer.

1. Set SETSUS of CHCTRL_m.

2. Poll the SUS bit of CHSTAT_m until it becomes 1 (if EN is already 0b at this time, proceed to step 6 because the DMAC has been stopped).

3. Set CLREN of CHCTRL_m.

4. If SBE = 0b, the DMAC is stopped according to the value of REQD, and if SBE = 1b, the data are flushed. If the setting of SBE = 1b, set REQD = 0b beforehand.

5. Read CHSTAT_m to check that the TACT bit is 0b. TACT = 0b means that the DMAC has been stopped completely. If TACT = 1b, poll this bit until it becomes 0b.

6. To proceed with a next DMA transfer after aborting the transfer, be sure to set the SWRST (software reset) bit of CHCTRLn before the next transfer starts.

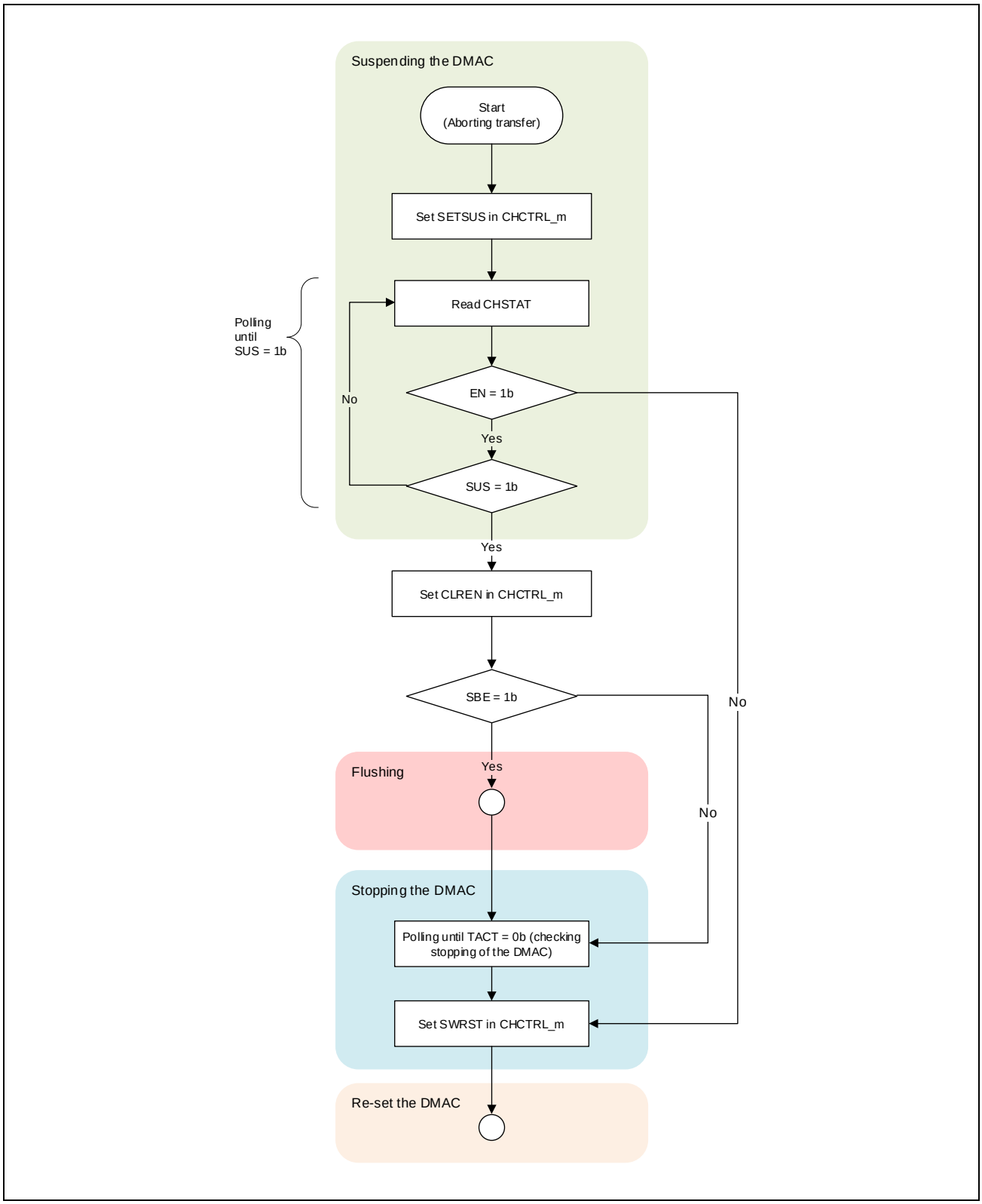


Figure 19.6-31 Flow of Aborting Transfer

19.6.3 AXI Address Conversion

Two bank switching address bits input by SYS are appended to the higher-order bits of the AXI master addresses to extend them to 34-bit master addresses, which makes a 16-GB address space accessible.

Since three bank switching addresses for the source, destination, and descriptor are input per DMAC number and channel number, the source, destination, and descriptor areas can be set in separate 4-GB address spaces.

Bank switching addresses are set by using the registers of the SYS unit.

The figure below shows an example of access to the 16-GB address space.

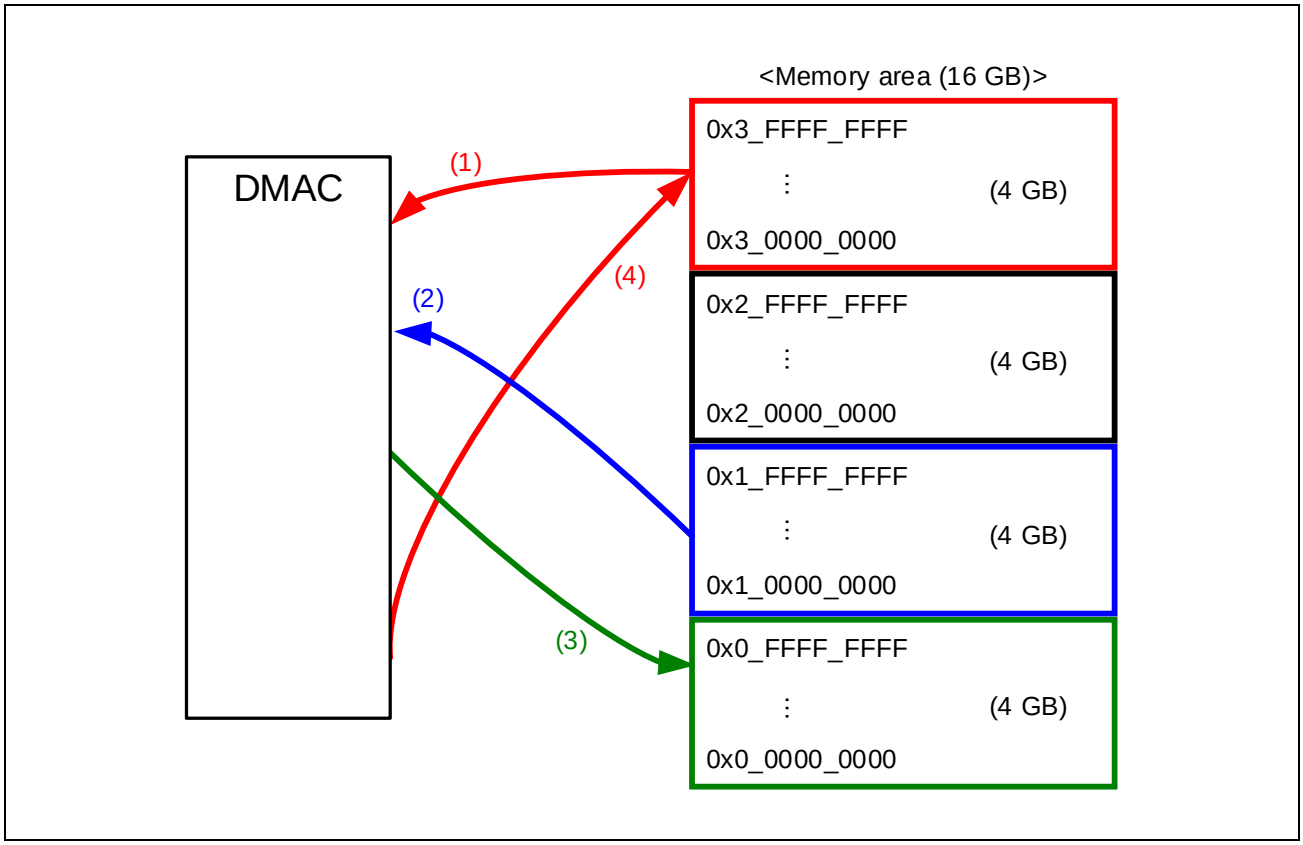


Figure 19.6-32 Example of Access to the 16-GB Address Space

(1) Descriptor read

- Access to a desired 4-GB address space is possible by setting the bank switching address (for the descriptor) for the corresponding DMAC number and channel.
- In the example of the above figure, the setting is 3.
- Setting is only required when link mode is in use.

(2) DMA transfer (source data read)

- Access to a desired 4-GB address space is possible by setting the bank switching address (for the source) for the corresponding DMAC number and channel.
- In the example of the above figure, the setting is 1.

(3) DMA transfer (destination data write)

- Access to a desired 4-GB address space is possible by setting the bank switching address (for the destination) for the corresponding DMAC number and channel.
- In the example of the above figure, the setting is 0.

(4) Descriptor write-back

- The same area as that in step 1.

19.6.3.1 Prohibited Items

This function has the following prohibited items.

- Changing a bank switching address value for a DMAC number and channel that is currently operating is prohibited.
- Usage that spans the 4-GB boundaries is prohibited.

19.7 Operating Procedure

For the individual setting procedures, see the following. The following gives supplementary information.

19.7.1 Example DMAC Settings

This section describes example settings when DMA transfer is to proceed with the use of the DMAC unit.

The conditions for transfer with the individual example settings are listed below.

Table 19.7-1 List of the Conditions for Transfer with Example DMA Transfer Settings

	DMA Mode	Transfer Mode	Transfer Request
Example setting 1	Register	Single	Hardware
Example setting 2	Register	Block	Software
Example setting 3	Register (continuous execution)	Block	Software
Example setting 4	Link	Block	Software

For details of the settings, see the individual example settings.

19.7.1.1 Example Setting 1 (Hardware Request in Register Mode)

The table below lists the settings when DMA transfer is to proceed with example setting 1.

Table 19.7-2 Example Setting 1 for DMA Transfer

Item		Description	
Channel to be used		3	
DMA mode		Register	
Transfer mode		Single transfer	
Register set to be used		Next0	
Transfer source/destination		Transfer source	Transfer destination
	Start address	1111_0000h	2222_0000h
	Address direction	Incremental	Incremental
	Transfer size	32 bits	32 bits
Number of bytes for DMA transfer		64 bytes	
DMAREQ/ACK/TCO		Select DMAREQ[3] and DMAACK[3].	
DMA transfer request		Rising-edge detection by hardware (the DMAREQ[3] pin)	
DMAACK signal		Pulse output at the time of reading	
DMAEND masking		No	
AXI setting (PROT, CACHE)		Initial value	

Example Setting 1

N0SA = 1111_0000h (Transfer source address)

N0DA = 2222_0000h (Transfer destination address)

N0TB = 0000_0040h (Number of transfer bytes)

CHCFG = 0002_2023h (Configuration)

CHITVL = 0000_0000h (Interval)

CHEXT = 0000_0000h (AXI setting)

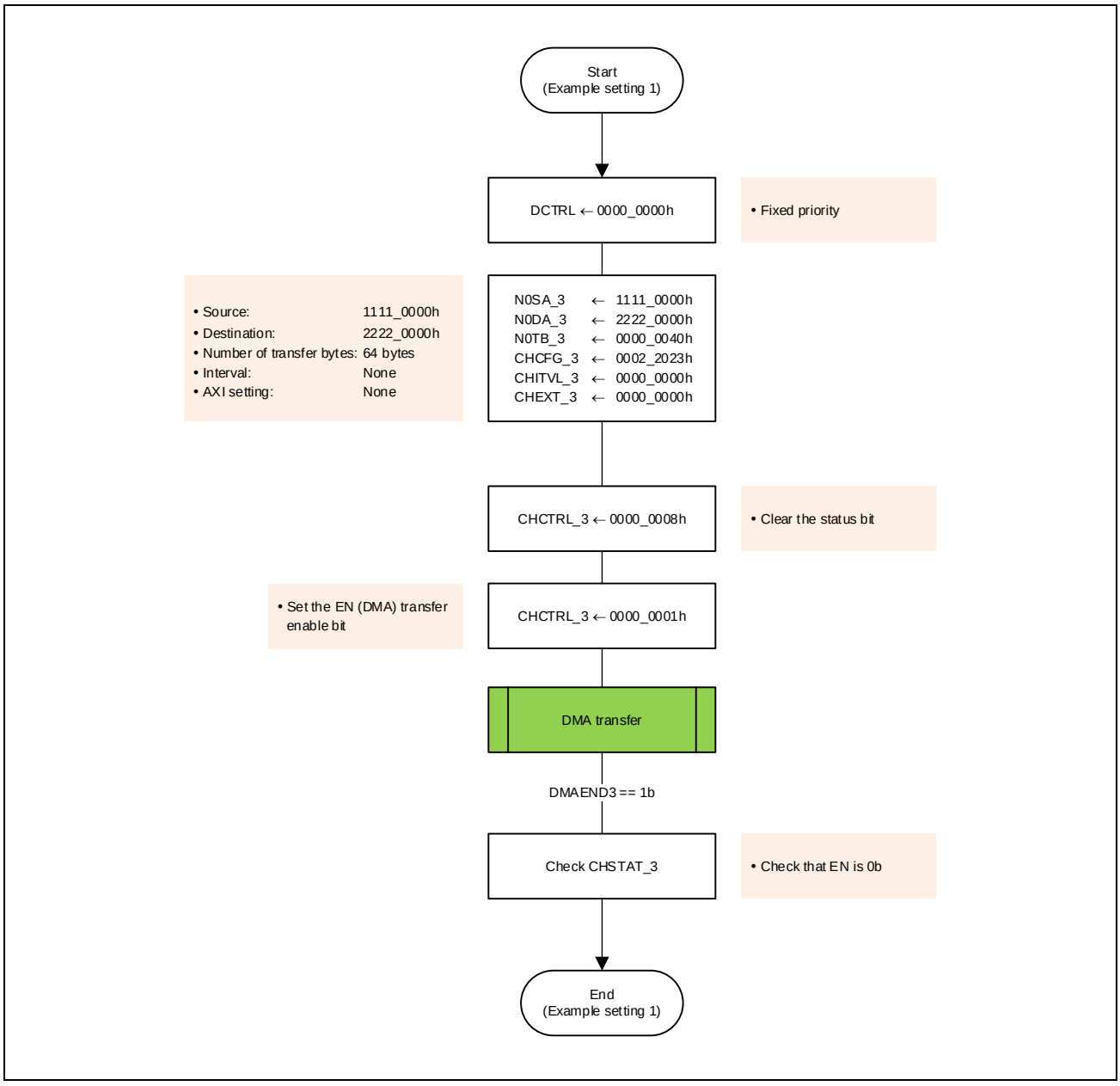


Figure 19.7-1 Example Setting 1

19.7.1.2 Example Setting 2 (Software Request in Register Mode)

The table below lists the settings when DMA transfer is to proceed with example setting 2.

Table 19.7-3 Example Setting 2 for DMA Transfer

Item		Description	
Channel to be used		2	
Priority control		Round-robin	
DMA mode		Register	
Transfer mode		Block transfer	
Register set to be used		Next1	
Transfer source/destination		Transfer source	Transfer destination
	Start address	0FFF_E000h	3333_0000h
	Address direction	Incremental	Incremental
	Transfer size	8 bits	256 bits
Number of bytes for DMA transfer		128 bytes	
DMAREQ/ACK/TCO		Select DMAREQ[7] and DMAACK[7].	
DMA transfer request		Software request	
DMAACK signal		Masking	
DMAEND masking		No	
AXI setting (PROT, CACHE)		Initial value	

Example Setting 2

DCTRL = 0000_0001h (DMAC setting)

N1SA = 0FFF_E000h (Transfer source address)

N1DA = 3333_0000h (Transfer destination address)

N1TB = 0000_0080h (Number of transfer bytes)

CHCFG = 1045_0407h (Configuration)

CHITVL = 0000_0000h (Interval)

CHEXT = 0000_0000h (AXI setting)

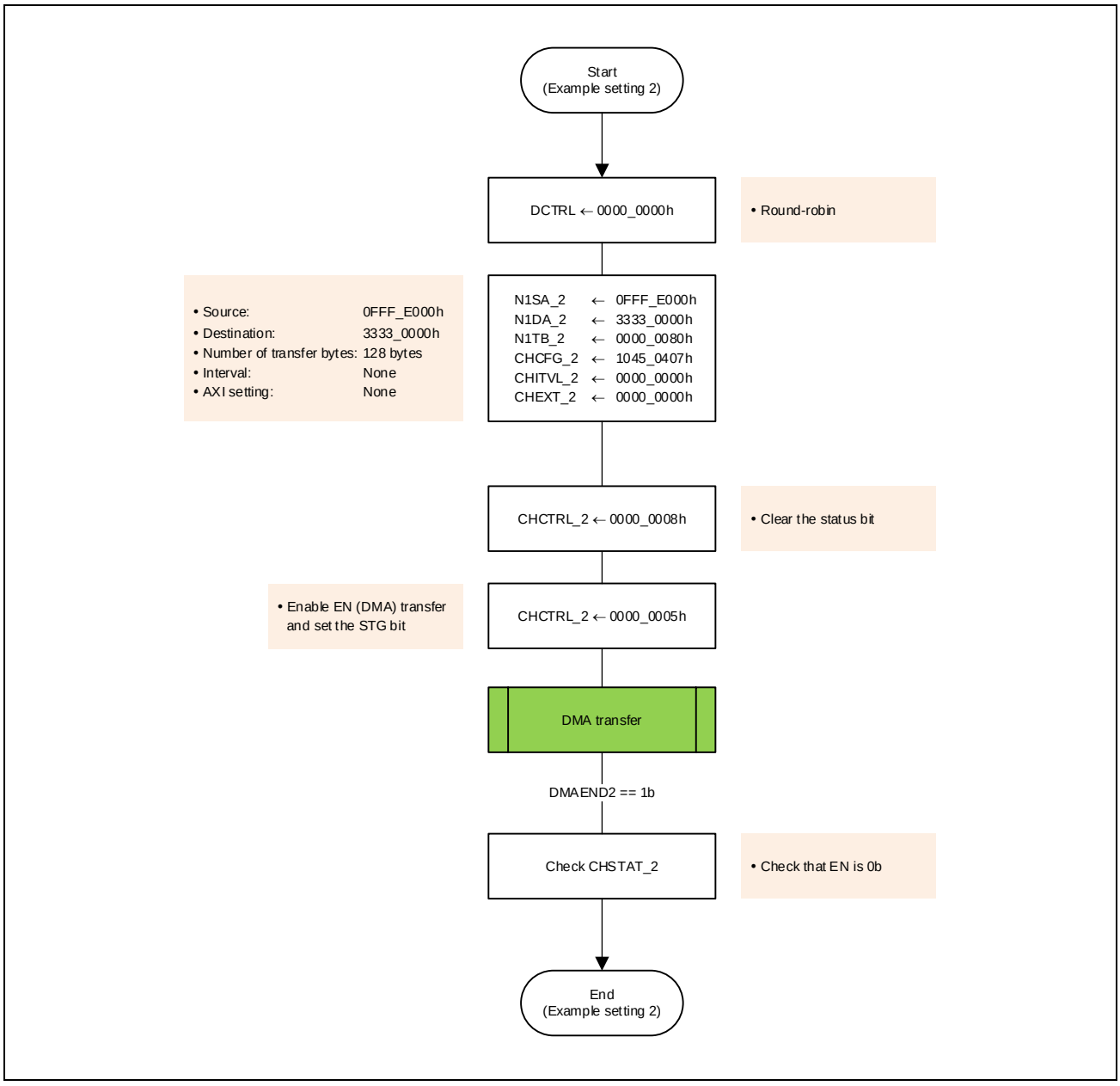


Figure 19.7-2 Example Setting 2

19.7.1.3 Example Setting 3 (Continuous Execution in Register Mode)

The table below lists the settings when DMA transfer is to proceed with example setting 3.

Table 19.7-4 Example Setting 3 for DMA Transfer

Item		Description	
Channel to be used		1	
Priority control		Round-robin	
DMA mode		Register	
Transfer mode		Block transfer	
Register set to be used		Continuous from Next0 to Next1	
Next0		Transfer source	Transfer destination
	Start address	1111_0000h	3333_0000h
	Address direction	Fixed	Fixed
	Transfer size	32 bits	512 bits
	Number of bytes for DMA transfer	512 bytes	
Next1		Transfer source	Transfer destination
	Start address	2222_0000h	4444_0000h
	Address direction	Fixed	Fixed
	Transfer size	32 bits	512 bits
	Number of bytes for DMA transfer	2048 bytes	
DMAREQ/ACK/TCO		Select DMAREQ[7] and DMAACK[7].	
DMA transfer request		Software request	
DMAACK signal		Not output	
DMAEND masking		Masking DMAEND on completion of Next0	
AXI setting (PROT, CACHE)		Initial value	

Example Setting 3

DCTRL = 0000_0001h (DMAC setting)

N0SA = 1111_0000h (Transfer source address)

N0DA = 3333_0000h (Transfer destination address)

N0TB = 0000_0200h (Number of transfer bytes)

N1SA = 2222_0000h (Transfer source address)

N1DA = 4444_0000h (Transfer destination address)

N1TB = 0000_0800h (Number of transfer bytes)

CHCFG = 6176_2007h (Configuration)

CHITVL = 0000_0000h (Interval)

CHEXT = 0000_0000h (AXI setting)

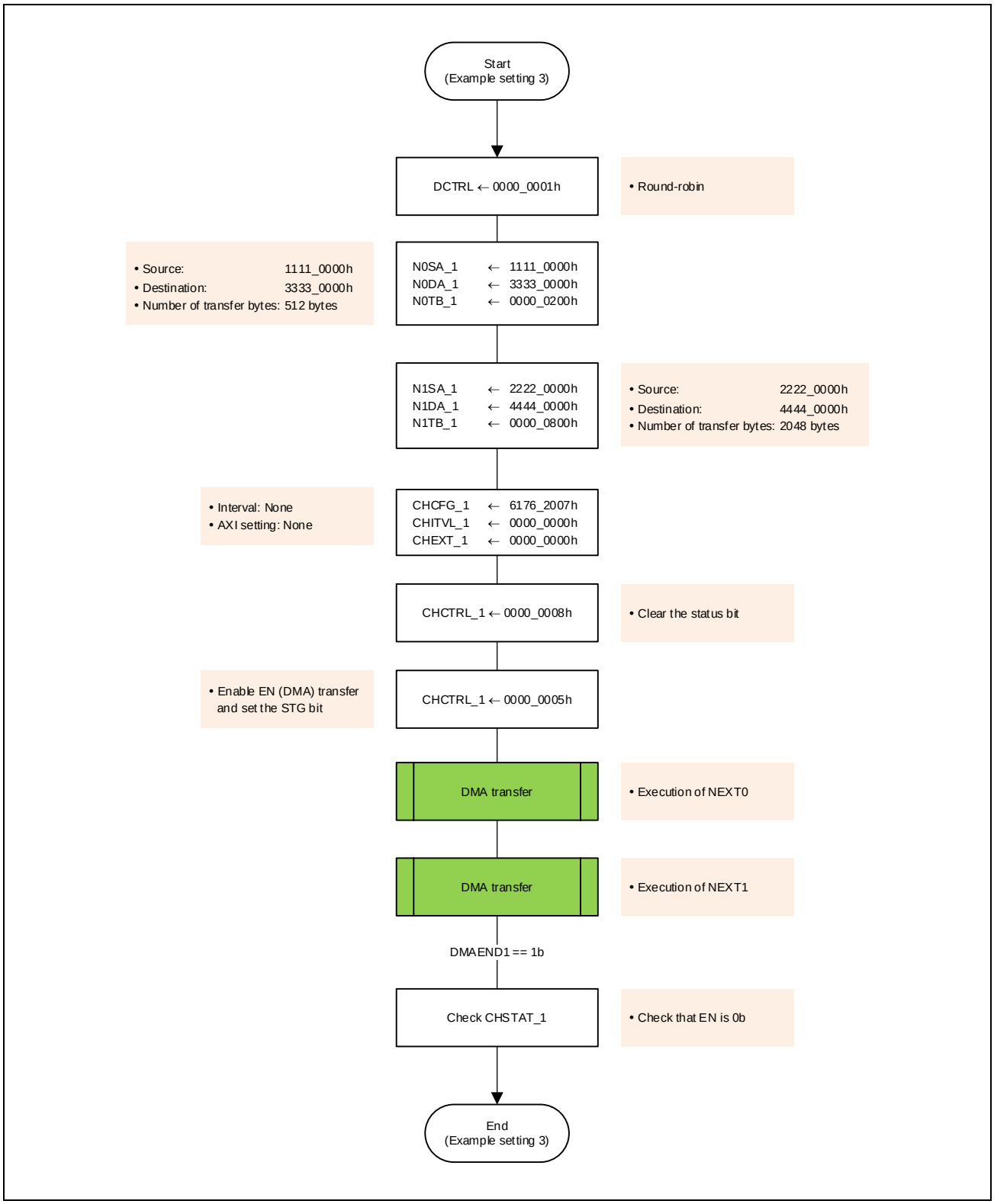


Figure 19.7-3 Example Setting 3

19.7.1.4 Example Setting 4 (Link Mode)

The table below lists the settings when DMA transfer is to proceed with example setting 4.

Table 19.7-5 Example Setting 4 for DMA Transfer

Item	Description
Channel to be used	0
Priority control	Round-robin
DMA mode	Link
Transfer mode	Block transfer
Register set to be used	—
Descriptor start address	0000_1000h

Table 19.7-6 Example Setting 4 for DMA Transfer (Descriptor 1)

Item		Description	
Descriptor start address		0000_1000h	
Next descriptor start address		0000_2000h	
Transfer mode		Block transfer	
Next0		Transfer source	Transfer destination
	Start address	1111_0000h	3333_0000h
	Address direction	Incremental	Incremental
	Transfer size	32 bits	32 bits
	Number of bytes for DMA transfer	2048 bytes	
DMAREQ/ACK/TCO		Select DMAREQ[0] and DMAACK[0].	
DMA transfer request		Software activation (STG)	
DMAACK signal		Not output	
DMAEND masking		Yes	
AXI setting (PROT, CACHE)		Initial value	
Header			
	DMAEND when LV = 1b	Issued (DIM = 0b)	
	LV write-back	Yes (WBD = 0b)	
	Next link destination	Yes (LE = 0b)	
	Descriptor enable	Enable (LV = 1b)	

Table 19.7-7 Example Setting 4 for DMA Transfer (Descriptor 2)

Item		Description	
Descriptor start address		0000_2000h	
Next descriptor start address		0000_5000h	
Transfer mode		Block transfer	
Next0		Transfer source	Transfer destination
	Start address	4444_0000h	5555_0000h
	Address direction	Incremental	Incremental
	Transfer size	64 bits	256 bits
	Number of bytes for DMA transfer	1024 bytes	
DMAREQ/ACK/TCO		Select DMAREQ[0] and DMAACK[0].	
DMA transfer request		Software activation (STG)	
DMAACK signal		Not output	
DMAEND masking		Yes	
AXI setting (PROT, CACHE)		Initial value	
Header			
	DMAEND when LV = 1b	Issued (DIM = 0b)	
	LV write-back	Yes (WBD = 0b)	
	Next link destination	Yes (LE = 0b)	
	Descriptor enable	Enable (LV = 1b)	

Table 19.7-8 Example Setting 4 for DMA Transfer (Descriptor 3)

Item		Description	
Descriptor start address		0000_5000h	
Next descriptor start address		—	
Transfer mode		Block transfer	
Next0		Transfer source	Transfer destination
	Start address	7777_0000h	AAAA_0000h
	Address direction	Incremental	Incremental
	Transfer size	512 bits	512 bits
	Number of bytes for DMA transfer	4096 bytes	
DMAREQ/ACK/TCO		Select DMAREQ[0] and DMAACK[0].	
DMA transfer request		Software activation (STG)	
DMAACK signal		Not output	
DMAEND masking		No	
AXI setting (PROT, CACHE)		Initial value	
Header			
	DMAEND when LV = 1b	Issued (DIM = 0b)	
	LV write-back	Yes (WBD = 0b)	
	Next link destination	No (LE = 1b)	
	Descriptor enable	Enable (LV = 1b)	

Example Setting 4

DCTRL= 0000_0001h (DMAC setting)

NXLA = 0000_1000h (Descriptor start address)

CHCFG = 8000_0000h (Configuration)

Table 19.7-9 Descriptor Settings

	Descriptor 1	Descriptor 2	Descriptor 3
Header	0000_0001h	0000_0001h	0000_0003h
SA (source address)	1111_0000h	4444_0000h	7777_0000h
DA (destination address)	3333_0000h	5555_0000h	AAAA_0000h
TB (transaction byte)	0000_0800h	0000_0400h	0000_1000h
CFG (configuration)	8342_2008h	8345_3008h	8246_6008h
ITVL (interval)	0000_0000h	0000_0000h	0000_0000h
EXT (extension)	0000_0000h	0000_0000h	0000_0000h
NXLA (next link address)	0000_2000h	0000_5000h	0000_0000h

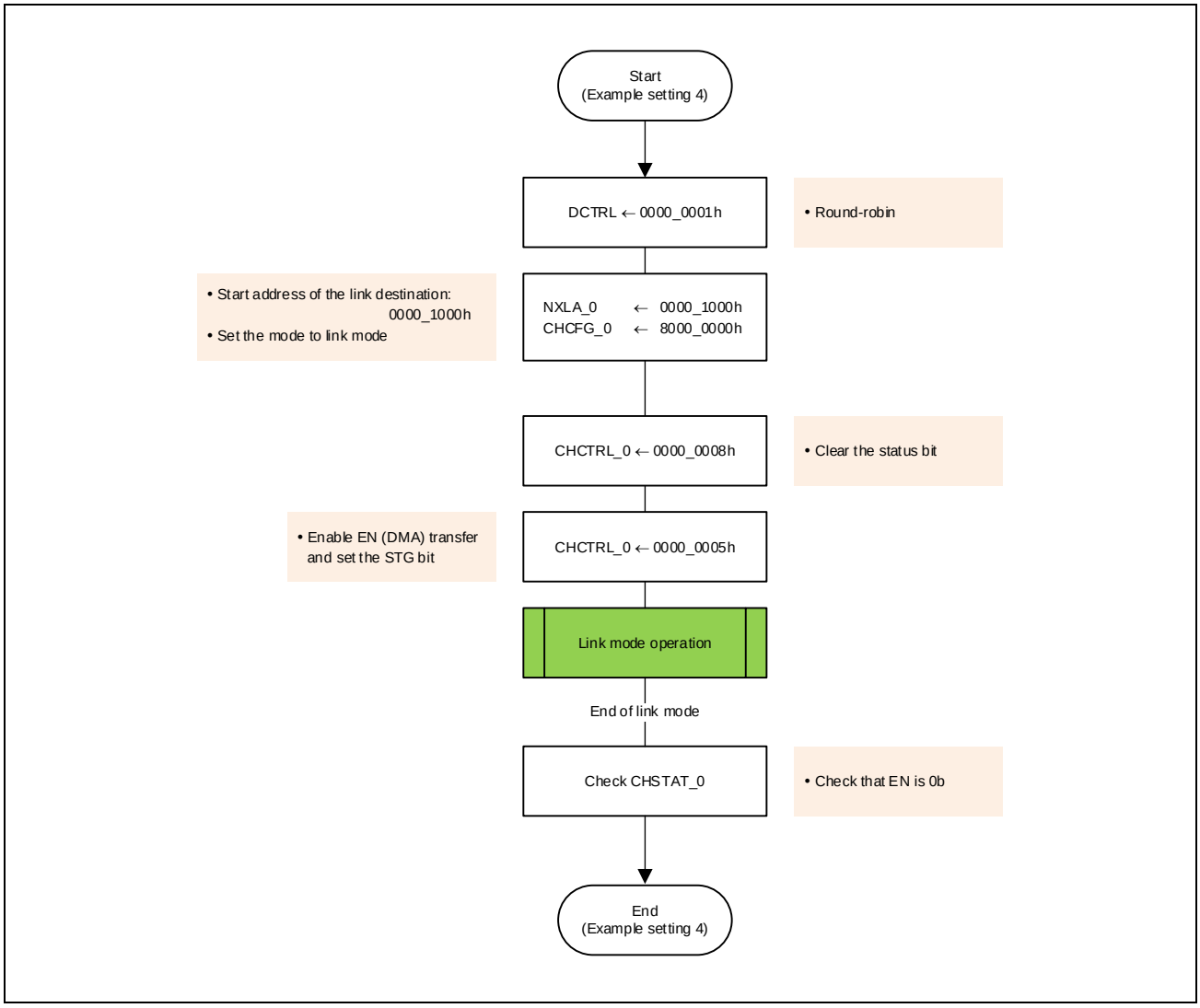


Figure 19.7-4 Example Setting 4

19.7.1.5 Setting for Next Register Continuous Execution

The figure below is a flowchart when DMA transfer continues with the use of two Next register sets in register mode. While the DMA transaction of one Next register is in progress, the other Next register is set to continue with DMA transfer.

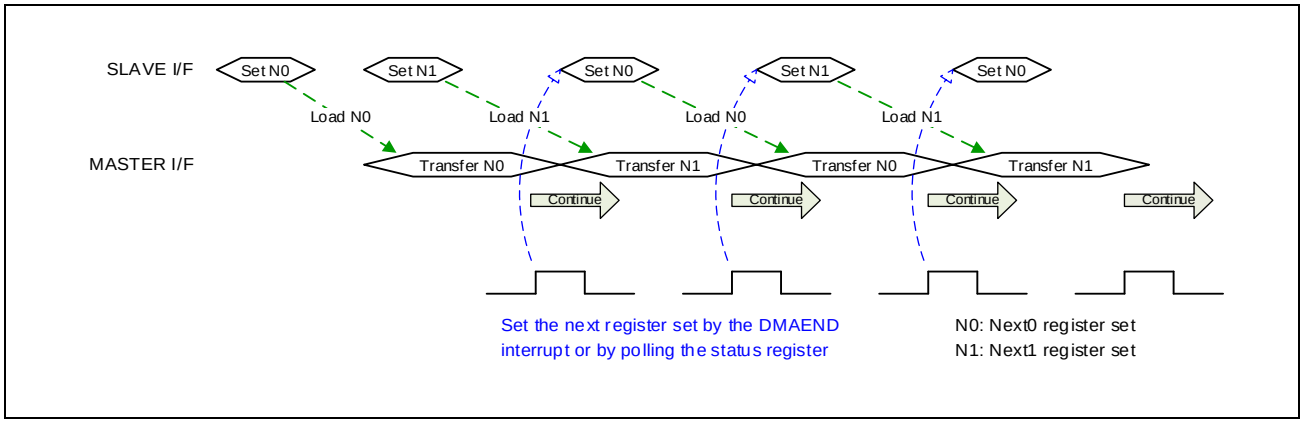


Figure 19.7-5 Schematic View of Next Register Continuous Execution

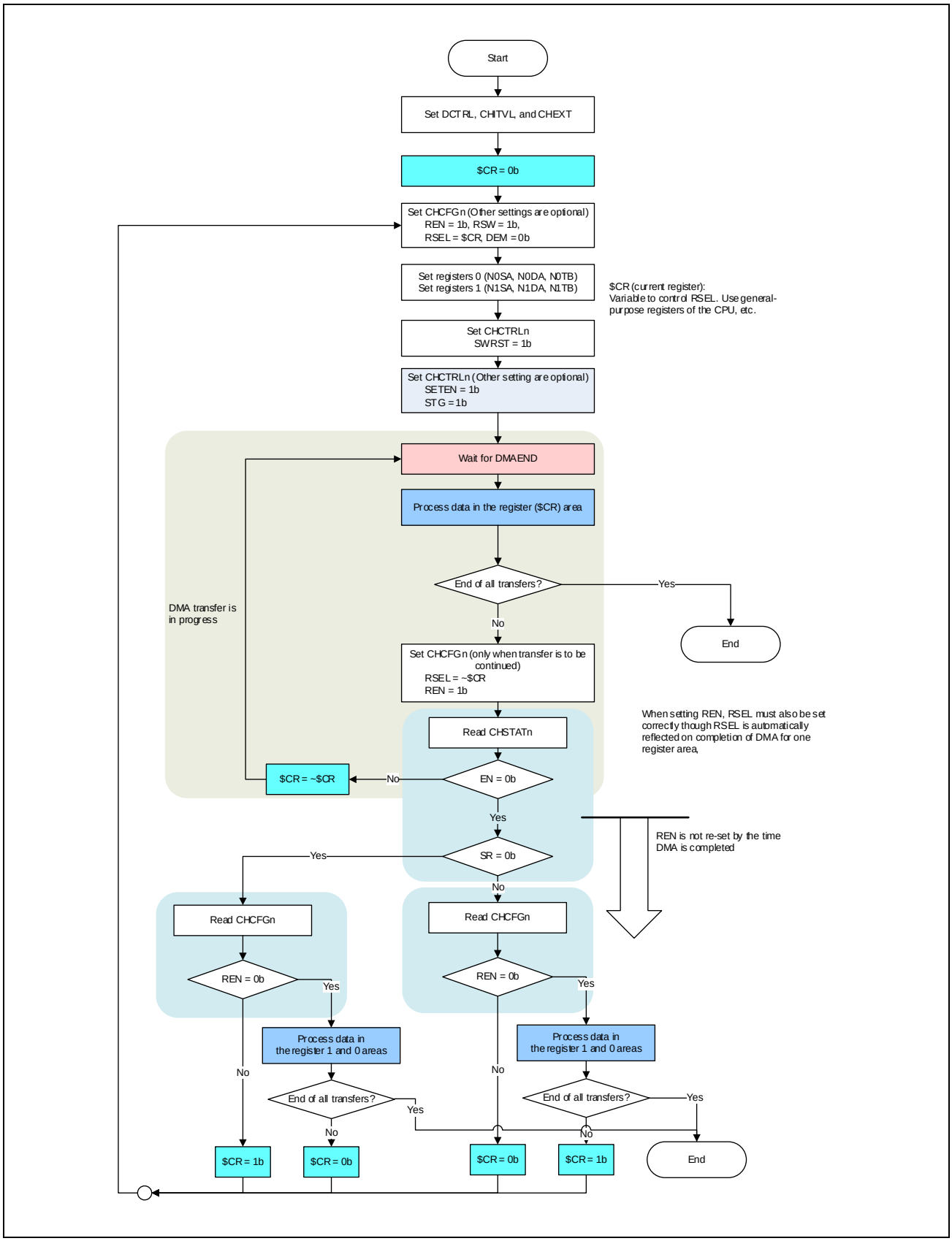


Figure 19.7-6 Example Setting 5

Supplementary Information

Store the first register sets (0 (N0SA, N0DA, N0TB) , 1 (N1SA, N1DA, N1TB)) to be transferred in general-purpose registers of the CPU (this register value called $CR for convenience).

Every time DMA transfer of one register set is completed (DMAEND is asserted), REN is automatically cleared to 0b. To continue transfer, REN of the CHCFG_m register must be set every time DMAEND is asserted. The same register also has the setting bit of RSEL, so this value must also be set correctly. To do this, use $CR.

In this mode, two Next registers are executed consecutively. However, if CLREN is not set by the time the DMA transaction is completed (next DMAEND is asserted), continuous execution stops. In such cases, check how far the transfer has proceeded by reading the SR and EN bits of the CHSTATn register and REN of the CHCFG_m register. To resume the transfer, follow the procedure in the above flowchart.

19.8 Points for Caution

19.8.1 Problem of DMAACK Overtaking DMA Transfer

When contention between access by this unit and access by another master arises or there is a bus bridge between this unit and the device that asserted the DMAREQ signal, DMA transfer may be delayed relative to assertion of the DMAACK signal.

In cases where the DMAACK signal is asserted but the corresponding bus access has not yet arrived, if the device that asserted the DMAREQ signal for the unfinished transfer asserts this signal again, DMA transfers may overlap.

Make sure that a device that asserts the DMAREQ signal does not assert this signal twice for a single DMA transfer activation source.

The following describes an example where DMA transfer is delayed relative to the assertion of the DMAACK signal.

19.8.1.1 Example Circuit 1 where DMA transfer is Delayed Relative to the DMAACK Signal

This unit starts to assert the DMAACK signal simultaneously with the start of transfer (MARVALID (or MAWVALID) is at the high level) even when the MARREADY (or MAWREADY) signal is at the low level. This start timing does not depend on the level of the MARREADY (or MAWREADY) signal.

For example, in the case of the circuit shown below, if this unit attempts to access slave A while master A has access to slave A, a low level is returned as the MARREADY signal by the AXI interconnect and transfer by this unit may be held pending, but the DMAACK signal will still be asserted.

As a result, a time lag is generated between assertion of the DMAACK signal and the actual time at which transfer on the bus becomes possible.

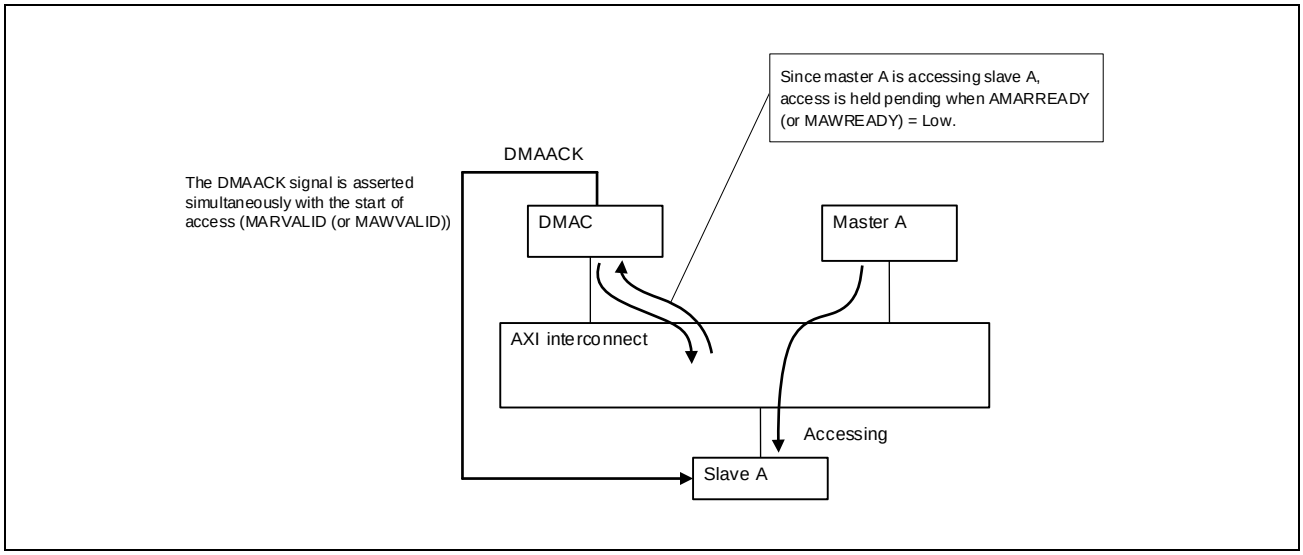


Figure 19.8-1 Example: Circuit where a Wait Causes a Delay from Activation of the DMAACK Signal to Actual Access

19.8.1.2 Example Circuit 2 where DMA transfer is Delayed Relative to the DMAACK Signal

If a device that receives DMAACK is connected to a different bus from that of this unit, a difference may be generated between access to that device by this unit and access until DMAACK is reached.

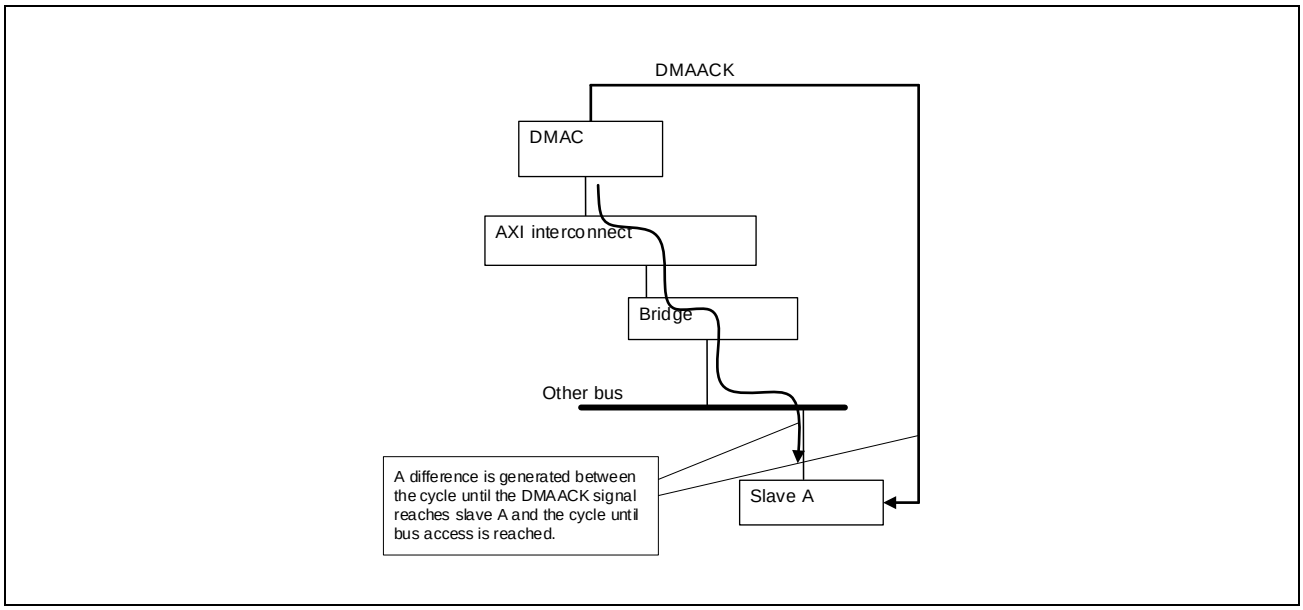


Figure 19.8-2 Example: Circuit where a Delay from Activation of the DMAACK Signal to Actual Access is Caused via a Bus Bridge

19.8.1.3 Example Circuit 3 where DMA transfer is Delayed Relative to the DMAACK Signal

Due to the configuration of the internal circuit, the MARVALID (or MAWVALID) signal is asserted with a delay of one or more cycles relative to the DMAACK signal.

19.8.2 Problem of the Interrupt Signal Overtaking DMA Transfer

19.8.2.1 Overview

This unit asserts the DMAINT interrupt signal on completion of transfer and this serves as a trigger for the CPU to start processing the data.

However, in cases such as where the device for writing is on another bus, the final data to be written may not yet have reached the device for writing at the time the DMAINT interrupt signal is asserted.

If the CPU accesses a device that has detected the DMAINT interrupt signal before the final data of the DMA transaction have been written to the device, it may be using some old data from before the writing.

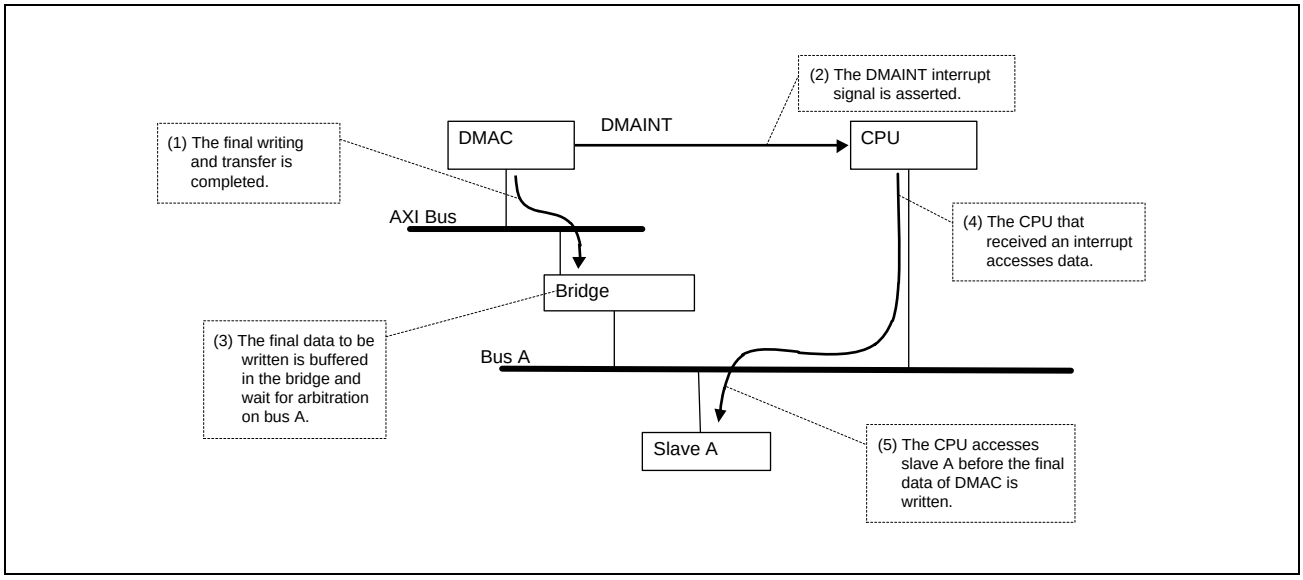


Figure 19.8-3 Example when Access by the CPU Overtakes Writing of the Final Data by the DMAC

19.8.2.2 Workarounds

The following describes workarounds for the above problems.

Workaround 1: Setting AWPROT as non-bufferable

Set the MAWPROT signal as non-bufferable for DMA transactions. By doing this, the above problems can be avoided because the DMAINT interrupt signal will only be asserted after the completion of writing to the device for access.

Setting all transfers to non-bufferable may reduce the efficiency of transfer. In such cases, divide up the register sets or descriptors by setting most of the transactions to bufferable for transfer, and then set only the last transfer to non-bufferable.

Exception)

The effect is not obtained if the device in the access path does not refer to AWPROT.

Workaround 2: Dummy access to the last written address by this unit

The completion of writing data is guaranteed by asserting the DMAINT interrupt signal after dummy reading the last written address area from this unit and then dummy writing it to the area that does not affect operation.

In register mode, set the main DMA transfer in one register set and set dummy access in the other register set. Since masking of the interrupt is automatically removed on completion of the DMA transaction of one register set, the interrupt can be asserted after dummy access.

In link mode, prepare a descriptor for dummy access and configure a descriptor chain such that this descriptor is accessed after the main DMA transfer. Since masking of the interrupt can be set in the descriptor, so mask the interrupt in the main DMA transaction and de-assert the interrupt in dummy access beforehand.

Exception)

This workaround cannot be used if dummy reading of the device affects its operation.
It also cannot be used if transfer is through a device for which the order of reading and writing may be reversed. The order of reading and writing may be reversed in the AXI bus. If this is the case, set ARPROT and AWPROT to non-bufferable for transfer.

Workaround 3: Polling the descriptor

Use link mode to provide descriptors in slave A and enable descriptor write-back to start DMA transfer.

This unit asserts the DMAINT interrupt signal after writing back the descriptor following the last DMAC write transfer. Make sure that the CPU refers to the last DMA write data after polling the descriptor in slave A to check that it has been written back.

Exception)

This workaround cannot be used if descriptors cannot be located in the device. In such cases, handle the problem by locating descriptors in another device on the same bus as the device, or a similar measure.

Section 20 Interrupt Controller (GIC)

This section describes the functions of the interrupt controller (GIC).

20.1 Functional Overview

The GIC incorporates the Arm® CoreLink™ GIC-400 generic interrupt controller from ARM. For details on the GIC-400, see *the ARM CoreLink GIC-400 Generic Interrupt Controller Technical Reference Manual*.

Table 20.1-1 lists a summary of the functions.

Table 20.1-1 Functional Overview

Item	Functions
Interrupt controller	GIC-400 generic interrupt controller r0p1 Compliant with ARM generic interrupt controller architecture version 2.0
Supported interrupt factors	• SGI (software generated interrupt): 16 factors • PPI (private peripheral interrupt): 6 factors • SPI (shared peripheral interrupt): 480 factors

20.1.1 GIC Configuration

Table 20.1-2 lists the GIC configuration.

Table 20.1-2 GIC Configuration

Item	Setting
Number of supported processors	2
Number of supported SPIs	480
ID width of AXI read channel	10
ID width of AXI write channel	10

20.2 Address Space

The register of the GIC is arranged in 4-KB address boundaries for individual functions. In the GIC of this LSI, it is reallocated to 64-KB address boundaries in order to support the virtualization feature of ARM-v8 architecture. **Figure 20.5-1** shows the relationship between the GIC address and the system address.

CAUTION

GIC Address: Addresses defined in the ARM GIC-400 specifications
System Address: Address of the GIC unit in this LSI

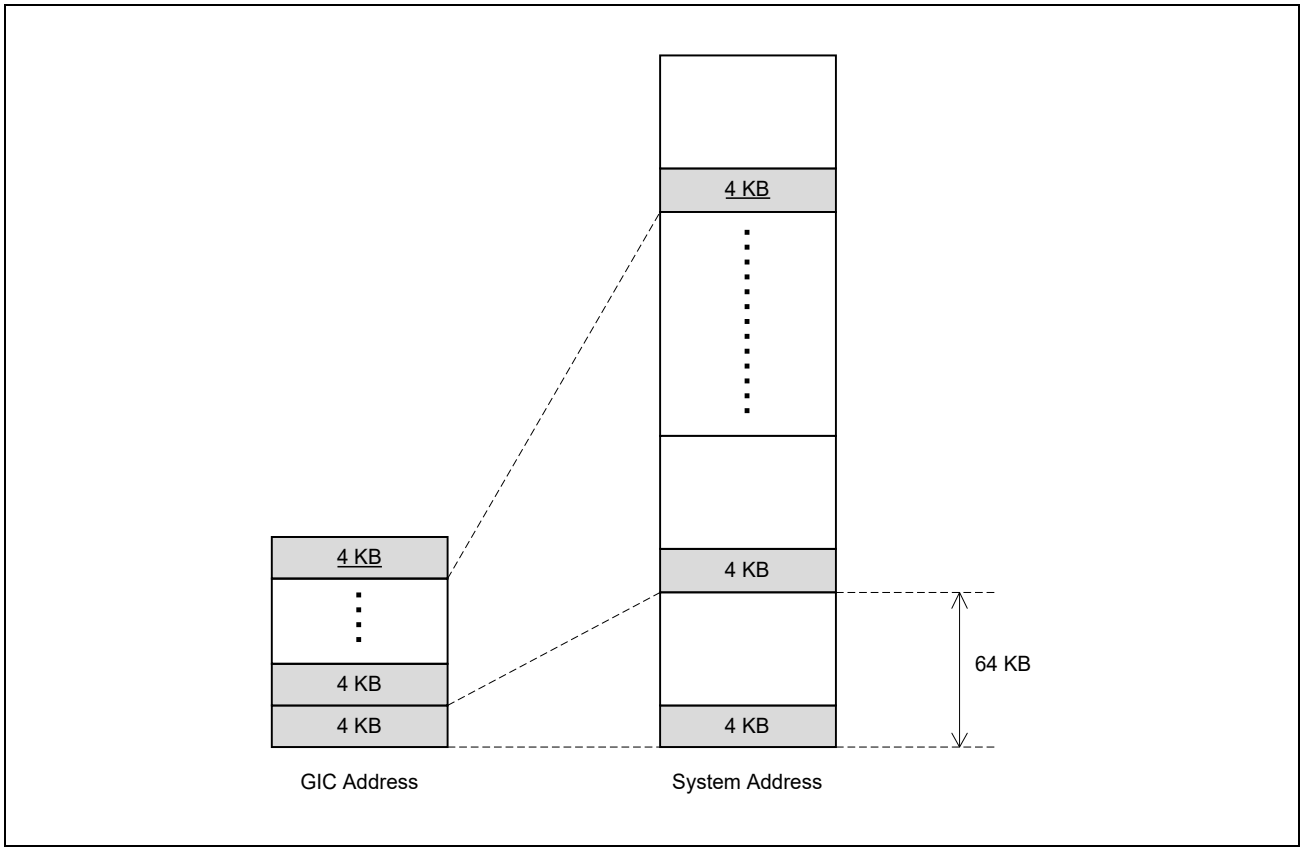


Figure 20.5-1 Relationship between the GIC Address and the System Address

Table 20.5-1 Address Space for GIC Functions

System Address	GIC Address	GIC Functions	Abbreviation
<GIC_S0_base> + 0_0000h to 0_0FFFh	0000h to 0FFFh	Reserved	—
<GIC_S0_base> + 1_0000h to 1_0FFFh	1000h to 1FFFh	Distributor	GICD_
<GIC_S0_base> + 2_0000h to 3_0FFFh	2000h to 3FFFh	CPU Interfaces	GICC_
<GIC_S0_base> + 4_0000h to 4_0FFFh	4000h to 4FFFh	Virtual interface control block, for the processor that is performing the access	GICH_
<GIC_S0_base> + 5_0000h to 5_01FFh	5000h to 51FFh	Virtual interface control block, for processor 0	GICH_CPU0_
<GIC_S0_base> + 5_0200h to 5_03FFh	5200h to 53FFh	Virtual interface control block, for processor 1	GICH_CPU1_
<GIC_S0_base> + 5_0400h to 5_0FFFh	5400h to 5FFFh	Reserved	—
<GIC_S0_base> + 6_0000h to 7_0FFFh	6000h to 7FFFh	Virtual CPU interfaces	GICV_

20.3 Register Descriptions

The GIC is the Arm® CoreLink™ GIC-400 generic interrupt controller.

The revision number of the IP module is r0p1.

For the details of these registers, refer to the ARM manual shown below.

- *ARM CoreLink GIC-400 Generic Interrupt Controller Technical Reference Manual*

20.4 Functional Description

For details on the functions of the GIC, see *the ARM CoreLink GIC-400 Generic Interrupt Controller Technical Reference Manual*.

Section 21 CMOS Image Sensor Interface (CIF)

This section describes the functions of the CMOS image sensor interface (CIF).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

21.1 Functional Overview

The CIF has the MIPI CSI-2 D-PHY and link which support the MIPI CSI-2 Ver1.2 interface.

The main functions of CIF are listed in **Table 21.1-1**.

Table 21.1-1 Function Overview

Classification	Description
CMOS image sensor interface (D-PHY)	• Supports MIPI D-PHY ver1.2 • Transfer rate: MIPI D-PHY: Max. 2.5 Gbps/lane • Maximum input clock frequency: Up to 1.25 GHz • Maximum number of lanes: Data: 4 lanes × 2 + Clock: 2 lanes • 8-bit/lane parallel output: 8 bits • 2 sensor input*1
CMOS image sensor interface (Link)	• Conforms to the MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2) v1.2 (*Note*: Ultra-low power mode is not supported.) • RAW8/10/12, YUV422*2, User defined byte-based data supported • Short/long packet supported • WDR supported (DOL DINFO, virtual channel)

Note 1. Using 2 sensor input requires software provided by a partner company. For details, contact a Renesas Electronics sales representative.

Note 2. The input of data in this format limits the available functions of the LSI chip. For details, contact a Renesas Electronics sales representative.

21.1.1 Conforming Standards

- Conforms to the MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2) version 1.2
- MIPI Alliance Specification for D-PHY Version 1.2

Section 22 Image Sensor Timing Generator (STG)

This section describes the functions of the image sensor timing generator (STG).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

22.1 Functional Overview

The STG unit generates the timing for CMOS image sensors.

- Timing generation for image sensors

  The image sensor timing generator (STG) is connected to the CMOS image sensor or sensors to generate the timing for synchronization. The STG internally generates a synchronization signal and supplies it to the image sensor in master mode.

- VD/HD generation/output for image sensors

  One or two image sensors can be connected to the STG. When two image sensors are in use, there are two choices in terms of synchronization. With synchronous driving, both sensors operate with the same timing; with asynchronous driving, the timing for each sensor is completely separate from that for the other.

- Serial interface dedicated for image sensors

  For serial communications for controlling the image sensor (or sensors), 4-wire clock-synchronous serial communications and IIC communications are available. Both types of communications support the automatic sending of values for setting by a dedicated DMAC and transfer in both directions under CPU control.

- Generation of shutter triggers

  The STG also has functionality for issuing an interrupt with a desired timing in terms of image-sensor driving and for the output of timing pulses to control mechanical shutters, strobes, and other devices of the imaging system.

Section 23 Audio Interface (AUI)

This section describes the functions of the audio interface (AUI).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

23.1 Functional Overview

The AUI supports DMA transfer and can send and receive data to and from audio devices that support the I2S interface. The audio device is used as the master and the AUI is used as the slave.

- I2S interface:
  - Slave mode
  - MSB first
  - AUBICK frequency 64 fs (fs: sampling rate)

- Audio format: Linear PCM 8/16 bits, monaural/stereo

- Sampling rate: 32 kHz, 44.1 kHz, or 48 kHz

- Audio processing:
  - Digital volume control (for both playback and recording)

    Function for changing the volume of audio data during playback or recording
  - Frequency conversion (only for playback)

    Function for converting the frequency of output audio data during playback

Section 24 AI Accelerator (DRP-AI)

This section describes the functions of the AI accelerator (DRP-AI).

24.1 Functional Overview

The AI accelerator contains a DRP and an AI-MAC, which are called DRP-AI. It uses the information on the LPDDR4 memory to perform AI inference and store the results.

The DRP-AI is an AI accelerator that can execute AI inference independently of the CPU. The DRP-AI works by the DRP-AI driver reading the descriptor for converting trained AI models by the DRP-AI translator.

- DRP-AI translator: Conversion tool to be provided separately
- DRP-AI driver: Linux device driver to be provided separately

24.2 Block Diagram

The AI accelerator contains a DRP and an AI-MAC.

■ DRP (programmable hardware)

[Configuration]

- DRP: Reconfigurable core
- DMAC: Improves the efficiency of data transfer

■ AI-MAC (hardware for high-speed processing of 16-bit floating-point (FP16) matrix operations)

[Configuration]

- MAC (multiply-accumulate calculator): Matrix multiply-accumulate operations
  - Local memory (SRAM for this unit): Holds matrix data, and the weight and bias values of the learning results.
- DMAC: Transfers matrix data, and weight and bias values from LPDDR4 to the local memory.
  Transfers the result of the multiply-and-accumulate operation output by MAC to LPDDR4.

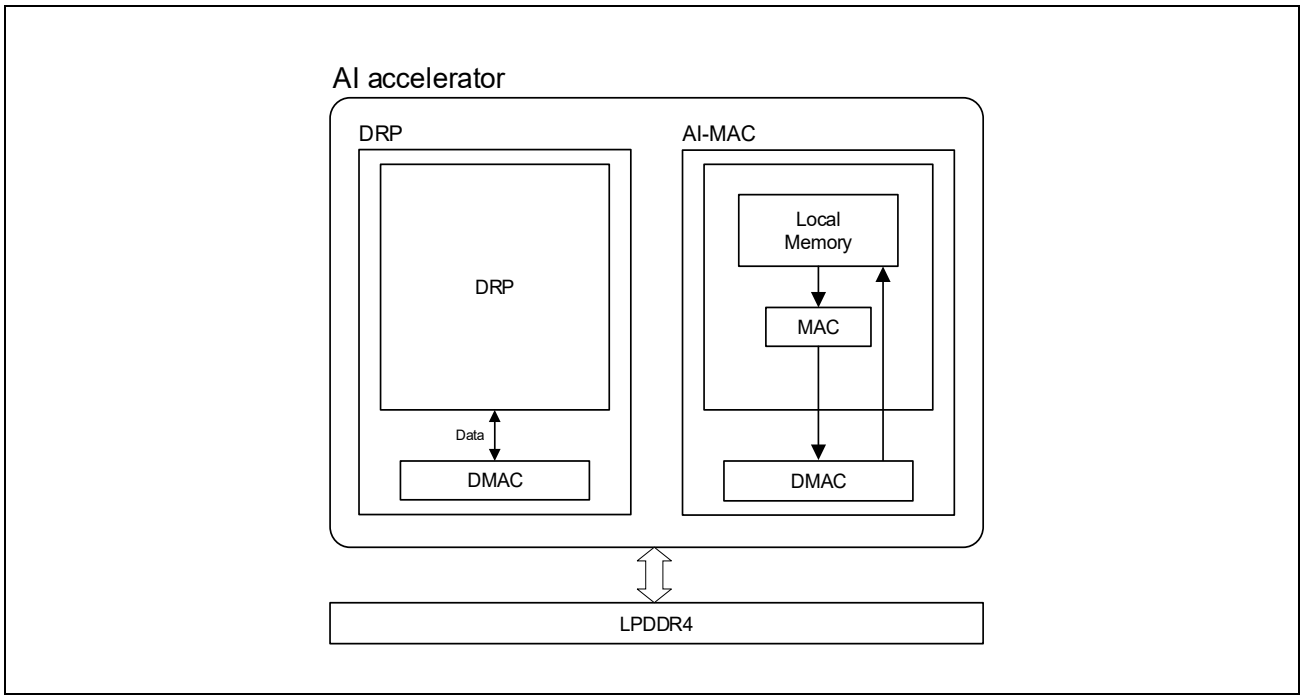


Figure 24.2-1 Block Diagram of AI Accelerator

24.3 Inference Operation Example on DRP-AI

Figure 24.3-1 shows the inference operation example. The DRP-AI can perform AI inference with the DRP and AI-MAC. This operation is performed automatically by reading the descriptor thorough the DRP-AI driver after kicking the API. When AI inference is completed, the DRP-AI sends the interrupt flag to the CPU.

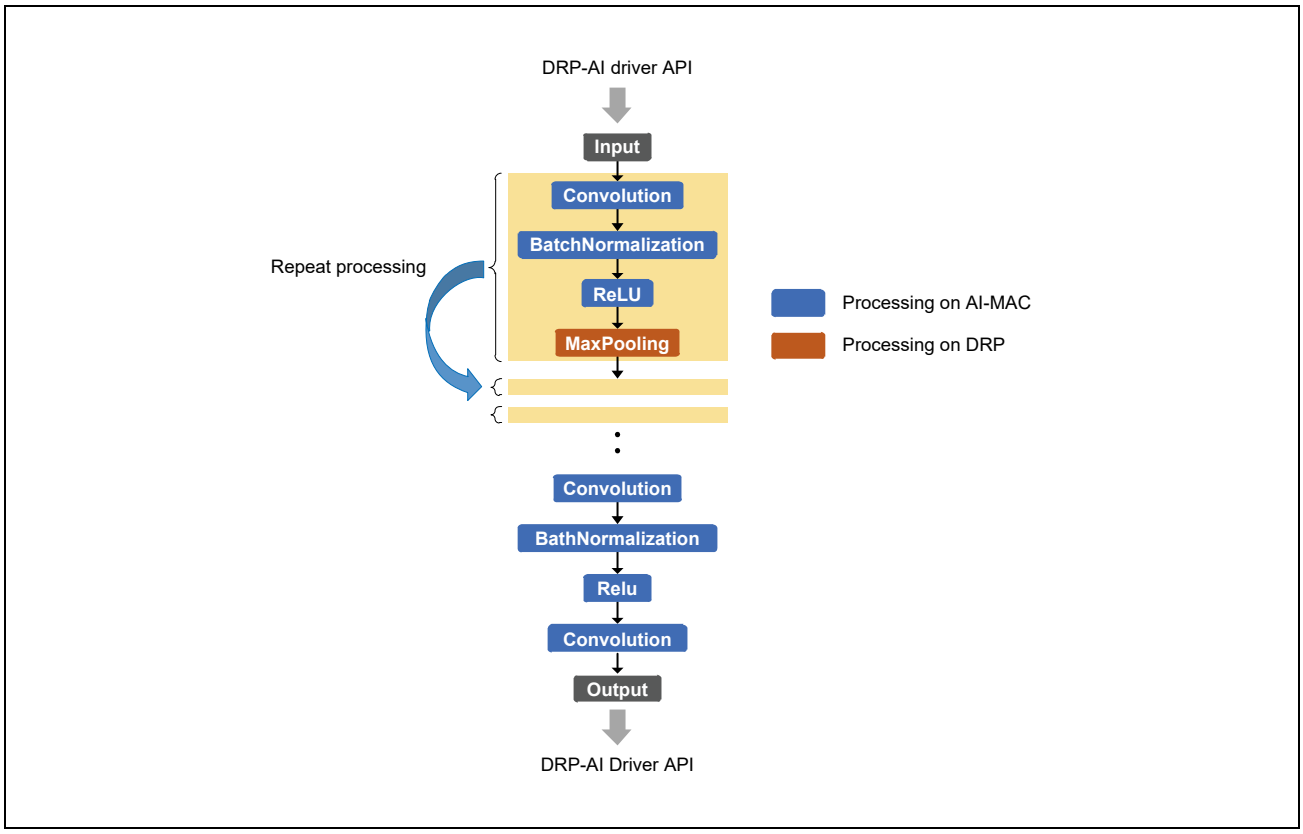


Figure 24.3-1 Inference Operation Example on DRP-AI

Section 25 Multi-Target Detection (MTD)

This section describes the functions of the multi-target detection (MTD).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

25.1 Functional Overview

The MTD detects faces and human bodies from input images and provides information on the number of detected faces or bodies, and their sizes and locations.

- Input image format: 8-bit luminance (Y)
- Input image size: 320 × 240 / 640 × 480 / 720 × 480 / 960 × 540
- Targets for detection: Faces, human bodies
- Summary for output: Number of detected items, sizes, center coordinates

25.2 Functional Description

25.2.1 Face Detection

The specification of the face detection function is as follows:

- The number of simultaneous detections: 35 (max.)
- Detection angle: ±45 degrees relative to the reference direction for detection.
- Detection direction: Up, down, left, and right are supported.
- Incidental information on detection: Position, size, evaluation value (0 to 9), detection angle (0 to 359 degrees), and direction (front / right oblique / right side / left oblique / left side)

25.2.2 Human Body Detection

The specification of the human body detection function is as follows:

- The number of simultaneous detections: 35 (max.)
- Detection angle: ±10 degrees relative to the reference direction for detection.
- Detection direction: Up, down, left, and right are supported.
- Incidental information on detection: Position, size, evaluation value (0 to 9), detection angle (0, 90, 180, and 270 degrees)

Section 26 General Processing Accelerator (GPA)

This section describes the functions of the general processing accelerator (GPA).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

26.1 Functional Overview

- General-purpose image processing (color space conversion, general-purpose filters, data string operations, etc.)
- Various assistance functions (WDR)

Section 27 Camera ISP (ISP)

This section describes the functions of the camera ISP (ISP).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

27.1 Functional Overview

The ISP unit handles image processing of raw data captured from an image sensor.

- The camera ISP unit consists of the following three processing blocks.
  - Image sensor image capturing block
  - Development processing block (Bayer to YUV processing)
  - Post processing block (deformation processing)

- Input: Raw data RGBG Bayer 10/12 bits
  *RGB-W and RGB-IR handling are also available options.
- Output: YUV422 8 bits
- Maximum resolution: 12,800 × 16,382 pixels (when a single camera is connected) / 6,400 × 16,382 pixels (when a dual camera is connected)
- Processing capacity: 3840 × 2160 p × 30 fps / 1920 × 1080 p × 60 fps / 1920 × 1080 p × 30 fps × 2 / 640 × 480p × 800 fps

Section 28 H.265/H.264 Multi Codec (VCD)

This section describes the functions of the H.265/H.264 multi codec (VCD).

28.1 Functional Overview

The VCD is a video codec that supports H.264 and H.265. It has the features shown below.

- H.265/HEVC MP (main profile) supported

  H.265/HEVC main profile at level 5

- H.264/AVC constrained baseline/main/high profile supported

  High profile at level 5.1,

  Progressive high profile at level 5.1,

  Constrained high profile at level 5.1,

  Main profile at level 5.1,

  Constrained baseline profile at level 5.1

- H.265 encoding and decoding performance

  3840 × 2160 × 30fps encoding, 3840 × 2160 × 30fps decoding

  1920 × 1080p × 60 fps encoding, 1920 × 1080p × 60 fps decoding

  640 × 480 × 800 fps encoding

- H.264 encoding and decoding performance

  1920 × 1080p × 60 fps encoding, 1920 × 1080p × 60 fps decoding

  640 × 480 × 800 fps encoding

- Supports the rate control among HW frames when encoding
- Supports the tile structure during H.265 encoding (vertical division into two only)
- Supports VPS (H.265 only), SPS, PPS, and AUD coding and output functions by HW during encoding
- Equipped with lossless compression and reference image buffer to reduce memory bandwidth

28.2 Connection Configuration

Figure 28.2-1 shows the connection configuration for the H.265/H.264 multi codec (VCD).

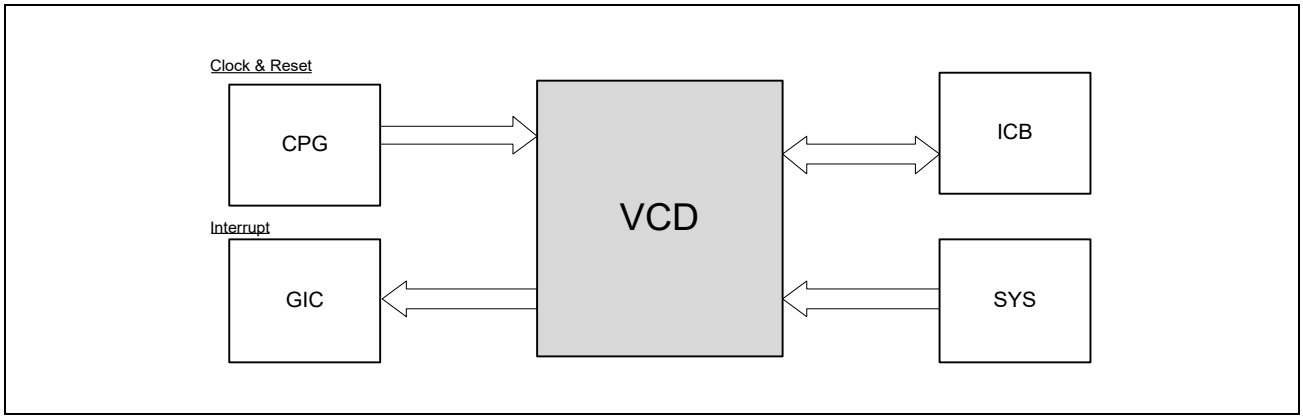


Figure 28.2-1 Configuration Diagram of VCD Connection

28.3 Operation Procedure

For VCD operations, APIs are defined. For details, see the ISP control software specification.

Section 29 2D Graphics Engine (GRP)

This section describes the functions of the 2D graphics engine (GRP).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

29.1 Functional Overview

This LSI is equipped with a 2D graphics core. The supported functions are as follows.

- Provides a wide variety of graphics primitives such as lines, triangles, squares, and circles.
- Supports anti-aliasing and high-precision sub-pixel rendering.
- Bezier line and bezier segment generation
- Flexible colorization using multiple paths
- Dedicated clearing unit to clear memory area with maximum bandwidth
- Texture size: 4096 × 4096

Section 30 JPEG Codec (JPG)

This section describes the functions of the JPEG codec (JPG).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

30.1 Functional Overview

The JPG is a unit for compression/decompression of still images according to the baseline process (BASELINE). As a compression/decompression process, it uses the discrete cosine transform (DCT), quantization, and Huffman code methods. The JPG is capable of processing up to 16 samples/clock.

(1) JPEG Function

Calculation accuracy:	JPEG Part2 (ISO/IEC10918-2)
Image input/output method:	Block interleaving method
Image data rate:	Max. 16 samples/clock
Image size:	The size that can be divided by MCU units
Quantization table:	**[At compression]** Set via a register. **[At decompression]** See the table contained in the code data.
Huffman table:	**[At compression]** Fixed table with embedded H/W **[At decompression]** See the table contained in the code data.
Marker:	Automatic generation at compression, automatic decoding at decompression • The target processing markers are SOI, SOF0, SOF1, SOS, DQT, DHT, DRI, RSTm, and EOI.
DHT marker:	Included (standard table fixed for BASELINE)
Sampling:	• Unit external input/output format The external input or external output color format is only as follows. – YUV422 (three color components) • Unit internal color format conversion The internal color format conversions on JPG unit are as follows. – From external YUV422 (three color components) to YUV422 or YUV420 (three color components) at compression. – From YUV422 or YUV420 (three color components) to external YUV422 (three color components) at decompression.

(2) Data Input/Output Function

The data input/output is performed by DMA transfer.

DMA function:

- DMA read function for image data arranged in raster on the memory
- DMA write function for image data to be arranged in raster on the memory
- DMA function for stream data to the memory

Section 31 LPDDR4 Interface (LPDDR4)

This section describes the functions of the LPDDR4 interface (LPDDR4).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

31.1 Overview

The LPDDR4 is a JEDEC 209-4A-compliant interface consisting of an LPDDR4 memory controller (MMC) and an LPDDR4 PHY interface (DDI) with the following functions.

- Supported data rate: 3200 Mbps
- Data bus width: 32 bits
- Supported memory capacities: 2 GB, 4 GB*1
- Supports 1- and 2-rank memory*1
- Operating modes:
  - Burst length: 16 (fixed)
  - Burst type: Sequential (fixed)
- ZQ calibration operation
- The following features for use with LPDDR4 are not supported:
  - MPC (multi-purpose command) is not supported except ZQ calibration
  - Modified refresh (for derating)
  - BL32 functionality
  - 12-Gb and 16-Gb (per channel) densities with byte mode

Note 1. This LSI supports the following LPDDR4 SDRAM devices.
1-rank memory: 2 GB
2-rank memory: 4 GB

Section 32 SD Host Interface (SDI)

This section describes the functions of the SD Host interface (SDI).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

32.1 Functional Overview

The SDI blocks mainly consist of the SD interface, which is the main control block, and the sampling clock controller (SCC), which is the sampling clock control block. This LSI chip is equipped with two SDIs; SDI0 and SDI1, and they are compatible with SD-UHS-I SDR104.

SDI1 includes a fail-safe function.

32.2 Block Diagram

For more information, contact a Renesas Electronics sales representative.

32.3 Pin Functions

Table 32.3-1 lists the external pins of the SDI..

Table 32.3-1 List of External Pins

Pin name	I/O	Function
SDnCLK	Output	Clock output (SDCLK)
SDnCMD	IO	Command output, response input
SDnDAT0	IO	Data [bit 0]
SDnDAT1	IO	Data [bit 1], SDIO interrupt
SDnDAT2	IO	Data [bit 2], Read wait
SDnDAT3	IO	Data [bit 3], Card detection
SDnWP	Input	Write protection
SDnCD	Input	Card detection

Note: SDn (= SD0, SD1F) is the prefix of the SDI0/SDI1 interface

32.4 Address Map

Table 32.4-1 lists the register address map.

Table 32.4-1 Register Address Map

Module	Address
SD interface	0000h - 09FFh
SCC	1000h - 1FFFh

32.5 SD Interface

32.5.1 Overview

- 2 units are included: SDI0, SDI1.
- All support SD memory/IO card interfaces (1-/4-bit SD bus).
- SD, SDHC, and SDXC SD memory card access are supported.
- Default, high-speed, UHS-I/SDR12, SDR25, SDR50, and SDR104 transfer modes are supported.

  * DDR50 is not supported.
  * SDR104 tuning is only supported for transfer at 200 MHz.

- SD clock (SDCLK) frequency = IMCLK*[1] frequency/2^n (n = 0 to 9).
- Error checking function: CRC7 (for command/responses), CRC16 (for data)
- Interrupt requests: 2
- Card detection
- Write protection

Note 1. IMCLK: Main clock from CPG

Section 33 eMMC Host Interface (eMMC)

This section describes the functions of the eMMC host interface (eMMC).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

33.1 Functional Overview

The eMMC block mainly consists of the eMMC interface, which is the main control block, and the sampling clock controller (SCC), which is the sampling clock control block for the HS200 eMMC interface. The eMMC block is compatible with SD-UHS-I SDR104 and HS200 eMMC.

In addition, the use of eMMC and NAND flash memory is exclusive of each other.

33.2 Block Diagram

For more information, contact a Renesas Electronics sales representative.

33.3 Pin Functions

Table 33.3-1 lists the external pins of the eMMC.

Table 33.3-1 List of External Pins

Pin name	I/O	Function
MMCLK	Output	eMMC clock output (SDCLK)
MMCMD	IO	Command output, response input
MMDAT0	IO	Data [bit 0]
MMDAT1	IO	Data [bit 1]
MMDAT2	IO	Data [bit 2]
MMDAT3	IO	Data [bit 3]
MMDAT4	IO	Data [bit 4]
MMDAT5	IO	Data [bit 5]
MMDAT6	IO	Data [bit 6]
MMDAT7	IO	Data [bit 7]

33.4 Address Map

Table 33.4-1 lists the register address map.

Table 33.4-1 Register Address Map

Module	Address
eMMC interface	0000h - 09FFh
SCC	1000h - 1FFFh

33.5 eMMC Interface

This unit uses the same IP as that of the SDI and the use of SD cards may be described. Read the "SD card" as "eMMC".

33.5.1 Overview

- eMMC interface (1-/4-/8-bit MMC bus)
- Only eMMC device access is supported.
- Backward-compatible, high-speed, and HS200 transfer modes are supported.

  * High-speed DDR and HS400 are not supported.
  * HS200 tuning is only supported for transfer at 200 MHz.

- High-priority interrupt (HPI) is supported.
- Boot operation and alternative boot operation are supported.
- eMMC clock (SDCLK) frequency = IMCLK*1 frequency/2^n (n = 0 to 9).
- Error checking function: CRC7 (for command/responses), CRC16 (for data)

Note 1. IMCLK: Main clock from CPG

Section 34 NAND Flash Interface (NAND)

This section describes the functions of the NAND flash interface (NAND).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

34.1 General Information

The following items are described in this section.

- Features
- Pin index

34.1.1 Features

The main features of NAND flash interface (for the configuration described in this document):

- Compatibility:
  - Is compatible with the ONFI 1.0 specification
  - The controller support only legacy devices that uses five cycle addressing scheme (3 row address bytes and 2 column address bytes). The flash devices with 2 row address cycles supported only when are able to ignores third row address cycle.
- The controller has 8 execution threads.
- Interrupt controller:
  - Each interrupt can be masked
  - Each interrupt has its own status flag
  - The status flags are also valid when the given interrupt is masked, and can be checked by the software polling mechanism
  - Common interrupt port is provided for all interrupt sources
- Standard interface pin labeling
- Separate port interface for data and control/status registers
- Support for up to one banks with up to eight targets per bank
- Support for volume addressing. Up to sixteen volumes supported.
- Support for pipeline read and write commands for maximum data throughput
- Programmable access timing
- Intelligent hardware abstraction layer to off-load the processor as well as to provide direct data and control paths to the device
- The controller supports only devices that has three bytes row address.
- The controller does not support the EDO work mode on the flash interface.
- NAND is used exclusively with eMMC.

For the relationship with eMMC, see the descrition on the exclusive control of eMMC and NAND, in the MMC section.

The following shows the configuration.

Table 34.1-1 List of Configurations

Item	Description
Page (Sector) size	512 or 2048 bytes
NAND flash interface	8 bits
Error correction	OFF, 4, 8, 16, or 40 bits
DMA data width	64 bits
DMA address width	64 bits
EDO support	None

34.1.2 Pin Functions

34.1.2.1 List of External Pins

Table 34.1-2 lists the external pins of the NAND.

Table 34.1-2 List of External Pins

Classification	Pin Name	I/O	Function
NAND flash interface (NAND)	NADAT7 to NADAT0	IO	NAND flash I/O data [7:0]
	NACEN	Output	NAND flash chip enable (active low)
	NAREN	Output	NAND flash read enable (active low)
	NAWEN	Output	NAND flash write enable (active low)
	NACLE	Output	NAND flash command latch enable
	NAALE	Output	NAND flash address latch enable
	NARBN	Input	NAND flash ready/busy input
	NAWPN	Output	NAND flash write protect

Section 35 USB3.1 Gen1 Interface (USB)

This section describes the functions of the USB3.1 Gen1 interface (USB).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

35.1 Functional Overview

This unit is composed of a USB3.1 Gen1 Dual Role Device controller (USB3DRD), a USB3.1 Gen1 Host controller (USB3HOST), a USB3.1 Gen1 Peripheral controller (USB3PERI), and a USB test module (USB3TEST). **Table 35.1-1** and **Table 35.1-2** list the functions in outline.

Table 35.1-1 Functions in Outline

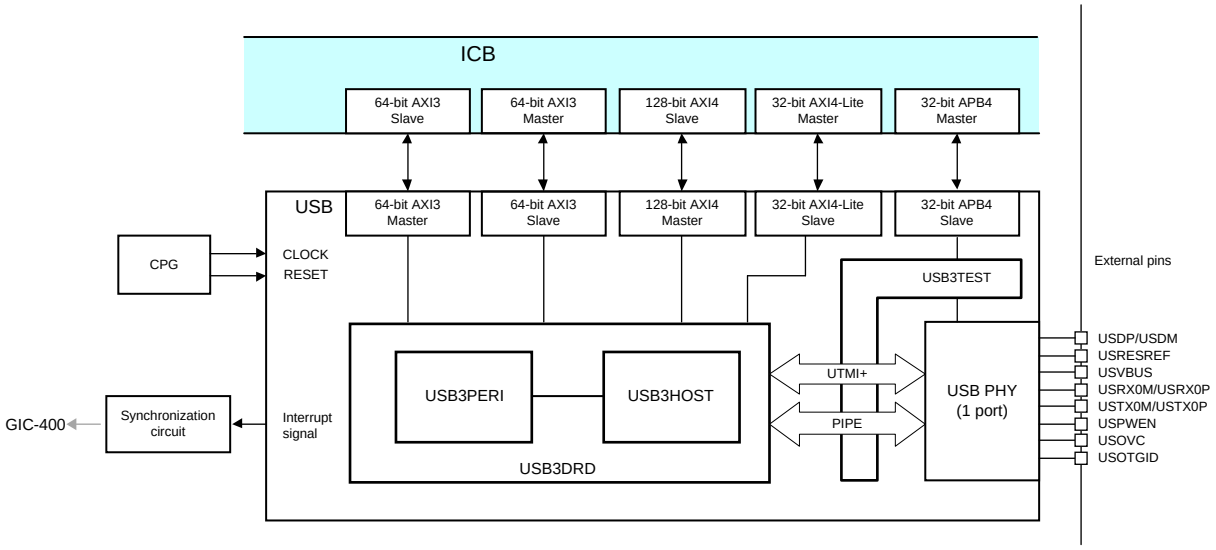
Item	Description
USB3DRD function	• Role swapping function by the ID pin of the Micro-AB receptacle • Battery Charging Specification Revision 1.2
USB3HOST function	• Support for super-speed (5 Gbps), high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transfer • Support for all transfer types: isochronous, interrupt, control, and bulk • Support for isochronous and interrupt high-band transfer • Compliant with the eXtensible Host Controller Interface(xHCI) Specification for USB
USB3PERI function	• Support for super-speed (5 Gbps), high-speed (480 Mbps), and full-speed (12 Mbps) transfer (low-speed (1.5 Mbps) is not supported) • Support for interrupt, control, and bulk transfer (isochronous transfer is not supported) • Number of pipes: 16, Buffer size: IN: 17 Kbytes; OUT: 16 Kbytes **[USB3.1 Function]** • Max. packet size: 512 bytes for PIPE0, up to 1024 bytes for others (*large bandwidth is not supported) • Max. burst size: Fixed to 1 for PIPE0 (control), between 1 and 16 (bulk) and between 1 and 3 (interrupt) • Max. sequence number: Fixed to 31 **[USB2.0 Function]** • Max. packet size: 64 bytes for PIPE0, up to 1024 bytes for others (*large bandwidth is not supported)
USB3TEST function	• Reset control • Control of PHY input pins • Monitor of PHY output pins

Table 35.1-2 Supported Speed Types

	Speed Type			
Function	Super Speed (5 Gbps)	High Speed (480 Mbps)	Full Speed (12 Mbps)	Low Speed (1.5 Mbps)
Host Controller	✓	✓	✓	✓
Peripheral Controller	✓	✓	✓	—

35.2 Connection Configuration

Figure 35.2-1 shows the connection configuration of this unit.



PIPE: The PHY Interface for the PCI Express, SATA, and USB3.1

UTMI+: The USB2.0 Transceiver Macrocell Interface Plus

Figure 35.2-1 USB Connection Configuration

35.3 Pin Functions

Table 35.3-1 lists the external pins of the USB.

Table 35.3-1 List of External Pins

Pin name	I/O	Function
USDP	IO	USB2.0 USB D+ signal (positive)
USDM	IO	USB2.0 USB D− signal (negative)
USRESREF	Input	Reference resistor connection pin * To connect a pull-down resistor. Resistance: 200Ω ±1%
USVBUS	Input	USB 5-V signal detection pin * Resistance partial pressure outside the chip*1
USRX0M	Input	USB3.1 super-speed differential reception pair (negative)
USRX0P	Input	USB3.1 super-speed differential reception pair (positive)
USTX0M	Output	USB3.1 super-speed differential transmission pair (negative)
USTX0P	Output	USB3.1 super-speed differential transmission pair (positive)
USOTGID	Input	ID detection (OTG ID input, 0: Host, 1: Peripheral)
USPWEN	Output	VBUS control signal (active high)
USOVC	Input	Overcurrent detection (active low)

Note 1. For the details, see the section of Pin.

35.4 USB3.1 Gen1 Dual Role Device Controller (USB3DRD)

35.4.1 Introduction

The USB3.1 Gen1 Dual Role Device Controller (USB3DRD) complies with the Universal Serial Bus (USB) 3.1 Specification.

This unit operates in DRD mode.

35.4.1.1 Features

The functions of the USB3DRD are outlined below.

(1) USB Functions

The USB3DRD is compliant with *the Universal Serial Bus 3.1 Specification Revision 1.0 and ECNs* approved in June 27, 2017 and *the Universal Serial Bus Specification Revision 2.0* and *the Universal Serial Bus Specification Revision 2.0 and ECNs related to LPM functions* as of July 16, 2007 and October 11, 2011.

[Host Controller-portion]

- Supports 1 downstream port.
- Supports Super Speed (5 Gbps), High Speed (480 Mbps), Full Speed (12 Mbps), and Low Speed (1.5 Mbps).
- Supports all transfer-types: Control, Bulk, Interrupt, Isochronous, and these split-transactions.
- Supports Power Control and Over Current Detection.
- Implements the following USB2.0 ECNs USB 2.0 Link Power Management Addendum and LPM functions that are compliant with the xHCI specification.
  - USB 2.0 Link Power Management Addendum Engineering Change Notice to the USB 2.0 specification as of July 16, 2007
  - Errata for USB 2.0 ECN: Link Power Management (LPM) – 7/2007 as of October 11, 2011
- Compliant with *the eXtensible Host Controller Interface for the Universal Serial Bus Specification Revision 1.1*.

[Peripheral Controller-portion]

- Supports 1 upstream port.
- Supports Super Speed (5 Gbps), High Speed (480 Mbps), and Full Speed (12 Mbps). (Low Speed (1.5 Mbps) is not supported.)
- Supports Control, Bulk, and Interrupt transfers. (Isochronous is not supported.)
- Up to 30 PIPEs (PIPE0 not included) can be used (configurable)
- Stream ID control supported (UASP can be supported)
- Supports Suspend/Resume function
  - USB3.1 Power Management by sending/receiving of link commands is supported (PHY clock stop is supported)
  - Remote Wakeup request can be transmitted
  - USB2.0 Link Power Management (LPM) is supported

(2) Dual Role Device Function

The USB3DRD supports the following function that is compliant with *the On-The-Go and Embedded Host Supplement to the USB Revision 3.0 Specification Revision 1.1* as of May 10, 2012 (OTG and EH 3.0 Rev.1.1) and *On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification Revision 2.0 version 1.1a* July 27, 2012 (OTG and EH 2.0 Ver.1.1a).

[On-The-Go]

- The USB3DRD supports the following function of On-The-Go (OTG).
  - Role swapping function by the ID pin of the Micro-AB receptacle

(3) Battery Charging Functions

The USB3DRD supports the following functions that are compliant with *the Battery Charging Specification Revision 1.2*.

[Charging port device (Host Controller-portion)]

- The USB3DRD supports the following modes of chargeable portable devices.
  - Standard Downstream Port (SDP) Mode
  - Charging Downstream Port (CDP) Mode
  - Dedicated Charging Port (DCP) Mode

[Portable device (Peripheral Controller-portion)]

- The USB3DRD supports the following modes of portable devices.
  - Standard Downstream Port (SDP) Mode
  - Charging Downstream Port (CDP) Mode
  - Dedicated Charging Port (DCP) Mode
- The USB3DRD also supports the following function of portable devices.
  - Data Contact Detect (DCD)

35.4.2 Resets

35.4.2.1 External Reset Inputs

The USB3DRD has the following signals as the reset input.

Table 35.4-1 USB3DRD Reset Inputs Information

Reset's Name	Description
aresetn_h	AXI bus reset signal to the AXI interface of the Host controller-portion. This signal is also the HW Reset input for the whole Host controller-portion. (This signal from CPG is USB_ARESETN_H)
aresetn_p	AXI bus reset signal to the AXI interface of the Peripheral controller-portion. This signal is also the HW Reset input for the whole Peripheral controller-portion. (This signal from CPG is USB_ARESETN_P)
drd_reset	This signal is the HW Reset input for the whole USB3DRD's logic including both of the Host Controller-portion and the Peripheral Controller-portion. (This signal from CPG is USB_DRD_RESET)

35.4.3 Interrupts

35.4.3.1 Interrupt Diagram

In the USB3DRD, the elements of interrupt are notified by the following layered structure.

The below red-colored interrupts are main interrupts.

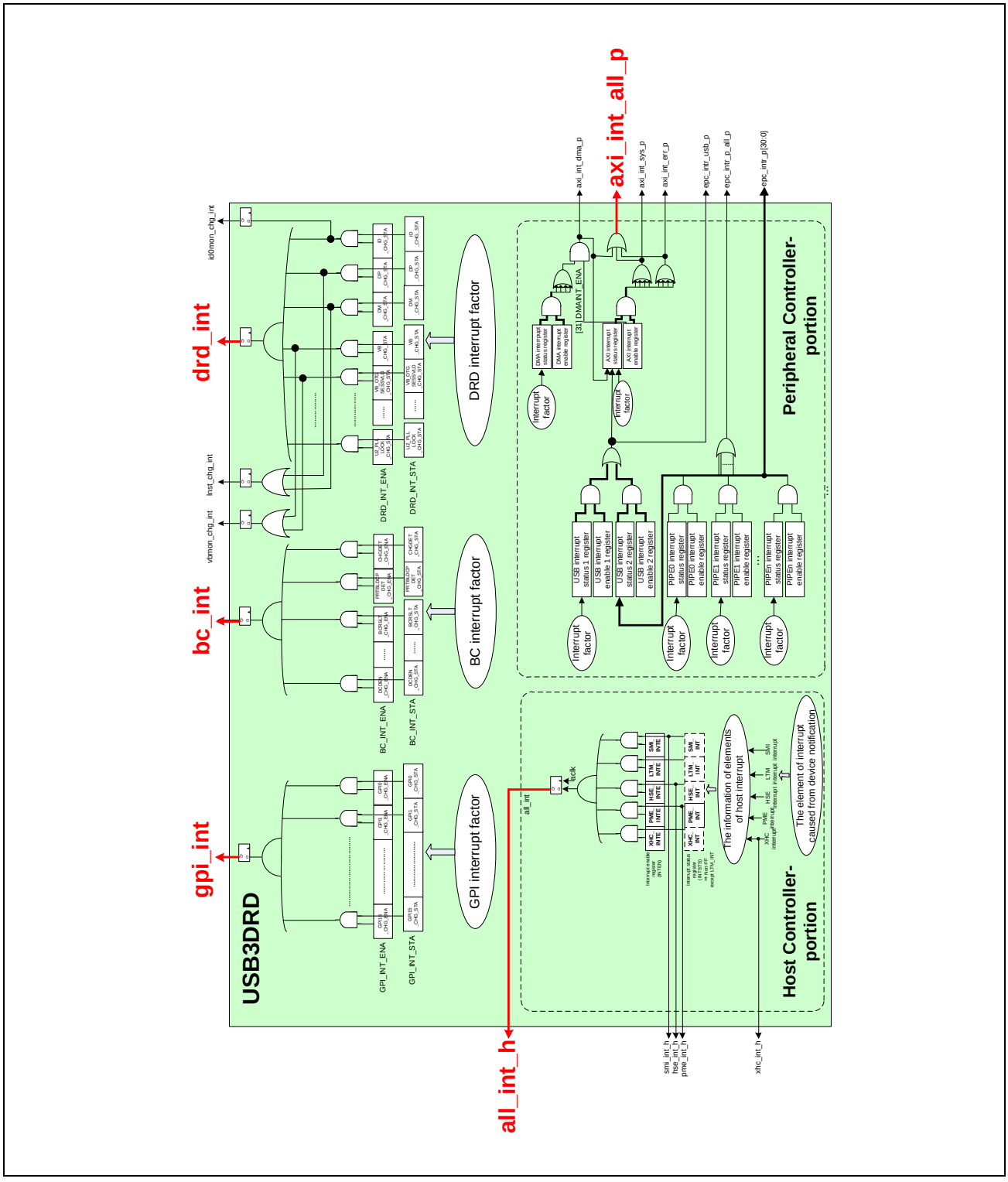


Figure 35.4-1 USB3DRD Interrupts Structure

35.4.3.2 Interrupt Sources

The USB3DRD has the following three categories as the interrupt sources.

1. The related DRD specific's interrupt-elements
2. The related Host Controller-portion's interrupt-elements
3. The related Peripheral Controller-portion's interrupt-elements

(1) Related DRD Specific's Interrupt-Elements

The USB3DRD has the following interrupt sources as the related DRD specific's interrupt-elements.

Table 35.4-2 Information of Related DRD Specific's Interrupt-Elements (1/2)

Interrupt Name	Type of Notification	Description
vbmon _chg_int	Level	The interrupt signal to indicate to change the voltage level of the USB-VBUS line. This signal is monitored whether the signal level of VBUS is changed or not. This signal is asserted by one of the following conditions. • DRD_INT_ENA.VB_CHG_ENA = 1 and DRD_INT_STA.VB_CHG_STA = 1 • DRD_INT_ENA.VB_OTGSESSVLD_CHG_ENA = 1 and DRD_INT_STA.VB_OTGSESSVLD_CHG_STA = 1
Inst_chg _int	Level	The interrupt signal to indicate to change the signal level of the UTMI+ LineState[1:0]. This signal is monitored whether the signal level of "utmi_linestate"'s each bit is changed or not. This signal is asserted by one of the following conditions. • DRD_INT_ENA.DM_CHG_ENA = 1 and DRD_INT_STA.DM_CHG_STA = 1 • DRD_INT_ENA.DP_CHG_ENA = 1 and DRD_INT_STA.DP_CHG_STA = 1
id0mon _chg_int	Level	The interrupt signal to indicate to change the signal level of USB3.1 AB receptacle's ID-pin. This signal is monitored whether the signal level of ID pin is changed or not. This signal is asserted by the following condition. • DRD_INT_ENA.ID_CHG_ENA = 1 and DRD_INT_STA.ID_CHG_STA = 1
drd_int	Level	The interrupt signal to be logical ORed all interrupt elements in DRD_INT_STA register. All interrupt elements of above "vbmon_chg_int", "Inst_chg_int" and "id0mon_chg_int" are included in this interrupt elements. This signal is asserted by one of the following conditions. • DRD_INT_ENA.U2_PLLLOCK_CHG_ENA = 1 and DRD_INT_STA.U2_PLLLOCK_CHG_STA = 1 • DRD_INT_ENA.HC_PP_CHG_ENA = 1 and DRD_INT_STA.HC_PP_CHG_STA = 1 • DRD_INT_ENA.OC_CHG_ENA = 1 and DRD_INT_STA.OC_CHG_STA = 1 • DRD_INT_ENA.VB_OTGSESSVLD_CHG_ENA = 1 and DRD_INT_STA.VB_OTGSESSVLD_CHG_STA = 1 • DRD_INT_ENA.VB_CHG_ENA = 1 and DRD_INT_STA.VB_CHG_STA = 1 • DRD_INT_ENA.DM_CHG_ENA = 1 and DRD_INT_STA.DM_CHG_STA = 1 • DRD_INT_ENA.DP_CHG_ENA = 1 and DRD_INT_STA.DP_CHG_STA = 1 • DRD_INT_ENA.ID_CHG_ENA = 1 and DRD_INT_STA.ID_CHG_STA = 1
bc_int	Level	The interrupt signal to be logical ORed all Interrupt elements in BC_INT_STA register. One of elements is whether the signal level of either PRTBL_DET or CHG_DET is changed or not. This signal is asserted by one of the following conditions. • BC_INT_ENA.DCDEN_CHG_ENA = 1 and BC_INT_STA.DCDEN_CHG_STA = 1 • BC_INT_ENA.BCRSLT_CHG_ENA = 1 and BC_INT_STA.BCRSLT_CHG_STA = 1 • BC_INT_ENA.PRTBLDCPDET_CHG_ENA = 1 and BC_INT_STA.PRTBLDCPDET_CHG_STA = 1 • BC_INT_ENA.CHGDET_CHG_ENA = 1 and BC_INT_STA.CHGDET_CHG_STA = 1

Table 35.4-2 Information of Related DRD Specific's Interrupt-Elements (2/2)

Interrupt Name	Type of Notification	Description
gpi_int	Level	The interrupt signal to indicate to change global purpose input signal "gpi[x] (x:0 to 15)" This signal is monitored whether the signal level of each "gpi[x]" is changed or not. This interrupt is used for debugging purpose only. This signal is asserted by one of the following conditions. • GPI_INT_ENA.GPI15_CHG_ENA = 1 and GPI_INT_STA.GPI15_CHG_STA = 1 • GPI_INT_ENA.GPI14_CHG_ENA = 1 and GPI_INT_STA.GPI14_CHG_STA = 1 • GPI_INT_ENA.GPI13_CHG_ENA = 1 and GPI_INT_STA.GPI13_CHG_STA = 1 • GPI_INT_ENA.GPI12_CHG_ENA = 1 and GPI_INT_STA.GPI12_CHG_STA = 1 • GPI_INT_ENA.GPI11_CHG_ENA = 1 and GPI_INT_STA.GPI11_CHG_STA = 1 • GPI_INT_ENA.GPI10_CHG_ENA = 1 and GPI_INT_STA.GPI10_CHG_STA = 1 • GPI_INT_ENA.GPI9_CHG_ENA = 1 and GPI_INT_STA.GPI9_CHG_STA = 1 • GPI_INT_ENA.GPI8_CHG_ENA = 1 and GPI_INT_STA.GPI8_CHG_STA = 1 • GPI_INT_ENA.GPI7_CHG_ENA = 1 and GPI_INT_STA.GPI7_CHG_STA = 1 • GPI_INT_ENA.GPI6_CHG_ENA = 1 and GPI_INT_STA.GPI6_CHG_STA = 1 • GPI_INT_ENA.GPI5_CHG_ENA = 1 and GPI_INT_STA.GPI5_CHG_STA = 1 • GPI_INT_ENA.GPI4_CHG_ENA = 1 and GPI_INT_STA.GPI4_CHG_STA = 1 • GPI_INT_ENA.GPI3_CHG_ENA = 1 and GPI_INT_STA.GPI3_CHG_STA = 1 • GPI_INT_ENA.GPI2_CHG_ENA = 1 and GPI_INT_STA.GPI2_CHG_STA = 1 • GPI_INT_ENA.GPI1_CHG_ENA = 1 and GPI_INT_STA.GPI1_CHG_STA = 1 • GPI_INT_ENA.GPI0_CHG_ENA = 1 and GPI_INT_STA.GPI0_CHG_STA = 1

(2) Related Host Controller-Portion's Interrupt-Elements

All interrupt-elements of the category "2" in **Section 35.4.3.2, Interrupt Sources** is logical ORed and output to "all_int_h".

Refer to the Host Controller-portion (USB3HOST)'s section for details.

(3) Related Peripheral Controller-Portion's Interrupt-Elements

All interrupt-elements of the category "3" in **Section 35.4.3.2, Interrupt Sources** is logical ORed and output to "axi_int_all_p".

Refer to the Peripheral Controller-portion (USB3PERI)'s section for details.

35.4.4 Registers Specification

For the register base address (<USB_S1_base>), see the section of Address Map.

35.4.4.1 Register Overview

When the USB3DRD core works in DRD mode, DRD registers are mapped in the AXI address space for the Peripheral role.

The AXI address map is as follows.

The 12-bit offset address space from 400h to 4FFh is mapped as the DRD Registers' address space.

Therefore, in this mode, DRD registers are accessed by using the AXI slave interface of the Peripheral Controller-portion.

(i.e. in this mode, DRD registers is not mapped in the AXI address space for the Host role.)

Figure 35.4-2 AXI Address Space for DRD Registers in DRD Mode

NOTE

The DRD registers are located in USB3DRD and are not located in EPC RAM of the Peripheral Controller-portion.

35.4.4.2 Registers List

(1) DRD Common Registers

Table 35.4-3 List of DRD Common Registers (1/2)

Offset Address / 12 bits / DRD Mode (Peripheral)	bit31 / bit23 / bit15 / bit7	bit30 / bit22 / bit14 / bit6	bit29 / bit21 / bit13 / bit5	bit28 / bit20 / bit12 / bit4	bit27 / bit19 / bit11 / bit3	bit26 / bit18 / bit10 / bit2	bit25 / bit17 / bit9 / bit1	bit24 / bit16 / bit8 / bit0
DRD Common Control Register (USB_PERI_DRD_CON)								
403h	PERI_RST	HOST_RST	U2PHY_REG_RST	U3PHY_REG_RST	—	—	—	PERI_CON
402h	—	—	—	—	—	—	—	U2_SUSPEND_CON
401h	DM_RPD_CON_ENA	DM_RPD_CON	CONNECT_SEL	IDPSRCEN_CON	IDMSINKEN_CON	IDPSINKEN_CON	VDMSRCEN_CON	VDPSRCEN_CON
400h	—	—	—	—	—	—	VB_FORCE_ENA	VB_CON
DRD Common Control 2 Register (USB_PERI_DRD_CON2)								
407h	Renesas Private	Renesas Private	—	—	—	—	—	—
406h	—	—	—	—	—	—	—	—
405h	—	—	—	—	—	—	—	—
404h	—	—	—	—	—	—	—	—
Reserved								
40Bh	—	—	—	—	—	—	—	—
40Ah	—	—	—	—	—	—	—	—
409h	—	—	—	—	—	—	—	—
408h	—	—	—	—	—	—	—	—
Reserved								
40Fh	—	—	—	—	—	—	—	—
40Eh	—	—	—	—	—	—	—	—
40Dh	—	—	—	—	—	—	—	—
40Ch	—	—	—	—	—	—	—	—
DRD Status Register (USB_PERI_DRD_STA)								
413h	—	—	—	—	—	—	—	—
412h	—	—	—	—	—	—	—	U2_PLLLOCK_STA
411h	—	—	—	—	HC_PP_STA	OC_STA	VB_OTGSESSVLD_STA	VB_STA
410h	—	—	—	—	—	DM_STA	DP_STA	ID_STA

Table 35.4-3 List of DRD Common Registers (2/2)

	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
Offset Address	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
12 bits	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
DRD Mode (Peripheral)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DRD Interrupt Status Register (USB_PERI_DRD_INT_STA)								
417h	—	—	—	—	—	—	—	—
416h	—	—	—	—	—	—	—	U2 _PLLLOCK _CHG_STA
415h	—	—	—	—	HC_PP _CHG_STA	OC_CHG _STA	VB _OTGSESS VLD _CHG_STA	VB_CHG _STA
414h	—	—	—	—	—	DM_CHG _STA	DP_CHG _STA	ID_CHG _STA
DRD Interrupt Enable Register (USB_PERI_DRD_INT_ENA)								
41Bh	—	—	—	—	—	—	—	—
41Ah	—	—	—	—	—	—	—	U2 _PLLLOCK _CHG_ENA
419h	—	—	—	—	HC_PP _CHG_ENA	OC_CHG _ENA	VB _OTGSESS VLD _CHG_ENA	VB_CHG _ENA
418h	—	—	—	—	—	DM_CHG _ENA	DP_CHG _ENA	ID_CHG _ENA
Reserved								
41Fh	—	—	—	—	—	—	—	—
41Eh	—	—	—	—	—	—	—	—
41Dh	—	—	—	—	—	—	—	—
41Ch	—	—	—	—	—	—	—	—

(2) Battery Charging Registers

Table 35.4-4 List of Battery Charging Registers

Offset Address 12 bits DRD Mode (Peripheral)	bit31 bit23 bit15 bit7	bit30 bit22 bit14 bit6	bit29 bit21 bit13 bit5	bit28 bit20 bit12 bit4	bit27 bit19 bit11 bit3	bit26 bit18 bit10 bit2	bit25 bit17 bit9 bit1	bit24 bit16 bit8 bit0
Battery Charging Status Register (USB_PERI_BC_STA)								
423h	—	—	—	—	—	—	—	—
422h	—	—	—	—	—	—	—	—
421h	—	—	—	—	—	DCDEN_STA	BCRSLT_STA	
420h	—	—	—	—	—	—	PRTBLDCPDET_STA	CHGDET_STA
Battery Charging Interrupt Status Register (USB_PERI_BC_INT_STA)								
427h	—	—	—	—	—	—	—	—
426h	—	—	—	—	—	—	—	—
425h	—	—	—	—	—	DCDEN_CHG_STA	—	BCRSLT_CHG_STA
424h	—	—	—	—	—	—	PRTBLDCPDET_CHG_STA	CHGDET_CHG_STA
Battery Charging Interrupt Enable Register (USB_PERI_BC_INT_ENA)								
42Bh	—	—	—	—	—	—	—	—
42Ah	—	—	—	—	—	—	—	—
429h	—	—	—	—	—	DCDEN_CHG_ENA	—	BCRSLT_CHG_ENA
428h	—	—	—	—	—	—	PRTBLDCPDET_CHG_ENA	CHGDET_CHG_ENA
Reserved								
42Fh	—	—	—	—	—	—	—	—
42Eh	—	—	—	—	—	—	—	—
42Dh	—	—	—	—	—	—	—	—
42Ch	—	—	—	—	—	—	—	—

(3) Global Purpose Registers

Table 35.4-5 List of Global Purpose Registers

	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
Offset Address	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
12 bits	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
DRD Mode (Peripheral)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Global Purpose Output Control Register (USB_PERI_GPO_CON)								
433h	—	—	—	—	—	—	—	—
432h	—	—	—	—	—	—	—	—
431h	GPO15_CON	GPO14_CON	GPO13_CON	GPO12_CON	GPO11_CON	GPO10_CON	GPO9_CON	GPO8_CON
430h	GPO7_CON	GPO6_CON	GPO5_CON	GPO4_CON	GPO3_CON	GPO2_CON	GPO1_CON	GPO0_CON
Global Purpose Input Status Register (USB_PERI_GPI_STA)								
437h	—	—	—	—	—	—	—	—
436h	—	—	—	—	—	—	—	—
435h	GPI15_STA	GPI14_STA	GPI13_STA	GPI12_STA	GPI11_STA	GPI10_STA	GPI9_STA	GPI8_STA
434h	GPI7_STA	GPI6_STA	GPI5_STA	GPI4_STA	GPI3_STA	GPI2_STA	GPI1_STA	GPI0_STA
Global Purpose Input Interrupt Status Register (USB_PERI_GPI_INT_STA)								
43Bh	—	—	—	—	—	—	—	—
43Ah	—	—	—	—	—	—	—	—
439h	GPI15_CHG_STA	GPI14_CHG_STA	GPI13_CHG_STA	GPI12_CHG_STA	GPI11_CHG_STA	GPI10_CHG_STA	GPI9_CHG_STA	GPI8_CHG_STA
438h	GPI7_CHG_STA	GPI6_CHG_STA	GPI5_CHG_STA	GPI4_CHG_STA	GPI3_CHG_STA	GPI2_CHG_STA	GPI1_CHG_STA	GPI0_CHG_STA
Global Purpose Input Interrupt Enable Register (USB_PERI_GPI_INT_ENA)								
43Fh	—	—	—	—	—	—	—	—
43Eh	—	—	—	—	—	—	—	—
43Dh	GPI15_CHG_ENA	GPI14_CHG_ENA	GPI13_CHG_ENA	GPI12_CHG_ENA	GPI11_CHG_ENA	GPI10_CHG_ENA	GPI9_CHG_ENA	GPI8_CHG_ENA
43Ch	GPI7_CHG_ENA	GPI6_CHG_ENA	GPI5_CHG_ENA	GPI4_CHG_ENA	GPI3_CHG_ENA	GPI2_CHG_ENA	GPI1_CHG_ENA	GPI0_CHG_ENA

(4) Reserved Address Space

Table 35.4-6 Reserved Address Space Information

	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
Offset Address	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
12 bits	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
DRD Mode (Peripheral)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved								
460h to 4FFh	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—

35.4.4.3 Register Initial Value

Table 35.4-7 List of Initial Values for DRD Registers

Offset Address 12 bits DRD Mode (Peripheral)	Register Name	Initial Value	
400h	USB_PERI_DRD_CON	DRD mode	C100_0000h
404h	USB_PERI_DRD_CON2	0000_0000h	
408h	Reserved	0000_0000h	
40Ch	Reserved	0000_0000h	
410h	USB_PERI_DRD_STA	This value depends on several external input-pins' values.	
414h	USB_PERI_DRD_INT_STA	0000_0000h	
418h	USB_PERI_DRD_INT_ENA	0000_0000h	
41Ch	Reserved	0000_0000h	
420h	USB_PERI_BC_STA	0000_0000h	
424h	USB_PERI_BC_INT_STA	0000_0000h	
428h	USB_PERI_BC_INT_ENA	0000_0000h	
42Ch	Reserved	0000_0000h	
430h	USB_PERI_GPO_CON	0000_0000h	
434h	USB_PERI_GPI_STA	This value depends on "gpi*" (* : 0 to 15).	
438h	USB_PERI_GPI_INT_STA	0000_0000h	
43Ch	USB_PERI_GPI_INT_ENA	0000_0000h	
440h	U2PHYRCNTSET	0000_0000h	
444h	U2PHYRRD	0000_0000h	
448h	Reserved	0000_0000h	
44Ch	Reserved	0000_0000h	
450h	U3PHYRCNTSET	0000_0000h	
454h	U3PHYRWD	0000_0000h	
458h	U3PHYRRD	This value depends on USB_HOST_U3PHYRWD.	
45Ch	Reserved	0000_0000h	
460h to 4FFh	Reserved	Each bit is read "0b" as the value.	

35.4.5 Register Descriptions

The function description of each register is given below.

The prefix (USB_PERI_) of the register names is omitted in the register descriptions and the field descriptions in this section.

35.4.5.1 DRD Common Registers

(1) DRD Common Control Register (USB_PERI_DRD_CON)

This register controls the common functions.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0400h

Initial Value: C100_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PERI_RST	HOST_RST	U2PHY_REG_RST	U3PHY_REG_RST	—	—	—	PERI_CON	—	—	—	—	—	—	—	U2_SUSPEND_CON
Initial Value	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	R	R	R	RW	R	R	R	R	R	R	R	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DM_RPD_CON_ENA	DM_RPD_CON	—	IDPSRCEN_CON	IDMSINKEN_CON	IDPSINKEN_CON	VDMSRCEN_CON	VDPSRCEN_CON	—	—	—	—	—	—	VB_FORCE_ENA	VB_CON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	R	RW	RW	RW	RW	RW	R	R	R	R	R	R	RW	RW

Table 35.4-8 USB_PERI_DRD_CON Register Contents (1/2)

Bit Position	Bit Name	Description
31	PERI_RST	The reset control bit to the Peripheral Controller-portion.
30	HOST_RST	The reset control bit to the Host Controller-portion.
29	U2PHY_REG_RST	The reset control bit to the USB2.0 PHY Register Interface. 1b: Reset active. 0b: Reset inactive.
28	U3PHY_REG_RST	The reset control bit to the USB3.1 PHY Register Interface. 1b: Reset active. 0b: Reset inactive.
27 to 25	—	Reserved
24	PERI_CON	[DRD mode] The reset control bit to the Host Controller-portion.
23 to 17	—	Reserved
16	U2_SUSPEND_CON	The control bit to control SuspendM signal of UTMI+ interface by the DRD specific portion. 1b: Request to set SuspendM to ‘0’ (Accept to move the suspend state) 0b: Request to set SuspendM to ‘1’ (Request to stay the state supplied UTMI+ clock signal.)
15	DM_RPD_CON_ENA	The bit to enable the control DM’s pull-down resistor by DRD_CON.DM_RPD_CON. This bit can be set to ‘1’ at the same timing that DRD_CON.DM_RPD_CON is set to ‘1’. 1b: Enable 0b: Disable

Table 35.4-8 USB_PERI_DRD_CON Register Contents (2/2)

Bit Position	Bit Name	Description
14	DM_RPD_CON	The bit to control the operation of DM-Line's pull-down resistor. This bit can be set to '1' at the same timing that DRD_CON.DM_PRD_CON.ENA is set to '1'. Table 35.4-8-1 DRD_CON DM_RPD_CON_ENA / SW Attribute 1b / RW 0b / R
13	—	Reservd.
12	IDPSRCEN_CON	[Host role in DRD mode] This bit is not used. [Peripheral role in DRD mode] The bit to enable D+ Source Voltage.
11	IDMSINKEN_CON	[Host role in DRD mode] This bit is not used. [Peripheral role in DRD mode] The bit to enable D- Sink Current.
10	IDPSINKEN_CON	[Host role in DRD mode] This bit is not used. [Peripheral role in DRD mode] The bit to enable D+ Sink Current.
9	VDMSRCEN_CON	[Host role in DRD mode] This bit is not used. [Peripheral role in DRD mode] The bit to enable D- Source Voltage.
8	VDPSRCEN_CON	[Host role in DRD mode] This bit is not used. [Peripheral role in DRD mode] The bit to enable D+ Source Voltage.
7 to 2	—	Reserved
1	VB_FORCE_ENA	[Host role in DRD mode] The bit to enable the control of USB-VBUS Output by DRD_CON.VB_CON. [Peripheral role in DRD mode] This bit is not used.
0	VB_CON	The bit to control the USB-VBUS Output. [A-device in DRD mode] When this bit is set to '1', USPWEN outputs '1'. [B-device in DRD mode] This bit is not used. 1b: USPWEN outputs '1'. 0b: USPWEN is not controlled by this bit. This bit's pre-condition is that DRD_CON.PERI_CON is set to '1' or that DRD_CON.VB_FORCE_ENA is set to '1'. This bit can be set to '1' at the same timing that either DRD_CON.PERI_CON or DRD_CON.VB_FORCE_ENA is set to '1'. Table 35.4-8-2 DRD_CON PERI_CON / DRD_CON VB_FORCE_ENA / SW Attribute 1b / Don't care / RW Don't care / 1b / RW 0b / 0b / R

(2) DRD Common Control 2 Register (USB_PERI_DRD_CON2)

This register controls the common functions.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0404h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Renesas Private		—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.4-9 USB_PERI_DRD_CON2 Register Contents

Bit Position	Bit Name	Description
31, 30	—	Renesas Private bits. These bits shall be set to 0b.
29 to 0	—	Reserved

(3) DRD Status Register (USB_PERI_DRD_STA)

This register shows the DRD status.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0410h

Initial Value: 000x_0x0xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U2_PLLLOCK_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	HC_PP_STA	OC_STA	VB_OTGSESSVLD_STA	VB_STA	—	—	—	—	—	DM_STA	DP_STA	ID_STA
Initial Value	0	0	0	0	0	0	x	x	0	0	0	0	0	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.4-10 USB_PERI_DRD_STA Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved
16	U2_PLLLOCK_STA	The bit to indicate the status of USB2.0 PHY PLL Lock. 1b: USB2.0 PHY PLL is locked. 0b: USB2.0 PHY PLL is not locked.
15 to 12	—	Reserved
11	HC_PP_STA	The bit to indicate the status of USPWEN signal from the Host Controller-portion.
10	OC_STA	The bit to indicate the notification of the ‘Over Current’ from Power IC. 1b: The situation of ‘Over Current’ has occurred. 0b: The situation of ‘Over Current’ has not occurred.
9	VB_OTGSESSVLD_STA	The bit to indicate the status of OTG Device Session valid. 1b: The voltage on VBUS is above the OTG Device Session Valid threshold. 0b: The voltage on VBUS is below the OTG Device Session Valid threshold.
8	VB_STA	The bit to indicate the status of VBUS. The initial value reflects the initial value of VBUS.
7 to 3	—	Reserved
2	DM_STA	The bit to indicate the status of ‘utmi_linestate[1]’. The initial value reflects the initial value of ‘utmi_linestate[1]’.
1	DP_STA	The bit to indicate the status of ‘utmi_linestate[0]’. The initial value reflects the initial value of ‘utmi_linestate[0]’.
0	ID_STA	The initial value reflects the initial value of DRD ID pin. [DRD mode] The bit to indicate the status of USOTGID.

(4) DRD Interrupt Status Register (USB_PERI_DRD_INT_STA)

This register shows the DRD interrupt status. These bits are cleared by writing 1.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0414h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U2_PLLLOCK_CHG_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	HC_PP_CHG_STA	OC_CHG_STA	VB_OTGSESSVLD_CHG_STA	VB_CHG_STA	—	—	—	—	—	DM_CHG_STA	DP_CHG_STA	ID_CHG_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW1	RW1	RW1	RW1	R	R	R	R	R	RW1	RW1	RW1

Table 35.4-11 USB_PERI_DRD_INT_STA Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved
16	U2_PLLLOCK_CHG_STA	The bit to indicate the status-change of DRD_STA.U2_PLLLOCK_STA. 1b: The status is changed. 0b: The status is not changed.
15 to 12	—	Reserved
11	HC_PP_CHG_STA	The bit to indicate the status-change of DRD_STA.HC_PP_STA. 1b: The status is changed. 0b: The status is not changed.
10	OC_CHG_STA	The bit to indicate the status-change of DRD_STA.OC_STA. 1b: The status is changed. 0b: The status is not changed.
9	VB_OTGSESSVLD_CHG_STA	The bit to indicate the status-change of DRD_STA.VB_OTGSESSVLD_STA. 1b: The status is changed. 0b: The status is not changed.
8	VB_CHG_STA	The bit to indicate the status-change of DRD_STA.VB_STA. 1b: The status is changed. 0b: The status is not changed.
7 to 3	—	Reserved
2	DM_CHG_STA	The bit to indicate the status-change of DRD_STA.DM_STA. 1b: The status is changed. 0b: The status is not changed.
1	DP_CHG_STA	The bit to indicate the status-change of DRD_STA.DP_STA. 1b: The status is changed. 0b: The status is not changed.
0	ID_CHG_STA	The bit to indicate the status-change of DRD_STA.ID_STA. 1b: The status is changed. 0b: The status is not changed.

(5) DRD Interrupt Enable Register (USB_PERI_DRD_INT_ENA)

This register is used to enable DRD interrupts.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0418h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U2_PLLLOCK_CHG_ENA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	HC_PP_CHG_ENA	OC_CHG_ENA	VB_OTGSESSVLD_CHG_ENA	VB_CHG_ENA	—	—	—	—	—	DM_CHG_ENA	DP_CHG_ENA	ID_CHG_ENA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	R	R	R	R	R	RW	RW	RW

Table 35.4-12 USB_PERI_DRD_INT_ENA Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 17	—	Reserved
16	U2_PLLLOCK_CHG_ENA	This bit selects whether the interrupt state of DRD_INT_STA.U2_PLLLOCK_CHG_STA is joined ‘drd_int’ interrupt output or not. 1b: The interrupt state is joined ‘drd_int’. 0b: The interrupt state is not joined ‘drd_int’.
15 to 12	—	Reserved
11	HC_PP_CHG_ENA	This bit selects whether the interrupt state of DRD_INT_STA.HC_PP_CHG_STA is joined ‘drd_int’ interrupt output or not. 1b: The interrupt state is joined ‘drd_int’. 0b: The interrupt state is not joined ‘drd_int’.
10	OC_CHG_ENA	This bit selects whether the interrupt state of DRD_INT_STA.OC_CHG_STA is joined ‘drd_int’ interrupt output or not. 1b: The interrupt state is joined ‘drd_int’. 0b: The interrupt state is not joined ‘drd_int’.
9	VB_OTGSESSVLD_CHG_ENA	This bit selects whether the interrupt state of DRD_INT_STA.VB_OTGSESSVLD_CHG_STA is joined ‘vbmon_chg_int’ interrupt output or not. 1b: The interrupt state is joined 'vbmon_chg_int'. 0b: The interrupt state is not joined 'vbmon_chg_int’.
8	VB_CHG_ENA	This bit selects whether the interrupt state of DRD_INT_STA.VB_CHG_STA is joined ‘vbmon_chg_int’ interrupt output or not. 1b: The interrupt state is joined 'vbmon_chg_int’ and 'drd_int'. 0b: The interrupt state is not joined 'vbmon_chg_int’.
7 to 3	—	Reserved
2	DM_CHG_ENA	This bit selects whether the interrupt state of DRD_INT_STA.DM_CHG_STA is joined ‘lnst_chg_int’ interrupt output or not. 1b: The interrupt state is joined ‘lnst_chg_int’ and ‘drd_int’. 0b: The interrupt state is not joined ‘lnst_chg_int’.

Table 35.4-12 USB_PERI_DRD_INT_ENA Register Contents (2/2)

Bit Position	Bit Name	Description
1	DP_CHG_ENA	This bit selects whether the interrupt state of DRD_INT_STA.DP_CHG_STA is joined 'Inst_chg_int' interrupt output or not. 1b: The interrupt state is joined 'Inst_chg_int' and 'drd_int'. 0b: The interrupt state is not joined 'Inst_chg_int'.
0	ID_CHG_ENA	This bit selects whether the interrupt state of DRD_INT_STA.ID_CHG_STA is joined 'id0mon_chg_int' interrupt output or not. 1b: The interrupt state is joined ' id0mon_chg_int'. 0b: The interrupt state is not joined ' id0mon_chg_int'.

35.4.5.2 Battery Charging Registers

(1) Battery Charging Status Register (USB_PERI_BC_STA)

This register shows the Battery Charging status.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0420h

Initial Value: 0000_000xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	DCDEN_STA	BCRSLT_STA		—	—	—	—	—	—	PRTBLDCPDET_STA	CHGDET_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x
R/W	R	R	R	R	R	RW	RW	R	R	R	R	R	R	R	R	R

Table 35.4-13 USB_PERI_BC_STA Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 11	—	Reserved
10	DCDEN_STA	[Host role in DRD mode] This field is not used. [Peripheral role in DRD mode] The field to be able to store information of whether the USB peripheral executes the Data Contact Detect (DCD) or not. 1b: The system executes DCD. 0b: The system does not execute DCD.
9, 8	BCRSLT_STA	[Host role in DRD mode] This field is not used. [Peripheral role in DRD mode] The field to be able to store the Good Battery Algorithm SDP/DCP/CDP detection result. 00b: SDP 01b: CDP 10b: DCP 11b: DCP/CDP If this field is not needed, this initial value should be kept and BC_INT_ENA.BCRSLT_CHG_ENA should be set to ‘0’.
7 to 2	—	Reserved

Table 35.4-13 USB_PERI_BC_STA Register Contents (2/2)

Bit Position	Bit Name	Description
1	PRTBLDCPDET_STA	[Host role in DRD mode] This bit is not used. [Peripheral role in DRD mode] The bit to indicate the detection signal's status for the Secondary handshake in Battery Charging specification.
0	CHGDET_STA	[Host role in DRD mode] This bit is not used. [Peripheral role in DRD mode] The bit to indicate the detection signal's status for the Primary handshake in Battery Charging specification.

(2) Battery Charging Interrupt Status Register (USB_PERI_BC_INT_STA)

This register shows the Battery Charging interrupt status. These bits are cleared by writing 1.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0424h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	DCDEN_CHG_STA	—	BCRSLT_CHG_STA	—	—	—	—	—	—	PRTBLDCPDET_CHG_STA	CHGDET_CHG_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW1	R	RW1	R	R	R	R	R	R	RW1	RW1

Table 35.4-14 USB_PERI_BC_INT_STA Register Contents

Bit Position	Bit Name	Description
31 to 11	—	Reserved
10	DCDEN_CHG_STA	The bit to indicate the status-change of BC_STA.DCDEN_STA. 1b: The status is changed. 0b: The status is not changed.
9	—	Reserved
8	BCRSLT_CHG_STA	The bit to indicate the status-change of BC_STA.BCRSLT_STA. 1b: The status is changed. 0b: The status is not changed.
7 to 2	—	Reserved
1	PRTBLDCPDET_CHG_STA	The bit to indicate the status-change of BC_STA.PRTBLDCPDET_STA. 1b: The status is changed. 0b: The status is not changed.
0	CHGDET_CHG_STA	The bit to indicate the status-change of BC_STA.CHGDET_STA. 1b: The status is changed. 0b: The status is not changed.

(3) Battery Charging Interrupt Enable Register (USB_PERI_BC_INT_ENA)

This register is used to enable the Battery Charging interrupt status.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0428h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	DCDEN_CHG_ENA	—	BCRSLT_CHG_ENA	—	—	—	—	—	—	PRTBLDCPDET_CHG_ENA	CHGDET_CHG_ENA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	R	RW	R	R	R	R	R	R	RW	RW

Table 35.4-15 USB_PERI_BC_INT_ENA Register Contents

Bit Position	Bit Name	Description
31 to 11	—	Reserved
10	DCDEN_CHG_ENA	This bit selects whether the interrupt state of BC_INT_STA.DCDEN_CHG_STA is joined ‘bc_int’ interrupt output or not. 1b: The interrupt state is joined ‘bc_int’. 0b: The interrupt state is not joined ‘bc_int’.
9	—	Reserved
8	BCRSLT_CHG_ENA	This bit selects whether the interrupt state of BC_INT_STA.BCRSLT_CHG_STA is joined ‘bc_int’ interrupt output or not. 1b: The interrupt state is joined ‘bc_int. 0b: The interrupt state is not joined ‘bc_int’.
7 to 2	—	Reserved
1	PRTBLDCPDET_CHG_ENA	This bit selects whether the interrupt state of BC_INT_STA.PRTBLDCPDET_CHG_STA is joined ‘bc_int’ interrupt output or not. 1b: The interrupt state is joined ‘bc_int’. 0b: The interrupt state is not joined ‘bc_int’.
0	CHGDET_CHG_ENA	This bit selects whether the interrupt state of BC_INT_STA.CHGDET_CHG_STA is joined ‘bc_int’ interrupt output or not. 1b: The interrupt state is joined ‘bc_int’. 0b: The interrupt state is not joined ‘bc_int’.

35.4.5.3 Global Purpose Registers

(1) Global Purpose Output Control Register (USB_PERI_GPO_CON)

This register controls the global-purpose output. This output is used for debugging only.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0430h

Initial Value: 0000_0000h

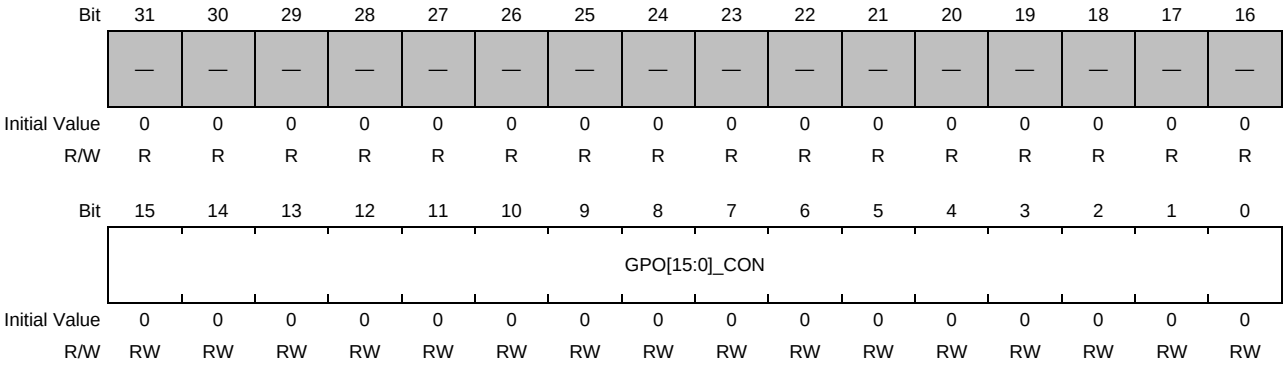


Table 35.4-16 USB_PERI_GPO_CON Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved
15 to 0	GPO[15:0]_CON	The bit to control the output value of ‘gpo[i]’. (i = 15 to 0) 1b: ‘gpo[i]’ is output ‘1’. 0b: ‘gpo[i]’ is output ‘0’.

(2) Global Purpose Input Status Register (USB_PERI_GPI_STA)

This register indicates the status of global-purpose input.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0434h

Initial Value: 0000_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GPO[15:0]_STA															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.4-17 USB_PERI_GPI_STA Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved
15 to 0	GPO[15:0]_STA	This bit to indicate the status of ‘gpi[i]’. (i = 15 to 0) *Note*: The initial value reflects the initial value of ‘gpi[i]’.

(3) Global Purpose Input Interrupt Status Register (USB_PERI_GPI_INT_STA)

This register indicates the status-change of global-purpose input. These bits are cleared by writing 1.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0438h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GPO[15:0]_CHG_STA															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1

Table 35.4-18 USB_PERI_GPI_INT_STA Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved
15 to 0	GPO[15:0]_CHG_STA	These bits indicate the status-change of GPI_STA.GPIi_STA. (i = 15 to 0) 1b: The status is changed. 0b: The status is not changed.

(4) Global Purpose Input Interrupt Enable Register (USB_PERI_GPI_INT_ENA)

This register selects whether the status-change interrupt of global-purpose input is joined ‘gpi_int’ interrupt output or not.

Access Size: 32 bits

Address(es): <USB_S1_base> + 043Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GPO[15:0]_CHG_ENA															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.4-19 USB_PERI_GPI_INT_ENA Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved
15 to 0	GPO[15:0]_CHG_ENA	This bit selects whether the interrupt state of GPI_INT_STA.GPIi_CHG_STA is joined ‘gpi_int’ interrupt output or not. (i = 15 to 0) 1b: The interrupt state is joined ‘gpi_int’. 0b: The interrupt state is not joined ‘gpi_int’.

35.4.6 Description of Functions

The USB3DRD supports the following DRD-specific functions.

The prefix (USB_PERI_) of the register names is omitted in this and subsequent sections.

35.4.6.1 DRD Mode

The USB3DRD supports the “DRD mode” in which role swapping function is enable by the ID pin “drd_id”.

The default role is the peripheral role in this mode. ID pin “drd_id” is needed to be set to the “Pull Up”’s situation. The role swapping event is occurred by the status change of the ID pin “drd_id”.

The role's selection is decided by USB3.1 Micro-AB receptacle. This receptacle can be connected by using the USB3.1 cable with USB3.1 Micro-A plug and USB3.1 Micro-B plug. This USB cable decides either "A-device" or "B-device" by connected USB plug. The “A-device” shall supply VBUS to USB bus and the “B-device” shall not supply VBUS to USB bus.

Therefore, the "A-device" is fixed as the "A-Host" and the "B-device" is fixed as the "B-Peripheral".

The ID pin’s status can be monitored by the register-bit “DRD_STA.ID_STA”, and this ID pin’s changed status can be monitored by the register-bit “DRD_INT_STA.ID_CHG_STA”. When the interrupt enable register-bit “DRD_INT_ENA.ID_CHG_ENA is set to “1b”, the event of this ID pin’s status change can be transmitted to the USB-SW’s system as the interrupted notification by the interrupt signal.

Both of the Host role’s SW driver “xHCI” driver and the Peripheral role’s SW driver are needed to be treated as the module.

Because, when the role-swapping is occurred, a driver for the active role shall be loaded and a driver for the inactive role shall be unloaded.

(1) Power On

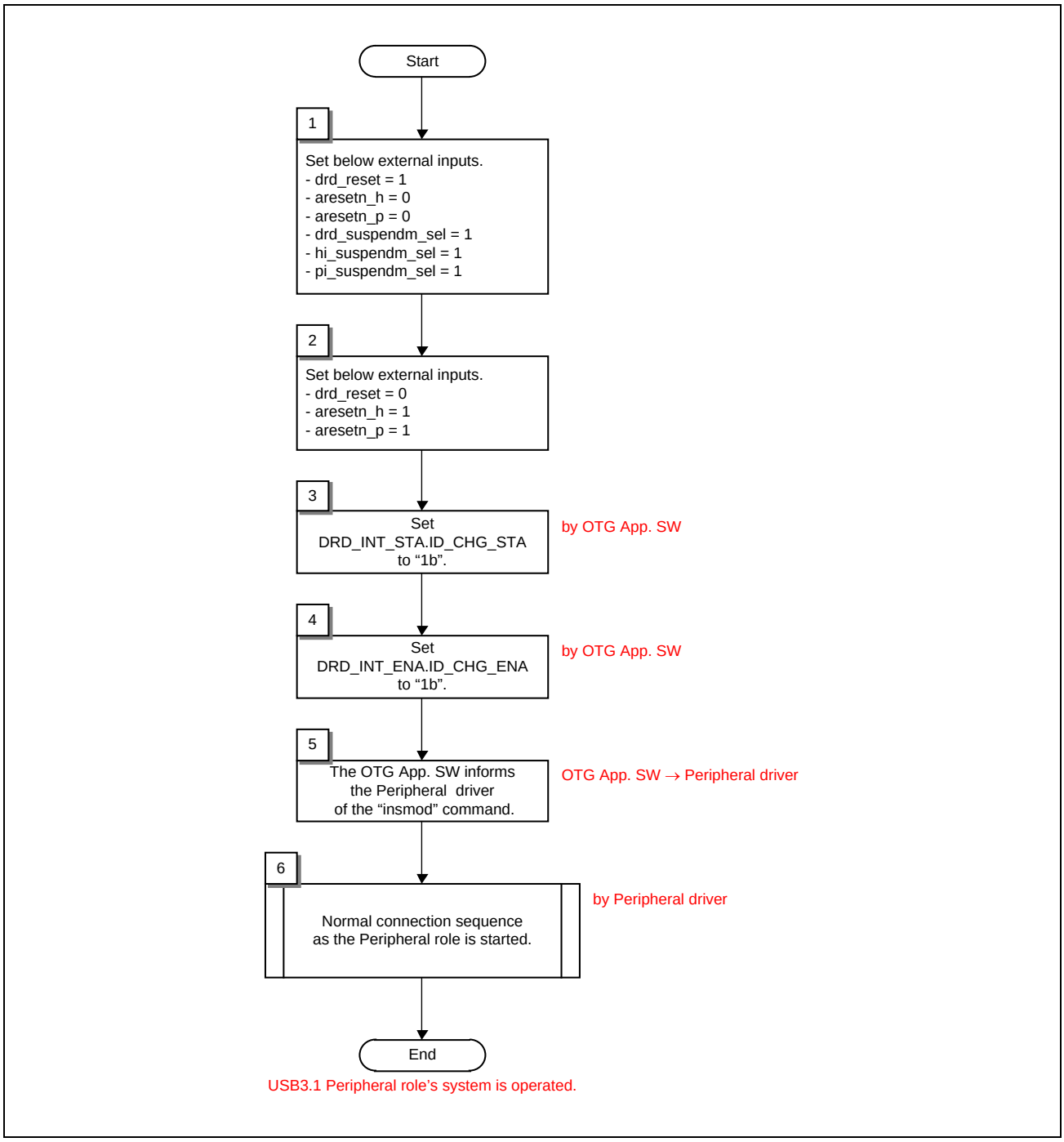


Figure 35.4-3 Power-On Flowchart in DRD Mode

1. Set below external reset-inputs to the value to assert these reset-lines.
   – drd_reset = 1
   – aresetn_h = 0
   – aresetn_p = 0
   Set below external inputs to “1” to activate these “SuspendM” lines.
   – drd_suspendm_sel
   – hi_suspendm_sel
   – pi_suspendm_sel
2. Set below external inputs to the value to deassert these reset-lines.
   – drd_reset = 0
   – aresetn_h = 1
   – aresetn_p = 1
3. The OTG Application SW sets the below bit of the DRD_INT_STA register to “1b”.
   – ID_CHG_STA
4. The OTG Application SW sets the below bit of the DRD_INT_ENA register to “1b”.
   – ID_CHG_ENA
5. The OTG Application SW informs the Peripheral driver of the “insmod” command to enable a driver.
6. The Peripheral driver starts the normal connection-sequence as the peripheral role.

(2) Role Swapping Function by ID Pin

The ID pin “drd_id” : “1 (Peripheral role) → 0 (Host role)” or “0 (Host role) → 1 (Peripheral role)”

The USB3DRD supports the below only for the role swapping usage.

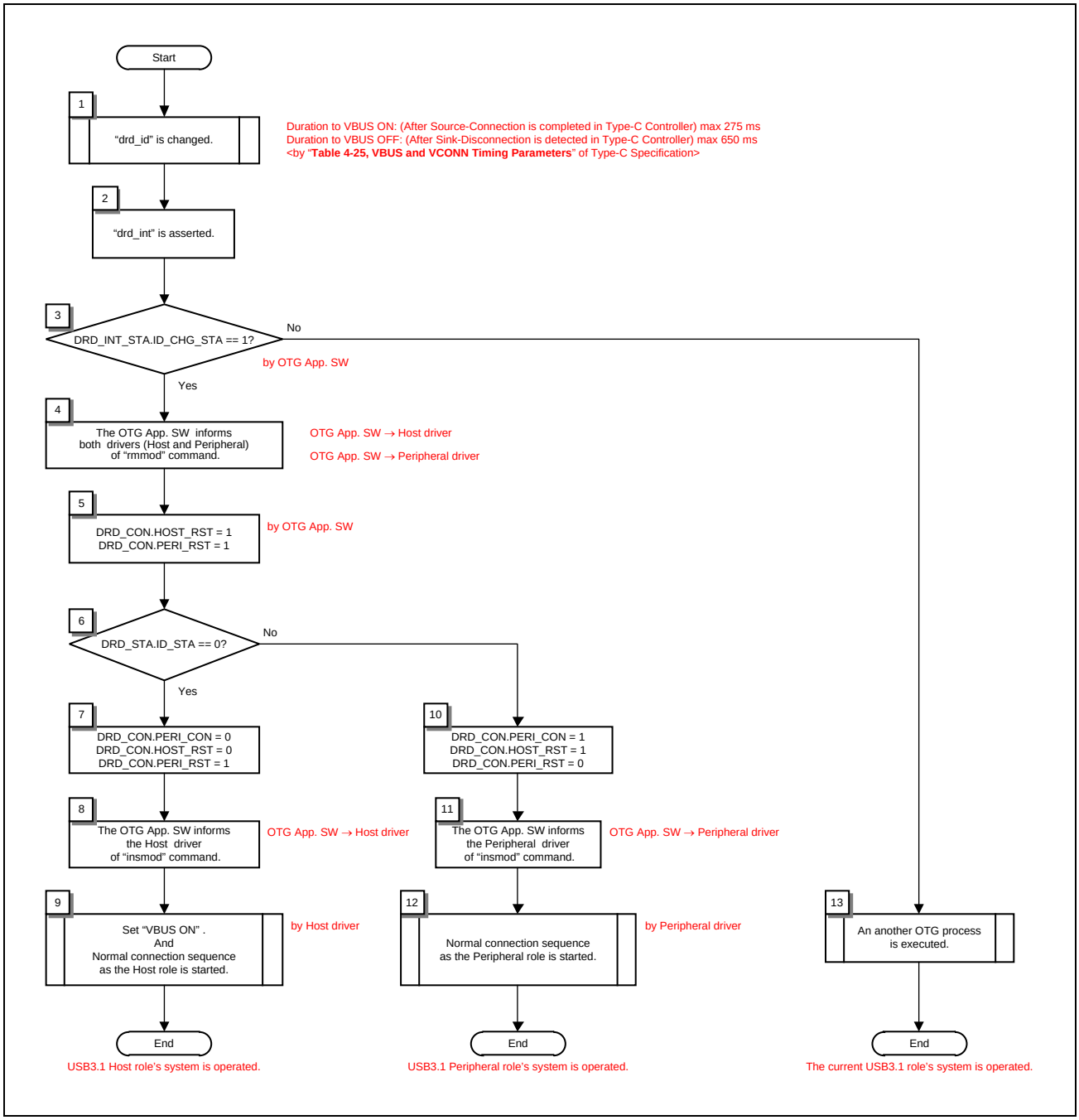


Figure 35.4-4 Role Swapping Flowchart in DRD Mode

1. “drd_id” is changed.
2. “drd_int” is asserted.
3. The OTG Application SW reads the below bit of the DRD_INT_STA register.
   If the ID_CHG_STA is read “1”, go to “Step 4”.
   If the ID_CHG_STA is read “0”, go to “Step 13”.
4. The OTG Application SW informs both drivers (Host and Peripheral) of the “rmmod” command to disable a driver.
5. The OTG Application SW sets below reset-bits of the DRD_CON register to “1”.
   – HOST_RST
   – PERI_RST
6. The OTG Application SW reads the below bit of DRD_STA register.
   If the ID_STA is read “0”, go to “Step 7”.
   If the ID_STA is read “1”, go to “Step 10”.
7. The OTG Application SW sets below bits as follows.
   – PERI_CON : 0
   – HOST_RST : 0
   – PERI_RST : 1
8. The OTG Application SW informs the Host driver of the “insmod” command to enable a driver.
9. The Host driver starts the normal connection-sequence including “VBUS ON” as the host role.
10. The OTG Application SW sets below bits as follows.
    – PERI_CON : 1
    – HOST_RST : 1
    – PERI_RST : 0
11. The OTG Application SW informs the Peripheral driver of the “insmod” command to enable a driver.
12. The Peripheral driver starts the normal connection-sequence as the peripheral role.
13. The OTG Application SW executes an another OTG process.

NOTE

The Type-C specification defines the following specifications.

Therefore, if Type-C receptacle is used as the USB receptacle, the duration between above sequence “Step 1” and “Step 9” shall be completed until 275 ms.

[“Table 4-29 VBUS and VCONN Timing Parameters” in USB Type-C Spec R2.0 - August 2019 specification]

Duration to VBUS ON	: (After Source-Connection is completed in Type-C controller)	Max. 275 ms
Duration to VBUS OFF	: (After Sink-Disconnection is detected in Type-C controller)	Max. 650 ms

35.4.6.2 Battery Charging Function

The USB3DRD supports the Battery Charging function of both the Charging Port device (A-device) and the Portable device (B-device).

(1) Charging Port Device (A-Device)

The USB3DRD supports the Charging Port's functions which are defined in the Battery Charging Specification Revision 1.2.

The Battery Charging function supplies more current from VBUS than the current specified in the USB specification.

The USB3DRD's A-device supports the following modes.

- Standard Downstream Port (SDP)
- Charging Downstream Port (CDP)
- Dedicated Charging Port (DCP)

These functions are controlled by the Host role's registers in the Host Controller-portion.

When the user uses the battery charging function, the user can select one of BC modes by setting BC_MODE_P1 field of Battery Charging Control Register (BCCTRL) in the Host Controller-portion.

(2) Portable Device (B-Device)

The USB3DRD supports the Portable device's functions which are defined in the Battery Charging Specification Revision 1.2.

The USB3DRD supports the following modes of portable device.

- Standard Downstream Port (SDP) Mode
- Charging Downstream Port (CDP) Mode
- Dedicated Charging Port (DCP) Mode

The USB3DRD also supports the following function of portable device.

- Data Contact Detect (DCD)

When the B-device connects to the A-device, it is allowed to draw current from A-device and start charging until the process of device connection is valid with Dead Battery Provision which is defined in the Battery Charging Specification Revision 1.2.

Then the B-device can detect the settable A-device's Battery Charging Mode that is compliant with Good Battery Algorithm in the Battery Charging Specification Revision 1.2.

These functions are controlled by DRD registers in the USB3DRD.

Therefore, it describes how to implement these functions in this sub-sections.

(a) Pre Sequence

Before starting the Battery Charging functions in B-device, the user shall access and confirm the following bits. Otherwise the Battery Charging functions are terminated.

- DRD_CON.PERI_CON = 1

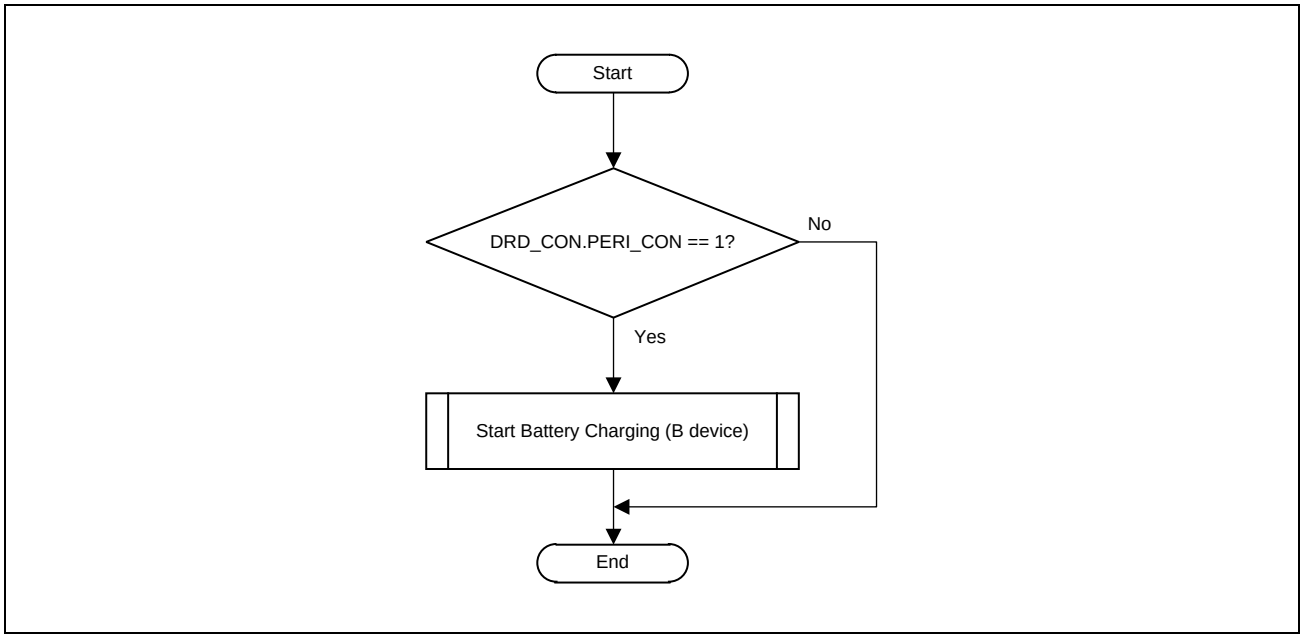


Figure 35.4-5 Prior Confirmation Flow for the Battery Charging of B-Device

(b) Weak Battery Algorithm

As the viewpoint of the battery condition, if the USB peripheral system is not able to execute the USB initialization to connect as the USB device, that USB system is able to operate the Weak Battery Algorithm.

This section describes how to operate the Weak Battery Algorithm in the USB3DRD.

The Weak Battery Algorithm is operated after a detection of “USB-VBUS ON” by the Peripheral driver.

It presupposes that the USB-VBUS is already ON when this flow starts.

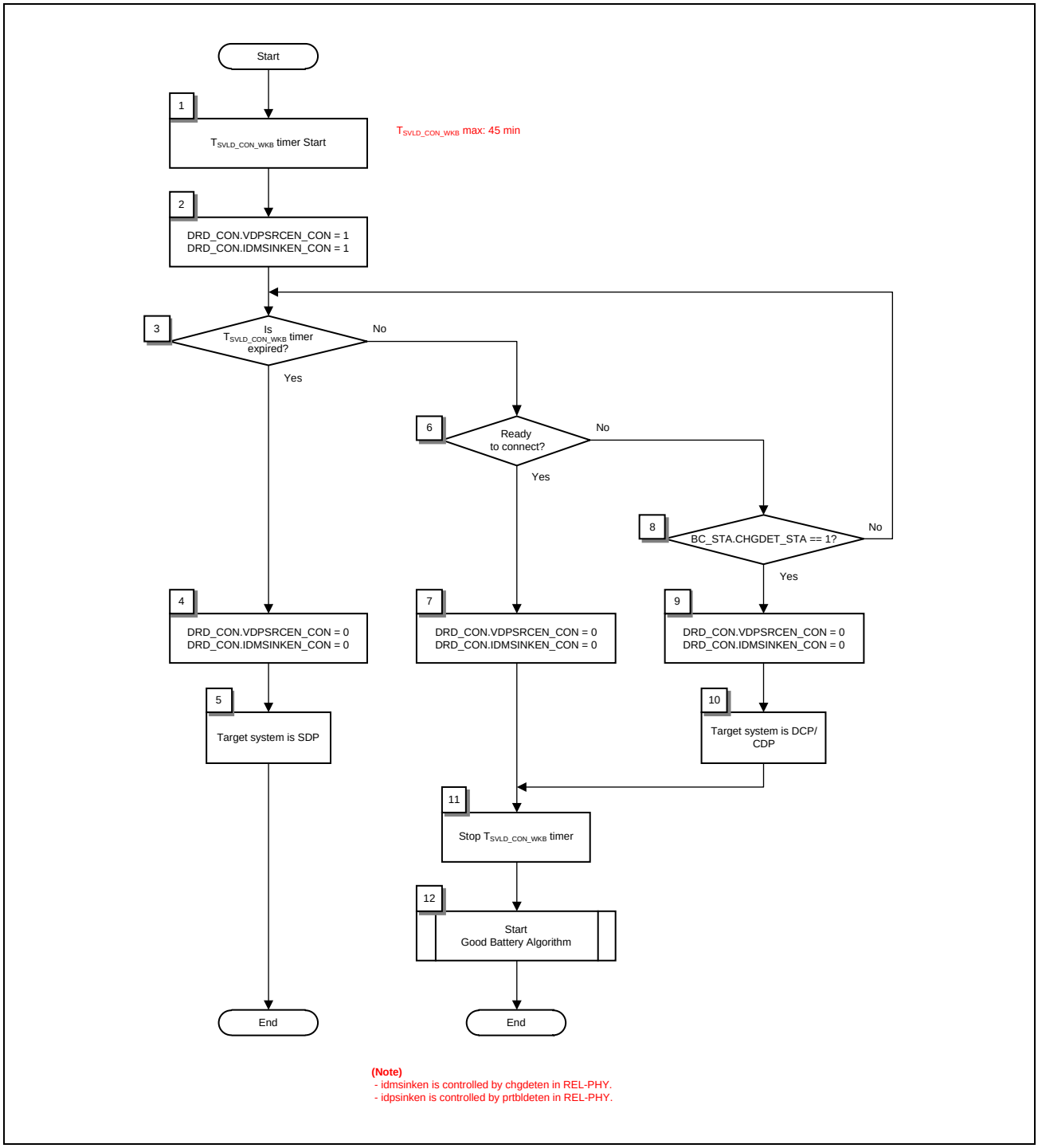


Figure 35.4-6 Weak Battery Algorithm Flowchart

1. Start the $T_{SVLD\_CON\_WKB}$ timer.
   – $T_{SVLD\_CON\_WKB}$: max. 45 min
2. Set below bits of the DRD_CON register to “1”
   – VDPSRCEN_CON
   – IDMSINKEN_CON
   → The drawable current-level of the USB peripheral system is able to be I_{UNIT} (100 mA at USB2.0 port / 150 mA
   at USB3.1 port).
3. If the $T_{SVLD\_CON\_WKB}$ timer has been expired, go to “Step 4”.
   If the $T_{SVLD\_CON\_WKB}$ timer has not been expired yet, go to “Step 6”.
4. Set below bits of the DRD_CON register to “0”.
   – VDPSRCEN_CON
   – IDMSINKEN_CON
5. The Peripheral driver judges that the target system is SDP.
   And the drawable current-level of the USB peripheral system shall be I_{SUSP} (2.5 mA).
   Because, this current-level is the current-level in the case of the “Dead Battery Provision”.
   And the Peripheral driver may set BC_STA.BCRSLT_STA to “00b”.
6. If the USB peripheral system has already completed a preparation of “Pull Up” for the USB connection, go to “Step 7”.
   If the USB peripheral system has not completed a preparation of “Pull Up” for the USB connection yet, go to “Step 8”.
7. Set below bits of the DRD_CON register to “0”.
   – VDPSRCEN_CON
   – IDMSINKEN_CON
8. The Peripheral driver reads the below bit of the BC_STA register.
   If the CHGDET_STA is read “1”, go to “Step 9”.
   If the CHGDET_STA is read “0”, go to “Step 3”.
9. Set below bits of the DRD_CON register to “0”.
   – VDPSRCEN_CON
   – IDMSINKEN_CON
10. The Peripheral driver judges that the target system is DCP / CDP.
    And the drawable current-level of the USB peripheral system is able to be I_{DEV_CHG} (Max.: 1.5 A).
    And the Peripheral driver may set BC_STA.BCRSLT_STA to “00b”.
11. Stop the $T_{SVLD\_CON\_WKB}$ timer.
12. Start the Good Battery Algorithm.

(c) Good Battery Algorithm

This section describes how to operate the Good Battery Algorithm.

The Good Battery Algorithm is operated after completion of the Weak Battery Algorithm or after a detection of USB-VBUS ON by the Peripheral driver. It presupposes that that USB-VBUS is already ON when this flow starts. And it also presupposes that BC_STA.DCDEN_STA has already been set to the DCD capability's value of the USB peripheral system.

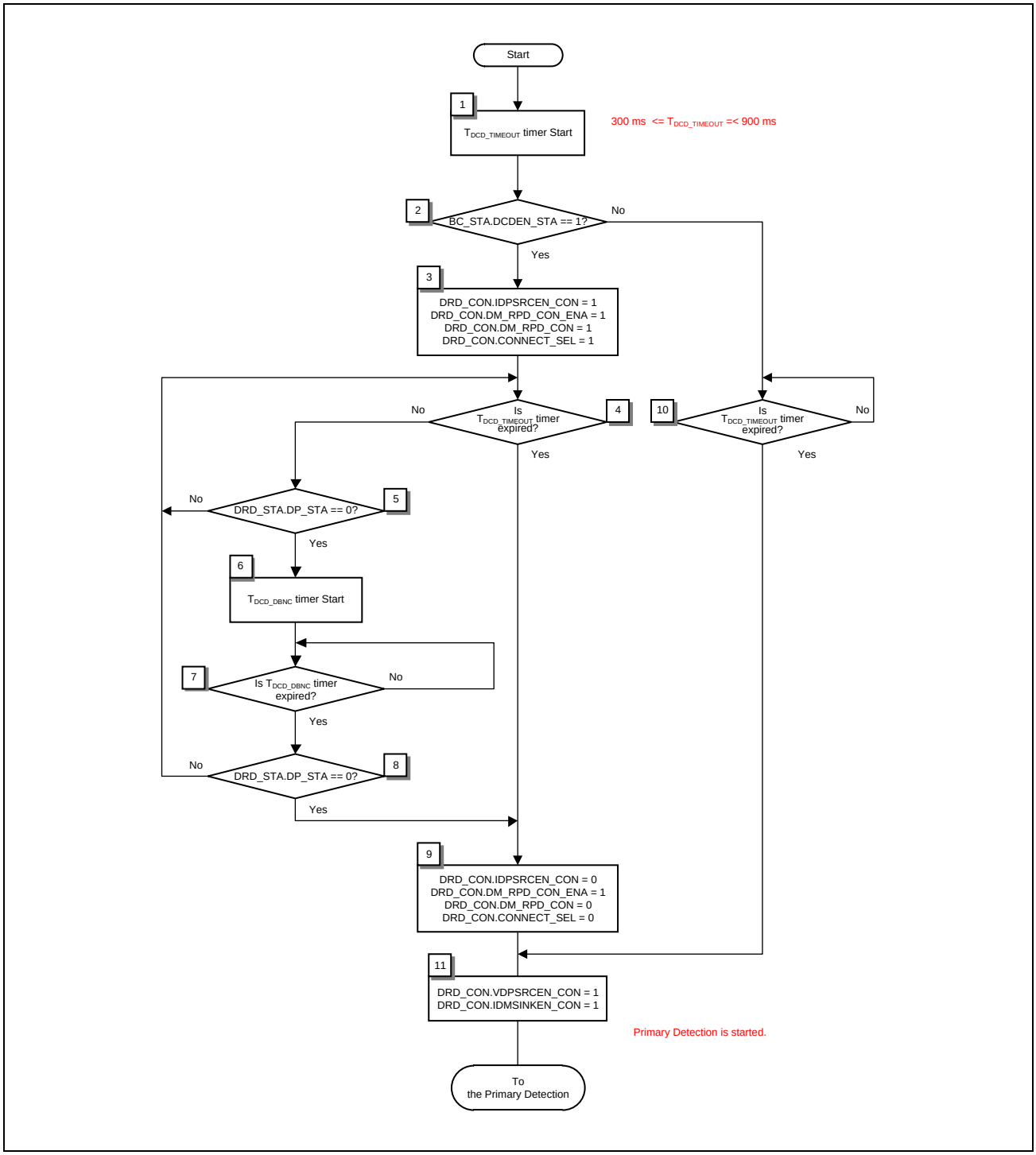


Figure 35.4-7 Good Battery Algorithm Flowchart (DCD Flow)

1. Start the $T_{DCD\_TIMEOUT}$ timer.
   – $T_{DCD\_TIMEOUT}$: min. 300 ms max. 900 ms
2. The Peripheral driver reads the below bit of the BC_STA register.
   If the DCDEN_STA is read “1”, go to “Step 3”.
   If the DCDEN_STA is read “0”, go to “Step 10”.
3. Set below bits of the DRD_CON register to “1”.
   – IDPSRCEN_CON
   – DM_RPD_CON_ENA
   – DM_RPD_CON
   – CONNECT_SEL
4. If the $T_{DCD\_TIMEOUT}$ timer has been expired, go to “Step 9”.
   If the $T_{DCD\_TIMEOUT}$ timer has not been expired yet, go to “Step 5”.
5. The Peripheral driver reads the below bit of the DRD_STA register.
   If the DP_STA is read “0”, go to “Step 6”.
   If the DP_STA is read “1”, go to “Step 4”.
6. Start the T_{DCD_DBNC} timer.
   – T_{DCD_DBNC} : min. 10 ms
7. If the T_{DCD_DBNC} timer has been expired, go to “Step 8”.
   If the T_{DCD_DBNC} timer has not been expired yet, stay in “Step 7” until the T_{DCD_DBNC} timer is expired.
8. The Peripheral driver reads the below bit of the DRD_STA register.
   If the DP_STA is read “0”, go to “Step 9”.
   If the DP_STA is read “1”, go to “Step 4”.
9. Set below bits of the DRD_CON register as follows.
   – IDPSRCEN_CON : 0
   – DM_RPD_CON_ENA : 1
   – DM_RPD_CON : 0
   – CONNECT_SEL : 0
10. If the $T_{DCD\_TIMEOUT}$ timer has been expired, go to “Step 11”.
    If the $T_{DCD\_TIMEOUT}$ timer has not been expired yet, stay in “Step 7” until the DCD timer is expired.
11. Set below bits of the DRD_CON register to “1”.
    – VDPSRCEN_CON
    – IDMSINKEN_CON

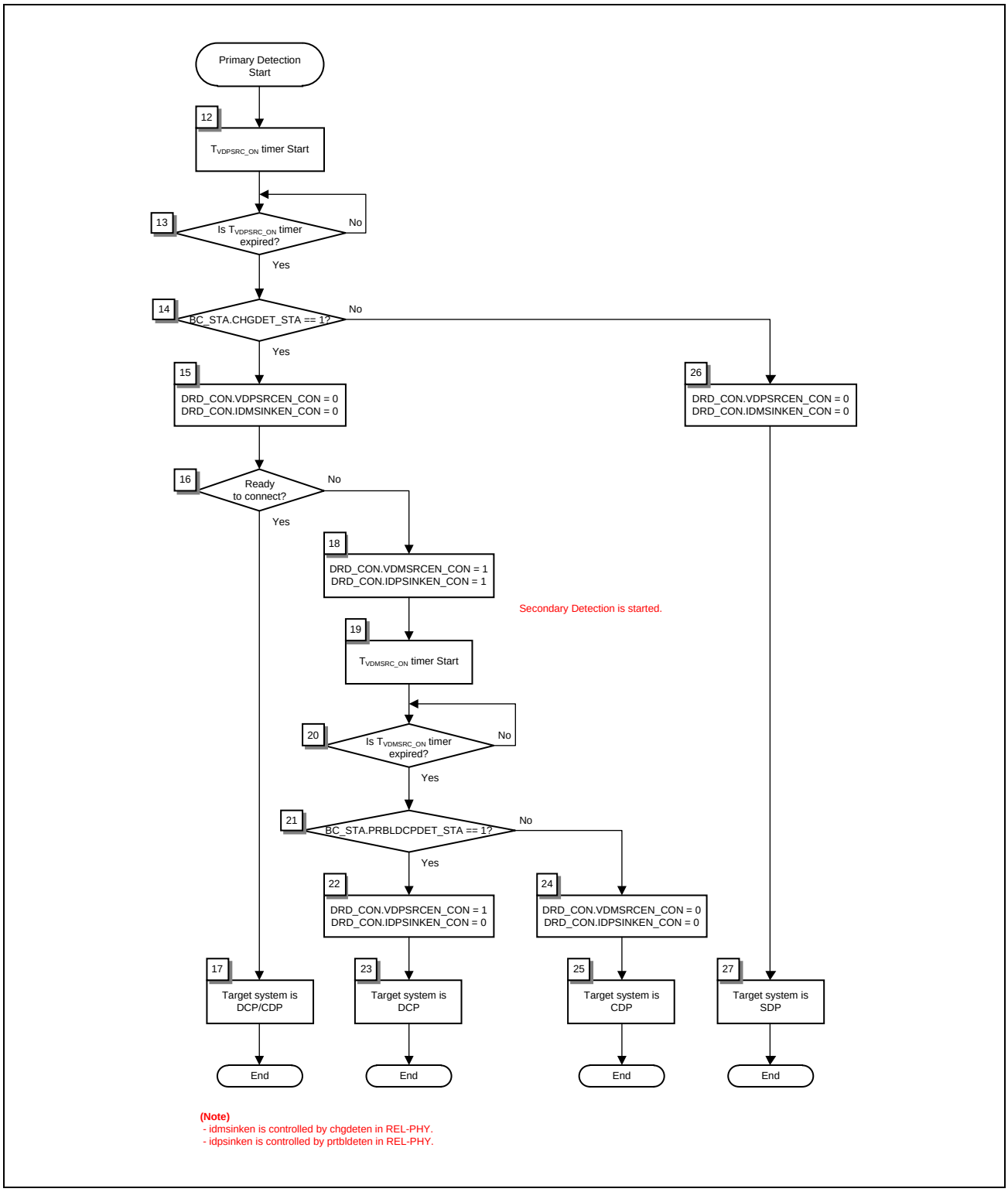


Figure 35.4-8 Good Battery Algorithm Flowchart (Primary & Secondary Detection Flow)

12. Start the T_{VDPSRC_ON} timer.
    – T_{VDPSRC_ON} : Min. 40 ms
13. If the T_{VDPSRC_ON} timer has been expired, go to “Step 14”.
    If the T_{VDPSRC_ON} timer has not been expired yet, stay in “Step 13” until the T_{VDPSRC_ON} timer is expired.

14. The Peripheral driver reads the below bit of the BC_STA register.
    If the CHGDET_STA is read “1”, go to “Step 15”.
    If the CHGDET_STA is read “0”, go to “Step 26”.
15. Set below bits of the DRD_CON register to “0”.
    – VDPSRCEN_CON
    – IDMSINKEN_CON
16. If the USB peripheral system has already completed a preparation of “Pull Up” for the USB connection, go to “Step 17”.
    If the USB peripheral system has not completed a preparation of “Pull Up” for the USB connection yet, go to “Step 18”.
17. The Peripheral driver judges that the target system is DCP or CDP.
    And the drawable current-level of the USB peripheral system is able to set to I_{DEV_CHG} (Max.: 1.5 A).
    And the Peripheral driver may set BC_STA.BCRSLT_STA to “11b”.
18. Set below bits of the DRD_CON register to “1”.
    – VDMSRCEN_CON
    – IDPSINKEN_CON
19. Start the T_{VDMSRC_ON} timer.
    – T_{VDMSRC_ON} : min. 40 ms
20. If the T_{VDMSRC_ON} timer has been expired, go to “Step 21”.
    If the T_{VDMSRC_ON} timer has not been expired yet, stay in “Step 20” until the T_{VDMSRC_ON} timer is expired.
21. The Peripheral driver reads the below bit of the BC_STA register.
    If the PRTBLDCPDET_STA is read “1”, go to “Step 22”.
    If the PRTBLDCPDET_STA is read “0”, go to “Step 24”.
22. Set below bits of the DRD_CON register as follows.
    – VDPSRCEN_CON : 1
    – IDPSINKEN_CON : 0
23. The Peripheral driver judges that the target system is DCP.
    And the drawable current-level of the USB peripheral system is able to set to IDEV_CHG (Max.: 1.5 A).
    And the Peripheral driver may set BC_STA.BCRSLT_STA to “10b”.
24. Set below bits of the DRD_CON register as follows.
    – VDMSRCEN_CON : 0
    – IDPSINKEN_CON : 0
25. The Peripheral driver judges that the target system is CDP.
    And the drawable current-level of the USB peripheral system is able to set to IDEV_CHG (Max.: 1.5 A).
    And the Peripheral driver may set BC_STA.BCRSLT_STA to “01b”.
26. Set below bits of the DRD_CON register to “0”.
    – VDPSRCEN_CON
    – IDMSINKEN_CON
27. The Peripheral driver judges that the target system is SDP.
    And the Peripheral driver may set BC_STA.BCRSLT_STA to “00b”.

(d) Post Sequence

When the Peripheral driver detects the USB-VBUS OFF such as a device disconnection, a subsequent process is operated to prevent from the false-operation in Battery Charging function.

This is operated after a detection of the USB-VBUS OFF by the Peripheral driver, so it presupposes that USB-VBUS has already been set to OFF when this flow starts.

If this operation is called during the Weak or Good Battery Algorithm, it shall put a highest priority on these clearing bits of the DRD_CON register. Moreover, that interrupted processing is not restarted, and the processing for the Battery Charging function is terminated.

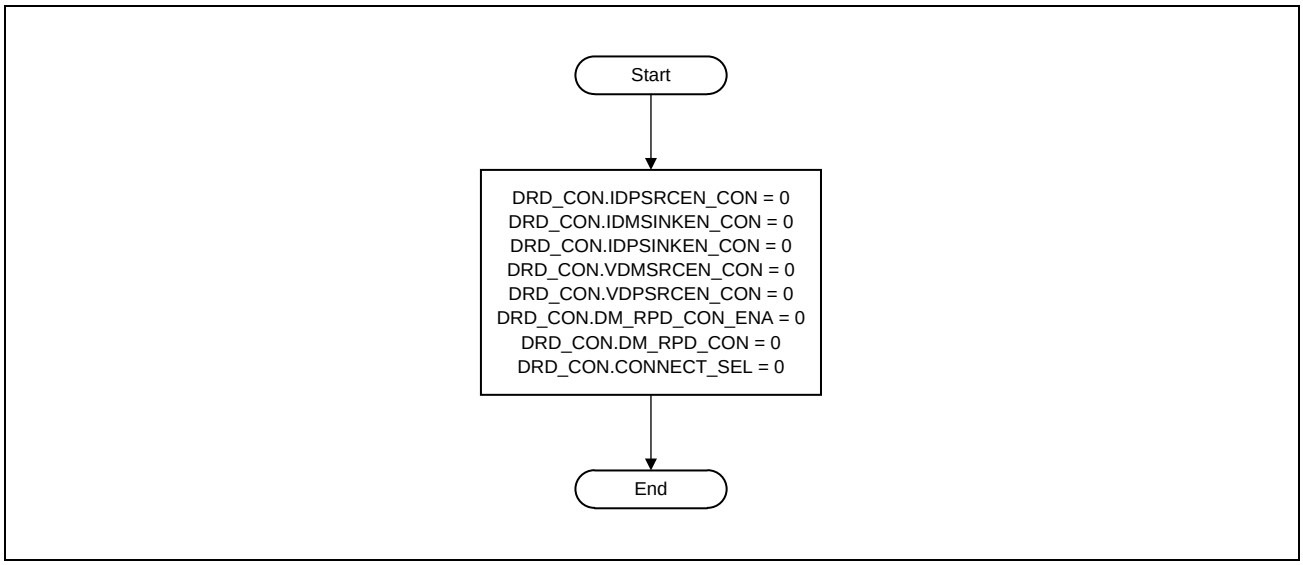


Figure 35.4-9 Register-Bits' Clear for the Battery Charging Function

35.4.6.3 Over Current Checking Flow

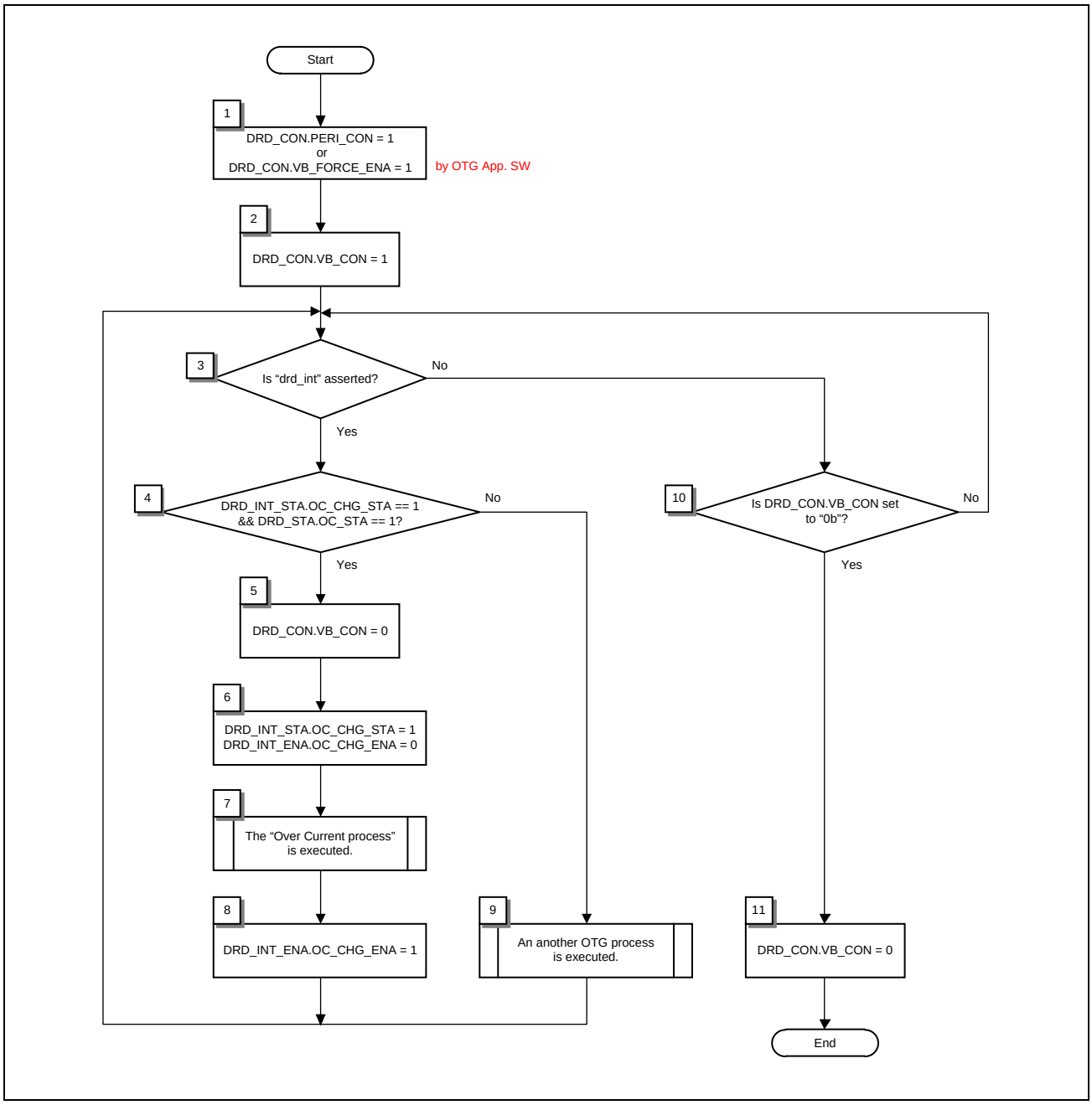


Figure 35.4-10 Over-Current Checking Flowchart

1. The OTG Application SW sets either DRD_CON.PERI_CON or DRD_CON.VB_FORCE_ENA to “1”.
2. The OTG Application SW sets the below bit of the DRD_CON register to “1”.
   – VB_CON
3. If the OTG Application SW reports that interrupt-event, go to “Step 4”.
   If the OTG Application SW reports that interrupt-event, go to “Step 10”.
4. The OTG Application SW reads DRD_INT_STA.OC_CHG_STA and DRD_STA.OC_STA.
   If both of these two bits are set to “1”, go to “Step 5”.
   If an either bit is set to “0”, go to “Step 9”.
5. The OTG Application SW sets the below bit of the DRD_CON register to “0”.
   – VB_CON
6. The OTG Application SW sets below register-bits as follows.
   – DRD_INT_STA.OC_CHG_STA : 1
   – DRD_INT_ENA.OC_CHG_ENA : 0
7. The OTG Application SW executes the “Over Current process”.
8. The OTG Application SW sets the below bit of the DRD_INT_ENA register to “1”.
   – DRD_INT_ENA.OC_CHG_ENA
9. The OTG Application SW executes an another OTG process.
10. The OTG Application SW considers how to set DRD_CON.VB_CON.
    If it is OK that VB_CON is set to “0”, go to “Step 11”.
    If the VB_CON is kept to be set to “1”, go to “Step 3”.
11. The OTG Application SW sets the below bit of the DRD_CON register to “0”.
    – VB_CON

35.4.6.4 Control of SuspendM Signal

SuspendM is the UTMI+ interface signal. This signal controls the current-situation of USB2.0 PHY. And this signal also controls the output of UTMI clock signal.

If SuspendM is set to the high level, UTMI clock signal is supplied by USB2.0 PHY.

If SuspendM is set to the low level, UTMI clock signal is stopped to be supplied by USB2.0 PHY.

The SuspendM signal is a OR of following three signals. That is, actual SuspendM signal will be asserted to low only when all of following three signals are asserted.

- SuspendM signal from Host Controller.

- SuspendM signal from Peripheral Controller.

- SuspendM signal from DRD Controller. (Value specified to DRD_CON.U2_SUSPEND_CON)

SuspendM outputs “0b” during asserting reset.

35.5 USB3.1 Gen1 Host Controller (USB3HOST)

35.5.1 Introduction

The USB3.1 Gen1 Host Controller (USB3HOST) complies with the Universal Serial Bus (USB) 3.1 Specification.

35.5.1.1 Features

The functions of the USB3HOST are outlined below.

(1) USB Functions

The USB3HOST is compliant with *the Universal Serial Bus 3.1 Specification Revision 1.0 and ECNs* approved in June 27, 2017.

- Supports 1 downstream USB receptacles
  - Number of SS ports: 1
  - Number of HS or FS or LS ports: 1
- Supports all USB3.1 Gen1 bus-speeds: Super Speed (5 Gbps), High Speed (480 Mbps), Full Speed (12 Mbps), and Low Speed (1.5 Mbps).
- Supports all transfer-types : Control, Bulk, Interrupt, Isochronous, and these split-transactions.
- Supports Power Control and Over Current Detection.
- Implements the following USB2.0 ECNs USB 2.0 Link Power Management Addendum and LPM functions that are compliant with the xHCI specification.
  - *USB 2.0 Link Power Management Addendum Engineering Change Notice* to the USB 2.0 specification as of July 16, 2007
  - Errata for USB 2.0 ECN: Link Power Management (LPM) - 7/2007 as of October 11, 2011

(2) Battery Charging Functions

The USB3HOST supports the following functions that are compliant with *the Battery Charging Specification Revision 1.2*.

- The USB3HOST supports the following modes of chargeable port devices.
  - Standard Downstream Port (SDP) Mode
  - Charging Downstream Port (CDP) Mode
  - Dedicated Charging Port (DCP) Mode

(3) xHCI Capabilities

The USB3HOST has the following capabilities that are compliant with *the eXtensible Host Controller Interface for the Universal Serial Bus Specification Revision 1.1*.

- Supports 64-bit address capability
- xHCI Host Capability
  - Number of Device Slots (MaxSlots): 32
  - Number of Total Endpoints: 64
  - Number of Event Ring Segment Tables (ERST Max): 2(1)
  - Supported Page Size: 4 Kbytes
  - Context Size (CSZ): 64 bytes(1)
  - Number of Interrupter (MaxIntrs): 1
  - Number of Stream IDs (MaxPSASize): 65536(15)
  - Supports Primary Stream Array
  - Supports the USB Legacy Support.
  - Supports the Hardware LPM Capability.
  - Supports Best Effort Service Latency (BESL) LPM Capability.

(4) Clock Control

The USB3HOST has the following clock and PLL control functions.

- Clock gating: Enables/disables clock gating to applicable functional sub-blocks depending on the USB state.
- PLL control: Enables/disables PLLs for USB2.0 and USB3.1 depending on their USB states.

35.5.2 Interrupts

35.5.2.1 Interrupt Diagram

In the USB3HOST, the elements of interrupt are notified by the following layered structure.

INTSTS register is not implemented in any FFs.

This register is a read-only register (monitor register).

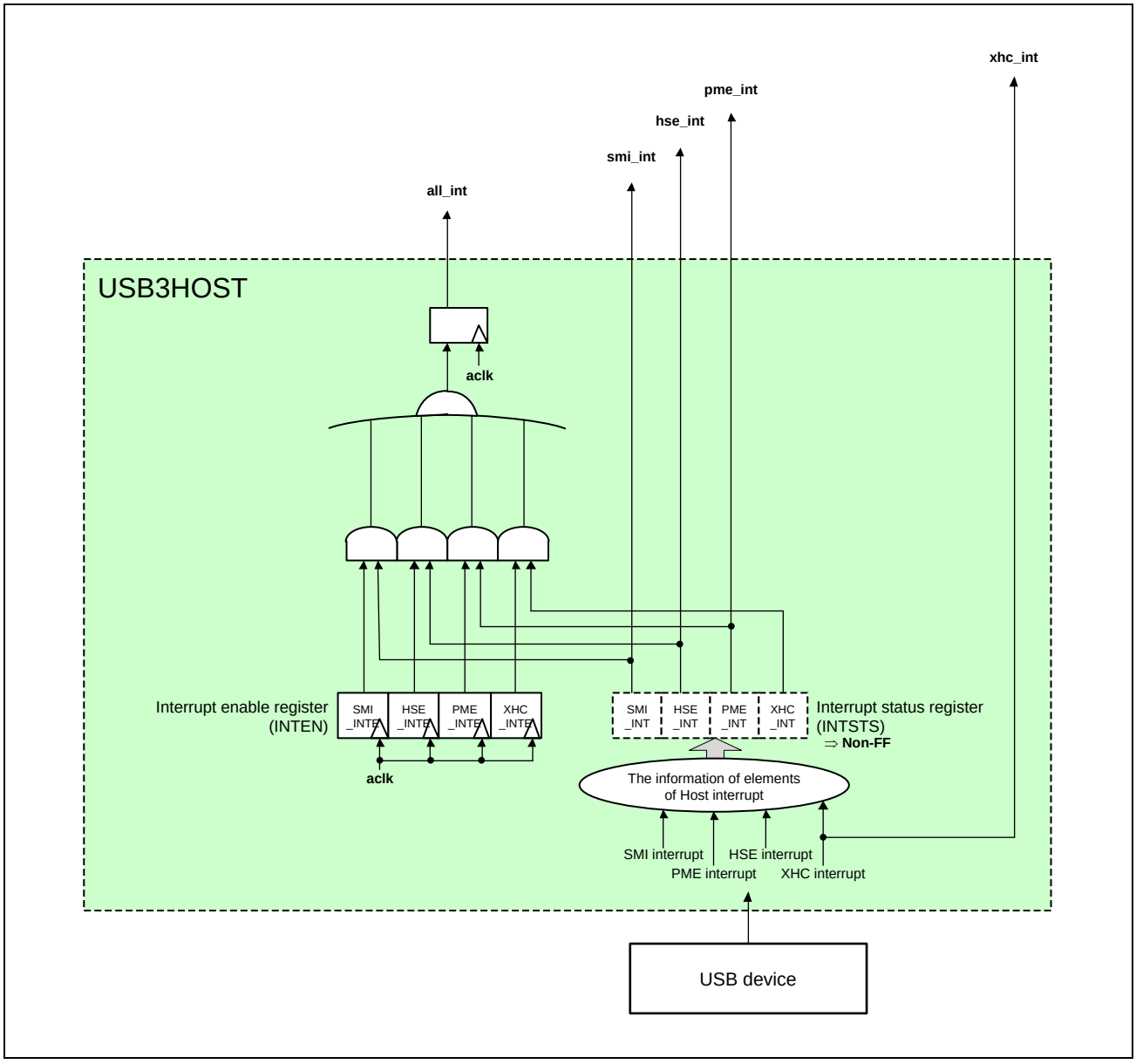


Figure 35.5-1 USB3HOST Interrupts Structure

35.5.2.2 Interrupt Sources

The USB3HOST has the following interrupt sources.

Table 35.5-1 USB3HOST Interrupt Source Information

Interrupt Name	Type of Notification	Description
xhc_int	Level Pulse	xHC interrupt This signal notifies that Event Data TRB is set in Event Ring of a system memory. In this LSI, “level mode” is selected for the interrupt. Refer to the section 4.17 of the xHCI specification for details.
pme_int	Level	Power management event interrupt. When PMCSR.PME Enable is set to 1b and PMCSR.PME Status is set to 1b, this signal is asserted. PMCSR.PME Status is set to 1b by one of the following conditions. • PORTSC.WCE = 1b, and Connected condition • PORTSC.WDE = 1b, and Disconnected condition • PORTSC.WOE = 1b, and Overcurrented condition • PORTSC.PLS = U3, and Remote Wakeup condition
hse_int	Level	Host system error interrupt When the USBCMD.HSEE is set to 1b and the USBSTS.HSE is set to 1b, this signal is asserted. The USBSTS.HSE is set to 1b by one of the following conditions. • Either SLVERR or DECERR is received as the Response in the transaction of AXI master write. • Either SLVERR or DECERR is received as the Response in the transaction of AXI master read.
smi_int	Level	System management interrupt This signal is asserted by one of the following conditions. • USBLEGCTLSTS.SEI = 1b and USBLEGCTLSTS.USE = 1b • USBLEGCTLSTS.SHSE = 1b and USBLEGCTLSTS.SHSEE = 1b • USBLEGCTLSTS.SOOC = 1b and USBLEGCTLSTS.SOOE = 1b • USBLEGCTLSTS.SPC = 1b and USBLEGCTLSTS.SPCE = 1b • USBLEGCTLSTS.SBA = 1b and USBLEGCTLSTS.SBAE = 1b
all_int	Level	Logical OR of all interrupt signals. This signal is asserted by one of the following conditions. • INTEN.XHC_INTE = 1b and INTSTS.XHC_INT = 1b • INTEN.PME_INTE = 1b and INTSTS.PME_INT = 1b • INTEN.HSE_INTE = 1b and INTSTS.HSE_INT = 1b • INTEN.SMI_INTE = 1b and INTSTS.SMI_INT = 1b

35.5.3 Register Specification

Registers in the USB3HOST are composed of the following register groups.

- xHCI compliant registers
  - Host Controller Capability Registers
  - Host Controller Operational Registers
  - Port Register Sets in Host Controller Registers
  - xHCI Extended Capabilities
  - Host Controller Runtime Registers
  - Doorbell Registers

- USB3HOST's specific registers
  - Core Control and Status Registers
  - Battery Charging Register

aclk is supplied to the USB3HOST from CPG, when the user reads or writes a valid value from/to these registers.

When the situations below occurred, the USB3HOST replies "SLVERR" to the AXI interconnect.

[Conditions in which the USB3HOST replies "SLVERR"]

- The case of access to the Renesas private registers in the register group "Renesas Private Registers", when CORECTRL.RELPVAEN is set to 0.
- The case of access to the related CPC's registers (CRCRL, and CRCRH) or the related HEP's registers (IMAN, IMOD, ERSTSZ, ERSTBAL, ERSTBAH, ERDPL, and ERDPH) in the "Suspend" state of the USB Power State.

For the register base address (<USB_S0_base>), see the section of Address Map.

35.5.3.1 Register Overview

Operational Base = CAPLENGTH : 0020h

U3 Port Register Offset : 0420h

U2 Port Register Offset : 0420h + (CFGSTS1.U3NUM)*10h

Extended Capability Base = HCCPARAMS1.xECP << 2 : 0500h

USB Legacy Support Capability : 0500h

xHCI Supported Protocol Capability for USB3.1 : 0510h

xHCI Supported Protocol Capability for USB2.0 : 0530h

xHCI Extended Power Management Capability : 0550h

Runtime Base = RTSOFF : 0600h

Doorbell Base = DBOFF : 0700h

Table 35.5-2 USB3HOST Registers Overview (1/4)

Offset Address	Register Group		Register Name
0000h	Host Controller Capability Registers		Capability Register Length and Interface Version Number Register (USB_HOST_CAPLENGTH_HCIVERSION)
0004h			Structual Parameters 1 Register (USB_HOST_HCSPARAMS1)
0008h			Structual Parameters 2 Register (USB_HOST_HCSPARAMS2)
000Ch			Structual Parameters 3 Register (USB_HOST_HCSPARAMS3)
0010h			Capability Parameter 1 Register (USB_HOST_HCCPARAMS1)
0014h			Doorbell Offset Register (USB_HOST_DBOFF)
0018h			Runtime Register Space Offest Register (USB_HOST_RTSOFF)
001Ch			Capability Parameter 2 Register (USB_HOST_HCCPARAMS2)
0020h	Host Controller Operational Registers	—	USB Command Register (USB_HOST_USBCMD)
0024h			USB Status Register (USB_HOST_USBSTS)
0028h			Page Size Register (USB_HOST_PAGESIZE)
002Ch to 0033h			Reserved
0034h			Device Notification Control Register (USB_HOST_DNCTRL)
0038h			Command Ring Control Low Register (USB_HOST_CRCRL)
003Ch			Command Ring Control High Register (USB_HOST_CRCRH)
0040h to 004Fh			Reserved
0050h			Device Context Base Addrtess Array Pointer Low Register (USB_HOST_DCBAAPL)
0054h			Device Context Base Address Array Pointer High Register (USB_HOST_DCBAAPH)
0058h			Configure Register (USB_HOST_CONFIG)
005Ch to 041Fh		Reserved	Reserved

Table 35.5-2 USB3HOST Registers Overview (2/4)

Offset Address	Register Group		Register Name
0420h		Port Register Set 1 <U3 Port1>	U3P1 Port Status and Control Register (USB_HOST_U3P1PORTSC)
0424h			U3P1 Port Power Management Status and Control Register (USB_HOST_U3P1PORTPMSC)
0428h			U3P1 Port Link Info Register (USB_HOST_U3P1PORTLI)
042Ch			U3P1 Port Hardware LPM Control Register (USB_HOST_U3P1PORTHLPMC)
0430h		Port Register Set 2 <U2 Port1>	U2P1 Port Status and Control Register (USB_HOST_U2P1PORTSC)
0434h			U2P1 Port Power Management Status and Control Register (USB_HOST_U2P1PORTPMSC)
0438h			USB_HOST_U2P1 Port Link Info Register (U2P1PORTLI)
043Ch			U2P1 Port Hardware LPM Control Register (USB_HOST_U2P1PORTHLPMC)
0440h to 04FFh	Reserved		Reserved
0500h	xHCI Extended Capabilities	USB Legacy Support Capability	USB Legacy Support Capability Register (USB_HOST_USBLEGSUP)
0504h			USB Legacy Support Control and Status Register (USB_HOST_USBLEGCTLSTS)
0508h to 050Fh		Reserved	Reserved
0510h		xHCI Supported Protocol Capability for USB3.1	Offset 00h – xHCI Supported Protocol Capability Field Definitions (USB_HOST_U3HCSPC1)
0514h			Offset 04h – xHCI Supported Protocol Capability Field Definitions (USB_HOST_U3HCSPC2)
0518h			Offset 08h – xHCI Supported Protocol Capability Field Definitions (USB_HOST_U3HCSPC3)
051Ch			Offset 0Ch – xHCI Supported Protocol Capability Field Definitions (USB_HOST_U3HCSPC4)
0520h			Protocol Speed ID for SS (USB_HOST_PSISS)
0524h			Renesas Private (USB_HOST_RP)
0528h to 052Fh		Reserved	Reserved
0530h		xHCI Supported Protocol Capability for USB2.0	Offset 00h – xHCI Supported Protocol Capability Field Definitions (USB_HOST_U2HCSPC1)
0534h			Offset 04h – xHCI Supported Protocol Capability Field Definitions (USB_HOST_U2HCSPC2)
0538h			Offset 08h – xHCI Supported Protocol Capability Field Definitions (USB_HOST_U2HCSPC3)
053Ch			Offset 0Ch – xHCI Supported Protocol Capability Field Definitions (USB_HOST_U2HCSPC4)
0540h			Protocol Speed ID for FS (USB_HOST_PSIFS)
0544h			Protocol Speed ID for LS (USB_HOST_PSILS)
0548h			Protocol Speed ID for HS (USB_HOST_PSIHS)
054Ch		Reserved	Reserved
0550h		xHCI Extended Power Management Capability	Power Management Capabilities (USB_HOST_PMC)
0554h			Power Management Control/Status (USB_HOST_PMCSR)
0558h to 05FFh	Reserved		Reserved

Table 35.5-2 USB3HOST Registers Overview (3/4)

Offset Address	Register Group		Register Name
0600h	Host Controller Runtime Registers	—	Microframe Index Register (USB_HOST_MFINDEX)
0604h to 061Fh		Reserved	Reserved
0620h		Interrupter Register Set 0	Interrupter Management Register (USB_HOST_IMAN)
0624h			Interrupter Moderation Register (USB_HOST_IMOD)
0628h			Event Ring Segment Table Size Register (USB_HOST_ERSTSZ)
062Ch			Reserved
0630h			Event Ring Segment Table Base Address Low Register (USB_HOST_ERSTBAL)
0634h			Event Ring Segment Table Base Address High Register (USB_HOST_ERSTBAH)
0638h			Event Ring Dequeue Pointer Low Register (USB_HOST_ERDPL)
063Ch			Event Ring Dequeue Pointer High Register (USB_HOST_ERDPH)
0640h to 06FFh	Reserved		Reserved
0700h	Doorbell Registers		Host Controller Doorbell Register (USB_HOST_HCD)
0704h			Device Context Doorbell Register (Slot #1) (USB_HOST_DCD01)
0708h			Device Context Doorbell Register (Slot #2) (USB_HOST_DCD02)
070Ch			Device Context Doorbell Register (Slot #3) (USB_HOST_DCD03)
0710h			Device Context Doorbell Register (Slot #4) (USB_HOST_DCD04)
0714h			Device Context Doorbell Register (Slot #5) (USB_HOST_DCD05)
0718h			Device Context Doorbell Register (Slot #6) (USB_HOST_DCD06)
071Ch			Device Context Doorbell Register (Slot #7) (USB_HOST_DCD07)
0720h			Device Context Doorbell Register (Slot #8) (USB_HOST_DCD08)
0724h			Device Context Doorbell Register (Slot #9) (USB_HOST_DCD09)
0728h			Device Context Doorbell Register (Slot #10) (USB_HOST_DCD10)
072Ch			Device Context Doorbell Register (Slot #11) (USB_HOST_DCD11)
0730h			Device Context Doorbell Register (Slot #12) (USB_HOST_DCD12)
0734h			Device Context Doorbell Register (Slot #13) (USB_HOST_DCD13)
0738h			Device Context Doorbell Register (Slot #14) (USB_HOST_DCD14)
073Ch			Device Context Doorbell Register (Slot #15) (USB_HOST_DCD15)
0740h			Device Context Doorbell Register (Slot #16) (USB_HOST_DCD16)
0744h			Device Context Doorbell Register (Slot #17) (USB_HOST_DCD17)
0748h			Device Context Doorbell Register (Slot #18) (USB_HOST_DCD18)
074Ch			Device Context Doorbell Register (Slot #19) (USB_HOST_DCD19)
0750h			Device Context Doorbell Register (Slot #20) (USB_HOST_DCD20)
0754h			Device Context Doorbell Register (Slot #21) (USB_HOST_DCD21)
0758h			Device Context Doorbell Register (Slot #22) (USB_HOST_DCD22)
075Ch			Device Context Doorbell Register (Slot #23) (USB_HOST_DCD23)
0760h			Device Context Doorbell Register (Slot #24) (USB_HOST_DCD24)
0764h			Device Context Doorbell Register (Slot #25) (USB_HOST_DCD25)
0768h			Device Context Doorbell Register (Slot #26) (USB_HOST_DCD26)
076Ch			Device Context Doorbell Register (Slot #27) (USB_HOST_DCD27)
0770h			Device Context Doorbell Register (Slot #28) (USB_HOST_DCD28)

Table 35.5-2 USB3HOST Registers Overview (4/4)

Offset Address	Register Group		Register Name
0774h			Device Context Doorbell Register (Slot #29) (USB_HOST_DCD29)
0778h			Device Context Doorbell Register (Slot #30) (USB_HOST_DCD30)
077Ch			Device Context Doorbell Register (Slot #31) (USB_HOST_DCD31)
0780h			Device Context Doorbell Register (Slot #32) (USB_HOST_DCD32)
0784h to 0FFFh	Reserved		Reserved
1000h	Core Difined Registers	Core Control and Status Registers	Revision ID Register (USB_HOST_REVID)
1004h			Configuration Status1 Register (USB_HOST_CFGSTS1)
1008h			Configuration Status2 Register (USB_HOST_CFGSTS2)
100Ch			Configuration Status3 Register (USB_HOST_CFGSTS3)
1010h			Configuration Status4 Register (USB_HOST_CFGSTS4)
1014h			Configuration Status5 Register (USB_HOST_CFGSTS5)
1018h			Configuration Status6 Register (USB_HOST_CFGSTS6)
101Ch			Configuration Status7 Register (USB_HOST_CFGSTS7)
1020h			Configuration Status8 Register (USB_HOST_CFGSTS8)
1024h			Configuration Status9 Register (USB_HOST_CFGSTS9)
1028h			Configuration Status10 Register (USB_HOST_CFGSTS10)
102Ch			Data Buffer Threshold Control Register (USB_HOST_DBUFTH)
1030h			Core Control Register (USB_HOST_CORECTRL)
1034h			PHY Control Register (USB_HOST_PHYCTRL)
1038h			PHY Status Register (USB_HOST_PHYSTS)
103Ch			Renesas Private Register (USB_HOST_RP2)
1040h			Interrupt Status Register (USB_HOST_INTSTS)
1044h			Interrupt Enable Register (USB_HOST_INTEN)
1048h to 104Fh			Reserved
1050h			Frame Length Adjustment Register (FLADJ) & Serial Bus Release Number Register (SBRN) (USB_HOST_FLADJ_SBRN)
1054h to 107Fh		Reserved	Reserved
1080h		Battery Charging Register	Battery Charging Control Register (USB_HOST_BCCTRL)
1084h to 10AFh		Reserved	Reserved
10B0h to 1AFFh	Renesas Private Registers	—	—

35.5.3.2 Register List of Each Category

(1) Host Controller Capability Registers

Table 35.5-3 List of Host Controller Capability Registers (1/2)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
eXtensible Host Controller Capability (000h to 01Ch)								
CAPLENGTH and HCIVERSION								
003h	Host Controller Interface Version Number (HCIVERSION)							
002h								
001h	—	—	—	—	—	—	—	—
000h	Capability Registers Length (CAPLENGTH)							
HCSPARAMS1								
007h	Max Ports							
006h	—	—	—	—	—	Max Interrupters		
005h	Max Interrupters							
004h	Max Device Slots							
HCSPARAMS2								
00Bh	Max Scratchpad Buffers					Scratchpad Restore (SPR)	—	—
00Ah	—	—	—	—	—	—	—	—
009h	—	—	—	—	—	—	—	—
008h	Event Ring Segment Table Max (ERST Max)				ISO Scheduling Threshold (IST)			
HCSPARAMS3								
00Fh	U2 Device Exit Latency							
00Eh								
00Dh	—	—	—	—	—	—	—	—
00Ch	U1 Device Exit Latency							
HCCPARAMS1								
013h	xHCI Extended Capabilities Pointer (xECP)							
012h								
011h	Maximum Primary Stream Array Size (MaxPSASize)				Contiguous Frame ID Capability (CFC)	Stopped EDTLA Capability (SEC)	Stopped Short Packet Capability (SPC)	Parse All Event data (PAE)
010h	No Secondary SID Support (NSS)	Latency Tolerance Messaging Capability (LTC)	Light HC Reset Capability (LHRC)	Port Indicators (PIND)	Port Power Control (PPC)	Context Size (CSZ)	BW Negotiation Capability (BNC)	64-bit Addressing Capability (AC64)
DBOFF								
017h	DBOFF							
016h								
015h								
014h	DBOFF						—	—

Table 35.5-3 List of Host Controller Capability Registers (2/2)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RSTOFF								
01Bh	RTSOFF							
01Ah								
019h								
018h	RTSOFF			—	—	—	—	—
HCCPARAMS2								
01Fh	—	—	—	—	—	—	—	—
01Eh	—	—	—	—	—	—	—	—
01Dh	—	—	—	—	—	—	—	—
01Ch	—	—	Configuration Information Capability (CIC)	Large ESIT Payload Capability (LEC)	Compliance Transition Capability (CTC)	Force Save Context Capability (FSC)	Configure Endpoint Command Max Exit Latency Too Large Capability (CMC)	U3 Entry Capability (U3C)

(2) Host Controller Operational Registers

Table 35.5-4 List of Host Controller Operational Registers (1/2)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Host Controller Operational (020h to 05Ch)								
USBCMD								
023h	—	—	—	—	—	—	—	—
022h	—	—	—	—	—	—	—	—
021h	—	—	CEM Enable (CME)	Stopped Short Packet Enable (SPE)	Enable U3 MFINDEX Stop (EU3S)	Enable Wrap Event (EWE)	Controller Restore State (CRS)	Controller Save State (CSS)
020h	Light Host Controller Reset (LHCRST)	—	—	—	Host System Error Enable (HSEE)	Interrupter Enable (INTE)	Host Controller Reset (HCRST)	Run/Stop (RS)
USBSTS								
027h	—	—	—	—	—	—	—	—
026h	—	—	—	—	—	—	—	—
025h	—	—	—	Host Controller Error (HCE)	Controller Not Ready (CNR)	Save/Restore Error (SRE)	Restore State Status (RSS)	Save State Status (SSS)
024h	—	—	—	Port Change Detect (PCD)	Event Interrupt (EINT)	Host System Error (HSE)	—	HC Halted (HCH)
PAGESIZE								
02Bh	—	—	—	—	—	—	—	—
02Ah	—	—	—	—	—	—	—	—
029h	Page Size							
028h								
Reserved								
02Ch to 033h	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
DNCTRL								
037h	—	—	—	—	—	—	—	—
036h	—	—	—	—	—	—	—	—
035h	Notification Enable (N15)	Notification Enable (N14)	Notification Enable (N13)	Notification Enable (N13)	Notification Enable (N11)	Notification Enable (N10)	Notification Enable (N9)	Notification Enable (N8)
034h	Notification Enable (N7)	Notification Enable (N6)	Notification Enable (N5)	Notification Enable (N4)	Notification Enable (N3)	Notification Enable (N2)	Notification Enable (N1)	Notification Enable (N0)

Table 35.5-4 List of Host Controller Operational Registers (2/2)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CRCRL								
03Bh	Command Ring Pointer Lo							
03Ah								
039h								
038h	Command Ring Pointer Lo		—	—	Command Ring Running (CRR)	Command Abort (CA)	Command Stop (CS)	Ring Cycle State (RCS)
CRCRH								
03Fh	Command Ring Pointer Hi							
03Eh								
03Dh								
03Ch								
Reserved								
040h to 04Fh	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	
DCBAAPL								
053h	Device Context Base Address Array Pointer Lo							
052h								
051h								
05Ch	Device Context Base Address Array Pointer Lo		—	—	—	—	—	—
DCBAAPH								
057h	Device Context Base Address Array Pointer Hi							
056h								
055h								
054h								
CONFIG								
05Bh	—	—	—	—	—	—	—	—
05Ah	—	—	—	—	—	—	—	—
059h	—	—	—	—	—	—	CIE	U3E
058h	Max Device Slots Enabled (MaxSlotsEn)							
Reserved								
05Ch to 041Fh	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—

(3) Port Register Sets in Host Controller Operational Registers

Table 35.5-5 List of Port Register Sets in Host Controller Operational Registers (1/2)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
USB3.1 Port Status and Control Register (U3P[m]PORTSC) [m : 1]								
423h	WPR	DR	—	—	WOE	WDE	WCE	CAS
422h	CEC	PLC	PRC	OOC	WRC	PEC	CSC	LWS
421h	PIC		Port Speed				PP	PLS[3]
420h	PLS[2:0]			PR	OCA	—	PED	CCS
USB3.1 Port Power Management Status and Control Register (U3P[m]PORTPMSC) [m : 1]								
427h	—	—	—	—	—	—	—	—
426h	—	—	—	—	—	—	—	FLA
425h	U2 Timeout							
424h	U1 Timeout							
USB3.1 Port Link Info Register (U3P[m]PORTLI) [m : 1]								
42Bh	—	—	—	—	—	—	—	—
42Ah	TLC				RLC			
429h	Link Error Count							
428h								
USB3.1 Port Hardware LPM Control Register (U3P[m]PORTHLPMC) [m : 1]								
42Fh	—	—	—	—	—	—	—	—
42Eh	—	—	—	—	—	—	—	—
42Dh	—	—	—	—	—	—	—	—
42Ch	—	—	—	—	—	—	—	—
USB2.0 Port Status and Control Register (U2P[m]PORTSC) [m : 1]								
433h	—	DR	—	—	WOE	WDE	WCE	CAS
432h	—	PLC	PRC	OOC	—	PEC	CSC	LWS
431h	PIC		Port Speed				PP	PLS[3]
430h	PLS[2:0]			PR	OCA	—	PED	CCS
USB2.0 Port Power Management Status and Control Register (U2P[m]PORTPMSC) [m : 1]								
437h	Test Mode				—	—	—	—
436h	—	—	—	—	—	—	—	HLE
435h	L1 Device Slot							
434h	BESL				RWE	L1S		
USB2.0 Port Link Info Register (U2P[m]PORTLI) [m : 1]								
43Bh	—	—	—	—	—	—	—	—
43Ah	—	—	—	—	—	—	—	—
439h	—	—	—	—	—	—	—	—
438h	—	—	—	—	—	—	—	—
USB2.0 Port Hardware LPM Power Control Register (U2P[m]PORTHLPMC) [m : 1]								
43Fh	—	—	—	—	—	—	—	—
43Eh	—	—	—	—	—	—	—	—
43Dh	—	—	BESLD				L1 Timeout [7:6]	
43Ch	L1 Timeout [5:0]						HIRDM	

Table 35.5-5 List of Port Register Sets in Host Controller Operational Registers (2/2)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved								
440h to 4FFh	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—

(4) xHCI Extended Capabilities

Table 35.5-6 List of xHCI Extended Capabilities (1/3)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
USB Legacy Support Capability (500h to 50Fh)								
USB Legacy Support Capability Register (USBLEGSUP)								
503h	—	—	—	—	—	—	—	HOOS
502h	—	—	—	—	—	—	—	HBOS
501h	Next Capability Pointer							
500h	Capability ID							
USB Legacy Support Control and Status Register (USBLEGCTLSTS)								
507h	SBA	SPC	SOOC	—	—	—	—	—
506h	—	—	—	SHSE	—	—	—	SEI
505h	SBAE	SPCE	SOOE	—	—	—	—	—
504h	—	—	—	SHSEE	—	—	—	USE
Reserved								
50Bh	—	—	—	—	—	—	—	—
50Ah	—	—	—	—	—	—	—	—
509h	—	—	—	—	—	—	—	—
508h	—	—	—	—	—	—		
Reserved								
50Fh	—	—	—	—	—	—	—	—
50Eh	—	—	—	—	—	—	—	—
50Dh	—	—	—	—	—	—	—	—
50Ch	—	—	—	—	—	—		
xHCI Supported Protocol Capability for USB3.1 (510h to 52Fh)								
Offset 00h – xHCI Supported Protocol Capability Field Definitions								
513h	Major Revision							
512h	Minor Revision							
511h	Next Capability Pointer							
510h	Capability ID							
Offset 04h – xHCI Supported Protocol Capability Field Definitions								
517h	Name String							
516h								
515h								
514h								
Offset 08h – xHCI Supported Protocol Capability Field Definitions								
51Bh	Protocol Speed ID Count (PSIC)				Hub Depth (MHD)			—
51Ah	—	—	—	—	—	—	—	—
519h	Compatible Port Count							
518h	Compatible Port Offset							

Table 35.5-6 List of xHCI Extended Capabilities (2/3)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Offset 0Ch – xHCI Supported Protocol Capability Field Definitions								
51Fh	—	—	—	—	—	—	—	—
51Eh	—	—	—	—	—	—	—	—
51Dh	—	—	—	—	—	—	—	—
51Ch	—	—	—	Protocol Slot Type				
Protocol Speed ID for SS (PSISS)								
523h	Protocol Speed ID Mantissa (PSIM)							
522h								
521h	—	—	—	—	—	—	—	PFD
520h	PLT		PSIE		Protocol Speed ID Value (PSIV)			
Renesas Private Register								
527h	Renesas Private							
526h								
525h	—	—	—	—	—	—	—	Renesas Private
524h	Renesas Private		Renesas Private		Renesas Private			
Reserved								
528h to 52Fh	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—		
xHCI Supported Protocol Capability for USB2.0 (530h to 54Fh)								
Offset 00h – xHCI Supported Protocol Capability Field Definitions								
533h	Major Revision							
532h	Minor Revision							
531h	Next Capability Pointer							
530h	Capability ID							
Offset 04h – xHCI Supported Protocol Capability Field Definitions								
537h	Name String							
536h								
535h								
534h								
Offset 08h – xHCI Supported Protocol Capability Field Definitions								
53Bh	Protocol Speed ID Count				Hub Depth (MHD)			—
53Ah	—	—	—	BLC	HLC	IHI	HSO	—
539h	Compatible Port Count							
538h	Compatible Port Offset							
Offset 0Ch – xHCI Supported Protocol Capability Field Definitions								
53Fh	—	—	—	—	—	—	—	—
53Eh	—	—	—	—	—	—	—	—
53Dh	—	—	—	—	—	—	—	—
53Ch	—	—	—	Protocol Slot Type				

Table 35.5-6 List of xHCI Extended Capabilities (3/3)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Protocol Speed ID for FS								
543h	Protocol Speed ID Mantissa (PSIM)							
542h								
541h	—	—	—	—	—	—	—	PFD
540h	PLT		PSIE		Protocol Speed ID Value			
Protocol Speed ID for LS								
547h	Protocol Speed ID Mantissa (PSIM)							
546h								
545h	—	—	—	—	—	—	—	PFD
544h	PLT		PSIE		Protocol Speed ID Value			
Protocol Speed ID for HS								
54Bh	Protocol Speed ID Mantissa (PSIM)							
54Ah								
549h	—	—	—	—	—	—	—	PFD
548h	PLT		PSIE		Protocol Speed ID Value			
Reserved								
54Fh	—	—	—	—	—	—	—	—
54Eh	—	—	—	—	—	—	—	—
54Dh	—	—	—	—	—	—	—	—
54Ch	—	—	—	—	—	—		
xHCI Extended Power Management Capability								
Power Mangement Capabilities (PMC)								
553h	PME Support					D2 Support	D1 Support	Aux Current[2]
552h	Aux Current[1:0]		DSI	—	PME Clock	Version		
551h	Next Capability Pointer							
550h	Capability ID							
Power Management Control/Status (PMCSR)								
557h	—	—	—	—	—	—	—	—
556h	—	—	—	—	—	—	—	—
555h	PME Status	Data Scale		Data Select				PME En
554h	—	—	—	—	No Soft Reset	—	Power State	
Reserved								
558h to 55Fh	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—

(5) Host Controller Runtime Registers

Table 35.5-7 List of Host Controller Runtime Registers (1/2)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Host Controller Runtime (600h to 63Ch)								
MFINDEX Register								
603h	—	—	—	—	—	—	—	—
602h	—	—	—	—	—	—	—	—
601h	—	—	Microframe Index					
600h	Microframe Index							
Reserved								
604h to 61Fh	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
IMAN								
623h	—	—	—	—	—	—	—	—
622h	—	—	—	—	—	—	—	—
621h	—	—	—	—	—	—	—	—
620h	—	—	—	—	—	—	Interrupt Enable (IE)	Interrupt Pending (IP)
IMOD								
627h	Counter (IMODC)							
626h								
625h	Interval (IMODI)							
624h								
ERSTSZ								
62Bh	—	—	—	—	—	—	—	—
62Ah	—	—	—	—	—	—	—	—
629h	Event Ring Segment Table Size							
628h								
Reserved								
62Fh	—	—	—	—	—	—	—	—
62Eh	—	—	—	—	—	—	—	—
62Dh	—	—	—	—	—	—	—	—
62Ch	—	—	—	—	—	—	—	—
ERSTBAL								
633h	Event Ring Segment Table Base Address Register bit Definitions (ERSTBA) Lo							
632h								
631h								
630h	Event Ring Segment Table Base Address Register bit Definitions (ERSTBA) Lo		—	—	—	—	—	—

Table 35.5-7 List of Host Controller Runtime Registers (2/2)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ERSTBAH								
637h	Event Ring Segment Table Base Address Register bit Definitions (ERSTBA) Hi							
636h								
635h								
634h								
ERDPL								
63Bh	Event Ring Dequeue Pointer Lo							
63Ah								
639h								
638h	Event Ring Dequeue Pointer Lo				Event Handler Busy (EHB)	Dequeue ERST Segment Index (DESI)		
ERDPH								
63Fh	Event Ring Dequeue Pointer Hi							
63Eh								
63Dh								
63Ch								

(6) Doorbell Registers

Table 35.5-8 List of Doorbell Registers

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Host Controller Doorbell (700h to 783h)								
Host Controller Doorbell								
703h	—	—	—	—	—	—	—	—
702h	—	—	—	—	—	—	—	—
701h	—	—	—	—	—	—	—	—
700h	DB Target							
Device Context Doorbell #1 to #32								
704h to 783h	DB Stream ID							
	—	—	—	—	—	—	—	—
	DB Target							
Reserved								
784h to 7FFh	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—

(7) Core Defined Registers

Table 35.5-9 List of Core Defined Registers (1/4)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Core Control and Status Register (1000h to 107Fh)								
Revision ID Register (REVID)								
1003h	Core ID							
1002h	Library							
1001h	Major Version							
1000h	Minor Version							
Configuration Status1 Register (CFGSTS1)								
1007h	—	—	—	—	—	—	DENSPNDOP	INTEDGEN
1006h	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private		Renesas Private
1005h	Renesas Private	Renesas Private	Renesas Private	Renesas Private	—	REPNUM		
1004h	—	U3NUM			—	U2NUM		
Configuration Status2 Register (CFGSTS2)								
100Bh	ACLKFREQ							
100Ah								
1009h								
1008h								
Configuration Status3 Register (CFGSTS3)								
100Fh	—	—	—	—	—	—	—	Renesas Private
100Eh	Renesas Private	Renesas Private	Renesas Private	Renesas Private	—	Renesas Private		
100Dh	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private
100Ch	—	—	Renesas Private	Renesas Private	Renesas Private			
Configuration Status4 Register (CFGSTS4)								
1013h	—	—	—	—	—	—	Renesas Private	
1012h	Renesas Private							
1011h	—	—	—	—	—	—	Renesas Private	
1010h	Renesas Private							
Configuration Status5 Register (CFGSTS5)								
1017h	—	—	—	—	—	—	Renesas Private	
1016h	Renesas Private							
1015h	—	—	—	—	—	—	Renesas Private	
1014h	Renesas Private							
Configuration Status6 Register (CFGSTS6)								
101Bh	—	—	—	—	—	—	Renesas Private	
101Ah	Renesas Private							
1019h	—	—	—	—	—	—	Renesas Private	
1018h	Renesas Private							

Table 35.5-9 List of Core Defined Registers (2/4)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Configuration Status7 Register (CFGSTS7)								
101Fh	—	—	—	—	—	—	Renesas Private	
101Eh	Renesas Private							
101Dh	—	—	—	—	—	—	Renesas Private	
101Ch	Renesas Private							
Configuration Status8 Register (CFGSTS8)								
1023h	—	—	—	—	—	—	Renesas Private	
1022h	Renesas Private							
1021h	—	—	—	—	—	—	Renesas Private	
1020h	Renesas Private							
Configuration Status9 Register (CFGSTS9)								
1027h	—	—	—	—	—	—	Renesas Private	
1026h	Renesas Private							
1025h	—	—	—	—	—	—	Renesas Private	
1024h	Renesas Private							
Configuration Status10 Register (CFGSTS10)								
102Bh	—	—	—	—	—	—	—	—
102Ah	—	—	—	SS Data Buffer Size				
1029h	—	—	—	Renesas Private				
1028h	—	U2 Data Buffer Size			—	—	Renesas Private	
Data Buffer Threshold Control Register (BDUFTH)								
102Fh	—	—	Renesas Private		—	—	Renesas Private	
102Eh	—	—	Renesas Private		—	—	Renesas Private	
102Dh	—	—	—	—	—	—	Renesas Private	
102Ch	—	—	Renesas Private		—	—	Renesas Private	
Core Control Register (CORECTRL)								
1033h	Renesas Private	—	—	—	—	—	—	—
1032h	—	—	—	—	—	—	—	Renesas Private
1031h	Renesas Private				—	Renesas Private	Renesas Private	Renesas Private
1030h	—	—	—	—	—	—	—	Renesas Private
PHY Control Register (PHYCTRL)								
1037h	Renesas Private	Renesas Private	Renesas Private	Renesas Private	—	—	—	—
1036h	—	—	—	—	Renesas Private	Renesas Private	Renesas Private	U3P1PHY_RST
1035h	—	—	—	—	—	—	—	FA_U2PLL
1034h	—	—	—	—	—	—	—	U2PHY_RST

Table 35.5-9 List of Core Defined Registers (3/4)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PHY Status Register (PHYSTS)								
103Bh	—	—	—	—	—	—	—	—
103Ah	—	—	—	—	Renesas Private	Renesas Private	Renesas Private	U3P1PLL _LOCK
1039h	—	—	—	—	—	—	—	—
1038h	—	—	—	—	—	—	—	U2PLL _LOCK
Renesas Private Register								
103Fh	—	—	—	—	—	—	—	—
103Eh	—	—	—	—	—	—	Renesas Private	
103Dh	Renesas Private							
103Ch	Renesas Private							
Interrupt Status Register (INTSTS)								
1043h	—	—	—	—	—	—	—	—
1042h	—	—	—	—	—	—	—	—
1041h	—	—	—	—	—	—	—	—
1040h	—	—	—	SMI_INT	—	HSE_INT	PME_INT	XHC_INT
Interrupt Enable Register (INTEN)								
1047h	—	—	—	—	—	—	—	—
1046h	—	—	—	—	—	—	—	—
1045h	—	—	—	—	—	—	—	—
1044h	—	—	—	SMI_INTE	—	HSE_INTE	PME_INTE	XHC_INTE
Reserved								
1048h to 104Fh	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
Frame Length Adjustment Register (FLADJ) & Serial Bus Release Number Register (SBRN) <if define iHAVE_FLADJ_REG>								
1053h	—	—	—	—	—	—	—	—
1052h	Default Best Effort Service Latency Deep (DBESLD)				Default Best Effort Service Latency (DBESL)			
1051h	—	NFC	Frame Length Adjustment					
1050h	Serial Bus Release Number							
Reserved								
1054h to 106Fh	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—		
Reserved								
1070h	—	—	—	—	—	—	—	—
1071h	—	—	—	—	—	—	—	—
1072h	—	—	—	—	—	—	—	—
1073h	—	—	—	—	—	—	—	—

Table 35.5-9 List of Core Defined Registers (4/4)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved								
1074h to 107Fh	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—		—
Battery Charging Register (1080h to 108Fh)								
Battery Charging Control Register (BCCTRL)								
1083h	—	—	—	—	—	—	—	—
1082h	—	—	—	—	—	—	—	—
1081h	—	—	—	—	Renesas Private	Renesas Private	Renesas Private	Renesas Private
1080h	Renesas Private		Renesas Private		Renesas Private		BC_MODE_P1	
Reserved								
1084h to 10AFh	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
Renesas Private Registers								
10B0h to 1AFFh	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—

35.5.4 Register Descriptions

The function description of each register is given below.

The prefix (USB_HOST_) of the register names is omitted in the register descriptions and the field descriptions in this section.

35.5.4.1 Host Controller Capability Registers

(1) Capability Register Length and Interface Version Number Register (USB_HOST_CAPLENGTH_HCIVERSION)

This register indicates the capability register length and the interface version number.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0000h

Initial Value: 0110_0020h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	HCIVERSION															
Initial Value	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CAPLENGTH							
Initial Value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-10 USB_HOST_CAPLENGTH_HCIVERSION Register Contents

Bit Position	Bit Name	Description
31 to 16	HCIVERSION	This is a two-byte register containing a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision. (Ex) 0110h corresponds to xHCI version 1.1.
15 to 8	—	Reserved
7 to 0	CAPLENGTH	This register is used as an offset to add to register base to find the beginning of the Operational Register Space.

(2) Structural Parameters 1 Register (USB_HOST_HCSPARAMS1)

This register is the structural parameter register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0004h

Initial Value: 0200_0120h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Number of Ports								—	—	—	—	—	Number of Interrupters		
Initial Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Number of Interrupters								Number of Device Slots							
Initial Value	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-11 USB_HOST_HCSPARAMS1 Register Contents

Bit Position	Bit Name	Description
31 to 24	Number of Ports	This field specifies the maximum Port Number value, i.e. the highest numbered Port Register Sets that are addressable in the Operational Register Space. Valid values are in the range of 1h to FFh. The value in this field shall reflect the maximum Port Number value assigned by an xHCI Supported Protocol Capability, described in section 7.2 of xHCI Specification. Software shall refer to these capabilities to identify whether a specific Port Number is valid, and the protocol supported by the associated Port Register Set.
23 to 19	—	Reserved
18 to 8	Number of Interrupters	This field specifies the number of Interrupters implemented on this host controller. Each Interrupter may be allocated to MSI or MSI-X vector and controls its generation and moderation. The value of this field determines how many Interrupter Register Sets are addressable in the Runtime Register Space. Valid values are in the range of 1h to 400h. A 0h in this field is undefined
7 to 0	Number of Device Slots	This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255. The value of 0b is reserved.

(3) Structural Parameters 2 Register (USB_HOST_HCSPARAMS2)

This register is the structural parameter register 2.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0008h

Initial Value: 0000_0011h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Max Scratchpad Buffers (Max Scratchpad Bufs Lo)					Scratch pad Restore (SPR)	Max Scratchpad Buffers (Max Scratchpad Bufs Hi)					—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Event Ring Segment Table Max (ERST Max)				Isochronous Scheduling Threshold (IST)			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-12 USB_HOST_HCSPARAMS2 Register Contents

Bit Position	Bit Name	Description
31 to 27	Max Scratchpad Buffers (Max Scratchpad Bufs Lo)	Default = implementation dependent. Valid values for Max Scratchpad Buffers (Hi and Lo) are 0 to 1023. This field indicates the lower-order 5 bits of the number of Scratchpad Buffers system software reserves for the xHC.
26	Scratchpad Restore (SPR)	Default = implementation dependent. If Max Scratchpad Buffers is greater than 0 then this flag indicates whether the xHC uses the Scratchpad Buffers for saving state when executing Save and Restore State operations. If Max Scratchpad Buffers is = 0, then this flag is 0. The value 1 indicates that the xHC requires the integrity of the space for the Scratchpad Buffer to be maintained across power events. The value 0 indicates that the space for the Scratchpad Buffer can freed and reallocated between power events.
25 to 21	Max Scratchpad Buffers (Max Scratchpad Bufs Hi)	Default = implementation dependent. This field indicates the higher-order 5 bits of the number of Scratchpad Buffers system software reserves for the xHC.
20 to 8	—	Reserved
7 to 4	Event Ring Segment Table Max (ERST Max)	Default = implementation dependent. Valid values are 0 to 15. This field determines the maximum value supported the Event Ring Segment Table Base Size registers, where: The maximum number of Event Ring Segment Table entries = 2 ERST Max. e.g. if the ERST Max = 7, then the xHC Event Ring Segment Table(s) supports up to 128 entries, 15 then 32K entries, etc.
3 to 0	Isochronous Scheduling Threshold (IST)	Default = implementation dependent. The value in this field indicates to system software the minimum distance (in time) that it is required to stay ahead of the host controller while adding TRBs, in order to have the host controller process them at the correct time. The value shall be specified in terms of number of frames/microframes. If bit [3] of the IST is cleared to 0, software can add a TRB no later than IST[2:0] Microframes before that TRB is scheduled to be executed. If bit [3] of the IST is set to 1, a TRB is added by software no later than IST[2:0] Frames before that TRB is scheduled to be executed.

(4) Structural Parameters 3 Register (USB_HOST_HCSPARAMS3)

This register is the structural parameter register 3.

Access Size: 32 bits

Address(es): <USB_S0_base> + 000Ch

Initial Value: 0000_0000h

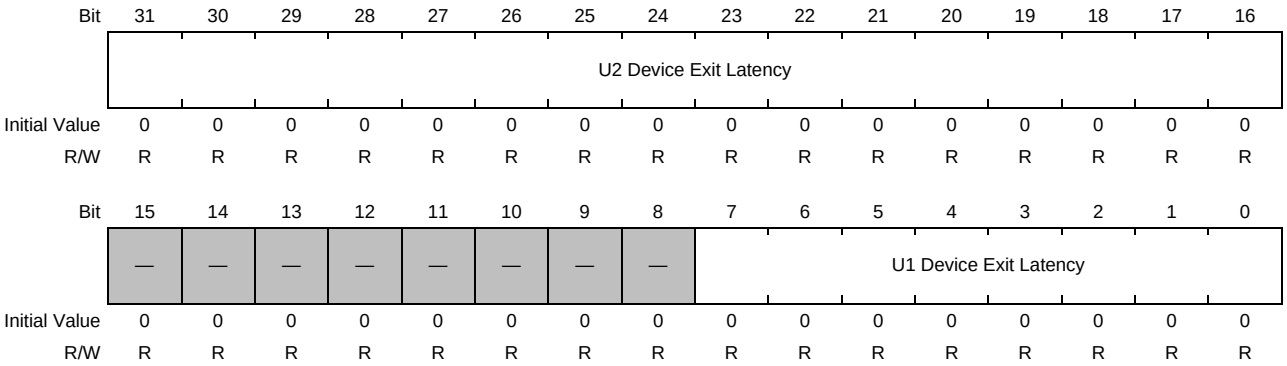


Table 35.5-13 USB_HOST_HCSPARAMS3 Register Contents

Bit Position	Bit Name	Description
31 to 16	U2 Device Exit Latency	Worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: 0000h: Zero 0001h: Less than 1 us 0002h: Less than 2 us | 07FFh: Less than 2027 us 0800h to FFFFh: Reserved
15 to 8	—	Reserved
7 to 0	U1 Device Exit Latency	Worst case latency to transition a root hub Port Link State (PLS) from U1 to U0. Applies to all root hub ports. The following are permissible values: 00h: Zero 01h: Less than 1 us 02h: Less than 2 us | 0Ah: Less than 10 us 0Bh to FFh: Reserved

(5) Capability Parameter 1 Register (USB_HOST_HCCPARAMS1)

This register is the capability parameter register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0010h

Initial Value: 0140_FE8Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	xHCI Extended Capabilities Pointer (xECP)															
Initial Value	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Maximum Primary Stream Array Size (MaxPSASize)				Contiguous Frame ID Capability (CFC)	Stopped EDTLA Capability (SEC)	Stopped Short Packet Capability (SPC)	Parse All Even Data (PAE)	No Secondary SID Support (NSS)	Latency Tolerance Messaging Capability (LTC)	Light HC Reset Capability (LHRC)	Port Indicators (PIND)	Port Power Control (PPC)	Context Size (CSZ)	BW Negotiation Capability (BNC)	64-bit Addressing Capability (AC64)
Initial Value	1	1	1	1	1	1	1	0	1	0	0	0	1	1	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-14 USB_HOST_HCCPARAMS1 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 16	xHCI Extended Capabilities Pointer (xECP)	This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability. For example, using the offset of Base is 1000h and the xECP value of 0068h, we can calculate the following effective address of the first extended capability: 1000h + (0068h << 2) -> 1000h + 01A0h -> 11A0h
15 to 12	Maximum Primary Stream Array Size (MaxPSASize)	This field identifies the maximum size Primary Stream Array that the xHC supports. The Primary Stream Array size = $2^{MaxPSASize}$+1. Valid MaxPSASize values are 0 to 15, where 0 indicates that streams are not supported
11	Contiguous Frame ID Capability (CFC)	This flag indicates that the host controller implementation is capable of matching the Frame ID of consecutive Isoch TDs.
10	Stopped EDTLA Capability (SEC)	This flag indicates that the host controller implementation Stream Context supports a Stopped EDTLA field. Stopped EDTLA Capability support (i.e. SEC = '1') shall be mandatory for all xHCI 1.1 compliant xHCs.
9	Stopped Short Packet Capability (SPC)	This flag indicates that the host controller implementation is capable of generating a Stopped Short Packet Completion Code.
8	Parse All Event Data (PAE)	This flag indicates whether the host controller implementation Parses all Event Data TRBs while advancing to the next TD after a Short Packet, or it skips all but the first Event Data TRB. A 1 in this bit indicates that all Event Data TRBs are parsed. A 0 in this bit indicates that only the first Event Data TRB is parsed.
7	No Secondary SID Support (NSS)	This flag indicates whether the host controller implementation supports Secondary Stream IDs. A 1 in this bit indicates that Secondary Stream ID decoding is not supported. A 0 in this bit indicates that Secondary Stream ID decoding is supported.
6	Latency Tolerance Messaging Capability (LTC)	This flag indicates whether the host controller implementation supports Latency Tolerance Messaging (LTM). A 1 in this bit indicates that LTM is supported. A 0 in this bit indicates that LTM is not supported.
5	Light HC Reset Capability (LHRC)	This flag indicates whether the host controller implementation supports a Light Host Controller Reset. A 1 in this bit indicates that Light Host Controller Reset is supported. A 0 in this bit indicates that Light Host Controller Reset is not supported. The value of this flag affects the functionality of the Light Host Controller Reset (LHCRST) flag in the USBCMD register.

Table 35.5-14 USB_HOST_HCCPARAMS1 Register Contents (2/2)

Bit Position	Bit Name	Description
4	Port Indicators (PIND)	This bit indicates whether the xHC root hub ports support port indicator control. When this bit is 1, the port status and control registers include a readable/writeable field for controlling the state of the port indicator.
3	Port Power Control (PPC)	This flag indicates whether the host controller implementation includes port power control. A 1 in this bit indicates the ports have port power switches. A 0 in this bit indicates the port do not have port power switches. The value of this flag affects the functionality of the PP flag in each port status and control register.
2	Context Size (CSZ)	If this bit is set to 1, then the xHC uses 64 byte Context data structures. If this bit is cleared to 0, then the xHC uses 32 byte Context data structures. *Note*: This flag does not apply to Stream Contexts
1	BW Negotiation Capability (BNC)	This flag identifies whether the xHC has implemented the Bandwidth Negotiation. Values for this flag have the following interpretation: 0b: BW Negotiation is not implemented. 1b: BW Negotiation is implemented.
0	64-bit Addressing Capability (AC64)	This flag documents the addressing range capability of this implementation. The value of this flag determines whether the xHC has implemented the higher-order 32 bits of a 64-bit register and data structure pointer fields. Values for this flag have the following interpretation: 0b: 32-bit address memory pointers are implemented 1b: 64-bit address memory pointers are implemented If 32-bit address memory pointers are implemented, the xHC ignores the higher-order 32 bits of a 64-bit data structure pointer fields, and system software ignores the higher-order 32 bits of a 64-bit xHC registers.

(6) Doorbell Offset Register (USB_HOST_DBOFF)

This register indicates the doorbell array offset.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0014h

Initial Value: 0000_0700h

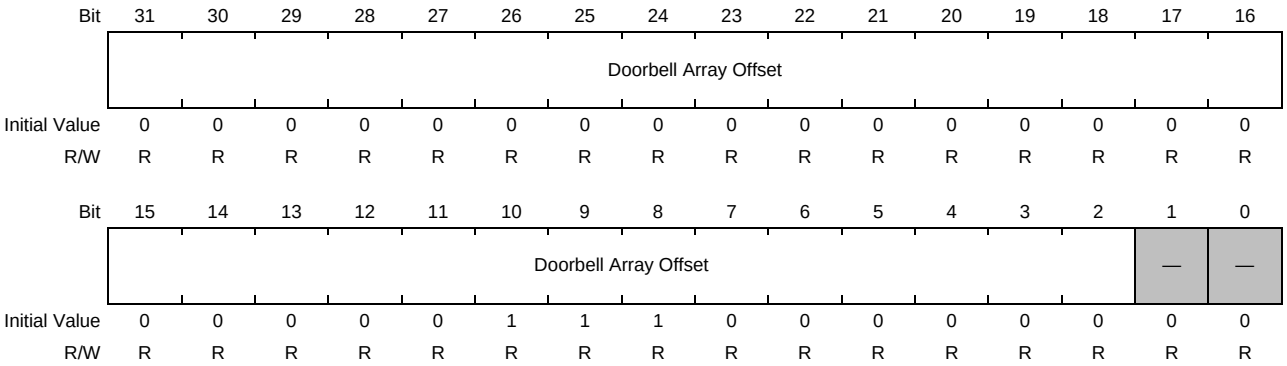


Table 35.5-15 USB_HOST_DBOFF Register Contents

Bit Position	Bit Name	Description
31 to 2	Doorbell Array Offset	Default = implementation dependent. This field defines the offset in Dwords of the base address of the Doorbell Array from main base address (i.e. the base address of the xHCI Capability register address space).
1, 0	—	Reserved

(7) Runtime Register Space Offset Register (USB_HOST_RSTOFF)

This register indicates the 32-byte offset of the xHCI Runtime Registers from the Base.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0018h

Initial Value: 0000_0600h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Runtime Register Space Offset															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Runtime Register Space Offset											—	—	—	—	—
Initial Value	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-16 USB_HOST_RSTOFF Register Contents

Bit Position	Bit Name	Description
31 to 5	Runtime Register Space Offset	Default = implementation dependent. This field defines the 32-byte offset of the xHCI Runtime Registers from the Base. i.e. Runtime Register Base Address = Base + Runtime Register Set Offset.
4 to 0	—	Reserved

(8) Capability Parameter 2 Register (USB_HOST_HCCPARAMS2)

This register is the capability parameter register 2.

Access Size: 32 bits

Address(es): <USB_S0_base> + 001Ch

Initial Value: 0000_002Dh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	Configuration Information Capability (CIC)	Large ESIT Payload Capability (LEC)	Compliance Transition Capability (CTC)	Force Save Context Capability (FSC)	Configure Endpoint Command Max Exit Latency Too Large Capability (CMC)	U3 Entry Capability (U3C)
Initial Value	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-17 USB_HOST_HCCPARAMS2 Register Contents

Bit Position	Bit Name	Description
31 to 6	—	Reserved
5	Configuration Information Capability (CIC)	This bit indicates if the xHC supports extended Configuration Information. When this bit is 1b, the Configuration Value, Interface Number, and Alternate Setting fields in the Input Control Context are supported. When this bit is 0b, the extended Input Control Context fields are not supported.
4	Large ESIT Payload Capability (LEC)	This bit indicates whether the xHC supports ESIT Payloads greater than 48K bytes. When this bit is 1b, ESIT Payloads greater than 48K bytes are supported. When this bit is 0b, ESIT Payloads greater than 48K bytes are not supported.
3	Compliance Transition Capability (CTC)	This bit indicates whether the xHC USB3 Root Hub ports support the Compliance Transition Enabled (CTE) flag. When this bit is 1b, transition of the port state machine of a USB3 Root Hub to the Compliance substate shall be explicitly enabled by software. When this bit is 0b, transition of the port state machine of a USB3 Root Hub to the Compliance substate are automatically enabled.
2	Force Save Context Capability (FSC)	This bit indicates whether the xHC supports the Force Save Context Capability. When this bit is 1b, the Save State operation shall save any cached Slot, Endpoint, Stream or other Context information to memory.
1	Configure Endpoint Command Max Exit Latency Too Large Capability (CMC)	This bit indicates whether a Configure Endpoint Command is capable of generating a Max Exit Latency Too Large Capability Error. When this bit is 1b, a Max Exit Latency Too Large Capability Error can be returned by a Configure Endpoint Command. When this bit is 0b, a Max Exit Latency Too Large Capability Error shall not be returned by a Configure Endpoint Command. This capability is enabled by the CME flag in the USBCMD register.
0	U3 Entry Capability (U3C)	This bit indicates whether the xHC Root Hub ports support port Suspend Complete notification. When this bit is 1b, PLC shall be asserted on any transition of PLS to the U3 State.

35.5.4.2 Host Controller Operational Registers

(1) USB Command Register (USB_HOST_USBCMD)

This register issues USB commands.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0020h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CEM Enable (CME)	Stopped – Short Packet Enable (SPE)	Enable U3 MFINDEX Stop (EU3S)	Enable Wrap Event (EWE)	Controller Restore State (CRS)	Controller Save State (CSS)	Light Host Controller Reset (LHCRST)	—	—	—	Host System Error Enable (HSEE)	Interrupter Enable (INTE)	Host Controller Reset (HCRST)	Run/Stop (R/S)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	R	R	RW	RW	RW	RW

Table 35.5-18 USB_HOST_USBCMD Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 14	—	Reserved
13	CEM Enable (CME)	When set to 1, a Max Exit Latency Too Large Capability Error can be returned by a Configure Endpoint Command. When cleared to 0b, a Max Exit Latency Too Large Capability Error shall not be returned by a Configure Endpoint Command. This bit is Reserved if CMC = ‘0’.
12	Stopped – Short Packet Enable (SPE)	When set to 1, the xHC can generate a Stopped Short Packet Completion Code. This bit is Reserved if SPC = ‘0’.
11	Enable U3 MFINDEX Stop (EU3S)	Default = 0. When set to 1, the xHC can stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to 0, the xHC can stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, Training, or Powered-off state. The USB3HOST does not implement this function.
10	Enable Wrap Event (EWE)	Default = 0. When set to 1, the xHC generates a MFINDEX Wrap Event every time the MFINDEX register transitions from 0_3FFFh to 0_0000h. When cleared to 0, no MFINDEX Wrap Events are generated
9	Controller Restore State (CRS)	Default = 0. When set to 1, and HCHalted (HCH) = 1, then the xHC performs a Restore State operation and restores its internal state. When set to 1 and Run/Stop (R/S) = 1 or HCHalted (HCH) = 0, or when cleared to 0, no Restore State operation is performed. This flag always returns 0 when read. Refer to the Restore State Status (RSS) flag in the USBSTS register for information on Restore State completion. Note that undefined behavior can occur if a Restore State operation is initiated while Save State Status (SSS) = 1.
8	Controller Save State (CSS)	Default = 0. When 1 is written by software and HCHalted (HCH) = 1, then the xHC saves any internal state that can be restored by a subsequent Restore State operation. When 1 is written by software and HCHalted (HCH) = 0, or 0 is written, no Save State operation is performed. This flag always returns 0 when read. Refer to the Save State Status (SSS) flag in the USBSTS register for information on Save State completion. Note that undefined behavior can occur if a Save State operation is initiated while Restore State Status (RSS) = 1.

Table 35.5-18 USB_HOST_USBCMD Register Contents (2/2)

Bit Position	Bit Name	Description
7	Light Host Controller Reset (LHCRST)	The Default = Controller Light HC Reset Capability (LHRC) bit in the HCCPARAMS1 register is formed on completion of the save state. Note that the xHC does not affect the state of the ports. When system software reads this bit, the value 0 indicates that the Light Host Controller Reset has been completed and it is safe for software to re-initialize the xHC. The value 1 indicates that the Light Host Controller Reset has not yet been completed. If not implemented, reading of this flag always returns a “0”.
6 to 4	—	Reserved
3	Host System Error Enable (HSEE)	Default = 0. When this bit is 1, and the HSE bit in the USBSTS register is 1, the xHC asserts the out-of-band error signal for the host. The signal is acknowledged by software clearing the HSE bit.
2	Interrupter Enable (INTE)	Default = 0. This bit provides system software with a means of enabling or disabling the host system interrupts generated by Interrupters. When this bit is 1, then Interrupter host system interrupt generation is allowed, e.g. the xHC issues an interrupt at the next interrupt threshold if the host system interrupt mechanism (e.g. MSI, MSI-X, etc.) is enabled. The interrupt is acknowledged by a host system interrupt specific mechanism.
1	Host Controller Reset (HCRST)	Default = 0. This control bit is used by software to reset the host controller. The effects of this bit on the xHC and the Root Hub registers are similar to those of a Chip Hardware Reset. When 1 is written to this bit by software, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial values. Any transaction currently in progress on the USB is immediately terminated. A USB reset is not driven on USB2 downstream ports, however a Hot or Warm Reset is initiated on USB3 Root Hub downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Software reinitializes the host controller in order to return the host controller to an operational state. This bit is cleared to 0 by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing 0 to this bit and does not write any xHC Operational or Runtime registers until while HCRST is 1. Note that the completion of the xHC reset process is not gated by the Root Hub port reset process. This bit is not set to 1 by software when the HCHalted (HCH) bit in the USBSTS register is 0. Attempting to reset an actively running host controller can result in undefined behavior.
0	Run/Stop (R/S)	Default = 0. 1 = Run. 0 = Stop. When set to 1, the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to 1. When this bit is cleared to 0, the xHC completes any current or queued commands or TDs, and any USB transactions associated with them, then halt. The xHC halts within 16 ms. After the Run/Stop bit is cleared by software if the above conditions have been met. The HCHalted (HCH) bit in the USBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. 1 is not written by software to this flag unless the xHC is in the Halted state (i.e. HCH in the USBSTS register is 1). Doing so can yield undefined results. Writing 0 to this flag when the xHC is in the Running state (i.e. HCH = 0) and any Event Rings are in the Event Ring Full state can result in lost events.

(2) USB Status Register (USB_HOST_USBSTS)

This register is the USB status register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0024h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	Host Controller Error (HCE)	Controller Not Ready (CNR)	Save/Restore Error (SRE)	Restore State Status (RSS)	Save State Status (SSS)	—	—	—	Port Change Detect (PCD)	Event Interrupt (EINT)	Host System Error (HSE)	—	HCHalted (HCH)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	RW1	R	R	R	R	R	RW1	RW1	RW1	R	R

Table 35.5-19 USB_HOST_USBSTS Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 13	—	Reserved
12	Host Controller Error (HCE)	Default = 0. 0 = No internal xHC error conditions exist and 1 = Internal xHC error condition. This flag shall be set to indicate detection of an internal error condition, which requires a reset and reinitialization of the xHC by software.
11	Controller Not Ready (CNR)	Default = 0. 0 = Ready and 1 = Not Ready. Doorbell or Operational register of the xHC, other than the USBSTS register, are not written by software while CNR = 0. This flag is set by the xHC after a Chip Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag remains cleared (0) until the next Chip Hardware Reset.
10	Save/Restore Error (SRE)	Default = 0. If an error occurs during a Save or Restore operation, this bit is set to 1. This bit is cleared to 0 when a Save or Restore operation is initiated or when written with 1.
9	Restore State Status (RSS)	Default = 0. When the Controller Restore State (CRS) flag in the USBCMD register is written with 1, this bit is set to 1 and remains 1 while the xHC restores its internal state. When the Restore State operation is complete, this bit is cleared to 0.
8	Save State Status (SSS)	Default = 0. When the Controller Save State (CSS) flag in the USBCMD register is written with 1, this bit is set to 1 and remains 1 while the xHC saves its internal state. When the Save State operation is complete, this bit is cleared to 0.
7 to 5	—	Reserved
4	Port Change Detect (PCD)	Default = 0. The xHC sets this bit to 1 when a bit of any port has a state transition from 0 to 1. This bit can be maintained in the Aux Power as well. Alternatively, loading this bit with the OR of all of the PORTSC change bits on a D3 to D0 transition of the xHC is also acceptable. This bit provides system software an efficient means of determining if there has been Root Hub port activity.
3	Event Interrupt (EINT)	Default = 0. The xHC sets this bit to 1 in response to a transition of the Interrupt Pending (IP) bit from any interrupt source from 0 to 1. Software that uses EINT clears it prior to clearing any IP flags. A race condition can occur if software clears the IP flags then clears the EINT flag, and another IP 0 to 1 transition occurs between these operations. In this case the new transition of the IP bit shall be lost.
2	Host System Error (HSE)	Default = 0. The xHC sets this bit to 1 when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. In a PCI system, conditions that lead to this bit being set to 1 include a PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the xHC clears the Run/Stop (R/S) bit in the USBCMD register to prevent further execution of the scheduled TDs. If the HSEE bit in the USBCMD register is 1, the xHC also asserts the out-of-band error signal to the host.
1	—	Reserved

Table 35.5-19 USB_HOST_USBSTS Register Contents (2/2)

Bit Position	Bit Name	Description
0	HCHalted (HCH)	Default = 1b. This bit is 0b whenever the Run/Stop (R/S) bit is set to 1b. The xHC sets this bit to 1b after it has stopped executing as a result of the Run/Stop (R/S) bit being cleared to 0b, either by software or by the xHC hardware (e.g. internal error). If this bit is 1b, then SOFs, microSOFs, or Isochronous Timestamp Packets (ITP) is not generated by the xHC, and any received Transaction Packet is dropped.

Note: EINT and HSE bit is cleared by writing 1b.

(3) Page Size Register (USB_HOST_PAGESIZE)

This register indicates the page size supported by the xHC implementation.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0028h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Page Size															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-20 USB_HOST_PAGESIZE Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved
15 to 0	Page Size	Default = Implementation defined. This field defines the page size supported by the xHC implementation. This xHC supports a page size of 2^(n+12) if bit n is set. For example, if bit 0 is set, the xHC supports 4-Kbyte page sizes. For a Virtual Function, this register reflects the page size selected in the System Page Size field of the SR-IOV Extended Capability structure. For the Physical Function 0, this register reflects the implementation dependent default xHC page size. Various xHC resources reference PAGESIZE to describe their minimum alignment requirements. The maximum possible page size is 128M.

(4) Device Notification Control Register (USB_HOST_DNCTRL)

This register controls the device notification.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0034h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Notification Enable															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.5-21 USB_HOST_DNCTRL Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved
15 to 0	Notification Enable	When a Notification Enable bit is set, a Device Notification Event is generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to 1 enables Device Notification Event generation if a Device Notification TP is received with its Notification Type field set to 1 (FUNCTION_WAKE), etc.

(5) Command Ring Control Low Register (USB_HOST_CRCRL)

This register contains the lower bits of the initial value of the 64-bit command ring dequeue pointer and the command ring control bits.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0038h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Command Ring Pointer Low															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Command Ring Pointer Low										—	—	Command Ring Running (CRR)	Command Abort (CA)	Command Stop (CS)	Ring Cycle State (RCS)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	RW1	RW1	RW

Table 35.5-22 USB_HOST_CRCRL Register Contents

Bit Position	Bit Name	Description
31 to 6	Command Ring Pointer Low	Default = 0. This field defines lower-order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Writing to this field is ignored when Command Ring Running (CRR) = 1. In writing to the CRCR (combination of CRCRL and CRCRH) while the Command Ring is stopped (CRR = 0), the value of this field is used to fetch the first Command TRB the next time writing to the Host Controller Doorbell register proceeds with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CRR = 0), then the Command Ring begins fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns 0.
5, 4	—	Reserved
3	Command Ring Running (CRR)	Default = 0. This flag is set to 1 if the Run/Stop (R/S) bit is 1 and the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. It is cleared to 0 when the Command Ring is “stopped” after writing 1 to the Command Stop (CS) or Command Abort (CA) flags, or if the R/S bit is cleared to 0.
2	Command Abort (CA)	Default = 0. Writing a 1 to this bit immediately terminates the command currently being executed, stops the Command Ring, and generates a Command Completion Event with the Completion Code set to Command Ring Stopped. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writing to this flag is ignored by the xHC if Command Ring Running (CRR) = 0. Reading this bit always returns 0.
1	Command Stop (CS)	Default = 0. Writing a 1 to this bit stops the operation of the Command Ring after completion of the command currently being executed, and generates a Command Completion Event with the Completion Code set to Command Ring Stopped and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writing to this flag is ignored by the xHC if Command Ring Running (CRR) = 0. Reading this bit always returns 0.
0	Ring Cycle State (RCS)	This bit identifies the value of the xHC Consumer Cycle State (CCS) flag for the TRB referenced by the Command Ring Pointer. Writing to this flag is ignored if Command Ring Running (CRR) is 1. In case of writing to the CRCR while the Command Ring is stopped (CRR = 0), the value of this flag is used to fetch the first Command TRB the next time writing to the Host Controller Doorbell register proceeds with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CRR = 0), then the Command Ring begins fetching Command TRBs using the current value of the internal Command Ring CCS flag. Reading this flag always returns 0.

(6) Command Ring Control High Register (USB_HOST_CRCRH)

This register defines higher-order bits of the initial value of the 64-bit Command Ring Dequeue Pointer.

Access Size: 32 bits

Address(es): <USB_S0_base> + 003Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Command Ring Pointer High															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Command Ring Pointer High															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.5-23 USB_HOST_CRCRH Register Contents

Bit Position	Bit Name	Description
31 to 0	Command Ring Pointer High	Default = 0. This field defines higher-order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Writing to this field is ignored when Command Ring Running (CRR) = 1. In case of writing to the CRCR while the Command Ring is stopped (CRR = 0), the value of this field is used to fetch the first Command TRB the next time writing to the Host Controller Doorbell register proceeds with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CRR = 0) then the Command Ring begins fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns 0.

(7) Device Context Base Address Array Pointer Low Register (USB_HOST_DCBAAPL)

This register defines lower-order bits of the 64-bit base address of the Device Context Pointer Array.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0050h

Initial Value: 0000_0000h

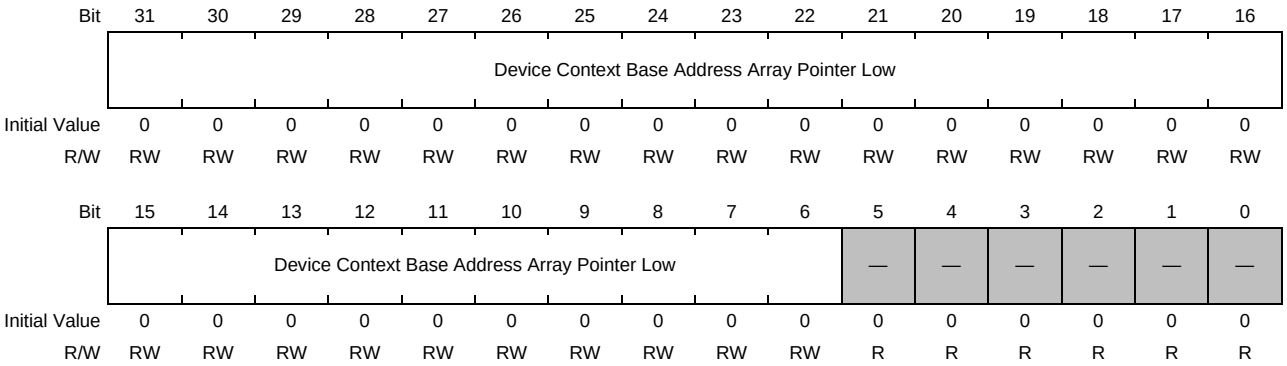


Table 35.5-24 USB_HOST_DCBAAPL Register Contents

Bit Position	Bit Name	Description
31 to 6	Device Context Base Address Array Pointer Low	This field defines lower-order bits of the 64-bit base address of the Device Context Pointer Array. A table of address pointers that reference Device Context structures for the devices is attached to the host.
5 to 0	—	Reserved

(8) Device Context Base Address Array Pointer High Register (USB_HOST_DCBAAPH)

This register defines higher-order bits of the 64-bit base address of the Device Context Pointer Array.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0054h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Device Context Base Address Array Pointer High															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Device Context Base Address Array Pointer High															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.5-25 USB_HOST_DCBAAPH Register Contents

Bit Position	Bit Name	Description
31 to 0	Device Context Base Address Array Pointer Low	This field defines higher-order bits of the 64-bit base address of the Device Context Pointer Array. A table of address pointers that reference Device Context structures for the devices are attached to the host.

(9) Configure Register (USB_HOST_CONFIG)

This register configures USB3HOST.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0058h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Configuration Information Enable (CIE)	U3 Entry Enable (U3E)	Max Device Slots Enabled (MaxSlotsEn)							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.5-26 USB_HOST_CONFIG Register Contents

Bit Position	Bit Name	Description
31 to 10	—	Reserved
9	Configuration Information Enable (CIE)	When set to 1, the software shall initialize the Configuration Value, Interface Number, and Alternate Setting fields in the Input Control Context when it is associated with a Configure Endpoint Command. When this bit is 0b, the extended Input Control Context fields are not supported.
8	U3 Entry Enable (U3E)	When set to 1, the xHC shall assert the PLC flag (1b) when a Root Hub port transitions to the U3 State.
7 to 0	Max Device Slots Enabled (MaxSlotsEn)	Default = 0. This field specifies the maximum number of enabled Device Slots. Valid values are in the range of 0 to MaxSlots. Enabled Devices Slots are allocated contiguously. E.g.) A value of 16 specifies that Device Slots 1 to 16 are active. A value of 0 disables all Device Slots. A disabled Device Slot shall not respond to Doorbell Register references. This field shall not be modified by software if the xHC is running (Run/Stop (R/S) = ‘1’).

35.5.4.3 Port Register Sets in Host Controller Operational Registers

(1) U3P1 Port Status and Control Register (USB_HOST_U3P1PORTSC)

This register contains the USB 3.1 port status and control bits.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0420h

Initial Value: 0000_02A0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Warm Port Reset (WPR)	Device Removable (DR)	—	—	Wake on Over-current Enable (WOE)	Wake on Disconnect Enable (WDE)	Wake on Connect Enable (WCE)	Cold Attach Status (CAS)	Port Config Error Change (CEC)	Port Link State Change (PLC)	Port Reset Change (PRC)	Over-current Change (OCC)	Warm Port Reset Change (WRC)	Port Enable/ Disable Change (PEC)	Connect Status Change (CSC)	Port Link State Write Strobe (LWS)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	R	R	R	RW	RW	RW	R	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Port Indicator Control (PIC)		Port Speed				Port Power (PP)	Port Link State (PLS)				Port Reset (PR)	Over-current Active (OCA)	—	Port Enable/ Disable (PED)	Current Connect Status (CCS)
Initial Value	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
R/W	RW	RW	R	R	R	R	RW	RW	RW	RW	RW	RW1	R	R	RW1	R

Table 35.5-27 USB_HOST_U3P1PORTSC Register Contents (1/4)

Bit Position	Bit Name	Description
31	Warm Port Reset (WPR)	Writing 1: Starts Warm Reset sequence, and sets the PR bit to 1.
30	Device Removable (DR)	1b: A device connected to this Port is non-removable. 0b: A device connected to this Port is removable.
29, 28	—	Reserved. The write value should always be 0b.
27	Wake on Over-current Enable (WOE)	Writing 1b: Enables over-current condition as System Wake-up Event The USB3HOST can write this bit in the case of both ”PED = 1” and “PED = 0”
26	Wake on Disconnect Enable (WDE)	Writing 1b: Enables device disconnection as System Wake-up Event The USB3HOST can write this bit in the case of both “PED = 1” and “PED = 0”.
25	Wake on Connect Enable (WCE)	Writing 1b: Enables device connection as System Wake-up Event The USB3HOST can write this bit in the case of both “PED = 1” and “PED = 0”.
24	Cold Attach Status (CAS)	1b: Far-end Receiver Termination is detected but Port Status cannot transition to Enabled State. This bit is fixed to “0” in the USB3HOST.
23	Port Config Error Change (CEC)	This bit is set when configuration with Link Partner fails.
22	Port Link State Change (PLC)	0b: No Change 1b: Link state is changed. This bit is set in the case of below Link transitions. • U3 -> Resume • Resume -> Recovery -> U0 • U3 -> Recovery ->U0 • Any state -> Inactive • (In the case of U3E = 1) Any state -> U3 When 1 is written by software, the bit is cleared

Table 35.5-27 USB_HOST_U3P1PORTSC Register Contents (2/4)

Bit Position	Bit Name	Description
21	Port Reset Change (PRC)	This bit is set when Port reset process completes. (Port Reset changes from 1 to 0) But if Port reset process is finished in below cases, this bit is not set to “1”. • When SW sets PP bit to “0” • When SW sets PED bit to “1” • When the Over Current is occurred 0b: No Change 1b: Reset is complete. Writing 1 by software clears this bit. When 1 is written by software, this bit is cleared.
20	Over-current Change (OCC)	When Over-current Active changes from “0” to “1”, this bit is set to 1. When 1 is written by software, this bit is cleared.
19	Warm Port Reset Change (WRC)	This bit is set to 1 when a Warm Reset is completed
18	Port Enable/Disable Change (PEC)	0b: No Change 1b: Port enabled/disabled status has changed. This bit for a port is set when the port is a USB2 protocol port and is disabled due to exit under the appropriate conditions at the EOF2 point. When 1 is written by software, this bit is cleared. If Port Power is 0, this bit is set to 0. U3P[m]PORTSC.PEC is fixed to “0”.
17	Connect Status Change (CSC)	0b: No Change 1b: Change in Current Connect Status The xHC sets this bit to 1 at change of port device connection status. When 1 is written by software, this bit is cleared. If Port Power is 0, this bit is set to 0.
16	Port Link State Write Strobe (LWS)	Writing 1b: Writing to PLS field is enabled. 0b: Writing to PLS field is ignored. The read value is 0
15, 14	Port Indicator Control (PIC)	If Port Indicator (PIND) bit in HCCPRAMS1 Register is 0, writing to this field has no effect. If the Port Indicator (PIND) bit is 1b: 00b: Port indicators are off 01b: Amber 10b: Green 11b: Undefined If Port Power is 0, this field is set to 0.
13 to 10	Port Speed	Speed type of USB device connected to the port. This is enabled only when a device is connected to the port. (Current Connect Status is 1) After a port reset, this field indicates the speed of the device connected to the port. If the reset or speed detection fails, this field indicates an unknown speed. When the Current Connect Status changes from 0 to 1, this field indicates an undefined speed. 0000b: Undefined speed (before speed detection) 0001b to 0011b: Reserved 0100b: SuperSpeed device is attached. 0101b: SuperSpeed Plus device is attached. 0110b to 1111b: Reserved
9	Port Power (PP)	This field reflects a port’s logical power state. 0b: This port is in the Powered-off state. 1b: This port is not in the Powered-off state. When the Port Power Control (PPC) bit in the HCCPARAMS1 Register is 1, the xHC has a port power control switch and this bit shows the current state of the switch. (0: off, 1: on) When the Port Power Control (PPC) bit in the HCCPARAMS1 Register is set to “0”, the xHC has no port power control switch and each port is hard wired to power and not affected by this bit. If an over-current condition is detected at a powered port, the PP bit of each port is changed from 1 to 0. After modifying PP, software shall read PP and confirm that it is reached its target state before modifying it again (page 312 of the xHCI specification). PP flag can be delayed in reflecting this change, (Ex) due to waiting for a port related state machine to complete reset signaling or other operation. (page 315 of the xHCI specification)

Table 35.5-27 USB_HOST_U3P1PORTSC Register Contents (3/4)

Bit Position	Bit Name	Description
8 to 5	Port Link State (PLS)	This field is used for port power management and shows the Current Link state. When the PED is 1, System software sets this bit then sets Link U state. Port Link State is not set to Disabled, RxDetect, or Inactive State. 0000b: The link makes a transition to the U0 state from any U state. 0001b: Ignored. 0010b: Ignored. 0011b: The link makes a transition to the U0 state from any U state. 0100b: Ignored. 0101b: When PLS is set to the Disabled and PP is set to “1”, the link makes a transition to the Disconnected. 0110b to 1001b: Ignored. 1010b: The link makes a transition to the Compliance mode. 1011b to 1111b: Ignored. To write to this field, the Port Link State Write strobe should be 1. Software reads this field to determine the success or failure of a transition to the U2 state. Write 0: Deasserts L1 signal. Write 1: No influence 0000b: Link is in the U0 State 0001b: Link is in the U1 State 0010b: Link is in the U2 State 0011b: Link is in the U3 State (Device Suspended) 0100b: Link is in the Disabled State 0101b: Link is in the RxDetect State 0110b: Link is in the Inactive State 0111b: Link is in the Polling State 1000b: Link is in the Recovery State 1001b: Link is in the Hot Reset State 1010b: Link is in the Compliance Mode State 1011b: Link is in the Test State 1100 to 1110b: Reserved 1111b: Link is in the Resume State If Port Power is 0, this field is undefined. Transitions between different states are not reflected until the transition is complete. (page 311 of the xHCI specification)
4	Port Reset (PR)	0b: Port is not being reset. 1b: Port reset signal is being asserted. When software sets this bit from 0 to 1, the bus reset sequence is started. This bit remains set to 1 until a reset by root hub is completed. When an error is detected during resetting, Port Speed field indicates an undefined speed. If Port Power is 0, this field is set to 0.
3	Over-current Active (OCA)	0b: Not over-current condition 1b: Over-current condition When an over-current condition is removed, this bit changes from 1 to 0 automatically
2	—	Reserved. The write value should always be 0b.
1	Port Enable/Disable (PED)	0b: Disabled 1b: Enabled After detecting a connection at a port, if SS port initialization or reset by the system software is successful, this bit is automatically enabled by the xHC. The Port is disabled by fault condition (disconnection event or other fault condition), or USB System Software. The bit status does not change until port status changes. If Port Power is 0, this field is set to 0.

Table 35.5-27 USB_HOST_U3P1PORTSC Register Contents (4/4)

Bit Position	Bit Name	Description
0	Current Connect Status (CCS)	0b: No device is present 1b: A device is present on port. Reflects current port status. If Port Power is 0, this field is set to 0.

(2) U3P1 Port Power Management Status and Control Register (USB_HOST_U3P1PORTPMSC)

This register contains the USB 3.1 port power management status and control bits.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0424h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Force Link PM Accept (FLA)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	U2 Timeout								U1 Timeout							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.5-28 USB_HOST_U3P1PORTPMSC Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved
16	Force Link PM Accept (FLA)	0b -> 1b: St Link Function LMP with FLA = 1 is generated. 1b -> 0b: Set Link Function LMP with FLA = 0 is generated. This bit is set to 0 when PR changes from “0” to “1” or CCS changes from “0” to “1”. While PP is set to “0”, writing action to this bit is ignored.
15 to 8	U2 Timeout	U2 inactivity timer Timeout value If FFh, a port is in the U2 entry disabled state. When PR bit is changed from “0” to “1”, this bit is initialized. 00h: Zero (default) 01h: 256 µs 02h: 512 µs | FEh: 65.024 ms FFh: Infinite
7 to 0	U1 Timeout	U1 inactivity timer Timeout value If FFh, port is in the U1 entry disabled state. When PR bit is changed from “0” to “1”, this bit is initialized. 00h: Zero (default) 01h: 1 µs 02h: 2 µs | 7Fh: 127 µs 80h to FEh: Reserved FFh: Infinite

(3) U3P1 Port Link Info Register (USB_HOST_U3P1PORTLI)

This register indicates the USB 3.1 port link information.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0428h

Initial Value: 0000_0000h

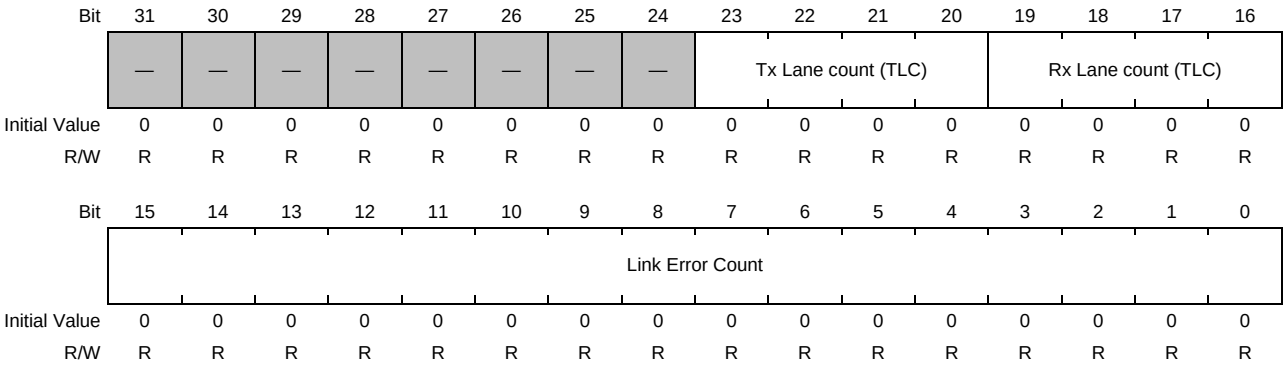


Table 35.5-29 USB_HOST_U3P1PORTLI Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved
23 to 20	Tx Lane count (TLC)	This field that identifies the number of Transmit Lanes negotiated by the port. This is a “zero-based” value, where 0 to 15 represents Lane Counts of 1 to 16, respectively. This value is valid only when CCS = ‘1’. TLC shall equal ‘0’ for a simplex Sublink. This core’s value is fixed to “0h”.
19 to 16	Rx Lane Count (RLC)	This field that identifies the number of Receive Lanes negotiated by the port. This is a “zero-based” value, where 0 to 15 represents Lane Counts of 1 to 16, respectively. This value is valid only when CCS = ‘1’. RLC shall equal ‘0’ for a simplex Sublink. This core’s value is fixed to “0h”.
15 to 0	Link Error Count	This field returns the number of link errors detected by the port. This value shall be reset to ‘0’ by the assertion of a Chip Hardware Reset, HCRST, when PR transitions from ‘1’ to ‘0’, or when CCS = transitions from ‘0’ to ‘1’.

(4) U3P1 Port Hardware LPM Control Register (USB_HOST_U3P1PORTHLPMC)

This register reserved for USB 3.1. the Hardware LPM Control Register is used for USB 2.0 (**Section 35.5.4.3(8)**).

Access Size: 32 bits

Address(es): <USB_S0_base> + 042Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-30 USB_HOST_U3P1PORTHLPMC Register Contents

Bit Position	Bit Name	Description
31 to 0	—	Reserved

(5) U2P1 Port Status and Control Register (USB_HOST_U2P1PORTSC)

This register contains the USB 2.0 port status and control bits.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0430h

Initial Value: 0000_02A0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	Device Removable (DR)	—	—	Wake on Over-current Enable (WOE)	Wake on Disconnect Enable (WDE)	Wake on Connect Enable (WCE)	Cold Attach Status (CAS)	—	Port Link State Change (PLC)	Port Reset Change (PRC)	Over-current Change (OCC)	—	Port Enable/ Disable Change (PEC)	Connect Status Change (CSC)	Port Link State Write Strobe (LWS)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	R	R	RW1	RW1	RW1	R	RW1	RW1	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Port Indicator Control (PIC)		Port Speed				Port Power (PP)	Port Link State (PLS)				Port Reset (PR)	Over-current Active (OCA)	—	Port Enable/ Disable (PED)	Current Connect Status (CCS)
Initial Value	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
R/W	RW	RW	R	R	R	R	RW	RW	RW	RW	RW	RW1	R	R	RW1	R

Table 35.5-31 USB_HOST_U2P1PORTSC Register Contents (1/3)

Bit Position	Bit Name	Description
31	—	Reserved. The write value should always be 0b.
30	Device Removable (DR)	1b: A device connected to this Port is non-removable. 0b: A device connected to this Port is removable. In the USB3HOST, this bit is fixed to 0 to indicate that all USB2.0 ports are removable.
29, 28	—	Reserved. The write value should always be 0b.
27	Wake on Over-current Enable (WOE)	Write 1: Enables over-current condition as System Wake-up Event The USB3HOST can write this bit in the case of both “PED = 1” and “PED = 0”.
26	Wake on Disconnect Enable (WDE)	Write 1: Enables device disconnection as System Wake-up Event The USB3HOST can write this bit in the case of both “PED = 1” and “PED = 0”.
25	Wake on Connect Enable (WCE)	Write 1: Enables device connection as System Wake-up Event The USB3HOST can write this bit in the case of both “PED = 1” and “PED = 0”.
24	Cold Attach Status (CAS)	This bit is fixed to 0 for USB2 protocol ports.
23	—	Reserved. The write value should always be 0b.
22	Port Link State Change (PLC)	0b: No Change 1b: Port Link State has changed. This flag is set to 1 due to the following PLS transitions: Table 35.5-31-1 PLS transition Transition / Condition: U3 -> Resume: Wakeup signal from a device Resume -> U0: Host/Device Remote Resume complete U2 -> U0: L1 Resume complete U0 -> U0: L1 Entry Reject When 1 is written by software, the bit is cleared

Table 35.5-31 USB_HOST_U2P1PORTSC Register Contents (2/3)

Bit Position	Bit Name	Description
21	Port Reset Change (PRC)	This bit is set when Port reset process completes. (Port Reset changes from 1 to 0) 0b: No Change 1b: Reset is complete. When 1 is written by software, the bit is cleared
20	Over-current Change (OCC)	When Over-current Active changes, this bit is set to 1. When 1 is written by software, the bit is cleared.
19	—	Reserved. The write value should always be 0b.
18	Port Enable/Disable Change (PEC)	0b: No Change 1b: Port enabled/disabled has changed. This bit for a port is set when the port is a USB2 protocol port and is disabled due to exit under the appropriate conditions at the EOF2 point. When 1 is written by software, the bit is cleared. *Note*: This flag is not set if the PED transition was due to software setting PP to “0”.
17	Connect Status Change (CSC)	0b: No Change 1b: Change in Current Connect Status The xHC sets this bit to 1 at change of CCS-bit’s status. When 1 is written by software, the bit is cleared. *Note*: This flag shall not be set if the CCS transition was due to software setting PP to ‘0’.
16	Port Link State Write Strobe (LWS)	1b: Writing to PLS field is enabled. 0b: Writing to PLS field is ignored. The read value is 0
15, 14	Port Indicator Control (PIC)	If Port Indicator (PIND) bit in HCCPRAMS1 Register is 0, writing to this field has no effect. If the Port Indicator (PIND) bit is 1: 00b: Port indicators are off 01b: Amber 10b: Green 11b: Undefined In the USB3HOST, this bit is fixed to 0.
13 to 10	Port Speed	Speed type of USB device connected to the port. This is enabled only when a device is connected to the port (Current Connect Status is 1). After a port reset, this field indicates the speed of the device connected to the port. If the reset or speed detection fails, this field indicates an unknown speed. When the Current Connect Status changes from 0 to 1, this field indicates an undefined speed. 0000b: Undefined speed (before speed detection) 0001b: Full-speed device attached 0010b: Low-speed device attached 0011b: High-speed device attached 0100b to 1111b: Reserved
9	Port Power (PP)	This field reflects a port’s logical power state. 0b : This port is in the Powered-off state. 1b : This port is not in the Powered-off state. When the Port Power Control (PPC) bit in the HCCPARAMS1 Register is 1, the xHC has a port power control switch and this bit shows the current state of the switch. (0: off, 1: on) When the Port Power Control (PPC) bit in the HCCPARAMS1 Register is set to “0”, the xHC has no port power control switch and each port is hard wired to power and not affected by this bit. An over-current condition is detected at a powered port, the PP bit of each port is changed from 1 to 0. After the HC reset releases, this bit is set from 0 to 1 automatically. This bit is set to 1 when in the Compliance Test Mode.

Table 35.5-31 USB_HOST_U2P1PORTSC Register Contents (3/3)

Bit Position	Bit Name	Description
8 to 5	Port Link State (PLS)	This field is used for port power management and shows the Current Link state. When the PED is 1, System software sets this bit then sets Link U state. Port Link State is not set to Disabled, RxDetect, or Inactive State. Write 0000b: The link makes a transition to the U0 state from any U state. Write 0001b: Ignored. Write 0010b: Requests LPM and asserting L1 signal on the USB2 bus. The link should enter U2 state if device response ACK. Write 0011b: The link makes a transition to the U3 state from any U state. Write 0100b to 1110b: Ignored. Write 1111b: xHC initial resume when port in U3 state. Writing to this field sets the Port Link State Write strobe 1. For USB2 Protocol port, writing 2 requests LPM. Software reads this field to determine success/failure of transition to U2 state. Write 0b: Deasserts L1 signal Write 1b: No influenc Read 0000b: Link is in the Enabled / WLPM State Read 0001b: Reserved Read 0010b: Link is in the L1Suspend State Read 0011b: Link is in the Suspended State Read 0100b: Link is in the Powered-off State Read 0101b: Link is in the Disconnected State Read 0110b: Reserved Read 0111b: Link is in the Disabled State Read 1000b: Reserved Read 1001b: Link is in the Hot Reset State Read 1010b: Reserved Read 1011b: Link is in the Test Mode State Read 1100b to 1110b: Reserved Read 1111b: Link is in the Resuming / L1Resuming / SendEOR State If Port Power is set to “0”, this field is undefined.
4	Port Reset (PR)	0b: port is not in reset 1b: port reset assertion When this bit is set from 0 to 1 by software, the bus reset sequence is started. This bit remains to be set to 1 until a reset by root hub is completed. When an error is detected during resetting, Port Speed field indicates an undefined speed. If Port Power is 0, this field is set to 0.
3	Over-current Active (OCA)	0b: Over-current condition 1b: Not over-current condition When an over-current condition is removed, this bit changes from 1 to 0 automatically.
2	—	Reserved. The write value should always be 0b.
1	Port Enable/ Disable (PED)	0b: Disable 1b: Enable This bit is set to 1 when the USB2.0 port enters U0 state. If Port Power is 0, this field is set to 0.
0	Current Connect Status (CCS)	0b: No device is present. 1b: A device is present on port. Reflects current port status. If Port Power is 0, this field is set to 0.

(6) U2P1 Port Power Management Status and Control Register (USB_HOST_U2P1PORTPMSC)

This register contains the USB 2.0 port power management status and control bits.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0434h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Port Test Control (Test Mode)				—	—	—	—	—	—	—	—	—	—	—	Hardware LPM Enable (HLE)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	R	R	R	R	R	R	R	R	R	R	R	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	L1 device Slot								Best Effort Service Latency (BESL)				Remote Wake Enable (RWE)	L1 Status (L1S)		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R

Table 35.5-32 USB_HOST_U2P1PORTPMSC Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 28	Port Test Control (Test Mode)	When this field is ‘0’, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Powered-Off state (PLS = Disabled). If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. Refer to section 4.19.6 of xHCI 1.1 specification for the operational model for using these test modes. The encoding of the Test Mode bits for a USB2 protocol port are : 0000b: Test mode not enabled 0001b: Test J_STATE 0010b: Test K_STATE 0011b: Test SE0_NAK 0100b: Test Packet 0101b: Test FORCE_ENABLE 0110b to 1110b: Reserved 1111b: Port Test Control Error Refer to the sections 7.1.20 and 11.24.2.13 of the USB2 spec for more information on Test Modes.
27 to 17	—	Reserved
16	Hardware LPM Enable (HLE)	If this bit is set to ‘1’, then hardware controlled LPM shall be enabled for this port. Refer to section 4.23.5.1.1.1 of xHCI 1.1 specification. If the USB2 Hardware LPM Capability is not supported (HLC = ‘0’) this field shall be RsvdZ. Note the BESL LMP Capability support (i.e. HLE = ‘1’ and BLC = ‘1’) shall be mandatory for all xHCI 1.1 compliant xHCs.
15 to 8	L1 device Slot	System software sets this field to indicate the ID of the Device Slot associated with the device directly attached to the Root Hub port. A value of ‘0’ indicates no device is present. The xHC uses this field to lookup information necessary to generate the LPM Token packet.
7 to 4	Best Effort Service Latency (BESL)	System software sets this field to indicate to the recipient device how long the xHC will drive resume if it (the xHC) initiates an exit from L1. The BESL value encoding is defined in Table 13 of xHCI 1.1 specification. *Note*: That the BESL field is used by both software and hardware controlled LPM. Refer to section 4.23.5.1.1 of xHCI 1.1 for more information on BESL use. Refer to section 5.2.5 of xHCI 1.1 for information on how DBESL can be used to establish an initial value for BESL.

Table 35.5-32 USB_HOST_U2P1PORTPMSC Register Contents (2/2)

Bit Position	Bit Name	Description
3	Remote Wake Enable (RWE)	System software sets this flag to enable or disable the device for remote wake from L1. The value of this flag shall temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9.
2 to 0	L1 Status (L1S)	This field is used by software to determine whether an L1-based suspend request (LPM transaction) was successful, specifically: 000b: Invalid – This field shall be ignored by software. 001b: Success – Port successfully transitioned to L1 (ACK) 010b: Not Yet – Device is unable to enter L1 at this time (NYET) 011b: Not Supported – Device does not support L1 transitions (STALL) 100b: Timeout/Error – Device failed to respond to the LPM Transaction or an error occurred 101b to 111b: Reserved The value of this field is only valid when the port resides in the L0 or L1 state (PLS = ‘0’ or ‘2’). Refer to section 4.23.5.1.1 of xHCI 1.1 for more information.

(7) U2P1 Port Link Info Register (USB_HOST_U2P1PORTLI)

This register reserved for USB 2.0. the Port Link Info Register is used for USB 3.1 (**Section 35.5.4.3(3)**).

Access Size: 32 bits

Address(es): <USB_S0_base> + 0438h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-33 USB_HOST_U2P1PORTLI Register Contents

Bit Position	Bit Name	Description
31 to 0	—	Reserved

(8) U2P1 Port Hardware LPM Power Control Register (USB_HOST_U2P1PORTHLPMC)

This register control USB 2.0 port Hardware LPM Power.

Access Size: 32 bits

Address(es): <USB_S0_base> + 043Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	Best Effort Service Latency Deep (BESLD)				L1 Timeout								Host Initiated Resume Duration Mode (HIRDM)	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.5-34 USB_HOST_U2P1PORTHLPMC Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved
13 to 10	Best Effort Service Latency Deep (BESLD)	System software sets this field to indicate to the recipient device how long the xHC will drive resume on an exit from U2. Refer to section 4.23.5.1.1.1 of xHCI 1.1 for more information on BESLD use. The BESLD value encoding is defined in Table 13 of xHCI 1.1. Refer to section 5.2.6 of xHCI 1.1 for information on how DBESLD can be used to establish an initial value for BESLD.
9 to 2	L1 Timeout	Timeout value for the L1 inactivity timer (LPM Timer). This field shall be set to 00h by the assertion of PR to '1'. Refer to section 4.23.5.1.1.1 of xHCI 1.1 for more information on L1 Timeout operation. The following are permissible values: 00h: 128 µs (default) 01h: 256 µs 02h: 512 µs 03h: 768 µs | FFh: 65.280 ms
1, 0	Host Initiated Resume Duration Mode (HIRDM)	Indicates which HIRD value should be used. The following are permissible values: 00b: Initiate L1 using BESL only on timeout. (default) 01b: Initiate L1 using BESLD on timeout. If rejected by device, initiate L1 using BESL. 10b to 11b: Reserved

35.5.4.4 xHCI Extended Capabilities

(1) USB Legacy Supported Protocol Capability

(a) USB Legacy Support Capability Register (USB_HOST_USBLEGSUP)

USB legacy support capability register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0500h

Initial Value: 0000_0401h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	HC OS Owned Semaphore (HOOS)	—	—	—	—	—	—	—	HC BIOS Owned Semaphore (HBOS)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	R	R	R	R	R	R	R	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability ID							
Initial Value	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-35 USB_HOST_USBLEGSUP Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved
24	HC OS Owned Semaphore (HOOS)	System software sets this bit to request ownership of the xHC. Ownership is obtained when this bit is reads as 1 and the HC BIOS Owned Semaphore bit is reads as 0.
23 to 17	—	Reserved. These bits are read as 0b. Writing is invalid.
16	HC BIOS Owned Semaphore (HBOS)	The BIOS sets this bit to establish ownership of the xHC. System BIOS will set this bit to a 0 in response to a request for ownership of the xHC by system software.
15 to 8	Next Capability Pointer	This field indicates the location of the next capability relative to the effective address of the current capability.
7 to 0	Capability ID	Legacy Support

(b) USB Legacy Support Control and Status Register (USB_HOST_USBLEGCTLSTS)

USB legacy support control and status register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0504h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SMI on BAR (SBA)	SMI on PCI Command (SPC)	SMI on OS Ownership Change (SOOC)	—	—	—	—	—	—	—	—	SMI on Host System Error (SHSE)	—	—	—	SMI on Event Interrupt (SEI)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W1	R/W1	R/W1	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SMI on BAR Enable (SBAE)	SMI on PCI Command Enable (SPCE)	SMI on OS Ownership Enable (SOOE)	—	—	—	—	—	—	—	—	SMI on Host System Error Enable (SHSEE)	—	—	—	USB SMI Enable (USE)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	R	R	R	R	R	R	R	R	RW	R	R	R	RW

Table 35.5-36 USB_HOST_USBLEGCTLSTS Register Contents (1/2)

Bit Position	Bit Name	Description
31	SMI on BAR (SBA)	This bit is set to 1 whenever the Base Address Register (BAR) is written. This bit is fixed to 0b, because the USB3HOST does not have the Base Address Register.
30	SMI on PCI Command (SPC)	This bit is set to 1 whenever the PCI Command Register is written. This bit is fixed to 0b, because the USB3HOST does not have the PCI Command Register.
29	SMI on OS Ownership Change (SOOC)	This bit is set to 1 whenever the HC OS Owned Semaphore bit in the USBLEGSUP register transitions from 1 to a 0 or 0 to a 1.
28 to 21	—	Reserved
20	SMI on Host System Error (SHSE)	Shadow bit of the Host System Error (HSE) bit in the USBSTS register.
19 to 17	—	Reserved. These bits are read as 0b. Writing is invalid.
16	SMI on Event Interrupt (SEI)	Shadow bit of Event Interrupt (EINT) bit in the USBSTS register.
15	SMI on BAR Enable (SBAE)	When this bit is 1 and SMI on BAR is 1, then the host controller will issue an SMI.
14	SMI on PCI Command Enable (SPCE)	When this bit is 1 and SMI on PCI Command is 1, then the host controller will issue an SMI.
13	SMI on OS Ownership Enable (SOOE)	When this bit is 1 and the OS Ownership Change bit is 1, the host controller will issue an SMI
12 to 5	—	Reserved
4	SMI on Host System Error Enable (SHSEE)	When this bit is 1 and the SMI on Host System Error bit (below) in this register is 1, the host controller will issue an SMI immediately.
3 to 1	—	Reserved

Table 35.5-36 USB_HOST_USBLEGCTLSTS Register Contents (2/2)

Bit Position	Bit Name	Description
0	USB SMI Enable (USE)	When this bit is 1 and the SMI on Event Interrupt bit in this register is 1, the host controller will issue an SMI immediately.

(2) xHCI Supported Protocol Capability for USB3.1

(a) Offset 00h - xHCI Supported Protocol Capability Field Definitions (USB3.1) Register (USB_HOST_U3HCSPC1)

xHCI supported protocol capability field definitions (USB3.1) register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0510h

Initial Value: 0301_0802h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Major Revision								Minor Revision							
Initial Value	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability ID							
Initial Value	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-37 USB_HOST_U3HCSPC1 Register Contents

Bit Position	Bit Name	Description
31 to 24	Major Revision	Major Specification Release Number in Binary-Coded Decimal (i.e., version 3.x is 03h). This field identifies the major release number component of the specification with which the xHC is compliant.
23 to 16	Minor Revision	Minor Specification Release Number in Binary-Coded Decimal (i.e., version x.10 is 10h). This field identifies the minor release number component of the specification with which the xHC is compliant.
15 to 8	Next Capability Pointer	This field indicates the location of the next capability with relative to the effective address of the current capability.
7 to 0	Capability ID	xHCI Supported Protocol

(b) Offset 04h - xHCI Supported Protocol Capability Field Definitions (USB3.1) Register (USB_HOST_U3HCSPC2)

xHCI supported protocol capability field definitions (USB3.1) register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0514h

Initial Value: 2042_5355h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Name String															
Initial Value	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Name String															
Initial Value	0	1	0	1	0	0	1	1	0	1	0	1	0	1	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-38 USB_HOST_U3HCSPC2 Register Contents

Bit Position	Bit Name	Description
31 to 0	Name String	This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters can be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive

(c) Offset 08h - xHCI Supported Protocol Capability Field Definitions (USB3.1) Register (USB_HOST_U3HCSPC3)

xHCI supported protocol capability field definitions (USB3.1) register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0518h

Initial Value: 0000_0101h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Protocol Speed ID Count (PSIC)				Hub Depth (MHD)			—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Compatible Port Count								Compatible Port Offset							
Initial Value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-39 USB_HOST_U3HCSPC3 Register Contents

Bit Position	Bit Name	Description
31 to 28	Protocol Speed ID Count (PSIC)	This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains. If this field is non-zero, then all speeds supported by the protocol shall be defined using PSI Dwords, i.e. no implied Speed ID mappings apply. PSIC value of 0 implies that only the default SuperSpeed bit rate is supported
27 to 25	Hub Depth (MHD)	If this field is ‘0’, then the standard USB2 hub depth constraints apply, if this field is > ‘0’, then it indicates the maximum hub depth supported by the USB2 ports. This bit is fixed to 0h in the USB3HOST.
24 to 16	—	Reserved
15 to 8	Compatible Port Count	This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts
7 to 0	Compatible Port Offset	This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are 1 to MaxPorts.

(d) Offset 0Ch - xHCI Supported Protocol Capability Field Definitions (USB3.1) Register (USB_HOST_U3HCSPC4)

xHCI supported protocol capability field definitions (USB3.1) register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 051Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	Protocol Slot Type				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-40 USB_HOST_U3HCSPC4 Register Contents

Bit Position	Bit Name	Description
31 to 5	—	Reserved
4 to 0	Protocol Slot Type	This field specifies the Slot Type value which can specified when allocating Device Slots that support this protocol. Valid values are 0 to 31.

(e) Protocol Speed ID for SS Register (USB_HOST_PSISS)

Protocol speed ID for ss register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0520h

Initial Value: 0005_0134h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Protocol Speed ID Mantissa (PSIM)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PSI Full-duplex (PFD)	PSI Type (PLT)		Protocol Speed ID Exponent (PSIE)		Protocol Speed ID Value (PSIV)			
Initial Value	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-41 USB_HOST_PSISS Register Contents

Bit Position	Bit Name	Description
31 to 16	Protocol Speed ID Mantissa (PSIM)	This field defines the mantissa that is applied to the PSIE when calculating the maximum bit rate represented by this PSI Dword.
15 to 9	—	Reserved
8	PSI Full-duplex (PFD)	If this bit is 1, the link is full-duplex, and if 0, the link is half-duplex.
7, 6	PSI Type (PLT)	This field identifies whether the PSI Dword defines a symmetric or asymmetric bit rate, and if asymmetric, then this field also indicates if this Dword defines the receive or transmit bit rate. Note that the Asymmetric PSI Dwords shall be paired, i.e. an Rx immediately followed by a Tx, and both Dwords shall define the same value for the PSIV. Table 35.5-41-1

RLT Value	Bit Rate	Note
0	Symmetric	Single PSI Dword
1	Reserved	
2	Asymmetric Rx	Paired with Asymmetric Tx PSI Dword
3	Asymmetric Tx	Immediately follows Rx Asymmetric PSI Dword

Bit Position	Bit Name	Description
5, 4	Protocol Speed ID Exponent (PSIE)	This field defines the base 10 exponent to be applied with the Protocol Speed ID Mantissa is used in calculating the maximum bit rate represented by this PSI Dword. The power is three times the value of the field. Table 35.5-41-2

PSIE Value	Bit Rate
0	Bits per second
1	Kb/s
2	Mb/s
3	Gb/s

Bit Position	Bit Name	Description
3 to 0	Protocol Speed ID Value (PSIV)	If a device is attached that operates at the bit rate defined by this PSI Dword, then the value of this field is reported in the Port Speed field of PORTSC register of a compatible port. Note that the PSIV value of 0 is reserved and shall not be defined by a PSI.

(f) Renesas Private Register (USB_HOST_RP)

Renesas private register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0524h

Initial Value: 000A_0135h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Renesas Private															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	Renesas Private	Renesas Private		Renesas Private		Renesas Private			
Initial Value	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-42 USB_HOST_RP Register Contents

Bit Position	Bit Name	Description
31 to 16	Renesas Private	Renesas Private field
15 to 9	—	Reserved
8	Renesas Private	Renesas Private field
7, 6	Renesas Private	Renesas Private field
5, 4	Renesas Private	Renesas Private field
3 to 0	Renesas Private	Renesas Private field

(3) xHCI Supported Protocol Capability for USB2.0

(a) Offset 00h - xHCI Supported Protocol Capability Field Definitions (USB2.0) Register (USB_HOST_U2HCSPC1)

xHCI supported protocol capability field definitions (USB2.0) register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0530h

Initial Value: 0200_0802h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Major Revision								Minor Revision							
Initial Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability ID							
Initial Value	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-43 USB_HOST_U2HCSPC1 Register Contents

Bit Position	Bit Name	Description
31 to 24	Major Revision	Major Specification Release Number in Binary-Coded Decimal (i.e., version 3.x is 03h). This field identifies the major release number component of the specification with which the xHC is compliant.
23 to 16	Minor Revision	Minor Specification Release Number in Binary-Coded Decimal (i.e., version x.10 is 10h). This field identifies the minor release number component of the specification with which the xHC is compliant.
15 to 8	Next Capability Pointer	This field indicates the location of the next capability with relative to the effective address of the current capability.
7 to 0	Capability ID	xHCI Supported Protocol

(b) Offset 04h - xHCI Supported Protocol Capability Field Definitions (USB2.0) Register (USB_HOST_U2HCSPC2)

xHCI supported protocol capability field definitions (USB2.0) register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0534h

Initial Value: 2042_5355h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Name String															
Initial Value	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Name String															
Initial Value	0	1	0	1	0	0	1	1	0	1	0	1	0	1	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-44 USB_HOST_U2HCSPC2 Register Contents

Bit Position	Bit Name	Description
31 to 0	Name String	This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters can be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive.

(c) Offset 08h - xHCI Supported Protocol Capability Field Definitions (USB2.0) Register (USB_HOST_U2HCSPC3)

xHCI supported protocol capability field definitions (USB2.0) register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0538h

Initial Value: 0018_0102h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Protocol Speed ID Count (PSIC)				Hub Depth (MHD)			—	—	—	—	BESL LPM Capability (BLC)	Hardware LPM Capability (HLC)	Integrated Hub Implemented (IHI)	High-speed Only (HSO)	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Compatible Port Count								Compatible Port Offset							
Initial Value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-45 USB_HOST_U2HCSPC3 Register Contents

Bit Position	Bit Name	Description
31 to 28	Protocol Speed ID Count (PSIC)	This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains. If this field is non-zero, then all speeds supported by the protocol shall be defined using PSI Dwords, i.e. no implied Speed ID mappings apply. PSIC value of 0 implies that the default Full-speed, Low-speed, and High-speed bit rates are supported.
27 to 25	Hub Depth (MHD)	If this field is ‘0’, then the standard USB2 hub depth constraints apply, if this field is > ‘0’, then it indicates the maximum hub depth supported by the USB2 ports. This bit is fixed to 0h in the USB3HOST.
24 to 21	—	Reserved
20	BESL LPM Capability (BLC)	If this bit is set to 1b, the ports described by this xHCI Supported Protocol Capability shall apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. If this bit is cleared to 0b, the ports described by this xHCI Supported Protocol Capability shall apply HIRD timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. Note the BESL LMP Capability support (i.e. HLE = ‘1’ and BLC = ‘1’) shall be mandatory for all xHCI 1.1 compliant xHCs. This bit is fixed to 1b in the USB3HOST.
19	Hardware LPM Capability (HLC)	If this bit is set to 1b, the ports described by this xHCI Supported Protocol Capability support hardware controlled USB2 Link Power Management. This bit is fixed to 1b in the USB3HOST.
18	Integrated Hub Implemented (IHI)	If this bit is cleared to 0b, the Root hub to External xHC port mapping adheres to the default mapping. If this bit is set to 1b, the Root Hub to External xHC port mapping does not adhere to the default mapping, and ACPI or other mechanism is required to define the mapping. This bit is fixed to 0b in the USB3HOST.
17	High-speed Only (HSO)	If this bit is cleared to 0b, the USB2 ports described by this capability are High-speed only, e.g. the ports do not support Low- or Full-speed operation. High-speed only implementations can introduce a “Tier mismatch”.
16	—	Reserved
15 to 8	Compatible Port Count	This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts.
7 to 0	Compatible Port Offset	This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are 1 to MaxPorts.

(d) Offset 0Ch - xHCI Supported Protocol Capability Field Definitions (USB2.0) Register (USB_HOST_U2HCSPC4)

xHCI supported protocol capability field definitions (USB2.0) register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 053Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	Protocol Slot Type				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-46 USB_HOST_U2HCSPC4 Register Contents

Bit Position	Bit Name	Description
31 to 5	—	Reserved
4 to 0	Protocol Slot Type	This field specifies the Slot Type value which can specified when allocating Device Slots that support this protocol. Valid values are 0 to 31.

(e) Protocol Speed ID for FS Register (USB_HOST_PSIFS)

Protocol speed ID for fs register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0540h

Initial Value: 000C_0021h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Protocol Speed ID Mantissa (PSIM)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PSI Full-duplex (PFD)	PSI Type (PLT)		Protocol Speed ID Exponent (PSIE)		Protocol Speed ID Value (PSIV)			
Initial Value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-47 USB_HOST_PSIFS Register Contents

Bit Position	Bit Name	Description
31 to 16	Protocol Speed ID Mantissa (PSIM)	This field defines the mantissa that is applied to the PSIE when calculating the maximum bit rate represented by this PSI Dword.
15 to 9	—	Reserved
8	PSI Full-duplex (PFD)	If this bit is 1, the link is full-duplex, and if 0, the link is half-duplex.
7, 6	PSI Type (PLT)	This field identifies whether the PSI Dword defines a symmetric or asymmetric bit rate, and if asymmetric, then this field also indicates if this Dword defines the receive or transmit bit rate. Note that the Asymmetric PSI Dwords shall be paired, i.e. an Rx immediately followed by a Tx, and both Dwords shall define the same value for the PSIV.

Table 35.5-47-1

RLT Value	Bit Rate	Note
0	Symmetric	Single PSI Dword
1	Reserved	
2	Asymmetric Rx	Paired with Asymmetric Tx PSI Dword
3	Asymmetric Tx	Immediately follows Rx Asymmetric PSI Dword

5, 4	Protocol Speed ID Exponent (PSIE)	This field defines the base 10 exponent to be applied with the Protocol Speed ID Mantissa is used in calculating the maximum bit rate represented by this PSI Dword. The power is three times the value of the field.

Table 35.5-47-2

PSIE Value	Bit Rate
0	Bits per second
1	Kb/s
2	Mb/s
3	Gb/s

3 to 0	Protocol Speed ID Value (PSIV)	If a device is attached that operates at the bit rate defined by this PSI Dword, then the value of this field is reported in the Port Speed field of PORTSC register of a compatible port. Note that the PSIV value of 0 is reserved and shall not be defined by a PSI.

(f) Protocol Speed ID for LS Register (USB_HOST_PSILS)

Protocol speed ID for ls register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0544h

Initial Value: 05DC_0012h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Protocol Speed ID Mantissa (PSIM)															
Initial Value	0	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PSI Full-duplex (PFD)	PSI Type (PLT)		Protocol Speed ID Exponent (PSIE)		Protocol Speed ID Value (PSIV)			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-48 USB_HOST_PSILS Register Contents

Bit Position	Bit Name	Description
31 to 16	Protocol Speed ID Mantissa (PSIM)	This field defines the mantissa that is applied to the PSIE when calculating the maximum bit rate represented by this PSI Dword.
15 to 9	—	Reserved
8	PSI Full-duplex (PFD)	If this bit is 1, the link is full-duplex, and if 0, the link is half-duplex.
7, 6	PSI Type (PLT)	This field identifies whether the PSI Dword defines a symmetric or asymmetric bit rate, and if asymmetric, then this field also indicates if this Dword defines the receive or transmit bit rate. Note that the Asymmetric PSI Dwords shall be paired, i.e. an Rx immediately followed by a Tx, and both Dwords shall define the same value for the PSIV.

Table 35.5-48-1

RLT Value	Bit Rate	Note
0	Symmetric	Single PSI Dword
1	Reserved	
2	Asymmetric Rx	Paired with Asymmetric Tx PSI Dword
3	Asymmetric Tx	Immediately follows Rx Asymmetric PSI Dword

5, 4	Protocol Speed ID Exponent (PSIE)	This field defines the base 10 exponent to be applied with the Protocol Speed ID Mantissa is used in calculating the maximum bit rate represented by this PSI Dword. The power is three times the value of the field.

Table 35.5-48-2

PSIE Value	Bit Rate
0	Bits per second
1	Kb/s
2	Mb/s
3	Gb/s

3 to 0	Protocol Speed ID Value (PSIV)	If a device is attached that operates at the bit rate defined by this PSI Dword, then the value of this field is reported in the Port Speed field of PORTSC register of a compatible port. Note that the PSIV value of 0 is reserved and shall not be defined by a PSI.

(g) Protocol Speed ID for HS Register (USB_HOST_PSIHS)

Protocol speed ID for HS register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0548h

Initial Value: 01E0_0023h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Protocol Speed ID Mantissa (PSIM)															
Initial Value	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PSI Full-duplex (PFD)	PSI Type (PLT)		Protocol Speed ID Exponent (PSIE)		Protocol Speed ID Value (PSIV)			
Initial Value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-49 USB_HOST_PSIHS Register Contents

Bit Position	Bit Name	Description
31 to 16	Protocol Speed ID Mantissa (PSIM)	This field defines the mantissa that is applied to the PSIE when calculating the maximum bit rate represented by this PSI Dword.
15 to 9	—	Reserved
8	PSI Full-duplex (PFD)	If this bit is 1, the link is full-duplex, and if 0, the link is half-duplex.
7, 6	PSI Type (PLT)	This field identifies whether the PSI Dword defines a symmetric or asymmetric bit rate, and if asymmetric, then this field also indicates if this Dword defines the receive or transmit bit rate. Note that the Asymmetric PSI Dwords shall be paired, i.e. an Rx immediately followed by a Tx, and both Dwords shall define the same value for the PSIV. Table 35.5-49-1

RLT Value	Bit Rate	Note
0	Symmetric	Single PSI Dword
1	Reserved	
2	Asymmetric Rx	Paired with Asymmetric Tx PSI Dword
3	Asymmetric Tx	Immediately follows Rx Asymmetric PSI Dword

Bit Position	Bit Name	Description
5, 4	Protocol Speed ID Exponent (PSIE)	This field defines the base 10 exponent to be applied with the Protocol Speed ID Mantissa is used in calculating the maximum bit rate represented by this PSI Dword. The power is three times the value of the field. Table 35.5-49-2

PSIE Value	Bit Rate
0	Bits per second
1	Kb/s
2	Mb/s
3	Gb/s

Bit Position	Bit Name	Description
3 to 0	Protocol Speed ID Value (PSIV)	If a device is attached that operates at the bit rate defined by this PSI Dword, then the value of this field is reported in the Port Speed field of PORTSC register of a compatible port. Note that the PSIV value of 0 is reserved and shall not be defined by a PSI.

(4) xHCI Extended Power Management Capability

(a) Power Management Capabilities Register (USB_HOST_PMC)

Power management capabilities register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0550h

Initial Value: 4803_0003h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PME Support					D2 Support	D1 Support	Aux Current			DSI	—	PME Clock	Version		
Initial Value	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability ID							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-50 USB_HOST_PMC Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 27	PME Support	This 5-bit field indicates the power states in which the function can assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal in that power state. Bit[27] XXXX1b – PME# can be asserted from D0 Bit[28] XXX1Xb – PME# can be asserted from D1 Bit[29] XX1XXb – PME# can be asserted from D2 Bit[30] X1XXXb – PME# can be asserted from D3hot Bit[31] 1XXXXb – PME# can be asserted from D3cold
26	D2 Support	If this bit is 1, this function supports the D2 Power Management State. Functions that do not support D2 shall always return a value of 0 for this bit.
25	D1 Support	If this bit is 1, this function supports the D1 Power Management State. Functions that do not support D1 shall always return a value of 0 for this bit.
24 to 22	Aux Current	This 3 bit field reports the 3.3 Vaux auxiliary current requirements for the PCI function. If the Data Register has been implemented by this function: • Reading this field returns a value of 000b. • The Data Register takes precedence over this field for 3.3 Vaux current requirement reporting. If PME# generation from D3cold is not supported by the function (PMC (15) = 0), this field returns a value of 000b, when read.
21	DSI	The Device Specific Initialization bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. Note that this bit is not used by some operating systems. Microsoft Windows and Windows NT, for instance, do not use this bit to determine whether to use D3. Instead, they use the driver's capabilities to determine this. A 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.
20	—	Reserved
19	PME Clock	When this bit is 1, it indicates that the function relies on the presence of the PCI clock for PME# operation. When this bit is 0, it indicates that no PCI clock is required for the function to generate PME#. Functions that do not support PME# generation in any state returns 0 for this field.
18 to 16	Version	A value of 011b indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification.

Table 35.5-50 USB_HOST_PMC Register Contents (2/2)

Bit Position	Bit Name	Description
15 to 8	Next Capability Pointer	This field provides an offset into the function's PCI Configuration Space pointing to the location of next item in the function's capability list. If there are no additional items in the Capabilities List, this register is set to 0h.
7 to 0	Capability ID	Extended Power Management

(b) Power Management Control/Status Register (USB_HOST_PMCSR)

Power management control/status register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0554h

Initial Value: 0000_0008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PME Status	Data Scale		Data Select				PME En	—	—	—	—	No Soft Reset	—	PowerState	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W	RW1	R	R	R	R	R	R	RW	R	R	R	R	R	R	RW	RW

Table 35.5-51 USB_HOST_PMCSR Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 16	—	Reserved
15	PME Status	This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit. Writing 1 clears this bit and causes the function to stop asserting a PME# (if enabled). Writing 0 has no effect. This bit defaults to 0 if the function does not support PME# generation from D3cold. If the function supports PME# from D3cold, then this bit is sticky and shall be explicitly cleared by the operating system each time the operating system is initially loaded.
14, 13	Data Scale	This 2-bit read-only field indicates the scaling factor to be used when interpreting the value of the Data register. The value and meaning of this field will vary depending on which data value has been selected by the Data_Select field. This field is a required component of the Data register (offset 7) and shall be implemented if the Data register is implemented. If the Data register has not been implemented, this field shall return 00b when the PMCSR is read.
12 to 9	Data Select	This 4-bit field is used to select which data is to be reported through the Data register and Data_Scale field. This field is a required component of the Data register (offset 7) and shall be implemented if the Data register is implemented. If the Data register is not implemented, this field should be read only and return 0000b when the PMCSR is read
8	PME En	Writing 1 to this bit enables the function to assert PME#. When 0, PME# assertion is disabled. This bit defaults to 0 if the function does not support PME# generation from D3cold. If the function supports PME# from D3cold, then this bit is sticky and shall be explicitly cleared by the operating system each time it is initially loaded. Functions that do not support PME# generation from any D-state (i.e., PMC (15:11) = 0 0000b), can hardwire this bit to be read-only always returning 0 when read by system software.
7 to 4	—	Reserved. These bits are read as 0b. Writing is invalid.
3	No Soft Reset	When set (1), this bit indicates that devices are transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.

Table 35.5-51 USB_HOST_PMCSR Register Contents (2/2)

Bit Position	Bit Name	Description
2	—	Reserved. This bit is read as 0b. Writing is invalid.
1, 0	PowerState	This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below. 00b: D0 01b: D1 10b: D2 11b: D3hot If an unsupported or optional state is written to this field by software, the write operation shall complete normally on the bus. However, the data is discarded and no state change occurs.

35.5.4.5 Host Controller Runtime Registers

(1) Microframe Index Register (USB_HOST_MFINDEX)

Microframe index register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0600h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	Microframe Index													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-52 USB_HOST_MFINDEX Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved
13 to 0	Microframe Index	The value in this register increments at the end of each microframe (e.g. 125us.). Bits [13:3] can be used to determine the current 1ms Frame Index.

(2) Interrupter Register Set 0

(a) Interrupter Management Register (USB_HOST_IMAN)

Interrupter management register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0620h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Interrupt Enable (IE)	Interrupt Pending (IP)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW1

Table 35.5-53 USB_HOST_IMAN Register Contents

Bit Position	Bit Name	Description
31 to 2	—	Reserved
1	Interrupt Enable (IE)	Default = 0. This flag specifies whether the Interrupter is capable of generating interrupts. When this bit and the IP bit are set to (1), the Interrupter generates an interrupt when the Interrupter Moderation Counter reaches 0. If this bit is 0, then the Interrupter is prohibited from generating interrupts.
0	Interrupt Pending (IP)	Default = 0. This flag represents the current state of the Interrupter. If IP = 1, an interrupt is pending for this Interrupter. A 0 value indicates that no interrupt is pending for the Interrupter.

(b) Interrupter Moderation Register (USB_HOST_IMOD)

Interrupter moderation register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0624h

Initial Value: 0000_0FA0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Interrupt Moderation Counter (IMODC)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Interrupt Moderation Interval (IMODI)															
Initial Value	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.5-54 USB_HOST_IMOD Register Contents

Bit Position	Bit Name	Description
31 to 16	Interrupt Moderation Counter (IMODC)	Default = undefined. Down counter. Loaded with the IMODI value whenever IP is cleared to 0, counts down to 0, and stops. The associated interrupt is signaled whenever this counter is 0, the Event Ring is not empty, the IE and IP flags = 1, and EHB = 0. This counter can be directly written by software at any time to alter the interrupt rate.
15 to 0	Interrupt Moderation Interval (IMODI)	Default = ‘4000’ (up to 1 ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of 0 disables interrupt throttling logic and interrupts are generated immediately if IP = 0, EHB = 0, and the Event Ring is not empty.

(c) Event Ring Registers

Event Ring Segment Table Size Register (USB_HOST_ERSTSZ)

Event ring segment table size register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0628h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Event Ring Segment Table Size															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.5-55 USB_HOST_ERSTSZ Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved
15 to 0	Event Ring Segment Table Size	Default = 0. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register. For the Primary Interrupter: Writing a value of 0 to this field results in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled.

Event Ring Segment Table Base Address Low Register (USB_HOST_ERSTBAL)

Event ring segment table base address low register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0630h

Initial Value: 0000_0000h

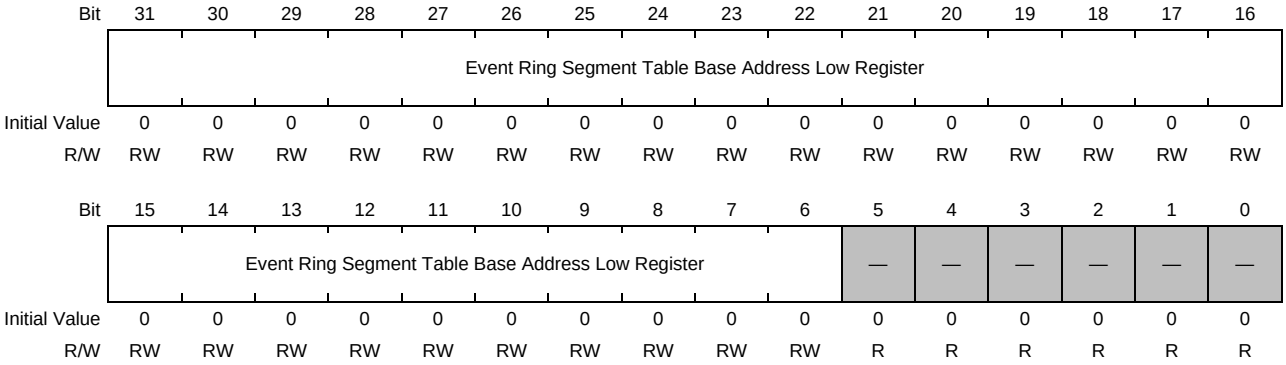


Table 35.5-56 USB_HOST_ERSTBAL Register Contents

Bit Position	Bit Name	Description
31 to 6	Event Ring Segment Table Base Address Low Register	Default = 0. This field defines the lower-order bits of the address of where the Event Ring Segment Table starts. Writing to this register sets advancement of the event ring state machine (EREP) to the start state. This field shall not be modified if HCHalted (HCH) = 0.
5 to 0	—	Reserved

Event Ring Segment Table Base Address High Register (USB_HOST_ERSTBAH)

Event ring segment table base address high register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0634h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Event Ring Segment Table Base Address High Register															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Event Ring Segment Table Base Address High Register															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.5-57 USB_HOST_ERSTBAH Register Contents

Bit Position	Bit Name	Description
31 to 0	Event Ring Segment Table Base Address High Register	Default = 0. This field defines the higher-order bits of the start address where the Event Ring Segment Table starts. Writing to this register sets advancement of the event ring state machine (EREP) to the start state. This field shall not be modified if HCHalted (HCH) = 0.

Event Ring Dequeue Pointer Low Register (USB_HOST_ERDPL)

Event ring dequeue pointer low register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0638h

Initial Value: 0000_0000h

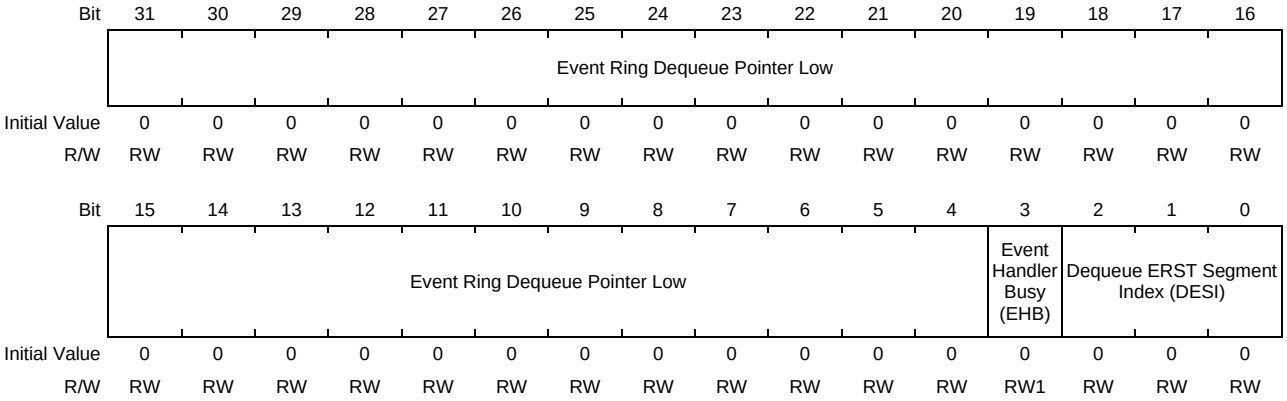


Table 35.5-58 USB_HOST_ERDPL Register Contents

Bit Position	Bit Name	Description
31 to 4	Event Ring Dequeue Pointer Low	Default = 0. This field defines the lower-order bits of the 64-bit address of the current Event Ring Dequeue Pointer.
3	Event Handler Busy (EHB)	Default = 0. This flag is set to 1 when the IP bit is set to 1 and cleared to 0 by software when the Dequeue Pointer register is written.
2 to 0	Dequeue ERST Segment Index (DESI)	Default = 0. This field can be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the lower-order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in.

Event Ring Dequeue Pointer High Register (USB_HOST_ERDPH)

Event ring dequeue pointer high register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 063Ch

Initial Value: 0000_0000h

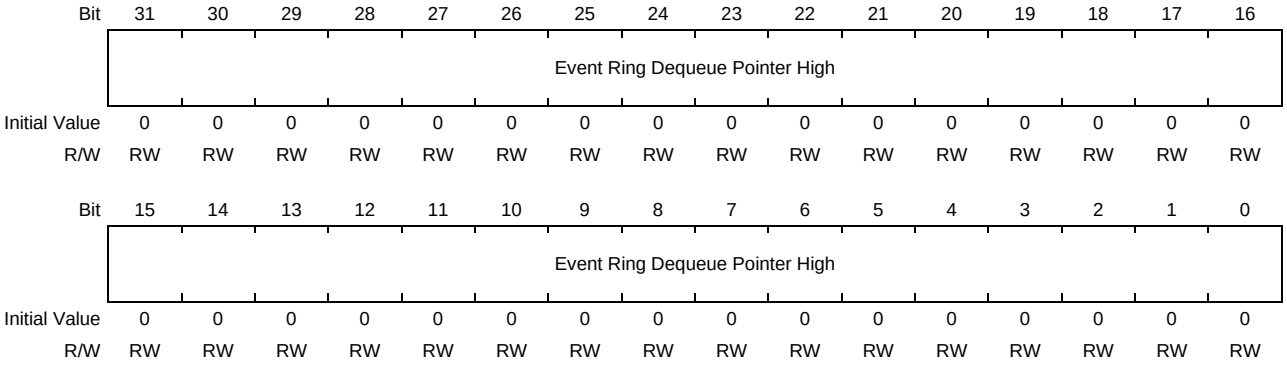


Table 35.5-59 USB_HOST_ERDPH Register Contents

Bit Position	Bit Name	Description
31 to 0	Event Ring Segment Table Base Address High Register	Default = 0. This field defines the higher-order bits of the start address of where the Event Ring Segment Table starts. Writing this register sets advancement of the event ring state machine (EREP) to the start state. This field shall not be modified if HCHalted (HCH) = 0.

35.5.4.6 Doorbell Registers

(1) Host Controller Doorbell Register (USB_HOST_HCD)

Host controller doorbell register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 0700h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DB Target							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW1	RW	RW	RW

Table 35.5-60 USB_HOST_HCD Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved
7 to 0	DB Target	Doorbell Target. This field defines the target of a doorbell reference. The table below defines the xHC notifications that are generated by ringing a doorbell. Note that Doorbell Register 0 is dedicated to the Command Ring and this field of that register is decoded differently from the field in the Doorbell Registers. Host Controller Doorbell (0) 00h: Command Doorbell 01h to F7h: Reserved F8h to FFh: Vendor Defined This field returns 0 when read and should be treated as “undefined” by software.

(2) Device Context Doorbell Register (Slot #m) (USB_HOST_DCDm) (m = 01 to 32)

Device context doorbell register.

Access Size: 32 bits

Address(es): USB_HOST_DCD01 : <USB_S0_base> + 0704h
USB_HOST_DCD02 : <USB_S0_base> + 0708h
USB_HOST_DCD03 : <USB_S0_base> + 070Ch
USB_HOST_DCD04 : <USB_S0_base> + 0710h
USB_HOST_DCD05 : <USB_S0_base> + 0714h
USB_HOST_DCD06 : <USB_S0_base> + 0718h
USB_HOST_DCD07 : <USB_S0_base> + 071Ch
USB_HOST_DCD08 : <USB_S0_base> + 0720h
USB_HOST_DCD09 : <USB_S0_base> + 0724h
USB_HOST_DCD10 : <USB_S0_base> + 0728h
USB_HOST_DCD11 : <USB_S0_base> + 072Ch
USB_HOST_DCD12 : <USB_S0_base> + 0730h
USB_HOST_DCD13 : <USB_S0_base> + 0734h
USB_HOST_DCD14 : <USB_S0_base> + 0738h
USB_HOST_DCD15 : <USB_S0_base> + 073Ch
USB_HOST_DCD16 : <USB_S0_base> + 0740h
USB_HOST_DCD17 : <USB_S0_base> + 0744h
USB_HOST_DCD18 : <USB_S0_base> + 0748h
USB_HOST_DCD19 : <USB_S0_base> + 074Ch
USB_HOST_DCD20 : <USB_S0_base> + 0750h
USB_HOST_DCD21 : <USB_S0_base> + 0754h
USB_HOST_DCD22 : <USB_S0_base> + 0758h
USB_HOST_DCD23 : <USB_S0_base> + 075Ch
USB_HOST_DCD24 : <USB_S0_base> + 0760h
USB_HOST_DCD25 : <USB_S0_base> + 0764h
USB_HOST_DCD26 : <USB_S0_base> + 0768h
USB_HOST_DCD27 : <USB_S0_base> + 076Ch
USB_HOST_DCD28 : <USB_S0_base> + 0770h
USB_HOST_DCD29 : <USB_S0_base> + 0774h
USB_HOST_DCD30 : <USB_S0_base> + 0778h
USB_HOST_DCD31 : <USB_S0_base> + 077Ch
USB_HOST_DCD32 : <USB_S0_base> + 0780h

Initial Value: 0000_0000h

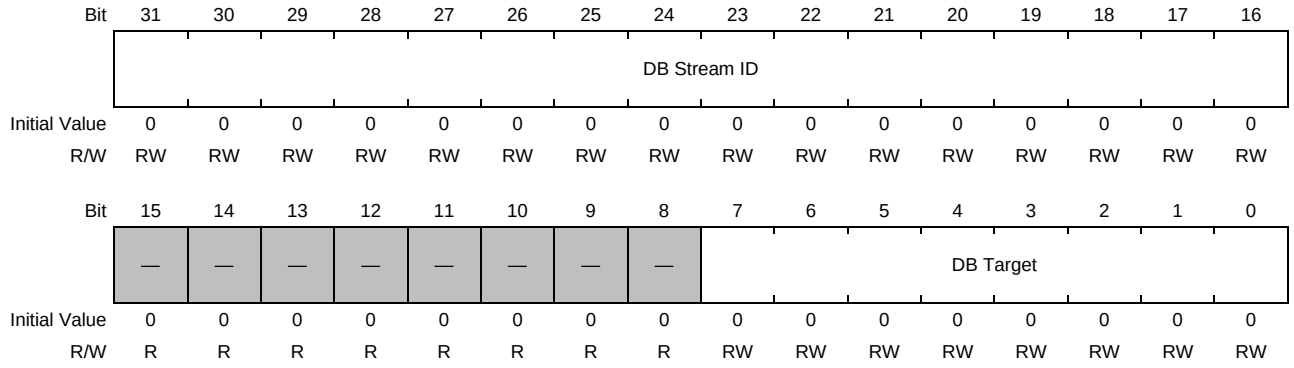


Table 35.5-61 USB_HOST_DCDm Register Contents

Bit Position	Bit Name	Description
31 to 16	DB Stream ID	Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines streams, then this field can be used to identify the stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines streams (MaxPStreams > 0), then 0, 65535 (no stream) and 65534 (prime) are reserved stream ID values and shall not be written to this field. If the endpoint does not define streams (MaxPStreams = 0) and a non-0 value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Command Doorbells. This field returns '0' when read.
15 to 8	—	Reserved
7 to 0	DB Target	Doorbell Target. This field defines the target of a doorbell reference. The table below defines the xHC notifications that are generated by ringing a doorbell. Note that Doorbell Register 0 is dedicated to the Command Ring and this field of that register is decoded differently from the field in the Doorbell Registers. Device Context Doorbells (1-255) 00h: Reserved 01h: Control EP 0 Enqueue Pointer Update 02h: EP 1 OUT Enqueue Pointer Update 03h: EP 1 IN Enqueue Pointer Update 04h: EP 2 OUT Enqueue Pointer Update 05h: EP 2 IN Enqueue Pointer Update | 1Eh: EP 15 OUT Enqueue Pointer Update 1Fh: EP 15 IN Enqueue Pointer Update 20h to F7h: Reserved F8h to FFh: Vendor Defined This field returns 0 when read and should be treated as "undefined" by software.

35.5.4.7 Core Defined Registers

(1) Core Control and Status Registers

(a) Revision ID Register (USB_HOST_REVID)

Revision ID register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1000h

Initial Value: E300_0100h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Core ID1								Core ID2							
Initial Value	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Major Version								Minor Version							
Initial Value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-62 USB_HOST_REVID Register Contents

Bit Position	Bit Name	Description
31 to 24	Core ID1	Identified upper number of the core
23 to 16	Core ID2	Identified lower number of the core
15 to 8	Major Version	Major version of the core
7 to 0	Minor Version	Minor version of the core

(b) Configuration Status1 Register (USB_HOST_CFGSTS1)

Register for reading core configuration values.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1004h

Initial Value: 0x21_4111h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private		Renesas Private
Initial Value	0	0	0	0	0	0	x	x	0	0	1	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Renesas Private	Renesas Private	Renesas Private	Renesas Private	—	Number of USB Receptacle (REPNUM)			—	Number of U3 Port (U3NUM)			—	Number of U2 Port (U2NUM)		
Initial Value	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-63 USB_HOST_CFGSTS1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	Renesas Private	Renesas Private bit
30	Renesas Private	Renesas Private bit
29	Renesas Private	Renesas Private bit
28	Renesas Private	Renesas Private bit
27	Renesas Private	Renesas Private bit
26	Renesas Private	Renesas Private bit
25	Renesas Private	Renesas Private bit.
24	Renesas Private	Renesas Private bit.
23	Renesas Private	Renesas Private bit
22	Renesas Private	Renesas Private bit
21	Renesas Private	Renesas Private bit
20	Renesas Private	Renesas Private bit
19	Renesas Private	Renesas Private bit
18, 17	Renesas Private	Renesas Private bit
16	Renesas Private	Renesas Private bit
15	Renesas Private	Renesas Private bit
14	Renesas Private	Renesas Private bit
13	Renesas Private	Renesas Private bit
12	Renesas Private	Renesas Private bit
11	—	Reserved
10 to 8	Number of USB Receptacle (REPNUM)	Indicate the number of USB receptacle
7	—	Reserved
6 to 4	Number of U3 Port (U3NUM)	Indicate the number of U3 ports
3	—	Reserved

Table 35.5-63 USB_HOST_CFGSTS1 Register Contents (2/2)

Bit Position	Bit Name	Description
2 to 0	Number of U2 Port (U2NUM)	Indicate the number of USB2.0 ports.

(c) Configuration Status2 Register (USB_HOST_CFGSTS2)

Register for reading core configuration values.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1008h

Initial Value: 0000_1388h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ACLK's period (ACLKFREQ)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ACLK's period (ACLKFREQ)															
Initial Value	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-64 USB_HOST_CFGSTS2 Register Contents

Bit Position	Bit Name	Description
31 to 0	ACLK's period (ACLKFREQ)	Indicates "the aclk's Period". This value 1388h means aclk's period is 5000ps (5ns), that is 200MHz.

(d) Configuration Status3 Register (USB_HOST_CFGSTS3)

Register for reading core configuration values.

Access Size: 32 bits

Address(es): <USB_S0_base> + 100Ch

Initial Value: 0011_0111h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	—	Renesas Private		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private	—	—	Renesas Private	Renesas Private	Renesas Private			
Initial Value	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-65 USB_HOST_CFGSTS3 Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved
24	Renesas Private	Renesas Private bit
23	Renesas Private	Renesas Private bit
22	Renesas Private	Renesas Private bit
21	Renesas Private	Renesas Private bit
20	Renesas Private	Renesas Private bit
19	—	Reserved
18 to 16	Renesas Private	Renesas Private bit
15	Renesas Private	Renesas Private bit
14	Renesas Private	Renesas Private bit
13	Renesas Private	Renesas Private bit
12	Renesas Private	Renesas Private bit
11	Renesas Private	Renesas Private bit
10	Renesas Private	Renesas Private bit
9	Renesas Private	Renesas Private bit
8	Renesas Private	Renesas Private bit
7, 6	—	Reserved
5	Renesas Private	Renesas Private bit
4	Renesas Private	Renesas Private bit
3 to 0	Renesas Private	Renesas Private bit

(e) Configuration Status4 Register (USB_HOST_CFGSTS4)

Register for reading core configuration values.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1010h

Initial Value: 0000_0021h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	Renesas Private									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Renesas Private									
Initial Value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-66 USB_HOST_CFGSTS4 Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved
25 to 16	Renesas Private	Renesas Private field.
15 to 10	—	Reserved
9 to 0	Renesas Private	Renesas Private field.

(f) Configuration Status5 Register (USB_HOST_CFGSTS5)

Register for reading core configuration values.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1014h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	Renesas Private									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Renesas Private									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-67 USB_HOST_CFGSTS5 Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved
25 to 16	Renesas Private	Renesas Private field.
15 to 10	—	Reserved
9 to 0	Renesas Private	Renesas Private field.

(g) Configuration Status6 Register (USB_HOST_CFGSTS6)

Register for reading core configuration values.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1018h

Initial Value: 0000_0129h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	Renesas Private									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Renesas Private									
Initial Value	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-68 USB_HOST_CFGSTS6 Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved
25 to 16	Renesas Private	Renesas Private field.
15 to 10	—	Reserved
9 to 0	Renesas Private	Renesas Private field.

(h) Configuration Status7 Register (USB_HOST_CFGSTS7)

Register for reading core configuration values.

Access Size: 32 bits

Address(es): <USB_S0_base> + 101Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	Renesas Private									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Renesas Private									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-69 USB_HOST_CFGSTS7 Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved
25 to 16	Renesas Private	Renesas Private field.
15 to 10	—	Reserved
9 to 0	Renesas Private	Renesas Private field.

(i) Configuration Status8 Register (USB_HOST_CFGSTS8)

Register for reading core configuration values.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1020h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	Renesas Private									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Renesas Private									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-70 USB_HOST_CFGSTS8 Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved
25 to 16	Renesas Private	Renesas Private field.
15 to 10	—	Reserved
9 to 0	Renesas Private	Renesas Private field.

(j) Configuration Status9 Register (USB_HOST_CFGSTS9)

Register for reading core configuration values.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1024h

Initial Value: 0000_0000h

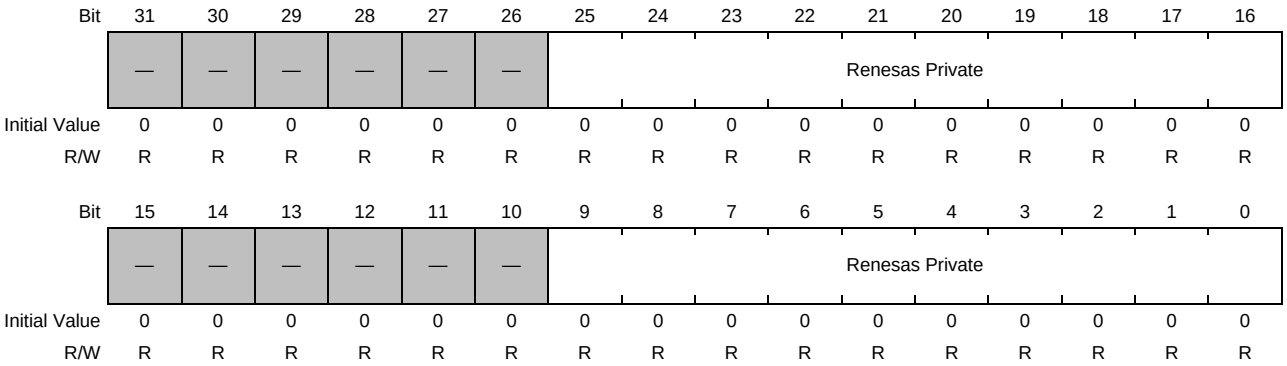


Table 35.5-71 USB_HOST_CFGSTS9 Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved
25 to 16	Renesas Private	Renesas Private field.
15 to 10	—	Reserved
9 to 0	Renesas Private	Renesas Private field.

(k) Configuration Status10 Register (USB_HOST_CFGSTS10)

Register for reading core configuration values.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1028h

Initial Value: 0006_0030h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	SS Data Buffer Size				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	Renesas Private					—	U2 Data Buffer Size			—	—	Renesas Private	
Initial Value	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-72 USB_HOST_CFGSTS10 Register Contents

Bit Position	Bit Name	Description
31 to 21	—	Reserved
20 to 16	SS Data Buffer Size	Indicate the Data buffer size for U3. 6: 6 Kbytes
15 to 13	—	Reserved
12 to 8	Renesas Private	Renesas Private field.
7	—	Reserved
6 to 4	U2 Data Buffer Size	Indicate the Data buffer size for U2. 3: 1 Kbyte
3, 2	—	Reserved
1, 0	Renesas Private	Renesas Private field.

(l) Data Buffer Threshold Control Register (USB_HOST_DBUFTH)

Before USBCMD register's Run/Stop bit is set to 1, this register shall be written.

Access Size: 32 bits

Address(es): <USB_S0_base> + 102Ch

Initial Value: 1111_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	Renesas Private		—	—	Renesas Private		—	—	Renesas Private		—	—	Renesas Private	
Initial Value	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
R/W	R	R	RW	RW	R	R	RW	RW	R	R	RW	RW	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	Renesas Private		—	—	Renesas Private		—	—	Renesas Private		—	—	Renesas Private	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	R	R	RW	RW	R	R	RW	RW	R	R	RW	RW

Table 35.5-73 USB_HOST_DBUFTH Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved
29, 28	Renesas Private	Renesas Private bit This field shall be set to 1h.
27, 26	—	Reserved
25, 24	Renesas Private	Renesas Private bit This field shall be set to 1h.
23, 22	—	Reserved
21, 20	Renesas Private	Renesas Private bit This field shall be set to 1h.
19, 18	—	Reserved
17, 16	Renesas Private	Renesas Private bit This field shall be set to 1h.
15, 14	—	Reserved
13, 12	Renesas Private	Renesas Private bit This field shall be set to 0h.
11, 10	—	Reserved
9, 8	Renesas Private	Renesas Private bit This field shall be set to 0h.
7, 6	—	Reserved
5, 4	Renesas Private	Renesas Private bit This field shall be set to 0h.
3, 2	—	Reserved
1, 0	Renesas Private	Renesas Private bit This field shall be set to 0h.

(m) Core Control Register (USB_HOST_CORECTRL)

Core control register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1030h

Initial Value: 0000_2000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Renesas Private	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Renesas Private
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Renesas Private				—	Renesas Private	Renesas Private	Renesas Private	—	—	—	—	—	—	—	Renesas Private
Initial Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	R	RW	RW	RW	R	R	R	R	R	R	R	RW

Table 35.5-74 USB_HOST_CORECTRL Register Contents

Bit Position	Bit Name	Description
31	Renesas Private	Renesas Private bit This field shall be set to 0h.
30 to 17	—	Reserved
16 to12	Renesas Private	Renesas Private bit This field shall be set to 2h.
11	—	Reserved
10	Renesas Private	Renesas Private bit This field shall be set to 0h.
9	Renesas Private	Renesas Private bit This field shall be set to 0h.
8	Renesas Private	Renesas Private bit This field shall be set to 0h.
7 to 1	—	Reserved
0	Renesas Private	Renesas Private bit This field shall be set to 0h.

(n) PHY Control Register (USB_HOST_PHYCTRL)

Phy control register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1034h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Renesas Private	Renesas Private	Renesas Private	Renesas Private	—	—	—	—	—	—	—	—	Renesas Private	Renesas Private	Renesas Private	USB3.0 PHY for Port1's Reset (U3P1PHY_RST)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	Force Active USB2.0 PHY PLL (FA_U2PLL)	—	—	—	—	—	—	—	USB2.0 PHY Reset (U2PHY_RST)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	R	R	R	R	R	R	R	RW

Table 35.5-75 USB_HOST_PHYCTRL Register Contents

Bit Position	Bit Name	Description
31	Renesas Private	Renesas Private bit This field shall be set to 0h.
30	Renesas Private	Renesas Private bit This field shall be set to 0h.
29	Renesas Private	Renesas Private bit This field shall be set to 0h.
28	Renesas Private	Renesas Private bit This field shall be set to 0h.
27 to 20	—	Reserved
19	Renesas Private	Renesas Private bit
18	Renesas Private	Renesas Private bit
17	Renesas Private	Renesas Private bit
16	USB3.0 PHY for Port1's Reset (U3P1PHY_RST)	This is a bit to output a reset signal for USB3.0 PHY for Port1. 0b: Non-reset assertion 1b: Reset assertion
15 to 9	—	Reserved
8	Force Active USB2.0 PHY PLL (FA_U2PLL)	Setting this bit forces the PLL for USB2.0 to the active condition. 0b: PLL for USB2.0 does not force to the active condition 1b: PLL for USB2.0 forces to the active condition
7 to 1	—	Reserved
0	USB2.0 PHY Reset (U2PHY_RST)	This is a bit to output a reset signal for USB2.0 PHY. 0b: Non-reset assertion 1b: Reset assertion

(o) PHY Status Register (USB_HOST_PHYSTS)

Phy status register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1038h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	Renesas Private	Renesas Private	Renesas Private	USB3.0 for Port1 PLL Lock (U3P1PLL_LOCK)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	USB2.0 PLL Lock (U2PLL_LOCK)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-76 USB_HOST_PHYSTS Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved
19	Renesas Private	Renesas Private bit
18	Renesas Private	Renesas Private bit
17	Renesas Private	Renesas Private bit
16	USB3.0 for Port1 PLL Lock (U3P1PLL_LOCK)	Indicates that USB3.0 for Port 1 PLL is locked. 0b: USB3.0 PLL is not locked. 1b: USB3.0 PLL is locked.
15 to 1	—	Reserved
0	USB2.0 PLL Lock (U2PLL_LOCK)	Indicates that USB2.0 PLL is locked. 0b: USB2.0 PLL is not locked. 1b: USB2.0 PLL is locked

(p) Renesas Private Register (USB_HOST_RP2)

Renesas private register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 103Ch

Initial Value: 000x_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Renesas Private	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Renesas Private															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.5-77 USB_HOST_RP2 Register Contents

Bit Position	Bit Name	Description
31 to 18	—	Reserved
17 to 0	Renesas Private	Renesas Private field. This field shall be set to this field's read value. *Note*: The default value depends on User-settable Keywords.

(q) Interrupt Status Register (USB_HOST_INTSTS)

This register indicates interrupt s' status of the USB3HOST.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1040h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	SMI Interrupt (SMI_INT)	—	HSE Interrupt (HSE_INT)	PME Interrupt (PME_INT)	XHC Interrupt (XHC_INT)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.5-78 USB_HOST_INTSTS Register Contents

Bit Position	Bit Name	Description
31 to 5	—	Reserved
4	SMI Interrupt (SMI_INT)	SMI interrupt status When an SMI interrupt occurs, this bit is set to 1b. Smi_int is this interrupt output signal.
3	—	Reserved
2	HSE Interrupt (HSE_INT)	HSE interrupt status When an HSE interrupt occurs, this bit is set to 1b. Hse_int is this interrupt output signal
1	PME Interrupt (PME_INT)	PME interrupt status When a PME interrupt occurs, this bit is set to 1b. Pme_int is this interrupt output signal.
0	XHC Interrupt (XHC_INT)	XHC interrupt status When an XHC interrupt occurs, this bit is set to 1b. Xhc_int is this interrupt output signal.

(r) Interrupt Enable Register (USB_HOST_INTEN)

Interrupt enable register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1044h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	SMI Interrupt Enable (SMI_INTE)	—	HSE Interrupt Enable (HSE_INTE)	PME Interrupt Enable (PME_INTE)	XHC Interrupt Enable (XHC_INTE)
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW

Table 35.5-79 USB_HOST_INTEN Register Contents

Bit Position	Bit Name	Description
31 to 5	—	Reserved
4	SMI Interrupt Enable (SMI_INTE)	This bit selects whether the interrupt state of INTSTS.SMI_INT is joined all_int interrupt output or not. 0b: The interrupt state of INTSTS.SMI_INT is not joined all_int. 1b: The interrupt state of INTSTS.SMI_INT is joined all_int.
3	—	Reserved. When writing to these bits, the software shall write the same value as is read from the bits.
2	HSE Interrupt Enable (HSE_INTE)	This bit selects whether the interrupt state of INTSTS.HSE_INT is joined all_int interrupt output. 0b: The interrupt state of INTSTS.HSE_INT is not joined all_int. 1b: The interrupt state of INTSTS.HSE_INT is joined all_int.
1	PME Interrupt Enable (PME_INTE)	This bit selects whether the interrupt state of INTSTS.PME_INT is joined all_int interrupt output. 0b: The interrupt state of INTSTS.PME_INT is not joined all_int. 1b: The interrupt state of INTSTS.PME_INT is joined all_int.
0	XHC Interrupt Enable (XHC_INTE)	This bit selects whether the interrupt state of INTSTS.XHC_INT is joined all_int interrupt output. 0b: The interrupt state of INTSTS.XHC_INT is not joined all_int. 1b: The interrupt state of INTSTS.XHC_INT is joined all_int.

(s) Frame Length Adjustment Register (FLADJ) & Serial Bus Release Number Register (SBRN) (USB_HOST_FLADJ_SBRN)

This is Serial Bus Release Number (SBRN) & Frame Length Adjustment (FLADJ) & Default Best Effort Service Latency (DBESL) & Default Best Effort Service Latency Deep (DBESLD) Register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1050h

Initial Value: 00xx_2031h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	Default Best Effort Service Latency Deep (DBESLD)				Default Best Effort Service Latency (DBESL)			
Initial Value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	No Frame Length Timing Capability (NFC)	Frame Length Adjustment (FLADJ)						Serial Bus Release Number (SBRN)							
Initial Value	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	1
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	R

Table 35.5-80 USB_HOST_FLADJ_SBRN Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved
23 to 20	Default Best Effort Service Latency Deep (DBESLD)	If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field.
19 to 16	Default Best Effort Service Latency (DBESL)	If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field.
15	—	Reserved
14	No Frame Length Timing Capability (NFC)	This flag indicates whether the host controller implementation supports a Frame Length Timing Value. A 1b in this bit indicates that the Frame Length Timing Value is not supported. A 0b in this bit indicates that the Frame Length Timing Value is supported.
13 to 8	Frame Length Adjustment (FLADJ)	Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate an SOF microframe length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives an SOF cycle time of 60000. Table 35.5-80-1

Table 35.5-80-1

Frame Length (# HS bit times)(decimal)	FLADJ Value(decimal)
59488	0(00h)
59504	1(01h)
59520	2(02h)
…	
59984	31(1Fh)
60000	32(20h)
…	
60480	62(3Eh)
60496	63(3Fh)

7 to 0	Serial Bus Release Number (SBRN)	The version of the Universal Serial Bus Specification that is compliant with Host Controller. 31h: Release 3.1

(2) Battery Charging Register

(a) Battery Charging Control Register (USB_HOST_BCCTRL)

Battery charging control register.

Access Size: 32 bits

Address(es): <USB_S0_base> + 1080h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Renesas Private	Renesas Private	Renesas Private	Renesas Private	Renesas Private		Renesas Private		Renesas Private		BC_MODE_P1	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.5-81 USB_HOST_BCCTRL Register Contents

Bit Position	Bit Name	Description
31 to 12	—	Reserved
11	Renesas Private	Renesas Private bit This bit shall be set to 0.
10	Renesas Private	Renesas Private bit This bit shall be set to 0.
9	Renesas Private	Renesas Private bit This bit shall be set to 0.
8	Renesas Private	Renesas Private bit This bit shall be set to 0.
7, 6	Renesas Private	Renesas Private bit
5, 4	Renesas Private	Renesas Private bit
3, 2	Renesas Private	Renesas Private bit
1, 0	BC_MODE_P1	Battery Charging Mode for Port1 00b: SDP 01b: CDP 10b: DCP 11b: Reserved

35.5.5 Description of Functions

The prefix (USB_HOST_) of the register names is omitted in this and subsequent sections.

35.5.5.1 Battery Charging

The USB3HOST supports the Battery Charging function of the Charging Port Device which is on the supply side.

The Battery Charging function is used to pull more current from VBUS than the current specified in the USB specification.

The following Port Modes are supported in the USB3HOST;

- Standard Downstream Port (SDP)
- Charging Downstream Port (CDP)
- Dedicated Charging Port (DCP)

NOTE

For detail, please refer to the Battery Charging Specification Revision1.2.

(1) Setting Battery Charging Mode

The user can select one of BC modes by setting BCCTRL.BC_MODE_P[m] (m : 1)'s field in Battery Charging Control Register (BCCTRL) [Refer to **Section 35.5.4.7(2)(a)**], when the user uses the battery charging function.

Table 35.5-82 BC_MODE_P[m]'s information of Battery Charging Control Register (BCCTRL)

Bit	Field	SW	Default Value	Function
1:0	BC_MODE_P1	RW	0h	Battery Charging Mode for Port1 0: SDP 1: CDP 2: DCP 3: Reserved

(2) How to Set Battery Charging Mode

The host driver can set the battery charging mode by executing the flow in the **Figure 35.5-2**.

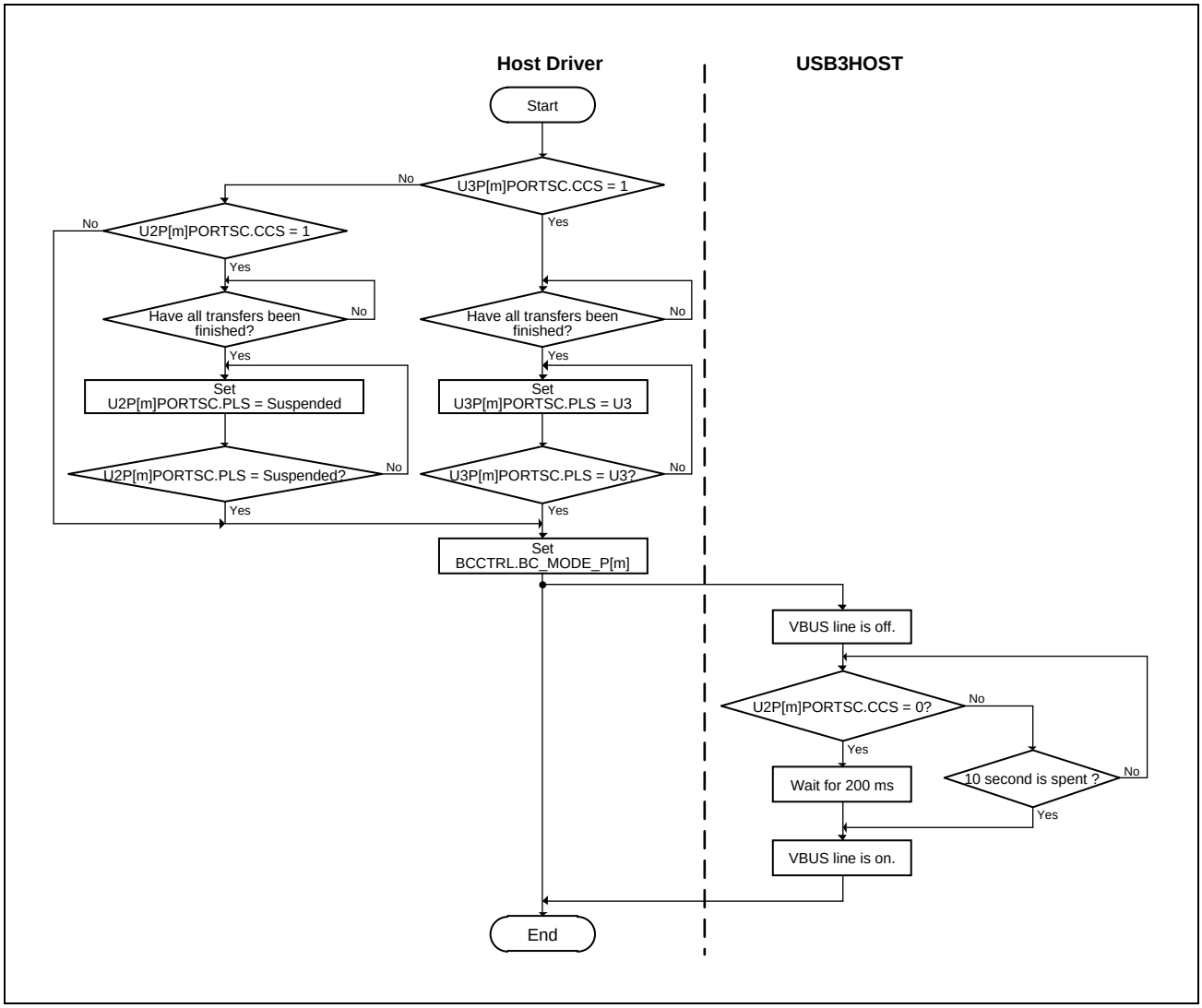


Figure 35.5-2 Host Driver's Flow to Set BC Mode (m = 1)

35.5.5.2 Initialization Flow

Figure 35.5-3 shows the “initialization flow” to the USB3HOST in USB system.

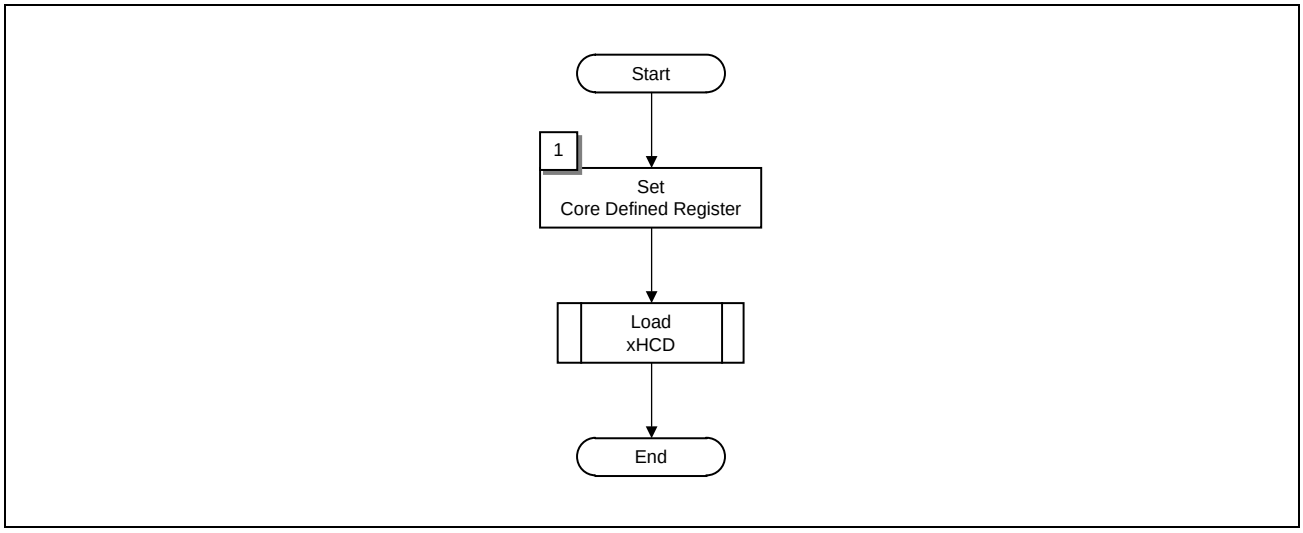


Figure 35.5-3 Initialization Flowchart

1. Set Core Defined Register
   Information of related interrupts is set in this phase.

35.5.5.3 xHCD Initialization Flow

Figure 35.5-4 shows the “initialization flow by xHCD (xHCI Driver)” to the USB3HOST in USB system.

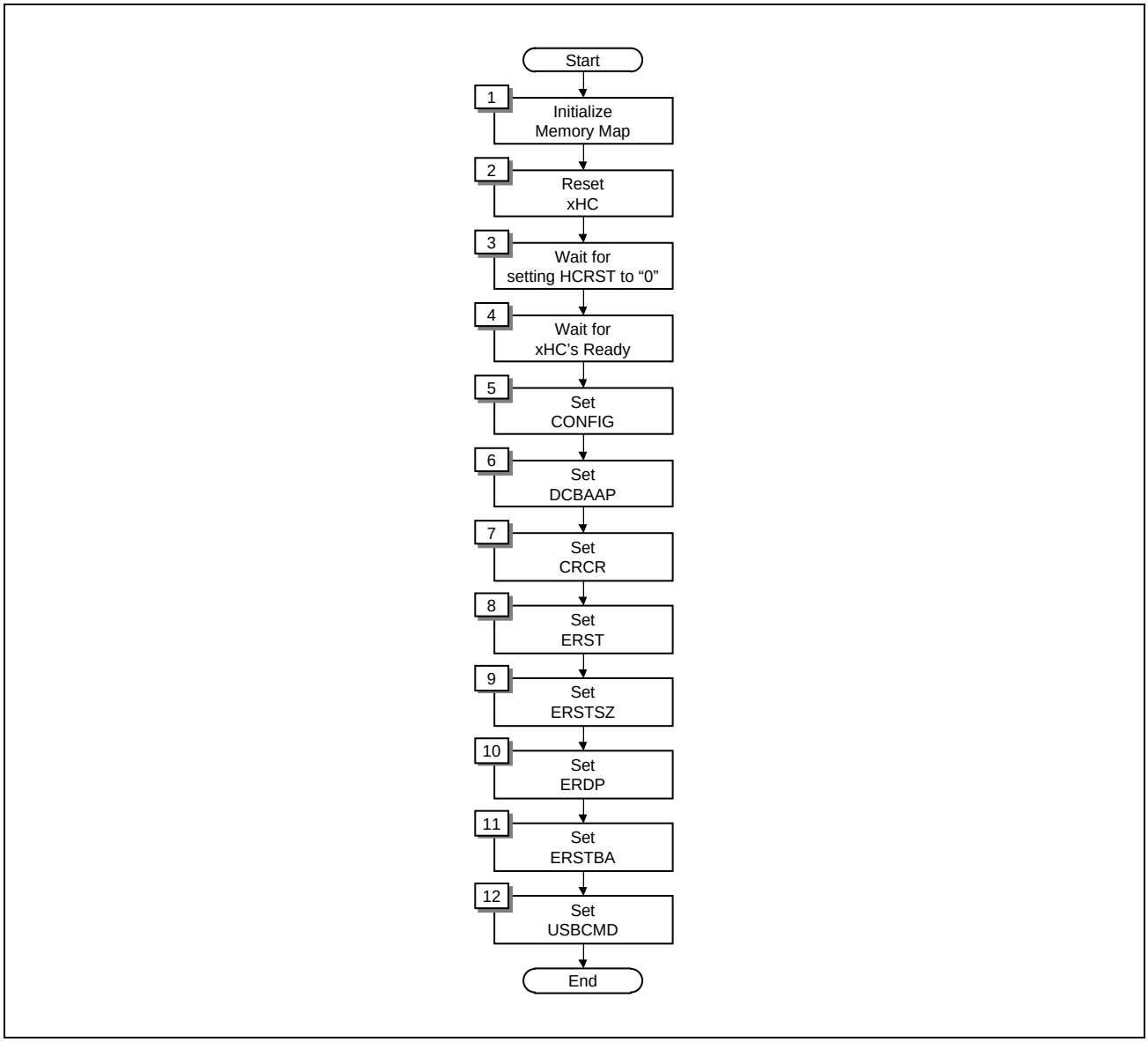


Figure 35.5-4 Initialization Flowchart by xHCD (xHCI Driver)

1. Initialize Memory Map
   xHCD initializes the memory area in the system.
2. Reset xHC
   xHCD confirms that USBSTS.HCH is set to “1b”.
   Then, xHCD resets xHC (the USB3HOST) by setting USBCMD.HCRST to “1b”.
3. Wait for setting HCRST to “0”
   xHCD waits for setting USBCMD.HCRST to “0b”.
4. Wait for xHC’s Ready
   xHCD waits for setting USBSTS.CNR to “0b”.

5. Set CONFIG
   xHCD sets CONFIG.MaxSlotsEn to a valid value.
6. Set DCBAAP
   xHCD sets the “Device Context Base Address Array (DCBAAP)” to a valid value.
7. Set CRCR
   xHCD sets the “Command Ring Control Register (CRCR)” to the Command Ring’s address.
8. Set ERST
   xHCD sets the “Event Ring Segment Table (ERST)” to the Event Ring’s address and size in the system memory.
9. Set ERSTSZ
   xHCD sets the “Event Ring Segment Table Size (ERSTSZ)” to the Event Ring Segment Table’s size.
10. Set ERDP
    xHCD sets the “Event Ring Dequeue Pointer (ERDP) Register” to the Event Ring’s read address.
11. Set ERSTBA
    xHCD sets the “Event Ring Segment Table Base Address (ERSTBA) Register” to the Event Ring Segment Table’s address.
12. Set USBCMD
    xHCD sets USBCMD.INTE to”1b” and also sets USBCMD.R/S to “1b”.

35.5.5.4 Interrupt Flow

(1) “all_int” Interrupt Flow

Figure 35.5-5 shows “all_int” interrupt flow in USB system.

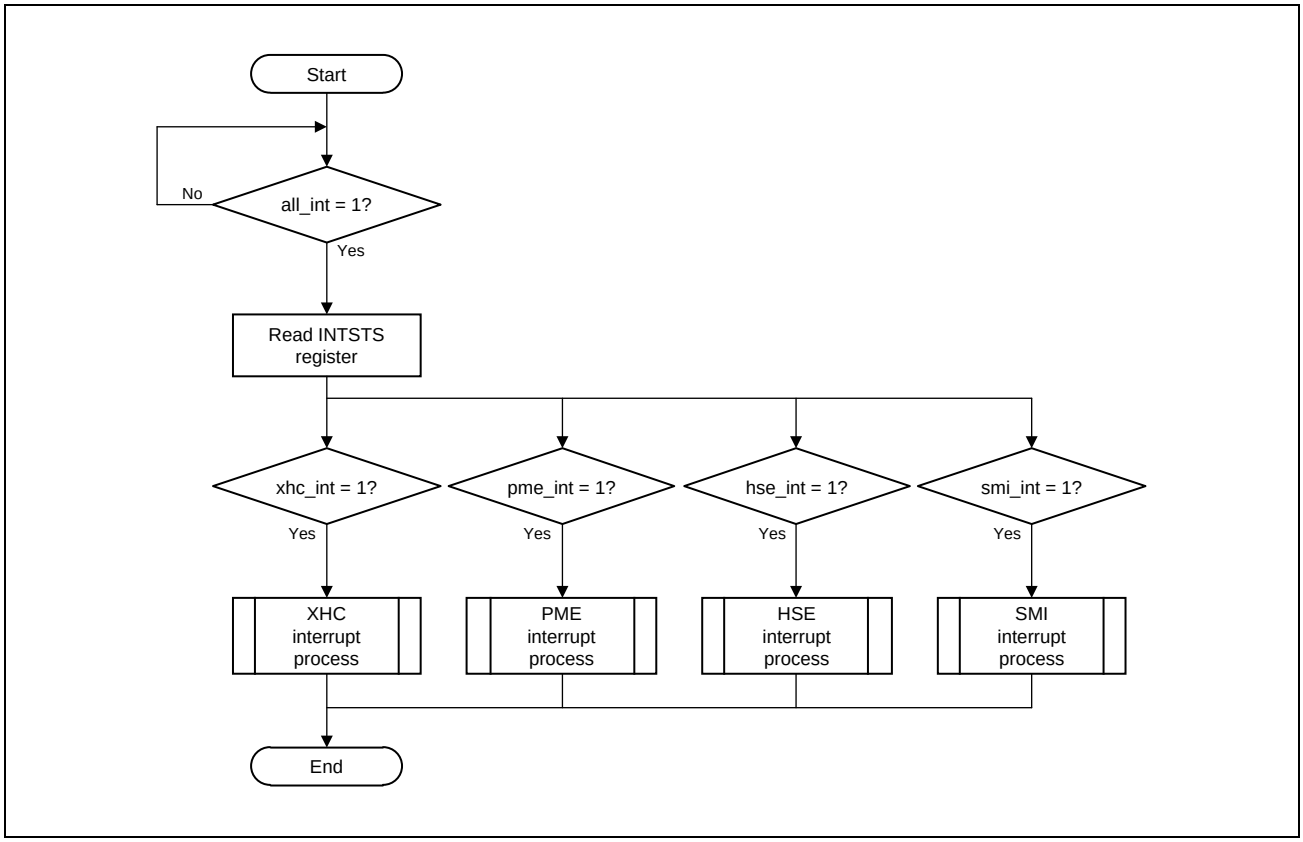


Figure 35.5-5 “all_int” Interrupt Flowchart

(2) XHC Interrupt Flow

Figure 35.5-6 shows “xhc_int” interrupt flow in USB system.

In the case of “CFGSTS1.INTEDGEN = 0”, the notification mode of “xhc_int” is the Level mode.

(This mode is the same as INTA# in PCI System.)

In the case of “CFGSTS1.INTEDGEN = 1”, the notification mode of “xhc_int” is the Pulse mode.

(This is the same as MSI / MSI-X in PCI System.)

In this LSI, “level mode” is selected as default interrupt mode.

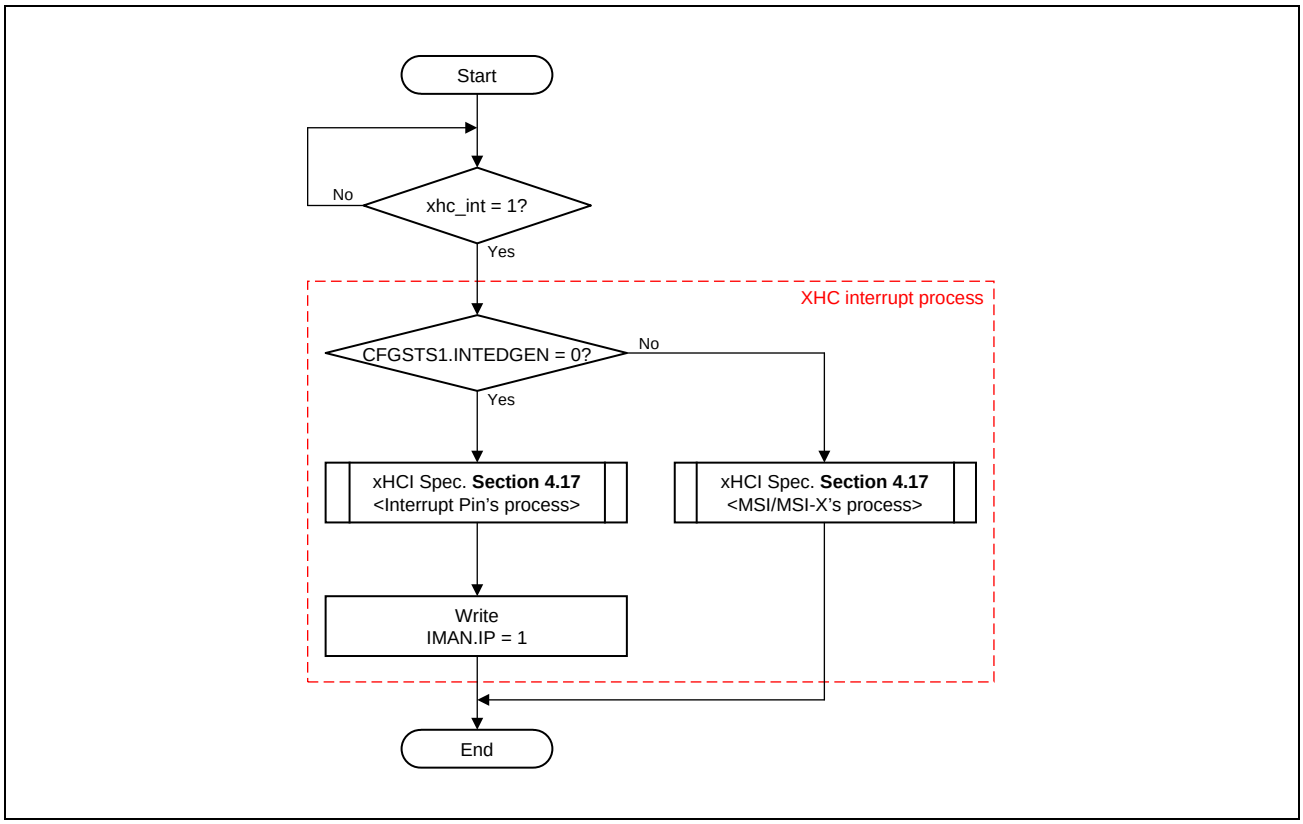


Figure 35.5-6 XHC Interrupt Flowchart

(3) PME Interrupt Flow

Figure 35.5-7 shows “pme_int”’s interrupt flow in USB system.

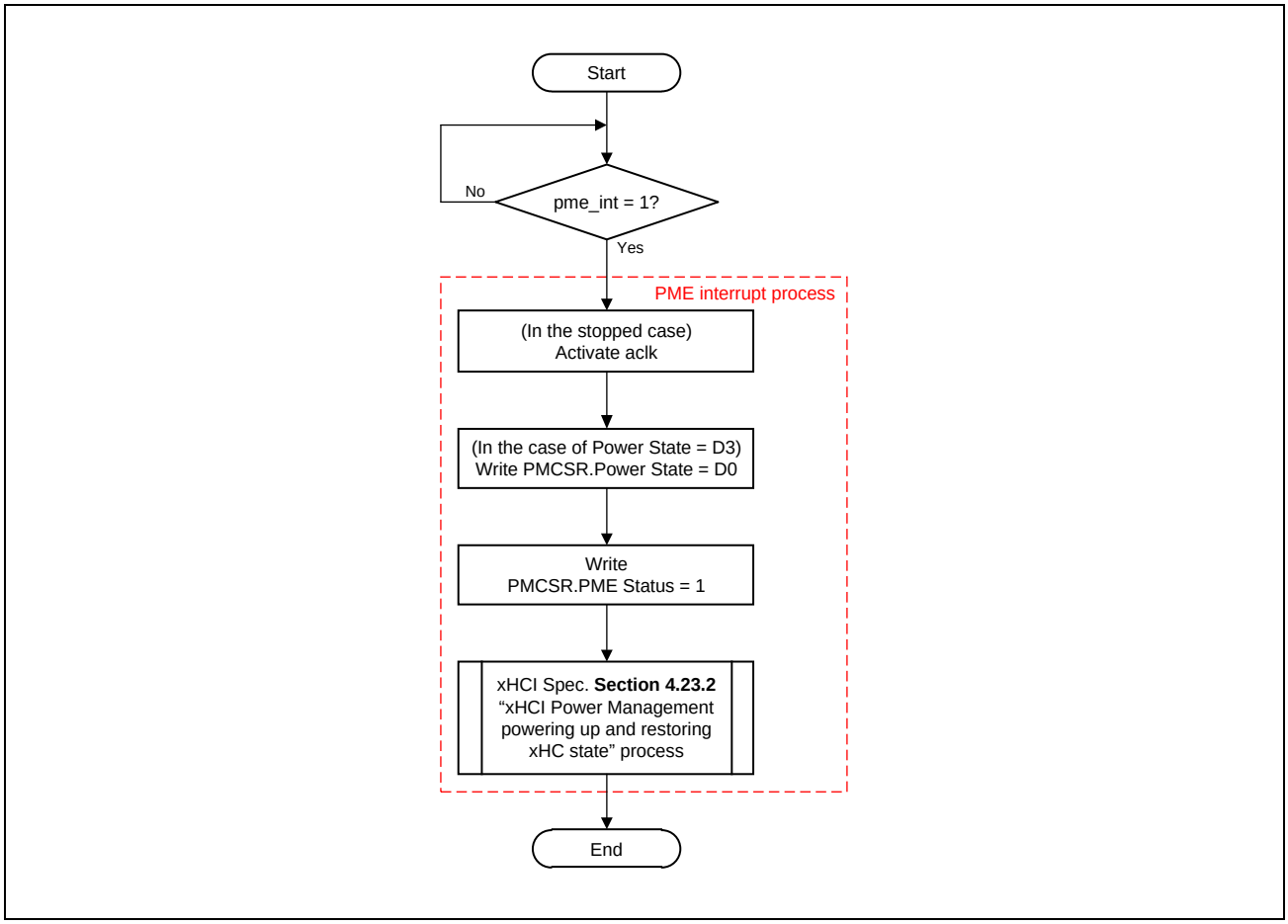


Figure 35.5-7 PME Interrupt Flowchart

(4) HSE Interrupt Flow

Figure 35.5-8 shows “hse_int”’s interrupt flow in USB system.

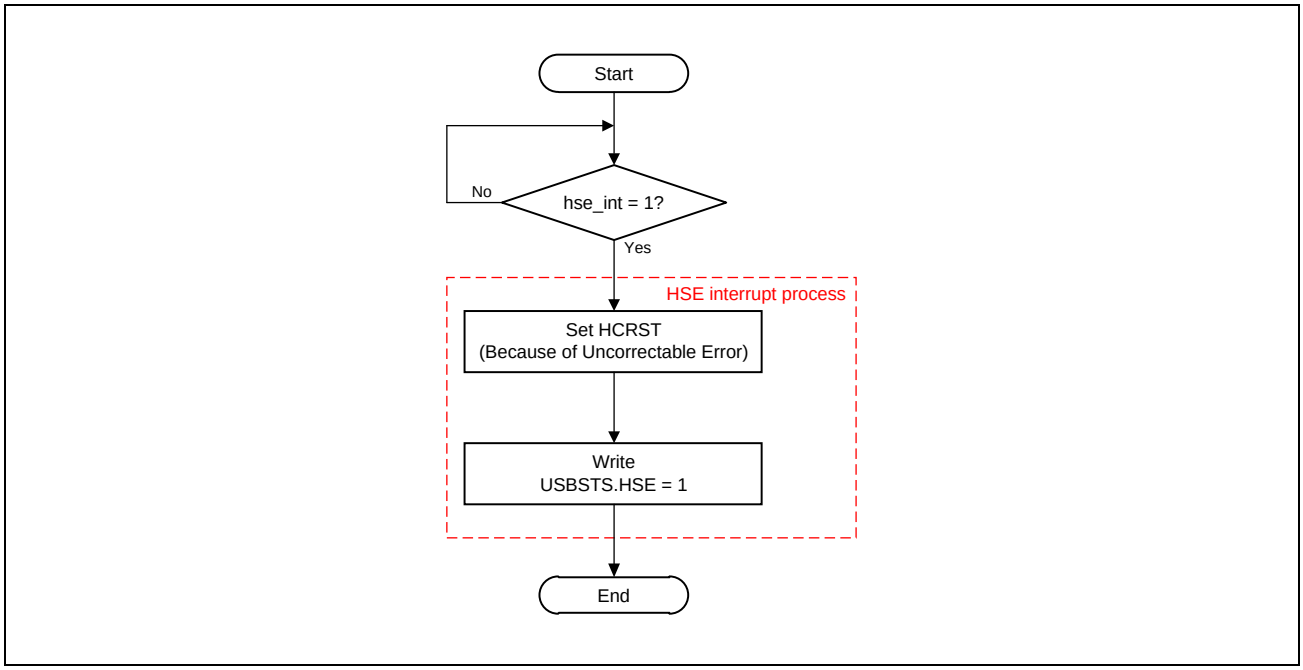


Figure 35.5-8 HSE Interrupt Flowchart

(5) SMI Interrupt Flow

Figure 35.5-9 shows “smi_int”’s interrupt flow in USB system.

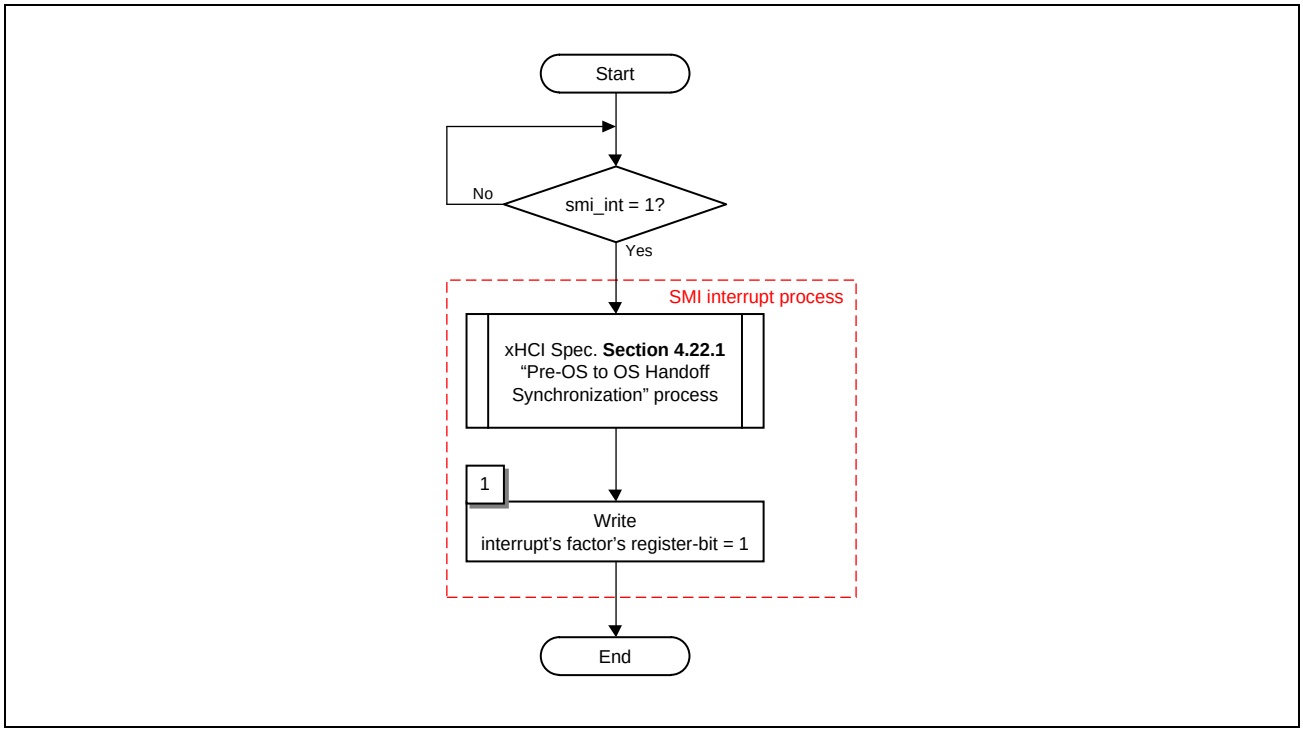


Figure 35.5-9 SMI Interrupt Flowchart

1. Write interrupt’s factor’s register-bit = 1
   If this interrupt’s factor is USBLEGCTLSTS.SBA, write “1” to USBLEGCTLSTS.SBA.
   If this interrupt’s factor is USBLEGCTLSTS.SPC, write “1” to USBLEGCTLSTS.SPC.
   If this interrupt’s factor is USBLEGCTLSTS.SOOC, write “1” to USBLEGCTLSTS.SOOC.
   If this interrupt’s factor is USBLEGCTLSTS.SHSE, write “1” to USBSTS.HSE.
   If this interrupt’s factor is USBLEGCTLSTS.SEI, write “1” to USBSTS.EINT.

35.5.5.5 xHCI Command

Figure 35.5-10 shows an abstract of xHCI Command flow by using the USB3HOST.

Refer to section 4.11.3 “Event TRBs” and section 4.11.4 “Command TRBs”of the xHCI specification for detail information.

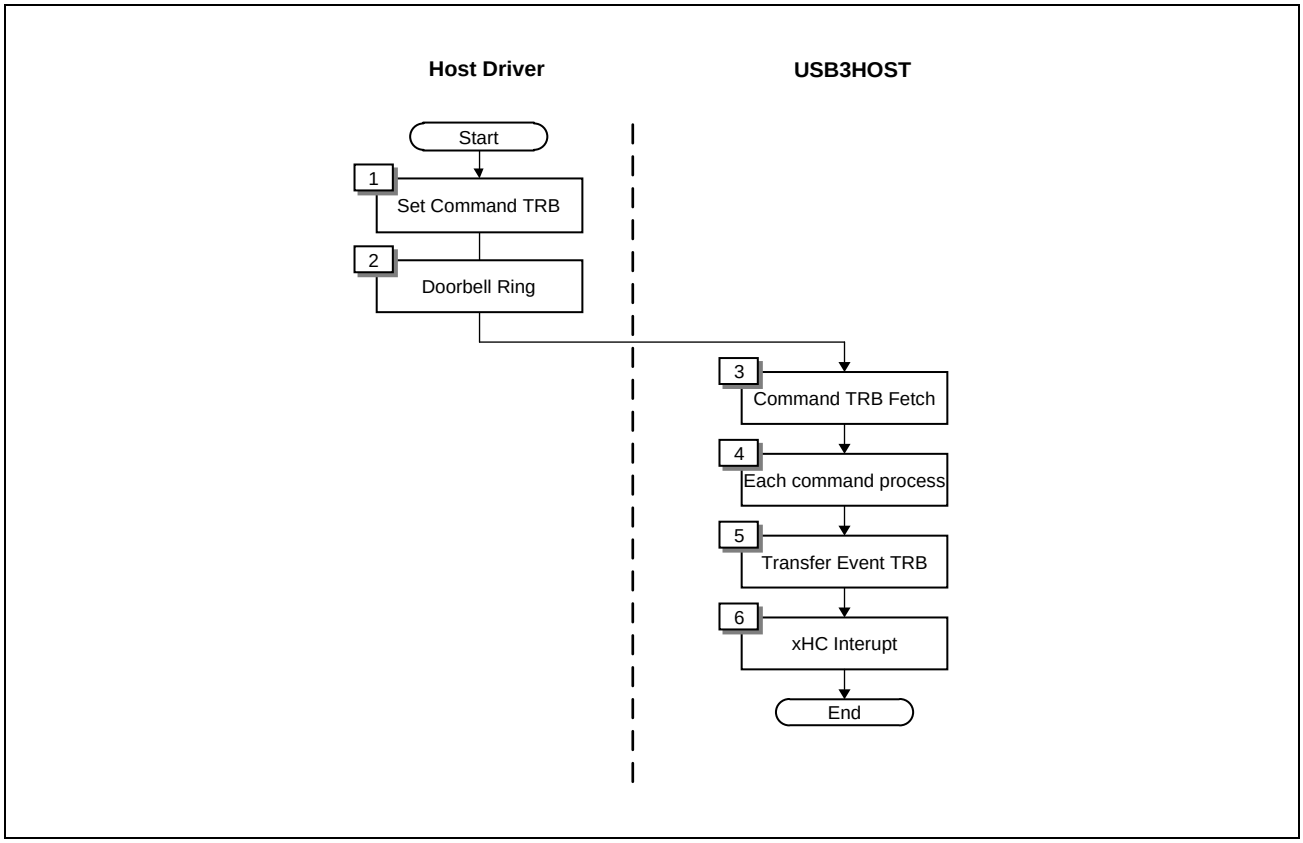


Figure 35.5-10 xHCI Command Flowchart

1. Set Command TRB
   Host driver sets the Command TRB in the Command Ring.
2. Doorbell Ring
   Host driver rings the Doorbell to prepare data for each xHCI command’s process.
3. Command TRB Fetch
   The USB3HOST fetches Command TRB from Command Ring,
4. Each command process
   The USB3HOST decodes that command’s content and executes each command process.
5. Transfer Event TRB
   The USB3HOST writes Event TRB to Event Ring.
6. xHC Interrupt
   The USB3HOST sends the interrupt to the system.

35.5.5.6 Examples of Transactions' Flow

This section describes transactions when the USB3HOST is used.

As examples, Bulk OUT and Bulk IN transactions are described.

The USB3HOST complies with the xHCI Specification.

Refer to section 4.11.2 "Transfer TRBs" and section 4.11.3 "Event TRBs" of the xHCI Specification for detail information.

Bulk OUT Transaction Flow

Bulk OUT transaction flow is shown below.

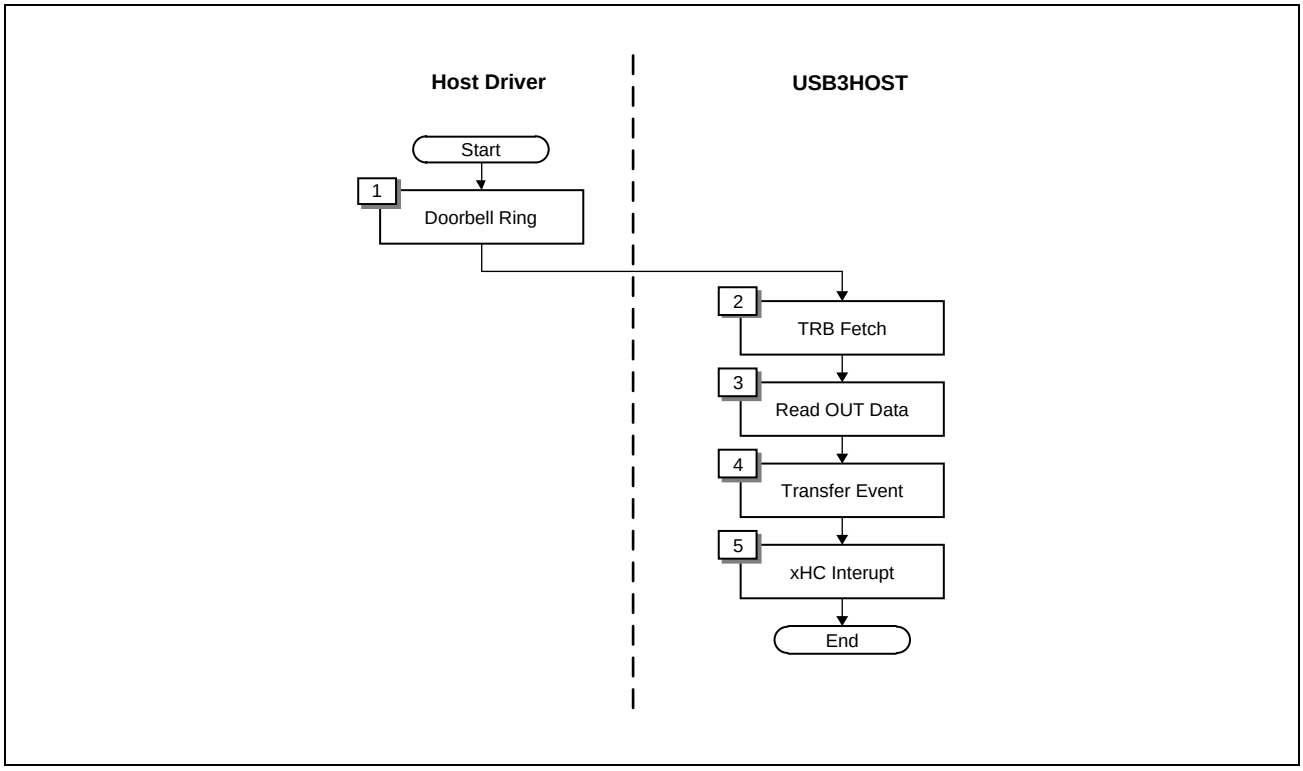


Figure 35.5-11 Example of Bulk OUT Transaction Flowchart

1. Doorbell Ring
   Host Driver rings Doorbell to prepare Transfer Data.
2. TRB Fetch
   The USB3HOST fetches TRB from OUT Transfer Ring,
3. Read OUT Data
   The USB3HOST reads OUT Data from Data Buffer Pointer.
4. Transfer Event
   The USB3HOST writes Transfer Event TRB to Event Ring.
5. xHC Interrupt
   The USB3HOST sends the interrupt to the system.

Bulk IN transaction

Bulk IN transaction flow is shown below.

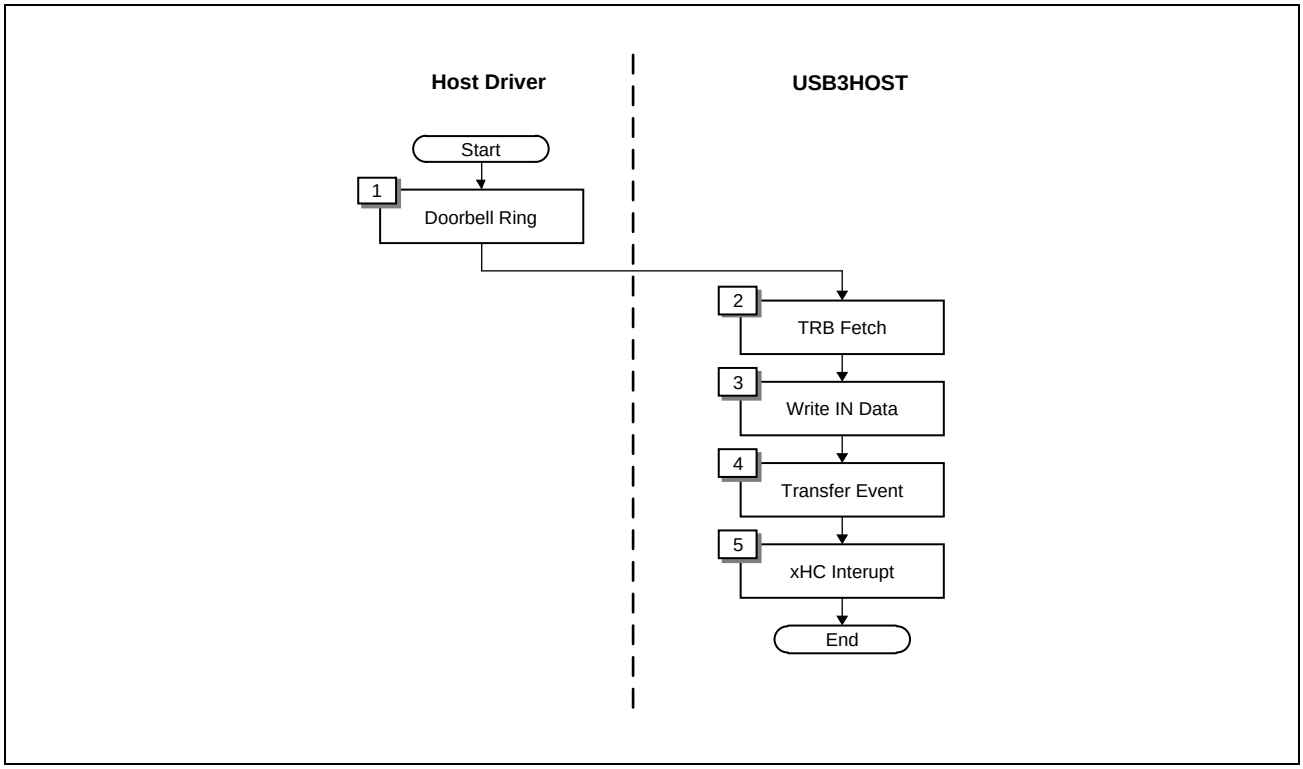


Figure 35.5-12 Example of Bulk IN Transaction Flowchart

1. Doorbell Ring
   Host driver rings Doorbell to prepare Transfer Data.
2. TRB Fetch
   The USB3HOST fetches TRB from OUT Transfer Ring,
3. Write IN Data
   The USB3HOST writes IN Data to Data Buffer Pointer.
4. Transfer Event
   The USB3HOST writes Transfer Event TRB to Event Ring.
5. xHC Interrupt
   The USB3HOST sends the interrupt to the system.

35.5.5.7 Functional Implementation Constraint

The USB3HOST core has functional implementation constraints.

One packet shall be composed of 8TRBs or less.

If one packet is composed of nine or more TRBs, the USB3HOST generates a TRB Error for the higher-level system.

SW shall not set to U3 state before an event of the Force Header Command is completed.

If SW sets to U3 state before this event is completed, the USB3HOST results in undefined xHC behavior.

35.6 USB3.1 Gen1 Peripheral Controller (USB3PERI)

35.6.1 Introduction

USB3.1 Gen1 Peripheral Controller (USB3PERI) is compliant with USB3.1 specification and enables connectivity to USB3.1 system with proven design experiences. It works as USB3.1 device when connected to USB host controller supporting USB3.1, and it works as USB2.0 device when connected to USB host controller supporting not USB3.1 but USB2.0. USB3PERI is compliant with USB2.0 specification as well when it works as USB2.0 device.

USB3PERI contains two function blocks, EPC (endpoint controller) function and AXI-bridge function (as both of master and slave).

35.6.1.1 Features

The features of USB3PERI are as follows.

- *Universal Serial Bus 3.1 Specification Revision 1.0 and ECNs* approved in June 27, 2017
- *Universal Serial Bus Specification Revision 2.0* April 27, 2000
- *USB 2.0 Link Power Management Addendum Engineering Change Notice* to the USB 2.0 specification as of July 16, 2007

(1) USB3.1 Function

- USB3.1 Gen1 super-speed (5 Gbps) transfer
- Stream ID control supported (UASP can be supported)
- Suspend/Resume function
  - Power Management by sending/receiving of link commands (PHY clock stop is supported) is supported.
  - Remote Wakeup request can be transmitted.

(2) USB2.0 Function

- USB2.0 high-speed (480 Mbps) and USB2.0 full-speed (12 Mbps) transfer
- Suspend/Resume function
  - Power Management provided by Suspend/Resume (PHY clock stop is supported) is supported.
  - Remote Wakeup request can be transmitted.
  - Link Power Management (LPM) is supported.

35.6.1.2 Block Diagram

Block components in USB3PERI are shown in **Figure 35.6-1**.

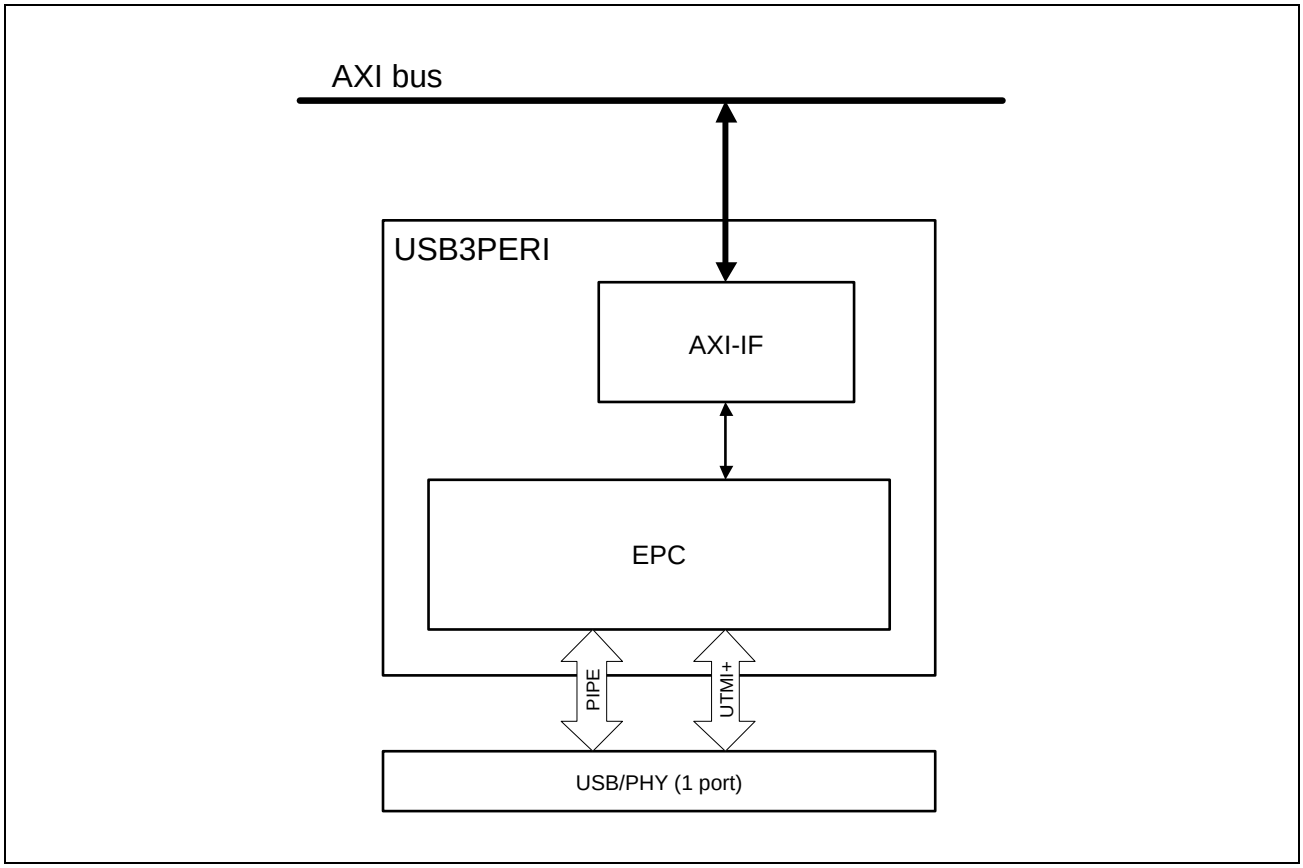


Figure 35.6-1 USB3PERI Block Diagram

35.6.2 Register Map

For the register base address (<USB_S1_base>), see the section of Address Map.

35.6.2.1 USB3PERI Address Space

There are 4 register groups, AXI-IF registers, EPC registers, SSIF registers and PHY registers inside USB3PERI.

PHY registers are mapped to the same address space as EPC registers and SSIF registers, but it can be accessed when AXI_CON.PHY_CTRL = 1.

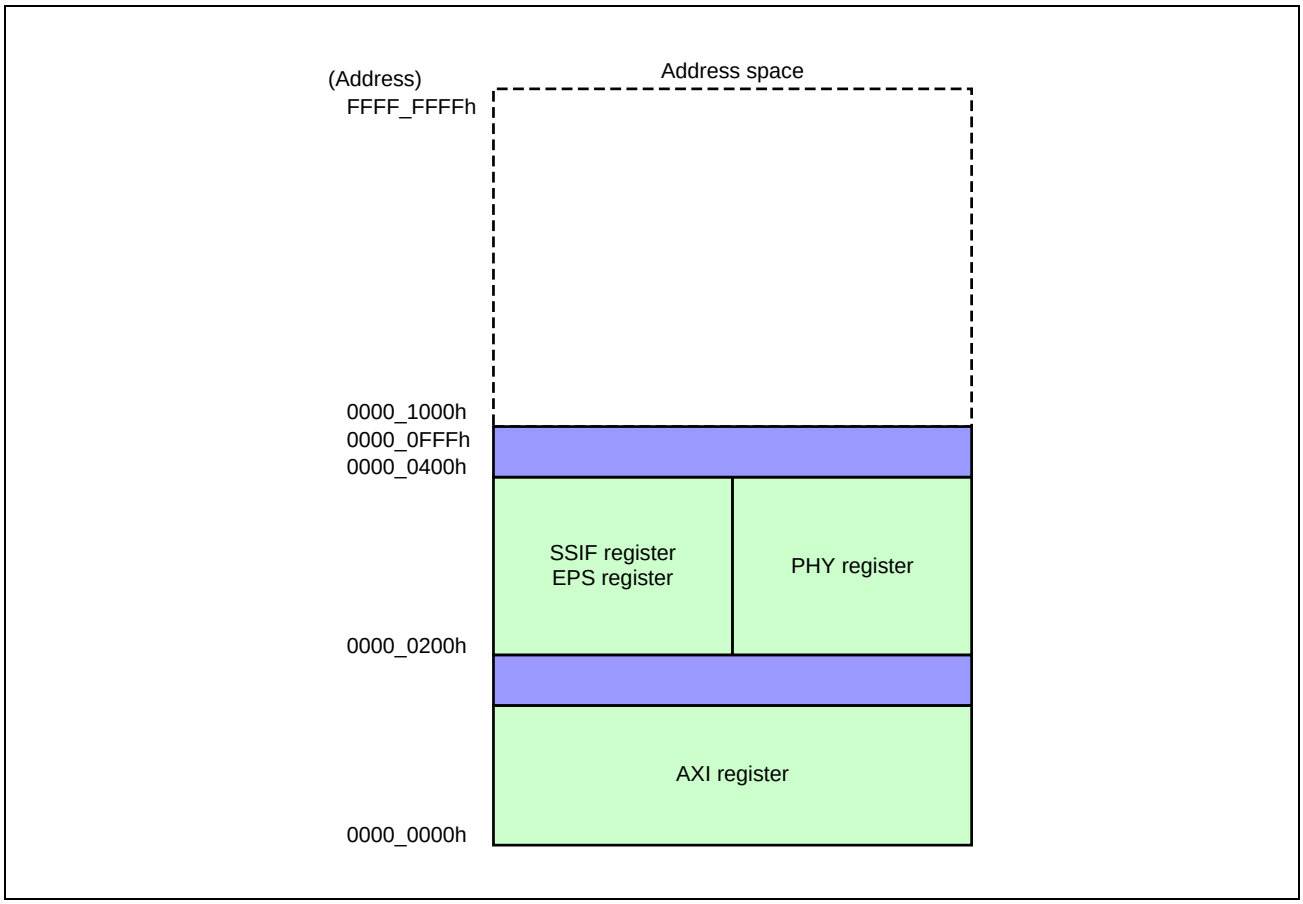


Figure 35.6-2 Register Address Map

35.6.2.2 AXI Register

AXI register groups are selectable from 4 groups or 14 groups, which have information of PRD Table. This unit only supports AXI Register Mode 2 (14 register groups).

(1) AXI Register Mode 2 (14 register groups to have the information of PRD Table)

Table 35.6-1 AXI Register Mode 2 (14 register groups to have the information of PRD Table) List (1/3)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
AXI Control Register (USB_PERI_AXI_CON)								
003h	AXI_RESET	—	—	—	—	—	—	PHY_CTRL
002h	MST_PCACHE [3:0]				—	—	MST_BSIZE [1:0]	
001h	—	MST_ARPROT [2:0]			—	MST_AWPROT [2:0]		
000h	—	—	—	—	—	—	—	MST_WAIT0
AXI Status Register (USB_PERI_AXI_STA)								
007h	AXI_RESET_STA	—	—	—	—	—	—	—
006h	—	—	—	—	—	—	—	—
005h	PRD_DIRO	—	—	—	DMA_PRDNO [3:0]			
004h	PRD_WRITE0	PRD_READ0	DMA_PIPE0 [4:0]					DMA_TRANS0
AXI Interrupt Status Register (USB_PERI_AXI_INT_STA)								
00Bh	DMAINT_STA	EPCINT_STA	PRDEN14_CLR_STA	PRDEN13_CLR_STA	PRDEN12_CLR_STA	PRDEN11_CLR_STA	PRDEN10_CLR_STA	PRDEN9_CLR_STA
00Ah	PRDEN8_CLR_STA	PRDEN7_CLR_STA	PRDEN6_CLR_STA	PRDEN5_CLR_STA	PRDEN4_CLR_STA	PRDEN3_CLR_STA	PRDEN2_CLR_STA	PRDEN1_CLR_STA
009h	—	—	PRDERR0_14_STA	PRDERR0_13_STA	PRDERR0_12_STA	PRDERR0_11_STA	PRDERR0_10_STA	PRDERR0_9_STA
008h	PRDERR0_8_STA	PRDERR0_7_STA	PRDERR0_6_STA	PRDERR0_5_STA	PRDERR0_4_STA	PRDERR0_3_STA	PRDERR0_2_STA	PRDERR0_1_STA
AXI Interrupt Enable Register (USB_PERI_AXI_INT_ENA)								
00Fh	DMAINT_ENA	EPCINT_ENA	PRDEN14_CLR_ENA	PRDEN13_CLR_ENA	PRDEN12_CLR_ENA	PRDEN11_CLR_ENA	PRDEN10_CLR_ENA	PRDEN9_CLR_ENA
00Eh	PRDEN8_CLR_ENA	PRDEN7_CLR_ENA	PRDEN6_CLR_ENA	PRDEN5_CLR_ENA	PRDEN4_CLR_ENA	PRDEN3_CLR_ENA	PRDEN2_CLR_ENA	PRDEN1_CLR_ENA
00Dh	—	—	PRDERR0_14_ENA	PRDERR0_13_ENA	PRDERR0_12_ENA	PRDERR0_11_ENA	PRDERR0_10_ENA	PRDERR0_9_ENA
00Ch	PRDERR0_8_ENA	PRDERR0_7_ENA	PRDERR0_6_ENA	PRDERR0_5_ENA	PRDERR0_4_ENA	PRDERR0_3_ENA	PRDERR0_2_ENA	PRDERR0_1_ENA
DMA Interrupt Status Register (USB_PERI_DMA_INT_STA)								
013h	—	—	—	—	—	—	—	—
012h	—	—	—	—	—	—	—	—
011h	P15_DMACNG_STA	P14_DMACNG_STA	P13_DMACNG_STA	P12_DMACNG_STA	P11_DMACNG_STA	P10_DMACNG_STA	P9_DMACNG_STA	P8_DMACNG_STA
010h	P7_DMACNG_STA	P6_DMACNG_STA	P5_DMACNG_STA	P4_DMACNG_STA	P3_DMACNG_STA	P2_DMACNG_STA	P1_DMACNG_STA	—

Table 35.6-1 AXI Register Mode 2 (14 register groups to have the information of PRD Table) List (2/3)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DMA Interrupt Enable Register (USB_PERI_DMA_INT_ENA)								
017h	—	—	—	—	—	—	—	—
016h	—	—	—	—	—	—	—	—
015h	P15 _DMACNG _ENA	P14 _DMACNG _ENA	P13 _DMACNG _ENA	P12 _DMACNG _ENA	P11 _DMACNG _ENA	P10 _DMACNG _ENA	P9 _DMACNG _ENA	P8 _DMACNG _ENA
014h	P7 _DMACNG _ENA	P6 _DMACNG _ENA	P5 _DMACNG _ENA	P4 _DMACNG _ENA	P3 _DMACNG _ENA	P2 _DMACNG _ENA	P1 _DMACNG _ENA	—
Data Enable Status Register (USB_PERI_DATAEN_STA)								
01Bh	—	—	—	—	—	—	—	—
01Ah	—	—	—	—	—	—	—	—
019h	P15 _DATAEN	P14 _DATAEN	P13 _DATAEN	P12 _DATAEN	P11 _DATAEN	P10 _DATAEN	P9 _DATAEN	P8 _DATAEN
018h	P7 _DATAEN	P6 _DATAEN	P5 _DATAEN	P4 _DATAEN	P3 _DATAEN	P2 _DATAEN	P1 _DATAEN	—
AXI Extended Status Register (USB_PERI_AXI_EXT_STA)								
01Fh	—	—	EXTPRD _EN14_R	EXTPRD _EN13_R	EXTPRD _EN12_R	EXTPRD _EN11_R	EXTPRD _EN10_R	EXTPRD _EN9_R
01Eh	EXTPRD _EN8_R	EXTPRD _EN7_R	EXTPRD _EN6_R	EXTPRD _EN5_R	EXTPRD _EN4_R	EXTPRD _EN3_R	EXTPRD _EN2_R	EXTPRD _EN1_R
01Dh	—	—	PRD _EN14_R	PRD _EN13_R	PRD _EN12_R	PRD _EN11_R	PRD _EN10_R	PRD _EN9_R
01Ch	PRD _EN8_R	PRD _EN7_R	PRD _EN6_R	PRD _EN5_R	PRD _EN4_R	PRD _EN3_R	PRD _EN2_R	PRD _EN1_R
AXI Common Input Register (USB_PERI_AXI_COM_IN)								
023h	COM_IN [31:0]							
022h								
021h								
020h								
AXI Common Output Register (USB_PERI_AXI_COM_OUT)								
027h	COM_OUT [31:0]							
026h								
025h								
024h								
Reserved								
02Bh	—	—	—	—	—	—	—	—
02Ah	—	—	—	—	—	—	—	—
029h	—	—	—	—	—	—	—	—

Table 35.6-1 AXI Register Mode 2 (14 register groups to have the information of PRD Table) List (3/3)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
028h	—	—	—	—	—	—	—	—
Reserved								
02Fh	—	—	—	—	—	—	—	—
02Eh	—	—	—	—	—	—	—	—
02Dh	—	—	—	—	—	—	—	—
02Ch	—	—	—	—	—	—	—	—
DMA Ch0 Control Register n (USB_PERI_DMA_Ch0_CONn)								
ADDC+3 h	—	—	—	—	—	—	—	—
ADDC+2 h	—	—	—	—	—	—	—	—
ADDC+1 h	PIPE_DIRn	—	—	PIPE_NOn [4:0]				
ADDC h	EXTPRD_NOn [3:0]				—	—	EXTPRD_ENn	PRD_ENn
DMA Ch0 PRD Address Register n (USB_PERI_DMA_Ch0_PRD_ADRn)								
ADDP+3 h	PRD_ADRn [31:0]							
ADDP+2 h								
ADDP+1 h								
ADDP h								

Note: n = 1 to 14
ADDC: 020 + (010 × n)
ADDP: 024 + (010 × n)

(a) Initial Value of AXI Register Mode 2 after Reset

Offset Address	Register Name	Initial Value
000h	USB_PERI_AXI_CON	2003_2200h
004h	USB_PERI_AXI_STA	0000_0000h
008h	USB_PERI_AXI_INT_STA	0000_0000h
00Ch	USB_PERI_AXI_INT_ENA	0000_0000h
010h	USB_PERI_DMA_INT_STA	0000_0000h
014h	USB_PERI_DMA_INT_ENA	7FFF_FFFEh
018h	USB_PERI_DATAEN_STA	0000_0000h
01Ch	USB_PERI_AXI_EXT_STA	0000_0000h
020h	USB_PERI_AXI_COM_IN	0000_0000h
024h	USB_PERI_AXI_COM_OUT	The initial value depends on the configuration of core. See **Section 35.6.3.1(1)(j), AXI Common Output Register (AXI_COM_OUT)** for details.
ADDC h	USB_PERI_DMA_Ch0_CONn	0000_0000h
ADDP h	USB_PERI_DMA_Ch0_PRD_ADRn	0000_0000h

Note: n = 1 to 14
ADDC: 020 + (010 × n)
ADDP: 024 + (010 × n)

35.6.2.3 EPC Register

Table 35.6-2 List of EPC Registers (1/9)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
USB Common Control Register (USB_PERI_USB_COM_CON)								
203h	—	—	—	—	—	—	—	CONF
202h	Pn _WDATAIF _NL	Pn _RDATAIF _NL	Pn _LSTTR_PP	—	—	—	SPD_MODE	EP0_EN
201h	—	DEV _ADDR6	DEV _ADDR5	DEV _ADDR4	DEV _ADDR3	DEV _ADDR2	DEV _ADDR1	DEV _ADDR0
200h	—	—	—	—	—	—	RX_ DETECTION	PIPE_CLR
USB20 Control Register (USB_PERI_USB20_CON)								
207h	B2_PUE	—	—	—	—	—	B2 _RSUM_IN	B2 _SUSPEND
206h	B2 _FORCE _HS	B2 _FORCE _FS	—	LPM _DISABLE	LPM _ENABLE1	LPM _ENABLE0	B2 _CONNECT	B2 _PHYRST
205h	—	—	—	—	—	B2 _TSTMOD2	B2 _TSTMOD1	B2 _TSTMOD0
204h	—	—	—	—	—	—	—	B2 _TSTMOD _EN
USB30 Control Register (USB_PERI_USB30_CON)								
20Bh	B3_SIMMOD	—	—	U3 _POWSEL1	U3 _POWSEL0	POWSEL2	POWSEL1	POWSEL0
20Ah	B3 _PLLWAKE	—	—	—	LPS _ENABLE1	LPS _ENABLE0	B3 _CONNECT	B3 _PHYRST
209h	—	—	—	—	—	—	—	—
208h	—	—	—	—	—	POW_SEL _WEN	B3 _HOTRST _CMP	B3_ TP_SEND
Renesas private								
20Fh	—	—	—	—	—	—	—	—
20Eh	—	—	—	—	—	—	—	—
20Dh	—	—	—	—	—	—	—	—
20Ch	—	—	—	—	—	—	—	—
USB Status Register (USB_PERI_USB_STA)								
213h	—	—	—	—	—	—	—	—
212h	—	DEV_ADDR _STA_6	DEV_ADDR _STA_5	DEV_ADDR _STA_4	DEV_ADDR _STA_3	DEV_ADDR _STA_2	DEV_ADDR _STA_1	DEV_ADDR _STA_0
211h	B2 _LSTATE_1	B2 _LSTATE_0	—	B2 _USBRST	B2 _L1SPND _OUT	B2 _L1RSUM _OUT	B2 _SPND _OUT	B2 _RSUM _OUT
210h	—	—	—	—	—	SPEED_1	SPEED_0	VBUS_STA

Table 35.6-2 List of EPC Registers (2/9)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
USB20 Frame No. Register (USB_PERI_USB20_FRAME)								
217h	—	—	—	—	—	—	—	—
216h	—	—	—	—	—	—	—	—
215h	—	—	—	—	—	B2 _FRAME_10	B2 _FRAME_9	B2 _FRAME_8
214h	B2 _FRAME_7	B2 _FRAME_6	B2 _FRAME_5	B2 _FRAME_4	B2 _FRAME_3	B2 _FRAME_2	B2 _FRAME_1	B2 _FRAME_0
Renesas private								
21Bh	—	—	—	—	—	—	—	—
21Ah	—	—	—	—	—	—	—	—
219h	—	—	—	—	—	—	—	—
218h	—	—	—	—	—	—	—	
Reserved								
21Fh	—	—	—	—	—	—	—	—
21Eh	—	—	—	—	—	—	—	—
21Dh	—	—	—	—	—	—	—	—
21Ch	—	—	—	—	—	—	—	—
USB Interrupt Status 1 Register (USB_PERI_USB_INT_STA_1)								
223h	B3_ PLLWKUP _STA	B3 _LUPSUCS _STA	B3 _POLLING _STA	B3 _INACTV _STA	B3 _DISABLE _STA	B3 _VNDTST _STA	B3 _U2INACT _STA	B3 _SETLNK _STA
222h	—	B3 _LNKCNG _STA	B3 _WRMRST _STA	B3 _HOTRST _STA	B3 _PSFAIL _STA	B3 _PSSUCS _STA	B3 _U12REQ _STA	B3 _TPSUCS _STA
221h	—	—	B2 _LPMRCV _STA	B2 _USBRST _STA	B2 _L1SPND _STA	B2 _L1RSUM _STA	B2 _SPND _STA	B2 _RSUM _STA
220h	—	—	—	—	—	—	SPEED_STA	VBUS_CNG _STA
USB Interrupt Status 2 Register (USB_PERI_USB_INT_STA_2)								
227h	—	—	—	—	—	—	—	—
226h	—	—	—	—	—	—	—	—
225h	PIPE15 _INT_STA	PIPE14 _INT_STA	PIPE13 _INT_STA	PIPE12 _INT_STA	PIPE11 _INT_STA	PIPE10 _INT_STA	PIPE9 _INT_STA	PIPE8 _INT_STA
224h	PIPE7 _INT_STA	PIPE6 _INT_STA	PIPE5 _INT_STA	PIPE4 _INT_STA	PIPE3 _INT_STA	PIPE2 _INT_STA	PIPE1 _INT_STA	PIPE0 _INT_STA

Table 35.6-2 List of EPC Registers (3/9)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
USB Interrupt Enable 1 Register (USB_PERI_USB_INT_ENA_1)								
22Bh	B3 _PLLWKUP _ENA	B3 _LUPSUCS _ENA	B3 _POLLING _ENA	B3 _INACTV _ENA	B3 _DISABLE _ENA	B3 _VNDTST _ENA	B3 _U2INACT _ENA	B3 _SETLNK _ENA
22Ah	—	B3 _LNKCNG _ENA	B3 _WRMRST _ENA	B3 _HOTRST _ENA	B3 _PSFAIL _ENA	B3 _PSSUCS _ENA	B3 _U12REQ _ENA	B3 _TPSUCS _ENA
229h	—	—	B2 _LPMRCV _ENA	B2 _USBRST _ENA	B2 _L1SPND _ENA	B2 _L1RSUM _ENA	B2 _SPND _ENA	B2 _RSUM _ENA
228h	—	—	—	—	—	—	SPEED _ENA	VBUS_CNG _ENA
USB Interrupt Enable 2 Register (USB_PERI_USB_INT_ENA_2)								
22Fh	—	—	—	—	—	—	—	—
22Eh	—	—	—	—	—	—	—	—
22Dh	PIPE15 _INT_ENA	PIPE14 _INT_ENA	PIPE13 _INT_ENA	PIPE12 _INT_ENA	PIPE11 _INT_ENA	PIPE10 _INT_ENA	PIPE9 _INT_ENA	PIPE8 _INT_ENA
22Ch	PIPE7 _INT_ENA	PIPE6 _INT_ENA	PIPE5 _INT_ENA	PIPE4 _INT_ENA	PIPE3 _INT_ENA	PIPE2 _INT_ENA	PIPE1 _INT_ENA	PIPE0 _INT_ENA
Setup Data 0 Register (USB_PERI_STUP_DAT_0)								
233h	SETUP_3 [7:0]							
232h	SETUP_2 [7:0]							
231h	SETUP_1 [7:0]							
230h	SETUP_0 [7:0]							
Setup Data 1 Register (USB_PERI_STUP_DAT_1)								
237h	SETUP_7 [7:0]							
236h	SETUP_6 [7:0]							
235h	SETUP_5 [7:0]							
234h	SETUP_4 [7:0]							
Reserved								
23Bh	—	—	—	—	—	—	—	—
23Ah	—	—	—	—	—	—	—	—
239h	—	—	—	—	—	—	—	—
238h	—	—	—	—	—	—	—	—
Reserved								
23Fh	—	—	—	—	—	—	—	—
23Eh	—	—	—	—	—	—	—	—
230h	—	—	—	—	—	—	—	—
23Ch	—	—	—	—	—	—	—	—
USB30 TP Send Data 0 Register (USB_PERI_USB3_TPDAT_0)								
243h	TP_DATA_0 [31:0]							
242h								
241h								
240h								

Table 35.6-2 List of EPC Registers (4/9)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
USB30 TP Send Data 1 Register (USB_PERI_USB3_TPDAT_1)								
247h	TP_DATA_1 [31:0]							
246h								
245h								
244h								
USB30 TP Send Data 2 Register (USB_PERI_USB3_TPDAT_2)								
24Bh	TP_DATA_2 [31:0]							
24Ah								
249h								
248h								
Reserved								
24Fh	—	—	—	—	—	—	—	—
24Eh	—	—	—	—	—	—	—	—
24Dh	—	—	—	—	—	—	—	—
24Ch	—	—	—	—	—	—	—	—
USB20 LPM Status Register (USB_PERI_USB20_LPM_STA)								
253h	—	—	—	—	—	—	—	—
252h	—	—	—	—	—	—	—	—
251h	—	—	—	—	—	—	—	BRW
250h	BESL3	BESL2	BESL1	BESL0	LINKST3	LINKST2	LINKST1	LINKST0
USB30 Vendor Device Test Register (USB_PERI_USB30_VND_DEV)								
257h	—	—	—	—	—	—	—	—
256h	—	—	—	—	—	—	—	—
255h	—	—	—	—	—	—	—	—
254h	VND_DTST_7	VND_DTST_6	VND_DTST_5	VND_DTST_4	VND_DTST_3	VND_DTST_2	VND_DTST_1	VND_DTST_0
USB30 Vendor Defined Data 0 Register (USB_PERI_USB30_VND_DAT_0)								
25Bh	VND_DAT_0 [31:0]							
25Ah								
259h								
258h								
USB30 Vendor Defined Data 1 Register (USB_PERI_USB30_VND_DAT_1)								
25Fh	VND_DAT_1 [31:0]							
25Eh								
25Dh								
25Ch								
EPC Version Register (USB_PERI_USB_VER)								
263h	AXI_MODE	—	—	—	—	—		
262h	—	—	—	PIPE_NUM[4:0]				
261h	MJR_VER [7:0]							
260h	MIN_VER [7:0]							

Table 35.6-2 List of EPC Registers (5/9)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Scratch Pad Register (USB_PERI_USB_SCRATCH)								
267h	SCRATCH [31:0]							
266h								
265h								
264h								
Reserved								
26Bh	—	—	—	—	—	—	—	—
26Ah	—	—	—	—	—	—	—	—
269h	—	—	—	—	—	—	—	—
268h	—	—	—	—	—	—	—	—
Reserved								
26Fh	—	—	—	—	—	—	—	—
26Eh	—	—	—	—	—	—	—	—
26Dh	—	—	—	—	—	—	—	—
26Ch	—	—	—	—	—	—	—	—
Reserved								
273h	—	—	—	—	—	—	—	—
272h	—	—	—	—	—	—	—	—
271h	—	—	—	—	—	—	—	—
270h	—	—	—	—	—	—	—	—
Reserved								
277h	—	—	—	—	—	—	—	—
276h	—	—	—	—	—	—	—	—
275h	—	—	—	—	—	—	—	—
274h	—	—	—	—	—	—	—	—
Reserved								
27Bh	—	—	—	—	—	—	—	—
27Ah	—	—	—	—	—	—	—	—
279h	—	—	—	—	—	—	—	—
278h	—	—	—	—	—	—	—	—
Reserved								
27Fh	—	—	—	—	—	—	—	—
27Eh	—	—	—	—	—	—	—	—
27Dh	—	—	—	—	—	—	—	—
27Ch	—	—	—	—	—	—	—	—
PIPE0 Mode Setting Register (USB_PERI_P0_MOD)								
283h	—	—	—	—	—	—	—	—
282h	—	—	—	—	—	—	—	—
281h	—	—	—	—	—	—	—	—
280h	—	P0_DIR	—	—	—	—	—	—

Table 35.6-2 List of EPC Registers (6/9)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved								
287h	—	—	—	—	—	—	—	—
286h	—	—	—	—	—	—	—	—
285h	—	—	—	—	—	—	—	—
284h	—	—	—	—	—	—	—	—
PIPE0 Control Register (USB_PERI_P0_CON)								
28Bh	—	—	—	—	P0_ST_RES [1:0]		P0_OT_RES [1:0]	
28Ah	—	—	—	—	—	—	P0_IN_RES [1:0]	
289h	—	—	—	—	—	P0_BYTE_EN [1:0]		P0_SEND
288h	P0 _RES_WEN	—	—	—	—	—	P0_BCLR	P0_CLR
PIPE0 Status Register (USB_PERI_P0_STA)								
28Fh	—	—	—	—	—	—	—	—
28Eh	—	—	—	—	—	—	—	—
28Dh	—	—	—	—	—	—	—	—
28Ch	—	—	—	—	P0 _FLOWSTS	P0 _ACKSTS	P0 _SNDSTS	P0 _BUFSTS
PIPE0 Interrupt Status Register (USB_PERI_P0_INT_STA)								
293h	—	—	—	—	—	—	—	—
292h	—	—	—	—	—	P0_STSED _STA	P0_STSST _STA	P0_SETUP _STA
291h	—	—	—	—	—	—	—	P0_RCVNL _STA
290h	P0_ERDY _STA	P0_FLOW _STA	P0_DF_STA	—	—	P0_STALL _STA	P0_NRDY _STA	P0_BFRDY _STA
PIPE0 Interrupt Enable Register (USB_PERI_P0_INT_ENA)								
297h	—	—	—	—	—	—	—	—
296h	—	—	—	—	—	P0_STSED _ENA	P0_STSST _ENA	P0_SETUP _ENA
295h	—	—	—	—	—	—	—	P0_RCVNL _ENA
294h	P0_ERDY _ENA	P0_FLOW _ENA	P0_DF_ENA	—	—	P0_STALL _ENA	P0_NRDY _ENA	P0_BFRDY _ENA
Reserved								
29Bh	—	—	—	—	—	—	—	—
29Ah	—	—	—	—	—	—	—	—
299h	—	—	—	—	—	—	—	—
298h	—	—	—	—	—	—	—	—
Reserved								
29Fh	—	—	—	—	—	—	—	—
29Eh	—	—	—	—	—	—	—	—
29Dh	—	—	—	—	—	—	—	—
29Ch	—	—	—	—	—	—	—	—

Table 35.6-2 List of EPC Registers (7/9)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PIPE0 Length Register (USB_PERI_P0_LNG)								
2A3h	—	—	—	—	—	—	—	—
2A2h	—	—	—	—	—	—	—	—
2A1h	—	—	—	—	—	—	P0_LENGTH [9:8]	
2A0h	P0_LENGTH [7:0]							
PIPE0 Read Register (USB_PERI_P0_READ)								
2A7h	P0_RDATA [31:0]							
2A6h								
2A5h								
2A4h								
PIPE0 Write Register (USB_PERI_P0_WRITE)								
2ABh	P0_WDATA [31:0]							
2AAh								
2A9h								
2A8h								
Reserved								
2AFh	—	—	—	—	—	—	—	—
2AEh	—	—	—	—	—	—	—	—
2ADh	—	—	—	—	—	—	—	—
2ACh	—	—	—	—	—	—	—	—
PIPE Common Setting Register (USB_PERI_PIPE_COM)								
2B3h	—	—	—	—	—	—	—	—
2B2h	—	—	—	—	—	—	—	—
2B1h	—	—	—	—	—	—	—	—
2B0h	—	—	—	PIPE_NUM [4:0]				
Reserved								
2B7h	—	—	—	—	—	—	—	—
2B6h	—	—	—	—	—	—	—	—
2B5h	—	—	—	—	—	—	—	—
2B4h	—	—	—	—	—	—	—	—
Reserved								
2BBh	—	—	—	—	—	—	—	—
2BAh	—	—	—	—	—	—	—	—
2B9h	—	—	—	—	—	—	—	—
2B8h	—	—	—	—	—	—	—	—
Reserved								
2BFh	—	—	—	—	—	—	—	—
2BEh	—	—	—	—	—	—	—	—
2BDh	—	—	—	—	—	—	—	—
2BCh	—	—	—	—	—	—	—	—

Table 35.6-2 List of EPC Registers (8/9)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PIPEn Mode Setting Register (USB_PERI_Pn_MOD)								
2C3h	—	—	—	—	—	—	Pn_ERDY_CON [1:0]	
2C2h	—	—	—	—	—	—	Pn_BOT	Pn_STREAM
2C1h	—	—	—	—	—	—	—	—
2C0h	—	Pn_DIR	Pn_TYPE [1:0]		Pn_EPNUM [3:0]			
PIPEn RAM Mapping Register (USB_PERI_Pn_RAMMAP)								
2C7h	Pn_RAMAREA[2:0]			—	—	Pn_MPKT [10:8]		
2C6h	Pn_MPKT [7:0]							
2C5h	Pn_RAMIF [1:0]		Pn_BASEAD [13:8]					
2C4h	Pn_BASEAD [7:0]							
PIPEn Control Register (USB_PERI_Pn_CON)								
2CBh	Pn_EN	Pn_DATAIF_EN	—	—	—	—	—	Pn_ERDY_SEND
2CAh	—	—	—	—	—	—	Pn_RES [1:0]	
2C9h	—	—	—	—	Pn_LAST	Pn_BYTE_EN [1:0]		Pn_SEND
2C8h	Pn_RES_WEN	—	—	—	—	—	Pn_BCLR	Pn_CLR
PIPEn Status Register (USB_PERI_Pn_STA)								
2CFh	—	—	—	—	—	—	—	—
2CEh	—	—	—	—	—	—	—	—
2CDh	—	—	—	—	—	—	—	—
2CCh	—	—	—	—	Pn_FLOWSTS	Pn_ACKSTS	Pn_SNDSTS	Pn_BUFSTS
PIPEn Interrupt Status Register (USB_PERI_Pn_INT_STA)								
2D3h	—	—	—	—	—	—	—	Pn_CBW_STA
2D2h	—	—	—	Pn_STERR_STA	Pn_STRMX_STA	—	Pn_NSTRM_STA	Pn_PRIME_STA
2D1h	—	—	—	—	—	—	—	Pn_RCVNL_STA
2D0h	Pn_ERDY_STA	Pn_FLOW_STA	Pn_DF_STA	Pn_LSTTR_STA	—	Pn_STALL_STA	Pn_NRDY_STA	Pn_BFRDY_STA
PIPEn Interrupt Enable Register (USB_PERI_Pn_INT_ENA)								
2D7h	—	—	—	—	—	—	—	Pn_CBW_ENA
2D6h	—	—	—	Pn_STERR_ENA	Pn_STRMX_ENA	—	Pn_NSTRM_ENA	Pn_PRIME_ENA
2D5h	—	—	—	—	—	—	—	Pn_RCVNL_ENA
2D4h	Pn_ERDY_ENA	Pn_FLOW_ENA	Pn_DF_ENA	Pn_LSTTR_ENA	—	Pn_STALL_ENA	Pn_NRDY_ENA	Pn_BFRDY_ENA
Reserved								
2DBh	—	—	—	—	—	—	—	—
2DAh	—	—	—	—	—	—	—	—
2D9h	—	—	—	—	—	—	—	—
2D8h	—	—	—	—	—	—	—	—

Table 35.6-2 List of EPC Registers (9/9)

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PIPEn Reserved Packet Register (USB_PERI_Pn_RSVPKT)								
2DFh	—	—	—	—	—	—	—	—
2DEh	—	—	—	—	—	—	—	—
2DDh	—	—	—	—	—	—	—	—
2DCh	—	—	—	Pn_RSVPKT [4:0]				
PIPEn Length Register (USB_PERI_Pn_LNG)								
2E3h	—	—	—	—	—	—	—	—
2E2h	—	—	—	—	—	—	—	—
2E1h	Pn_LENGTH [15:0]							
2E0h								
PIPEn Read Register (USB_PERI_Pn_READ)								
2E7h	Pn_RDATA [31:0]							
2E6h								
2E5h								
2E4h								
PIPEn Write Register (USB_PERI_Pn_WRITE)								
2EBh	Pn_WDATA [31:0]							
2EAh								
2E9h								
2E8h								
Reserved								
2EFh	—	—	—	—	—	—	—	—
2EEh	—	—	—	—	—	—	—	—
2EDh	—	—	—	—	—	—	—	—
2ECh	—	—	—	—	—	—	—	—
PIPEn Stream ID Register (USB_PERI_Pn_STREAMID)								
2F3h	Pn_STREAM_C [15:0]							
2F2h								
2F1h	Pn_STREAM_N [15:0]							
2F0h								
PIPEn NRDY Stream ID Register (USB_PERI_Pn_NRDYSTRM)								
2F7h	—	—	—	—	—	—	—	—
2F6h	—	—	—	—	—	—	—	—
2F5h	Pn_NRDYSTRM [15:0]							
2F4h								
Reserved								
2FBh	—	—	—	—	—	—	—	—
2FAh	—	—	—	—	—	—	—	—
2F9h	—	—	—	—	—	—	—	—
2F8h	—	—	—	—	—	—	—	—

(1) Initial Value of EPC Register after Reset

Offset Address	Register Name	Initial Value
200h	USB_PERI_USB_COM_CON	0000_0000h
204h	USB_PERI_USB20_CON	0000_0000h
208h	USB_PERI_USB30_CON	1000_0000h
20Ch	Renesas private	0000_0000h
210h	USB_PERI_USB_STA	0000_0000h
214h	USB_PERI_USB20_FRAME	0000_0000h
218h	Renesas private	0000_0000h
220h	USB_PERI_USB_INT_STA_1	0000_0000h
224h	USB_PERI_USB_INT_STA_2	0000_0000h
228h	USB_PERI_USB_INT_ENA_1	0000_0000h
22Ch	USB_PERI_USB_INT_ENA_2	0000_0000h
230h	USB_PERI_STUP_DAT_0	0000_0000h
234h	USB_PERI_STUP_DAT_1	0000_0000h
240h	USB_PERI_USB3_TPDAT_0	0000_0000h
244h	USB_PERI_USB3_TPDAT_1	0000_0000h
248h	USB_PERI_USB3_TPDAT_2	0000_0000h
250h	USB_PERI_USB20_LPM_STA	0000_0000h
254h	USB_PERI_USB30_VND_DEV	0000_0000h
258h	USB_PERI_USB30_VND_DAT_0	0000_0000h
25Ch	USB_PERI_USB30_VND_DAT_1	0000_0000h
260h	USB_PERI_USB_VER	The initial value depends on the configuration of core. See **Section 35.6.3.3(19), EPC Version Register (USB_PERI_USB_VER)** for details.
264h	USB_PERI_USB_SCRATCH	0000_0000h
280h	USB_PERI_P0_MOD	0000_0000h
288h	USB_PERI_P0_CON	0000_0000h
28Ch	USB_PERI_P0_STA	0000_0000h
290h	USB_PERI_P0_INT_STA	0000_0000h
294h	USB_PERI_P0_INT_ENA	0000_0000h
2A0h	USB_PERI_P0_LNG	0000_0000h
2A4h	USB_PERI_P0_READ	0000_0000h
2A8h	USB_PERI_P0_WRITE	0000_0000h
2B0h	USB_PERI_PIPE_COM	0000_0000h
2C0h	USB_PERI_Pn_MOD	0000_0000h
2C4h	USB_PERI_Pn_RAMMAP	0000_0000h
2C8h	USB_PERI_Pn_CON	0000_0000h
2CCh	USB_PERI_Pn_STA	0000_0000h
2D0h	USB_PERI_Pn_INT_STA	0000_0000h
2D4h	USB_PERI_Pn_INT_ENA	0000_0000h
2DCh	USB_PERI_Pn_RSVPKT	0000_0000h
2E0h	USB_PERI_Pn_LNG	0000_0000h
2E4h	USB_PERI_Pn_READ	0000_0000h
2E8h	USB_PERI_Pn_WRITE	0000_0000h
2F0h	USB_PERI_Pn_STREAMID	0000_0000h
2F4h	USB_PERI_Pn_NRDYSTRM	0000_0000h

35.6.2.4 SSIF Register (a part of EPC Register)

Table 35.6-3 SSIF Register (a part of EPC Register) List

Offset Address	bit31	bit30	bit29	bit28	bit27	bit26	bit25	bit24
	bit23	bit22	bit21	bit20	bit19	bit18	bit17	bit16
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Port Status and Control Register (USB_PERI_PORTSC)								
303h	—	—	—	—	—	—	—	—
302h	—	—	—	—	—	—	—	LWS
301h	—	—	—	—	—	—	—	PLS [3]
300h	PLS [2:0]			—	—	—	—	—
Port PM Status and Control Register (USB_PERI_PORTPMSC)								
307h	—	—	—	—	—	—	—	—
306h	—	—	—	—	—	—	—	FLA
305h	U2_TIMEOUT [7:0]							
304h	U1_TIMEOUT [7:0]							
Port Link Information Register (USB_PERI_PORTLI)								
30Bh	—	—	—	—	—	—	—	—
30Ah	—	—	—	—	—	—	—	—
309h	LINK_ERCNT [15:0]							
308h								
SSIF Command Register (USB_PERI_SSIFCMD)								
343h	—	—	—	—	—	—	—	—
342h	—	—	—	—	—	—	—	—
341h	—	—	—	—	—	—	SSIF_URES [1:0]	
340h	SSIF_UDIR [1:0]		SSIF_UREQ [1:0]		—	—	—	—
Reserved								
377h	—	—	—	—	—	—	—	—
376h	—	—	—	—	—	—	—	—
375h	—	—	—	—	—	—	—	—
374h	—	—	—	—	—	—	—	—
Reserved								
37Bh	—	—	—	—	—	—	—	—
37Ah	—	—	—	—	—	—	—	—
379h	—	—	—	—	—	—	—	—
378h	—	—	—	—	—	—	—	—
SSIF Link Setting 3 Register (USB_PERI_SSIFLINKSET3)								
37Fh	—	—	—	—	—	—	—	—
37Eh	—	—	—	—	—	—	—	—
37Dh	—	—	—	—	—	—	—	—
37Ch	—	—	—	—	SSIF_NUM_RDET [3:0]			
SSIF Link Setting 4 Register (USB_PERI_SSIFLINKSET4)								
383h	—	—	—	—	—	—	—	—
382h	—	SSIF_TXMGN [2:0]			—	—	—	—
381h	—	—	—	—	—	—	SSIF_DEEMPH [1:0]	
380h	—	—	—	SSIF _SWING	—	—	—	SSIF_SCRD

(1) Initial Value of SSIF Register after Reset

Offset Address	Register Name	Initial Value
300h	USB_PERI_PORTSC	0000_0080h
304h	USB_PERI_PORTPMSC	0000_0000h
308h	USB_PERI_PORTLI	0000_0000h
340h	USB_PERI_SSIFCMD	030C_30C0h
37Ch	USB_PERI_SSIFLINKSET3	0760_0AC8h
380h	USB_PERI_SSIFLINKSET4	0000_FF00h

35.6.3 Register Descriptions

The function description of each register is given below.

The prefix (USB_PERI_) of the register names is omitted in the register descriptions and the field descriptions in this section.

35.6.3.1 AXI Register

(1) AXI Register Mode 2 (14 register groups to have the information of PRD Table)

(a) AXI Control Register (AXI_CON)

This register is used to control the basic functions of AXI-IF.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0000h

Initial Value: 2003_2200h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	AXI_RESET	—	—	—	—	—	—	PHY_CTRL	MST_PCACHE[3:0]				—	—	MST_BSIZE[1:0]	
Initial Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W	W	RW	RW	W	R	R	R	RW	RW	RW	RW	RW	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	MST_ARPROT[2:0]			—	MST_AWPROT[2:0]			—	—	—	—	—	—	—	MST_WAIT0
Initial Value	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	R	R	R	R	R	R	RW

Table 35.6-4 AXI_CON Register Contents (1/2)

Bit Position	Bit Name	Description
31	AXI_RESET	This bit is used to reset AXI Master IF. AXI Master block is reset when 1 is written to this bit. Read value from this bit is always 0. All circuits in AXI-IF except for the contents of registers and Slave interface are reset with this bit. PRD_ENx bits in all DMA_Ch0_CONx registers shall be set to “0” before setting this bit.
30	Renesas Private	The initial value of this bit is 0. This bit can be read and written but it is not allowed to change the value of this bit. Only 0 is allowed as the value to be written.
29	Renesas Private	The initial value of this bit is 1. This bit can be read and written but it is not allowed to change the value of this bit. Only 1 is allowed as the value to be written.
28	Renesas Private	This bit is writable and write-only bit but is not allowed to write 1 to this bit. Only 0 is allowed as the value to be written.
27 to 25	Reserved	This field is read only. The value of this field is 000b.

Table 35.6-4 AXI_CON Register Contents (2/2)

Bit Position	Bit Name	Description
24	PHY_CTRL	When 1 is set to this bit, the access to USB3.1-PHY control register is enabled. EPC register and USB3.1-PHY control register share the same address space. This bit is used to select which register is currently accessed. Make sure to set this bit back to 0 after the access to USB3.1-PHY control register is completed. 1b: Access to USB3.1-PHY control register is selected 0b: Access to EPC register is selected
23 to 20	MST_PCACHE	This field specifies CACHE signal (MARCACHE or MAWCACHE) for access to read or write back PRD table in AXI Master IF. The function of this field to select CACHE signal is not applied to DMA transfer. For DMA transfer, the setting information in the descriptor of PRD table is applied. It is prohibited to change the setting of this field during DMA transfer.
19 to 18	Reserved	This field is read only. The value of this field is 0h.
17 to 16	MST_BSIZE	This field specifies burst size (AxSIZE) in AXI Master IF. It is prohibited to change the setting of this field during DMA transfer. When it is required to change the setting of this field during DMA transfer, write 1 to MST_WAIT0 and make sure that DMA transfer is stopped by checking DMA_TRANS0. 00b: 1 byte (AxSIZE = 000b) 01b: 2 bytes (AxSIZE = 001b) 10b: 4 bytes (AxSIZE = 010b) 11b: 8 bytes (AxSIZE = 011b)
15	Reserved	This bit is read only the value of this bit is 0.
14 to 12	MST_ARPROT	This field specifies the protection type for read access in AXI Master IF. Master IF outputs protection type according to the setting of this field, but it makes no difference in internal operation. It is prohibited to change the setting of this field during DMA transfer. [0] 1b: Special Privileged Access 0b: Normal Access [1] 1b: Non-Secure Access 0b: Secure Access [2] 1b: Command Access 0b: Data Access
11	Reserved	This field is read only. The value of this bit is 0.
10 to 8	MST_AWPROT	This field specifies the protection type for write access in AXI Master IF. Master IF outputs protection type according to the setting of this field, but it makes no difference in internal operation. It is prohibited to change the setting of this field during DMA transfer. [0] 1b: Special Privileged Access 0b: Normal Access [1] 1b: Non-Secure Access 0b: Secure Access [2] 1b: Command Access 0b: Data Access
7 to 1	Reserved	This field is read only. The value of this field is 0h.
0	MST_WAIT0	This bit is used to suspend all DMA transfers being executed in AXI Master IF. When 1 is written to this bit, AXI_STA.DMA_TRANS0 shows 1 until all transfers are suspended. Wait till AXI_STA.DMA_TRANS0 changes to 0 to make sure all DMA transfers are suspended. It is required to set this bit back to 0 when resume of the transfer is requested. 1b: Transfer suspended 0b: Normal operation

(b) AXI Status Register (AXI_STA)

This register shows the status of AXI-IF.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0004h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	AXI_RESET_STA	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PRD_DIR0	—	—	—	DMA_PRDNO[3:0]				PRD_WRITE0	PRD_READ0	DMA_PIPE0[4:0]					DMA_TRANS0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-5 AXI_STA Register Contents

Bit Position	Bit Name	Description
31	AXI_RESET_STA	This bit indicates the reset status of AXI-IF. 1b: Reset is being executed. 0b: Reset is not being executed.
30 to 16	Reserved	This field is read only. The value of this field is 0000h.
15	PRD_DIR0	This bit indicates the direction of transfer in the PIPE which is currently in progress at AXI Master I/F when DMA_TRANS0 = 1. If DMA transfer is not being executed (DMA_TRANS0 = 0), this bit indicates the direction of last transfer of the PIPE.
14 to 12	Reserved	This field is read only. The value of this field is 0h.
11 to 8	DMA_PRDNO	This field indicates the index of PRD table for which DMA transfer is in progress when DMA_TRANS = 1. It indicates the index of last PRD table that was used for DMA transfer when DMA_TRANS0 = 0.
7	PRD_WRITE0	This bit indicates that write access to PRD table for PIPE indexed by DMA_PIPE0 is in progress. 1b: Writing to PRD table is in progress 0b: Writing to PRD table is not in progress
6	PRD_READ0	This bit indicates that read access from PRD Table for PIPE indexed by DMA_PIPE0 is in progress. 1b: Reading from PRD table is in progress 0b: Reading from PRD table is not in progress
5 to 1	DMA_PIPE0	This field indicates the index of PIPE that is currently being used for DMA transfer in AXI Master IF when DMA_TRANS0 = 1. It indicates the index of last PIPE which was used for DMA transfer when DMA_TRANS0 = 0.
0	DMA_TRANS0	This bit indicates that DMA transfer is in progress at AXI Master IF. 1b: DMA transfer is in progress 0b: DMA transfer is not in progress

(c) AXI Interrupt Status Register (AXI_INT_STA)

This register shows the interrupt statuses in AXI-IF.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0008h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DMAINT_STA	EPCINT_STA	PRDEN14_CLR_STA	PRDEN13_CLR_STA	PRDEN12_CLR_STA	PRDEN11_CLR_STA	PRDEN10_CLR_STA	PRDEN9_CLR_STA	PRDEN8_CLR_STA	PRDEN7_CLR_STA	PRDEN6_CLR_STA	PRDEN5_CLR_STA	PRDEN4_CLR_STA	PRDEN3_CLR_STA	PRDEN2_CLR_STA	PRDEN1_CLR_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PRDER R0-14 STA	PRDER R0-13 STA	PRDER R0-12 STA	PRDER R0-11 STA	PRDER R0-10 STA	PRDER R0-9 STA	PRDER R0-8 STA	PRDER R0-7 STA	PRDER R0-6 STA	PRDER R0-5 STA	PRDER R0-4 STA	PRDER R0-3 STA	PRDER R0-2 STA	PRDER R0-1 STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1

Table 35.6-6 AXI_INT_STA Register Contents (1/5)

Bit Position	Bit Name	Description
31	DMAINT_STA	This bit indicates that an interrupt due to the status change during DMA transfer occurs. The interrupt with AXI_INT_DMA is asserted when this bit is set. Refer to DMA_INT_STA register to know which PIPE completes DMA transfer. This bit is reset to 0 when all factors in DMA_INT_STA register are cleared. 1b: interrupt of DMA transfer completion occurs 0b: No interrupt of DMA transfer completion occurs
30	EPCINT_STA	This bit indicates that an interrupt of EPC_INTR_USB occurs. Refer to USB_INT_STA_1 register and USB_INT_STA_2 register to know which factor occurs. This bit is reset to 0 when all factors in USB_INT_STA_1 register and USB_INT_STA_2 register are cleared. 1b: interrupt fromEPC_INTR_USB occurs 0b: No interrupt from EPC_INTR_USB occurs
29	PRDEN14_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON14 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.
28	PRDEN13_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON13 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.
27	PRDEN12_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON12 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.

Table 35.6-6 AXI_INT_STA Register Contents (2/5)

Bit Position	Bit Name	Description
26	PRDEN11_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON11 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.
25	PRDEN10_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON10 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.
24	PRDEN9_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON9 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.
23	PRDEN8_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON8 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.
22	PRDEN7_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON7 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.
21	PRDEN6_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON6 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.
20	PRDEN5_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON5 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.
19	PRDEN4_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON4 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.
18	PRDEN3_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON3 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.
17	PRDEN2_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON2 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.

Table 35.6-6 AXI_INT_STA Register Contents (3/5)

Bit Position	Bit Name	Description
16	PRDEN1_CLR_STA	This bit indicates that PRD_EN in DMA_CH0_CON1 is cleared by hardware. The interrupt with AXI_INT_SYS is asserted when this bit is set. The interrupt might be asserted when the condition to clear PRD_EN by hardware is satisfied even if PRD_EN has already been cleared in the table. This bit is cleared when 1 is written to it.
15 to 14	Reserved	This field is read only. The value of this field is 0h.
13	PRDERR0-14_STA	This bit indicates that the information of PRD table in DMA_CH0_CON14 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON14 register and DMA_Ch0_PRD_ADR14 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The cases this bit is set are as follows. - Target PIPE has conflicted settings. - Wrong PIPE_DIR or PIPE_NO is assigned. - PRD table does not follow the correct format. - An error occurs during transfer. The interrupt with AXI_INT_ERR is asserted when this bit is set.
12	PRDERR0-13_STA	This bit indicates that the information of PRD table in DMA_CH0_CON13 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON13 register and DMA_Ch0_PRD_ADR13 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The cases this bit is set are as follows. - Target PIPE has conflicted settings. - Wrong PIPE_DIR or PIPE_NO is assigned. - PRD table does not follow the correct format. - An error occurs during transfer. The interrupt with AXI_INT_ERR is asserted when this bit is set.
11	PRDERR0-12_STA	This bit indicates that the information of PRD table in DMA_CH0_CON12 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON12 register and DMA_Ch0_PRD_ADR12 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The cases this bit is set are as follows. - Target PIPE has conflicted settings. - Wrong PIPE_DIR or PIPE_NO is assigned. - PRD table does not follow the correct format. - An error occurs during transfer. The interrupt with AXI_INT_ERR is asserted when this bit is set.
10	PRDERR0-11_STA	This bit indicates that the information of PRD table in DMA_CH0_CON11 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON11 register and DMA_Ch0_PRD_ADR11 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The cases this bit is set are as follows. - Target PIPE has conflicted settings. - Wrong PIPE_DIR or PIPE_NO is assigned. - PRD table does not follow the correct format. - An error occurs during transfer. The interrupt with AXI_INT_ERR is asserted when this bit is set.

Table 35.6-6 AXI_INT_STA Register Contents (4/5)

Bit Position	Bit Name	Description
9	PRDERR0-10_STA	This bit indicates that the information of PRD table in DMA_CH0_CON10 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON10 register and DMA_Ch0_PRD_ADR10 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The cases this bit is set are as follows. - Target PIPE has conflicted settings. - Wrong PIPE_DIR or PIPE_NO is assigned. - PRD table does not follow the correct format. - An error occurs during transfer. The interrupt with AXI_INT_ERR is asserted when this bit is set.
8	PRDERR0-9_STA	This bit indicates that the information of PRD table in DMA_CH0_CON9 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON9 register and DMA_Ch0_PRD_ADR9 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The cases this bit is set are as follows. - Target PIPE has conflicted settings. - Wrong PIPE_DIR or PIPE_NO is assigned. - PRD table does not follow the correct format. - An error occurs during transfer. The interrupt with AXI_INT_ERR is asserted when this bit is set.
7	PRDERR0-8_STA	This bit indicates that the information of PRD table in DMA_CH0_CON8 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON8 register and DMA_Ch0_PRD_ADR8 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The cases this bit is set are as follows. - Target PIPE has conflicted settings. - Wrong PIPE_DIR or PIPE_NO is assigned. - PRD table does not follow the correct format. - An error occurs during transfer. The interrupt with AXI_INT_ERR is asserted when this bit is set.
6	PRDERR0-7_STA	This bit indicates that the information of PRD table in DMA_CH0_CON7 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON7 register and DMA_Ch0_PRD_ADR7 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The cases this bit is set are as follows. - Target PIPE has conflicted settings. - Wrong PIPE_DIR or PIPE_NO is assigned. - PRD table does not follow the correct format. - An error occurs during transfer. The interrupt with AXI_INT_ERR is asserted when this bit is set.
5	PRDERR0-6_STA	This bit indicates that the information of PRD table in DMA_CH0_CON6 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON6 register and DMA_Ch0_PRD_ADR6 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The cases this bit is set are as follows. - Target PIPE has conflicted settings. - Wrong PIPE_DIR or PIPE_NO is assigned. - PRD table does not follow the correct format. - An error occurs during transfer. The interrupt with AXI_INT_ERR is asserted when this bit is set.

Table 35.6-6 AXI_INT_STA Register Contents (5/5)

Bit Position	Bit Name	Description
4	PRDERR0-5_STA	This bit indicates that the information of PRD table in DMA_CH0_CON5 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON5 register and DMA_Ch0_PRD_ADR5 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The cases this bit is set are as follows. - Target PIPE has conflicted settings. - Wrong PIPE_DIR or PIPE_NO is assigned. - PRD table does not follow the correct format. - An error occurs during transfer. The interrupt with AXI_INT_ERR is asserted when this bit is set.
3	PRDERR0-4_STA	This bit indicates that the information of PRD table in DMA_CH0_CON4 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON4 register and DMA_Ch0_PRD_ADR4 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The cases this bit is set are as follows. - Target PIPE has conflicted settings. - Wrong PIPE_DIR or PIPE_NO is assigned. - PRD table doesn't follow the correct format. - An error occurs during transfer. The interrupt with AXI_INT_ERR is asserted when this bit is set.
2	PRDERR0-3_STA	This bit indicates that the information of PRD table in DMA_CH0_CON3 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON3 register and DMA_Ch0_PRD_ADR3 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The interrupt with AXI_INT_ERR is asserted when this bit is set.
1	PRDERR0-2_STA	This bit indicates that the information of PRD table in DMA_CH0_CON2 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON2 register and DMA_Ch0_PRD_ADR2 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The interrupt with AXI_INT_ERR is asserted when this bit is set.
0	PRDERR0-1_STA	This bit indicates that the information of PRD table in DMA_CH0_CON1 is wrong. This bit is set to 1 when it is determined that PRD table used for DMA_Ch0_CON1 register and DMA_Ch0_PRD_ADR1 register has a wrong information. In that case, the PRD table is disabled. This bit is cleared when 1 is written to it. The interrupt with AXI_INT_ERR is asserted when this bit is set.

(d) AXI Interrupt Enable Register (AXI_INT_ENA)

This register is used to enable interrupts from AXI-IF.

Access Size: 32 bits

Address(es): <USB_S1_base> + 000Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DMAINT_ENA	EPCINT_ENA	PRDEN14_CLR_ENA	PRDEN13_CLR_ENA	PRDEN12_CLR_ENA	PRDEN11_CLR_ENA	PRDEN10_CLR_ENA	PRDEN9_CLR_ENA	PRDEN8_CLR_ENA	PRDEN7_CLR_ENA	PRDEN6_CLR_ENA	PRDEN5_CLR_ENA	PRDEN4_CLR_ENA	PRDEN3_CLR_ENA	PRDEN2_CLR_ENA	PRDEN1_CLR_ENA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PRDER R0-14_ ENA	PRDER R0-13_ ENA	PRDER R0-12_ ENA	PRDER R0-11_ ENA	PRDER R0-10_ ENA	PRDER R0-9_ ENA	PRDER R0-8_ ENA	PRDER R0-7_ ENA	PRDER R0-6_ ENA	PRDER R0-5_ ENA	PRDER R0-4_ ENA	PRDER R0-3_ ENA	PRDER R0-2_ ENA	PRDER R0-1_ ENA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.6-7 AXI_INT_ENA Register Contents (1/3)

Bit Position	Bit Name	Description
31	DMAINT_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.DMAINT_STA. 1b: An interrupt due to AXI_INT_STA.DMAINT_STA is enabled. 0b: An interrupt due to AXI_INT_STA.DMAINT_STA is disabled.
30	EPCINT_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.EPCINT_STA. 1b: An interrupt due to AXI_INT_STA.EPCINT_STA is enabled. 0b: An interrupt due to AXI_INT_STA.EPCINT_STA is disabled.
29	PRDEN14_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN14_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN14_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN14_CLR_STA is disabled.
28	PRDEN13_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN13_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN13_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN13_CLR_STA is disabled.
27	PRDEN12_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN12_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN12_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN12_CLR_STA is disabled.
26	PRDEN11_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN11_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN11_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN11_CLR_STA is disabled.
25	PRDEN10_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN10_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN10_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN10_CLR_STA is disabled.
24	PRDEN9_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN9_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN9_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN9_CLR_STA is disabled.
23	PRDEN8_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN8_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN8_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN8_CLR_STA is disabled.
22	PRDEN7_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN7_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN7_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN7_CLR_STA is disabled.

Table 35.6-7 AXI_INT_ENA Register Contents (2/3)

Bit Position	Bit Name	Description
21	PRDEN6_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN6_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN6_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN6_CLR_STA is disabled.
20	PRDEN5_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN5_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN5_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN5_CLR_STA is disabled.
19	PRDEN4_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN4_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN4_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN4_CLR_STA is disabled.
18	PRDEN3_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN3_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN3_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN3_CLR_STA is disabled.
17	PRDEN2_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN2_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN2_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN2_CLR_STA is disabled.
16	PRDEN1_CLR_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDEN1_CLR_STA. 1b: An interrupt due to AXI_INT_STA.PRDEN1_CLR_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDEN1_CLR_STA is disabled.
15 to 14	Reserved	This field is read only. The value of this field is 0h.
13	PRDERR0-14_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-14_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-14_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-14_STA is disabled.
12	PRDERR0-13_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-13_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-13_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-13_STA is disabled.
11	PRDERR0-12_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-12_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-12_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-12_STA is disabled.
10	PRDERR0-11_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-11_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-11_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-11_STA is disabled.
9	PRDERR0-10_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-10_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-10_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-10_STA is disabled.
8	PRDERR0-9_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-9_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-9_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-9_STA is disabled.
7	PRDERR0-8_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-8_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-8_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-8_STA is disabled.
6	PRDERR0-7_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-7_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-7_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-7_STA is disabled.
5	PRDERR0-6_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-6_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-6_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-6_STA is disabled.
4	PRDERR0-5_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-5_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-5_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-5_STA is disabled.

Table 35.6-7 AXI_INT_ENA Register Contents (3/3)

Bit Position	Bit Name	Description
3	PRDERR0-4_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-4_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-4_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-4_STA is disabled.
2	PRDERR0-3_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-3_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-3_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-3_STA is disabled.
1	PRDERR0-2_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-2_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-2_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-2_STA is disabled.
0	PRDERR0-1_ENA	This bit is used to enable the interrupt due to AXI_INT_STA.PRDERR0-1_STA. 1b: An interrupt due to AXI_INT_STA.PRDERR0-1_STA is enabled. 0b: An interrupt due to AXI_INT_STA.PRDERR0-1_STA is disabled.

(e) DMA Interrupt Status Register (DMA_INT_STA)

This register shows the interrupt statuses of DMA transfers with each PIPE.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0010h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	P15_DMACNG_STA	P14_DMACNG_STA	P13_DMACNG_STA	P12_DMACNG_STA	P11_DMACNG_STA	P10_DMACNG_STA	P9_DMACNG_STA	P8_DMACNG_STA	P7_DMACNG_STA	P6_DMACNG_STA	P5_DMACNG_STA	P4_DMACNG_STA	P3_DMACNG_STA	P2_DMACNG_STA	P1_DMACNG_STA	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	R

Table 35.6-8 DMA_INT_STA Register Contents (1/2)

Bit Position	Bit Name	Description
31	Reserved	This bit is read only. The value of this bit is 0.
30 to 16	Reserved	These bits are read as 0b. The write value should be 0b.
15	P15_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE15 is changed. This bit is cleared when 1 is written to it.
14	P14_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE14 is changed. This bit is cleared when 1 is written to it.
13	P13_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE13 is changed. This bit is cleared when 1 is written to it.
12	P12_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE12 is changed. This bit is cleared when 1 is written to it.
11	P11_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE11 is changed. This bit is cleared when 1 is written to it.
10	P10_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE10 is changed. This bit is cleared when 1 is written to it.
9	P9_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE9 is changed. This bit is cleared when 1 is written to it.
8	P8_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE8 is changed. This bit is cleared when 1 is written to it.
7	P7_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE7 is changed. This bit is cleared when 1 is written to it.
6	P6_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE6 is changed. This bit is cleared when 1 is written to it.
5	P5_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE5 is changed. This bit is cleared when 1 is written to it.
4	P4_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE4 is changed. This bit is cleared when 1 is written to it.
3	P3_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE3 is changed. This bit is cleared when 1 is written to it.

Table 35.6-8 DMA_INT_STA Register Contents (2/2)

Bit Position	Bit Name	Description
2	P2_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE2 is changed. This bit is cleared when 1 is written to it.
1	P1_DMACNG_STA	This bit indicates that the status of DMA transfer with PIPE1 is changed. This bit is cleared when 1 is written to it.
0	Reserved	This bit is read only. The value of this bit is 0.

(f) DMA Interrupt Enable Register (DMA_INT_ENA)

This register is used to enable interrupts of DMA Transfers with each PIPEs.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0014h

Initial Value: 7FFF_FFFEh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	P15_DMACNG_ENA	P14_DMACNG_ENA	P13_DMACNG_ENA	P12_DMACNG_ENA	P11_DMACNG_ENA	P10_DMACNG_ENA	P9_DMACNG_ENA	P8_DMACNG_ENA	P7_DMACNG_ENA	P6_DMACNG_ENA	P5_DMACNG_ENA	P4_DMACNG_ENA	P3_DMACNG_ENA	P2_DMACNG_ENA	P1_DMACNG_ENA	—
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R

Table 35.6-9 DMA_INT_ENA Register Contents (1/2)

Bit Position	Bit Name	Description
31	Reserved	This bit is read only. The value of this bit is 0.
30 to 16	Reserved	These bits are read as 1b. The write value should be 1b.
15	P15_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P15_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P15_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P15_DMACNG_STA is disabled.
14	P14_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P14_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P14_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P14_DMACNG_STA is disabled.
13	P13_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P13_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P13_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P13_DMACNG_STA is disabled.
12	P12_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P12_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P12_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P12_DMACNG_STA is disabled.
11	P11_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P11_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P11_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P11_DMACNG_STA is disabled.
10	P10_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P10_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P10_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P10_DMACNG_STA is disabled.
9	P9_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P9_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P9_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P9_DMACNG_STA is disabled.
8	P8_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P8_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P8_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P8_DMACNG_STA is disabled.
7	P7_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P7_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P7_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P7_DMACNG_STA is disabled.

Table 35.6-9 DMA_INT_ENA Register Contents (2/2)

Bit Position	Bit Name	Description
6	P6_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P6_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P6_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P6_DMACNG_STA is disabled.
5	P5_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P5_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P5_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P5_DMACNG_STA is disabled.
4	P4_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P4_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P4_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P4_DMACNG_STA is disabled.
3	P3_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P3_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P3_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P3_DMACNG_STA is disabled.
2	P2_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P2_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P2_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P2_DMACNG_STA is disabled.
1	P1_DMACNG_ENA	This bit is used to enable the interrupt due to DMA_INT_STA.P1_DMACNG_STA. 1b: An interrupt due to DMA_INT_STA.P1_DMACNG_STA is enabled. 0b: An interrupt due to DMA_INT_STA.P1_DMACNG_STA is disabled.
0	Reserved	This bit is read only. The value of this bit is 0.

(g) Data Enable Status Register (DATAEN STA)

This register shows the statuses of PIPEn (n = 1 to 15).

Access Size: 32 bits

Address(es): <USB_S1_base> + 0018h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	P15_DATAEN	P14_DATAEN	P13_DATAEN	P12_DATAEN	P11_DATAEN	P10_DATAEN	P9_DATAEN	P8_DATAEN	P7_DATAEN	P6_DATAEN	P5_DATAEN	P4_DATAEN	P3_DATAEN	P2_DATAEN	P1_DATAEN	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-10 DATAEN STA Register Contents (1/2)

Bit Position	Bit Name	Description
31	Reserved	This bit is read only. The value of this bit is 0.
30 to 16	Reserved	This field is read only. The value of this field is 0000h.
15	P15_ DATAEN	This bit shows the status of PIPE15. 1b: PIPE15 is ready for data transfer. 0b: PIPE15 is not ready for data transfer.
14	P14_ DATAEN	This bit shows the status of PIPE14. 1b: PIPE14 is ready for data transfer. 0b: PIPE14 is not ready for data transfer.
13	P13_ DATAEN	This bit shows the status of PIPE13. 1b: PIPE13 is ready for data transfer. 0b: PIPE13 is not ready for data transfer.
12	P12_ DATAEN	This bit shows the status of PIPE12. 1b: PIPE12 is ready for data transfer. 0b: PIPE12 is not ready for data transfer.
11	P11_ DATAEN	This bit shows the status of PIPE11. 1b: PIPE11 is ready for data transfer. 0b: PIPE11 is not ready for data transfer.
10	P10_ DATAEN	This bit shows the status of PIPE10. 1b: PIPE10 is ready for data transfer. 0b: PIPE10 is not ready for data transfer.
9	P9_ DATAEN	This bit shows the status of PIPE9. 1b: PIPE9 is ready for data transfer. 0b: PIPE9 is not ready for data transfer.
8	P8_ DATAEN	This bit shows the status of PIPE8. 1b: PIPE8 is ready for data transfer. 0b: PIPE8 is not ready for data transfer.
7	P7_ DATAEN	This bit shows the status of PIPE7. 1b: PIPE7 is ready for data transfer. 0b: PIPE7 is not ready for data transfer.

Table 35.6-10 DATAEN STA Register Contents (2/2)

Bit Position	Bit Name	Description
6	P6_ DATAEN	This bit shows the status of PIPE6. 1b: PIPE6 is ready for data transfer. 0b: PIPE6 is not ready for data transfer.
5	P5_ DATAEN	This bit shows the status of PIPE5. 1b: PIPE5 is ready for data transfer. 0b: PIPE5 is not ready for data transfer.
4	P4_ DATAEN	This bit shows the status of PIPE4. 1b: PIPE4 is ready for data transfer. 0b: PIPE4 is not ready for data transfer.
3	P3_ DATAEN	This bit shows the status of PIPE3. 1b: PIPE3 is ready for data transfer. 0b: PIPE3 is not ready for data transfer.
2	P2_ DATAEN	This bit shows the status of PIPE2. 1b: PIPE2 is ready for data transfer. 0b: PIPE2 is not ready for data transfer.
1	P1_ DATAEN	This bit shows the status of PIPE1. 1b: PIPE1 is ready for data transfer. 0b: PIPE1 is not ready for data transfer.
0	Reserved	This bit is read only. The value of this bit is 0.

(h) AXI Extended Status Register (AXI_EXT_STA)

This register shows the extended status of AXI-IF.

Access Size: 32 bits

Address(es): <USB_S1_base> + 001Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	EXTPRD_EN14_R	EXTPRD_EN13_R	EXTPRD_EN12_R	EXTPRD_EN11_R	EXTPRD_EN10_R	EXTPRD_EN9_R	EXTPRD_EN8_R	EXTPRD_EN7_R	EXTPRD_EN6_R	EXTPRD_EN5_R	EXTPRD_EN4_R	EXTPRD_EN3_R	EXTPRD_EN2_R	EXTPRD_EN1_R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PRD_EN14_R	PRD_EN13_R	PRD_EN12_R	PRD_EN11_R	PRD_EN10_R	PRD_EN9_R	PRD_EN8_R	PRD_EN7_R	PRD_EN6_R	PRD_EN5_R	PRD_EN4_R	PRD_EN3_R	PRD_EN2_R	PRD_EN1_R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-11 AXI_EXT_STA Register Contents (1/3)

Bit Position	Bit Name	Description
31 to 30	Reserved	This field is read only. The value of this field is 0h.
29	EXTPRD_EN14_R	This bit indicates the status of EXTPRD_EN14. This bit shows the same value as that of bit1 (EXTPRD_EN14) in DMA_CH0_CON14 register, but is used as read-only bit.
28	EXTPRD_EN13_R	This bit indicates the status of EXTPRD_EN13. This bit shows the same value as that of bit1 (EXTPRD_EN13) in DMA_CH0_CON13 register, but is used as read-only bit.
27	EXTPRD_EN12_R	This bit indicates the status of EXTPRD_EN12. This bit shows the same value as that of bit1 (EXTPRD_EN12) in DMA_CH0_CON12 register, but is used as read-only bit.
26	EXTPRD_EN11_R	This bit indicates the status of EXTPRD_EN11. This bit shows the same value as that of bit1 (EXTPRD_EN11) in DMA_CH0_CON11 register, but is used as read-only bit.
25	EXTPRD_EN10_R	This bit indicates the status of EXTPRD_EN10. This bit shows the same value as that of bit1 (EXTPRD_EN10) in DMA_CH0_CON10 register, but is used as read-only bit.
24	EXTPRD_EN9_R	This bit indicates the status of EXTPRD_EN9. This bit shows the same value as that of bit1 (EXTPRD_EN9) in DMA_CH0_CON9 register, but is used as read-only bit.
23	EXTPRD_EN8_R	This bit indicates the status of EXTPRD_EN8. This bit shows the same value as that of bit1 (EXTPRD_EN8) in DMA_CH0_CON8 register, but is used as read-only bit.
22	EXTPRD_EN7_R	This bit indicates the status of EXTPRD_EN7. This bit shows the same value as that of bit1 (EXTPRD_EN7) in DMA_CH0_CON7 register, but is used as read-only bit.
21	EXTPRD_EN6_R	This bit indicates the status of EXTPRD_EN6. This bit shows the same value as that of bit1 (EXTPRD_EN6) in DMA_CH0_CON6 register, but is used as read-only bit.
20	EXTPRD_EN5_R	This bit indicates the status of EXTPRD_EN5. This bit shows the same value as that of bit1 (EXTPRD_EN5) in DMA_CH0_CON5 register, but is used as read-only bit.

Table 35.6-11 AXI_EXT_STA Register Contents (2/3)

Bit Position	Bit Name	Description
19	EXTPRD_EN4_R	This bit indicates the status of EXTPRD_EN4. This bit shows the same value as that of bit1 (EXTPRD_EN4) in DMA_CH0_CON4 register, but is used as read-only bit.
18	EXTPRD_EN3_R	This bit indicates the status of EXTPRD_EN3. This bit shows the same value as that of bit1 (EXTPRD_EN3) in DMA_CH0_CON3 register, but is used as read-only bit.
17	EXTPRD_EN2_R	This bit indicates the status of EXTPRD_EN2. This bit shows the same value as that of bit1 (EXTPRD_EN2) in DMA_CH0_CON2 register, but is used as read-only bit.
16	EXTPRD_EN1_R	This bit indicates the status of EXTPRD_EN1. This bit shows the same value as that of bit1 (EXTPRD_EN1) in DMA_CH0_CON1 register, but is used as read-only bit.
15 to 14	Reserved	This field is read only. The value of this field is 0h.
13	PRD_EN14_R	This bit indicates the status of PRD_EN14. This bit shows the same value as that of bit0 (PRD_EN14) in DMA_CH0_CON14 register, but is used as read-only bit.
12	PRD_EN13_R	This bit indicates the status of PRD_EN13. This bit shows the same value as that of bit0 (PRD_EN13) in DMA_CH0_CON13 register, but is used as read-only bit.
11	PRD_EN12_R	This bit indicates the status of PRD_EN12. This bit shows the same value as that of bit0 (PRD_EN12) in DMA_CH0_CON12 register, but is used as read-only bit.
10	PRD_EN11_R	This bit indicates the status of PRD_EN11. This bit shows the same value as that of bit0 (PRD_EN11) in DMA_CH0_CON11 register, but is used as read-only bit.
9	PRD_EN10_R	This bit indicates the status of PRD_EN10. This bit shows the same value as that of bit0 (PRD_EN10) in DMA_CH0_CON10 register, but it is used as read-only bit.
8	PRD_EN9_R	This bit indicates the status of PRD_EN9. This bit shows the same value as that of bit0 (PRD_EN9) in DMA_CH0_CON9 register, but it is used as read-only bit.
7	PRD_EN8_R	This bit indicates the status of PRD_EN8. This bit shows the same value as that of bit0 (PRD_EN8) in DMA_CH0_CON8 register, but is used as read-only bit.
6	PRD_EN7_R	This bit indicates the status of PRD_EN7. This bit shows the same value as that of bit0 (PRD_EN7) in DMA_CH0_CON7 register, but is used as read-only bit.
5	PRD_EN6_R	This bit indicates the status of PRD_EN6. This bit shows the same value as that of bit0 (PRD_EN6) in DMA_CH0_CON6 register, but it is used as read-only bit.
4	PRD_EN5_R	This bit indicates the status of PRD_EN5. This bit shows the same value as that of bit0 (PRD_EN5) in DMA_CH0_CON5 register, but it is used as read-only bit.
3	PRD_EN4_R	This bit indicates the status of PRD_EN4. This bit shows the same value as that of bit0 (PRD_EN4) in DMA_CH0_CON4 register, but is used as read-only bit.
2	PRD_EN3_R	This bit indicates the status of PRD_EN3. This bit shows the same value as that of bit0 (PRD_EN3) in DMA_CH0_CON3 register, but is used as read-only bit.
1	PRD_EN2_R	This bit indicates the status of PRD_EN2. This bit shows the same value as that of bit0 (PRD_EN2) in DMA_CH0_CON2 register, but it is used as read-only bit.

Table 35.6-11 AXI_EXT_STA Register Contents (3/3)

Bit Position	Bit Name	Description
0	PRD_EN1_R	This bit indicates the status of PRD_EN1. This bit shows the same value as that of bit0 (PRD_EN1) in DMA_CH0_CON1 register, but it is used as read-only bit.

(i) AXI Common Input Register (AXI_COM_IN)

This register is used for the general purpose input.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0020h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	COM_IN[31:24]								COM_IN[23:16]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	COM_IN[15:8]								COM_IN[7:0]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-12 AXI_COM_IN Register Contents

Bit Position	Bit Name	Description
31 to 0	COM_IN[31: 0]	This field shows the value input from “AXI_COM_IN[31:0]”.

(j) AXI Common Output Register (AXI_COM_OUT)

This register is used for the general purpose output.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0024h

Initial Value: xxxx_ xxxxh

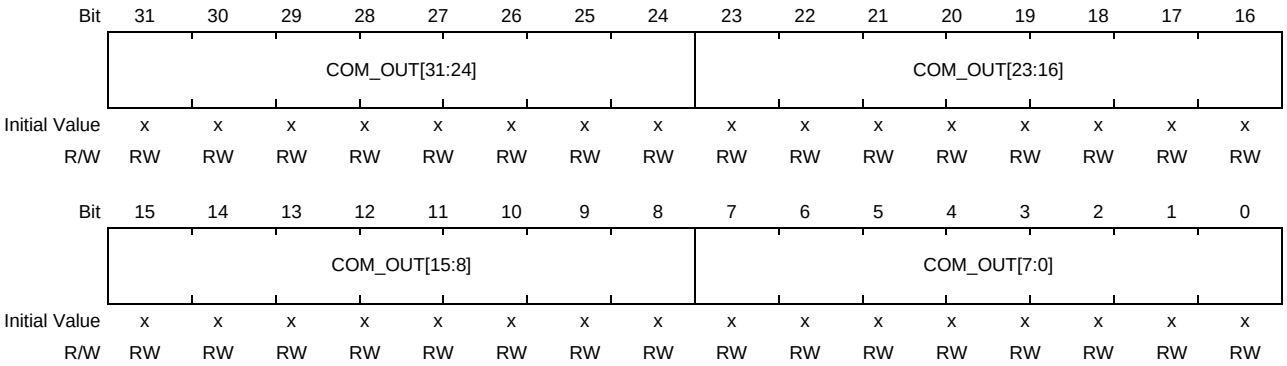


Table 35.6-13 AXI_COM_OUT Register Contents

Bit Position	Bit Name	Description
31 to 0	COM_OUT[31: 0]	The value in this field is output on “AXI_COM_OUT[31:0]”.

(k) DMA Ch0 Control Register n (DMA_Ch0_CONn)

This register is used to control DMA transfer with PRD table.

When it is required to change the setting in this register, disable PRD_ENn (=0) and make sure that DMA transfer on DMA_Ch0_CONn is not being executed before the change.

n = 1 to 14

ADDC: 020 + (010 × n)

Access Size: 32 bits

Address(es): <USB_S1_base> + ADDCh

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPE_DIRn	—	—	PIPE_NOn [4:0]					EXTPRD_NOn[3:0]				—	—	EXTPRD_ENn	PRD_ENn
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	RW	RW

Table 35.6-14 DMA_Ch0_CONn Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 16	Reserved	This field is read only. The value of this field is 0000h.
15	PIPE_DIRn	This bit specifies the direction of transfer in AXI Master IF. 1b: IN transfer 0b: OUT transfer
14 to 13	Reserved	This field is read only. The value of this field is 0h.
12 to 8	PIPE_NOn	This field specifies the index of the PIPE to which PRD table is assigned. The value from 1 to 30 is valid.
7 to 4	EXTPRD_NOn	This field specifies another DMA_Ch0_CONx in which the completion of transfer is waited for using EXTPRD_ENn. This field is valid only when PRD_ENn is set to 1. 0000b: DMA_Ch0_CON1 0001b: DMA_Ch0_CON2 0010b: DMA_Ch0_CON3 : : 1100b: DMA_Ch0_CON13 1101b: DMA_Ch0_CON14 1110b: Reserved 1111b: Reserved Do not set the same value with EXTPRD_NOn[7:4] and “n-1”.
3 to 2	Reserved	This field is read only. The value of this field is 0h.

Table 35.6-14 DMA_Ch0_CONn Register Contents (2/2)

Bit Position	Bit Name	Description
1	EXTPRD_ENn	This bit is used to keep DMA transfer on DMA_Ch0_CONn waiting until the transfer on another DMA_Ch0_CONx is completed. DMA_Ch0_CONx in which the completion of transfer is waited is specified on EXTPRD_NOn[3:0]. When both of this bit and PRD_ENn are set to 1, DMA_Ch0_CONn waits for the completion of transfer on another DMA_Ch0_CONx specified in EXTPRD_NOn[3:0]. When it has completed, EXTPRD_ENn is cleared to 0 and DMA transfer on DMA_Ch0_CONn is started. When setting EXTPRD_ENn and EXTPRD_NOn[3:0], make sure that PRD_ENx of DMA_Ch0_CONx in which the completion of transfer is waited is still 1. 1b : The function of EXTPRD_ENn is enabled. 0b : The function of EXTPRD_ENn is disabled.
0	PRD_ENn	This bit is used to enable DMA transfer on DMA_Ch0_CONn. Make sure that the address of the first PRD table for the transfer is set in DMA_Ch0_PRD_ADRn register before this bit is set. This bit is cleared to 0 when the transfer on DMA_Ch0_CONn is completed. 1b : DMA transfer is enabled. 0b : DMA transfer is disabled.

(l) DMA Ch0 PRD Address Register n (DMA_Ch0_PRD_ADRn)

This register is used to control DMA transfer with PRD table.

When it is required to change the setting in this register, disable DMA_Ch0_CONn.PRD_ENn(=0) and make sure that DMA transfer on DMA_Ch0_CONn is not being executed before the change.

n = 1 to 14

ADDP: 024 + (010 × n)

Access Size: 32 bits

Address(es): <USB_S1_base> + ADDPh

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PRD_ADRn[31:24]								PRD_ADRn[23:16]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PRD_ADRn[15:8]								PRD_ADRn[7:0]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-15 DMA_Ch0_PRD_ADRn Register Contents

Bit Position	Bit Name	Description
31 to 0	PRD_ADRn[31:0]	This field specifies the address of PRD table used for DMA transfer on DMA_Ch0_CONn. If the transfer on DMA_Ch0_CONn has been started, this field may show the address of PRD table being used at present. The value of this field after the transfer is completed is undefined.

35.6.3.2 Physical Region Descriptor (PRD) Table

Physical Region Descriptor (PRD) table is used to give the source or destination address, the size and other settings for the transfer to AXI-IF. It is assumed that the software prepares PRD table in system memory and assign it to DMA_Ch0_CONx.

PRD table is prepared individually for each PIPE and PIPEs cannot share a PRD table.

Make sure that PRD table does not cross the 4KB address boundary in system memory.

The format of PRD table and the definitions of fields are as follows.

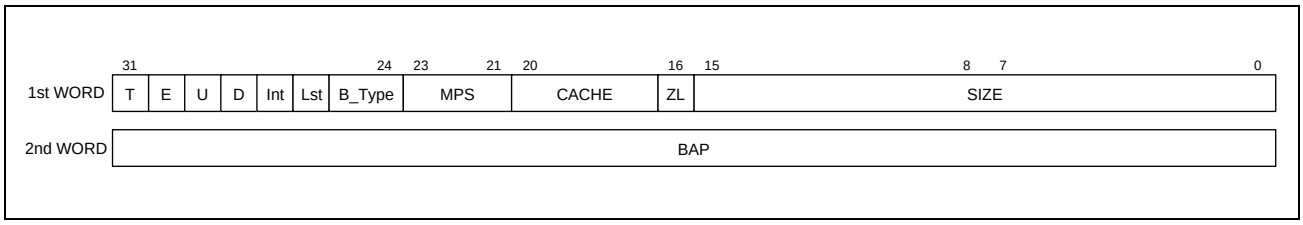


Figure 35.6-3 PRD Table Format

Table 35.6-16 1st Word in PRD Table (1/3)

Bit	Field Name	Updated by	Description
31	T	SW —	Type bit.: This bit indicates the type of descriptor. 1b: Link pointer 0b: Buffer pointer
30	E	SW —	End bit: This bit indicates the end of descriptor chain. Set 0 to this bit in case of link pointer. 1b: The end of chain 0b: Not the end of chain
29	U	— HW	Used bit : This bit indicates that the PRD table has been read for the transfer. Set 0 to this bit when PRD table is created. 1b: The PRD table has been read for the transfer. 0b: The PRD table has not been read for the transfer.
28	D	— HW	Data Error bit : This bit indicates that an error has occurred during transfer. Set 0 to this bit when PRD table is created. 1b: An error has been occurred. 0b: No error has been occurred.
27	Int	SW —	This bit specifies whether the completion of transfer on the descriptor causes an interrupt or not. In case this bit is set to 1, DMA_INT_STA.Pn_DMACNG_STA is asserted upon the completion of transfer on the descriptor. Set 0 to this bit in case of link pointer. 1b: An interrupt is asserted upon the completion of transfer. 0b: No interrupt is asserted upon the completion of transfer. In case that the short packet is received in OUT transfer, an interrupt is asserted as the completion of transfer regardless of the value in this bit. In case that USB3PERI has transferred all data related to the PRD table and End bit of the PRD table is set to 1, an interrupt is asserted as the completion of transfer regardless of the value in this bit.

Table 35.6-16 1st Word in PRD Table (2/3)

Bit	Field Name	Updated by	Description
26	Lst	SW HW	This bit indicates the last packet of the transfer. In case that this bit is set to 1 in IN transfer, EPC_D_DBWTRANSEND is required to be asserted to indicates that the current packet is last one at the end of writing of the last packet. When EPC has transmitted all data including the last packet at which EPC_D_DBWTRANSEND was asserted, EPC asserts Pn_INT_STA.Pn_LSTTR_STA. In case of OUT transfer, set 0 to this bit. When USB3PERI asserts EPC_D_DBTRANSEND at the end of transfer of the last packet, it sets 1 to this bit. 1b: The last packet 0b: Not the last packet
25:24	B_Type	FW —	This field specifies the type of burst. Set 00 to this field in case of link pointer. 00b: Fixed burst 01b: Incrementing burst
23:21	MPS	FW —	This field specifies the max packet size or the unit of transfer at Data Interface. Set 000 to this field in case of link pointer. 000b: 8 bytes 001b: 16 bytes 010b: 32 bytes 011b: 64 bytes 100b: 512 bytes 101b: 1024 bytes Others: Reserved
20:17	CACHE	FW —	This field specifies CACHE signal (MARCACHE/MAWCACHE) in data transfer.
16	ZL	FW HW	Zero Length Packet (ZLP) is used as the boundary of transfer. When this bit is set and the size of last data packet of transfer equals to the max packet size of the PIPE, USB3PERI expects ZLP comes in case of OUT transfer, or sends ZLP in case of IN transfer. Set this bit to 1 for USB device class which uses ZLP. When this bit is set to 1, Set USB_COM_CON.Pn_WDATAIF_NL, USB_COM_CON.Pn_RDATAIF_NL and USB_COM_CON.Pn_LSSTR_PP to 1 as well. If the bits are not set to 1 but ZLP is used, it is treated as PRD table format error and AXI_INT_STA.PRDERR0_x_STA. 1b: ZLP is transferred through Data Interface or on AXI DMA transfer 0b: ZLP is not transferred through Data Interface or on AXI DMA transfer. This bit is used with Lst bit in PRD table as well. If Lst=1, ZL=1 and the value in SIZE is multiples of the max packet size of the PIPE for IN transfer, USB3PERI sends ZLP after the last data packet of the PRD table automatically. In case of OUT transfer, USB3PERI sets ZL bit in the PRD table when it receives short packet including ZLP. The software isn't required to set the bit in that case. In case T bit shows link pointer, set this bit to 0.

Table 35.6-16 1st Word in PRD Table (3/3)

Bit	Field Name	Updated by	Description
15:0	SIZE	FW	This field specifies the number of byte to be transferred.
		HW	This field is updated to “the number of remaining bytes to be transferred” by hardware at each end of transfer of packet.
			The value from 1 byte to 64 Kbytes can be specified in this register.
			The meaning of 0000h differs depending on the statuses of Lst bit and ZL bit. If Lst = 1 and ZL = 1, 0000h means 0 byte. Otherwise, 0000h means 64 Kbytes. If it is required that data of 64 Kbytes is sent then ZLP is sent in order to show the boundary of transfer, prepare two PRD tables. The first PRD table has data of 64 Kbytes with Lst = 0, ZL = 0 and SIZE = 0000h (64 Kbytes), and the second PRD table has data of 0byte with Lst=1, ZL=1 and SIZE = 0000h (0 bytes).
			It is not allowed to divide a single USB packet into two or more PRD tables.
			For OUT direction, the transfer following the PRD table is terminated when USB3PERI receives the short packet. The initial value in this field should be multiples of the max packet size so that the last packet is accepted even when its size is the max packet size.
			For IN direction, if the size of data to be transferred is not multiples of the max packet size, the residue is transmitted as the last packet.
			In case of link pointer, set 0 to this field.

Table 35.6-17 2nd Word of PRD Table

Bit	Field Name	Updated by	Description
31:0	BAP	FW	In case that Type bit is buffer pointer:
		HW	This field indicates the start address of data.
			In this case, the next descriptor should be placed continuously in system memory.
			In case that Type bit is link pointer:
			This field indicates the address of next descriptor.
			In this case, the lower 3 bits of the address of descriptor should be 0.
			This field is updated at each end of transfer of packet.
			The value in this field is undefined when the transfer is terminated by receiving short packet or when the transfer is terminated due to error.

35.6.3.3 EPC Register

(1) USB Common Control Register (USB_PERI_USB_COM_CON)

This register provides the common functions to control USB3.1/USB2.0 behavior.

Only 32-bit access is allowed to this register.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0200h

Initial Value: 0000_0000h

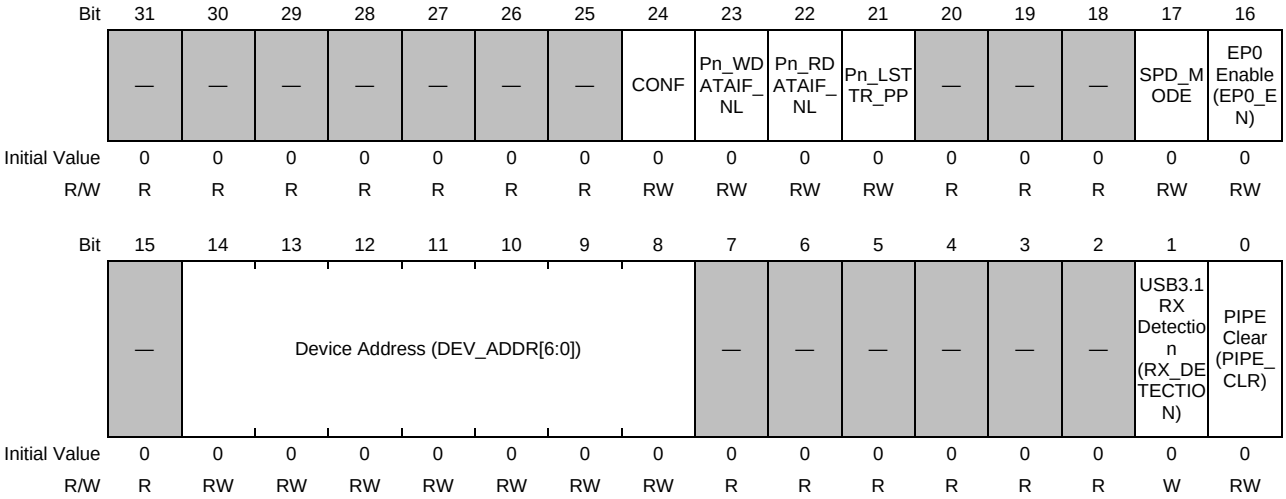


Table 35.6-18 USB_PERI_USB_COM_CON Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24	CONF	This bit is used to enable endpoints other than EP0. 1b: Endpoints other than EP0 are enabled. 0b: Endpoints other than EP0 are disabled.
23	Pn_WDATAIF_NL	This bit is used to enable the write of ZLP to be transmitted in IN transfer through Data interface or on AXI DMA transfer. 1b: The write of ZLP to be transmitted through Data Interface or on AXI DMA transfer is enabled. 0b: The write of ZLP to be transmitted through Data Interface or on AXI DMA transfer is disabled. When ZLP is transferred through Data Interface or on AXI DMA transfer, set this bit to 1. Otherwise, set this bit to 0.
22	Pn_RDATAIF_NL	This bit is used to enable the read of received ZLP in OUT transfer through Data Interface or on AXI DMA transfer. 1b: The read of received ZLP through Data Interface or on AXI DMA transfer is enabled. 0b: The read of received ZLP through Data Interface or on AXI DMA transfer is disabled. When ZLP is transferred through Data Interface or on AXI DMA transfer, set this bit to 1. Otherwise, set this bit to 0.
21	Pn_LSTTR_PP	This bit is used to disable the function to interpret the received packet with PP = 0 as the last one of the transfer. 1b: The received packet with PP = 0 is not interpreted as the last one. 0b: The received packet with PP = 0 is interpreted as the last one. When ZLP is transferred through Data Interface or on AXI DMA transfer, set this bit to 1. Otherwise, set this bit to 0.
20 to 18	—	Reserved. These bits are read as 0b.

Table 35.6-18 USB_PERI_USB_COM_CON Register Contents (2/2)

Bit Position	Bit Name	Description
17	SPD_MODE	This bit is used to set the operational mode of USB3PERI. It is prohibited to change the value in this bit except for the time the device is being connected to host. 1b: USB2.0 (HS/FS) 0b: USB3.1 (SS)
16	EP0 Enable (EP0_EN)	This bit is used to enable PIPE0 (EP0). 1b: PIPE0 is enabled 0b: PIPE0 is disabled
15	—	Reserved. This bit is read as 0b.
14 to 8	Device Address (DEV_ADDR[6:0])	The address of the device is set to this field. When Set Address is requested, set the address on the request to this field before USB3PERI completes the status stage of Set Address. If so, USB3PERI updates its address to the value given in this field when it completes the status stage of Set Address. This field is cleared automatically by warm reset, hot reset, bus reset or the assertion of USB_COM_CON.PIPE_CLR or P0_CON.P0_CLR.
7 to 2	—	Reserved. These bits are read as 0b.
1	USB3.1 RX Detection (RX_DETECTION)	This bit is used to start USB3.1 Rx Detection. When 1 is written to this bit, USB3PERI starts USB3.1 Rx Detection. This bit is valid only when USB30_CON.B3_CONNECT = 1 and PORTSC.PLS[3:0] is in Disabled state. This bit is write only and the value read from this bit is always 0.
0	PIPE Clear (PIPE_CLR)	This bit is used to initialize all PIPEs (PIPE0-PIPEn). When 1 is written to this bit, sequence numbers, data PIDs and data buffers are initialized. It has the same meaning to set all P0_CON.P0_CLR and Pn_CON.Pn_CLR for all PIPEs. The time required to initialize PIPEs varies depending on the number of PIPEs. When this bit shows 1, it means that the initialization of all PIPEs is still being executed. It is prohibited to access other registers until this bit becomes 0 after writing 1 to this bit.

(2) USB20 Control Register (USB_PERI_USB20_CON)

This register provides the basic functions to control USB2.0(HS/FS) behavior.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0204h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	B2_PUE	—	—	—	—	—	B2_RSUM_IN	B2_SUSPEND	—	—	—	LPM_DISABLE	LPM_ENABLE1	LPM_ENABLE0	B2_CONNECT	B2_PHYRST
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	B2_TSTMOD			—	—	—	—	—	—	—	B2_TSTMOD_EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	RW	RW	R	R	R	R	R	R	R	W

Table 35.6-19 USB_PERI_USB20_CON Register Contents (1/2)

Bit Position	Bit Name	Description
31	USB2 Pull-up Enable (B2_PUE)	This bit enables pull-up of D+ signal. The value in this bit is output on the signal “B2_PUE” directly. It is also required to set B2_CONNECT to 1 at the same time this bit is set. 1b: USB3PERI pulls up D+ Signal. 0b: USB3PERI does not pull up D+ Signal.
30 to 26	—	Reserved. These bits are read as 0b.
25	USB2 RSUM_IN Output (B2_RSUM_IN)	This bit is used to transmit USB2.0 resume signal. If the device does not support remote wake-up, it is not required to use this bit. The value in this bit is output on the signal “B2_RSUM_IN” directly. This bit is cleared automatically when the resume sequence is started internally. 1b: Resume signal is transmitted. 0b: Resume signal is not transmitted.
24	USB2 SUSPEND Output (B2_SUSPEND)	This bit is used to stop PLL in USB2.0 PHY. When USB_STA.B2_SPND_OUT = 1, it means that USB2.0 PHY is in suspended state, and PLL in USB2.0 PHY is stopped in order to reduce power consumption. PLL can be resumed by setting this bit to 0 when PLL is stopped. This bit is cleared to 0 automatically in case USB_STA.B2_RSUM_OUT or B2_PLL_WAKEIN is asserted. 1b: PLL in USB2.0 PHY is stopped 0b: PLL in USB2.0 PHY is not stopped. *Note*: The registers related to USB2.0 function cannot respond to the access when clock from USB2.0 PHY is stopped, and it can cause hung-up. Make sure to confirm clock from USB2.0 PHY is running when accessing the registers related to USB2.0 function.
23	—	Reserved. This bit is read as 0b. The write value should be 0b.

Table 35.6-19 USB_PERI_USB20_CON Register Contents (2/2)

Bit Position	Bit Name	Description
22	—	Reserved. This bit is read as 0b. The write value should be 0b.
21	Renesas Private	The initial value of this bit is 0. This bit can be read and written but it is not allowed to change the value of this bit. Only 0 is allowed as the value to be written.
20	LPM Disable (LPM_DISABLE)	This bit is used to disable LPM functions. When this bit is set to 1, USB3PERI gives no response to Extended Token of LPM from host. 1b: LPM functions are disabled. 0b: LPM functions are enabled. Basically this bit should always be 0.
19 to 18	LPM Enable (LPM_ENABLE[1:0])	This field specifies the response to LPM. 00b: Accept (default) USB3PERI basically accepts LPM request (But it might be rejected due to other reasons. Especially it will reject when it has data to be transmitted). 01b: Forced Accept USB3PERI always accepts LPM request and sends ACK as a response. 10b: Forced Reject USB3PERI always rejects LPM request and sends NYET as a response. 11b: Forced STALL USB3PERI always responds with STALL to LPM request. Basically this field should always be 00b.
17	USB2 Vbus CONNECT (B2_CONNECT)	This bit is used for USB2.0 connection. Set this bit to 1 when USB2.0 connection is started. The value in this bit is output on the signal “B2_CONNECT” directly. Note that it might be required to wait approx. 100 ms to change the value in this bit after detecting VBUS is changed, so that the influence of chattering of VBUS is removed. See section 7.3.2 for details. It is also required to set B2_PUE to 1 at the same time this bit is set.
16	USB2 PHY Reset (B2_PHYRST)	This bit is used to reset USB2.0 PHY. The value in this bit is output on the signal “B2_PHY_RESET” directly. USB3PERI also outputs “1” on B2_PHY_RESET when ARESETn is asserted. 1b: Reset 0b: No reset
15 to 11	—	Reserved. These bits are read as 0b.
10 to 8	USB2 Testmode (B2_TSTMOD[2:0])	This field specifies the function for USB2.0 compliance test. Set the value of the selected test function to this field at the timing of SetFeature (TEST_MODE) request has been successfully completed. USB3PERI enters the selected test mode when this field has the value other than normal mode and USB20_CON.B2_TSTMOD_EN is set to 1. 000b: Normal 001b: Test_J 010b: Test_K 011b: Test_SE0_NAK 100b: Test_Packet 101b - 111b: Reserved
7 to 1	—	Reserved. These bits are read as 0b.
0	USB2 Testmode Enable (B2_TSTMOD_EN)	When this bit is set to 1, the selected test function in USB20_CON.B2_TSTMODE[2:0] is enabled. This bit is write only and the value read from this bit is always 0.

(3) USB30 Control Register (USB_PERI_USB30_CON)

This register provides the basic functions to control USB3.1 (SS) behavior.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0208h

Initial Value: 1000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	U3_POWSEL[1:0]		POW_SEL[2:0]			B3_PLLWAKE	—	—	—	LPS_ENABLE[1:0]		B3_CONNECT	B3_PHYRST
Initial Value	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	R	R	RW	RW	RW	RW	RW	RW	R	R	R	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	POW_SEL_WEN	B3_HOTRST_CMP	B3_TP_SEND
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	W	W	W

Table 35.6-20 USB_PERI_USB30_CON Register Contents (1/3)

Bit Position	Bit Name	Description
31	—	Reserved. These bits are read as 0b. The write value should be 0b.
30, 29	—	Reserved. These bits are read as 0b.
28, 27	U3 State Power Select (U3_POWSEL[1:0])	This field specifies POWERDOWN mode (PHY_POWERDOWN[1:0]) to USB3.1-PHY when LTSSM transits to U3 state by the reception of LGO_U3. USB3PERI automatically requests USB3.1 PHY to transit to the selected state when it receives LGO_U3. 00b: P0 01b: Reserved 10b: P2 11b: Reserved Use USB30_CON.POW_SEL[2:0] if it is required to change POWERDOWN mode after the transition of LTSSM to U3 state has been completed. *Note*: That P3 is not listed here and USB3PERI does not specify P3 as USB3.1-PHY state when it transits to U3 state, so that clock from USB3.1-PHY is not suspended suddenly by autonomous operation by hardware. It is required to use USB30_CON.POW_SEL[2:0] in order to change POWERDOWN mode to P3.

Table 35.6-20 USB_PERI_USB30_CON Register Contents (2/3)

Bit Position	Bit Name	Description
26 to 24	Power State Change Select (POW_SEL[2:0])	This field is used to request to change POWERDOWN mode (PHY_POWERDOWN[1:0]). 000b: Transition from P0 to P2 in disconnected state (SS.Disabled) 001b: Transition from P0 to P3 in disconnected state (SS.Disabled) 010b: Transition from P2 to P0 in disconnected state (SS.Disabled) 011b: Reserved 100b: Transition from P0 to P2 in U3 state 101b: Transition from P0 to P3 in U3 state 110b: Transition from P2 to P0 in U3 state 111b: Reserved Transition of POWERDOWN mode other than above is automatically operated by USB3PERI. *Note*: That it is also required to set USB30_CON.POW_SEL_WEN when this field is used. If not, the request in this field is ignored. It is notified on USB_INT_STA_1.B3_PSSUCS_STA or USB_INT_STA_1.B3_PSFAIL_STA whether the transition succeeded or failed. *Note*: This field cannot be used to request the transition from P3. In that case, the transition is automatically operated by hardware. This register cannot be accessed when clock from USB3.1-PHY is suspended. Make sure to confirm clock from USB3.1 PHY is running when accessing to this register.
23	USB30-PHY PLL WAKEUP (B3_PLLWAKE)	This bit is used to change POWERDOWN mode from P3 to P0 in order to wake up PLL in case PHY_POWERDOWN[1:0] is in P3 state (PLL is stopped). Transition from P3 to P0 wakes up PLL. This bit is not cleared automatically after PLL is woken up. So make sure to clear this bit by software after confirming PLL is running. 1b: Requesting to wake up PLL 0b: Normal state The registers related to USB3.1 function cannot respond to the access when clock from USB3.1 PHY is stopped, and it can cause hung-up. Make sure to confirm clock from USB3.1 PHY is running when accessing the registers related to USB3.1 function
22 to 20	—	Reserved. These bits are read as 0b.
19, 18	LPS Enable (LPS_ENABLE[1:0])	This field specifies the response to LGO_U1/LGO_U2. 00b: Accept (default) USB3PERI basically accepts LPM request (But it might be rejected due to other reasons. Especially the hardware will reject when it has data to be transmitted). 01b: Forced Accept USB3PERI always accepts LGO_Ux request and sends LAU as the response. It also sends LGO_Ux to request the transition to low power state when PORTPMSC.Ux_TIMEOUT[7:0] is expired. 10b: Forced Reject USB3PERI always rejects LGO_Ux request and sends LXU as the response. It never sends LGO_Ux even when PORTPMSC.Ux_TIMEOUT[7:0] is expired. 11b: Reserved
17	USB3 Vbus CONNECT (B3_CONNECT)	This bit is used for USB3.1 connection. Set this bit to 1 to start USB3.1 connection. The value in this bit is output on the signal “B3_CONNECT” directly. Note that it might be required to wait approx. 100 ms to change the value in this bit after detecting VBUS is changed in order to remove the influence of chattering of VBUS.
16	USB3 PHY Reset (B3_PHYRST)	This bit is used to reset USB3.1 PHY. The value in this bit is output on the signal “B3_PHY_RESET” directly. USB3PERI also outputs “1” on B3_PHY_RESET when ARESETn is asserted. 1b: Reset 0b: No reset
15 to 3	—	Reserved. These bits are read as 0b.

Table 35.6-20 USB_PERI_USB30_CON Register Contents (3/3)

Bit Position	Bit Name	Description
2	POW_SEL_WEN (POW_SEL Write Enable)	When this bit is set to 1, the transition selected in USB30_CON.POW_SEL[2:0] is requested. This bit is write only and the value read from this bit is always 0.
1	USB3 Hot Reset Complete (B3_HOTRST_CMP)	This bit is used to notify the link layer of USB3PERI that the software process of hot reset has been completed and it can complete the reset sequence. Set this bit to 1 when the Hot Reset Process operation is complete. The reception of TS1/TS2 in which hot reset bit is set is notified on USB_INT_STA_1.B3_HOTRST_STA. Since the timeout of hot reset is defined as 12 ms in USB3.1 specification, make sure that the operation for hot reset has been completed and set this bit to 1 within 12 ms from the time USB_INT_STA_1.B3_HOTRST_STA is asserted. After this bit is set to 1, USB3PERI sends TS1 or TS2 in which hot reset bit is cleared to show that hot reset has been completed. This bit is write only and the value read from this bit is always 0.
0	USB3 TP Send (B3_TP_SEND)	This bit is used to allow the transmission of TP Data which is written to USB3_TPDAT0/1/2 register. When this bit is set to 1, USB3PERI sends TP_DATA which is written to USB3_TPDAT0/1/2 register. When warm reset or hot reset is detected before the transmission of TP Data, the transmission is cancelled. This bit is write only and the value read from this bit is always 0.

(4) USB Status Register (USB_PERI_USB_STA)

This register shows the status of several features of USB.

Access Size: 32 bits

Address(es): <USB_S1_base> + 020Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	DEV_ADDR_STA[6:0]						
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	B2_LSTATE		—	B2_USBRST	B2_L1SPND_OUT	B2_L1RSUM_OUT	B2_SPND_OUT	B2_RSUM_OUT	—	—	—	—	—	SPEED		VBUS_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-21 USB_PERI_USB_STA Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b.
22 to 16	Device Address Status (DEV_ADDR_STA [6:0])	This field indicates the device address. The value in USB_COM_CON.DEV_ADDR[6:0] is shown in this field after the status stage of Set Address has been finished. It is allowed to change the value in this field only for debug use and specific USB2.0 Compliance Test (Receiver Sensitivity). See 7.9.9 (e) for details. When warm reset, hot reset (USB3.1) or bus reset (USB2.0) is received, this field is cleared to 0.
15, 14	B2 LINE STATE (B2_LSTATE)	This field indicates the status of the input signal “B2_LINESTATE” (line state signal of USB2.0). 00b: SE0 01b: J-State 10b: K-State 11b: SE1
13	—	Reserved. This bit is read as 0b.
12	B2 USB_RESET (B2_USBRST)	This bit indicates the status of USB2.0 bus reset. This bit shows 1 from the detection of USB2.0 bus reset to the completion of speed negotiation (chirp). 1b: USB2.0 bus reset is in progress 0b: Normal state
11	B2 L1 SPND_OUT (B2_L1SPND_OUT)	This bit indicates that USB3PERI is in L1 state of LPM. This bit shows the level of the input signal “B2_L1_SPND_OUT”. 1b: L1 state 0b: Normal state
10	B2 L1 RSUM_OUT (B2_L1RSUM_OUT)	This bit indicates that the resume from L1 state is in progress. This bit shows the level of the input signal “B2_L1_RSUM_OUT”. 1b: Resume from L1 state is in progress. 0b: Normal state
9	B2 SPND_OUT (B2_SPND_OUT)	This bit indicates that USB3PERI is L2 state of LPM. This bit shows the level of the input signal “B2_SPND_OUT”. 1b: L2 state 0b: Normal state

Table 35.6-21 USB_PERI_USB_STA Register Contents (2/2)

Bit Position	Bit Name	Description
8	B2 RSUM_OUT (B2_RSUM_OUT)	This bit indicates that the resume from L2 state is in progress. This bit shows the level of the input signal “B2_RSUM_OUT”. 1b: Resume from L2 state is in progress. 0b: Normal state
7 to 3	—	Reserved. These bits are read as 0b.
2, 1	SPEED Mode (SPEED[1:0])	This bit indicates the operational mode of USB3PERI. 00b: SS 01b: FS 10b: HS Make sure to refer this bit after USB_INT_STA_1.SPEED_STA is asserted.
0	VBUS State (VBUS_STA)	This bit indicates the level of the input signal “VBUS”.

(5) USB20 Frame No. Register (USB_PERI_USB20_FRAME)

This register shows the frame number received in (u)SOF in USB2.0 operation.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0210h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	B2_FRAME										
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-22 USB_PERI_USB20_FRAME Register Contents

Bit Position	Bit Name	Description
31 to 11	—	Reserved. These bits are read as 0b.
10 to 0	B2_FRAME	This field shows the frame number received in (u)SOF in USB2.0 operation.

(6) USB Interrupt Status 1 Register (USB_PERI_USB_INT_STA_1)

This register indicates the interrupt statuses related to USB functions.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0220h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	B3_PLLWKUP_STA	B3_LUPSUCS_STA	B3_POLLING_STA	B3_INACTV_STA	B3_DISABLE_STA	B3_VNDTST_STA	B3_U2INACT_STA	B3_SETLNK_STA	—	B3_LNKCNG_STA	B3_WRMRST_STA	B3_HOTRST_STA	B3_PSFAIL_STA	B3_PSSUCS_STA	B3_U12REQ_STA	B3_TPSUCS_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	R	RW1	RW1	RW1	RW1	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	B2_LPMRCV_STA	B2_USBRST_STA	B2_L1SPND_STA	B2_L1RSUM_STA	B2_SPND_STA	B2_RSUM_STA	—	—	—	—	—	—	SPEED_STA	VBUS_CNG_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW1	RW1	RW1	RW1	RW1	RW1	R	R	R	R	R	R	RW1	RW1

Table 35.6-23 USB_PERI_USB_INT_STA_1 Register Contents (1/3)

Bit Position	Bit Name	Description
31	PLL Wakeup Status (B3_PLLWKUP_STA)	This bit is set to 1 when PHY30_CLK125_IN has been resumed due to PLL wakeup (USB30_CON.B3_PLLWAKE is set or the input signal “B3_PLL_WAKEIN” is asserted) or U3 Wakeup LFPS from host.
30	USB3 LinkUp Success Status (B3_LUPSUCS_STA)	This bit is set to 1 when the link of USB3.1 has been established (LTTSM enters U0 state from Polling state).
29	Enter USB3 Polling Status (B3_POLLING_STA)	This bit is set to 1 when LTSSM has entered Polling state.
28	Enter USB3 Inactive Status (B3_INACTV_STA)	This bit is set to 1 when LTSSM has entered Inactive state.
27	Enter USB3 Disabled Status (B3_DISABLE_STA)	This bit is set to 1 when LTSSM has entered Disabled state (But this bit is set only in the case LTTSM transits to Disabled state after USB30_CON.B3_CONNECT is set to 1).
26	USB3 Vendor DTEST LMP Receive Status (B3_VNDTST_STA)	This bit is set to 1 when Vendor Device Test LMP has been received.
25	USB3 U2Inact Timeout LMP Receive Status (B3_U2INACT_STA)	This bit is set to 1 when U2 Inactivity Timeout LMP has been received. When U2 Inactivity Timeout LMP is received, PORTPMSC.U2_TIMEOUT is automatically updated by hardware to the value in the received LMP.
24	USB3 SetLnkFunction LMP Receive Status (B3_SETLNK_STA)	This bit is set to 1 when Set Link Function LMP has been received. When Set Link Function LMP is received, PORTPMSC.FLA is automatically updated by hardware to the value in the received LMP.
23	—	Reserved. This bit is read as 0b.

Table 35.6-23 USB_PERI_USB_INT_STA_1 Register Contents (2/3)

Bit Position	Bit Name	Description
22	USB3 Link Status Change Status (B3_LNKCNG_STA)	This bit is set to 1 when LTSSM has made the transition as listed below. U0 -> U1 U0 -> U2 U0 -> U3 U3 -> Recovery -> U0 U2 -> Recovery -> U0 U1 -> Recovery -> U0 Refer to PORTSC.PLS[3:0] to know the current state.
21	USB3 Warm Reset Receive Status (B3_WRMRST_STA)	This bit is set to 1 when warm reset has been detected.
20	USB3 Hot Reset Receive Status (B3_HOTRST_STA)	This bit is set to 1 when hot reset has been detected.
19	USB3 Power Select Fail Status (B3_PSFAIL_STA)	This bit is set to 1 when the transition of POWERDOWN mode on USB30_CON.POW_SEL[2:0] has failed.
18	USB3 Power Select Success Status (B3_PSSUCS_STA)	This bit is set to 1 when the transition of POWERDOWN mode on USB30_CON.POW_SEL[2:0] has been completed successfully.
17	USB3 Enter U12 Request Receive Status (B3_U12REQ_STA)	This bit is set to 1 when USB3PERI has received LGO_U1or LGO_U2 or when U1 TIMEOUT of U2 TIMEOUT has occurred. USB3PERI responds with LAU or LXU when it receives LGO_U1 or LGO_U2, and sends LGO_U1 or LGO_U2 when U1 TIMEOUT or U2_TIMEOUT occurs, following the setting in USB30_CON.LPS_ENABLE[1:0].
16	USB3 TP Success Status (B3_TP_SUCS_STA)	This bit is set to 1 when the transmission of TP (Device Notification) requested on USB30_CON.B3_TP_SEND has been successfully completed.
15, 14	—	Reserved. These bits are read as 0b.
13	USB2 LPM Receive Status (B2_LPMRCV_STA)	This bit is set to 1 when USB3PERI has received LPM request from USB2.0 host and has returned ACK to it. Note this bit does not mean the device has made the transition to L1. In order to confirm the device has entered L1, wait for the assertion of B2_L1SPND_STA.
12	USB2 USB Reset Receive Status (B2_USBRST_STA)	This bit is set to 1 when USB2.0 bus reset has been detected.
11	USB2 L1 SPND_OUT Receive Status (B2_L1SPND_STA)	This bit is set to 1 when the transition request to L1 has been received from USB2.0 host and the device has accepted it. USB_STA.B2_L1_SPND_OUT is changed from 0 to 1 in that case.
10	USB2_L1 RSUM_OUT Receive Status (B2_L1RSUM_STA)	This bit is set to 1 when PLL wakeup is requested (USB20_CON.B2_SUSPEND = 0 or B2_PLL_WAKEIN = 1) or when the resume request from USB2.0 host is received (USB_STA.B2_L1RSUM_OUT changes from 0 to 1) during L1 state (USB_STA.B2_L1_SPND_OUT = 1).
9	USB2 SPND_OUT Receive Status (B2_SPND_STA)	This bit is set to 1 when the suspend request has been received from USB2.0 host (the device cannot deny it) and USB_STA.B2_SPND_OUT changes from 0 to 1.
8	USB2_RSUM_OUT Receive Status (B2_RSUM_STA)	This bit is set to 1 when PLL wakeup is requested (USB20_CON.B2_SUSPEND = 0 or B2_PLL_WAKEIN = 1) or when the resume request from USB2.0 host is received (USB_STA.B2_RSUM_OUT changes from 0 to 1) during L2 state (USB_STA.B2_SPND_OUT = 1) or L3 state (USB20_CON.B2_CONNECT=0).
7 to 2	—	Reserved. These bits are read as 0b.

Table 35.6-23 USB_PERI_USB_INT_STA_1 Register Contents (3/3)

Bit Position	Bit Name	Description
1	USB Speed Status (SPEED_STA)	This bit is set to 1 when there is any change in the speed mode of USB. Refer to USB_STA.SPEED[1:0] to know which speed mode is currently running. If the speed negotiation is executed again but the speed mode is not changed as a result of the negotiation, USB_STA.SPEED[1:0] shows the same value as that before the negotiation even when USB_INT_STA_1.SPEED_STA is set.
0	VBUS Change Status (VBUS_CNG_STA)	This bit is set to 1 when the level of the input signal “VBUS” changes. Refer to USB_STA.VBUS_STA to see the current level of VBUS.

(7) USB Interrupt Status 2 Register (USB_PERI_USB_INT_STA_2)

This register indicates the interrupt statuses of USB endpoints.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0224h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPE[15:0]_INT_STA															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-24 USB_PERI_USB_INT_STA_2 Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15 to 0	PIPEn_INT_STA (n = 15 to 0)	This bit indicates that an interrupt related to PIPEn occurs. (n = 15 to 0) Refer to Pn_INT_STA register with PIPE_COM.PIPE_NUM = n to know the cause of the interrupt. This bit is automatically cleared when all factors of interrupts in Pn_INT_STA register with PIPE_COM.PIPE_NUM = n are cleared.

(8) USB Interrupt Enable 1 Register (USB_PERI_USB_INT_ENA_1)

This register is used to enable the interrupts of USB.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0228h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	B3_PLLWKUP_ENA	B3_LUPSUCS_ENA	B3_POLLING_ENA	B3_INACTV_ENA	B3_DISABLE_ENA	B3_VNDTST_ENA	B3_U2INACT_ENA	B3_SETLNK_ENA	—	B3_LNKCNG_ENA	B3_WRMRST_ENA	B3_HOTRST_ENA	B3_PSFAIL_ENA	B3_PSSUCS_ENA	B3_U12REQ_ENA	B3_TPSUCS_ENA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	B2_LPMRCV_ENA	B2_USBRST_ENA	B2_L1SPND_ENA	B2_L1RSUM_ENA	B2_SPND_ENA	B2_RSUM_ENA	—	—	—	—	—	—	SPEED_ENA	VBUS_CNG_ENA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	RW	RW

Table 35.6-25 USB_PERI_USB_INT_ENA_1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	B3_PLLWKUP_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_PLLWKUP_STA. 1b: An interrupt due to USB_INT_STA_1.B3_PLLWKUP_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_PLLWKUP_STA is disabled.
30	B3_LUPSUCS_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_LUPSUCS_STA. 1b: An interrupt due to USB_INT_STA_1.B3_LUPSUCS_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_LUPSUCS_STA is disabled.
29	B3_POLLING_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_POLLING_STA. 1b: An interrupt due to USB_INT_STA_1.B3_POLLING_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_POLLING_STA is disabled.
28	B3_INACTV_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_INACTV_STA 1b: An interrupt due to USB_INT_STA_1.B3_INACTV_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_INACTV_STA is disabled.
27	B3_DISABLE_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_DISABLE_STA 1b: An interrupt due to USB_INT_STA_1.B3_DISABLE_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_DISABLE_STA is disabled.
26	B3_VNDTST_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_VNDTST_STA 1b: An interrupt due to USB_INT_STA_1.B3_VNDTST_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_VNDTST_STA is disabled.
25	B3_U2INACT_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_U2INACT_STA. 1b: An interrupt due to USB_INT_STA_1.B3_U2INACT_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_U2INACT_STA is disabled.
24	B3_SETLNK_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_SETLNK_STA. 1b: An interrupt due to USB_INT_STA_1.B3_SETLNK_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_SETLNK_STA is disabled.
23	—	Reserved. This bit is read as 0b.
22	B3_LNKCNG_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_LNKCNG_STA. 1b: An interrupt due to USB_INT_STA_1.B3_LNKCNG_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_LNKCNG_STA is disabled.
21	B3_WRMRST_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_WRMRST_STA. 1b: An interrupt due to USB_INT_STA_1.B3_WRMRST_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_WRMRST_STA is disabled.

Table 35.6-25 USB_PERI_USB_INT_ENA_1 Register Contents (2/2)

Bit Position	Bit Name	Description
20	B3_HOTRST_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_HOTRST_STA. 1b: An interrupt due to USB_INT_STA_1.B3_HOTRST_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_HOTRST_STA is disabled.
19	B3_PSFAIL_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_PSFAIL_STA. 1b: An interrupt due to USB_INT_STA_1.B3_PSFAIL_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_PSFAIL_STA is disabled.
18	B3_PSSUCS_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_PSSUCS_STA. 1b: An interrupt due to USB_INT_STA_1.B3_PSSUCS_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_PSSUCS_STA is disabled.
17	B3_U12REQ_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_U12REQ_STA. 1b: An interrupt due to USB_INT_STA_1.B3_U12REQ_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_U12REQ_STA is disabled.
16	B3_TP_SUCS_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B3_TPSUCS_STA. 1b: An interrupt due to USB_INT_STA_1.B3_TPSUCS_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B3_TPSUCS_STA is disabled.
15, 14	—	Reserved. These bits are read as 0b.
13	B2_LPMRCV_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B2_LPMRCV_STA. 1b: An interrupt due to USB_INT_STA_1.B2_LPMRCV_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B2_LPMRCV_STA is disabled.
12	B2_USBRST_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B2_USBRST_STA. 1b: An interrupt due to USB_INT_STA_1.B2_USBRST_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B2_USBRST_STA is disabled
11	B2_L1SPND_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B2_L1SPND_STA. 1b: An interrupt due to USB_INT_STA_1.B2_L1SPND_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B2_L1SPND_STA is disabled.
10	B2_L1RSUM_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B2_L1RSUM_STA. 1b: An interrupt due to USB_INT_STA_1.B2_L1RSUM_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B2_L1RSUM_STA is disabled.
9	B2_SPND_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B2_SPND_STA. 1b: An interrupt due to USB_INT_STA_1.B2_SPND_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B2_SPND_STA is disabled.
8	B2_RSUM_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.B2_RSUM_STA. 1b: An interrupt due to USB_INT_STA_1.B2_RSUM_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.B2_RSUM_STA is disabled.
7 to 2	—	Reserved. These bits are read as 0b.
1	SPEED_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1. SPEED_STA. 1b: An interrupt due to USB_INT_STA_1.SPEED_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.SPEED_STA is disabled.
0	VBUS_CNG_ENA	This bit is used to enable an interrupt due to USB_INT_STA_1.VBUS_CNG_STA. 1b: An interrupt due to USB_INT_STA_1.VBUS_CNG_STA is enabled. 0b: An interrupt due to USB_INT_STA_1.VBUS_CNG_STA is disabled.

(9) USB Interrupt Enable 2 Register (USB_PERI_USB_INT_ENA_2)

This register is used to enable the interrupts of USB endpoints.

Access Size: 32 bits

Address(es): <USB_S1_base> + 022Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPE[15:0]_INT_ENA															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.6-26 USB_PERI_USB_INT_ENA_2 Register Contents

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b.
30 to 16	—	Reserved. These bits are read as 0b. The write value should be 0b.
15 to 0	PIPE[15:0]_INT_ENA	This bit is used to enable an interrupt due to USB_INT_STA_2.PIPEi_INT_STA (i = 15 to 0). 1b: Interrupt due to USB_INT_STA_2.PIPEi_INT_STA is enabled. 0b: Interrupt due to USB_INT_STA_2.PIPEi_INT_STA is disabled.

(10) Setup Data 0 Register (USB_PERI_STUP_DAT_0)

This register shows the first 4 bytes of setup data which has been received in control transfer.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0230h

Initial Value: 0000_0000h

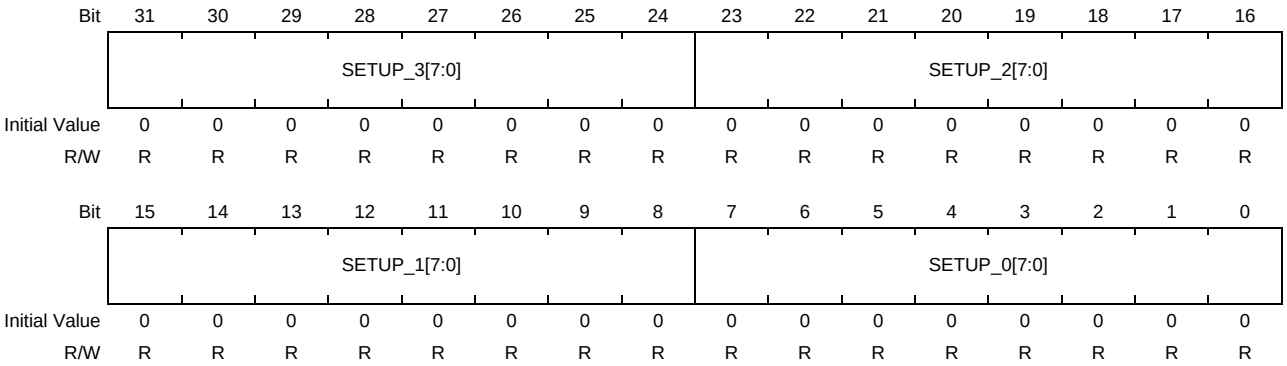


Table 35.6-27 USB_PERI_STUP_DAT_0 Register Contents

Bit Position	Bit Name	Description
31 to 24	SETUP_3[7:0]	This field shows the 4th byte of setup data.
23 to 16	SETUP_2[7:0]	This field shows the 3rd byte of setup data.
15 to 8	SETUP_1[7:0]	This field shows the 2nd byte of setup data.
7 to 0	SETUP_0[7:0]	This field shows the 1st byte of setup data.

(11) Setup Data 1 Register (USB_PERI_STUP_DAT_1)

This register shows the last 4 bytes of setup data which has been received in control transfer.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0234h

Initial Value: 0000_0000h

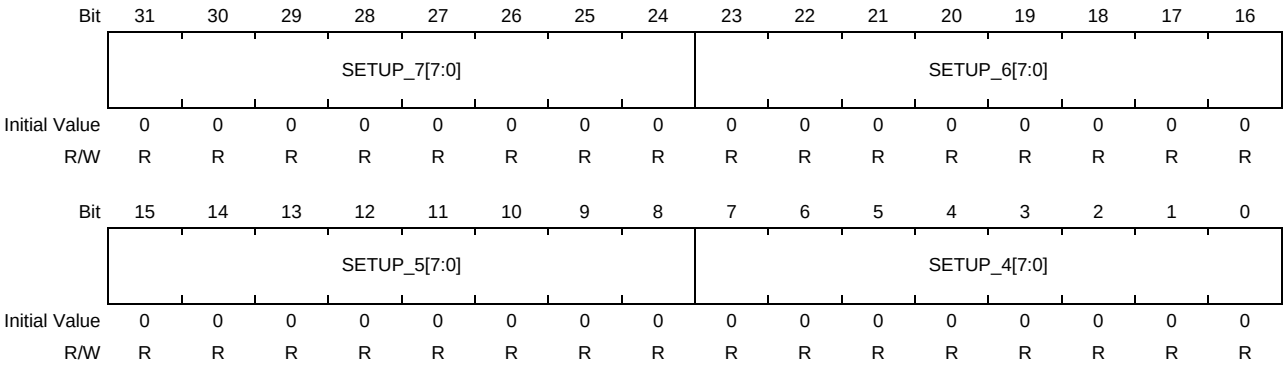


Table 35.6-28 USB_PERI_STUP_DAT_1 Register Contents

Bit Position	Bit Name	Description
31 to 24	SETUP_7[7:0]	This field shows the 8th byte of setup data.
23 to 16	SETUP_6[7:0]	This field shows the 7th byte of setup data.
15 to 8	SETUP_5[7:0]	This field shows the 6th byte of setup data.
7 to 0	SETUP_4[7:0]	This field shows the 5th byte of setup data.

(12) USB30 TP_Send Data 0 Register (USB_PERI_USB3_TPDAT_0)

This register is used to set DWORD 0 of TP to be transmitted to USB3.1 host.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0240h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TP_DATA_0[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TP_DATA_0[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.6-29 USB_PERI_USB3_TPDAT_0 Register Contents

Bit Position	Bit Name	Description
31 to 0	TP_Send_Data 0 (TP_DATA_0[31:0])	DWORD 0 of TP Bit[31:25]: Device Address Bit[24:5]: Reserved Bit[4:0]: Type

(13) USB30 TP_Send Data 1 Register (USB_PERI_USB3_TPDAT_1)

This register is used to set DWORD 1 of TP to be transmitted to USB3.1 host.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0244h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TP_DATA_1[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TP_DATA_1[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.6-30 USB_PERI_USB3_TPDAT_1 Register Contents

Bit Position	Bit Name	Description
31 to 0	TP_Send_Data 1 (TP_DATA_1[31:0])	DWORD 1 of TP Bit[31:8]: Notification Type Specific Bit[7:4]: Notification Type Bit[3:0]: Sub Type

(14) USB30 TP_Send Data 2 Register (USB_PERI_USB3_TPDAT_2)

This register is used to set DWORD 2 of TP to be transmitted to USB3.1 host.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0248h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TP_DATA_2[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TP_DATA_2[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.6-31 USB_PERI_USB3_TPDAT_2 Register Contents

Bit Position	Bit Name	Description
31 to 0	TP_Send_Data 2 (TP_DATA_2[31:0])	DWORD 2 of TP Bit[31:0]: Notification Type Specific

(15) USB20 LPM Status Register (USB_PERI_USB20_LPM_STA)

This register shows some fields in the received USB2.0 LPM.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0250h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BRW	BSEL				LINKST			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-32 USB_PERI_USB20_LPM_STA Register Contents

Bit Position	Bit Name	Description
31 to 9	—	Reserved. These bits are read as 0b.
8	LPM bRW Field (BRW)	This field indicates bRemoteWake field in received LPM. 1b: Remote Wakeup enable 0b: Remote Wakeup disable Check this field when an interrupt due to USB_INT_STA_1.B2_L1SPND_STA is asserted. This field is updated every time when LPM is successfully received.
7 to 4	LPM BESL Field (BESL[3:0])	This field indicates BESL field in received LPM. The value in this field means the period host initiates the resume signal in L1 state (75us step). 0000b: 125µs 0001b: 150µs 0010b: 200µs | 1111b: 10000µs Check this field when an interrupt due to USB_INT_STA_1.B2_L1SPND_STA is asserted. This field is updated every time when LPM is successfully received.
3 to 0	LPM LINKST Field (LINKST[3:0])	This field indicates bLinkState field in received LPM. The value in this field means the link state where USB3PERI shall make the transition to after it returns ACK to LPM token. 0001b: L1 (Sleep) others: Reserved Check this field when an interrupt due to USB_INT_STA_1.B2_L1SPND_STA is asserted. This field is updated every time when LPM is successfully received.

(16) USB30 Vendor Device Test Register (USB_PERI_USB30_VND_DEV)

This register shows Vendor Device Test field in DWORD 0 of the received Vendor Device Test LMP.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0254h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	VND_DTST							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-33 USB_PERI_USB30_VND_DEV Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	Vendor Device Test Status (VND_DTST[7:0])	This field indicates Vendor Device Test field of received Vendor Device Test LMP. Check this field when an interrupt due to USB_INT_STA_1.B3_VNDTST_STA is asserted. This field is updated every time when Vendor Device Test LMP is received.

(17) USB30 Vendor Defined Data 0 Register (USB_PERI_USB30_VND_DAT_0)

This register shows Vendor Defined Data field in DWORD 1 of the received Vendor Device Test LMP.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0258h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VND_DAT_0															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VND_DAT_0															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-34 USB_PERI_USB30_VND_DAT_0 Register Contents

Bit Position	Bit Name	Description
31 to 0	Vendor Defined Data 0 Register (VND_DAT_0[31:0])	This field indicates Vendor Defined Data field in DWORD 1 of the received Vendor Device Test LMP. Check this field when an interrupt due to USB_INT_STA_1.B3_VNDTST_STA is asserted. This field is updated every time when Vendor Device Test LMP is received.

(18) USB30 Vendor Defined Data 1 Register (USB_PERI_USB30_VND_DAT_1)

This register shows Vendor Defined Data field in DWORD 2 of the received Vendor Device Test LMP.

Access Size: 32 bits

Address(es): <USB_S1_base> + 025Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VND_DAT_1															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VND_DAT_1															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-35 USB_PERI_USB30_VND_DAT_1 Register Contents

Bit Position	Bit Name	Description
31 to 0	Vendor Defined Data 0 Register (VND_DAT_1[31:0])	This field indicates Vendor Defined Data field in DWORD 2 of the received Vendor Device Test LMP. Check this field when an interrupt due to USB_INT_STA_1. B3_VNDTST_STA is asserted. This field is updated every time when Vendor Device Test LMP is received.

(19) EPC Version Register (USB_PERI_USB_VER)

This register shows the release version or other information of EPC core of USB3PERI .

Access Size: 32 bits

Address(es): <USB_S1_base> + 0260h

Initial Value: xxxx_0203h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	AXI_MODE	—	—	—	—	Renesas Private			—	—	—	PIPE_NUM[4:0]				
Initial Value	x	0	0	0	0	x	x	x	0	0	0	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MJR_VER[7:0]								MIN_VER[7:0]							
Initial Value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-36 USB_PERI_USB_VER Register Contents

Bit Position	Bit Name	Description
31	AXI Mode (AXI_MODE)	This field shows the AXI mode of register groups to have the information of PRD Table. In this unit, AXI Register Mode2 is used
30 to 27	—	Reserved. These bits are read as 0b.
26 to 24	Renesas Private	This field is read only. The initial value of this field is 100b, but it depends on setting of HW.
23 to 21	—	Reserved. These bits are read as 0b.
20 to 16	Number of PIPEs (PIPE_NUM[4:0])	This field shows the number of PIPEs.
15 to 8	Major Version (MJR_VER[7:0])	This field shows the major version of EPC .
7 to 0	Minor Version (MIN_VER[7:0])	This field shows the minor version of EPC .

(20) Scratch Pad Register (USB_PERI_USB_SCRATCH)

This register provides the function of scratch pad. The main purpose of this register is debug use.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0264h

Initial Value: 0000_0000h

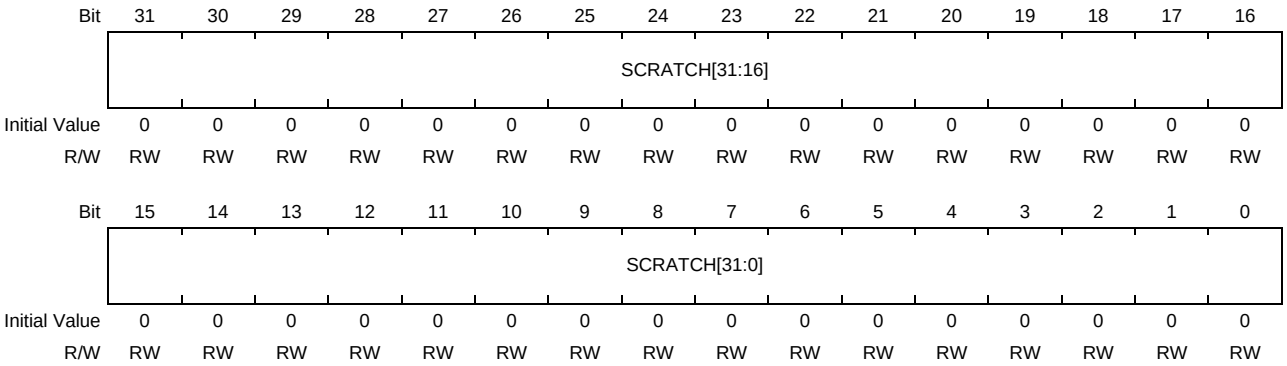


Table 35.6-37 USB_PERI_USB_SCRATCH Register Contents

Bit Position	Bit Name	Description
31 to 0	Scratch Pad (SCRATCH[31:0])	This field is used as scratch pad. This field holds the written data and it can be read any time as long as USB3PERI is not reset.

(21) PIPE0 Mode Setting Register (USB_PERI_P0_MOD)

This register indicates the mode settings for PIPE0.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0280h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	P0_DIR	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	RW	R	R	R	R	R	R

Table 35.6-38 USB_PERI_P0_MOD Register Contents

Bit Position	Bit Name	Description
31 to 7	—	Reserved. These bits are read as 0b.
6	PIPE0 Direction (P0_DIR)	This bit specifies the direction of transfer in the data stage of control transfer. Set this bit according to the direction bit in the received SETUP data. 0b: OUT (Control Write) 1b: IN (Control Read) *Note*: The response in the data stage is also specified by P0_CON.P0_IN_RES[1:0] or P0_CON.P0_OT_RES[1:0].
5 to 0	—	Reserved. These bits are read as 0b.

(22) PIPE0 Control Register (USB_PERI_P0_CON)

This register is used to control PIPE0.

Only 32-bit access is allowed to this register.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0288h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	P0_ST_RES		P0_OT_RES		—	—	—	—	—	—	P0_IN_RES	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	R	R	R	R	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	P0_BYTE_EN		P0_SEND	P0_RES_WEN	—	—	—	—	—	P0_BCLR	P0_CLR
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	RW	RW	RW	R	R	R	R	R	RW	RW

Table 35.6-39 USB_PERI_P0_CON Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b.
27, 26	PIPE0 Status Response (P0_ST_RES[1:0])	This field specifies the response of PIPE0 in the status stage of control transfer. 00b: Forced NRDY/NAK response 01b: Normal response In case of SS, USB3PERI responds with ACK for STATUS TP. In case of HS or FS, USB3PERI transmits zero length packet for IN token of status stage or responds with ACK for OUT token of status stage. 10b: Forced STALL response 11b: Reserved This field is changed to 00b automatically upon the reception of SETUP data and requires to be set again before the status stage of control transfer.
25, 24	PIPE0 OUT Response (P0_OT_RES[1:0])	This field specifies the response of PIPE0 for OUT data reception. 00b: Forced NRDY/NAK response 01b: Normal response (The data can be accepted depending on buffer status.) 10b: Forced STALL response 11b: Reserved This field is changed to 00b automatically upon the reception of SETUP data and requires to be set again before the data stage of control transfer if required. In case there is available space in buffer and data is acceptable in SS, ERDY is sent when this field changes from 00b to 01b.
23 to 18	—	Reserved. These bits are read as 0b.
17, 16	PIPE0 IN Response (P0_IN_RES[1:0])	This field specifies the response of PIPE0 for IN data request. 00b: Forced NRDY/NAK response 01b: Normal response (data can be transmitted depending on buffer status.) 10b: Forced STALL response 11b: This setting is prohibited This field is changed to 00b automatically upon the reception of Setup data and requires to be set again before the data stage of control transfer if required. In order to start the data stage, change this field from 00b to 01b. ERDY is automatically transmitted when the value of this bit is changed from 00b to 01b and USB3PERI has available buffer for the PIPE.
15 to 11	—	Reserved. These bits are read as 0b.

Table 35.6-39 USB_PERI_P0_CON Register Contents (2/2)

Bit Position	Bit Name	Description
10, 9	PIPE0 Byte Enable (P0_BYTE_EN[1:0])	This field specifies the number of bytes in last data which is written to P0_WRITE register. Select one of the values below and set it to this field at the same time P0_SEND is set. 00b: 4 bytes are valid. 01b: Only 1 byte is valid (Only DATA[7:0] is valid). 10b: Only 2 bytes are valid (Only DATA[15:0] is valid). 11b: Only 3 bytes are valid (Only DATA[23:0] is valid). This field is write only and the value read from this field is always 00b.
8	PIPE0 DP Send (P0_SEND)	Write 1b to this bit in order to transmit the packet written to P0_WRITE register or zero length packet. This bit is write only and the value read from this bit is always 0.
7	PIPE0 RES Write Enable (P0_RES_WEN)	Write 1 to this bit when changing P0_OT_RES[1:0], P0_IN_RES[1:0] or P0_ST_RES[1:0]. This bit is write only and the value read from this bit is always 0.
6 to 2	—	Reserved. These bits are read as 0b.
1	PIPE0 Buffer Clear (P0_BCLR)	Write 1 to this bit in order to clear buffer of PIPE0. Set P0_IN_RES[1:0] and P0_OT_RES[1:0] to 00b (forced NRDY/NAK response mode) and make sure P0_ACKSTS = 0 (no data is being transferred) and stop the access to the buffer of PIPE0 before the buffer is initialized with this bit. The interrupt statuses and the operation modes are not cleared by setting this bit. This bit shows 1 until the initialization is completed. It is not allowed to access other registers until this bit is cleared to 0b after writing 1b to this bit.
0	PIPE0 Clear (P0_CLR)	Write 1 to this bit in order to initialize PIPE0 (clearing sequence number, data PID and buffer). Set P0_IN_RES[1:0] and P0_OT_RES[1:0] to 00b (forced NRDY/NAK response mode) and make sure P0_ACKSTS = 0 (no date is being transferred) and stop the access to the buffer of PIPE0 before the buffer is initialized with this bit. The interrupt statuses and the operation modes are not cleared by setting this bit. This bit shows 1 until the initialization is completed. It is not allowed to access other registers until this bit is cleared to 0b after writing 1b to this bit.

(23) PIPE0 Status Register (USB_PERI_P0_STA)

This register is used to control PIPE0.

Only 32-bit access is allowed to this register.

Access Size: 32 bits

Address(es): <USB_S1_base> + 028Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	P0_FLOWSTS	P0_ACKSTS	P0_SNDSTS	P0_BUFSTS
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-40 USB_PERI_P0_STA Register Contents

Bit Position	Bit Name	Description
31 to 4	—	Reserved. These bits are read as 0b.
3	PIPE0 Flow Control Status (P0_FLOWSTS)	This bit shows the flow control status of PIPE0. 1b: Flow control state 0b: Normal state
2	PIPE0 ACK_TP Receive Status (P0_ACKSTS)	This bit shows whether PIPE0 has data that is currently being transferred or not. In case that the direction of transfer is OUT (P0_MOD.P0_DIR = 0), this bit shows 1b if PIPE0 has data which has been received but ACK for it has not been transmitted yet. In case that the direction of transfer is IN (P0_MOD.P0_DIR = 1), this bit shows 1b if PIPE0 has data which has already been transmitted but has not received ACK for it yet.
1	PIPE0 Send Status (P0_SNDSTS)	This bit shows 1b if PIPE0 has data which has not been transmitted yet. This bit is reset to 0b when all of written data have been transmitted and ACKs for them have been received. This bit is invalid for the case that the direction of transfer is OUT (P0_MOD.P0_DIR = 0).
0	PIPE0 Buffer Status (P0_BUFSTS)	This bit shows the buffer status of PIPE0. 0: The buffer cannot accept data for write, or it has no packet for read. 1: the buffer can accept data for write, or it has one or more packets For read,In case that the direction of transfer is OUT (P0_MOD.P0_DIR = 0), this bit shows 1 if it has one or more received packets in the buffer. In case that the direction of transfer is IN (P0_MOD.P0_DIR = 1), this bit shows 1 if data to be transmitted can be written to the buffer.

Note: Once the access to one of P0_READ, Pn_READ, P0_WRITE and Pn_WRITE registers is started in order to read or write a packet, it is prohibited to access to other Px_yyy register before whole of a packet has been read or written with the register which is currently used. The access to these registers is controlled in a unit of a packet, so the targeted register can be changed at the point that the read or write of the current packet has been completed and the access for the next packet is not started yet.

(24) PIPE0 Interrupt Status Register (USB_PERI_P0_INT_STA)

This register shows the interrupt factors of EPC_INTR_P[0].

Access Size: 32 bits

Address(es): <USB_S1_base> + 0290h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	P0_STSED_STA	P0_STSST_STA	P0_SETUP_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	P0_RCVNL_STA	P0_ERDY_STA	P0_FLOW_STA	P0_DF_STA	—	—	P0_STALL_STA	P0_NRDY_STA	P0_BFRDY_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW1	RW1	RW1	RW1	R	R	RW1	RW1	RW1

Table 35.6-41 USB_PERI_P0_INT_STA Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b.
18	PIPE0 STATUS Stage End Status (P0_STSED_STA)	This bit is set to 1 when the status stage of control transfer has been completed successfully.
17	PIPE0 STATUS Stage Start Status (P0_STSST_STA)	This bit is set to 1 when the status stage of control transfer is started.
16	PIPE0 SETUP Stage Status (P0_SETUP_STA)	This bit is set to 1 when valid setup data is received. When this bit is set, clear this bit first and then decode setup data and do the required operation for it.
15 to 9	—	Reserved. These bits are read as 0b.
8	PIPE0 Receive Null Data Status (P0_RCVNL_STA)	This bit indicates that zero length packet is received at PIPE0. The zero length packet received is automatically discarded when P0_LNG register is read for it. Therefore, this bit is asserted when P0_LNG register shows 0 for the zero length packet received. When this bit is asserted, it is required to read P0_LNG register as the read action for the zero length packet. If P0_LNG register shows 0, it means the zero length packet has been read.
7	PIPE0 ERDY_TP Send Status (P0_ERDY_STA)	This bit indicates that the condition to transmit ERDY from PIPE0 is satisfied. If P0_CON.P0_RES[1:0] has the value other than NRDY response and this bit is asserted, ERDY is transmitted to host. This bit is invalid in case of HS and FS.
6	PIPE0 Flow Control Status (P0_FLOW_STA)	This bit indicates that PIPE0 enters the flow control state. In case the direction of transfer is IN (P0_MOD.P0_DIR = 1), this bit is set to 1 when PIPE0 sends NRDY or DP with EOB = 1. In case the direction of transfer is OUT (P0_MOD.P0_DIR = 0), this bit is set to 1 when PIPE0 sends NRDY or ACK with NumP = 0. This bit is also set to 1 when PIPE0 receives the deferred packet. But this bit is not set to 1 in the case of received SETUP DP (deferred = 1) etc. It is recommended to use bit[5] to detect the deferred packet. This bit is invalid in case of HS and FS.
5	PIPE0 Deferred Status (P0_DF_STA)	This bit indicates that PIPE0 receives the deferred packet. This bit is set to 1 when PIPE0 receives the deferred packet. This bit is invalid in case of HS and FS.
4, 3	—	Reserved. These bits are read as 0b.

Table 35.6-41 USB_PERI_P0_INT_STA Register Contents (2/2)

Bit Position	Bit Name	Description
2	PIPE0 STALL Response Status (P0_STALL_STA)	This bit is set to 1 when STALL has been transmitted from PIPE0.
1	PIPE0 NRDY_TP Response Status (P0_NRDY_STA)	This bit is set to 1 when NRDY or NAK has been transmitted from PIPE0.
0	PIPE0 Buffer Ready Status (P0_BFRDY_STA)	This bit indicates the buffer status of PIPE0. In case the direction of transfer is IN (P0_MOD.P0_DIR = 1), this bit is set to 1 when the buffer of PIPE0 is ready to accept the next IN data. This bit is not asserted for the write of first packet after USB3PERI is initialized by a reset (hardware reset, USB_COM_CON.PIPE_CLR, P0_CON.P0_BCLR and P0_CON.P0_CLR). After a reset, the first packet can be written immediately although this bit is not asserted. In case the direction of transfer is OUT (P0_MOD.P0_DIR = 0), this bit is set to 1 when the next packet in the buffer of PIPE0 is ready to be read.

(25) PIPE0 Interrupt Enable Register (USB_PERI_P0_INT_ENA)

This register shows the interrupt factors of EPC_INTR_P[0].

Access Size: 32 bits

Address(es): <USB_S1_base> + 0294h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	P0_STSED_ENA	P0_STSST_ENA	P0_SETUP_ENA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	P0_RCVNL_ENA	P0_ERDY_ENA	P0_FLOW_ENA	P0_DF_ENA	—	—	P0_ENALL_ENA	P0_NRDY_ENA	P0_BFRDY_ENA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	R	R	RW	RW	RW

Table 35.6-42 USB_PERI_P0_INT_ENA Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b.
18	P0_STSED_ENA	This bit is used to enable the interrupt due to P0_INT_STA.P0_STSED_STA. 1b: an interrupt due to P0_INT_STA.P0_STSED_STA is enabled. 0b: an interrupt due to P0_INT_STA.P0_STSED_STA is disabled.
17	P0_STSST_ENA	This bit is used to enable the interrupt due to P0_INT_STA.P0_STSST_STA. 1b: an interrupt due to P0_INT_STA.P0_STSST_STA is enabled. 0b: an interrupt due to P0_INT_STA.P0_STSST_STA is disabled.
16	P0_SETUP_ENA	This bit is used to enable the interrupt due to P0_INT_STA.P0_SETUP_STA. 1b: an interrupt due to P0_INT_STA.P0_SETUP_STA is enabled. 0b: an interrupt due to P0_INT_STA.P0_SETUP_STA is disabled.
15 to 9	—	Reserved. These bits are read as 0b.
8	P0_RCVNL_ENA	This bit is used to enable the interrupt due to P0_INT_STA.P0_RCVNL_STA. 1b: an interrupt due to P0_INT_STA.P0_RCVNL_STA is enabled. 0b: an interrupt due to P0_INT_STA.P0_RCVNL_STA is disabled.
7	P0_ERDY_ENA	This bit is used to enable the interrupt due to P0_INT_STA.P0_ERDY_STA. 1b: an interrupt due to P0_INT_STA.P0_ERDY_STA is enabled. 0b: an interrupt due to P0_INT_STA.P0_ERDY_STA is disabled.
6	P0_FLOW_ENA	This bit is used to enable the interrupt due to P0_INT_STA.P0_FLOW_STA. 1b: an interrupt due to P0_INT_STA.P0_FLOW_STA is enabled. 0b: an interrupt due to P0_INT_STA.P0_FLOW_STA is disabled.
5	P0_DF_ENA	This bit is used to enable the interrupt due to P0_INT_STA.P0_DF_STA. 1b: an interrupt due to P0_INT_STA.P0_DF_STA is enabled. 0b: an interrupt due to P0_INT_STA.P0_DF_STA is disabled.
4, 3	—	Reserved. These bits are read as 0b.
2	P0_ENALL_ENA	This bit is used to enable the interrupt due to P0_INT_STA.P0_STALL_STA. 1b: an interrupt due to P0_INT_STA.P0_STALL_STA is enabled. 0b: an interrupt due to P0_INT_STA.P0_STALL_STA is disabled
1	P0_NRDY_ENA	This bit is used to enable the interrupt due to P0_INT_STA.P0_NRDY_STA. 1b: an interrupt due to P0_INT_STA.P0_NRDY_STA is enabled. 0b: an interrupt due to P0_INT_STA.P0_NRDY_STA is disabled.

Table 35.6-42 USB_PERI_P0_INT_ENA Register Contents (2/2)

Bit Position	Bit Name	Description
0	P0_BFRDY_ENA	This bit is used to enable the interrupt due to P0_INT_STA.P0_BFRDY_STA. 1b: an interrupt due to P0_INT_STA.P0_BFRDY_STA is enabled. 0b: an interrupt due to P0_INT_STA.P0_BFRDY_STA is disabled.

(26) PIPE0 Length Register (USB_PERI_P0_LNG)

This register shows the number of bytes in received packet which is currently read from P0_READ register.

Only 32-bit access is allowed to this register.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02A0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	P0_LENGTH									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-43 USB_PERI_P0_LNG Register Contents

Bit Position	Bit Name	Description
31 to 10	—	Reserved. These bits are read as 0b.
9 to 0	PIPE0 Data Length (P0_LENGTH[9:0])	This field shows the number of bytes in received packet which is currently read from P0_READ register. The value is decremented every time P0_READ register is read. Since P0_READ register allows only 32-bit access, the value is decremented by 4. Since P0_READ register is controlled in a unit of a packet, the length of received packet is shown in this register when the first 4 bytes of it are shown in P0_READ register and have not been read yet. This register is valid only for OUT direction.

Note: Once the access to one of P0_READ, Pn_READ, P0_WRITE and Pn_WRITE registers is started in order to read or write a packet, it is prohibited to access to other Px_yyy register before whole of a packet has been read or written with the register which is currently used. The access to these registers is controlled in a unit of a packet, so the targeted register can be changed at the point that the read or write of the current packet has been completed and the access for the next packet is not started yet.

(27) PIPE0 Read Register (USB_PERI_P0_READ)

This register is used to read OUT data which has been received at PIPEn.

If there is no data in buffer, 0000_0000h is returned.

Only 32-bit access is allowed to this register.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02A4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	P0_RDATA															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	P0_RDATA															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-44 USB_PERI_P0_READ Register Contents

Bit Position	Bit Name	Description
31 to 0	PIPE0 Read Data (P0_RDATA[31:0])	Read data from PIPE0. This register is controlled in a unit of a packet and cannot be read across the packet. That is, this register is updated in a unit of a packet. The current packet is never concatenated with the next packet even when the length of the current packet is not multiples of 4 and the last word of it is less than 4 bytes. In that case, the first 4 bytes of the next packet are shown in this register after the last word of the previous packet has been read. If the length of the current packet is not multiples of 4 and the last word of it is less than 4 bytes, the last word has one or more invalid bytes. In order to know how many valid bytes the last word has, see P0_LENGTH[7:0] before the read of the packet and calculate from it. The valid bytes are aligned from P0_RDATA[7:0]. This register is valid only for OUT direction.

Note: Once the access to one of P0_READ, Pn_READ, P0_WRITE and Pn_WRITE registers is started in order to read or write a packet, it is prohibited to access to other Px_yyy register before whole of a packet has been read or written with the register which is currently used. The access to these registers is controlled in a unit of a packet, so the targeted register can be changed at the point that the read or write of the current packet has been completed and the access for the next packet is not started yet.

(28) PIPE0 Write Register (USB_PERI_P0_WRITE)

This register is used to write IN data which is to be transmitted from PIPE0.

Only 32-bit access is allowed to this register.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02A8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	P0_WDATA															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	P0_WDATA															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-45 USB_PERI_P0_WRITE Register Contents

Bit Position	Bit Name	Description
31 to 0	PIPE0 Write Data (P0_WDATA[31:0])	Write data to PIPE0. This register is controlled in a unit of a packet and cannot be written across the packet. That is, it is not allowed to concatenate the current packet with the next packet to write them to this register even when the length of the current packet is not multiples of 4 and the last word of it is less than 4 bytes. In that case, the next packet can be written to this register after the write of the previous packet has been completed and it has been transmitted. This register is valid only for IN direction.

Note: Once the access to one of P0_READ, Pn_READ, P0_WRITE and Pn_WRITE registers is started in order to read or write a packet, it is prohibited to access to other Px_yyy register before whole of a packet has been read or written with the register which is currently used. The access to these registers is controlled in a unit of a packet, so the targeted register can be changed at the point that the read or write of the current packet has been completed and the access for the next packet is not started yet.

(29) PIPE Common Setting Register (USB_PERI_PIPE_COM)

This register is used for common settings for PIPEs.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02B0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Renesas Private
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PIPE_NUM				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW

Table 35.6-46 USB_PERI_PIPE_COM Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b.
16	Renesas Private	The initial value of this bit is 0. This bit can be read and written but it is not allowed to change the value of this bit. Only 0 is allowed as the value to be written.
15 to 5	—	Reserved. These bits are read as 0b.
4 to 0	Index of PIPE (PIPE_NUM[4:0])	Set the index of the target PIPE (the setting is from 1 to 15). 0_0000b: Invalid 0_0001b to 1_1111b: Index of PIPE

Note: Once the access to one of P0_READ, Pn_READ, P0_WRITE and Pn_WRITE registers is started in order to read or write a packet, it is prohibited to access to other Px_yyy register before whole of a packet has been read or written with the register which is currently used. The access to these registers is controlled in a unit of a packet, so the targeted register can be changed at the point that the read or write of the current packet has been completed and the access for the next packet is not started yet.

(30) PIPEn Mode Setting Register (USB_PERI_Pn_MOD)

This register is used to set the setting of mode for PIPEn.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02C0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	Pn_ERDY_CON		—	—	—	—	—	—	Pn_BOT	Pn_STREAM
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	R	R	R	R	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	Pn_DIR	Pn_TYPE		Pn_EPNUM			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW

Table 35.6-47 USB_PERI_Pn_MOD Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 26	—	Reserved. These bits are read as 0b.
25, 24	PIPEn ERDY Control (Pn_ERDY_CON)	This field specifies the condition to resume the transfer for PIPE. In case the device works in SS, USB3PERI requests the exit from U1 or U2 if it is in the low power state or transmits ERDY if it is in the flow-control state, when the condition below is satisfied. In case the device works in HS or FS and the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), USB3PERI requests the exit from L1 if it is in the low power state when the condition below is satisfied. The condition is as follows. In case the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0): • the device is in the flow-control state and the buffer of PIPEn has available space equivalent to the value in this field or more. In case the direction of transfer is IN (Pn_MOD.Pn_DIR = 1): • the device is in the flow-control state or L1 and the buffer of PIPEn has packets equivalent to the value in this field or more. • the device is in the flow-control state or L1 and the buffer of PIPEn has the last packet of the transfer. Note that USB3PERI requires clock from USB3.1-PHY when it requests the exit from U1 or U2 and clock from USB2.0-PHY when it requests the exit from L1. If not, USB3PERI does not request the exit from the states. [Setting Value] 00b: 1 Block (Packet) 01b: 2 Blocks (Packets) 10b: 4 Blocks (Packets) 11b: 8 Blocks (Packets)
23 to 18	—	Reserved. These bits are read as 0b.
17	PIPEn Bulk Only Transfer Select (Pn_BOT)	This bit specifies whether Bulk Only Transfer (BOT) mode is used or not. 1b: BOT mode 0b: Normal mode
16	PIPEn Stream ID Control (Pn_STREAM)	This bit is specified whether Stream bulk protocol is used or not. 1b: Stream bulk mode 0b: Normal mode This bit can be used only for bulk PIPE. (Pn_TYPE[1:0] = 10b)
15 to 7	—	Reserved. These bits are read as 0b.

Table 35.6-47 USB_PERI_Pn_MOD Register Contents (2/2)

Bit Position	Bit Name	Description
6	PIPEn Direction (Pn_DIR)	This bit specifies the direction of transfer. 0b: OUT 1b: IN
5, 4	PIPEn Transaction Type (Pn_TYPE[1:0])	This field specifies the type of transfer of PIPEn. 00b: Reserved (This setting is prohibited) 01b: Isochronous (This setting is prohibited) 10b: Bulk 11b: Interrupt
3 to 0	PIPEn Endpoint Number (Pn_EPNUM[3:0])	This field specifies the index of endpoint of PIPEn.

(31) PIPEn RAM Mapping Register (USB_PERI_Pn_RAMMAP)

This register is used to configure the mapping of SRAM for PIPEn.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02C4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Pn_RAMAREA			—	—	Pn_MPKT										
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Pn_RAMIF		Pn_BASEAD													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R

Table 35.6-48 USB_PERI_Pn_RAMMAP Register Contents

Bit Position	Bit Name	Description
31 to 29	PIPEn RAM Area Setting (Pn_RAMAREA[2:0])	This field specifies the area in SRAM for PIPEn. The area of SRAM attached to the interface specified in Pn_RAMIF[1:0] is given to PIPEn. The area is calculated as 1 Kbytes x 2^ (Pn_RAMAREA[2:0]). 1 Block requires 1 Kbytes regardless of the max packet size in Pn_MPKT[10:0]. Pn_RAMAREA[2:0] the area given to PIPEn. 000b: 1 Kbyte (1 block) 001b: 2 Kbytes (2 blocks) 010b: 4 Kbytes (4 blocks) 011b: 8 Kbytes (8 blocks) 100b: 16 Kbytes (16 blocks) 101b to 111b: Reserved
28, 27	—	Reserved. These bits are read as 0b.
26 to 16	PIPEn Max Packet Size Setting (Pn_MPKT[10:0])	This field specifies the max packet size of PIPEn. Select the value set to this field from among 8, 16, 32, 64, 512 and 1024. PIPE0 or bulk PIPE are defined to have the max packet size from among them in all speed mode. But interrupt PIPE can have the max packet size which is not equal to any of them. In that case, select the value which is more than the max packet size and proximate one, and set it to this field. USB3PERI controls buffer in the unit of the values above.
15, 14	PIPEn RAMIF (Pn_RAMIF[1:0])	This field specifies the index of SRAM interface connected to SRAM allocated to PIPEn.
13 to 0	PIPEn RAM Base Address (Pn_BASEAD[13:0])	This field specifies the base address in SRAM allocated to PIPEn. Sets Base Address of 64 bit buffer RAM for EPC to be allocated to PIPEn. The address for 64 bit word is used. (Ex) If 4K bytes from the start of RAM is assigned to PIPE1 and the area from the boundary is assigned to PIPE2, set 200h to this field for PIPE2. This field can be modified when Pn_CON.Pn_EN = 0. Since the area is assigned in the unit of 1K bytes, the lower 7 bits of this field is read only and fixed to 0.

(32) PIPEn Control Register (USB_PERI_Pn_CON)

This register provides control for PIPEn.

Only 32-bit access is allowed to this register.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02C8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Pn_EN	Pn_DATAIF_EN	—	—	—	—	—	Pn_ERDY_SEND	—	—	—	—	—	—	Pn_RES	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	R	R	R	R	R	W	R	R	R	R	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Pn_LAST	Pn_BYTE_EN		Pn_SEND	Pn_RES_WEN	—	—	—	—	—	Pn_BCLR	Pn_CLR
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	W	W	W	W	W	R	R	R	R	R	W	W

Table 35.6-49 USB_PERI_Pn_CON Register Contents (1/3)

Bit Position	Bit Name	Description
31	PIPEn Enable (Pn_EN)	This bit enables or disables PIPEn. The setting in this bit is valid when USB_COM_CON.CONF = 1. In case this bit is disabled, make sure that no data transfer is executed to PIPEn. In case this bit is enabled, make sure that the initialization of PIPEn has been done. 1b: PIPEn Enabled 0b: PIPEn disabled (PIPEn gives no response for any access.)
30	PIPEn DATAIF Enable (Pn_DATAIF_EN)	This bit enables or disables Data Interface of EPC for PIPEn. 1b: Data Interface is enabled 0b: Data Interface is disabled *Note*: This bit is reset to 0 every time CBW is received with Bulk Only Transfer (BOT) mode (Pn_MOD.Pn_BOT = 1). If data transfer is requested in CBW, it is required to set this bit to 1 again before the data transfer.
29 to 25	—	Reserved. These bits are read as 0b.
24	PIPEn ERDY Send (Pn_ERDY_SEND)	When 1 is written to this bit, USB3PERI transmits ERDY after it requests the exit from U1, U2 or L1 if it is in the states, or it transmits ERDY with no condition if it is not in the states (ERDY is sent only in case of SS). Since USB3PERI automatically sends ERDY when it wants to resume the transfer, it is not required to use this bit basically. If there is any case ERDY is required to be sent intentionally, this bit is available for that case. This bit is write only and the value read from this bit is always 0.
23 to 18	—	Reserved. These bits are read as 0b.

Table 35.6-49 USB_PERI_Pn_CON Register Contents (2/3)

Bit Position	Bit Name	Description
17, 16	PIPEn Response (Pn_RES[1: 0])	In case of the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0), this field specifies the response of PIPEn for the reception of OUT data. 00b: Forced NRDY/NAK Response 01b: Normal Response (Data can be accepted depending on the buffer status.) 10b: Forced STALL Response 11b: This setting is prohibited ERDY is transmitted when the value of this bit is changed from 00b to 01b if the device works in SS and the buffer has available space for PIPEn. In case of Stream bulk OUT (Pn_MOD.Pn_STREAM = 1), this bit is automatically changed to 00b (Forced NRDY/NAK response) when DP(PRIME) or DP(NoStream) is received. In case of the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), this field specifies the response of PIPEn for the transmission of IN data. 00b: Forced NRDY/NAK Response 01b: Normal Response (Data can be transmitted depending on the buffer status.) 10b: Forced STALL Response 11b: This setting is prohibited ERDY is transmitted when the value of this bit is changed from 00b to 01b if the device works in SS and the buffer has data to be transmitted from PIPEn. In case of Stream bulk OUT (Pn_MOD.Pn_STREAM = 1), this bit is automatically changed to 00b (Forced NRDY/NAK response) when ACK(PRIME) is received. *Note*: That Pn_RES_WEN is set to 1 at the same timing this field is modified.
15 to 12	—	Reserved. These bits are read as 0b.
11	PIPEn Last Data Send (Pn_LAST)	This bit indicates whether the packet written through Pn_WRITE register is the last one of the transfer (of the Stream ID). This bit is set at the same timing Pn_SEND is set in order to transmit the packet written through Pn_WRITE register. In case that the packet is the last one, set this bit and Pn_SEND in one word access. 1b: The last packet 0b: Not the last packet Pn_INT_STA.Pn_LSTTR_STA is asserted when the packet with this bit set has been sent and has been acknowledged by host. This bit is write only and the value read from this bit is always 0.
10, 9	PIPEn Byte Enable (Pn_BYTE_EN[1:0])	This bit specifies the number of valid bit in the last word that was written through Pn_WRITE register. This bit is set the same time as writing a value in Pn_SEND. 00b: 4 bytes are valid. 01b: Only 1 byte is valid. (Only DATA[7: 0] is valid.) 10b: Only 2 bytes are valid. (Only DATA[15: 0] is valid.) 11b: Only 3 bytes are valid. (Only DATA[23: 0] is valid.) This field is write only and the value read from this field is always 0.
8	PIPEn DP Send (Pn_SEND)	Write 1 to this bit in order to transmit the packet written to Pn_WRITE register or zero length packet. This bit is write only and the value read from this bit is always 0.
7	PIPEn RES Write Enable (Pn_RES_WEN)	Write 1 to this bit when changing Pn_RES[1:0]. This bit is write only and the value read from this bit is always 0.
6 to 2	—	Reserved. These bits are read as 0b.
1	PIPEn Buffer Clear (Pn_BCLR)	Write 1 to this bit in order to clear buffer of PIPEn. Set Pn_RES[1:0] to 00b (forced NRDY/NAK response mode) and make sure Pn_ACKSTS = 0 (no data is being transferred) and stop the access to buffer before initializing the buffer with this bit. In case of Stream bulk protocol (Pn_MOD.Pn_STREAM = 1), Pn STREAM register is also initialized when this bit is used. This bit shows 1 until the initialization is completed. It is not allowed to access other registers until this bit is cleared to 0 after writing 1 to this bit.

Table 35.6-49 USB_PERI_Pn_CON Register Contents (3/3)

Bit Position	Bit Name	Description
0	PIPEn Clear (Pn_CLR)	Write 1 to this bit in order to initialize PIPEn (clearing sequence number, data PID and buffer). Set Pn_RES[1:0] to 00b (forced NRDY/NAK response mode) and make sure Pn_ACKSTS = 0 (no date is being transferred) and stop the access to the buffer of PIPEn before PIPEn is initialized. This bit shows 1 until the initialization is completed. It is not allowed to access other registers until this bit is cleared to 0 after writing 1 to this bit.

(33) PIPEn Status Register (USB_PERI_Pn_STA)

This register shows the status of PIPEn.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02CCh

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	Pn_FLOWSTS	Pn_ACKSTS	Pn_SNDSTS	Pn_BUFSTS
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-50 USB_PERI_Pn_STA Register Contents

Bit Position	Bit Name	Description
31 to 4	—	Reserved. These bits are read as 0b.
3	PIPEn Flow Control Status (Pn_FLOWSTS)	This bit shows the flow control state of PIPEn. 1b: Flow control state 0b: Normal state
2	PIPEn ACK_TP Receive Status (Pn_ACKSTS)	This bit shows whether PIPEn has data that is currently being transferred or not. In case that the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0), this bit shows 1 if PIPEn has data which has been received but ACK for it has not been transmitted yet. In case that the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), this bit shows 1 if PIPEn has data which has already been transmitted but has not received ACK for it yet.
1	PIPEn Send Status (Pn_SNDSTS)	This bit shows 1 if PIPEn has data which has not been transmitted yet. This bit is reset to 0 when all of written data have been transmitted and ACKs for them have been received. This bit is invalid for the case that the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0).
0	PIPEn Buffer Status (Pn_BUFSTS)	This bit shows the buffer status of PIPEn. 0b: The buffer cannot accept data for write, or it has no packet for read. 1b: The buffer can accept data for write, or it has one or more packets for read. In case that the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0), this bit shows 1 if it has one or more received packets in the buffer. In case that the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), this bit shows 1 if data to be transmitted can be written to the buffer.

Note: Once the access to one of P0_READ, Pn_READ, P0_WRITE and Pn_WRITE registers is started in order to read or write a packet, it is prohibited to access to other Px_yyy register before whole of a packet has been read or written with the register which is currently used. The access to these registers is controlled in a unit of a packet, so the targeted register can be changed at the point that the read or write of the current packet has been completed and the access for the next packet is not started yet.

(34) PIPEn Interrupt Status Register (USB_PERI_Pn_INT_STA)

This register indicates Interrupt factor of INTR_Pn_B Pin.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02D0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	Pn_CBW_STA	—	—	—	Pn_STERR_STA	Pn_STRMX_STA	Renesas Private	Pn_NSTRM_STA	Pn_PRIME_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW1	R	R	R	RW1	RW1	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	Pn_RCVNL_STA	Pn_ERDY_STA	Pn_FLOW_STA	Pn_DF_STA	Pn_LSTTR_STA	—	Pn_STALL_STA	Pn_NRDY_STA	Pn_BFRDY_STA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW1	RW1	RW1	RW1	RW1	R	RW1	RW1	RW1

Table 35.6-51 USB_PERI_Pn_INT_STA Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24	PIPEn Receive CBW Status (Pn_CBW_STA)	This bit is valid only when Bulk Only Transfer is supported (Pn_MOD.Pn_BOT = 1) and the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0). This bit is set to1 when CBW is received to PIPEn and the data can be read from Pn_READ register. CBW is defined by the following conditions. • The length of the packet is 31 bytes. • The first 4 bytes of the packet (dCBWSignature) equals to 4342_5355h.
23 to 21	—	Reserved. These bits are read as 0b.
20	PIPEn Stream Error Status (Pn_STERR_STA)	This bit is set to 1 when Stream bulk protocol error occurs in PIPEn. See USB3.1 specification for detail of error in Stream bulk protocol. This bit is invalid in case of HS and FS. This bit is cleared by writing 1. Writing 0 to this bit has no effect.
19	PIPEn Stream ID-X Status (Pn_STRMX_STA)	This bit is set to 1 when Stream ID of the packet received at PIPEn from host is not equal to the value in Pn_STREAM.Pn_STREAM_C (except for PRIME and NoStream). See Pn_NRDYSTRM register to know the Stream ID of received packet which has been rejected. This bit is invalid in case of HS and FS. This bit is cleared by writing 1. Writing 0 to this bit has no effect.
18	Renesas Private	This bit might be changed and an interrupt due to it might be generated if not masked. Make sure not to set bit18 in Pn_INT_ENA register in order to disable the interrupt due to this bit.
17	PIPEn Receive NoStream Status (Pn_NSTRM_STA)	This bit indicates that NoStream is designated as Stream ID for PIPEn and is valid only in case Stream bulk protocol is used. (Pn_MOD.Pn_STREAM = 1). In case the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), this bit is set when ACK(NoStream) is received. Pn_CON.Pn_RES[1:0] is automatically set to NRDY response (= 00b) in that case. In case of the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0), this bit is set when DP(NoStream) is received. Pn_CON.Pn_ERS[1:0] is automatically set to NRDY response (= 00b) in that case. This bit is invalid in case of HS/FS.

Table 35.6-51 USB_PERI_Pn_INT_STA Register Contents (2/2)

Bit Position	Bit Name	Description
16	PIPEn Receive PRIME Status (Pn_PRIME_STA)	This bit indicates that PRIME is designated as Stream ID for PIPEn and is valid only in case Stream bulk protocol is used (Pn_MOD.Pn_STREAM = 1). In case the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), this bit is set when ACK(PRIME) is received. Pn_CON.Pn_RES[1:0] is automatically set to NRDY response (= 00b) in that case. In case of the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0), this bit is set when DP(PRIME) is received. Pn_CON.Pn_ERS[1:0] is automatically set to NRDY response (= 00b) in that case. This bit is invalid in case of HS/FS.
15 to 9	—	Reserved. These bits are read as 0b. Writing is invalid.
8	PIPEn Receive Null Data Status (Pn_RCVNL_STA)	This bit indicates that zero length packet has been received at PIPEn and becomes ready to be read. The zero length packet received is automatically discarded when Pn_LNG register is read for it. Therefore, this bit is asserted when Pn_LNG register shows 0 for the zero length packet received. When this bit is asserted, it is required to read Pn_LNG register as the read action for the zero length packet. If Pn_LNG register shows 0, it means the zero length packet has been read.
7	PIPEn ERDY_TP Send Status (Pn_ERDY_STA)	This bit indicates that the condition to transmit ERDY from PIPEn is satisfied. If Pn_CON.Pn_RES[1:0] has the value other than NRDY response and this bit is asserted, ERDY is transmitted to host. For Stream bulk protocol, Pn_CON.Pn_RES[1:0] should be set to normal response (= 01b) so that ERDY is transmitted to specify Stream ID. This bit is invalid in case of HS and FS.
6	PIPEn Flow Control Status (Pn_FLOW_STA)	This bit indicates that PIPEn enters the flow control state. In case the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), this bit is set to 1 when PIPEn sends NRDY or DP with EOB = 1. In case the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0), this bit is set to 1 when PIPEn sends NRDY or ACK with NumP = 0. This bit is also set to 1 when PIPEn receives the deferred packet. But this bit is not set to 1 in the case of received SETUP DP (deferred = 1) etc. It is recommended to use bit[5] to detect the deferred packet. This bit is invalid in case of HS and FS.
5	PIPEn Deferred Status (Pn_DF_STA)	This bit indicates that PIPEn receives the deferred packet. This bit is set to 1 when PIPEn receives the deferred packet. This bit is invalid in case of HS and FS.
4	PIPEn Last Transaction Status (Pn_LSTTR_STA)	This bit indicates that PIPEn has transmitted or received the last packet of the transfer. In case the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), this bit is set to 1 when PIPEn has transmitted the packet for which Pn_CON.Pn_LAST is set. In case the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0), this bit is set to 1 when PIPEn has received the short packet or the packet with PP = 0.
3	—	Reserved. This bit is read as 0b.
2	PIPEn STALL Response Status (Pn_STALL_STA)	This bit is set to 1 when STALL has been transmitted from PIPEn.
1	PIPEn NRDY_TP Response Status (Pn_NRDY_STA)	This bit is set to 1 when NRDY or NAK has been transmitted from PIPEn.
0	PIPEn Buffer Ready Status (Pn_BFRDY_STA)	This bit indicates the buffer status of PIPEn. In case the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), this bit is set to 1 when the buffer of PIPEn is ready to accept the next IN data. This bit is not asserted for the write of first packet after USB3PERI is initialized by a reset (hardware reset, USB_COM_CON.PIPE_CLR, Pn_CON.Pn_BCLR and Pn_CON.Pn_CLR). After a reset, the first packet can be written immediately although this bit is not asserted. In case the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0), this bit is set to 1 when the next packet in the buffer of PIPEn is ready to be read.

Note: These bits are cleared by writing 1.

(35) PIPEn Interrupt Enable Register (USB_PERI_Pn_INT_ENA)

This register is used to enable the interrupts related to PIPEn.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02D4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	Pn_CBW__ENA	—	—	—	Pn_STERR__ENA	Pn_STRMX__ENA	Renesas Private	Pn_NSTRM__ENA	Pn_PRIME__ENA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	R	R	R	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	Pn_RCVNL__ENA	Pn_ERDY__ENA	Pn_FLOW__ENA	Pn_DF_ENA	Pn_LSTTR__ENA	—	Pn_STALL__ENA	Pn_NRDY__ENA	Pn_BFRDY__ENA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	R	RW	RW	RW

Table 35.6-52 USB_PERI_Pn_INT_ENA Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24	Pn_CBW__ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_CBW_STA. 1b: an interrupt due to Pn_INT_STA.Pn_CBW_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_CBW_STA is disabled
23 to 21	—	Reserved. These bits are read as 0b.
20	Pn_STERR__ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_STERR_STA. 1b: an interrupt due to Pn_INT_STA.Pn_STERR_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_STERR_STA is disabled.
19	Pn_STRMX__ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_STRMX_STA. 1b: an interrupt due to Pn_INT_STA.Pn_STRMX_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_STRMX_STA is disabled.
18	Renesas Private	The initial value of this bit is 0. This bit can be read and written but it is not allowed to change the value of this bit. Only 0 is allowed as the value to be written.
17	Pn_NSTRM__ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_NSTRM_STA. 1b: an interrupt due to Pn_INT_STA.Pn_NSTRM_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_NSTRM_STA is disabled.
16	Pn_PRIME__ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_PRIME_STA. 1b: an interrupt due to Pn_INT_STA.Pn_PRIME_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_PRIME_STA is disabled.
15 to 9	—	Reserved. This bit is read as 0b.
8	Pn_RCVNL__ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_RCVNL_STA. 1b: an interrupt due to Pn_INT_STA.Pn_RCVNL_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_RCVNL_STA is disabled.
7	Pn_ERDY__ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_ERDY_STA. 1b: an interrupt due to Pn_INT_STA.Pn_ERDY_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_ERDY_STA is disabled.
6	Pn_FLOW__ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_FLOW_STA. 1b: an interrupt due to Pn_INT_STA.Pn_FLOW_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_FLOW_STA is disabled.

Table 35.6-52 USB_PERI_Pn_INT_ENA Register Contents (2/2)

Bit Position	Bit Name	Description
5	Pn_DF__ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_DF_STA. 1b: an interrupt due to Pn_INT_STA.Pn_DF_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_DF_STA is disabled.
4	Pn_LSTTR__ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_LSTTR_STA. 1b: an interrupt due to Pn_INT_STA.Pn_LSTTR_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_LSTTR_STA is disabled.
3	—	Reserved. This bit is read as 0b.
2	Pn_STALL_ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_STALL_STA. 1b: an interrupt due to Pn_INT_STA.Pn_STALL_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_STALL_STA is disabled.
1	Pn_NRDY__ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_NRDY_STA. 1b: an interrupt due to Pn_INT_STA.Pn_NRDY_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_NRDY_STA is disabled.
0	Pn_BFRDY__ENA	This bit is used to enable the interrupt due to Pn_INT_STA.Pn_BFRDY_STA. 1b: an interrupt due to Pn_INT_STA.Pn_BFRDY_STA is enabled. 0b: an interrupt due to Pn_INT_STA.Pn_BFRDY_STA is disabled.

(36) PIPEn Reserved Packet Register (USB_PERI_Pn_RSVPKT)

This register shows the number of packets those are not transmitted yet in the buffer of PIPEn.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02DCh

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	Pn_RSVPKT				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-53 USB_PERI_Pn_RSVPKT Register Contents

Bit Position	Bit Name	Description
31 to 5	—	Reserved. These bits are read as 0b.
4 to 0	PIPEn Reserved Packet Number (Pn_RSVPKT[4:0])	This field shows the number of packets that are not transmitted yet in the buffer of PIPEn (n is 0 to 16). This field is valid only for IN PIPE.

Note: Once the access to one of P0_READ, Pn_READ, P0_WRITE and Pn_WRITE registers is started in order to read or write a packet, it is prohibited to access to other Px_yyy register before whole of a packet has been read or written with the register which is currently used. The access to these registers is controlled in a unit of a packet, so the targeted register can be changed at the point that the read or write of the current packet has been completed and the access for the next packet is not started yet.

(37) PIPEn Length Register (USB_PERI_Pn_LNG)

This register shows the number of bytes in received packet which is currently read from Pn_READ register.

Only 32-bit access is allowed to this register.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02E0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Pn_LENGTH															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-54 USB_PERI_Pn_LNG Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15 to 0	PIPEn Data Length (Pn_LENGTH[15:0])	This field shows the number of bytes in received packet which is currently read from Pn_READ register. The value is decremented every time Pn_READ register is read. Since Pn_READ register allows only 32-bit access, the value is decremented by 4. Since Pn_READ register is controlled in a unit of a packet, the length of received packet is shown in this register when the first 4 bytes of it are shown in Pn_READ register and have not been read yet. This field is valid only for OUT PIPE.

Note: Once the access to one of P0_READ, Pn_READ, P0_WRITE and Pn_WRITE registers is started in order to read or write a packet, it is prohibited to access to other Px_yyy register before whole of a packet has been read or written with the register which is currently used. The access to these registers is controlled in a unit of a packet, so the targeted register can be changed at the point that the read or write of the current packet has been completed and the access for the next packet is not started yet.

(38) PIPEn Read Register (USB_PERI_Pn_READ)

This register is used to read OUT data which has been received at PIPEn.

If there is no data in buffer, 00000000h is returned.

Only 32-bit access is allowed to this register.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02E4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Pn_RDATA															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Pn_RDATA															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-55 USB_PERI_Pn_READ Register Contents

Bit Position	Bit Name	Description
31 to 0	PIPEn Read Data (Pn_RDATA[31:0])	Read data from PIPEn. This register is controlled in a unit of a packet and cannot be read across the packet. That is, this register is updated in a unit of a packet. The current packet is never concatenated with the next packet even when the length of the current packet is not multiples of 4 and the last word of it is less than 4 bytes. In that case, the first 4 bytes of the next packet are shown in this register after the last word of the previous packet has been read. If the length of the current packet is not multiples of 4 and the last word of it is less than 4 bytes, the last word has one or more invalid bytes. In order to know how many valid bytes the last word has, see Pn_LENGTH[7:0] before the read of the packet and calculate from it. The valid bytes are aligned from Pn_RDATA[7:0]. This register is valid only for OUT PIPE

Note: Once the access to one of P0_READ, Pn_READ, P0_WRITE and Pn_WRITE registers is started in order to read or write a packet, it is prohibited to access to other Px_yyy register before whole of a packet has been read or written with the register which is currently used. The access to these registers is controlled in a unit of a packet, so the targeted register can be changed at the point that the read or write of the current packet has been completed and the access for the next packet is not started yet.

(39) PIPEn Write Register (USB_PERI_Pn_WRITE)

This register is used to write IN data which is to be transmitted from PIPEn.

Only 32-bit access is allowed to this register.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02E8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Pn_WDATA															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Pn_WDATA															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-56 USB_PERI_Pn_WRITE Register Contents

Bit Position	Bit Name	Description
31 to 0	PIPEn Write Data (Pn_WDATA[31:0])	Write data to PIPEn. This register is controlled in a unit of a packet and cannot be written across the packet. That is, it is not allowed to concatenate the current packet with the next packet to write them to this register even when the length of the current packet is not multiples of 4 and the last word of it is less than 4 bytes. In that case, the next packet can be written to this register after the write of the previous packet has been completed and it has been transmitted. This register is valid only for IN PIPE.

Note: Once the access to one of P0_READ, Pn_READ, P0_WRITE and Pn_WRITE registers is started in order to read or write a packet, it is prohibited to access to other Px_yyy register before whole of a packet has been read or written with the register which is currently used. The access to these registers is controlled in a unit of a packet, so the targeted register can be changed at the point that the read or write of the current packet has been completed and the access for the next packet is not started yet.

(40) PIPEn Stream ID Register (USB_PERI_Pn_STREAMID)

This register is used to set Stream ID for PIPEn for Stream bulk protocol.

Only 32-bit access is allowed to this register. Always set Pn_STREAMID[15:0] to 0000h.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02F0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Pn_STREAM_C [15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Pn_STREAM_N [15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.6-57 USB_PERI_Pn_STREAMID Register Contents

Bit Position	Bit Name	Description
31 to 16	PIPEn Stream ID (Pn_STREAM_C [15:0])	This field indicates the Stream ID that is currently valid. This field is invalid in case of HS/FS. This field is valid only in case that the type of transfer is bulk (Pn_TYPE = 10b) and Stream ID is supported (Pn_MOD.Pn_STREAM = 1) for PIPEn. When this field shows 0000h, it means that Stream ID is not set yet. This field is reset when Pn_CON.Pn_BCLR is set.
15 to 0	PIPEn Next Stream ID (Pn_STREAM_N [15:0])	This field indicates the Stream ID to be used in the next transfer at PIPEn. This field is invalid in case of HS/FS. This field is valid only in case that the type of transfer is bulk (Pn_TYPE = 10b) and Stream ID is supported (Pn_MOD.Pn_STREAM = 1) for PIPEn. When Pn_STREAM_C[15:0] is switched to the ID in this field, this field is reset to 0000h. Make sure to confirm that this field is reset to 0000h before setting new ID.

(41) PIPEn NRDY Stream ID Register (USB_PERI_Pn_NRDYSTRM)

This register shows Stream ID which was requested from host but responded with NRDY at PIPEn.

USB3PERI responds with NRDY for the Stream ID which is not equal to the current Stream ID in Pn_STREAM register.

Access Size: 32 bits

Address(es): <USB_S1_base> + 02F4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Pn_NRDYSTRM															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-58 USB_PERI_Pn_NRDYSTRM Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15 to 0	PIPEn NRDY Stream ID (Pn_NRDYSTRM [15: 0])	This field indicates Stream ID that was requested from host but responded with NRDY at PIPEn. USB3PERI responds with NRDY for the Stream ID which is not equal to the current Stream ID in Pn_STREAM register. This register is used to know what Stream ID is requested by host and rejected. This field is not updated in case that NRDY is returned due to NoStream or PRIME. This field is invalid in case of HS or FS.

35.6.3.4 SSIF Register

(1) Port Status and Control Register (USB_PERI_PORTSC)

Only 32-bit access is allowed to this register.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0300h

Initial Value: 0000_0080h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LWS
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	RW	R	R	RW0	R	R	R	R	RW0	W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PLS				—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	R	R	R	R	R

Table 35.6-59 USB_PERI_PORTSC Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 17	—	Reserved
16	Port Link State Write Strobe (LWS)	Write 1 to this bit in order to enable the write access to PLS[3:0]. When this bit is 0, writing to PLS[3:0] is ignored. This bit is write only and the value read from this bit is always 0.
15 to 9	—	Reserved. These bits are read as 0b.

Table 35.6-59 USB_PERI_PORTSC Register Contents (2/2)

Bit Position	Bit Name	Description
8 to 5	Port Link State (PLS[3:0])	[for write access] This field is used to request the direct transition of LTSSM state. For the timeout control of the transition to U1 or U2, see **Section 35.6.3.4(4), SSIF Command Register (USB_PERI_SSIFCMD)**. Set LWS bit to 1 when this field is written. As only 32-bit access is allowed to this register, make sure to set LWS to 1 in one word write for this register in order to change PLS[3:0]. When the same state as the current state is written to this field, the write access is ignored. If the transition using this function has not been completed but the next write access to this field comes, the next write data is also ignored. If the request of transition to U2 state is written during the transition to U1 state is being executed due to U1 timeout, the request is ignored. If the request of transition to U0 state is written when LTSSM state is in U1, U2 or U3 state, the exit operation or the resume operation is started. If the remote wakeup is requested when LTSSM state is U1 or U2 state, hardware executes the resume operation to U0 state automatically and PLS[3:0] shows U0 after the operation has been completed. 0h: Transition request to U0 state 1h: Transition request to U1 state 2h: Transition request to U2 state 3h to Fh: Reserved It is prohibited to request the transition to U1 or U2 state during control transfer. [for read access] This field shows the current state of LTSSM. 0h: U0 state 1h: U1 state 2h: U2 state 3h: U3 state 4h: Disabled state 5h: RxDetect state 6h: Inactivity state 7h: Polling state 8h: Recovery state 9h: Hot Reset state Ah: Compliance state Bh: Loopback state Ch to Fh: Reserved
4 to 0	—	Reserved. These bits are read as 0b.

(2) Port PM Status and Control Register (USB_PERI_PORTPMSC)

This register contains the status bits for the Force Link PM Accept bit and the timeout values for the U1 and U2 inactivity timers.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0304h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FLA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	U2_TIMEOUT								U1_TIMEOUT							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 35.6-60 USB_PERI_PORTPMSC Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b.
16	Force Link PM Accept (FLA)	This bit is set to 1b when Force LinkPM Accept bit in the received Set Link Function LMP equals to 1b. In case this bit shows 1, the port accepts LGO_U1 and LGO_U2 with no condition. This bit is cleared to 0 when Set Link Function LMP with Force LinkPM Accept bit = 0 is received. Software can write 0 to clear this bit (To write 1 is ignored), but basically this bit is set or reset on the reception of Set Link Function LMP.

Table 35.6-60 USB_PERI_PORTPMSC Register Contents (2/2)

Bit Position	Bit Name	Description
15 to 8	U2 Timeout (U2_TIMEOUT[7:0])	This field indicates the timeout value in the U2 inactivity timer. 00h: No timeout but LGO_Ux is always denied with LXU : default 01h: 256 us 02h: 512 us | FEh: 65.204 ms FFh: No timeout and LGO_Ux is basically accepted. (But it might be rejected due to other reasons.) This field is automatically updated when U2 Inactivity LMP is received. When this field has the value from 01h to FEh, it means the idle timeout value for LTSSM to request the transition from U0 state to U2 state as well as the idle timeout value for to make the transition from U1 state to U2 state. If U1_TIMEOUT[7:0] has 00h or FFh but U2_TIMEOUT[7:0] has a value from 01h to FEh, U2 timeout occurs although U1 timeout never. In that case USB3PERI never sends LGO_U1 but sends LGO_U2 to request the transition from U0 state to U2 state. If downstream port accepts the request, the downstream port and USB3PERI enter U2 state. Otherwise, U1 timeout occurs first and USB3PERI sends LGO_U1 to request the transition from U0 state to U1 state. If downstream port accepts the request, the downstream port and USB3PERI enter U1 state. If they stay in U1 state and U2 timeout occurs, they make the transition from U1 state to U2 state silently, without going back to U0 state. The transition is executed automatically by hardware when the timeout occurs. *Note*: This field is initialized to 00h during reset and just after a reset, but changed to FFh when USB3PERI detects a disconnection from USB3.1 device. If reset (in this case, it will be power on reset) is asserted but the device is in the disconnected state, FFh might be loaded to this field. Since this field is changed to FFh when a disconnection is detected, set the adequate value to this field after the connection if required.
7 to 0	U1 Timeout (U1_TIMEOUT[7:0])	This field indicates the timeout value in the U1 inactivity timer. 00h: No timeout but LGO_Ux is always denied with LXU: default 01h: 1 us 02h: 2 us | 7Fh: 127 us 80h-FEh: Reserved FFh: No timeout and LGO_Ux is basically accepted. (But it might be rejected due to other reasons.) This field is not automatically updated unlike U2_TIMEOUT[7:0]. Software is required to set this field. When this field has the value from 01h to 7Fh, it means the idle timeout value for LTSSM to request the transition from U0 state to U1 state. The hardware automatically sends LGO_U1 when the timeout occurs. If it is accepted, the transition is also executed by hardware automatically. *Note*: This field is initialized to 00h during a reset and just after a reset, but changed to FFh when USB3PERI detects a disconnection from USB3.1 device. If reset (in this case, it will be power on reset) is asserted but the device is in the disconnected state, FFh might be loaded to this field. Since this field is changed to FFh when a disconnection is detected, set the adequate value to this field after the connection if required.

(3) Port Link Information Register (USB_PERI_PORTLI)

This register indicates the number of errors detected.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0308h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LINK_ERCNT															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 35.6-61 USB_PERI_PORTLI Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15 to 0	Link Error Count (LINK_ERCNT[15:0])	This field shows the number of errors detected. This field is reset when LTSSM enters U0 state in the first link-up after warm reset is received or when LTSSM comes back to U0 state after hot reset is received.

(4) SSIF Command Register (USB_PERI_SSIFCMD)

This register issues the SSIF commands.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0340h

Initial Value: 030C_30C0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SSIF_URES[1:0]		SSIF_UDIR[1:0]		SSIF_UREQ[1:0]		—	—	—	—
Initial Value	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	R	R	R	R

Table 35.6-62 USB_PERI_SSIFCMD Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 10	—	Reserved. The value of this field is 00C30Ch.
9, 8	SSIF Reject LGO U1/U2 Request (SSIF_URES[1:0])	This field specifies the response of EPC when it receives LGO_U1 or LGO_U2. [bit1] This bit specifies the response when LGO_U2 is received. 0b: Normal response (default) USB3PERI basically accepts LGO_U2 (But it might be rejected due to other reasons). 1b: Forced LXU response USB3PERI never accepts LGO_U2 and always returns LXU to it. [bit0] This bit specifies the response when LGO_U1 is received. 0b: Normal response (default) USB3PERI basically accepts LGO_U1 (But it might be rejected due to other reasons). 1b: Forced LXU response USB3PERI never accepts LGO_U1 and always returns LXU to it.
7, 6	SSIF Reject Direct U1/U2 Request (SSIF_UDIR[1:0])	This field enables to transmit LGO_U1 or LGO_U2 when the transition to U1 or U2 state is requested directly through PORTSC.PLS[3:0]. The transition to U1 or U2 state can be requested by writing the state to PORTSC.PLS[3:0]. If SSIF_UDIR[1:0] enables to send LGO_U1 or LGO_U2, USB3PERI sends LGO_U1 or LGO_U2. If it is accepted, LTSSM transits to U1 or U2 state. If SSIF_UDIR[1:0] disables, EPC does not send LGO_U1 and LGO_U2 and writing to PORTSC_PLS[3:0] has no meaning. [bit1] This bit specifies the behavior when the transition to U2 state is requested. 0b: LGO_U2 is transmitted. 1b: LGO_U2 is not transmitted. (default) [bit0] This bit specifies the behavior when the transition to U1 state is requested. 0b: LGO_U1 is transmitted. 1b: LGO_U1 is not transmitted. (default)

Table 35.6-62 USB_PERI_SSIFCMD Register Contents (2/2)

Bit Position	Bit Name	Description
5, 4	SSIF Reject U1/U2 Request (SSIF_UREQ[1:0])	This field enables the transmission of LGO_U1 or LGO_U2 when the timeout on the U1/U2 inactivity timer occurs. [bit1] This bit specifies the behavior when the timeout on the U2 inactivity timer occurs. 0b: LGO_U2 is transmitted. (default) 1b: LGO_U2 is not transmitted. [bit0] This bit specifies the behavior when the timeout on the U1 inactivity timer occurs. 0b: LGO_U1 is transmitted. (default) 1b: LGO_U1 is not transmitted. *Note*: This field is initialized to 00b during reset and just after a reset, but changed to 11b when USB3PERI detects a disconnection from USB3.1 device. If reset (in this case, it will be power on reset) is asserted but the device is in the disconnected state, 11b might be loaded to this field. Since this field is changed to 11b when a disconnection is detected, set this field to enable the transmission of LGO_Ux after the connection if required.
3 to 0	—	Reserved. These bits are read as 0b.

(5) SSIF Link Setting 3 Register (USB_PERI_SSIFLINKSET3)

This register indicates the number of trials to detect.

Access Size: 32 bits

Address(es): <USB_S1_base> + 037Ch

Initial Value: 0760_0AC8h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	Renesas Private							—	—	—	—	SSIF_NUM_RDET			
Initial Value	0	0	0	0	1	0	1	0	1	1	0	0	1	0	0	0
R/W	R	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	RW	RW	RW	RW

Table 35.6-63 USB_PERI_SSIFLINKSET3 Register Contents

Bit Position	Bit Name	Description
31 to 15	—	Reserved. The value of this field is 00EC0h.
14 to 8	Renesas Private	The initial value of this field is 0Ah. This field can be read and written but it is not allowed to change the value of this bit. Only 0Ah is allowed as the value to be written.
7 to 4	—	Reserved. The value of this field is Ch.
3 to 0	SSIF Number of Receiver Detection (SSIF_NUM_RDET)	This field indicates the number of trials to detect the far-end receiver termination in RxDetect.Active state.

(6) SSIF Link Setting 4 Register (USB_PERI_SSIFLINKSET4)

This register controls the transmitter of USB3.1-PHY and the scrambling in TS1/TS2 Order Set.

Access Size: 32 bits

Address(es): <USB_S1_base> + 0380h

Initial Value: 0000_FF00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	SSIF_TXMGN			—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	RW	RW	RW	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SSIF_DEEMPH		—	—	—	SSIF_SWING	—	—	—	SSIF_SCRD
Initial Value	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	R	R	R	RW	R	R	R	RW

Table 35.6-64 USB_PERI_SSIFLINKSET4 Register Contents

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b.
22 to 20	SSIF TX Margin (SSIF_TXMGN[2:0])	This field indicates the level of transmitter voltage of USB3.1-PHY. 000b: Normal operation range 001b to 111b: Reserved *Note*: Use this field in default setting (= 000b).
19 to 10	—	Reserved. The value of this field is 03Fh.
9, 8	SSIF DEEMPH (SSIF_DEEMPH[1:0])	This field indicates the level of transmitter de-emphasis of USB3.1-PHY. 00b: −6.0db 01b: −3.5db 10b: 0.0db 11b: Default setting (The compliance test of CP6/CP8 uses 0dB setting. For others, de-emphasis shall be -3.5dB.)
7 to 5	—	Reserved. These bits are read as 0b.
4	SSIF Swing (SSIF_SWING)	This field indicates the level of transmitter swing voltage of USB3.1-PHY. 0b: Full swing (default) 1b: Half swing
3 to 1	—	Reserved. These bits are read as 0b.
0	SSIF Scrambling Disabled (SSIF_SCRD)	This bit is used to set the Disable Scrambling bit in TS1/TS2 Order Set. Write 1 to this bit when the Disable Scrambling bit is required to be set.

35.6.4 Details of Functions

This section describes the functions of USB3PERI.

The prefix (USB_PERI_) of the register names is omitted in this and subsequent sections.

35.6.4.1 VBUS Connection

VBUS is the power supply signal from USB host or hub, device can know that it is connected to host or hub when VBUS is asserted. But since VBUS input might be unstable just after device is connected, device should wait for a certain time till it becomes stable especially if it is bus-powered device. In order to control the interval from the assertion of VBUS to the time VBUS becomes stable, VBUS signal is not directly connected to link layer (ssif_us) but USB30_CON.B3_CONNECT is connected to it instead. The value of the bit is output to link layer which sees the value to know whether it is being connected or not. This mechanism enables that firmware inserts the wait time between when it detects the assertion of VBUS by USB_INT_STA_1.VBUS_CNG_STA and when it sets USB30_CON.B3_CONNECT.

In the same way, VBUS signal is not directly connected to some modules of USB3PERI and USB2.0-PHY but USB20_CON.B2_CONNECT is used to notify them that device is connected.

NOTE

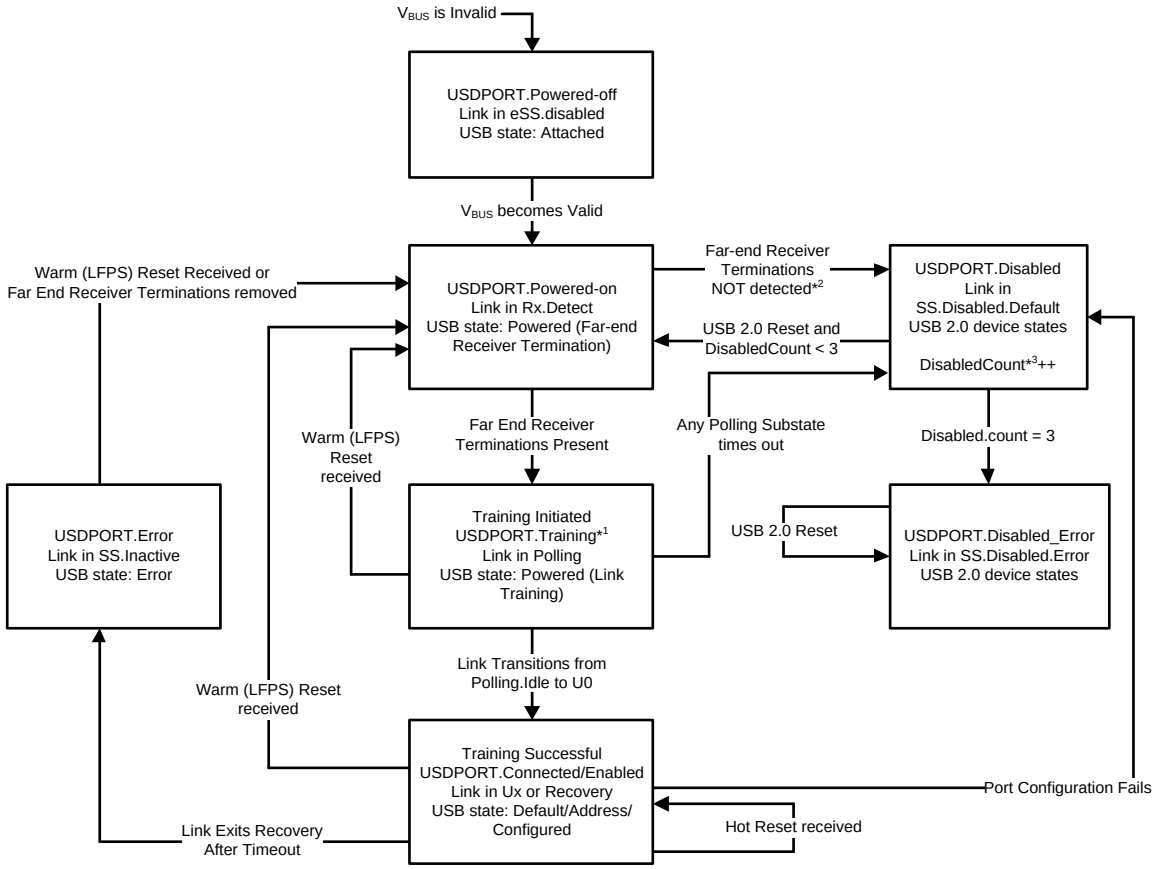
VBUS or USB30_CON.B3_CONNECT is not provided directly to USB3.1-PHY. USB3.1-PHY that is provided from Renesas is designed not to see the state of VBUS but to follow the instruction of power down from upper layer on POWERDOWN[1:0] for its power management. But some USB2.0-PHYs that is provided from Renesas are designed to see the state of VBUS and require that VBUS or similar signal is connected.

When device is in suspended state or unconnected, PLLs in USB3.1-PHY and USB2.0-PHY can be stopped in order to reduce their power consumptions. But if the device is disconnected when it is in suspended state, it means that the request to wake up from host never comes any more. In such case, it might be required to resume PLLs if they have been stopped so that device initializes by itself and prepares for the next connection. On the other hand, device might be required to resume PLLs if they have been stopped in unconnected state but device detects the connection. The state of connection or disconnection can be known on VBUS state. The change of VBUS state is notified on USB_INT_STA_1.VBUS_CNG_STA. As shown in the cases above, the software is required to control PLLs in USB3.1-PHY and USB2.0-PHY depending on VBUS state.

35.6.4.2 USB3.1/USB2.0 connection

In this section the outline of USB3.1 and USB2.0 connection in USB3.1 specification is explained. See **Section 35.6.5.3(6), USB2.0 Bus Reset Process** for details of the software flow.

The behavior of peripheral device upstream port state machine is described in 10.18.2 of USB3.1 specification Revision 1.0 July 26, 2013.



1. Peripheral Device must disconnect on USB2.0 within tUSB2SwitchDisconnect of entering this satte
2. If USPORT.Powered on was entered from any state except USPORT.Disabled then thistransition shall take place if Far-end Receiver Terminations (RRX-DC) are not detected after 8 successive Rx.Detect.Quiet to Rx.Detect.Active transitions. If USPORT.Powered on was entered from the USPORT.Disabled state, then this transition shall take place the first time that Far-end Receiver Terminations are not detected in the Rx.Detect.Active substate.
3. Disabled count is incremented each time the "Disabled" state is entered from the "Training Initiated" state. Disabled coount is reset to "0" each time the link completes PortConfiguration.

Figure 35.6-4 Peripheral Upstream Device Port State Machine (from Figure10-26 in USB3.1 specification)

As initial state, in which VBUS is off, the upstream port of the device is in USDPORT.Powered-off. The port should have the variable “DisabledCount” to control the transition to or from USDPORT.Disabled. The DisabledCount should be initialized to 0 when power is off or when the port’s link completes the port configuration.

When VBUS becomes valid (on), the port transits to USDPORT.Powered on. In this state, the port’s link is in Rx.Detect. On this first entry to USDPORT.Powered on, the port’s link makes the trial of Rx detection up to 8. If it detects Far End Receiver Termination of the link partner, the upstream port enters USDPORT.Training, and after the training has successfully completed it enters USDPORT.Connected/Enabled.

But if the port fails in the port configuration, it enters USDPORT.Disabled.

But if the port’t link cannot detect Far End Receiver Termination even when it tries 8 times, the port enters USDPORT.Disabled. With this transition DiableCount is incremented if it is less than 3. In this state, the function of USB3.1 is disabled once and the function of USB2.0 starts working.

If downstream port detects D+ line is pulled up, it recognizes the device wants to be connected as USB2.0 device. The downstream port asserts USB2.0 bus reset to start the process of USB2.0 connection.

Receiving USB2.0 bus reset, the upstream port returns to USDPORT.Powered on. On this entry to USDPORT.Powered on, the function of USB3.1 is enabled again and the port’s link makes the trial of Rx detection only one time. Note that the pull-up of D+ line is still enabled and the process of USB2.0 connection is still valid.

If the port’s link detects Far End Receiver Termination of the link partner, the upstream port enters USDPORT.Training and the connection as USB2.0 device is disabled within tUSB2SwitchDisconnect (= 1ms). If the port succeeds in the training, it enters USDPORT.Connected/Enabled.

But if the port’s link cannot detect Far End Receiver Terminaion, the function of USB3.1 is disabled again. When the port succeeds in USB2.0 connection, the device works in HS or FS of USB2.0. With this failure of Rx detection, the port enters USDPORT.Disabled as USB3.1 port and DisabledCount is incremented if it is less than 3.

If DisabledCount equals to 3 when the port enters USDPORT.Disabled, it makes the transition to USDPORT.Disabled_Error.

Whenever the port is in USDPORT.Disabled and USB2.0 bus reset comes, the port transits to USDPORT.Powered on and Rx detection for USB3.1 connection is started one time. Pull up of D+ can be seen from downstream port and USB2.0 connection is still active.

But if the port is in USDPORT.Disabled_Error when USB2.0 bus reset comes, it tries Rx detection no more and can only executes USB2.0 connection. Since DisabledCount is initialized to 0 when power is off or when the port configuration is completed, the port can exit from the state only when the power is removed.

35.6.4.3 Power Management Control

(1) USB3.1 Power Control

Table 35.6-65 USB3.1 Power Management

LTSSM State	USB3.1 PHY POWERDOWN	PLL Operation	Note
SS.Disabled	P2	Running	Default
	P0/P2	Running	The setting on USB30_CON.POW_SEL[2:0] is required.
	P3	Stopped	The setting on USB30_CON.POW_SEL[2:0] is required.
Rx.Detect	P2	Running	
U0	P0	Running	
U1	P1	Running	
U2	P2	Running	
U3	P0/P2	Running	Default Select P0 or P2 as the initial state on USB30_CON.U3_POW_SEL[1:0].
	P0/P2	Running	The setting on USB30_CON.POW_SEL[2:0] is required.
	P3	Stopped	The setting on USB30_CON.POW_SEL[2:0] is required.
U3 -> U3_Wakeup,Reset	P0	Running	Transition due to the reception of LFPS from host
U3 (P0/2) -> RemoteWakeup	P0	Running	The setting on PORTSC.PLS[3:0] is required after waking up PLL in USB3.1-PHY.
U3(P3) -> RemoteWakeup	P0	Running	The setting on USB30_CON.POW_SEL[2:0] is required.
Others	P0	Running	

Table 35.6-66 USB3.1 Power Management and Configured State

Configured/Unconfigured (CONF)	USB3.1 PHY POWERDOWN	CLK Gating			Note
		EPC	DLINK30		
		CLK125_P	CLK125	CLKLFPS	
Unconfigured	P0/P1/P2	Stopped	Running	Running	Only PIPE0 is accessible in EPC.
(CONF = 0)	P3	Stopped	Stopped	Running	PLL stopped
Configured	P0/P1/P2	Running	Running	Running	All PIPEs are accessible in EPC
(CONF = 1)	P3	Stopped	Stopped	Running	PLL Stopped

[The behavior of PHY_POWERDOWN[1:0] in Disconnected state (SS.Disabled)]

- P2 is designated on PHY_POWERDOWN[1:0] with default setting.
- P0 or P3 is selectable as the request on PHY_POWERDOWN[1:0] with the setting of USB30_CON.POW_SEL[2:0].

[The behavior of PHY_POWERDOWN[1:0] in U3 state]

- P0 or P2 is designated on PHY_POWERDOWN[1:0] depending on the setting of USB30_CON.POW_SEL[2:0].
- In order to place PHY in U3 state, the additional operation is required. See **Section 35.6.5.8(1), Suspend in USB3.1 (Transition of State from U0 to U3)** for details.

[In case of recovery from P3 (CLK125 is stopped in P3)]

- Transition from P3 to P0 can be requested on USB30_CON.B3_PLLWAKE or B3_PLL_WAKEIN signal. See **Section 35.6.5.8(6), USB3.1-PHY (PLL) Wakeup Process** for details.

(2) USB3.1 Power State Control

(a) In case downstream port requests the transition from U0 to U1

When LGO_U1 comes as the request of transition to U1 state from the downstream port, USB3PERI decides whether it accepts or not depending on the setting in registers and the internal status.

There are two fields in registers related to accepting LGO_U1, SSIFCMD.SSIF_URES[0] and USB30_CON.LPS_ENABLE[1:0].

SSIFCMD.SSIF_URES[0] is referred first in the decision whether LGO_U1 is accepted or not. If SSIFCMD.SSIF.URES[0] = 1 (forced LXU response), LGO_U1 is rejected and USB3PERI returns LXU. If SSIFCMD.SSIF.URES[0] = 0 (normal response), USB30_CON.LPS_ENABLE[1:0] is referred next.

If USB30_CON.LPS_ENABLE[1:0] = 10b (forced rejected), LGO_U1 is rejected and USB3PERI returns LXU. If USB30_CON.LPS_ENABLE[1:0] = 01b (forced accepted), LGO_U1 is accepted and USB3PERI returns LAU. If USB30_CON.LPS_ENABLE[1:0] = 00b (basically accepted), it depends on the internal status of USB3PERI whether it accepts LGO_U1 or not.

With USB30_CON.LPS_ENABLE[1:0] = 00b, LGO_U1 is rejected and USB3PERI returns LXU if one of the conditions below is satisfied. Otherwise, it is accepted and USB3PERI returns LAU.

- USB3PERI is still in U0 state
- 500 ms has not passed yet or the response from host has not come from the time when USB3PERI sends ERDY.
- ACK has not been received for the transmitted DP.
- IN PIPE has one or more packets to be transmitted in buffer.
- PP is 1 in the last packet received at OUT PIPE.

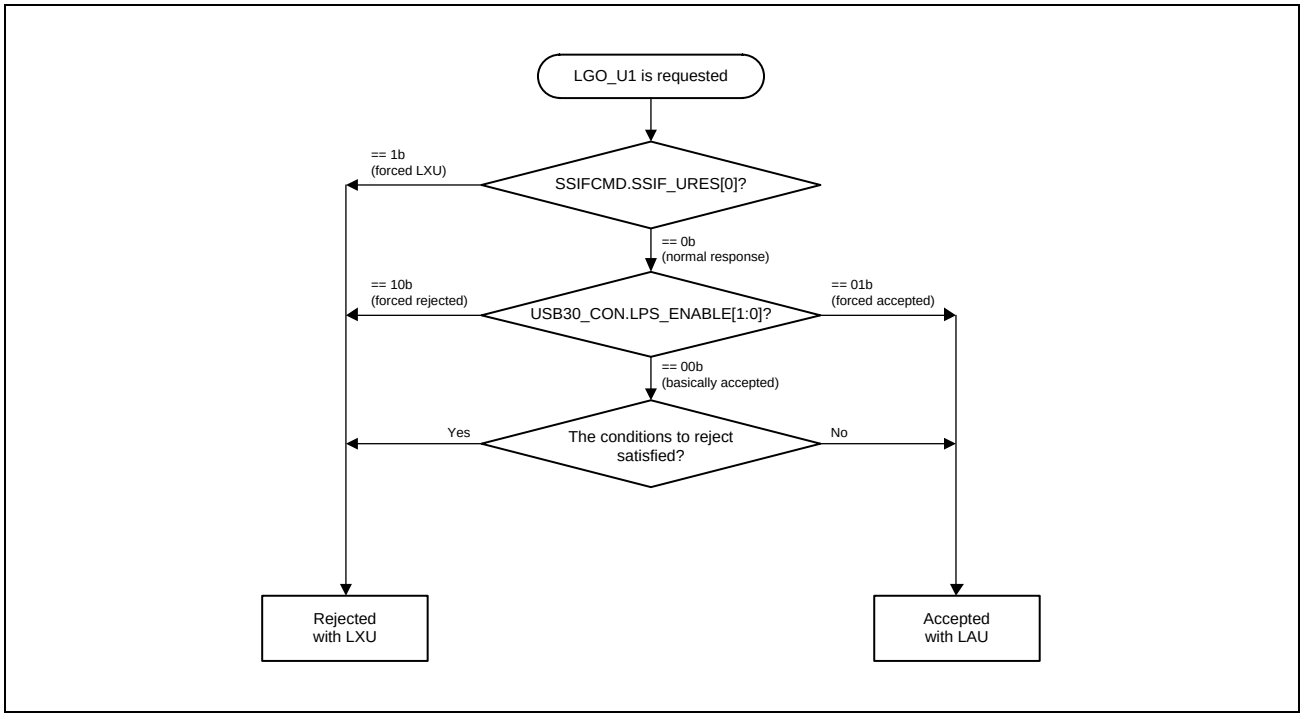


Figure 35.6-5 The Decision Flow Whether the Transition Request to U1 is Accepted or Not

(b) In case device requests the transition from U0 to U1

On the timeout of PORTPMSC.U1_TIMEOUT[15:0], USB3PERI requests the transition from U0 state to U1 state. But it depends on the setting in registers and the internal status of USB3PERI whether it really requests the transition from U0 state to U1 state.

There are two fields in registers related to sending LGO_U1, SSIFCMD.SSIF_UREQ[0] and USB30_CON.LPS_ENABLE[1:0].

SSIFCMD.SSIF.UREQ[0] is referred first in the decision whether LGO_U1 is sent or not. If SSIFCMD.SSIF.UREQ[0] = 1, LGO_U1 isn't sent and USB3PERI never requests the transition from U0 state to U1 state. If SSIFCMD.SSIF.UREQ[1] = 0, USB30_CON.LPS_ENABLE[1:0] is referred next.

If USB30_CON.LPS_ENABLE[1:0] = 10b (forced rejected), LGO_U1 isn't sent and USB3PERI never requests the transition from U0 state to U1 state. If USB30_CON.LPS_ENABLE[1:0] = 01b (forced accepted), LGO_U1 is sent and USB3PERI requests the transition from U0 state to U1 state on the timeout of PORTPMSC.U1_TIMEOUT[15:0]. If USB30_CON.LPS_ENABLE[1:0] = 00b (basically accepted), it depends on the internal status of USB3PERI whether it sends LGO_U1 or not.

With USB30_CON.LPS_ENABLE[1:0] = 00b, LGO_U1 isn't sent even when the timeout of PORTPMSC.U1_TIMEOUT[15:0] occurs if one of the conditions below is satisfied. Otherwise, LGO_U1 is sent and USB3PERI requests the transition from U0 to U1 on the timeout of PORTPMSC.U1_TIMEOUT[15:0].

- USB3PERI is still in U0 state.
- 500 ms has not passed yet or the response from host has not come from the time when USB3PERI sends ERDY.
- ACK has not been received for the transmitted DP.
- IN PIPE has one or more packets to be transmitted in buffer.
- PP is 1 in the last packet received at OUT PIPE.

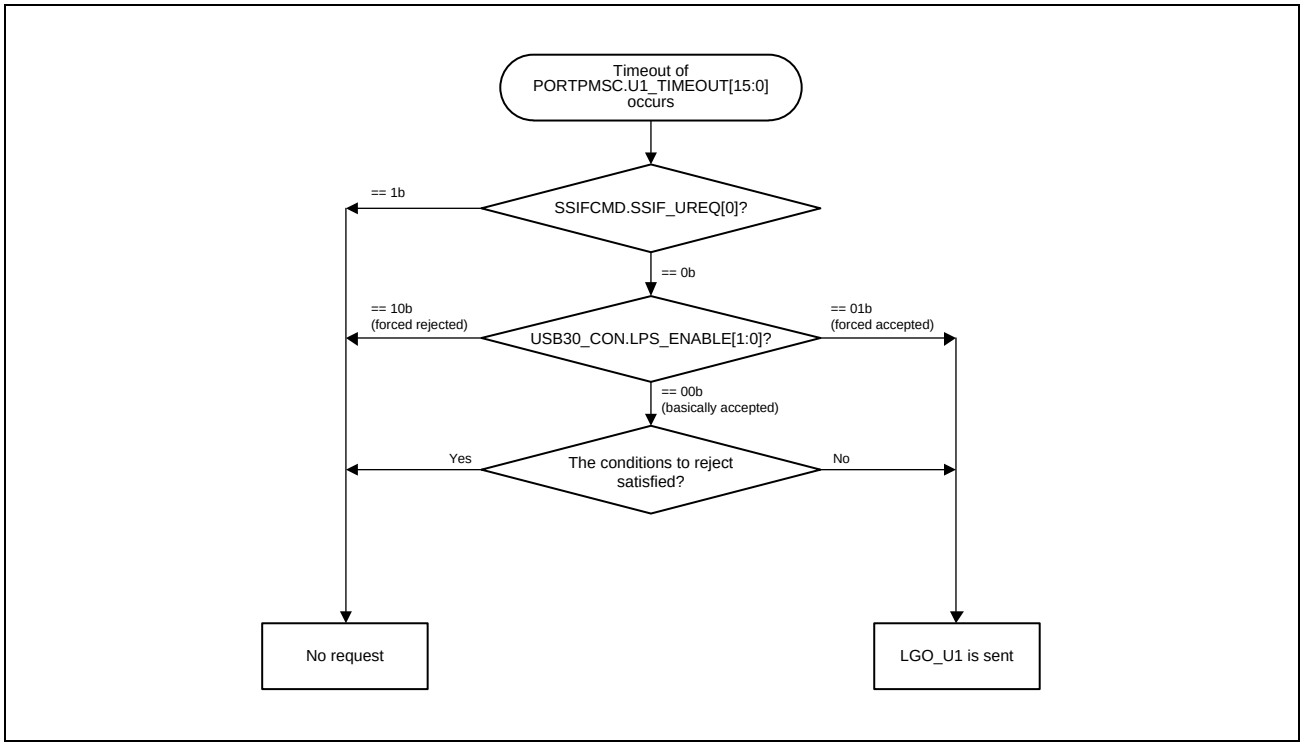


Figure 35.6-6 The Decision Flow Whether the Request of the Transition from U0 to U1 is Sent or Not

It is also available to use PORTPSC.PLS[3:0] in order to send LGO_U1 at any point the software wants. See **Section 35.6.5.8(11) Process of Transition from U0 to U1/U2 in USB3.1 (Initiated by Device)** for details.

(c) In case downstream port requests the transition from U1 to U0

When the downstream port wants to exit from U1 state and U1 Exit LFPS comes, USB3PERI automatically responds to it and returns to U0 state.

At that time, USB_INT_STA_1.B3_LNKCNG_STA is asserted and an interrupt due to it is asserted if enabled. PORTSC.PLS[3:0] shows U0 state (= 0h) after USB_INT_STA_1.B3_LNKCNG_STA is asserted.

(d) In case device requests the transition from U1 to U0

USB3PERI automatically requests the exit from U1 state to the downstream port by sending U1 Exit LFPS when one of the conditions below is satisfied.

- when USB3PERI wants to send ERDY for the next transfer
- when USB3PERI wants to send the transaction packet written in USB3_TPDAT_x registers

In the first case, USB3PERI sends ERDY when the packet to be transmitted is prepared in buffer for IN PIPE and when the PIPE becomes ready to receive the next packet (Pn_CON.Pn_RES[1:0] is changed from 00b to 01b, for example) for OUT PIPE.

In the second case, USB3PERI sends the transaction packet in USB3_TPDAT_x registers when USB30_CON.B3_TP_SEND is set to 1.

For both cases, the operations to send packet or start transfer are required, but there is no additional operation to exit from U1 state. Therefore, it is not required for user to mind whether the link is in U1 state or not before sending packet or starting transfer.

(e) In case downstream port requests the transition from U0 to U2

When LGO_U2 as the request of transition to U2 state from the downstream port comes, USB3PERI decides whether it accepts or not depending on the setting in registers and the internal status.

There are two fields in registers related to accepting LGO_U2, SSIFCMD.SSIF_URES[1] and USB30_CON.LPS_ENABLE[1:0].

SSIFCMD.SSIF.URES[1] is referred first in the decision whether LGO_U2 is accepted or not. If SSIFCMD.SSIF.URES[1] = 1 (forced LXU response), LGO_U2 is rejected and USB3PERI returns LXU. If SSIFCMD.SSIF.URES[1] = 0 (normal response), USB30_CON.LPS_ENABLE[1:0] is referred next.

If USB30_CON.LPS_ENABLE[1:0] = 10b (forced rejected), LGO_U2 is rejected and USB3PERI returns LXU. If USB30_CON.LPS_ENABLE[1:0] = 01b (forced accepted), LGO_U2 is accepted and USB3PERI returns LAU. If USB30_CON.LPS_ENABLE[1:0] = 00b (basically accepted), it depends on the internal status of USB3PERI whether it accepts LGO_U2 or not.

With USB30_CON.LPS_ENABLE[1:0] = 00b, LGO_U2 is rejected and USB3PERI returns LXU if one of the conditions below is satisfied. Otherwise, it is accepted and USB3PERI returns LAU.

- USB3PERI is still in U0 state.
- 500 ms has not passed yet or the response from host has not come from the time when USB3PERI sends ERDY.
- ACK has not been received for the transmitted DP.
- IN PIPE has one or more packets to be transmitted in buffer.
- PP is 1 in the last packet received at OUT PIPE.

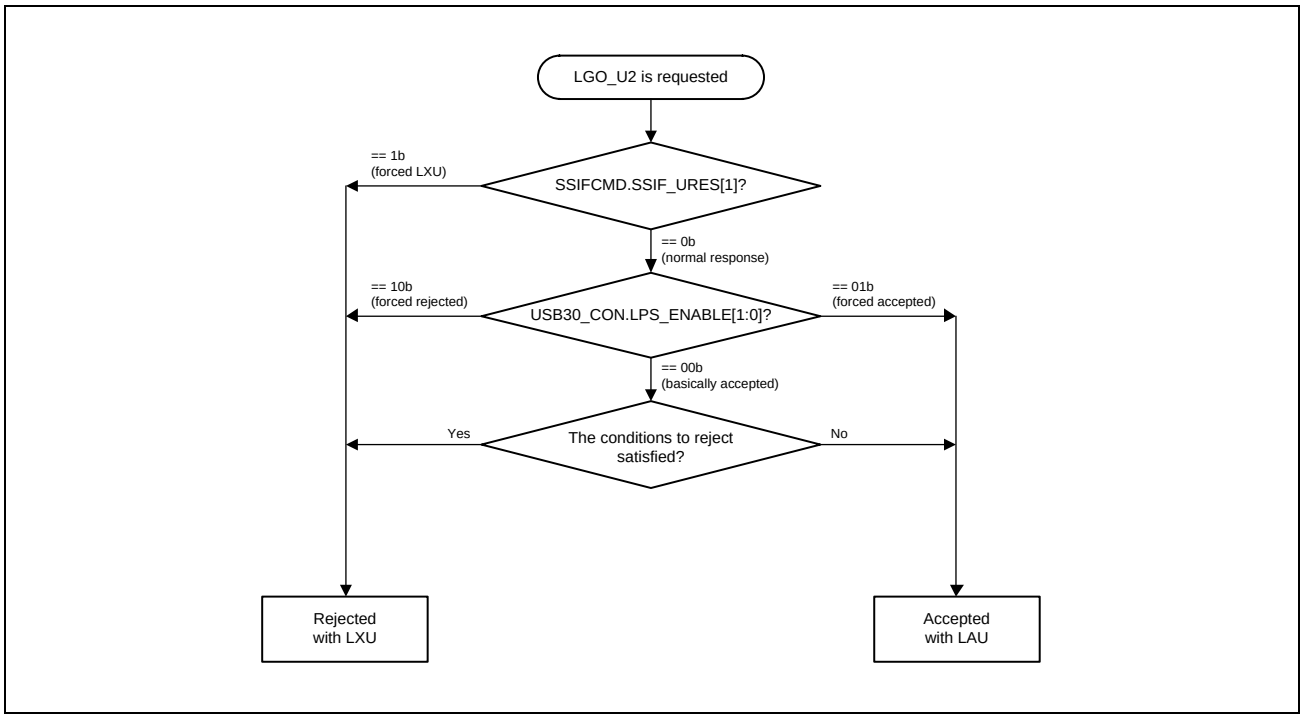


Figure 35.6-7 The Decision Flow Whether the Transition Request to U2 is Accepted or Not

(f) In case device requests the transition from U0 to U2

On the timeout of PORTPMSC.U2_TIMEOUT[15:0], USB3PERI requests the transition from U0 state to U2 state. But it depends on the setting in registers and the internal status of USB3PERI whether it really requests the transition from U0 state to U2 state.

But the timeout value in U1_TIMEOUT[15:0] is smaller than that in U2_TIMEOUT[15:0] in general. In that case, U1 timeout occurs first, then U2 timeout occurs next if the device is still in U1 state. See **Section 35.6.4.3(2)(g), In case device requests the transition from U1 to U2** for the case.

There are two fields in registers related to sending LGO_U2, SSIFCMD.SSIF_UREQ[1] and USB30_CON.LPS_ENABLE[1:0].

SSIFCMD.SSIF.UREQ[1] is referred first in the decision whether LGO_U2 is sent or not. If SSIFCMD.SSIF.UREQ[1] = 1, LGO_U2 isn't sent and USB3PERI never requests the transition from U0 state to U2 state. If SSIFCMD.SSIF.UREQ[1] = 0, USB30_CON.LPS_ENABLE[1:0] is referred next.

If USB30_CON.LPS_ENABLE[1:0] = 10b (forced rejected), LGO_U2 isn't sent and USB3PERI never requests the transition from U0 state to U2 state. If USB30_CON.LPS_ENABLE[1:0] = 01b (forced accepted), LGO_U2 is sent and USB3PERI requests the transition from U0 state to U2 state on the timeout of PORTPMSC.U2_TIMEOUT[15:0]. If USB30_CON.LPS_ENABLE[1:0] = 00b (basically accepted), it depends on the internal status of USB3PERI whether it sends LGO_U2 or not.

With USB30_CON.LPS_ENABLE[1:0] = 00b, LGO_U2 isn't sent even when the timeout of PORTPMSC.U2_TIMEOUT[15:0] occurs If one of the conditions below is satisfied. Otherwise, LGO_U2 is sent and USB3PERI requests the transition from U0 to U2 on the timeout of PORTPMSC.U2_TIMEOUT[15:0].

- USB3PERI is still in U0 state.
- 500 ms has not passed yet or the response from host has not come from the time when USB3PERI sends ERDY.
- ACK has not been received for the transmitted DP.

- IN PIPE has one or more packets to be transmitted in buffer.
- PP is 1 in the last packet received at OUT PIPE.

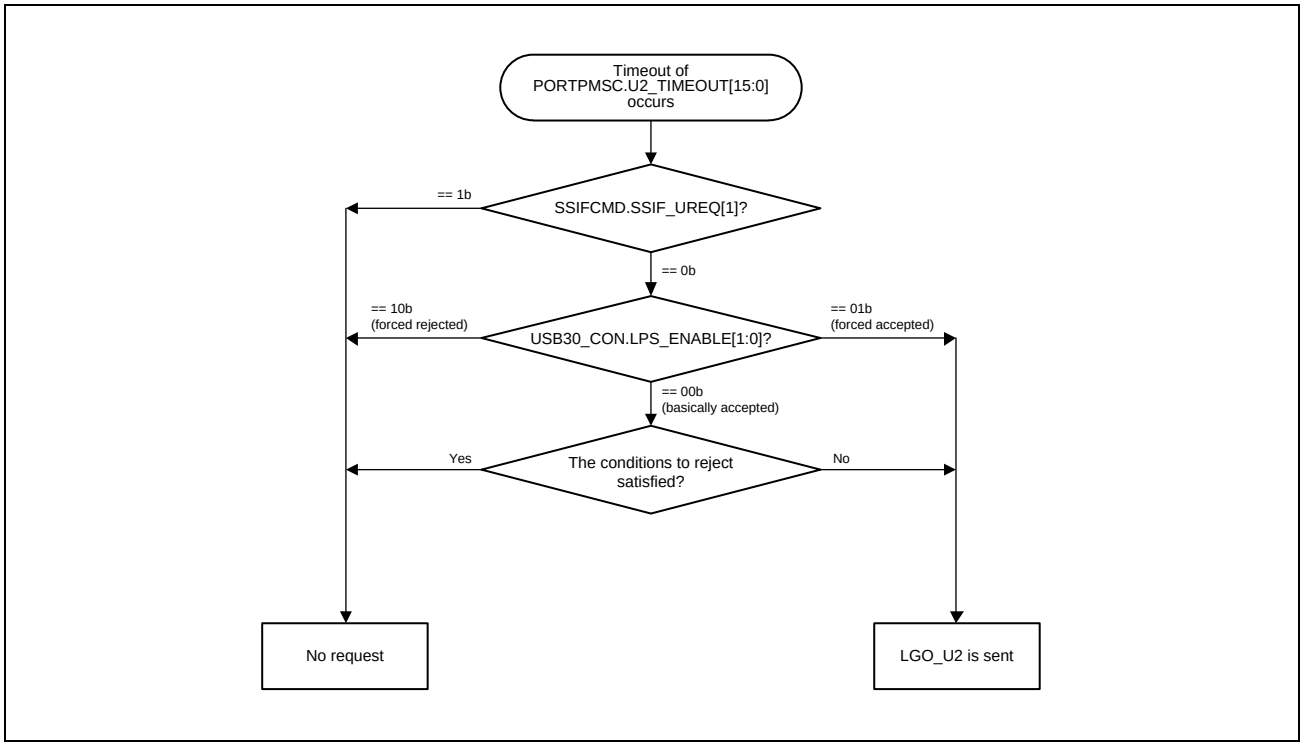


Figure 35.6-8 The Decision Flow Whether the Request of the Transition from U0 to U2 is Sent or Not

(g) In case device requests the transition from U1 to U2

As explained in **Section 35.6.4.3(2)(f), In case device requests the transition from U0 to U2**, when USB3PERI is in U1 state and the timeout of PORTPMSC.U2_TIMEOUT[15:0] occurs, USB3PERI transits from U1 state to U2 state without returning to U0 state. In that case, it is required that SSIFCMD.SSIF_UREQ[1] is set to 0.

(h) In case downstream port requests the transition from U2 to U0

When the downstream port wants to exit from U2 state and U2 Exit LFPS comes, USB3PERI automatically responds to it and returns to U0 state.

At that time, USB_INT_STA_1.B3_LNKCNG_STA is asserted and an interrupt due to it is asserted if enabled. PORTSC.PLS[3:0] shows U0 state (= 0h) after USB_INT_STA_1.B3_LNKCNG_STA is asserted.

(i) In case device requests the transition from U2 to U0

USB3PERI automatically requests the exit from U2 state to the downstream port by sending U2 Exit LFPS when one of the conditions below is satisfied.

- when USB3PERI wants to send ERDY for the next transfer
- when USB3PERI wants to send the transaction packet written in USB3_TPDAT_x registers

In the first case, USB3PERI sends ERDY when the packet to be transmitted is prepared in buffer for IN PIPE and when the PIPE becomes ready to receive the next packet (Pn_CON.Pn_RES[1:0] is changed from 00b to 01b, for example) for OUT PIPE.

In the second case, USB3PERI sends the transaction packet in USB3_TPDAT_x registers when USB30_CON.B3_TP_SEND is set to 1.

For both cases, the operation to send packet or start transfer is required, but there is no additional operation to exit from U2 state. Therefore, it is not required for user to mind whether the link is in U1 state or not before sending packet or starting transfer.

(j) In case downstream port requests the transition from U0 to U3

Only downstream port can initiate U3 entry. An upstream port shall not reject U3 entry.

USB3PERI automatically responds to LGO_U3, accepts it and transits to U3 state.
USB_INT_STA_1.B3_LNKCNG_STA is asserted and an interrupt due to it is asserted if enabled.
PORTSC.PLS[3:0] shows U3 state (=3h) after USB_INT_STA_1.B3_LNKCNG_STA is asserted.

But only with the transition to U3 above, USB3.1 PHY is placed in P0 state or P2 state. If it is required to place PHY in P3 state, See the flow shown in **Section 35.6.5.8(1), Suspend in USB3.1 (Transition of State from U0 to U3)**.

(k) In case downstream port requests the transition from U3 to U0

When the downstream port wants to exit from U3 state and U3 Wakeup LFPS comes, USB3PERI automatically responds to it and returns to U0 state.

At that time, USB_INT_STA_1.B3_LNKCNG_STA is asserted and an interrupt due to it is asserted if enabled.
PORTSC.PLS[3:0] shows U0 (= 0h) after USB_INT_STA_1.B3_LNKCNG_STA is asserted.

(l) In case device requests the transition from U3 to U0

USB3PERI automatically requests the transition from U3 state to U0 by sending U3 Wakeup LFPS when the transition is requested on PORTSC.PLS[3:0]. In U3, PORTSC.PLS[3:0] shows U3 state (= 3h). If PORTSC.PLS[3:0] is changed to U0 state (= 0h), USB3PERI sends U3 Wakeup LFPS to the link partner in order to request the transition from U3 state to U0 state.

When the LFPS handshake is completed and the link goes back to U0 state, USB_INT_STA_1.B3_LNKCNG_STA is asserted and an interrupt due to it is asserted if enabled. PORTSC.PLS[3:0] shows U0 state (= 0h) after USB_INT_STA_1.B3_LNKCNG_STA is asserted. See **Section 35.6.5.8(3), Resume in USB3.1 (from U3 to U0: Initiated by Device)** for details.

(3) USB2.0 Power Control

In the specification of USB2.0 link power management, L0 state is defined as “On” state.

L3 state is defined as “Off” state and corresponds to the powered-off, disconnected and disabled state.

L2 state is defined as “Suspend” state and corresponds to so-called “USB2.0 suspend” in the past.

L1 state is defined as “Sleep” state. LPM transaction is defined for the state.

Table 35.6-67 USB2.0 Power Management

State	Configured (CONF)	PLL Operation	CLK Gating				Supplement
			CLK60	CLK60_G	CLK60_P	CLK60_PG	
L3	—	Running	Running	Stopped	Stopped	Stopped	(default)
		Stopped	Stopped	Stopped	Stopped	Stopped	PLL stop is requested on USB20_CON.B2_SUSPEND
L0	Unconfigured (CONF = 0)	Running	Running	Running	Stopped	Stopped	Only PIPE0 is running
	Configured (CONF = 1)	Running	Running	Running	Running	Running	All PIPEs are running
L1/L2		Running	Running	Stopped	Running	Stopped	(default)
		Stopped	Stopped	Stopped	Stopped	Stopped	PLL stop is requested on USB20_CON.B2_SUSPEND
L1/L2 → L0		Running	Running	Running	Running	Running	Wakeup received from Host
		Running	Running	Running	Running	Running	Remote wakeup initiated by device

Note: CLK60 is a main clock used for USB2.0 related logic.
CLK60P is a generated clock from CLK60, and used for PIPEs other than PIPE0.
CLK60_G and CLK60_PG are generated clock from CLK60 and CLK60_P, respectively.

[L3 (Off) State]

- Disconnected state for USB2.0
- PLL is running in default setting but it can be stopped on USB20_CON.B2_SUSPEND.
- 60MHz clock other than CLK60 is suspended.

[L0 (On) State]

- Active state in USB2.0 connection
- PLL is running.
- In unconfigured state, CLK60_P and CLK60_PG are suspended. It means that clock to PIPEs other than PIPE0 is suspended.
- In configured state, all clocks of 60MHz is running.

[L1 (Sleep) State]

- Low power state selected on LPM in USB2.0 connection
- PLL is running.
- CLK60_G and CLK60_PG are suspended.

[L2 (Suspend) State]

- Suspended state in USB2.0 connection
- PLL is running but it can be stopped on USB20_CON.B2_SUSPEND.
  PLL is resumed automatically when the wakeup request from downstream port is received.
- CLK60_G and CLK60_PG are suspended.

(a) Transition from L0 to L1

L1 state in USB2.0 is similar to U1 state and U2 state in USB3.1 in the point that the hardware should control the transition to or the exit from the state mainly. But unlike the transition to U1 state or U2 state, the transition to L1 state is initiated only by a downstream port.

LPM token is defined as one of an extended token packet for the transition. The device returns ACK if it accepts the transition or NYET if it rejects the transition when LPM token comes. It is also allowed to return STALL if it does not support LPM functions.

USB3PERI can respond with “no response” or return STALL to LPM token with the setting to do so, but it should return only ACK or NYET basically.

When LPM token from the downstream port comes, USB3PERI decides whether it accepts or not depending on the setting in the registers and the internal status.

LPM functions can be enabled or disabled on USB20_CON.LPM_DISABLE. When USB20_CON.LPM_DISABLE = 1, USB3PERI disables LPM functions and return no response to LPM token and take no action for it. But the device should support LPM functions, so it should enable LPM functions.

USB20_CON.LPM_ENABLE[1:0] also defines the response of USB3PERI to LPM token. If USB20_CON.LPM_ENABLE[1:0] = 10b (forced rejected), the request is rejected and USB3PERI returns NYET to LPM token. If USB20_CON.LPM_ENABLE[1:0] = 01b (forced accepted), the request is accepted and USB3PERI returns ACK to LPM token. If USB20_CON.LPM_ENABLE[1:0] = 00b (basically accepted), it depends on the internal status of USB3PERI whether it accepts the request or not. If USB20_CON.LPM_ENABLE[1:0] = 11b (unsupported), USB3PERI returns STALL to LPM token. But the device should not return STALL if it supports LPM functions.

If one of the conditions below is satisfied, the request is rejected and USB3PERI returns NYET. Otherwise, it is accepted and USB3PERI returns ACK.

- IN PIPE has one or more packets to be transmitted in buffer.

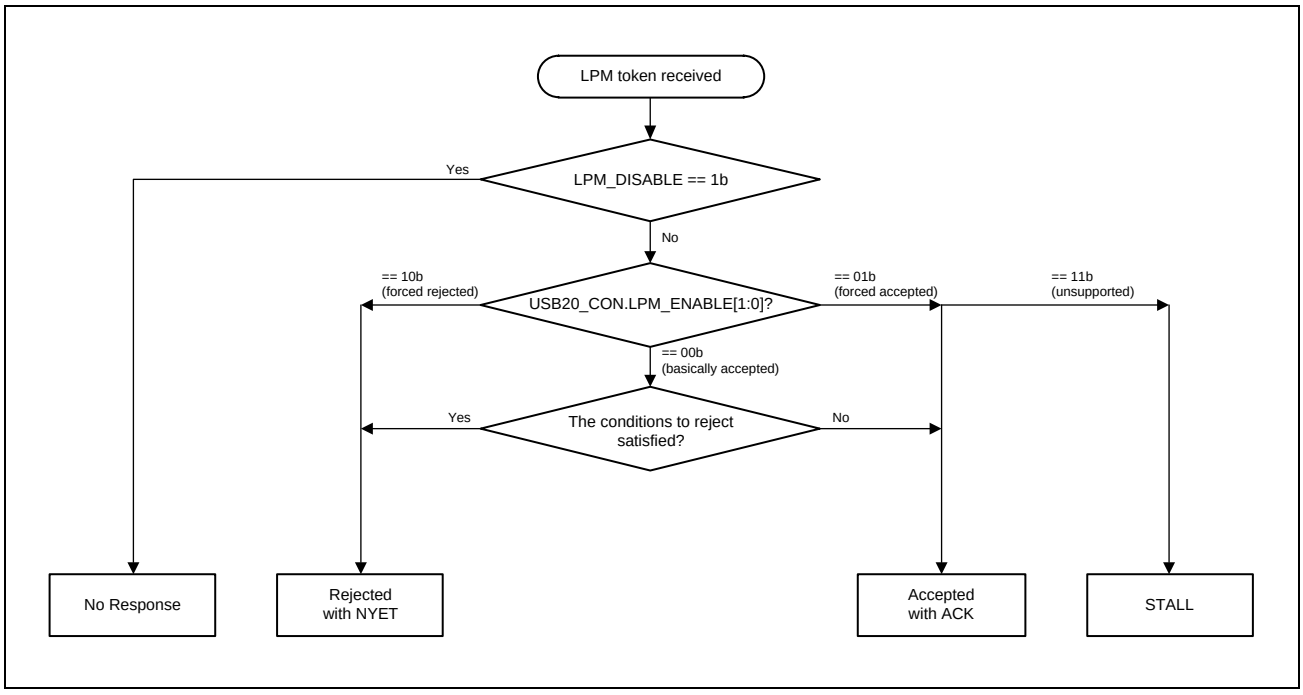


Figure 35.6-9 The Decision Flow Whether the Transition Request to L1 is Accepted or Not

The software can know that the transition to L1 state is requested on USB_INT_STA_1.B2_L1SPND_STA. An interrupt due to it is asserted if enabled.

(b) In case downstream port requests the transition from L1 to L0

When the downstream port wants to exit from L1 state and the resume signal comes, USB3PERI automatically responds to it and returns to L0 state.

At that time, USB_INT_STA_1.B2_L1RSUM_STA is asserted and an interrupt due to it is asserted if enabled.

(c) In case device requests the transition from L1 to L0

USB3PERI automatically requests the exit from L1 state to the downstream port by sending the resume signal when it has one or more packets to be transmitted in buffer for IN PIPE. In this case, there is no additional operation to exit from L1 state.

The transition from L1 state to L0 state is also required by setting USB20_CON.B2_RSUM_IN. When this bit is set, the resume signal to request the exit from L1 state is sent to the downstream port.

(d) Transition from L0 to L2 (Suspend)

L2 state is defined as USB2.0 Suspend in the original USB2.0 specification. The transition to L2 state is requested only from downstream port and is controlled automatically by the hardware of USB3PERI.

The downstream port can request the transition to L2 state by stopping any bus activity and put USB bus in a constant idle state for more than 3.0 ms and device cannot deny the transition.

When USB3PERI detects that the transition to L2 state is being requested from downstream port (that is, USB bus stays in idle state for more than 3.0 ms), it automatically follows it and asserts USB_INT_STA_1.B2_SPND_STA.

USB3PERI follows to the request of the transition to L2 state, but PLL in USB2.0-PHY is still running in L2 state. If it is required to stop PLL, set USB20_CON.B2_SUSPEND. See **Section 35.6.5.8(7), Suspend in USB2.0** for details.

(e) In case downstream port requests the transition from L2 to L0

When the downstream port wants to exit from L2 state and the resume signal comes, USB3PERI automatically responds to it and returns to L0 state.

At that time, USB_INT_STA_1.B2_RSUM_STA is asserted and an interrupt due to it is asserted if enabled.

(f) In case device requests the transition from L2 to L0

The sofware can requests the wakeup of USB3PERI from L2 state. If PLL in USB2.0-PHY is suspended, it should be awaken first. See **Section 35.6.5.8(10), USB2.0 PHY (PLL) Wakeup Process** for how to awake PLL in USB2.0-PHY.

After PLL is resumed, the software can send the resume signal from USB3PERI by setting USB20_CON.RSUM_IN. See **Section 35.6.5.8(9), Resume in USB2.0 (Initiated by Device)** for details

35.6.4.4 AXI DMA Transfer Control

USB3PERI executes DMA transfer to or from data buffers connected to SRAM interface using the bus master function of AXI-IF. The DMA master function of AXI-IF uses Physical Region Descriptor (PRD) Table on system memory, which has a source address, a destination address, a size of transfer and other information related to the DMA transfer. It is assumed that the software (driver, for example) prepares PRD table on system memory. PRD tables are prepared separately for each PIPE.

The operation flow of DMA transfer using master function of AXI-IF is described below.

(1) OUT Transfer

(1) Interrupt is asserted if PRD table is not prepared
AXI-IF asserts AXI_INT_SYS if a certain PIPE receives OUT packet and the OUT packet becomes ready to be read but PRD table is not prepared for it yet.
If PRD table is already prepared for the PIPE and DMA transfer is enabled, AXI-IF does not assert AXI_INT_SYS here. In that case, (2) and (3) can be skipped.

(2) Making PRD table
The software makes PRD table according to the defined format.

(3) Setting for bus master
The software specifies PRD table made at (2) to registers of AXI-IF, and enables DMA transfer.

(4) Start of DMA transfer
AXI-IF reads PRD table when it detects EPC_D_Pn_DATAEN[n] (n is the index of the PIPE for which PRD table is prepared for) is asserted and knows EPC requests DMA transfer. Then, AXI-IF writes received data in a unit of packet to the address which is assigned by PRD table.

(5) Writing back the result of transfer to PRD table
When DMA transfer is completed, AXI-IF writes back the result of transfer to PRD table.

(6) Interrupt is asserted to notify completion of DMA transfer
AXI-IF asserts AXI_INT_DMA when it completes DMA transfer.

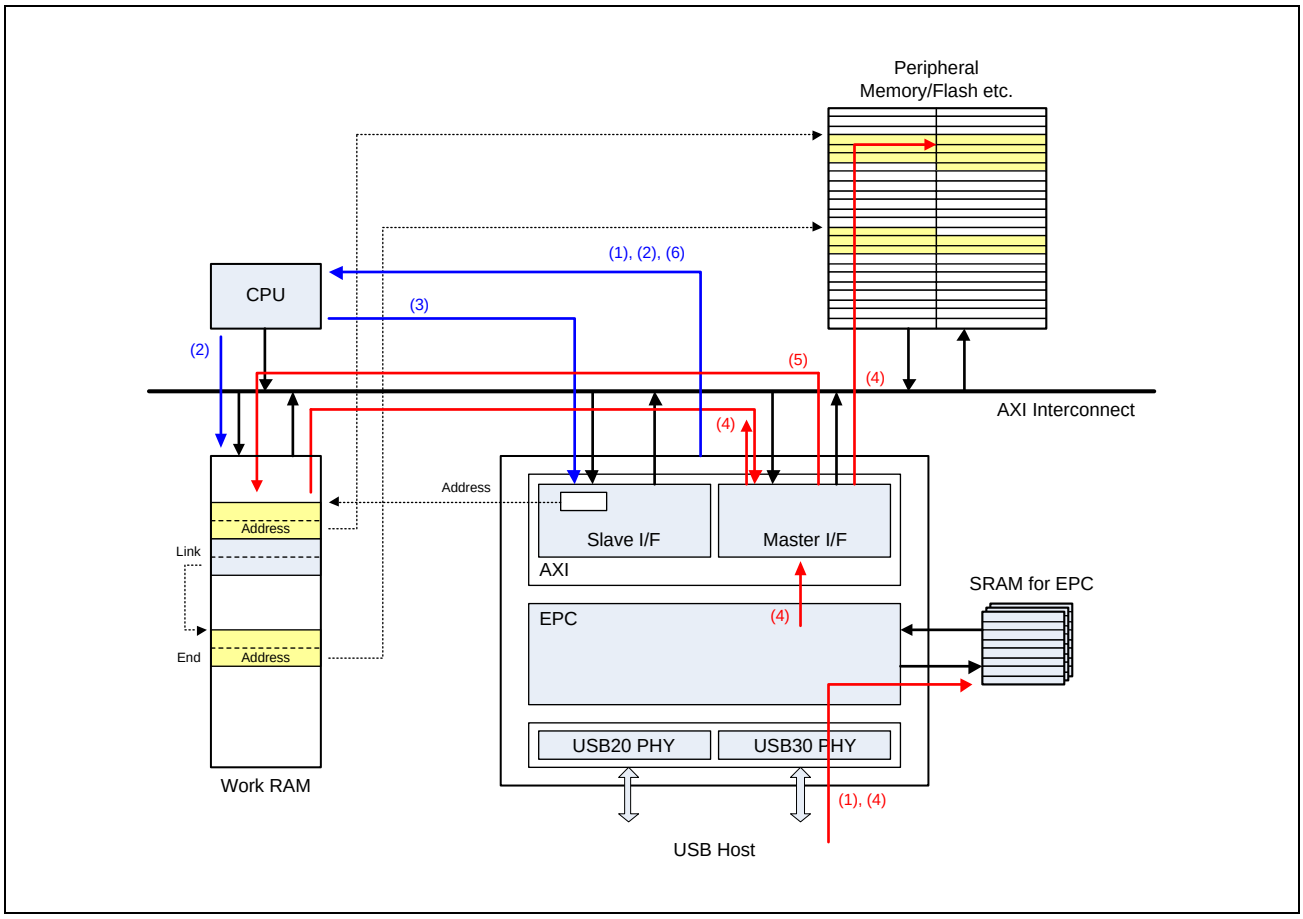


Figure 35.6-10 Example of Operation for OUT Transfer

(2) IN Transfer

(1) Interrupt asserted if PRD table is not prepared
AXI-IF asserts AXI_INT_SYS if a certain PIPE becomes ready to be written for IN packet but PRD table is not prepared for it yet.
If PRD table is already prepared for the PIPE and DMA transfer is enabled, AXI-IF does not assert an interrupt. In that case, (2) and (3) can be skipped.

(2) Making PRD table
The software makes PRD table according to the defined format.

(3) Setting for bus master
The software specifies PRD table made at (2) to registers of AXI-IF, and enables DMA transfer.

(4) Start of DMA transfer
AXI-IF reads PRD table when it detects EPC_D_Pn_DATAEN[n] (n is the index of the PIPE for which PRD table is prepared for) is asserted and knows EPC requests DMA transfer. Then, AXI-IF read data to be transmitted in unit of a packet from the address which is assigned by PRD table.

(5) Write back of result of transfer to PRD table
When DMA transfer is completed, AXI-IF writes back the result of transfer to PRD table.

(6) Interrupt asserted to notify completion of DMA transfer
AXI-IF asserts AXI_INT_DMA when it completes DMA transfer.

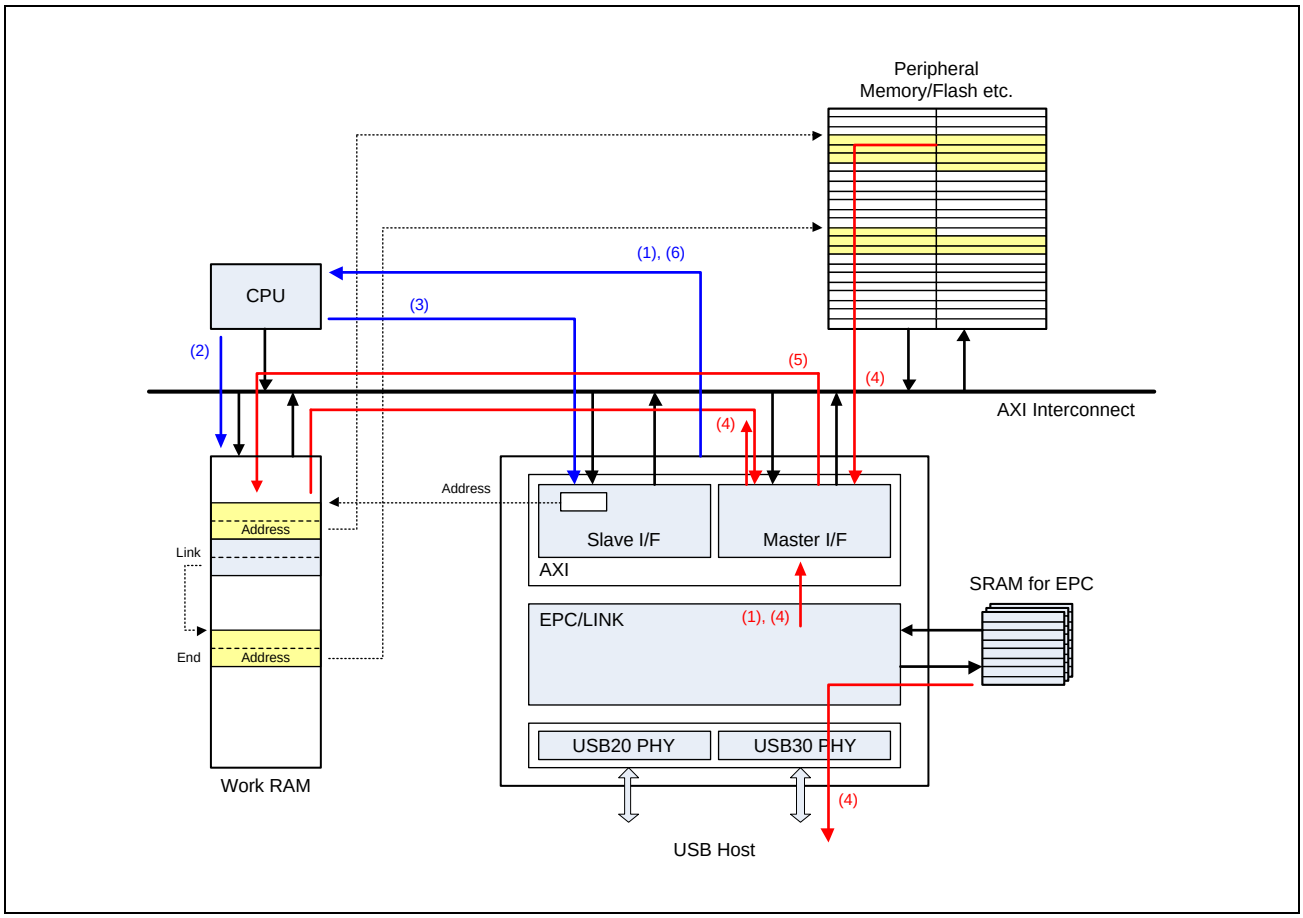


Figure 35.6-11 Example of Operation for IN Transfer

(3) Two PRD Tables for One Group of Transfer

The basic concept of two PRD tables used for one group of transfer is described below. Especially the Stream bulk protocol is assumed here.

For Stream bulk transfer, Stream ID is assigned to USB3PERI and it executes transfer related to the Stream ID. The Stream ID is set before PRD table is allocated to USB3PERI.

From the viewpoint of the performance of system, it is desirable to prepare for the next transfer just before the current OUT transfer is completed. USB3PERI can execute transfer seamlessly in that case.

In order to do so, there is a way to use PRD tables for one group of transfer.

Two PRD tables are prepared so that the group of transfer is divided to them beforehand. One PRD table has the part from the first packet to the (n)-th packet, and the other table has that from the (n+1) th packet to the last packet. The (n) is assumed as the second or the third packet from the last. The Int bits are set for both tables. With this usage, the software can know the current transfer is almost completed by the interrupt of the first PRD table. When the interrupt of the first PRD table comes, software can start the preparation for the next transfer. It can also confirm the completion of the current transfer by the interrupt of the second PRD table.

This method is applicable for non Stream bulk transfer.

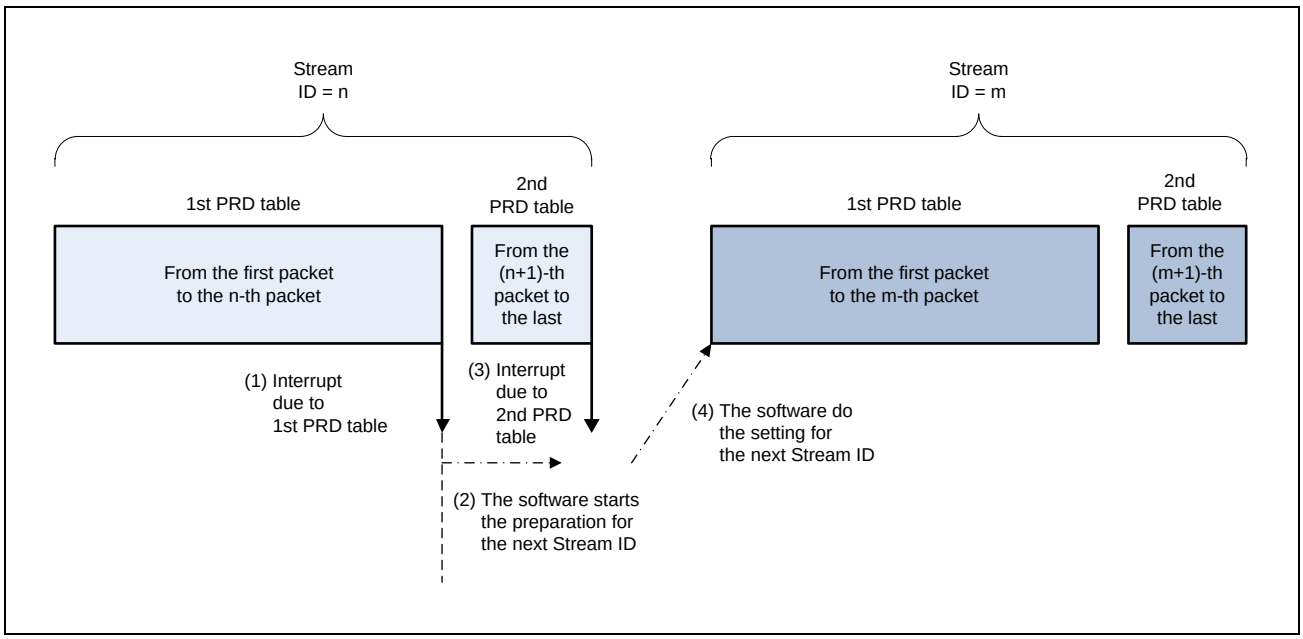


Figure 35.6-12 Two PRD Tables Used for One Group Transfer

(4) DMA Transfer using EXTPRD_EN

AXI-IF has four register groups used for DMA transfers, -- DMA_Ch0_CONx and DMA_Ch0_PRD_ADRx (x = 1-4). AXI-IF can coordinate multiple PRD tables and their transfers by making links between those PRD tables on DMA_Ch0_CONx.EXPRD_ENx and DMA_Ch0_CONx.EXTPRD_NOx[1:0].

An example in case that multiple PRD tables and their transfers are coordinated on DMA_Ch0_CONx.EXPRD_ENx is described below. In this example, PRD tables from (1) to (4) are set to registers at first, and then PRD table of (5) is set after DMA transfer of (1) is completed. Since DMA_Ch0_CONx.EXPRD_ENx is set to 1 for (2), (3) and (5), each DMA_Ch0_CONx.PRD_ENx is masked and each DMA transfer is kept waiting until the transfer related on DMA_Ch0_CONx.EXTPRD_NOx[1:0] is completed.

As for (2), DMA_Ch0_CON2.EXTPRD_NO2[1:0] = 0 is specified. In this case, the transfer related to (2) is suspended until the transfer at PIPE1 with DMA_Ch0_CON1 is completed. When the transfer at PIPE1 with DMA_CH0_CON1 is completed and DMA_Ch0_CON1.PRD_EN1 is cleared by hardware, DMA_Ch0_CON2.EXTPRD_EN2 is cleared automatically by hardware at the same time. The clearing of DMA_Ch0_CON2.EXTPRD_EN2 means that DMA_Ch0_CON2.PRD_EN2 gets unmasked, and the transfer of (2) is allowed at this point.

[Example of PRD Table Setting]

No.		PRD_EN	PIPE_NO	EXTPRD_EN	EXTPRD_NO
(1)	DMA_Ch0_CON1	1	PIPE1	0 (Normal)	—
(2)	DMA_Ch0_CON2	1	PIPE1	1 (Expanded)	0 (CON1)
(3)	DMA_Ch0_CON3	1	PIPE2	1 (Expanded)	1 (CON2)
(4)	DMA_Ch0_CON4	1	PIPE3	0 (Normal)	—
(5)	DMA_Ch0_CON1	1	PIPE1	1 (Expanded)	2 (CON3)

[Example of Operation]

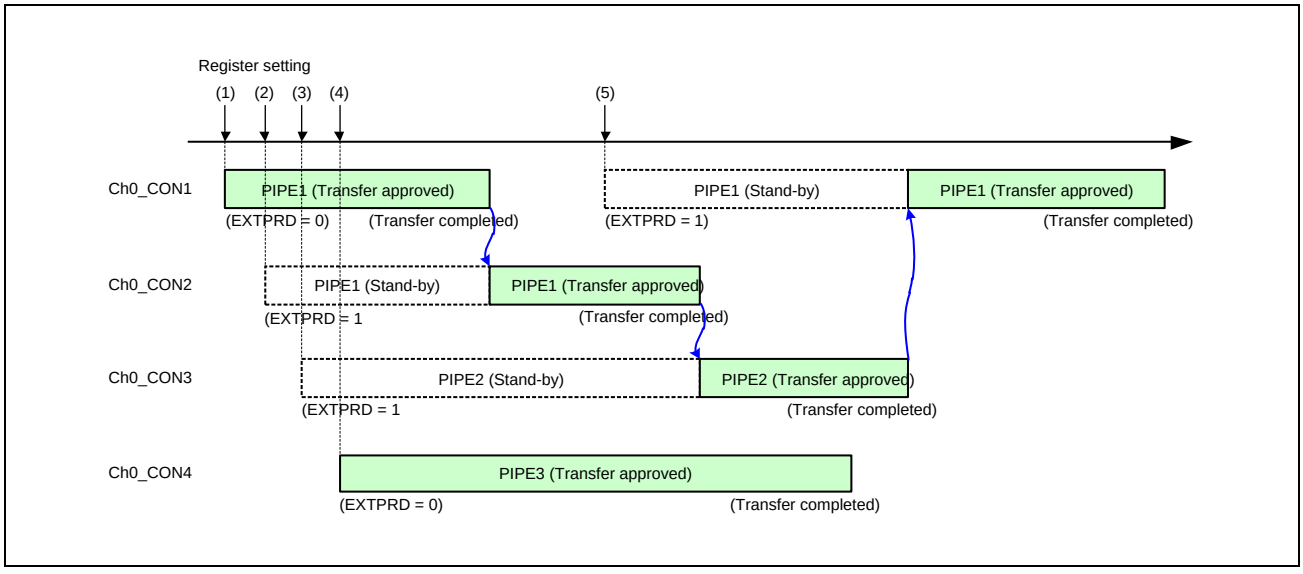


Figure 35.6-13 Transfer Using EXTPRD_EN

This function is also used for the case a certain PIPE is expected to start the transfer just after that at other PIPE is completed.

DMA_Ch0_CONx.EXTPRD_NOx[1:0] and DMA_Ch0_CONx.EXTPRD_ENx should be set before the transfer for PRD table related on DMA_Ch0_CONx.EXTPRD_NOx[1:0] is completed (when it is completed, DMA_Ch0_CONx.PRD_ENx is cleared). Make sure that DMA_Ch0_CONx.PRD_ENx is still 1 just when DMA_Ch0_CONx.EXTPRD_NOx[1:0] and DMA_Ch0_CONx.EXTPRD_ENx are set and related to it. If DMA_Ch0_CONx.PRD_ENx has already been cleared, do not use DMA_Ch0_CONx.EXTPRD_NOx[1:0] and DMA_Ch0_CONx.EXTPRD_ENx for it.

(5) Example of transfer using bus master function

An Example in which short packet is received as the last one at OUT (AXI write) PIPE is described below.

AXI-IF provides 4 register groups to have the information of PRD Tables. The software prepares PRD Table on system memory and requests the transfer by setting the start address of PRD table, the information of PIPE (index of PIPE and direction of transfer) and DMA_Ch0_CONx.PRD_ENx to one of register groups. Especially setting of DMA_Ch0_CONx.PRD_ENx to 1 means the transfer on the PIPE is enabled.

EPC indicates whether transfer is enabled or not for each PIPE on EPC_D_Pn_DATAEN[n] (n = 1-15), which is one of the signals at Data Interface of EPC.

AXI-IF is kept waiting until EPC notifies it that the transfer of PIPE related on the PRD table is enabled. AXI-IF starts the transfer when it detects that one of transfers related on PRD tables is enabled.

Upon the start of transfer, AXI-IF reads the first PRD table. When the type of PRD table is a link pointer, AXI-IF executes writing-back in order to set used bit of the PRD table first and then reads the next PRD table from the address which is held in BAP. When the type of PRD table is a buffer pointer, AXI-IF starts data transfer according to the PRD table.

EPC executes data transfer at Data Interface in a unit of a packet of USB (the size of packet is up to the max packet size of USB).

When the transfer of the packet is completed, AXI-IF updates the PRD table that was read just prior to the transfer and writes back it so that SIZE field and BAP field in the table are updated. If the remain size of the PRD table is not zero and EPC notifies AXI-IF that it can still continue transfer of the PIPE when AXI-IF completes writing-back of PRD table, AXI-IF uses PRD table currently held and start transfer of the next packet for the PIPE. On the contrary, in case that all transfers specified by the PRD table held currently in AXI-IF have been done, case that the transfer for the PRD table is terminated by receiving short packet or case that EPC notifies that no transfer on the PIPE is pending, AXI-IF returns back to the status to wait for transfer.

When the transfer is completed, the size information in SIZE field of table is updated to the value that the size of transferred packet is subtracted from the remaining size before the transfer, then AXI-IF writes back the PRD table.

If it is required to know the actual size transferred, store the remaining size before the transfer, and subtract the size in the updated PRD table after the transfer from it.

In case that short packet is received in the middle of PRD Table or case that all transfers specified by PRD table have been completed, AXI-IF completes the process of the current PRD table. At this time AXI-IF clears DMA_Ch0_CONx.PRD_ENx, sets the status bit in DMA_INT_STA register and asserts AXI_INT_DMA if enabled.

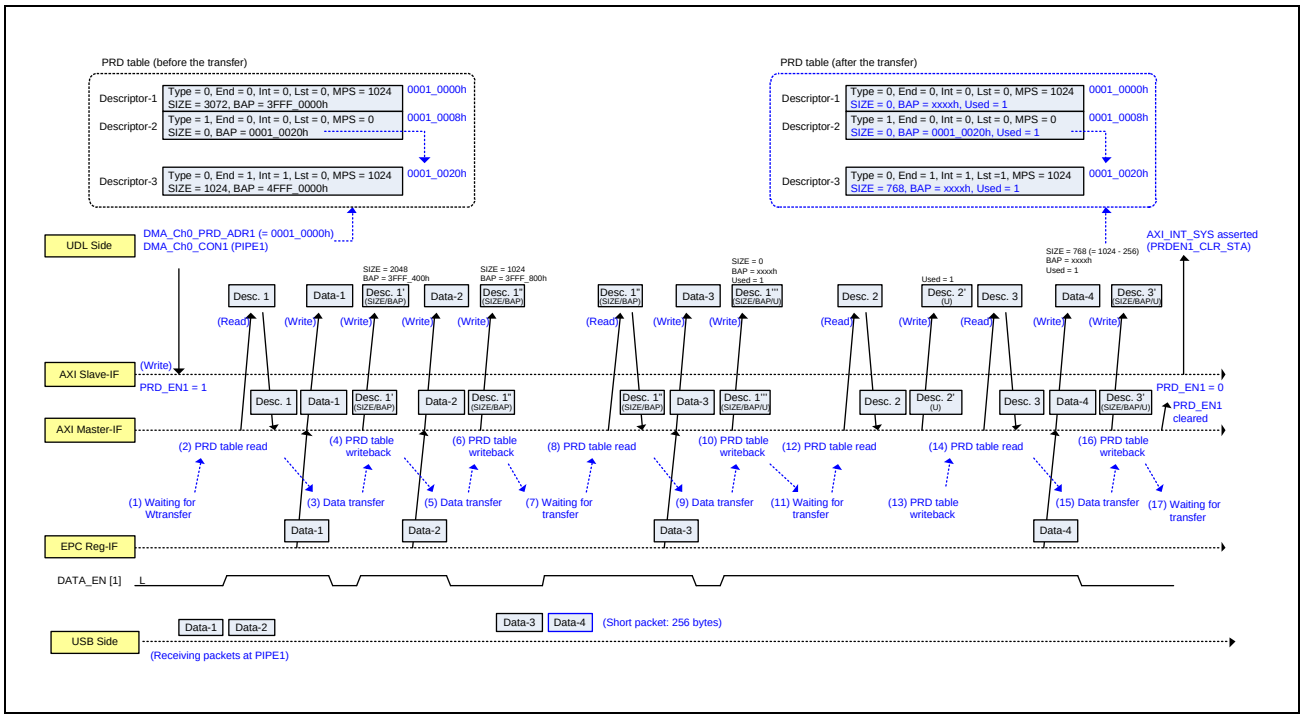


Figure 35.6-14 Example of OUT Transfer Terminated with Short Packet

(6) Finishing the Process for PRD Table and Its Conditions

AXI-IF has DMA_Ch0_CONx and DMA_Ch0_PRD_ADRx (x = 1-4) to have the information of PRD tables, and starts transfer when it detects EPC_D_Pn_DATAEN[n] (n = 1-15) at Data Interface is asserted from EPC. Asserting EPC_D_Pn_DATAEN[n] indicates that transfer on PIPE specified in one of register groups is enabled. Transfer is executed in a unit of a packet of USB (that is, the size is up to the max packet size of USB), following the order specified by PRD tables. When one of the conditions to finish the transfer is satisfied, AXI-IF recognizes that the process of the current PRD table has been completed, clears DMA_Ch0_CONx.PRD_ENx and sets the interrupt status in DMA_INT_STA register. AXI-IF finishes the transfer of PRD table when one of the conditions below is satisfied.

(1) All transfers related from the first PRD table to the last one (End bit is set) have been completed, or

(2) Transfer is terminated by receiving short packet in OUT transfer (AXI write transfer), or

(3) EPC_D_DBRTRANSEND which indicates the end of transfer is asserted in OUT transfer (AXI Write transfer), or

(4) PRD_Table is incorrect, or

(5) EPC requests ABORT during transfer on Data-IF.
(EPC never requests ABORT as far as the operation of the software is compliant to the flow in this manual.)

The following cases are the conditions of abnormal termination of transfer due to error. But they are avoidable by the configuration of system and assumed that they never occur in the normal usage. Make sure to configure the system so that those errors never occur.

(6) An error occurs in read process of PRD table, or

(7) An error response is received during data transfer on AXI, or

(8) An error occurs in writing-back of PRD Table.

In cases of (2) and (3) transfer is terminated in the middle of PRD tables. In these cases, used bit in the PRD table of the completed transfer is set. Besides, if the amount of transferred data is less than the size specified in PRD table, the size

field of the PRD table is changed to the remaining amount of data after the transfer has been terminated. The actual amount of transferred data can be calculated by subtracting the remaining amount of data from the size specified in PRD table initially.

The case of (5) occurs when clearing buffers of EPC is requested on Pn_CON.Pn_BCLR or P0_CON.P0_BCLR during transfer is being executed at Data interface. But since it is not recommended in this manual, the case of (5) is assumed to never occur as long as the software is compliant to the flow. When the case occurs, used bit and Data Error bit in the PRD table for which the transfer is being executed are set to 1 and AXI_INT_STA.PRDERR0_x_STA is asserted.

The cases of (6) and (8) mean that read or write specified by PRD Table could not be executed. In those cases, AXI_INT_STA.PRDERR0_x_STA is asserted.

For the case of (7), as far as (8) does not occur concurrently, used bit and Data Error bit in PRD table are set to 1 and AXI_INT_STA.PRDERR0_x_STA is asserted similarly to (5).

But in case (8) occurs at the same time, it means that writing-back of PRD table fails and the result of transfer is not stored in PRD table. AXI-IF terminates the transfer at Data Interface with EPC.

It is assumed in the design of USB3PERI that it would not receive an error response on AXI-bus. Make sure to configure the system not to return an error response on AXI bus to USB3PERI.

(7) Case of Error

There are two kinds of errors in USB3PERI. One is an error due to the mistake in the setting and the other is the transfer error caused by receiving an error response on AXI bus.

But USB3PERI was designed on the premise that it would not receive an error response (for both of read and write) on AXI bus when it executes DMA transfer, so USB3PERI only reports that the transfer error occurs for debug use. Make sure to configure system so that it does not return an error response on AXI bus to USB3PERI.

In case an error occurs at AXI-IF, AXI-IF automatically clears DMA_Ch0_CONx.PRD_ENx for the current PRD table so that the current transfer is terminated, and asserts AXI_INT_STA.PRDERR0_x_STA at the same time.

In case an error occurs at AXI-IF, the result of the current transfer is not guaranteed. Make sure not to use transferred data when the error occurs.

(8) Ordering of Transactions

USB3PERI operates AXI transactions in order. Hence USB3PERI always uses the same value “0h” as MAWID[3:0], MWID[3:0] and MARID[3:0].

(9) Write Transfer with All Zero Strobe

USB3PERI can execute two outstanding transactions and issues two outstanding addresses on AXI address channel checking the max packet size and the rest of buffer assigned by PRD table.

But, in OUT transfer (which requires the write transfer on AXI bus), the received packet might be the short one and its size might be less than both of the max packet size and the rest of buffer. In that case, USB3PERI might have no more data to be transferred although it has already issued the transfer address on AXI write address channel. For that case, USB3PERI executes the write transfer with all zero strobe on MWSTRB[7:0] so that no write occurs at target.

Figure 35.6-15 shows the case that USB3PERI receives the short packet and it has data to transferred for ADR1 but does not for ADR2. Then, USB3PERI executes the write transfer with all zero strobe on MWSTRB[7:0] for ADR2.

In **Figure 35.6-15** the write transfer with all zero strobe starts from the head of the transfer, but MWSTRB[7:0] might be set to all zero in the middle of transfer depending on the size of the received packet.

Therefore USB3PERI requires the target on AXI bus to accept the write transfer with all zero strobe and discard the write data for the transfer.

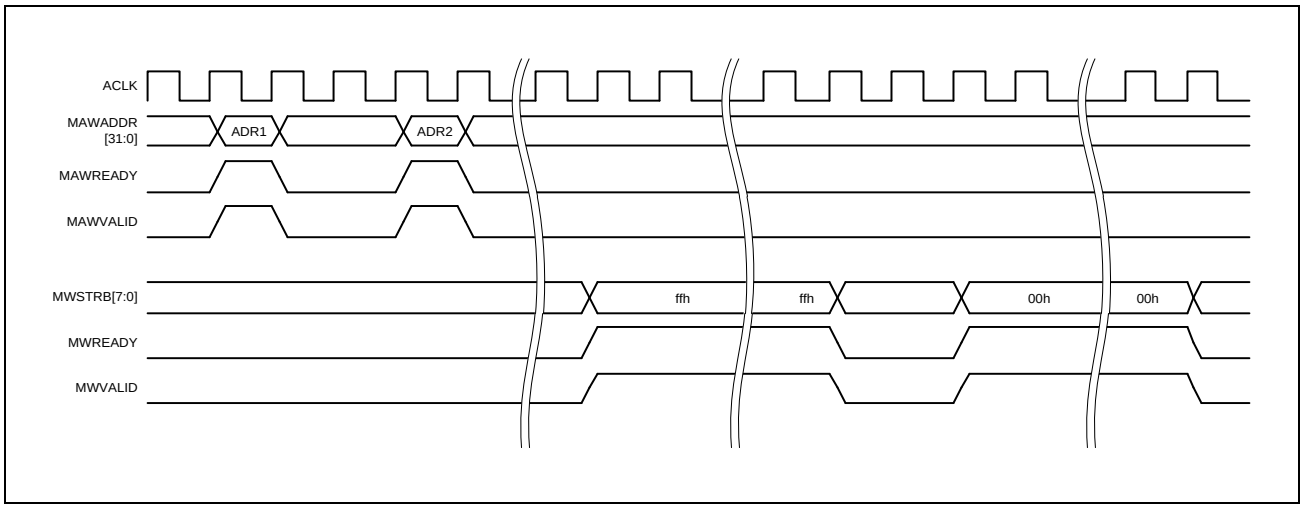


Figure 35.6-15 Write Transfer with All Zero Strobe

(10) Interrupts

Pn_DMACNG_STA(n = 1-15) in DMA_INT_STA is asserted in the cases below.

1. PRD_ENx in DMA_Ch0_CONx(x = 1-4) assigned for PIPE n is cleared due to the completion of transfer (completion of transfer means that Lst bit in PRD table is set and data assigned to it has been transferred, the short packet has been received for OUT PIPE, PP bit is cleared in received USB3.1 data packet with non ZLP mode or that an error has occurred in transfer).
2. PIPE which is not assigned to DMA_Ch0_CONx becomes ready (It can accept the next packet for IN transfer, or it has new received packet for OUT transfer).
3. Transfer of descriptor in which Int bit is set is completed.

Especially Pn_DMACNG_STA is asserted in case 2 as follows.

When PIPE n is IN pipe and DMA_Ch0_CON1 (for example) is assigned for the DMA transfer with it, Pn_DMACNG_STA is asserted at the completion of DMA transfer. If multiple pipes are enabled, DMA_Ch0_CON1 is assigned to another PIPE (PIPE m in this example) as soon as DMA transfer with PIPE n is completed. But the transmission of packets has not been completed at PIPEn. Pn_DMACNG_STA is asserted again when no DMA_Ch0_CONx is assigned to PIPE n and it has transmitted the last packet.

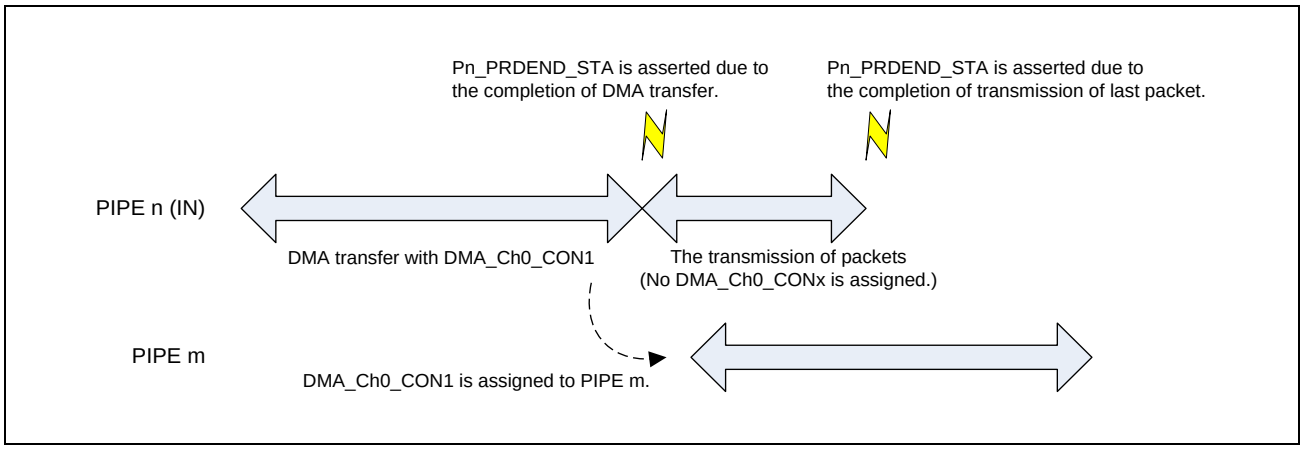


Figure 35.6-16 The Behavior of Pn_DMACNG_STA in IN Transfer

When PIPE n is OUT pipe but no DMA_Ch0_CONx is assigned to it, Pn_DMACNG_STA is asserted every time PIPEn receives a packet.

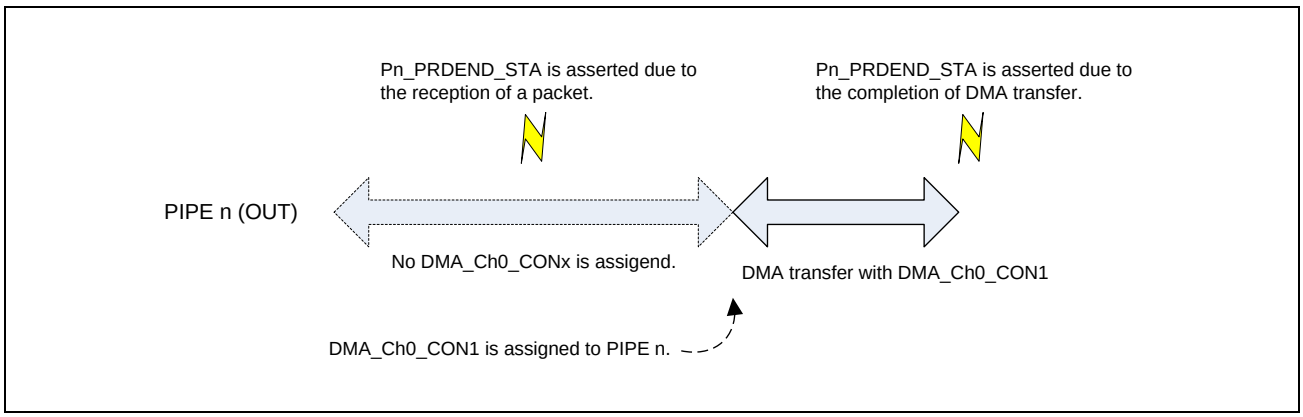


Figure 35.6-17 The Behavior of Pn_DMACNG_STA in OUT Transfer

Note that Pn_DMACNG_STA is not asserted if DMA_Ch0_CONx is assigned when the last IN packet has been transmitted or when the OUT packet has been received.

As noted above, Pn_DMACNG_STA might be asserted due to the causes except for DMA transfer. When it is required to know only the completion of DMA transfer, see PRD_ENx_CLR_STA in AXI_INT_STA instead.

35.6.4.5 List of Interrupt Factors

The interrupt factors for USB3PERI/EPC are shown below.

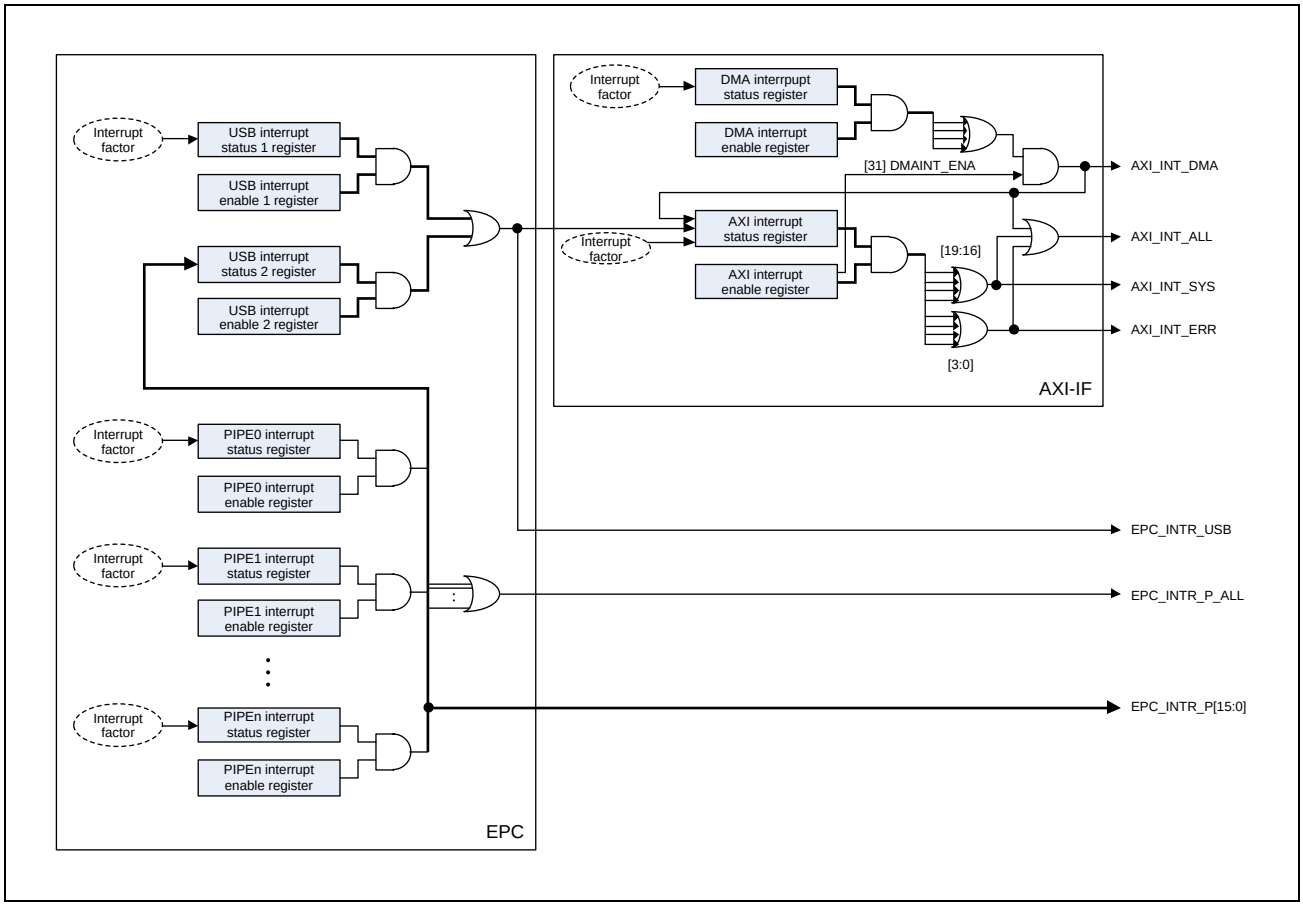


Figure 35.6-18 The System Diagram for the Interrupt

Table 35.6-68 Interrupt Factors at AXI-IF: AXI_INT_STA Register

Interrupt Factors	Descriptions
DMAINT_STA	This factor shows the status of the interrupt by DMA transfer.
EPCINT_STA	This factor shows the status of the interrupt of EPC_INTR_USB.
PRDEN4_CLR_STA	This factor indicates that DMA_CH0_CON4.PRD_EN4 has been cleared by hardware.
PRDEN3_CLR_STA	This factor indicates that DMA_CH0_CON3.PRD_EN3 has been cleared by hardware.
PRDEN2_CLR_STA	This factor indicates that DMA_CH0_CON2.PRD_EN2 has been cleared by hardware.
PRDEN1_CLR_STA	This factor indicates that DMA_CH0_CON1.PRD_EN1 has been cleared by hardware.
PRDERR0_4_STA	This factor indicates that there was an error in PRD table assigned to DMA_CH0_CON4.
PRDERR0_3_STA	This factor indicates that there was an error in PRD table assigned to DMA_CH0_CON3.
PRDERR0_2_STA	This factor indicates that there was an error in PRD table assigned to DMA_CH0_CON2.
PRDERR0_1_STA	This factor indicates that there was an error in PRD table assigned to DMA_CH0_CON1.

Table 35.6-69 Interrupt Factors at AXI-IF: DMA_INT_STA Register

Interrupt Factors	Descriptions
P[15-1]_DMACNG_STA	This factor shows the status of the interrupt by DMA transfer for PIPE[15-1].

Table 35.6-70 Interrupt Factors at AXI-IF: USB_INT_STA_1 Register

Interrupt Factors	Descriptions
B3_PLLWKUP_STA	This factor indicates that PHY30_CLK125_IN was resumed due to PLL wakeup (USB30_CON.B3_PLLWAKE was set or the input signal B3_PLL_WAKEIN is asserted) or U3 Wakeup LFPS from host.
B3_LUPSUCS_STA	This factor indicates that the link of USB3.1 has been established (LTTSM enters U0 state from Polling state).
B3_POLLING_STA	This factor indicates that LTSSM has made the transition to Polling state.
B3_INACTV_STA	This factor indicates that LTSSM has made the transition to Inactive state.
B3_DISABLE_STA	This factor indicates that LTSSM has made the transition to Disabled state.
B3_VNDTST_STA	This factor indicates that Vendor Device Test LMP has been received.
B3_U2INACT_STA	This factor indicates that U2 Inactivity Timeout LMP has been received.
B3_SETLNK_STA	This factor indicates that Set Link Function LMP has been received.
B3_LNKCNG_STA	This factor indicates that LTSSM has made the transition as listed below. U0 -> U1 U0 -> U2 U0 -> U3 U3 -> Recovery -> U0 U2 -> Recovery -> U0 U1 -> Recovery -> U0
B3_WRMRST_STA	This factor indicates that warm reset has been received.
B3_HOTRST_STA	This factor indicates that hot reset has been received.
B3_PSFAIL_STA	This factor indicates that the transition of POWERDOWN mode on USB30_CON.POW_SEL[2:0] failed.
B3_PSSUCS_STA	This factor indicates that the transition of POWERDOWN mode on USB30_CON.POW_SEL[2:0] has been completed successfully.
B3_U12REQ_STA	This factor indicates that USB3PERI received LGO_U1/U2 or when U1/U2_TIMER in SSIF was expired.
B3_TPSUCS_STA	This factor indicates that TP (Device Notification) requested on USB30_CON.B3_TP_SEND has been successfully completed.
B2_LPMRCV_STA	This factor indicates that USB3PERI has received LPM request from USB2.0 host and has returned ACK to it.
B2_USBRST_STA	This factor indicates that USB2.0 bus reset has been received.
B2_L1SPND_STA	This factor indicates that L1 suspend request has been received from USB2.0 host.
B2_L1RSUM_STA	This factor indicates that PLL wakeup has been requested (USB20_CON.B2_SUSPEND = 0 or B2_PLL_WAKEIN = 1) or when the resume request from USB2.0 host has been received (USB_STA.B2_L1RSUM_OUT changes from 0 to 1) during L1 state (USB_STA.B2_L1_SPND_OUT = 1).
B2_SPND_STA	This factor indicates that the suspend request has been received from USB2.0 host and USB_STA.B2_SPND_OUT changes from 0 to 1.
B2_RSUM_STA	This factor indicates that PLL wakeup has been requested (USB20_CON.B2_SUSPEND = 0 or B2_PLL_WAKEIN=1) or when the resume request from USB2.0 host has been received (USB_STA.B2_RSUM_OUT changes from 0 to 1) during L2 state (USB_STA.B2_SPND_OUT = 1) or L3 state (USB20_CON.B2_CONNECT = 0).
SPEED_STA	This factor indicates that there was a change in the speed mode of USB.
VBUS_CNG_STA	This factor indicates that the level of the input signal “VBUS” was changed.

Table 35.6-71 Interrupt Factors at AXI-IF: USB_INT_STA_2 Register

Interrupt Factors	Descriptions
PIPE[15:0]_INT_STA	This factor indicates that an interrupt related to PIPE[15-0] ocurred.

Table 35.6-72 Interrupt Factors at AXI-IF: P0_INT_STA Register

Interrupt Factors	Descriptions
P0_STSED_STA	This factor indicates that status stage of control transfer has been completed successfully.
P0_STSST_STA	This factor indicates that status stage of control transfer has been started at PIPE0.
P0_SETUP_STA	This factor indicates that valid setup data has been received at PIPE0.
P0_RCVNL_STA	This factor indicates that null data has been received at PIPE0.
P0_ERDY_STA	This factor indicates that the condition to send ERDY was satisfied at PIPE0.
P0_FLOW_STA	This factor indicates that PIPE0 has entered flow control state.
P0_STALL_STA	This factor indicates that STALL has been sent at PIPE0.
P0_NRDY_STA	This factor indicates that NRDY or NAK has been sent at PIPE0.
P0_BFRDY_STA	In case the direction of transfer is IN (P0_MOD.P0_DIR = 1), the next data can be written to P0_WRITE register. In case the direction of transfer is OUT (P0_MOD.P0_DIR = 0), the next data can be read from P0_READ register.

Table 35.6-73 Interrupt Factors at AXI-IF: Pn_INT_STA Factors

Interrupt Factors	Descriptions
Pn_CBW_STA	This factor indicates that CBW has been received at PIPEn and is ready to be read from Pn_READ register.
Pn_STERR_STA	This factor indicates that Stream bulk protocol error has occurred at PIPEn.
Pn_STRMX_STA	This factor indicates that Stream ID in received packet was different from that in Pn_STREAM.Pn_STREAM_C.
Pn_NSTRM_STA	In case the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), this factor indicates that ACK_TP(NoStream) has been received at PIPEn. In case the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0), this factor indicates that DP(NoStream) has been received at PIPEn.
Pn_PRIME_STA	In case the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), this factor indicates that ACK_TP(PRIME) has been received at PIPEn. In case the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0), this factor indicates that DP(PRIME) has been received at PIPEn.
Pn_RCVNL_STA	This factor indicates that zero length packet has been received at PIPEn.
Pn_ERDY_STA	This factor indicates that the condition to send ERDY has been satisfied at PIPEn.
Pn_FLOW_STA	This factor indicates that PIPEn has entered flow control state.
Pn_LSTTR_STA	In case the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), this factor indicates that the last data of the transfer (short packet, packet for which Pn_LAST was set or packet for which EPC_D_DBWTRANSEND was asserted) has been sent at PIPEn. In case the direction of transfer is OUT(Pn_MOD.Pn_DIR = 0), this factor indicates that the last data of the transfer (short packet or packet with PP = 0) has been received at PIPEn.
Pn_STALL_STA	This factor indicates that STALL has been sent at PIPEn.
Pn_NRDY_STA	This factor indicates that NRDY or NAK has been sent at PIPEn.
Pn_BFRDY_STA	In case the direction of transfer is IN (Pn_MOD.Pn_DIR = 1), the next data can be written to Pn_WRITE register. In case the direction of transfer is OUT (Pn_MOD.Pn_DIR = 0), the next data can be read from Pn_READ register.

35.6.4.6 Zero Length Packet (ZLP)

(1) Definition of Zero Length Packet

Zero length packet (ZLP) is the data packet (DP) but it has no data word in it's data payload. ZLP is used to show the boundary of the transfer in some USB device classes, in case that the size of the last data packet equals to the max packet size of the PIPE.

Short packet, which length of data is less than the max packet size of the PIPE, is interpreted as the last packet of transfer in general. For example, it is defined that the size of packet except the last one in bulk transfer should be the max packet size of the PIPE. But it differs how to treat the case that the size of the last packet of transfer equals to the max packet size of the PIPE, depending on USB device class.

It is difficult to know whether the received packet which has the length same as the max packet size is the last one or not for the receiver (host or device). In some USB device classes, ZLP is sent next to show that there is the boundary of transfer. But in Bulk Only Transfer (BOT), ZLP is not used because CBW notifies the amount of transfer in advance. The device might transmit data less than the amount shown in CBW and the size of the last data packet might be the max packet size, but CSW is transferred next even in that case and CSW of 13 bytes is the short packet in bulk transfer. Therefore host can know that the packet just before CSW was the last data packet. In Stream bulk transfer, the packet with PP = 0 to show the end of transfer related the current Stream ID.

See the specification of USB device class to know whether ZLP is really required or not.

(2) Transfer of ZLP Support Mode in USB3PERI

USB3PERI has the mode to support ZLP transfer. Set USB_COM_CON.Pn_WDATAIF_NL, USB_COM_CON.Pn_RDATAIF_NL and USB_COM_CON.Pn_LSTTR_PP to 1 in order to use the mode.

(3) In the Configuration with AXI-IF

USB3PERI sends ZLP for OUT transfer and receives ZLP for IN transfer automatically with the settings for them. In order to transmit ZLP in ZLP transfer, the software sets ZL bit in PRD table where ZLP is requested to be transmitted in advance. When USB3PERI receives ZLP in OUT transfer, it sets ZL bit in PRD table where ZLP is received.

USB_COM_CON.Pn_WDATAIF_NL, USB_COM_CON.Pn_RDATAIF_NL and USB_COM_CON.Pn_LSTTR_PP should be set to 1 as noted in **Section 35.6.4.4(2), IN Transfer**.

For IN transfer, with PRD table in which Lst=1 and ZL=1, USB3PERI sends ZLP after the last data packet of the PRD table in order to show the boundary of transfer. With PRD table in which Lst = 0 or ZL = 0, USB3PERI never sends ZLP.

Therefore, set both of Lst bit and ZL bit to 1 in the PRD table which has the last data packet and requires ZLP after it. In other PRD tables, set both of Lst bit and ZL bit to 0.

Note that the meaning of 0000h in SIZE field of PRD table differs depending on ZL bit and Lst bit. If ZL = 1 and Lst = 1, 0000h in SIZE field means that 0 byte transfer is requested by the PRD table. Otherwise, 0000h means that 64 Kbytes transfer is requested.

If ZLP is required after 64 Kbytes data has been transferred, prepare two PRD tables. The first one has 64 Kbytes data (SIZE field is 0000h) with Lst = 0 and ZL = 0, and the second one has 0 bytes data (SIZE field is 0000h) with Lst=1 and ZL=1.

For OUT transfer , the software is never required to set Lst bit and ZL bit in PRD table. When USB3PERI receives ZLP in OUT transfer, it sets both of Lst bit and ZL bit to 1 in the PRD table. If USB3PERI has already received some packets before ZLP, USB3PERI transfers them to system memory where the PRD table designates, then it sets Lst bit and ZL bit in the PRD table.

If USB3PERI does not receive ZLP but short packet (which length is not 0), it sets Lst bit to 1 but leave ZL bit as 0.

Note that the meaning of 0000h in SIZE field of PRD table differs depending on ZL bit and Lst bit. If ZL=1 and Lst = 1, 0000h in SIZE field means that 0 byte data is contained in the buffer designated by the PRD table. Otherwise, 0000h means 64 Kbytes data is contained in the buffer.

If ZLP is received after 64-Kbyte data has been received, two PRD tables are used. The first one shows SIZE = 0000h, Lst=0 and ZL=0, and it means that 64-Kbyte data has been received but ZLP isn’t included. The second one shows SIZE = 0000h, Lst=1 and ZL=1, and it means that only ZLP has been received for the PRD table.

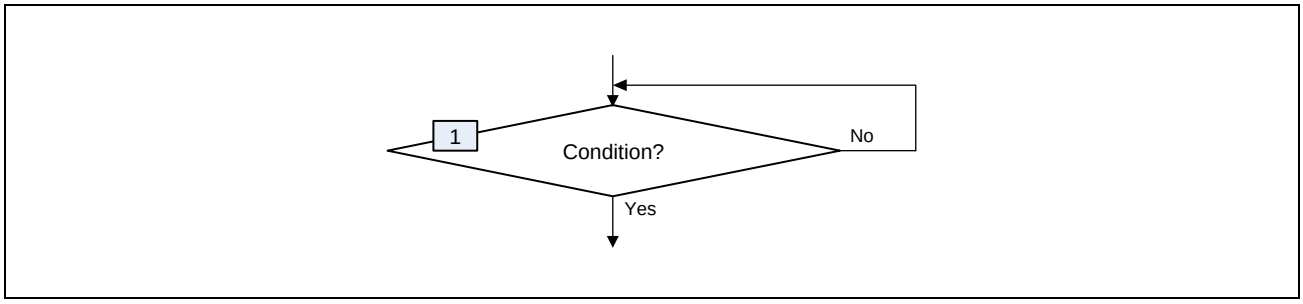
35.6.5 Examples of software flow

35.6.5.1 Outline of software flow

The software for USB3PERI is described in this section. The flow includes initialization, interrupt handling, control transfer process, bulk transfer process and interrupt transfer process.

Note that the flow described here is an example in general usage of USB3PERI. Modification of the flow or additional operation might be required depending on application in which user's system assumes.

The loop as below is used at some points in the flow and assumes the read polling of register by software. The interrupt notification might be used instead, but note that the setting to enable the interrupt is required in that case.



In order to access registers related to PIPEn, the index of PIPE should be set in PIPE_COM.PIPE_NUM[4:0] in advance. Note that the setting of the index of PIPE is omitted in each step of this section.

35.6.5.2 Initialization

The initialization should be completed before the device is used as USB device.

It is recommended that the initialization is done immediately after the power to device is turned on.

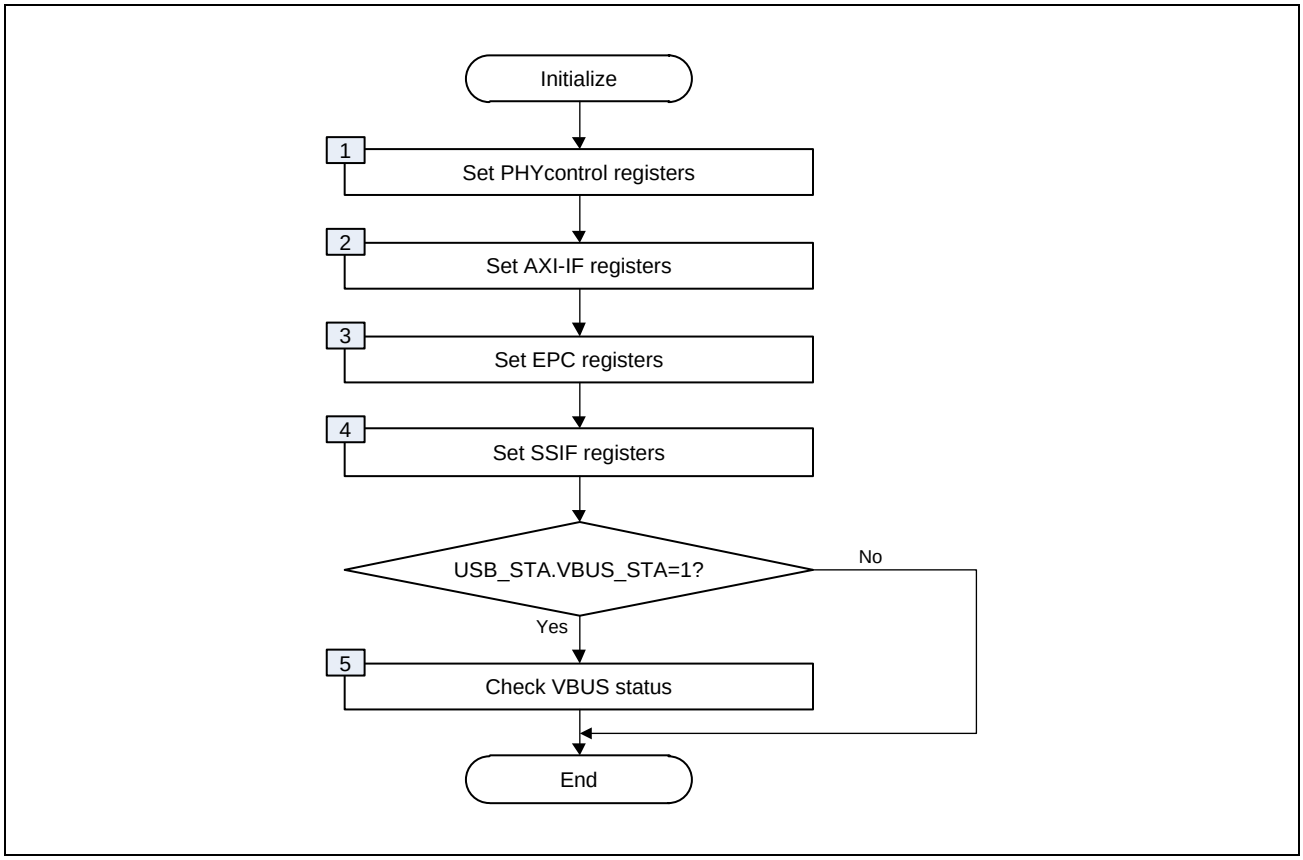


Figure 35.6-19 Initialization Flow

(1) Set PHY control registers
Set PHY control registers if required.
When the software accesses to PHY control register, set AXI_CON.PHY_CTRL before the access.

1. AXI_CON.PHY_CTRL = 1
2. Access to PHY control register
3. AXI_CON.PHY_CTRL = 0

(2) Set AXI-IF registers
The setting of AXI-Bridge is changed here if default values of the parameters for AXI-bus below are not consistent with the user's system.

- AXI_CON.MST_BSIZE[1:0] (Burst size setting: default value 8 bytes)
- AXI_CON.MST_ARPROT[2:0] (Read protection type: default value 010b)
- AXI_CON.MST_AWPROT[2:0] (Write protection type: default value 010b)

(3) Set EPC registers
Set the operation mode and initialize the interrupt status in EPC as follows.

a) USB30_CON register
If U3_POW_SEL[1:0] is required to be changed from default settings, change them here.

b) USB_INT_STA_1 register
Write 1 to all status bits in USB_INT_STA_1 in order to clear them.

c) USB_INT_ENA_1 register
Set VBUS_CNG_ENA to 1 in order to enable VBUS change interrupt.
It is also recommended to enable B3_HOTRST_ENA. See **Section 35.6.5.3(5), Hot Reset Process** for details.

(4) Set SSIF registers
The setting of SSIF is changed here if required. But it is recommended to use them with default settings basically.

(5) Check VBUS status
Check whether the status of USB_STA.VBUS_STA has already changed to 1 or not.
If USB_STA.VBUS_STA = 1, proceed to the operation of connection. See **Section 35.6.5.3(2), USB Connection**.

35.6.5.3 Interrupt Process

When an interrupt is asserted, see the interrupt status register to know what factor causes the interrupt, and then do the operation required.

Examples of the flow for interrupt are shown in this section.

(1) Interrupt Handler Process

The process in interrupt handler when an interrupt is asserted is described here.

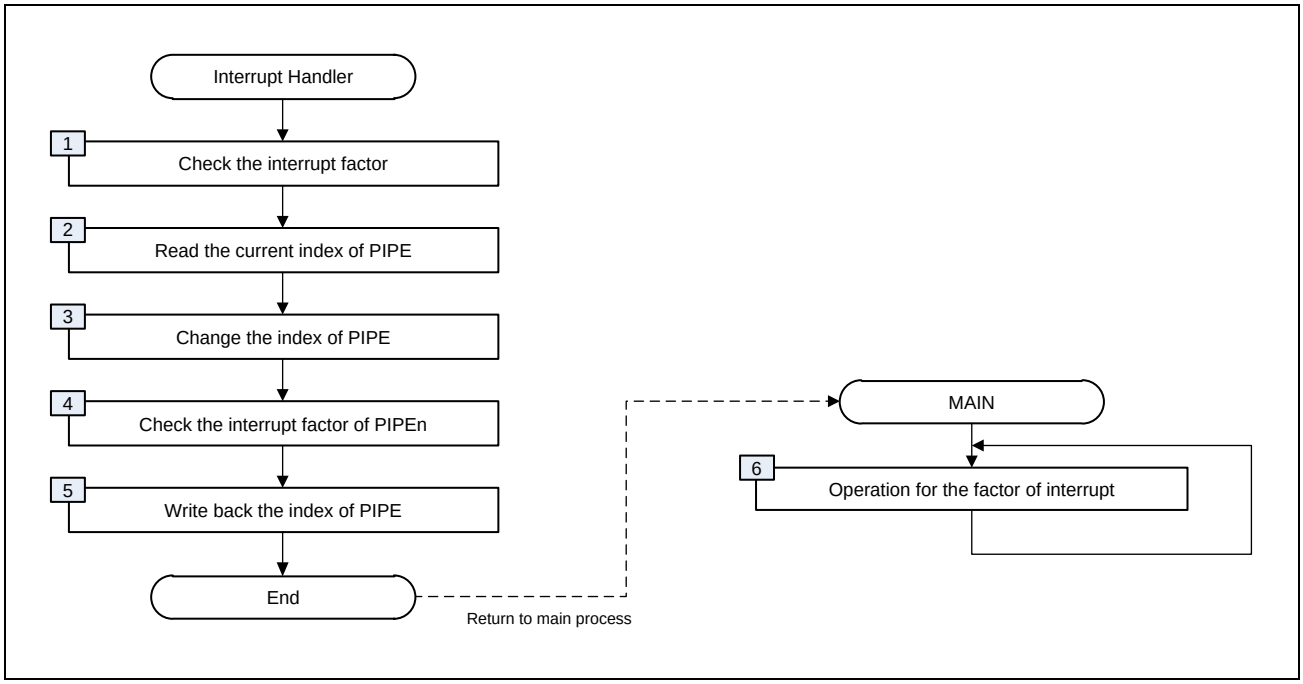


Figure 35.6-20 Interrupt Handler Process Flow

(1) Check the interrupt factor
See interrupt status register to know what factor is the cause of the interrupt. Then clear the status bit in interrupt status register.
It is assumed here that the interrupt is asserted due to PIPEn event, so registers related to PIPEn are accessed later.
If it is required to remember the interrupt factor in main process, prepare the variable to remember it.

(2) Read the current index of PIPE
The software should read the current index of PIPE and remember it before it changes the index of PIPE in PIPE_COM.PIPE_NUM[4:0] due to the interrupt asserted by PIPEn event and the succeeding operation for PIPEn.
The saved index of PIPE is written back at (5) if required.

(3) Change the index of PIPE
Change the index of PIPE in PIPE_COM.PIPE_NUM[4:0] to that of PIPE which generates the interrupt.

- PIPE_COM.PIPE_NUM[4:0] = the index of PIPE

(4) Check the interrupt factor of PIPEn
See the interrupt status register for PIPEn (Pn_INT_STA) to know what factor at PIPEn is the cause of the interrupt.
Note that Pn_INT_STA register shows the interrupt status of PIPE which is designated by the index of PIPE in PIPE_COM.PIPE_NUM[4:0].

Then clear the status bit in interrupt status register.
If it is required to remember the interrupt factor in main process, prepare the variable to remember it.

(5) Write back the index of PIPE
When the software exits the interrupt handler, write back the saved index of PIPE at (2) to PIPE_COM.PIPE_NUM[4:0] if required.

- PIPE_COM.PIPE_NUM[4:0] = the saved index of PIPE at (2)

(6) Operation for the factor of interrupt
The firmware does the operation required for the factor of interrupt after it returns to main process. In order to remember the factor, use the variable as noted at (1) and (4). After completing the operation, initialize the variable.

Especially note that it is prohibited to change the index of PIPE until read of the whole packet from P0_READ/Pn_READ or write of it to P0_WRITE/Pn_WRITE is completed.
If the interrupt due to PIPEn event is asserted (it can be known by USB_INT_STA_2 register) but read of the whole packet from P0_READ/Pn_READ or write of it to P0_WRITE/Pn_WRITE has been started, wait for the completion of read or write5 of the packet. Then change PIPE_COM.PIPE_NUM[4:0] to see the factor of interrupt at PIPEn.
See **Section 35.6.6.1, Prohibitions of Register Access** for details.

(2) USB Connection

The operation required for USB connection is described here.

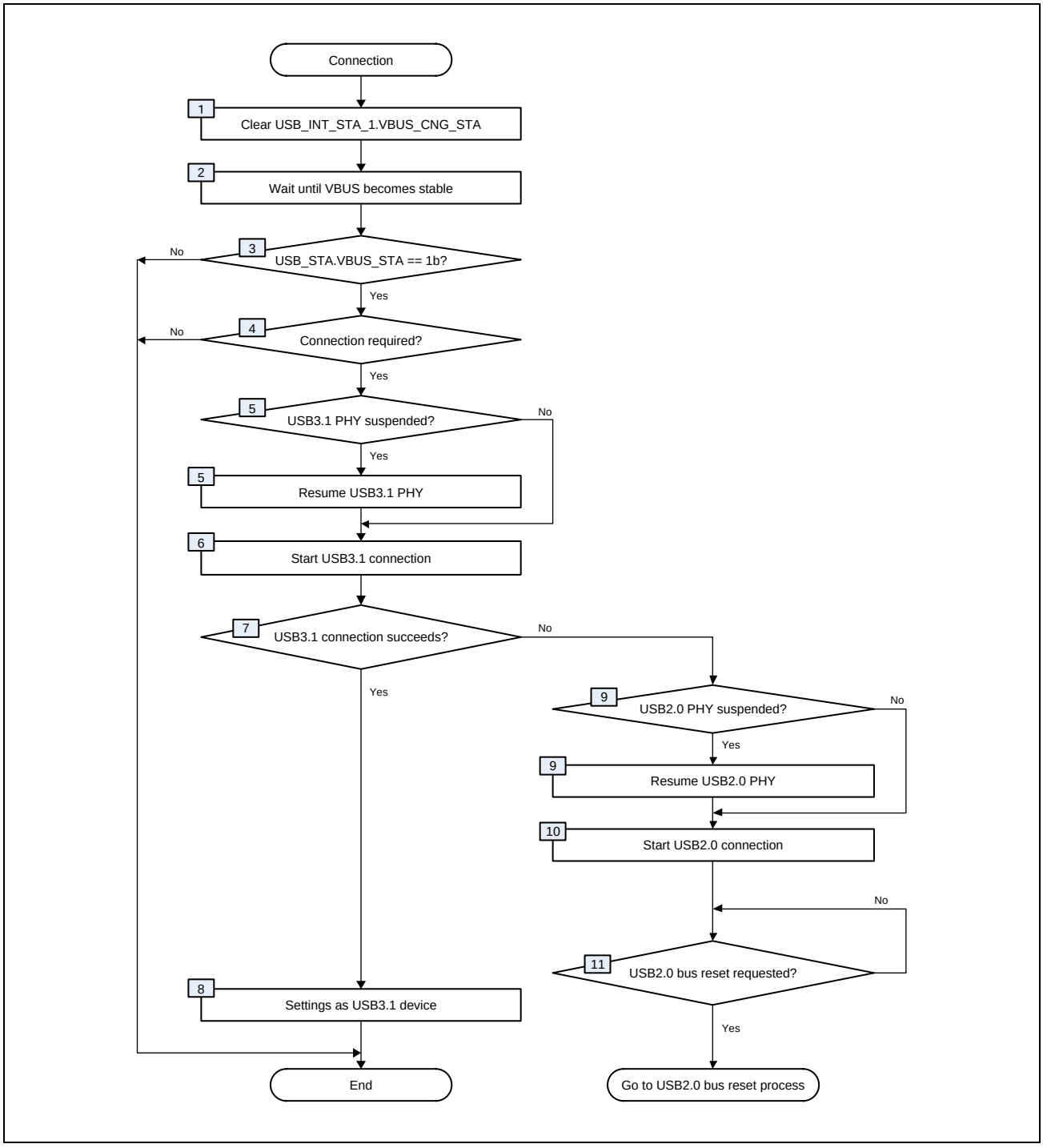


Figure 35.6-21 USB Connection Flow

(1) Clear USB_INT_STA_1.VBUS_CNG_STA
When VBUS status changes, USB_INT_STA_1.VBUS_CNG_STA is asserted. It is notified on an interrupt if enabled. If it is asserted, write 1 to USB_INT_STA_1.VBUS_CNG_STA to clear.

- USB_INT_STA_1.VBUS_CNG_STA = 1 (Clearing the event that the VBUS status is changed)

(2) Wait until VBUS becomes stable
In this subsection the device is assumed to be in disconnected state first. Therefore, it is required to check VBUS status in order to know if the device is really connected or not, because the change of VBUS status might be caused by noise.

To know VBUS status, USB_STA.VBUS_STA is available. If it shows 1, VBUS voltage level is valid and it means that the device is connected at present.
But VBUS voltage level is supposed to be unstable due to chattering just after the device is connected to host or hub. VBUS level will swing between 1 and 0 (therefore, USB_STA.VBUS_STA will also swing) for a while. During the chattering time, it is difficult to know the status of USB connection. Therefore, it is required to wait for VBUS to become stable. Wait for several dozens of milli-second in order to remove the influence of chattering of VBUS level.

If USB_INT_ENA_1.VBUS_CNG_ENA is enabled during the chattering time, there might be many interrupts caused by the swing of VBUS level. Disable USB_INT_ENA_1.VBUS_CNG_ENA to prevent that the software is annoyed at the swing of VBUS level for the chattering time.

- USB_INT_ENA_1.VBUS_CNG_ENA = 0 (The change of VBUS is masked)

(3) Is USB_STA.VBUS_STA = 1?
Check USB_STA.VBUS_STA to know whether the interrupt is caused by the change of VBUS level or merely noise. If USB_STA.VBUS_STA = 1, it means new USB connection. But if it shows 0, the interrupt detected at (1) would be caused by noise.

NOTE

If the device is frequently unconnected even when USB_STA.VBUS_STA = 1 is confirmed at this point, increase the wait time at (2). In that case, it might take more time to stabilize VBUS level.

(4) Is connection required?
If device requires to be connected, proceed to (5) to request the connection.
It is possible to insert the grace time here before the connection. The software can use the grace time for the preparation of the connection or other use.

(5) Resume USB3.1-PHY
If USB3.1-PHY is in the power down state and PLL is suspended, resume USB3.1-PHY so that it provides USB3.1 clock.
See **Section 35.6.5.8(6), USB3.1-PHY (PLL) Wakeup Process** for details.

(6) Start the operation for USB3.1 connection
Start the connecting operation as USB3.1 device when it is confirmed that device is connected to host.

- USB_COM_CON.EP0_EN = 1 (PIPE0 is enabled)
- USB_COM_CON.SPD_MODE = 0 (SS mode is requested)
- SSIFLINKSET3.SSIF_NUM_RDET[3:0]= 8h (The number of trial for Rx.Detect＝8)
- USB_COM_CON.RX_DETECTION = 1 (RxDetect is started)
- USB30_CON.B3_CONNECT = 1 (Starting the connection process for SS)

- USB_INT_ENA_1.B3_LUPSUCS_ENA = 1 (Interrupt due to the success of link up is enabled)
- USB_INT_ENA_1.B3_DISABLE_ENA = 1 (Interrupt due to the failure of link up is enabled)

Besides, if USB_INT_ENA_1.SPEED_ENA is enabled, the interrupt that SPEED state of USB is changed is asserted after LTSSM enters U0 as SS device or bus reset and chirp are completed as HS or FS device.

- USB_INT_ENA_1. SPEED_ENA = 1 (Interrupt of SPEED state is enabled)

(7) Does USB3.1 connection succeed?
As the result of the trial for USB3.1 connection, one of USB_INT_STA_1.B3_LUPSUCS_STA or USB_INT_STA_1.B3_DISABLE_STA is asserted. USB_INT_STA_1.B3_LUPSUCS_STA means that the link up process of LTSSM has been successfully done and LTSSM is in U0. USB_INT_STA_1.B3_DISABLE_STA means that the link up process of LTSSM has failed and LTSSM is in SS.Disabled. When they are asserted, an interrupt is generated if enabled.

- Check USB_INT_STA_1.B3_LUPSUCS_STA = 1 or USB_INT_STA_1.B3_DISABLE_STA = 1

After the confirmation above, write 1 to USB_INT_STA_1.B3_LUPSUCS_STA or USB_INT_STA_1.B3_DISABLE_STA to clear them.

- Write 1 to USB_INT_STA_1.B3_LUPSUCS_STA if asserted (Clearing the event that the link up has succeeded)
- Write 1 to USB_INT_STA_1.B3_DISABLE_STA if asserted (Clearing the event that USB3.1 connection has failed)

If USB_INT_STA_1.B3_LUPSUCS_STA is asserted, it means USB3.1 connection is successful, proceed to (8).
If USB_INT_STA_1.B3_DISABLE_STA is asserted, it means USB3.1 connection has failed, proceed to (9).

(8) Transition to default state
After the connecting operation has been successfully completed, enable the detection of control transfer at PIPE0 (endpoint 0). At the same time, the interrupts required for the operation mode should be enabled. An example for those cases are shown below. If there are other interrupts required for the usage of core, enable them as well.

- USB_INT_ENA_2.PIPE0_INT_ENA = 1 (Interrupt at PIPE0 is enabled)
- All bits in P0_INT_ENA register should be enabled (All interrupt factors for PIPE0 are enabled)

If the interrupt due to the change of USB SPEED state is enabled at (6), the interrupt is asserted when USB3.1 or USB2.0 connection is established. See USB_STA.SPEED[1:0] to know which speed the device is acting as. Then set the bits below according to the speed state.

In this state, the device is acting as USB3.1 device.

- USB_INT_ENA_1.B3_HOTRST_ENA = 1 (Interrupt due to hot reset is enabled)
- USB_INT_ENA_1.B3_WRMRST_ENA = 1 (Interrupt due to warm reset is enabled)

And it is recommended to disable USB2.0 setting explicitly as below for good interoperability to USB3.0 Host.

- USB20_CON.B2_CONNECT = 0 (USB2.0 connection is disabled)
- USB20_CON.B2_PUE = 0 (Pull up of D+ is disabled)

(9) Resume USB2.0-PHY
If USB2.0-PHY is in the power down state and PLL is suspended, resume USB2.0-PHY so that it provides USB2.0 clock.
See **Section 35.6.5.8(10), USB2.0 PHY (PLL) Wakeup Process** for details.

(10) Start USB2.0 connection

Start the connecting operation as USB2.0 device. Note that USB30_CON.B3_CONNECT is still 1. USB3.1 connection might be tried again after USB2.0 bus reset.

- In case of USB_INT_STA_1.B3_POLLING_STA =1 (it indicates connecting with USB3.1 Host), DisabledCount++, and write 1 to USB_INT_STA_1.B3_POLLING_STA.

For interoperability, it is recommended to include “B3_POLLING_STA =1” in the condition to increment DisabledCount.
About DisabledCount, see **Section 35.6.5.3(6), USB2.0 Bus Reset Process** for details.

- USB_COM_CON.EP0_EN = 1 (PIPE0 is enabled: this field is already enabled at (6))
- USB_COM_CON_SPD_MODE = 1 (USB2.0 mode is requested)
- USB20_CON.B2_PUE = 1 (Pull up on D+ is enabled)
- USB20_CON.B2_CONNECT = 1 (Starting the connection process for USB2.0)

(11) Is USB2.0 bus reset requested?

When USB2.0 bus reset comes, go to USB2.0 bus reset process. See **Section 35.6.5.3(6), USB2.0 Bus Reset Process** for details.

(3) USB Disconnection

The operation required for USB disconnection is described here.

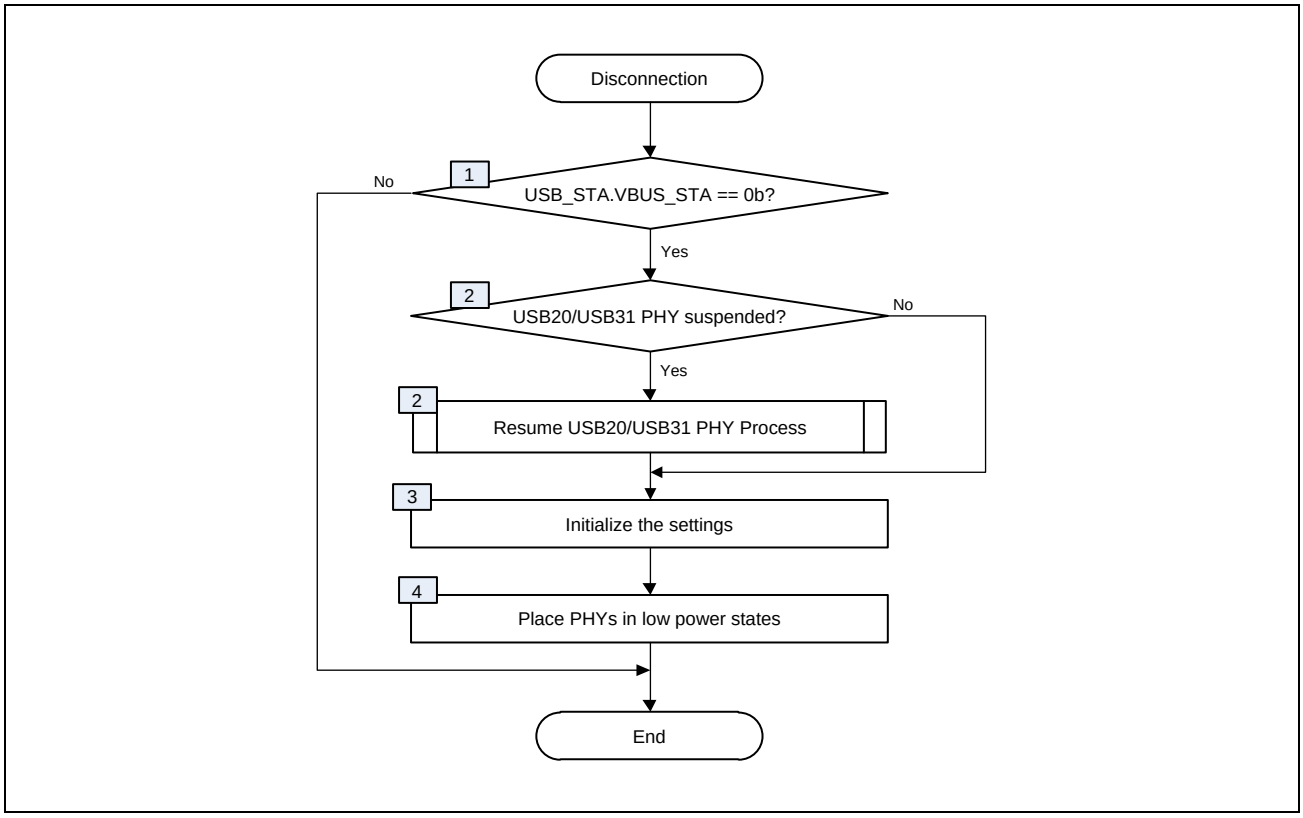


Figure 35.6-22 USB Disconnection Flow

(1) Is USB_STA.VBUS_STA = 0?
If USB_STA.VBUS_STA = 0b (it notifies on USB_INT_STA_1.VBUS_CNG_STA for example), the device is disconnected.

(2) Resume USB20/USB31-PHYs Process
If USB2.0-PHY is in the power down state and PLL is suspended, resume USB2.0-PHY so that it provides USB2.0 clock.
See **Section 35.6.5.8(10), USB2.0 PHY (PLL) Wakeup Process** for details.
If USB3.1-PHY is in the power down state and PLL is suspended, resume USB3.1-PHY so that it provides USB3.1 clock.
See **Section 35.6.5.8(6), USB3.1-PHY (PLL) Wakeup Process** for details.

(3) Initialize the settings
If the device is disconnected, initialize the settings below.

- USB20_CON.B2_PUE = 0 (D+ pull up is disabled)
- USB20_CON.B2_CONNECT = 0 (the request of connection as HS or FS device is disabled)
- USB30_CON.B3_CONNECT = 0 (the request of connection as SS device is disabled)
- USB_COM_CON.CONF = 0 (the device is in unconfigured state)

PIPEs should be initialized as well.

- USB_COM_CON.PIPE_CLR = 1 (PIPE is initialized)
  * Make sure that USB_COM_CON.PIPE_CLR returns to 0 after setting USB_COM_CON.PIPE_CLR = 1.

(4) Place PHYs in low power states

It is recommended to place USB3.1-PHY and USB2.0-PHY in low power state and PLLs in them are suspended in order to reduce the power consumption.

If USB3.1-PHY(PLL) is stopped, refer to **Section 35.6.5.8(1), Suspend in USB3.1 (Transition of State from U0 to U3)** (3),(4),(5). In this case, “U3 state” should be replaced with “disconnected state (SS.Disabled)“. Note that the values of USB30_CON.POW_SEL[2:0] are different in U3 and disconnected state. See **Section 35.6.3.3(3), USB30 Control Register (USB_PERI_USB30_CON)** for details.

If USB2.0-PHY(PLL) is stopped, refer to **Section 35.6.5.8(7), Suspend in USB2.0** (2).

(4) Warm Reset Process

The operation required when warm reset is detected is described here.

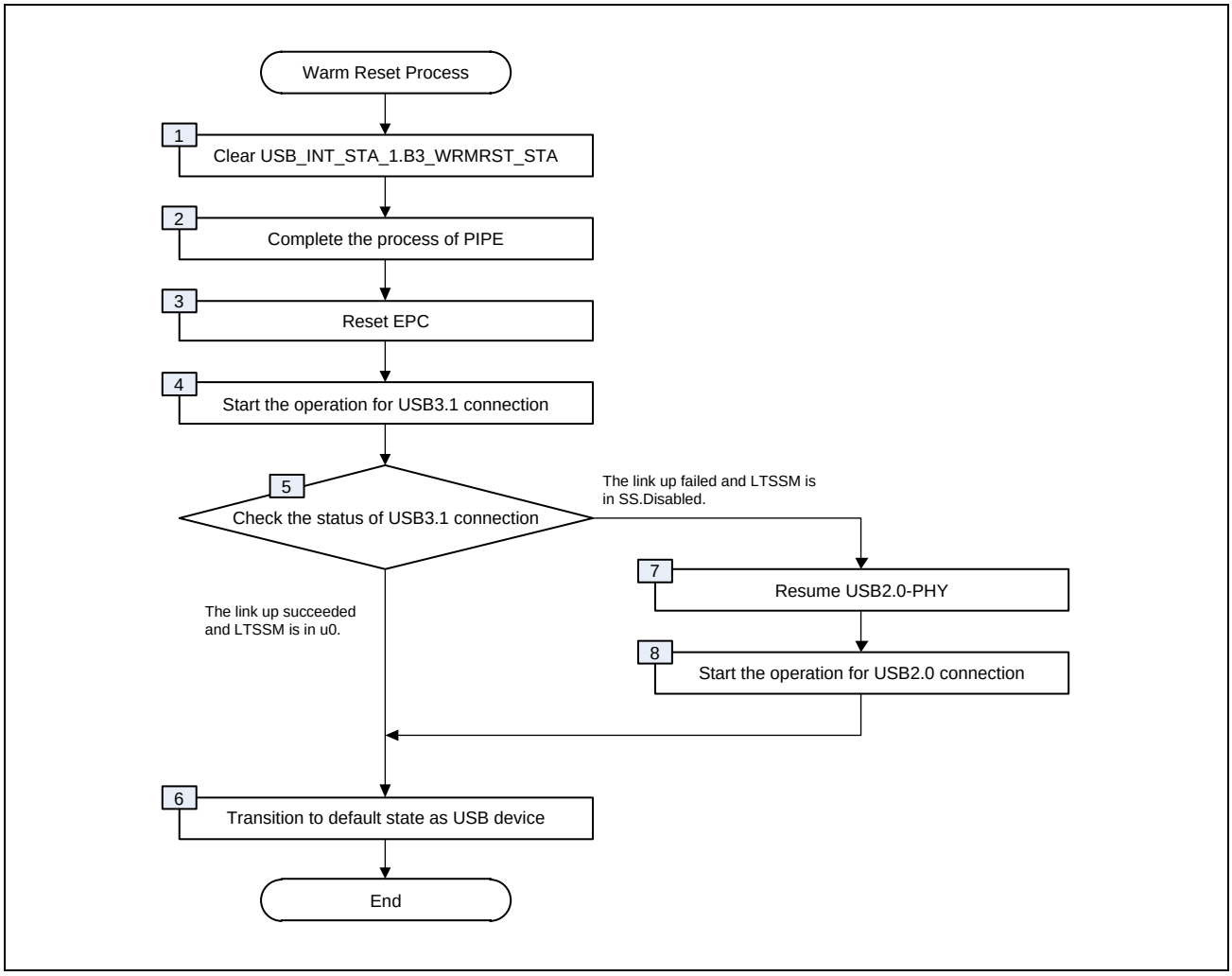


Figure 35.6-23 Warm Reset Process Flow

(1) Clear USB_INT_STA_1.B3_WRMRST_STA

When an interrupt is asserted and USB_INT_STA_1.B3_WRMRST_STA is set to 1, it means that USB3PERI receives warm reset. Write 1 to USB_INT_STA_1.B3_WRMRST_STA in order to clear it.

- Interrupt due to USB_INT_STA_1.B3_WRMRST_STA is generated
- Check that USB_INT_STA_1.B3_WRMRST_STA = 1
- USB_INT_STA_1.B3_WRMRST_STA = 1 (Clearing the event that warm reset is asserted)

(2) Complete the process of PIPE

Basically, as warm reset is requested when the device is just connected or when host and the device cannot communicate, it is unlikely that the device is executing data transfer when warm reset comes.
But if it is doing, stop the process of data transfer if it is being executed.
AXI_COM.MST_WAIT0 can be used to suspend the transfer.

- AXI_CON.MST_WAIT0 = 1 (DMA transfer at AXI-IF is requested to be suspended)

See AXI_STA.DMA_TRANS0 to know whether the transfer is really suspended or not. If the transfer is suspended, then clear DMA_Ch0_CONx.PRD_ENx to 0.

- DMA_Ch0_CONx.PRD_ENx = 0 (DMA transfer in AXI-IF is disabled)

(3) Reset EPC

Set the registers as follows in order to initialize EPC. In addition to the operations, clear all interrupt statuses.

- USB_COM_CON.CONF = 0
- USB_COM_CON.EP0_EN = 0
- USB_COM_CON.PIPE_CLR = 1 (PIPE is initialized)
  * Make sure that USB_COM_CON.PIPE_CLR returns to 0 after setting USB_COM_CON.PIPE_CLR = 1.
- Write 1 to all interrupt status bits in order to clear them.
- SSIFCMD.SSIF_UDIR[1:0] = 11b (The initiation of LGO_U1/LGO_U2 due to direct request is disabled.)
- SSIFCMD.SSIF_UREQ[1:0] = 11b (The initiation of LGO_U1/LGO_U2 due to timeout is disabled.)

(4) Start the operation for USB3.1 connection

Start the connecting operation as USB3.1 device.

- SSIFLINKSET3.SSIF_NUM_RDET[3:0] = 8h (The number of trial of Rx.Detect＝8)
- USB_COM_CON.EP0_EN = 1
- USB_COM_CON.SPD_MODE = 0
- USB30_CON.B3_CONNECT = 1 (Starting the connection process for USB3.1)
- USB_INT_ENA_1. SPEED_ENA = 1 (Interrupt of SPEED state is enabled)

If USB3.1 connection is established (the device works as USB3.1 device) before warm reset comes, the fields already has the values above. But SSIFLINKSET3.SSIF_NUM_RDET[3:0] might be changed. Set the field again to make sure.

(5) Check the status of USB3.1 connection

Check the status of connection process as USB3.1 device on the bits below.
If USB_INT_STA_1.B3_LUPSUCS_STA is asserted, USB3.1 connection is completed successfully. Clear the bit and proceed to (6).
If USB_INT_STA_1.B3_DISABLE_STA is asserted, the link up process as USB3.1 device has failed. Clear the bit and proceed to (7).

- Interrupt due to USB_INT_STA_1.B3_LUPSUCS_STA or USB_INT_STA_1.B3_DISABLE_STA is asserted
- Check whether USB_INT_STA_1.B3_LUPSUCS_STA = 1 or not (The link up succeeded or not)
- Check whether USB_INT_STA_1.B3_DISABLE_STA = 1 or not (The link up failed or not)
- Write 1 to the asserted bit to clear (Clearing the event that the link up succeeded or failed)

(6) Transition to default state as USB device

After the connecting operation has been successfully done, enable the detection of control transfer at PIPE0 (endpoint 0). At the same time, the interrupts required for the operation mode should be enabled. Examples for those cases are shown below. If there are other interrupts required for the usage of core, enable them as well.

- USB_INT_ENA_2.PIPE0_INT_ENA = 1 (Interrupt at PIPE0 is enabled)
- All bits in P0_INT_ENA register should be enabled (All interrupt factors for PIPE0 are enabled)

If the interrupt due to the change of USB SPEED state is enabled at (3), the interrupt is asserted when USB3.1 or USB2.0 connection is established. See USB_STA.SPEED[1:0] to know which speed the device is acting as. Then set the bits according to SPEED state as follows.

[when acting as USB3.1 device]

- USB_INT_ENA_1.B3_HOTRST_ENA = 1 (Interrupt due to hot reset is enabled)
- USB_INT_ENA_1.B3_WRMRST_ENA = 1 (Interrupt due to warm reset is enabled)

And it is recommended to disable USB2.0 setting explicitly as below for good interoperability to USB3.0 Host.

- USB20_CON.B2_CONNECT = 0 (USB2.0 connection is disabled)
- USB20_CON.B2_PUE = 0 (Pull up of D+ is disabled)

[when acting as USB2.0 device]

- USB_INT_ENA_1.B2_SPND_ENA = 1 (Interrupt due to USB2.0 suspend is enabled)
- USB_INT_ENA_1.B2_L1SPND_ENA = 1 (Interrupt due to L1 suspend is enabled)
- USB_INT_ENA_1.B2_USBRST_ENA = 1 (Interrupt due to USB2.0 bus reset is enabled)

(7) Resume USB2.0-PHY
If USB20 PHY is in the power down state and PLL is suspended, resume PLL so that it provides USB2.0 clock.

(8) Start the operation for USB2.0 connection
Start the connecting operation as USB2.0 device when USB3.1 connection is failed at (6).

- USB_COM_CON.EP0_EN = 1
- USB_COM_CON.SPD_MODE = 1
- USB20_CON.B2_PUE = 1b (Pull up on D+ is enabled)
- USB20_CON.B2_CONNECT = 1 (Starting the connection process for USB2.0)

If device is acting as USB2.0 device and USB3.1- PHY is expected to be in low power state, set it in low power state here. But note that USB2.0 bus reset will come when the operation for USB2.0 connection is started and it is required to try USB3.1 connection again collaterally. It means that USB3.1-PHY cannot be placed in low power state before USB2.0 connection is established. Make sure that the device is acting as USB2.0 device and the sequence of USB2.0 bus reset has already been done before setting USB3.1-PHY in low power state.

(5) Hot Reset Process

The operation required when hot reset is detected is described here.

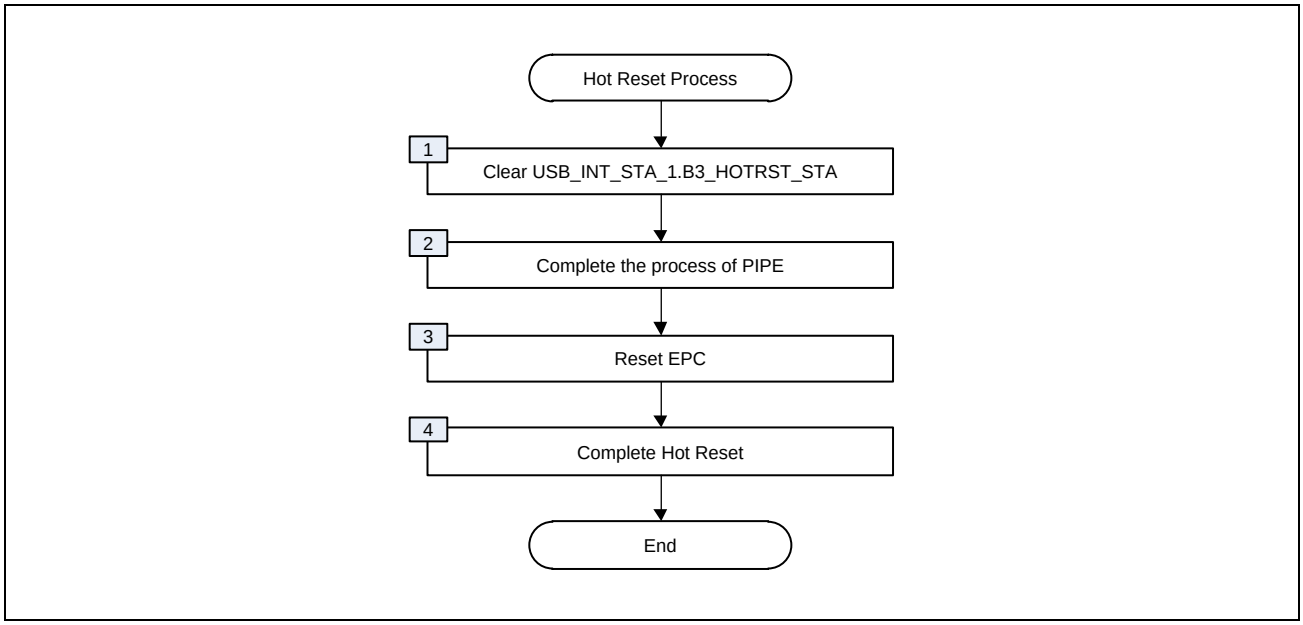


Figure 35.6-24 Hot Reset Process Flow

(1) Clear USB_INT_STA_1.B3_HOTRST_STA
When an interrupt is asserted and USB_INT_STA_1.B3_HOTRST_STA is set to 1, it means that USB3PERI receives hot reset. Write 1 to USB_INT_STA_1.B3_HOTRST_STA in order to clear it.

- Interrupt due to USB_INT_STA_1.B3_HOTRST_STA is generated
- Check that USB_INT_STA_1.B3_HOTRST_STA = 1
- USB_INT_STA_1.B3_HOTRST_STA = 1 (Clearing the event that hot reset is asserted)

(2) Complete the process of PIPE
Since hot reset comes during the training sequence, it is unlikely that the device is executing data transfer when hot reset comes.
But if it is doing, stop the process of data transfer if it is being executed.
AXI_COM.MST_WAIT0 can be used to suspend the transfer.

- AXI_CON.MST_WAIT0 = 1 (DMA transfer at AXI-IF is requested to be suspended)

See AXI_STA.DMA_TRANS0 to know whether the transfer is really suspended or not. If the transfer is suspended, then clear DMA_Ch0_CONx.PRD_ENx to 0.

- DMA_Ch0_CONx.PRD_ENx = 0 (DMA transfer in AXI-IF is disabled)

(3) Reset EPC
Set the registers as follows in order to initialize EPC. In addition to the operations, clear all interrupt statuses.

- USB_COM_CON.CONF = 0
- USB_COM_CON.EP0_EN = 0
- USB_COM_CON.PIPE_CLR = 1 (PIPE is initialized)
  * Make sure that USB_COM_CON.PIPE_CLR returns to 0 after setting USB_COM_CON.PIPE_CLR = 1.
- Write 1 to all interrupt status bits in order to clear them.

- SSIFCMD.SSIF_UDIR[1:0] = 11b (The initiation of LGO_U1/LGO_U2 due to direct request is disabled.)
- SSIFCMD.SSIF_UREQ[1:0] = 11b (The initiation of LGO_U1/LGO_U2 due to timeout is disabled.)

(4) Complete Hot Reset

Set the bit below to complete hot reset.

- USB_COM_CON.EP0_EN = 1
- USB30_CON.B3_HOTRST_CMP = 1

By setting USB30_CON.B3_HOTRST_CMP = 1, LTSSM state of USB3PERI transits from HotReset.Active to HotReset.Exit.
Setting B3_HOTRST_CMP = 1 allows the device to transit to HotReset.Exit from HotReset.Active. This process should be completed within 12 ms from detecting the start of HotReset at (1).

NOTE

The function of hot reset of device is tested in TD.7.28 of link layer test for compliane. The notations for the test are described here.

The downstream port can initiate a hot reset. When it transmits TS2 ordered sets with Reset bit asserted, the device shall respond by sending TS2 ordered sets with Reset bit asserted. When the device completes the operation for reset, it sends TS2 ordered set with Reset bit deasserted. The downstream port shall responds by sending TS2 ordered sets with Reset bit deasserted. Once both ports receive the TS2 ordered sets with Reset bit deasserted, it means the completion of hot reset and they shall exit from the hot reset state.

Note that USB3PERI automatically starts to transmit TS2 ordered sets with Reset bit asserted when it receives TS2 ordered sets with Reset bit asserted (tha is, hot reset requested from downstream port).

But it is required to set USB30_CON.B3_HOTRST_CMP in order to return TS2 ordered sets with Reset bit deasserted, if USB3PERI enters the state it returns TS2 ordered set with Reset bit asserted once. If there is any operation required for reset, it should be done before USB30_CON.B3_HOTRST_CMP is set. It is notified on USB_INT_STA_1.B3_HOTRST_STA that USB3PERI receives TS2 ordered sets with Reset bit asserted and starts to respond to them.

If the device does not return TS2 ordered sets with Reset bit asserted and hot reset isn’t completed with tHotResetActiveTimeout (= 12 ms), the device fails in the test of TD.7.28.

If the device including USB3PERI never deasserts Reset bit in TS2 ordered set, the software may not recognize that USB_INT_STA_1.B3_HOTRST_STA is asserted. In the test of TD.7.28, TS2 ordered sets with Reset bit asserted may come immediately after the device is connected to the downstream port. That case does not occur in normal operation. If the software masks interrupts except that due to the change of VBUS (USB_INT_STA_1.VBUS_CNG_STA) immediately after the device is connected, the software may not be able to know USB_INT_STA_1.B3_HOTRST_STA asserted. It is recommended to enable interrupts due to USB_INT_STA_1.VBUS_CNG_STA and USB_INT_STA_1.B3_HOTRST_STA just after the device is connected.

(6) USB2.0 Bus Reset Process

The operation required when USB2.0 bus reset is detected is described here.

There are two cases assumed as that USB2.0 bus reset comes.

- Device is just connected but fails in USB3.1 connection. USB2.0 connection is in progress.
- Device is working in HS or FS but host requests USB2.0 bus reset for some reason.
  This case also means device has failed in USB3.1 connection once.

That is, USB2.0 bus reset does not come when device works in SS, but it comes when device works in HS or FS.

USB2.0 bus reset means not only the reset as USB2.0 device but also the retry of USB3.1 connection for USB3.1 device. See **Section 35.6.4.2, USB3.1/USB2.0 connection** for the description of USB3.1 specification.

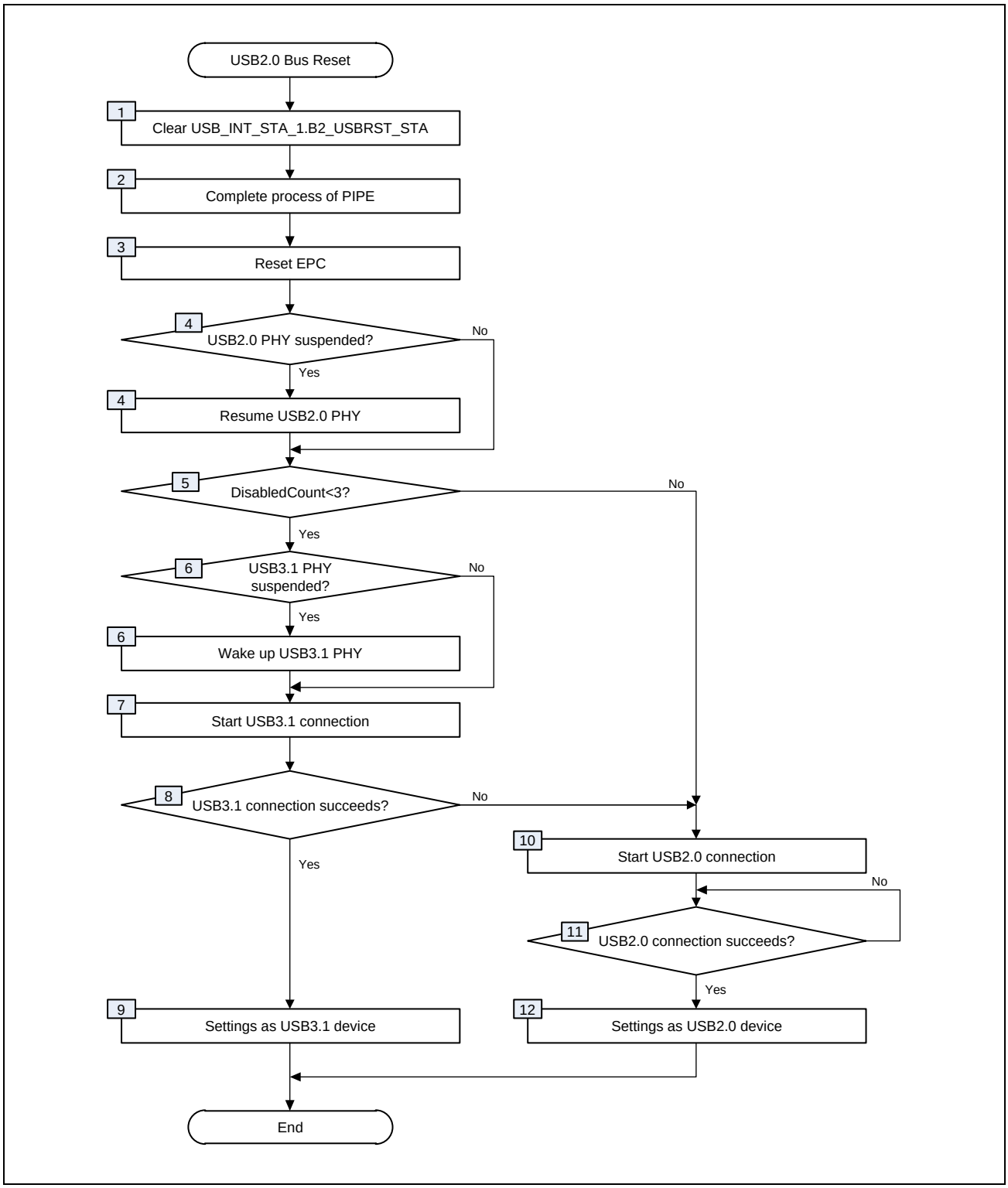


Figure 35.6-25 USB2.0 Bus Reset (switching from USB2.0 to USB3.1) Flow

The software is requierd to prepare the variable “DisabledCount”. The variable means the number of failrure in link up. The initial value of DisabledCount is 0 and it is initialized to 0 when one of the following conditions is satisfied.

- VBUS is disabled (No power is provided from VBUS).
- Port configuration exchange completes successfully.
- Power is removed.

Furthermore, being requested USB2.0 bus reset means that the device has already pulled up D+ (as HS or FS device) and has been detected by host. It is assuemed that the software has already set USB20_CON.B2_CONNECT = 1 when USB2.0 bus reset comes.

(1) Clear USB_INT_STA_1.B2_USBRST_STA
When an interrupt is asserted and USB_INT_STA_1.B2_USBRST_STA is set to 1, it means that USB3PERI receives USB2.0 bus reset. Write 1 to USB_INT_STA_1.B2_USBRST_STA in order to clear it.

(2) Complete the process of PIPE
Basically, as USB2.0 bus reset is requested when the device is just connected or when host and the device cannot communicate, it is unlikely that the device is executing data transfer when bus reset comes.
But if it is doing, stop the process of data transfer if it is being executed.
AXI_COM.MST_WAIT0 can be used to suspend the transfer.

- AXI_CON.MST_WAIT0 = 1 (DMA transfer at AXI-IF is requested to be suspended)

See AXI_STA.DMA_TRANS0 to know whether the transfer is really suspended or not. If the transfer is suspended, then clear DMA_Ch0_CONx.PRD_ENx to 0.

- DMA_Ch0_CONx.PRD_ENx = 0 (DMA transfer in AXI-IF is disabled)

(3) Reset EPC
Set the registers as follows in order to initialize EPC. In addition to the operations, clear all interrupt statuses.

- USB_COM_CON.CONF = 0
- USB_COM_CON.EP0_EN = 0
- USB_COM_CON.PIPE_CLR = 1 (PIPE is initialized)
  * Make sure that USB_COM_CON.PIPE_CLR returns to 0 after setting USB_COM_CON.PIPE_CLR = 1.
- USB20_CON.B2_TSTMOD[2:0] = 0h (if test mode is set)
- USB20_CON.B2_TSTMOD_EN = 0 (if test mode is set)
- Write 1 to all interrupt status bits in order to clear them.

(4) Resume USB2.0-PHY
It is assumed that the device works in HS or FS, but the device might be in suspended state and PLL in USB2.0-PHY might be stopped when USB2.0 bus reset comes.
In that case resume USB2.0-PHY so that it provides USB2.0 clock. USB3.1 connection might be requested depending on the value of DisabledCount, but the pull up of D+ for USB2.0 connection is still valid and USB2.0 connection is tried immediately when USB3.1 connection fails. That is, USB2.0-PHY clock is required regardless of the value of DisabledCount.

(5) Is DisabledCount < 3?
If DisabledCount < 3, it means the device state is in USDPORT.Powered on due to USB2.0 bus reset and the device requests USB3.1 connection. Proceed to (6).
If DisabledCount = 3, it means the device state is in USDPORT.Disabled_Error and the device does not request USB3.1 connection. Proceed to (10).

(6) Resume USB3.1-PHY
If USB3.1-PHY is in the power down state and PLL is suspended, resume USB3.1-PHY so that it provides USB3.1 clock.

(7) Start USB3.1 connection
As DisbledCount < 3, USB3.1 connection is tried again.
If USB2.0 bus reset is the first one just after the device is connected but fails in USB3.1 connection, most of the fields below has already been set at (6) in **Section 35.6.5.3(2), USB Connection**. In that case, the setting s for USB2.0 connection at (10) in **Section 35.6.5.3(2), USB Connection** should be still active as they are because USB2.0 connection might be required when USB3.1 connection fails.

- USB_COM_CON.EP0_EN = 1 (PIPE0 is enabled)
- USB_COM_CON.SPD_MODE = 0 (USB3.1 mode is requested)
- SSIFLINKSET3.SSIF_NUM_RDET[3:0] = 1h (The number of trial for Rx.Detect＝1)
- USB_COM_CON.RX_DETECTION = 1 (RxDetect is started)
- USB30_CON.B3_CONNECT = 1 (Starting the connection process for USB3.1)
- USB_INT_ENA_1.B3_LUPSUCS_ENA = 1 (Interrupt due to the success of link up is enabled)
- USB_INT_ENA_1.B3_DISABLE_ENA = 1 (Interrupt due to the failure of link up is enabled)
- USB_INT_ENA_1. SPEED_ENA = 1 (Interrupt of SPEED state is enabled)

The difference with (6) in **Section 35.6.5.3(2), USB Connection** is that the SSIFLINKSET3.SSIF_NUM_RDET[3:0] = 1h although it is set to 8h at (6) in **Section 35.6.5.3(2), USB Connection**. It means that the device can do only one trial of Rx detection.

(8) Does USB3.1 connection succeed?
As the result of the trial for USB3.1 connection, one of USB_INT_STA_1.B3_LUPSUCS_STA or USB_INT_STA_1.B3_DISABLE_STA is asserted. USB_INT_STA_1.B3_LUPSUCS_STA means that the link up process of LTSSM has been successfully done and LTSSM is in U0. USB_INT_STA_1.B3_DISABLE_STA means that the link up process of LTSSM has failed and LTSSM is in SS.Disabled. When they are asserted, an interrupt is generated if enabled.

- Check USB_INT_STA_1.B3_LUPSUCS_STA = 1 or USB_INT_STA_1.B3_DISABLE_STA = 1

After the confirmation above, write 1 to USB_INT_STA_1.B3_LUPSUCS_STA or USB_INT_STA_1.B3_DISABLE_STA to clear them.

- Write 1 to USB_INT_STA_1.B3_LUPSUCS_STA if asserted (Clearing the event that the link up has succeeded)
- Write 1 to USB_INT_STA_1.B3_DISABLE_STA if asserted (Clearing the event that USB3.1 connection has failed)

If USB_INT_STA_1.B3_LUPSUCS_STA is asserted, it means USB3.1 connection is successful, proceed to (9).
If USB_INT_STA_1.B3_DISABLE_STA is asserted, it means USB3.1 connection has failed, proceed to (10).

(9) Settings as USB3.1 device
After the connecting operation as SS device has been successfully completed, disable USB2.0 connection. It is defined in USB3.1 specification that USB2.0 connection should be disabled within tUSB2SwitchDisconnect (= 1ms) after Far End Receiver Termination is detected and LTSSM enters Polling.

- USB20_CON.B2_CONNECT = 0 (USB2.0 connection is disabled)
- USB20_CON.B2_PUE = 0 (Pull up of D+ is disabled)

Then enable the detection of control transfer at PIPE0 (endpoint 0). At the same time, the interrupts required for the operation mode should be enabled. An example for that cases are shown below. If there is another interrupt required for the usage of core, enable it as well.

- USB_INT_ENA_2.PIPE0_INT_ENA = 1 (Interrupt at PIPE0 is enabled)
- All bits in P0_INT_ENA register should be enabled (All interrupt factors for PIPE0 are enabled)

As the device is working as SS device, interrupts due to hot reset or warm reset shall be enabled.

- USB_INT_ENA_1.B3_HOTRST_ENA = 1 (Interrupt due to hot reset is enabled)
- USB_INT_ENA_1.B3_WRMRST_ENA = 1 (Interrupt due to warm reset is enabled)

When the port configuration is completed, DisabledCount is reset to 0.

If USB2.0 clock is not needed, USB2.0-PHY can be suspended. See **Section 35.6.5.8(7), Suspend in USB2.0** for details.

(10) Start USB2.0 connection

Since USB3.1 connection has failed, disable USB3.1 connection.

- USB30_CON.B3_CONNECT = 0
- In case of USB_INT_STA_1.B3_POLLING_STA= 1 (it indicates connecting with USB3.1 Host), DisabledCount++, and write 1 to USB_INT_STA_1.B3_POLLING_STA.

For interoperability, it is recommended to include “B3_POLLING_STA= 1” in the condition to increment DisabledCount.

Then, start USB2.0 connection.
The most of the fields below has already set, but USB_COM_CON.SPD_MODE is set for USB3.1 connection at (7), so it should be changed for USB2.0 connection.

- USB_COM_CON.EP0_EN = 1 (PIPE0 is enabled: this field is already enabled at (6))
- USB_COM_CON.SPD_MODE = 1 (USB2.0 mode is requested)
- USB20_CON.B2_PUE = 1 (Pull up on D+ is enabled)
- USB20_CON.B2_CONNECT = 1 (Starting the connection process for USB3.1)
- USB_INT_ENA_1. SPEED_ENA = 1 (Interrupt of SPEED state is enabled)

(11) Does USB2.0 connection succeed?

After USB2.0 bus reset and chirp, the device works as HS or FS device. For USB2.0 connection, there is no link training as that in USB3.1 connection, so it is assumed to be always completed successfully.

(12) Setting as USB2.0 device

After the connecting operation as HS or FS has been successfully done, enable the detection of control transfer at PIPE0 (endpoint 0). At the same time, the interrupts required for the operation mode should be enabled. Examples for those cases are shown below. If there are other interrupts required for the usage of core, enable them as well.

- USB_INT_ENA_2.PIPE0_INT_ENA = 1 (Interrupt at PIPE0 is enabled)
- All bits in P0_INT_ENA register should be enabled (All interrupt factors for PIPE0 are enabled)

If the interrupt due to the change of USB SPEED state is enabled at (10), the interrupt is asserted when USB2.0 connection is established. See USB_STA.SPEED[1:0] to know which speed the device is acting as. Then set the bits according to SPEED state as follows.

[when acting as USB2.0 device]

- USB_INT_ENA_1.B2_SPND_ENA = 1 (Interrupt due to USB2.0 suspend is enabled)

- USB_INT_ENA_1.B2_L1SPND_ENA = 1 (Interrupt due to L1 suspend is enabled)
- USB_INT_ENA_1.B2_USBRST_ENA = 1 (Interrupt due to USB2.0 bus reset is enabled)

35.6.5.4 Control Transfer

The operation for control transfer is described here.

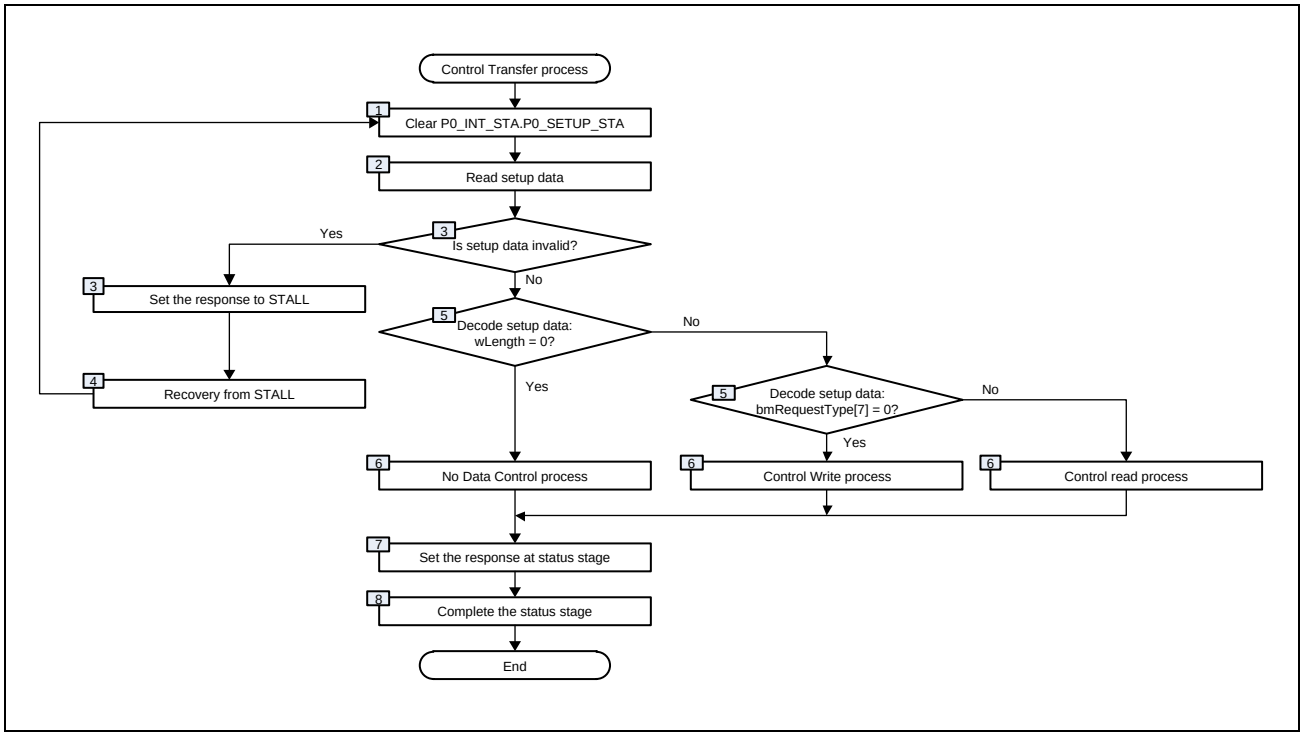


Figure 35.6-26 Control Transfer Process Flow

(1) Clear P0_INT_STA.P0_SETUP_STA

When an interrupt is asserted and P0_INT_STA.P0_SETUP_STA is set to 1, it means that USB3PERI has received setup data. Write 1 to P0_INT_STA.P0_SETUP_STA in order to clear it.

- Interrupt due to P0_INT_STA.P0_SETUP_STA is generated
- Check that P0_INT_STA.P0_SETUP_STA = 1
- P0_INT_STA.P0_SETUP_STA = 1 (Clearing the event setup data has been received)

In case the status bits related to control transfer are set, they should be cleared as follows.

- P0_INT_STA.P0_STSST_STA = 1
- P0_INT_STA.P0_STSED_STA = 1
- P0_INT_STA.P0_RCVNL_STA = 1
- P0_INT_STA.P0_ERDY_STA = 1
- P0_INT_STA.P0_FLOW_STA = 1
- P0_INT_STA.P0_STALL_STA = 1
- P0_INT_STA.P0_NRDY_STA = 1

The data buffer for PIPE0 should also be cleared just in case data of previous transfer is left in the buffer.

- P0_CON.P0_BCLR = 1 (Clearing data buffer for PIPE0)

(2) Read setup data

Read setup data from STUP_DAT_0 and STUP_DAT_1 registers.

(3) Is setup data invalid?
In case that setup data is invalid, respond with STALL. Set P0_ST_RES[1:0], P0_OT_RES[1:0] and P0_IN_RES[1:0] in P0_CON register to return STALL response in that case.

- P0_CON.P0_RES_WEN = 1
- P0_CON.P0_ST_RES[1:0] = 10b (forced STALL response)
- P0_CON.P0_OT_RES[1:0] = 10b (forced STALL response)
- P0_CON.P0_IN_RES[1:0] = 10b (forced STALL response)

With the settings above, USB3PERI returns STALL for all requests (IN, OUT or STATUS) to PIPE0. Whenever USB3PERI responds with STALL, P0_INT_STA.P0_STALL_STA is asserted. Since USB device is not required to change the response from PIPE0 until new setup data comes to PIPE0 as noted in (5) or any reset comes in that case, an interrupt due to P0_INT_STA.P0_STALL_STA can be ignored (that is, it can be masked).

(4) Recovery from STALL
If host wants to recovery the status, it will send ClearFeature(ENDPOINT_HALT) or other request. The device should initialize the response for it.
When host sends new setup data including it requests ClearFeature(ENDPOINT_HALT), P0_INT_STA.P0_SETUP_STA will be asserted again.
When the assertion of P0_INT_STA.P0_SETUP_STA is detected (it is notified on an interrupt if enabled), USB3PERI automatically sets P0_CON.P0_ST_RES[1:0], P0_CON.P0_OT_RES[1:0] and P0_CON.P0_IN_RES[1:0] to 00b (NRDY/NAK response). Note that it might take time to decide and prepare a response here. Hence it is assumed that the response is changed to normal one after the decision and the preparation.
If it does not take time, normal responses can be set here.

- New setup data is received. (It is notified on the assertion of P0_INT_STA.P0_SETUP_STA.)
  (-USB3PERI automatically sets P0_CON.P0_*_RES[1:0] to 00b, but the software can change them to normal response.)

Then, go back to (1).

(5) Decode setup data
Decode the content of setup data which is read at (2).
If wLength = 0, no data control process is being requested.
If wLength is not 0 and bmRequestType[7] is 0, control write data process is being requested. Otherwise control read process is being requested.

(6) No Data Control, Control Write or Control Read process
Refer each subsection as follows.

a) No Data Control process: Refer to **Section 35.6.5.4(1), No Data Control Process**

b) Control Write process: Refer to **Section 35.6.5.4(2), Control Write Process**

c) Control Read process: Refer to **Section 35.6.5.4(3), Control Read Process**

(7) Set the response at status stage
From (7) to (8) the settings for status stage are described. For the operations required in each process before status stage, refer to **Section 35.6.5.9, Device Requests**. Basically the process requested by setup data should be finished before the device completes the status stage. The status stage might be started before the completion of the process, but the device can put off the completion of the status stage by returning NRDY or NAK.

Set P0_CON.P0_ST_RES[1:0] as follows.

- P0_CON.P0_RES_WEN = 1

- P0_CON.P0_ST_RES[1:0] = 01b (Normal response)

For P0_CON.P0_OT_RES[1:0] and P0_CON.P0_IN_RES[1:0], keep the value set at (6) in case of Control Write process or Control Read process. In case of No Data Control process, they should be set to forced STALL response at the same time as the setting of P0_CON.P0_ST_RES[1:0].

- P0_CON.P0_OT_RES[1:0] = 10b (STALL response)
- P0_CON.P0_IN_RES[1:0] = 10b (STALL response)

(8) Complete Status Stage

Wait for the interrupt due to P0_INT_STA.P0_STSED_STA, which shows USB3PERI completes the status stage of the control transfer. Confirm P0_INT_STA.P0_STSED_STA is asserted, and then write 1 to it to clear.

- Interrupt due to P0_INT_STA.P0_STSED_STA is generated
- Check that P0_INT_STA.P0_STSED_STA = 1
- P0_INT_STA.P0_STSED_STA = 1 (Clearing the event that the status stage of control transfer has been completed.)

NOTE

In the specification of USB, it is defined that the sequence of control transfer should be initialized when new setup data is received during control transfer. Device should stop the operation for previous setup data and switch to the operation of new setup data. That case seldom occurs, but the consideration of it is required.

(1) No Data Control Process

The operation for no data control transfer is described here.

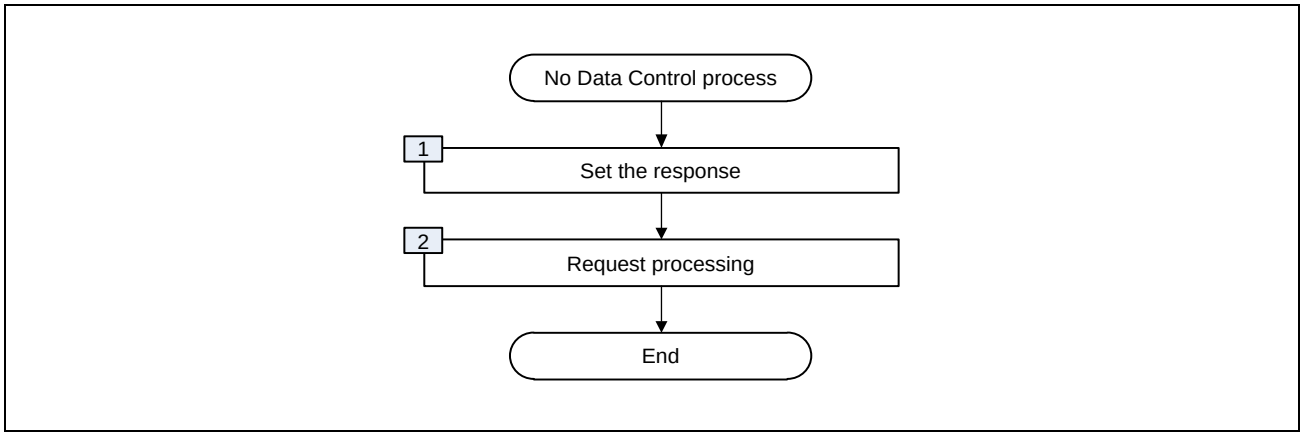


Figure 35.6-27 No Data Control Transfer Process Flow

(1) Set the response
After decoding setup data, set the response for the request.

- P0_MOD.P0_DIR = 0 (Direction = OUT)

Select NRDY/NAK response for the status stage until the operation at (2) is completed. If the operation is not needed, USB3PERI can respond with ACK immediately. The final response at the status stage is selected at (7) in the flow of **Section 35.6.5.4, Control Transfer**.
As no data is sent or received in this flow, select STALL response for IN and OUT transfer request. All of the settings below are for P0_CON register and it allows only 32-bit access, so note that they should be done in one word access.

- P0_CON.P0_RES_WEN = 1
- P0_CON.P0_ST_RES[1:0] = 00b (NRDY/NAK response. ACK response is also selectable.)
- P0_CON.P0_OT_RES[1:0] = 10b (STALL response)
- P0_CON.P0_IN_RES[1:0] = 10b (STALL response)

(2) Request processing
If any operation for the request is required, do it here.
See **Section 35.6.5.9, Device Requests** for the operations of major device requests.

(2) Control Write Process

The operation for control writer transfer is described here.

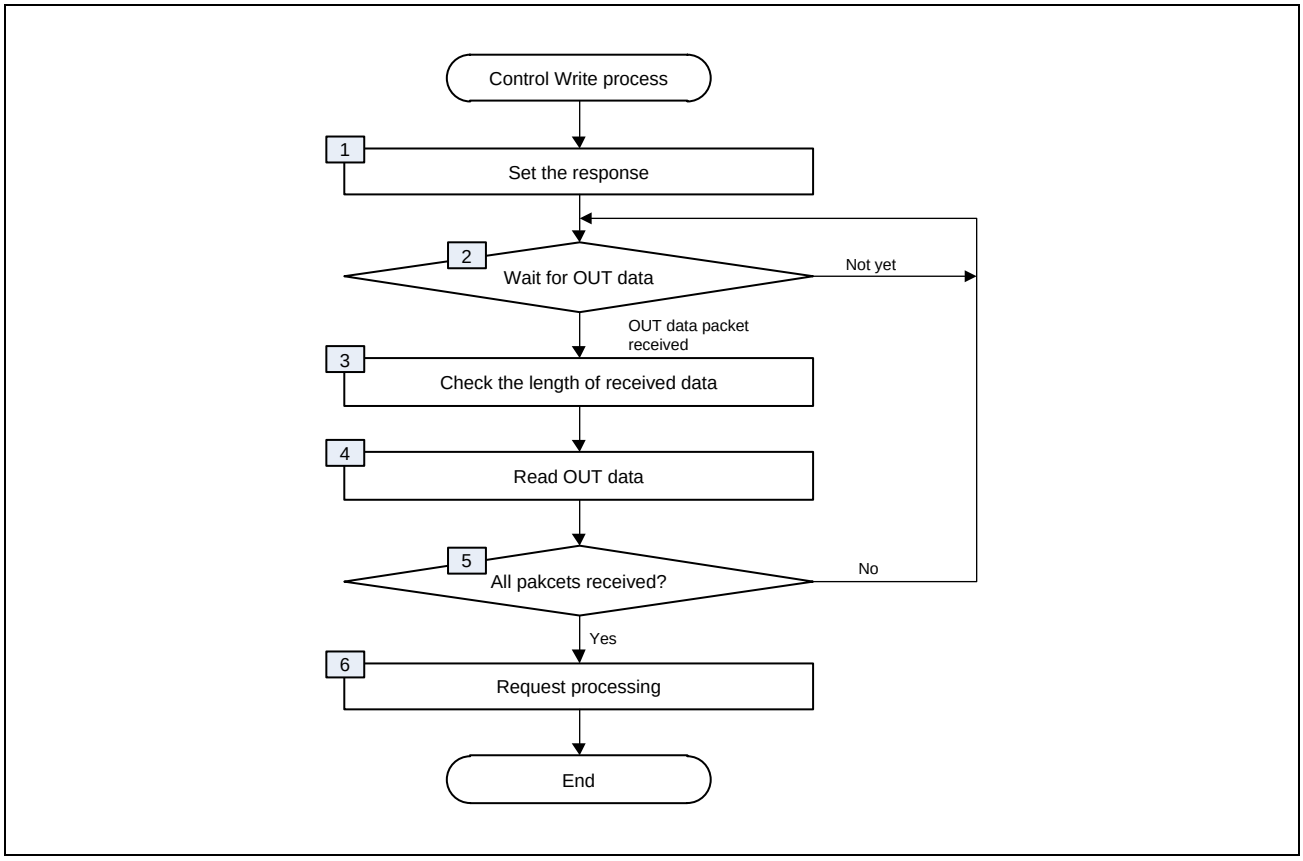


Figure 35.6-28 Control Write Process Flow

(1) Set the response

After decoding setup data, set the response for the request.

As control write transfer is requested here, select OUT as the direction of transfer.

Set NRDY/NAK response for the status stage since the data stage has not been finished yet. Set normal response for OUT and STALL response for IN.

- P0_MOD.P0_DIR = 0 (Direction = OUT)
- P0_CON.P0_RES_WEN = 1
- P0_CON.P0_ST_RES[1:0] = 00b (NRDY/NAK response)
- P0_CON.P0_OT_RES[1:0] = 01b (normal response)
- P0_CON.P0_IN_RES[1:0] = 10b (STALL response)

(2) Wait for OUT data

For control write transfer, the software reads each packet in data stage of the transfer through P0_READ register. When OUT data packet to PIPE0 Is received, an interrupt due to P0_INT_STA.P0_BFRDY_STA is asserted. In that case, write 1 to P0_INT_STA.P0_BFRDY_STA to clear.

- Interrupt due to P0_INT_STA.P0_BFRDY_STA is generated
- Check that P0_INT_STA.P0_BFRDY_STA = 1
- P0_INT_STA.P0_BFRDY_STA = 1 (Clearing the event that OUT data has been received at PIPE0)

When receiving OUT data packet, P0_STA.P0_BUFSTS is also asserted. The meaning of the bit is OUT data packet is ready to be read from P0_READ register. Polling P0_STA.P0_BUFSTS is available to know that OUT data packet has been received for the software as well.

(3) Check the length of received data
Read the following field to know the length of received data.

- Read P0_LNG.P0_LENGTH[9:0] (This field shows the number of bytes of received data)

(4) Read OUT data
Read OUT data through P0_READ register. Note that OUT data in control transfer cannot be read from Data Interface of EPC or cannot be transferred by AXI DMA transfer.
P0_READ register should be read in a unit of 32-bit. P0_READ register is updated and the next 32-bit word of received data is shown in P0_READ register every time it is read. The length of received data is known at (3) and the number of read from P0_READ register can be calculated from the length. The number of read = the length divided by 4, round-up is required if there is any residue. If there is residue, it also means the last 32-bit word read has one or more unnecessary bytes. In that case, discard unnecessary bytes.

(5) Are all packets received?
If wLength shown in setup data is more than the max packet size in control transfer, it means two or more OUT data packets would come. In that case, repeat the steps from (2) to (4) for the number of packets.

After all of OUT packets have been received and read, set the registers as follows. Note P0_CON register should be written in a unit of 32-bit and other fields should hold its value. That is, read-modify-write will be required.

- P0_CON.P0_RES_WEN = 1
- P0_CON.P0_OT_RES[1:0] = 10b (STALL response)

(6) Request processing
If any operation for the request is required, do it here.
See **Section 35.6.5.9, Device Requests** for the operations of major device requests.

(3) Control Read Process

The operation for control read transfer is described here.

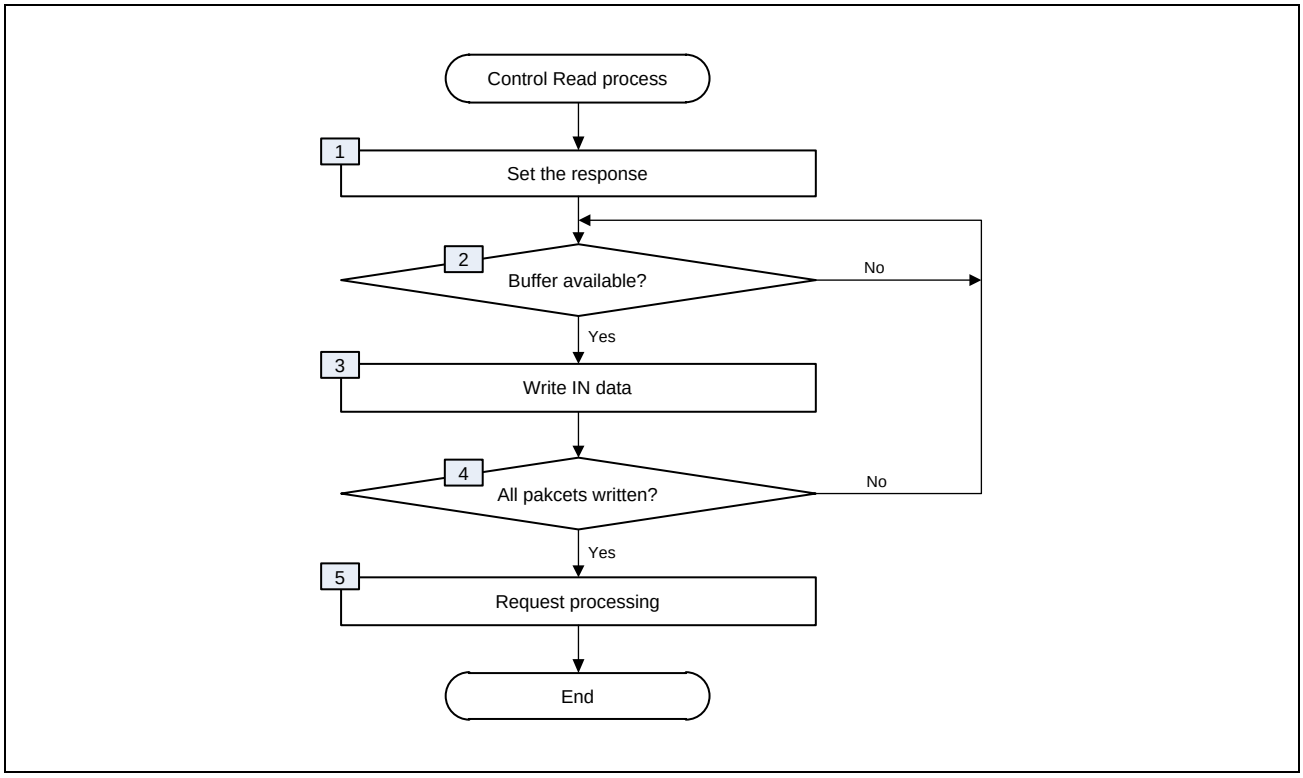


Figure 35.6-29 Control Read Process Flow

(1) Set the response

After decoding setup data, set the response for the request.

As control read transfer is requested here, select IN as the direction of transfer.

Set NRDY/NAK response for the status stage since the data stage has not been finished yet. Set normal response for IN and STALL response for OUT.

- P0_MOD.P0_DIR = 1 (Direction = IN)
- P0_CON.P0_RES_WEN = 1
- P0_CON.P0_ST_RES[1:0] = 00b (NRDY/NAK response)
- P0_CON.P0_OT_RES[1:0] = 10b (STALL response)
- P0_CON.P0_IN_RES[1:0] = 01b (Normal response)

(2) Check if buffer is available

For control read transfer, the software writes each packet in data stage of the transfer through P0_WRITE register. But if there is no space available in the buffer for PIPE0, it cannot write. P0_STA.P0_BUFSTS shows if there is available space in the buffer. See the bit before writing IN data packet to P0_WRITE register.

- Check whether P0_STA.P0_BUFSTS = 1 or not

If P0_STA.P0_BUFSTS is 0 and there is no available space in the buffer currently, wait until P0_STA.P0_BUFSTS becomes 1 or an interrupt due to P0_INT_STA.P0_BFRDY_STA is asserted. When IN is selected as the direction of PIPE0 (that is, P0_MOD.P0_DIR = 1), P0_INT_STA.P0_BFRDY_STA is asserted when the buffer for PIPE0 becomes available for new write data.

Therefore, the software can know the timing the buffer for PIPE0 prepares new available space by polling

P0_STA.P0_BUFSTS or an interrupt due to P0_INT_STA.P0_BFRDY_STA.
But, Note that P0_INT_STA.P0_BFRDY_STA is not asserted just after a reset (hardware reset, USB_COM_CON.PIPE_CLR, P0_CON.P0_BCLR and P0_CON.P0_CLR) and when the software writes the first packet. In that case, since the buffer has available space just after a reset, so the software can write the packet without being notified on an interrupt due to P0_INT_STA.P0_BFRDY_STA. The software still can see P0_STA.P0_BUFSTS in that case.

(3) Write IN data
Write IN data through P0_WRITE register. Note that IN data in control transfer cannot be written through Data Interface of EPC or cannot be transferred by AXI DMA transfer.
P0_WRITE register should be written in a unit of 32-bit. The number of write can be calculated as the number of write = the length divided by 4, round-up is required if there is any residue. The written words are concatenated as one packet.
When the length of packet is not multiples of 32-bit, the last word has unnecessary bytes. The last written word should be also written as a 32-bit word. The number of valid bytes in the last word is set in P0_CON.P0_BYTE_EN. Unnecessary bytes in the last word are discarded.
To send the packet, set the registers as follows after the last word has been written.

- P0_CON.P0_SEND = 1
- P0_CON.P0_BYTE_EN[1:0] = xxb (the number of valid byes in last written word)

NOTE

Zero length packet will be sent if P0_CON.P0_SEND is set to 1 after P0_WRITE register is written nothing in the above. In this case, P0_CON.P0_BYTE_EN[1:0] is ignored (it's usually set “00” at the same time P0_SEND is set).

See **Section 35.6.4.6, Zero Length Packet (ZLP)** about zero length packet.

(4) Are all packets written?
If wLength shown in setup data is more than the max packet size in control transfer, it means two or more IN data packets are required. In that case, repeat the steps from (2) to (3) for the number of packets.

After all of IN packets have been sent, set the registers as follows. Note P0_CON register should be written in a unit of 32-bit and other fields should hold its value. That is, read-modify-write will be required.

- P0_CON.P0_RES_WEN = 1
- P0_CON.P0_IN_RES[1:0] = 01b (STALL response)

(5) Request processing
If any operation for the request is required, do it here.
See **Section 35.6.5.9, Device Requests** for the operations of major device requests.

35.6.5.5 Bulk Transfer

The operation for bulk transfer is described here.

PIPEs other than PIPE0 (PIPE0 is used only for control transfer) can be used for bulk transfer. The settings for bulk transfer are shown below.

- PIPE_COM.PIPE_NUM[4:0] = the index of PIPE used for the current bulk transfer
- Pn_MOD.Pn_EPNUM[3:0] = the endpoint number of the PIPE
- Pn_MOD.Pn_TYPE[1:0] = 10b (bulk transfer)
- Pn_MOD.Pn_DIR = the direction of transfer
- Pn_MOD.Pn_STREAM = whether the PIPE is used for Stream bulk transfer or not
- Pn_MOD.Pn_BOT = whether the PIPE uses BOT or not
- Pn_MOD.Pn_ERDY_CON[1:0] = threshold to send ERDY
- Pn_RAMMAP.Pn_BASEAD[13:0] = the base address of buffer assigned for the PIPE
- Pn_RAMMAP.Pn_RAMIF[1:0] = the index of RAM interface of the PIPE
- Pn_RAMMAP.Pn_MPKT[10:0] = 1024bytes for SS, 512 bytes for HS or 64 bytes for FS
- Pn_RAMMAP.Pn_RAMAREA = the size of RAM area assigned for the PIPE
- Pn_CON.Pn_DATAIF_EN = whether Data Interface of EPC or AXI-IF is used or not.
- Pn_CON.Pn_EN = 1 (the PIPE is enabled)

These settings are done just after Set Configuration is completed and the device enters configured state. But if the device has only single configuration for each PIPE, these settings can be done after the device is turned on.

(1) Bulk-IN Process

The normal bulk IN process is described here. See **Section 35.6.5.5(3), Stream Bulk Process** for Stream bulk process.

In this subsection the process to write bulk IN packet through Data Interface of EPC or Pn_WRITE register is described. DMA transfer as the master function of AXI-IF is available. See **Section 35.6.5.7, DMA Transfer** for the process using DMA transfer.

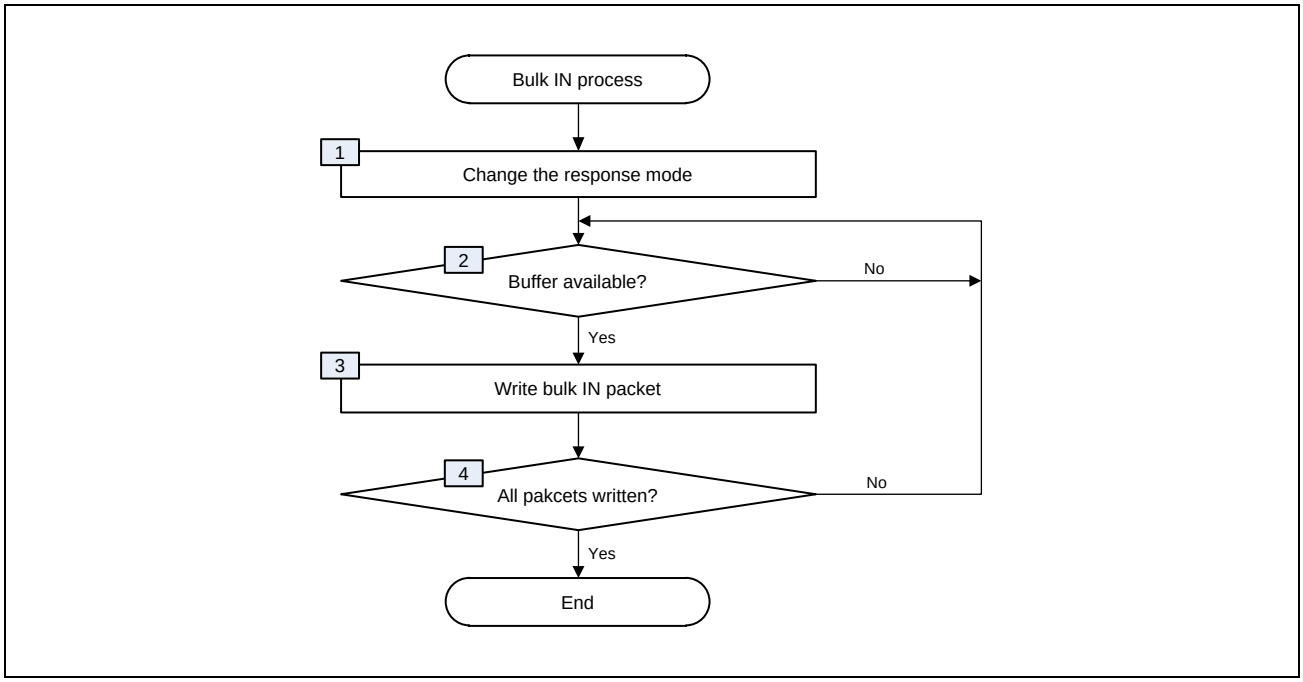


Figure 35.6-30 Bulk IN Process Flow

(1) Change the response mode of the bulk IN PIPE
Change the response mode of the bulk IN PIPE to normal response so that the PIPE can transmit data.

- Pn_CON.Pn_RES_WEN = 1
- Pn_CON.Pn_RES[1:0] = 01b (Normal response)

(2) Check if buffer is available
Check if buffer for the bulk IN PIPE is available before writing bulk IN packet. Pn_STA.Pn_BUFSTS shows if the buffer is available or not.

- Check whether Pn_STA.Pn_BUFSTS = 1 or not

If Pn_STA.Pn_BUFSTS is 0 and there is no available space in the buffer currently, wait until Pn_STA.Pn_BUFSTS becomes 1 or an interrupt due to Pn_INT_STA.Pn_BFRDY_STA is asserted. When IN is selected as the direction of the bulk PIPE (that is, Pn_MOD.Pn_DIR = 1), Pn_INT_STA.Pn_BFRDY_STA is asserted when the buffer of the PIPE becomes available for new write data.
Therefore, the software can know the timing the buffer of the PIPE prepares new available space by polling Pn_STA.Pn_BUFSTS or an interrupt due to Pn_INT_STA.Pn_BFRDY_STA.
But, Note that Pn_INT_STA.Pn_BFRDY_STA is not asserted just after a reset (hardware reset, USB_COM_CON.PIPE_CLR, Pn_CON.Pn_BCLR and Pn_CON.Pn_CLR) and when the software writes the first packet. In that case, since the buffer has available space just after a reset, so the software can write the packet without being notified on an interrupt due to Pn_INT_STA.Pn_BFRDY_STA. The software still can see Pn_STA.Pn_BUFSTS in that case.

(3) Write bulk IN packet
Write bulk IN packet to be transmitted to the buffer. Bulk IN data is written in a unit of packet and the buffer cannot accept data across the max packet size defined in Pn_RAMMAP.Pn_MPKT[10:0].

[writing through Pn_WRITE register]

a-1) Write data through Pn_WRITE register. Since only 32-bit access is allowed to the register, data should be written in a unit of 32-bit. The number of write can be calculated as the number of write = the length divided by 4, round-up is required if there is any residue. The written words are concatenated as one packet.
When the length of packet is not multiples of 32-bit, the last written word may have unnecessary bytes. The last word should be also written as a 32-bit word. The number of valid bytes in the last word is set in Pn_CON.Pn_BYTE_EN[1:0]. Unnecessary bytes in the last word are discarded.

a-2) Set fields as follows to send the packet. Since only 32-bit access is allowed to Pn_CON register, all fields below should be set in one word access.

- Pn_CON.Pn_SEND = 1
- Pn_CON.Pn_BYTE_EN[1:0] = xxb (the number of valid byes in last written word)
- In case of the last packet of data group, set Pn_CON.Pn_LAST = 1

NOTE

Zero length packet will be sent if Pn_CON.Pn_SEND is set to 1 after Pn_WRITE register is written nothing in the above. In this case, Pn_CON.Pn_BYTE_EN[1:0] is ignored (it's usually set “00” at the same time Pn_SEND is set).

See **Section 35.6.4.6, Zero Length Packet (ZLP)** about zero length packet.

(4) Are all packets written?
If it is required to send two or more packets, repeat the steps from (2) to (3).

NOTE

When the information of a certain PIPE is read from or write to PIPEn registers, PIPE_COM.PIPE_NUM[4:0] should have the index of the PIPE.

(2) Bulk-OUT Process

The normal Bulk-OUT process is described here. See **Section 35.6.5.5(3), Stream Bulk Process** for Stream bulk process.

In this subsection the process to read bulk OUT packet through Data Interface of EPC or Pn_READ register is described. DMA transfer as the master function of AXI-IF is available. See **Section 35.6.5.7, DMA Transfer** for the process using DMA transfer.

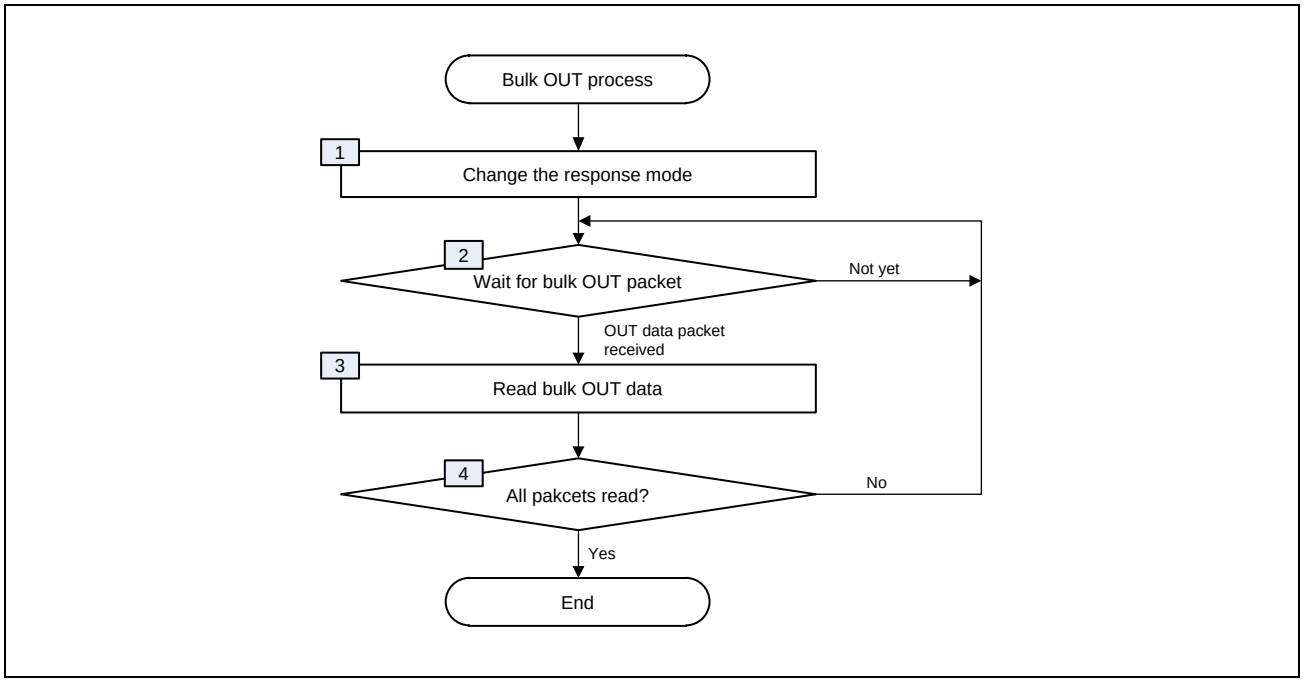


Figure 35.6-31 Bulk OUT Process Flow

(1) Change the response mode of the bulk OUT PIPE
Change the response mode of the bulk OUT PIPE to normal response so that the PIPE can receive data.

- Pn_CON.Pn_RES_WEN = 1
- Pn_CON.Pn_RES[1:0] = 01b (Normal response)

(2) Wait for bulk OUT data
When bulk OUT data to the PIPE is received, an interrupt due to Pn_INT_STA.Pn_BFRDY_STA is asserted. In that case, write 1 to Pn_INT_STA.Pn_BFRDY_STA to clear.

- Interrupt due to Pn_INT_STA.Pn_BFRDY_STA asserted
- Check whether Pn_INT_STA.Pn_BFRDY_STA = 1 or not.
- Pn_INT_STA.Pn_BFRDY_STA = 1 (clearing the event that OUT data is received at the PIPE)

When receiving OUT data packet, Pn_STA.Pn_BUFSTS is also asserted. The meaning of the bit is bulk OUT data packet is ready to be read from Pn_READ register or through Data Interface of EPC. Polling Pn_STA.Pn_BUFSTS is available to know that OUT data packet has been received for the software as well.

(3) Read bulk OUT packet
Read bulk OUT packet from the buffer. Bulk OUT data is read in a unit of packet and the buffer cannot be read across the max packet size defined in Pn_RAMMAP.Pn_MPKT[10:0].

[reading through Pn_READ register]

a-1) Read Pn_LNG register in order to know the length of received data

a-2) Read received packet through Pn_READ register.
Pn_READ register should be read in a unit of 32-bit. Pn_READ register is updated and the next 32-bit word of received data is shown in Pn_READ register every time it is read. The length of received data is known at a-1) and the number of read from Pn_READ register can be calculated from the length. The number of read = the length divided by 4, round-up is required if there is any residue. If there is residue, it also means the last 32-bit word read has one or more unnecessary bytes. In that case, discard unnecessary bytes.

(4) Are all packets read?
If the bulk OUT PIPE has more packets to be read, repeat the steps from (2) to (3).
Pn_INT_STA.Pn_LSTTR_STA is asserted when the last packet (short packet or packet with PP = 0) is received.

When a short packet or a packet with PP = 0 (PP is used only in USB3.1) is received, USB3PERI recognizes it is the last packet of the current transfer. It returns ACK with NumP = 0 to host after receiving the packet. ACK with NumP = 0 means that the device cannot receive any more packet currently. The device should send ERDY when it wants to resume the transfer. When the last packet (short packet or packet with PP = 0) has been read to DMAC side and the buffer of the PIPE has available space, USB3PERI automatically send ERDY to request the resume of transfer.
Note that USB3PERI may return ACK with NumP = 0 even when the received packet is not the last packet if it has no available buffer at that time. But when USB3PERI gets available space in the buffer of the PIPE, it automatically sends ERDY to resume the transfer for the PIPE.

NOTE

When the information of a certain PIPE is read from or write to PIPEn registers, PIPE_COM.PIPE_NUM[4:0] should have the index of the PIPE.

(3) Stream Bulk Process

The process of stream bulk, especially UASP (USB Attached SCSI protocol) application as an example is described here.

(a) PIPE structure of UASP

UASP assumes 4 pipe model, not including control pipe (PIPE0). The pipes are Command (OUT), Status (IN), Data-in (IN) and Data-out (OUT).

UAS driver sends a command through host stack to Command pipe, device receives it and returns the status or the result for the command from Status pipe. Device receives OUT packet at Data-out pipe or returns IN packet from Data-In pipe, if required.

Stream protocol is used for the parallel operation for commands. Device can receive multiple commands to Command pipe at once. It returns statuses from Status pipe or IN packets from Data-in pipe, or receives OUT packets to Data-out pipe, in “out-of-order” way. Each command has a Stream ID as a tag, and Stream protocol is used for the tagging.

Note Status pipe, Data-in pipe and Data-out pipe are Stream bulk pipes but Command pipe is not. Stream ID is provided in CIU (Command IU) which is received at Command pipe.

(b) Basic Stream Bulk IN Process

The basic process of Stream bulk IN is described here.

Stream bulk IN pipe should have Pn_MOD.Pn_STREAM = 1 as noted in the first part of **Section 35.6.5.5, Bulk Transfer**.

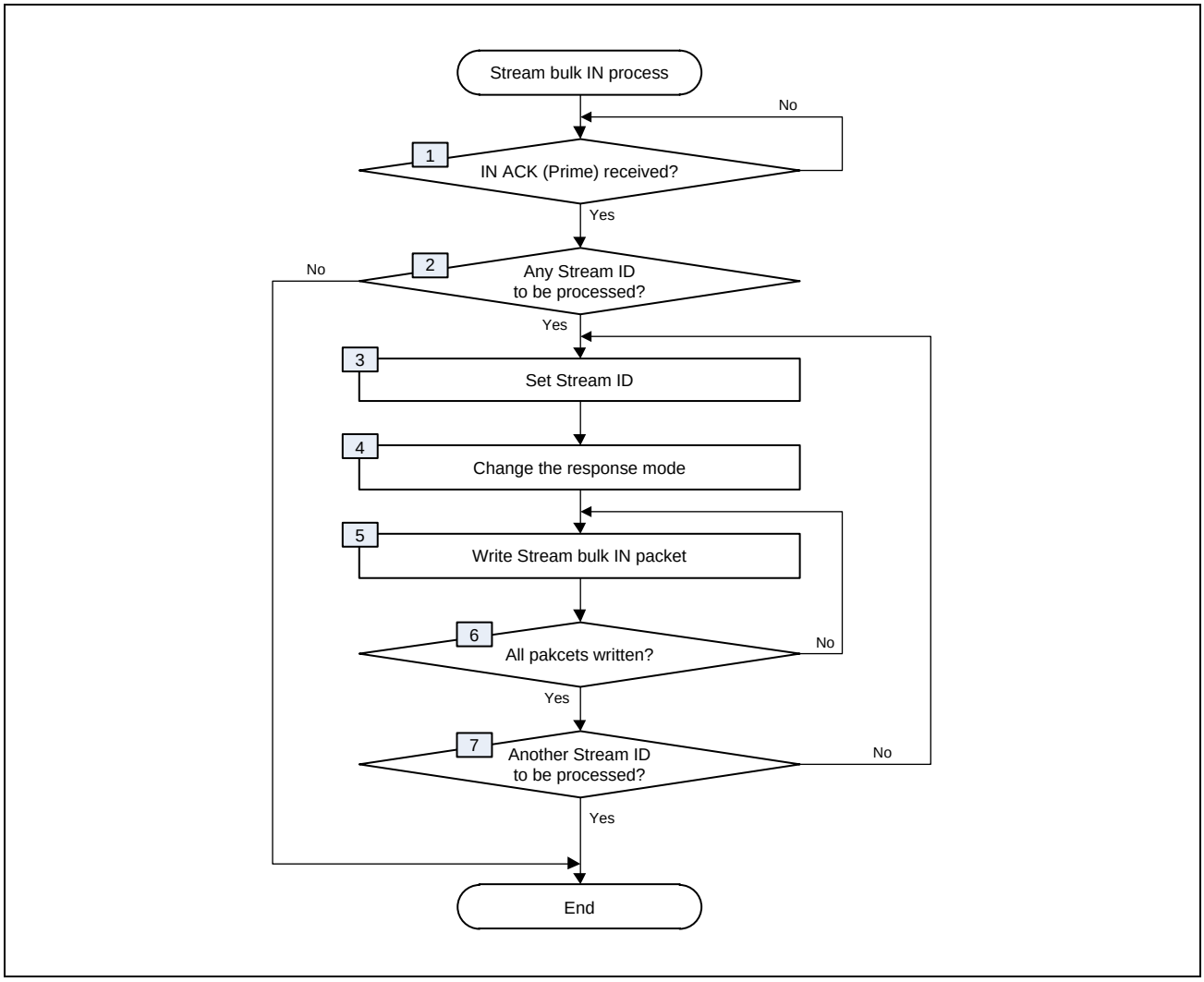


Figure 35.6-32 Basic Stream Bulk IN Process Flow

(1) Is IN ACK(Prime) received?

IN ACK(Prime) is used to inform device that one or more streams are added to the IN pipe and transfer for it will be started. In case Stream Bulk IN pipe receives IN ACK(Prime), it always responds with NRDY(Prime). Receiving IN ACK(Prime) means the pipe transits to Prime Pipe state of Stream Bulk state machine, and sending NRDY(Prime) means it goes back to Idle state.

USB3PERI automatically changes the setting of Pn_CON.Pn_RES[1:0] of the IN pipe to return NRDY (= 00b) and sends NRDY(Prime) to host.

The reception of IN ACK(Prime) is notified on the assertion of Pn_INT_STA.Pn_PRIME_STA. An interrupt due to it is asserted if enabled.

- Interrupt due to Pn_INT_STA.Pn_PRIME_STA is asserted, if enabled.
- Check that Pn_INT_STA.Pn_PRIME_STA = 1

After the confirmation above, clear Pn_INT_STA.Pn_PRIME_STA.

- Pn_INT_STA.Pn_PRIME_STA = 1 (Clearing the event that IN ACK(Prime) is received)

Then, the IN pipe is required to prepare to transfer Stream Bulk IN data.

(2) Is there any Stream ID to be returned?
The data returned from Stream bulk IN pipe should be tagged by Stream ID. The ID is notified in the command from host in advance. In UASP, CIU (Command IU) is sent to Command pipe and the command ID in CIU is used as Stream ID.
If device has received multiple commands, it should decide which command is processed first. In UASP, the operation for Stream is closely related to NCQ (native command queuing) of storage. Stream bulk IN pipe returns data in the order the storage returns.
If there is any Stream ID to be returned, proceed to (3).

(3) Set Stream ID
Set Stream ID of data which is to be returned next to Pn_STREAMID.Pn_STREAM_N[15:0].

- Pn_STREAMID.Pn_STREAM_N[15:0] = The next stream ID

(4) Change the response mode of Stream bulk IN pipe
As the IN pipe returned NRDY at (1), so it is in the flow control state. The response mode of the IN pipe was changed to “forced NRDY or NAK response” (= 00b).
Change the response mode of the IN pipe to normal response mode.

- Pn_CON.Pn_RES_WEN = 1
- Pn_CON.Pn_RES[1:0] = 01b (Normal response)

(5) Write Stream bulk IN packet
Write Stream bulk IN packet to be transmitted to the buffer. This step is the same as that for normal bulk IN.
Stream bulk IN data is written in a unit of packet and the buffer cannot accept data across the max packet size defined in Pn_RAMMAP.Pn_MPKT[10:0].
It is also required to see whether there is available space in the buffer or not on Pn_INT_STA.Pn_BFRDY_STA or Pn_STA.Pn_BUFSTS. See **Section 35.6.5.5(1), Bulk-IN Process** for details.

[writing through Pn_WRITE register]

a-1) Write data through Pn_WRITE register. Since only 32-bit access is allowed to the register, data should be written in a unit of 32-bit. The number of write can be calculated as the number of write = the length divided by 4, round-up is required if there is any residue. The written words are concatenated as one packet.
When the length of packet is not multiples of 32-bit, the last written word has unnecessary bytes.
The last word should be also written as a 32-bit word. The number of valid bytes in the last word is set in Pn_CON.Pn_BYTE_EN[1:0]. Unnecessary bytes in the last word are discarded.

a-2) Set fields as follows to send the packet. Since only 32-bit access is allowed to Pn_CON register, all fields below should be set in one word access.

- Pn_CON.Pn_SEND = 1
- Pn_CON.Pn_BYTE_EN[1:0] = xxb (The number of valid byes in last written word)
- In case of the last packet of data group, set Pn_CON.Pn_LAST= 1

NOTE

Zero length packet will be sent if Pn_CON.Pn_SEND is set to 1 after Pn_WRITE register is written nothing in the above. In this case, Pn_CON.Pn_BYTE_EN[1:0] is ignored (it's usually set “00” at the same time Pn_SEND is set).

See **Section 35.6.4.6, Zero Length Packet (ZLP)** about zero length packet.

[Using DMA transfer with AXI-IF]
See **Section 35.6.5.7, DMA Transfer** for details.

When the first packet for the Stream ID (= CStream) is written to buffer, USB3PERI returns ERDY(CStream) to host. This means not only the exit from flow control state but the selection of Stream from device. If host agrees the selection, it sends IN ACK(CStream) to start transfer for the Stream ID.

(6) Are all packets written?
If it is required to send two or more packets, repeat the step of (5).
When the last packet for the Stream ID is written, make sure to indicate that on Pn_CON.Pn_LAST (in case data is written through Pn_WRITE register), EPC_D_DBWTRANSEND (in case data is transferred through Data Interface of EPC) or Lst bit in PRD table (with AXI-IF).

(7) Is there another Stream ID to be returned?
When the last packet written at (6) is sent to host, EOB (end of burst) bit in it is set to 1 so that it shows the packet is the last one in the burst. Host will send ACK(NumP = 0) as the response to the packet with EOB=1. This means the IN pipe enters flow control state again.
If there is another Stream ID to be returned, repeat the steps from (2) to (6).

Note that USB3PERI might set EOB = 1 in the packet which is not the last one for the Stream ID (= CStream) in case that the preparation of data is delayed and there is no packet in buffer to be sent next to the current packet. In that case, actually EOB is set to 1 in the packet and the IN pipe is considered as being in the flow control state, but no additional operation is required by the software. When the next packet is written in buffer, the IN pipe sends ERDY(CStream) automatically. This means not only the exit from the flow control state but the selection of CStream again. The IN transfer for CStream will be started.

NOTE

When the information of a certain PIPE is read from or write to PIPEn registers, PIPE_COM.PIPE_NUM[4:0] should have the index of the PIPE.

NOTE

It is possible for host to send ACK(Stream x) and initiates the selection of the Stream. But, basically, to decrease the size of buffer and increase the performance of device, it is desirable that device decides what Stream is processed next seeing its status and initiates the selection of stream. Besides, device cannot send data related to the Stream ID which is not prepared yet. Therefore, USB3PERI responds with NRDY if Stream x is not equal to the Stream ID in Pn_STREAMID.Pn_STREAM_C[15:0]. USB3PERI asserts Pn_INT_STA.Pn_STRMX_STA in case Stream ID in the received packet is not same as that in Pn_STREAMID.Pn_STREAM_C[15:0], Prime nor NoStream. In that case, the Stream ID requested in the received packet is shown in Pn_NRDYSTRM register.
It is possible to give priority to the Stream ID requested from host by checking Pn_NRDYSTRM register, but it is assumed here that device requests another Stream ID which it decided to process.
Especially, READ READY IU and WRITE READY IU are defined to show which stream (command) is processed next from device in UASP. ERDY(Stream) is used in Super Speed Stream Bulk of UASP just as the substitution of them. Therefore the device initiates the selection of stream in this flow.

NOTE

From the definition in USB3.1 specification, device which selects the Stream by returning ERDY(Stream) may receive ACK(No Stream) from host. ACK(No Stream) means the rejection from host for proposed Stream ID in ERDY. In such case, device should consider the Stream as “Not Ready”, and may select another Stream.

It depends on the application whether No Stream is really used or not.

(c) Basic Stream Bulk OUT Process

The basic process of Stream bulk OUT is described here.

Stream bulk OUT pipe should have Pn_MOD.Pn_STREAM = 1 as noted in the first part of **Section 35.6.5.5, Bulk Transfer**.

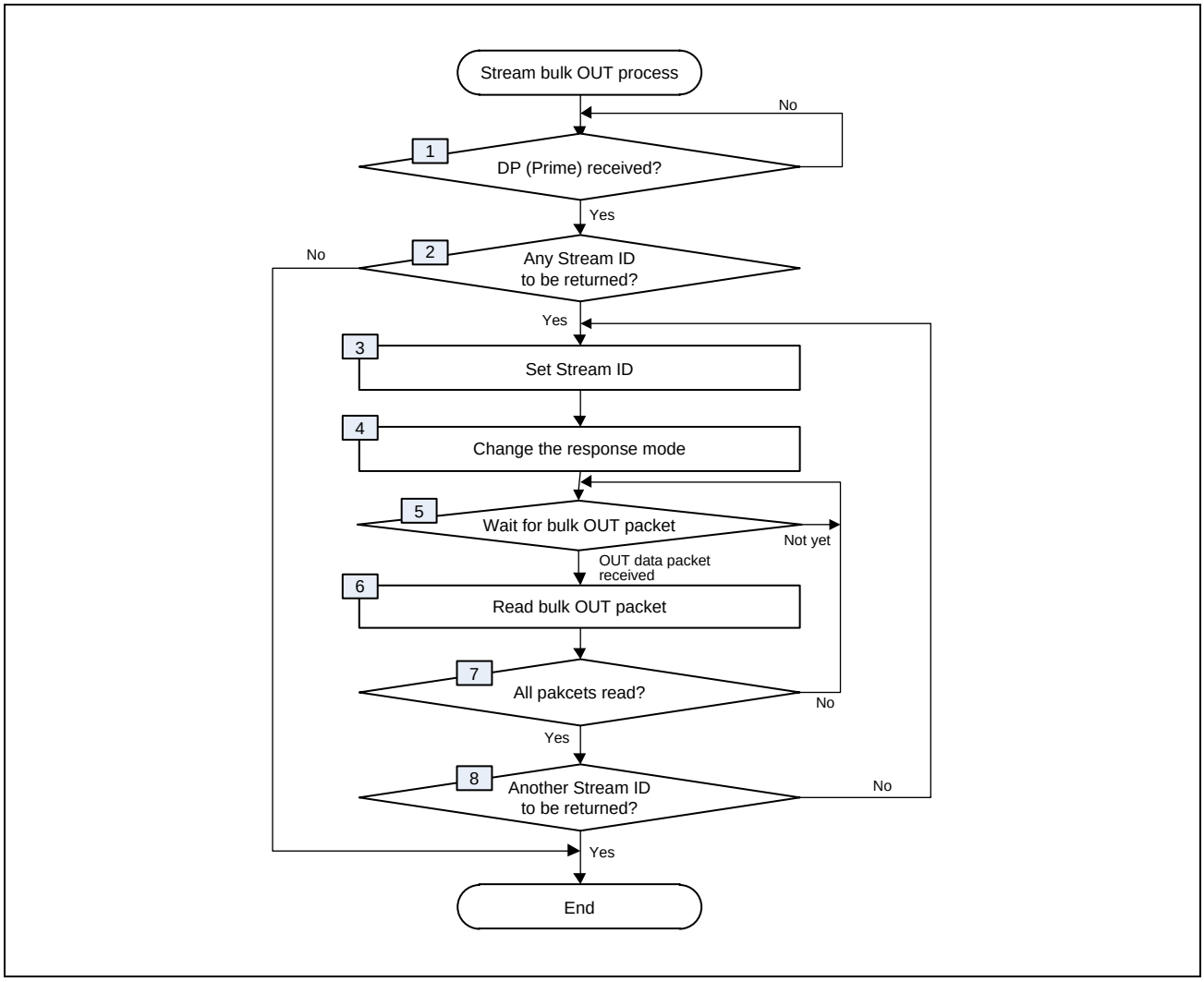


Figure 35.6-33 Basic Stream Bulk OUT Process Flow

(1) Is DP(Prime) received?

DP(Prime) is used to inform device that one or more streams are added to the OUT pipe and transfer for it will be started. In case Stream Bulk OUT pipe receives DP(Prime), it always responds with NRDY(Prime). Receiving DP(Prime) means the pipe is requested to enter Prime Pipe state of Stream Bulk state machine, and sending NRDY(Prime) means it goes back to Idle state.

USB3PERI automatically changes the setting of Pn_CON.Pn_RES[1:0] of the OUT pipe to return NRDY (= 00b) and sends NRDY(Prime) to host.

The reception of DP(Prime) is notified on the assertion of Pn_INT_STA.Pn_PRIME_STA. An interrupt due to it is asserted if enabled.

- Interrupt due to Pn_INT_STA.Pn_PRIME_STA is asserted, if enabled.
- Check that Pn_INT_STA.Pn_PRIME_STA = 1

After the confirmation above, clear Pn_INT_STA.Pn_PRIME_STA.

- Pn_INT_STA.Pn_PRIME_STA = 1 (Clearing the event that DP(Prime) is received)

Then, the OUT pipe is required to prepare to transfer Stream Bulk OUT data.

(2) Is there any Stream ID to be processed
The data received at Stream bulk OUT pipe should be tagged by Stream ID. The ID is notified in the command from host in advance. In UASP, CIU (Command IU) is sent to Command pipe and the command ID in CIU is used as Stream ID.
If device has received multiple commands, it should decide which command is processed. In UASP, the operation for Stream is closely related to NCQ (native command queuing) of storage. Stream bulk OUT pipe processes the stream in the order the storage specifies
If there is any Stream ID to be processed, proceed to (3).

(3) Set Stream ID
Set Stream ID of the Stream which is processed next to Pn_STREAMID.Pn_STREAM_N[15:0].

- Pn_STREAMID.Pn_STREAM_N[15:0] = The next stream ID

(4) Change the response mode of Stream bulk OUT pipe
As the OUT pipe returned NRDY at (1), so it is in the flow control state. The response mode of the OUT pipe was changed to “forced NRDY or NAK response” (= 00b).
Change the response mode of the OUT pipe to normal response mode.

- Pn_CON.Pn_RES_WEN = 1
- Pn_CON.Pn_RES[1:0] = 01b (Normal response)

After the setting above, ERDY(CStream) is sent from the OUT pipe to host. This means not only the exit from flow control state but the selection of Stream from device. If host agrees the selection, it start the transfer for the stream and sends DP(CStream)

(5) Wait for bulk OUT data
When bulk OUT data to the OUT PIPE is received, an interrupt due to Pn_INT_STA.Pn_BFRDY_STA is asserted. In that case, write 1 to Pn_INT_STA.Pn_BFRDY_STA to clear. This step is the same as that for normal bulk OUT.

- Interrupt due to Pn_INT_STA.Pn_BFRDY_STA asserted
- Check Pn_INT_STA.Pn_BFRDY_STA = 1 or not.
- Pn_INT_STA.Pn_BFRDY_STA = 1 (Clearing the event that OUT data is received at the PIPE)

When receiving OUT data packet, Pn_STA.Pn_BUFSTS is also asserted. The meaning of the bit is bulk OUT data packet is ready to be read from Pn_READ register or through Data Interface of EPC. The software can poll Pn_STA.Pn_BUFSTS to know that OUT data packet has been received for the software as well.

(6) Read bulk OUT packet
Read bulk OUT packet from the buffer. Bulk OUT data is read in a unit of packet and the buffer cannot be read across the max packet size defined in Pn_RAMMAP.Pn_MPKT[10:0]. This step is the same as that for normal bulk OUT.

[Reading through Pn_READ register]

a-1) Read Pn_LNG.Pn_LENGTH[15:0] in order to know the length of received data

a-2) Read received packet through Pn_READ register.
Pn_READ register should be read in a unit of 32-bit. Pn_READ register is updated and the next 32-bit word of received data is shown in Pn_READ register every time it is read. The length of received data is known at a-1) and the number of read from Pn_READ register can be calculated from the length. The

number of read = the length divided by 4, round-up is required if there is any residue. If there is residue, it also means the last 32-bit word read has one or more unnecessary bytes. In that case, discard unnecessary bytes.

[Using DMA transfer with AXI-IF]
See **Section 35.6.5.7, DMA Transfer** for details.

(7) Are all packets read?
If the bulk OUT PIPE has more packets to be read, repeat the steps from (5) to (6).
Pn_INT_STA.Pn_LSTTR_STA is asserted when the last packet (short packet or packet with PP = 0) is received.

(8) Is there another Stream ID to be processed?
When the last packet is received at (7), USB3PERI returns ACK with NumP = 0. This means the OUT pipe enters flow control state again.
If there is another Stream ID to be returned, repeat the steps from (2) to (7). Note that Pn_CON.Pn_RES[1:0] was changed to 00b (NAK/NRDY response) when the PIPE received the last packet and returned ACK with NumP=0. Pn_CON.Pn_RES[1:0] is changed to 01b (normal response) at (4) again, and the PIPE transmits ERDY to resume the transfer.
It is also noted that USB3PERI might return ACK with NumP = 0 for the packet which is not the last one for the Stream ID (= CStream) in case that there is no available space in the buffer for the PIPE currently. In that case, actually NumP is set to 0 in the ACK packet and the OUT pipe is considered as being in the flow control state, but no additional operation is required for the software. When the received packet is transferred to system memory and USB3PERI gets available space in the buffer, the OUT pipe sends ERDY(CStream) automatically. This means not only the exit from the flow control state but the selection of CStream again. The OUT transfer for CStream will be started.

NOTE

When the information of a certain PIPE is read from or write to PIPEn registers, PIPE_COM.PIPE_NUM[4:0] should have the index of the PIPE.

NOTE

It is possible for host to send ACK(Stream x) and initiates the selection of the Stream. But, basically, to decrease the size of buffer and increase the performance of device, it is desirable that device decides what Stream is processed first seeing its status and initiates the selection of stream. Besides, device cannot send for Stream ID which is not available yet. Therefore, USB3PERI responds with NRDY if Stream x is not equal to the Stream ID in Pn_STREAMID.Pn_STREAM_C[15:0]. USB3PERI asserts Pn_INT_STA.Pn_STRMX_STA in case Stream ID in the received packet is not equal to that in Pn_STREAMID.Pn_STREAM_C[15:0], Prime nor NoStream. In that case, the Stream ID contained in the received packet is shown in Pn_NRDYSTRM register.

It is possible to give priority to the Stream ID requested from host by checking Pn_NRDYSTRM register, but it is assumed here that device requests another Stream ID it decided to process.

Especially, READ READY IU and WRITE READY IU are defined to select which stream (command) is processed next from device in UASP. ERDY(Stream) used in super speed Stream Bulk of UASP is alternative of them. So the device initiates the selection of stream in UASP.

NOTE

From the definition in USB3.1 specification, device selects the Stream by returning ERDY(Stream) may receive ACK(No Stream) from host. ACK(No Stream) means the rejection from host for proposed Stream ID in ERDY. In such case, device should consider the Stream as “Not Ready”, and may select another Stream.

It depends on the application whether No Stream is really used or not.

(4) SuperSpeed UASP Non-Data Transfer

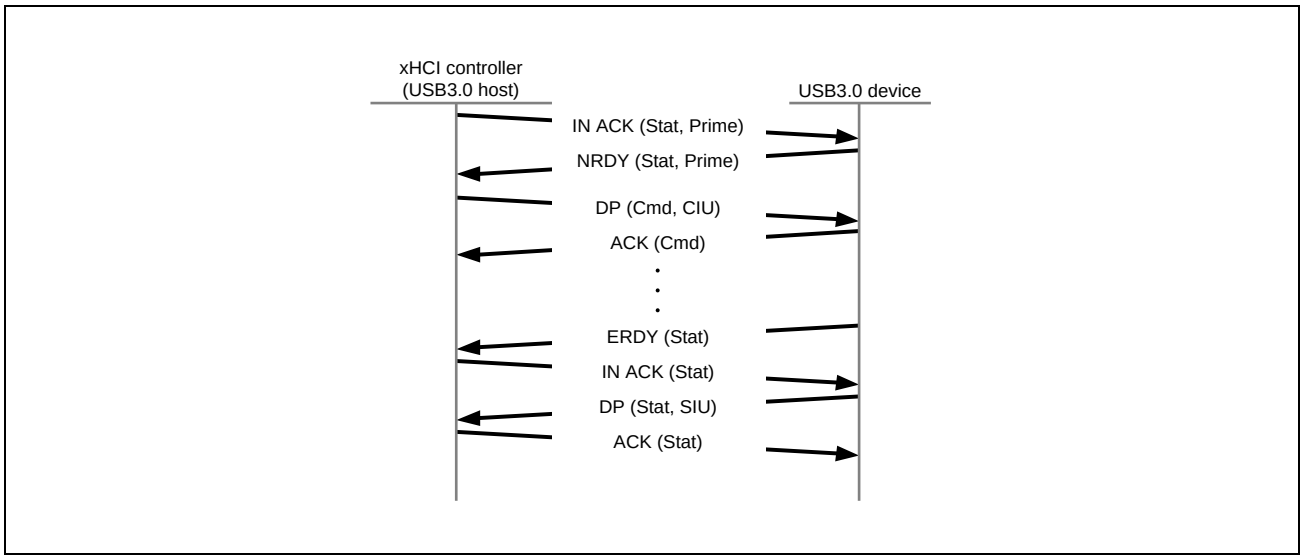


Figure 35.6-34 Example SuperSpeed UASP Non-Data Transfer

Figure 35.6-34 shows the part between USB3.1 host and USB3.1 device of Figure 6 in UASP specification Rev.1.0. The example is called as “Non-Data Transfer” but the status PIPE is working as the Stream bulk IN PIPE.

In this case, IN ACK(Stat, Prime) comes to the status PIPE first, then the status PIPE returns NRDY(Stat, Prime).

The some operation is requested on DP(Cmd, CIU) to the command PIPE. The command ID in CIU is used as Stream ID later. When the operation is completed, SIU as the result of the operation is returned from the status PIPE.

Pn_CON.Pn_RES[1:0] is set to 01b (normal response) at (4) of **Section 35.6.5.5(3)(b), Basic Stream Bulk IN Process**. When SIU is written to buffer of the status PIPE and it is ready to be transmitted, ERDY(Stat) is sent in order to resume the transfer. IN ACK(Stat) comes to the status PIPE, it sends DP(Stat, SIU) and DP(Stat, SIU) is acknowledged by ACK(Stat).

(5) SuperSpeed UASP Data-IN transfer

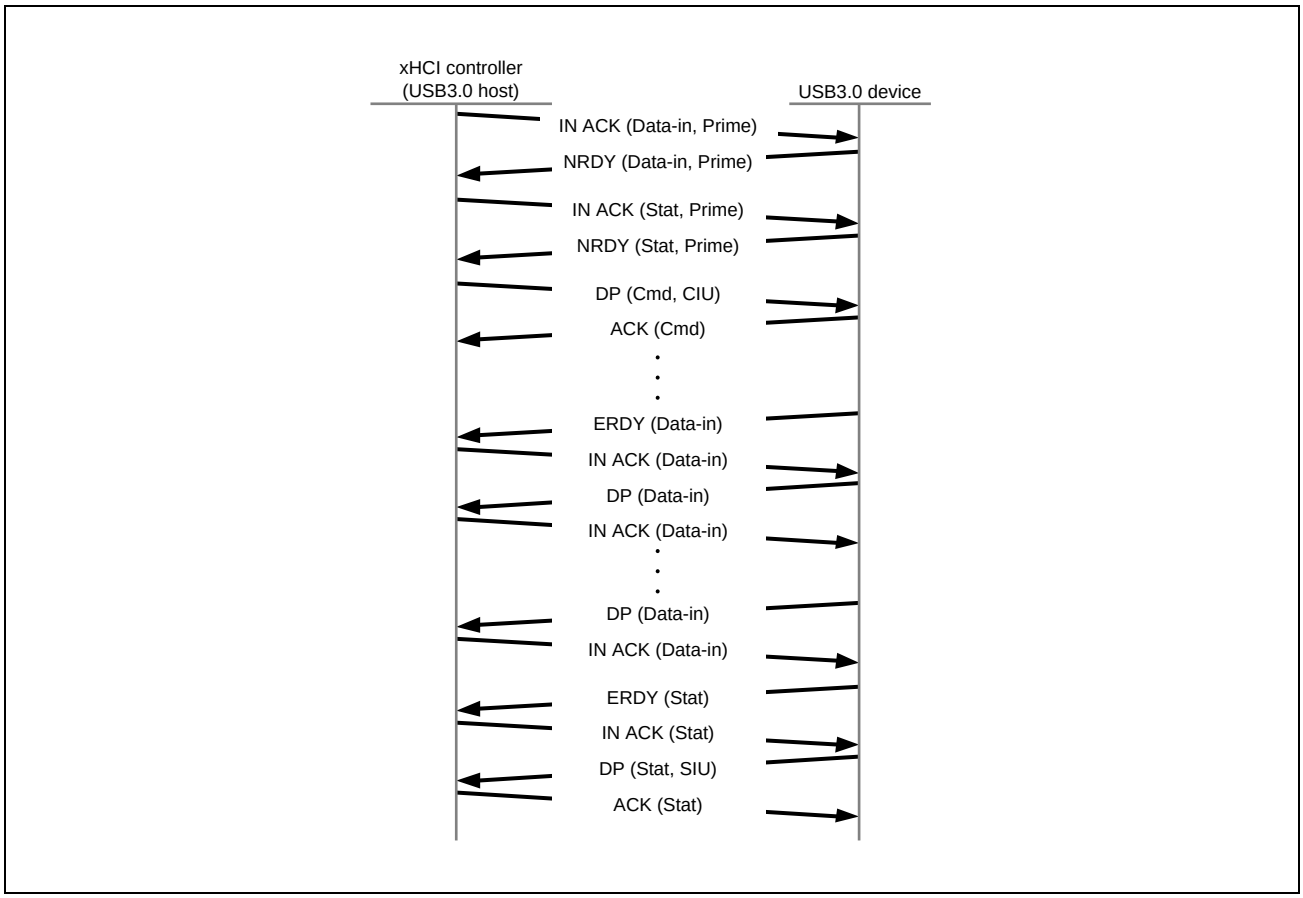


Figure 35.6-35 Example SuperSpeed UASP Data-IN Transfer

Figure 35.6-35 shows the part between USB3.1 host and USB3.1 device of Figure 7 in UASP specification Rev.1.0.

In this case, the Data-in PIPE and the status PIPE are working as Stream bulk IN PIPE.

To set each PIPE in Prime Pipe state, IN ACK(Data-in, Prime) and IN ACK(Stat, Prime) comes. Both PIPEs return NRDY(Prime) to them and go back to Idle state.

The bulk IN operation is requested on DP(Cmd, CIU) to the command PIPE. The command ID in CIU is used as Stream ID later.

If Pn_CON.Pn_RES[1:0] of the Data-in PIPE is already set to 01b (normal response), the Data-in PIPE sends ERDY(Data-in) when IN data becomes ready to be transmitted from it. The data transfer from the Data-in PIPE is started by receiving IN ACK(Data-in).

All data transfers from Data-in PIPE are completed, SIU is made as the result of the operation.

If Pn_CON.Pn_RES[1:0] of the status PIPE is already set to 01b (normal response), the status PIPE sends ERDY(Stat) when SIU is written to buffer and is ready to be transmitted from it. The SIU is sent as DP(Stat, SIU) when IN ACK(Stat) comes.

(6) SuperSpeed UASP Data-OUT Transfer

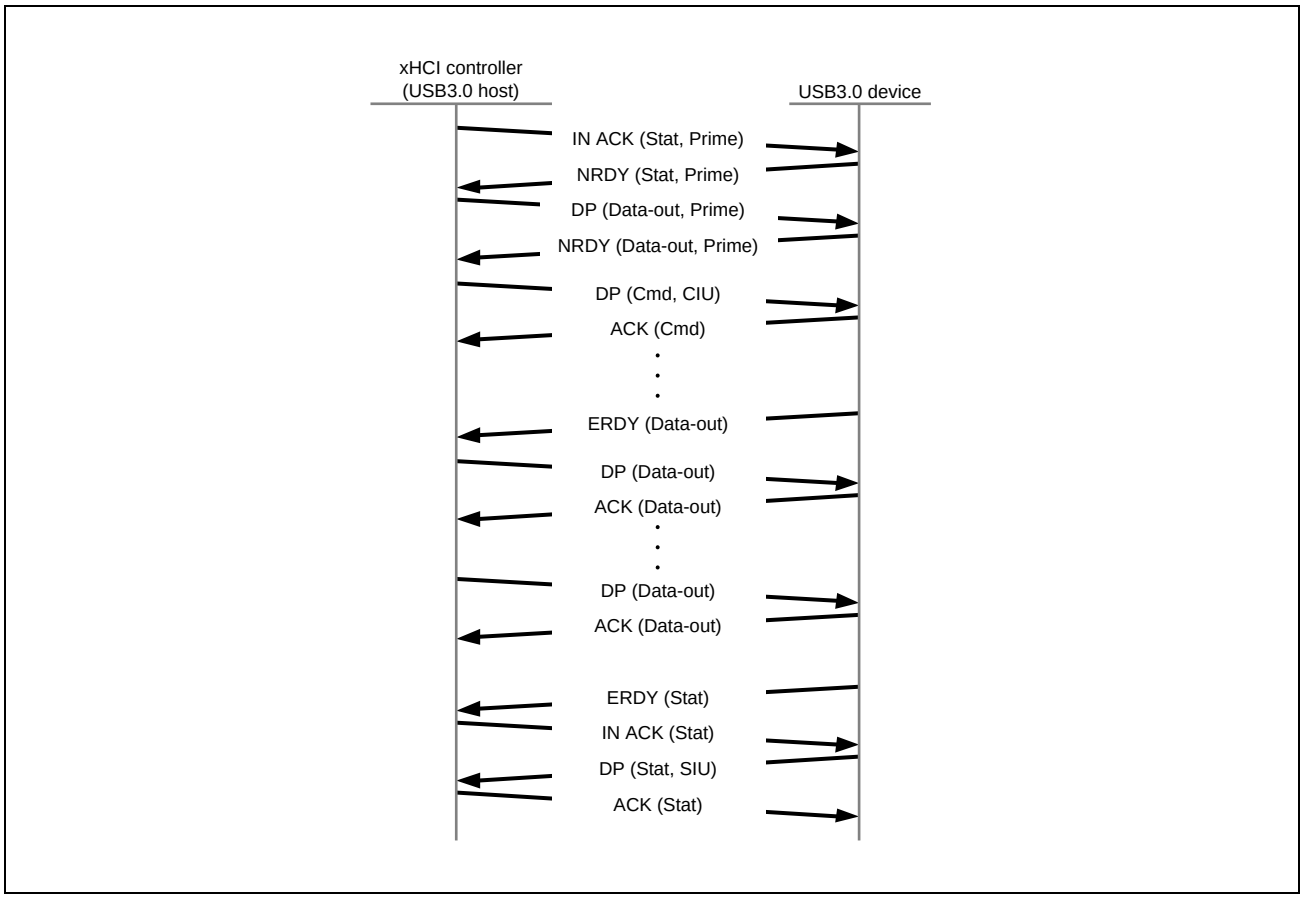


Figure 35.6-36 Example SuperSpeed UASP Data-OUT Transfer

Figure 35.6-36 shows the part between USB3.1 host and USB3.1 device of Figure 8 in UASP specification Rev.1.0.

In this case, the status PIPE is working as Stream bulk IN PIPE, and the Data-OUT PIPE is working as Stream bulk OUT PIPE.

To set each PIPE in Prime Pipe state, IN ACK(Stat, Prime) and DP(Data-out, Prime) comes. Both PIPEs return NRDY(Prime) to them and go back to Idle state.

The bulk IN operation is requested on DP(Cmd, CIU) to the command PIPE. The command ID in CIU is used as Stream ID later.

When Pn_CON.Pn_RES[1:0] of the Data-out PIPE is changed from 00b to 01b (normal response, note that Pn_CON.Pn_RES[1:0] is set to 00b once for Stream bulk PIPE when it receives DP(Prime) or ACK(Prime)), the Data-out PIPE sends ERDY(Data-out) if it has available space in buffer. The data transfer to the Data-out PIPE is started.

All data transfers to Data-out PIPE are completed, SIU is made as the result of the operation.

If Pn_CON.Pn_RES[1:0] of the status PIPE is already set to 01b (normal response), the status PIPE sends ERDY(Stat) when SIU is written to buffer and is ready to be transmitted from it. The SIU is sent as DP(Stat, SIU) when IN ACK(Stat) comes.

35.6.5.6 Interrupt Transfer

Interrupt Transfer process is described here.

PIPEs other than PIPE0 (PIPE0 is used only for control transfer) can be used for interrupt transfer. The settings for interrupt transfer are shown below.

- PIPE_COM.PIPE_NUM[4:0] = the index of PIPE used for the current interrupt transfer
- Pn_MOD.Pn_EPNUM[3:0] = the endpoint number of the PIPE
- Pn_MOD.Pn_TYPE[1:0] = 11b (interrupt transfer)
- Pn_MOD.Pn_DIR = the direction of transfer
- Pn_RAMMAP.Pn_BASEAD[13:0] = the base address of buffer assigned for the PIPE
- Pn_RAMMAP.Pn_RAMIF[1:0] = the index of RAM interface of the PIPE
- Pn_RAMMAP.Pn_MPKT[10:0] = the max packet size of the PIPE
- Pn_RAMMAP.Pn_RAMAREA = the size of RAM area assigned for the PIPE
- Pn_CON.Pn_DATAIF_EN = whether Data Interface of EPC or AXI-IF is used or not.
- Pn_CON.Pn_EN = 1 (the PIPE is enabled)

These settings are done just after Set Configuration is completed and the device enters configured state. But if the device has only single configuration for each PIPE, these settings can be done after the device is turned on.

(1) Interrupt IN Transfer

In this subsection it is assumed that interrupt transfer is used to return small data periodically, so the process to write through Pn_WRITE register is described here.

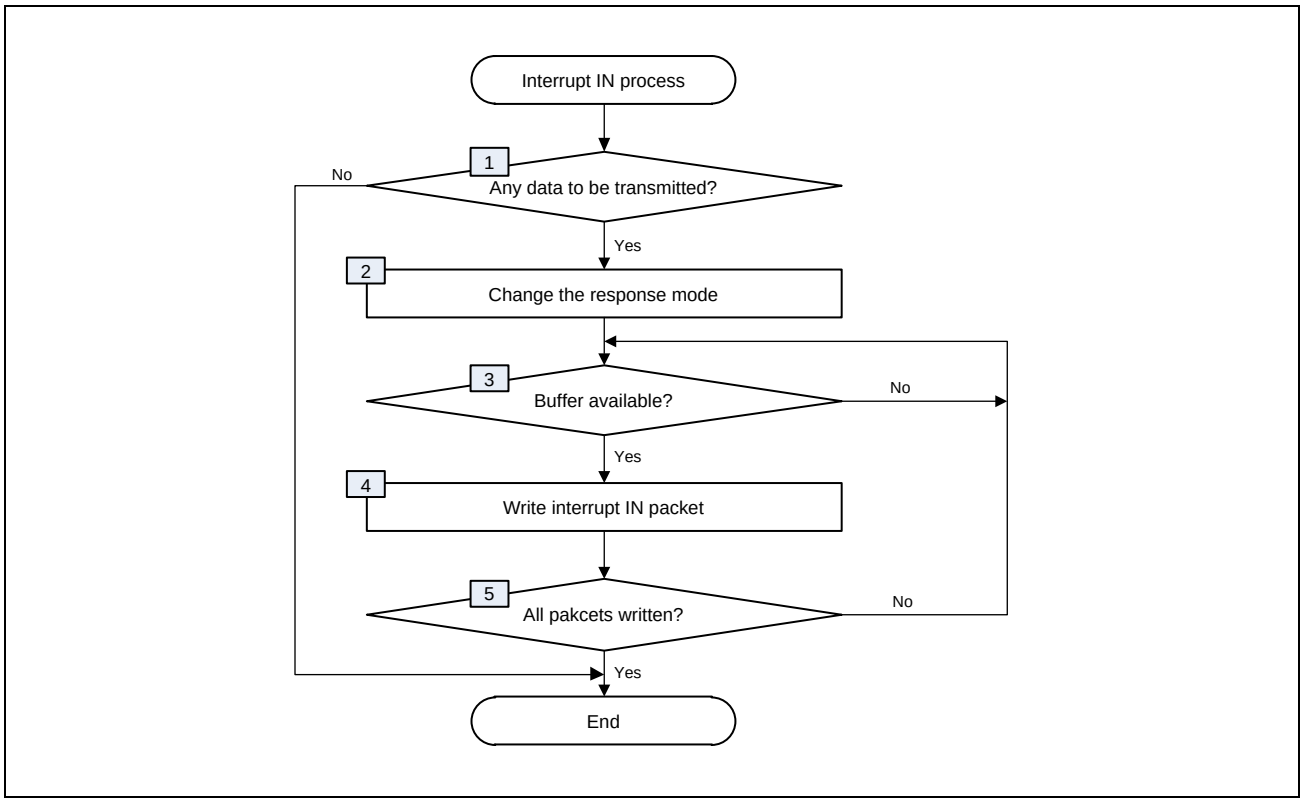


Figure 35.6-37 Interrupt IN Process Flow

(1) Is there any data to be transmitted?
Check if there is any data to be transmitted from interrupt IN PIPE.
If not, set Pn_CON.Pn_RES[1:0] = 00b so that the PIPE returns NRDY or NAK for IN request. When Pn_CON.Pn_RES[1:0] already has the value, leave it as it is.

- Pn_CON.Pn_RES_WEN = 1
- Pn_CON.Pn_RES[1:0] = 00b (NRDY/NAK response)

If there is, proceed to (2).

(2) Change the response mode of the interrupt IN PIPE
As it is confirmed that there is data to be transmitted at (1), change the response mode of the interrupt IN PIPE to enable the transmission of a packet.

- Pn_CON.Pn_RES_WEN = 1
- Pn_CON.Pn_RES[1:0] = 01b (normal response)

(3) Check if buffer is available
Check if buffer for the interrupt IN PIPE is available before writing interrupt IN packet. Pn_STA.Pn_BUFSTS shows if the buffer is available or not.

- Check whether Pn_STA.Pn_BUFSTS = 1 or not

If Pn_STA.Pn_BUFSTS is 0 and there is no available space in the buffer currently, wait until Pn_STA.Pn_BUFSTS becomes 1 or an interrupt due to Pn_INT_STA.Pn_BFRDY_STA is asserted. When IN is selected as the direction of the interrupt PIPE (that is, Pn_MOD.Pn_DIR = 1), Pn_INT_STA.Pn_BFRDY_STA is asserted when the buffer for the PIPE becomes available for new write data.
Therefore, the software can know the timing the buffer of the PIPE prepares new available space by polling Pn_STA.Pn_BUFSTS or an interrupt due to Pn_INT_STA.Pn_BFRDY_STA.

(4) Write interrupt IN packet
Write interrupt IN packet to be transmitted to the buffer. Interrupt IN data is written in a unit of packet and the buffer cannot accept data across the max packet size defined in Pn_RAMMAP.Pn_MPKT[10:0].

[writing through Pn_WRITE register]

a-1) Write data through Pn_WRITE register. Since only 32-bit access is allowed to the register, data should be written in a unit of 32-bit. The number of write can be calculated as the number of write = the length divided by 4, round-up is required if there is any residue. The written words are concatenated as one packet.
When the length of packet is not multiples of 32-bit, the last written word has unnecessary bytes.
The last word should be also written as a 32-bit word. The number of valid bytes in the last word is set in Pn_CON.Pn_BYTE_EN[1:0]. Unnecessary bytes in the last word are discarded.

a-2) Set fields as follows to send the packet. Since only 32-bit access is allowed to Pn_CON register, all fields below should be set in one word access.

- Pn_CON.Pn_SEND = 1
- Pn_CON.Pn_BYTE_EN[1:0] = xxb (The number of valid byes in last written word)
- In case of the last packet of data group, set Pn_CON.Pn_LAST = 1.

NOTE

Zero length packet will be sent if Pn_CON.Pn_SEND is set to 1 after Pn_WRITE register is written nothing in the above. In this case, Pn_CON.Pn_BYTE_EN[1:0] is ignored (it's usually set “00” at the same time Pn_SEND is set).

See **Section 35.6.4.6, Zero Length Packet (ZLP)** about zero length packet.

(5) Are all packets written?
If it is required to send two or more packets, repeat the steps from (3) to (4).

NOTE

When the information of a certain PIPE is read from or write to PIPEn registers, PIPE_COM.PIPE_NUM[4:0] should have the index of the PIPE.

35.6.5.7 DMA Transfer

(1) Settings for DMA Transfer

Data transfer using DMA in AXI-IF is described here.

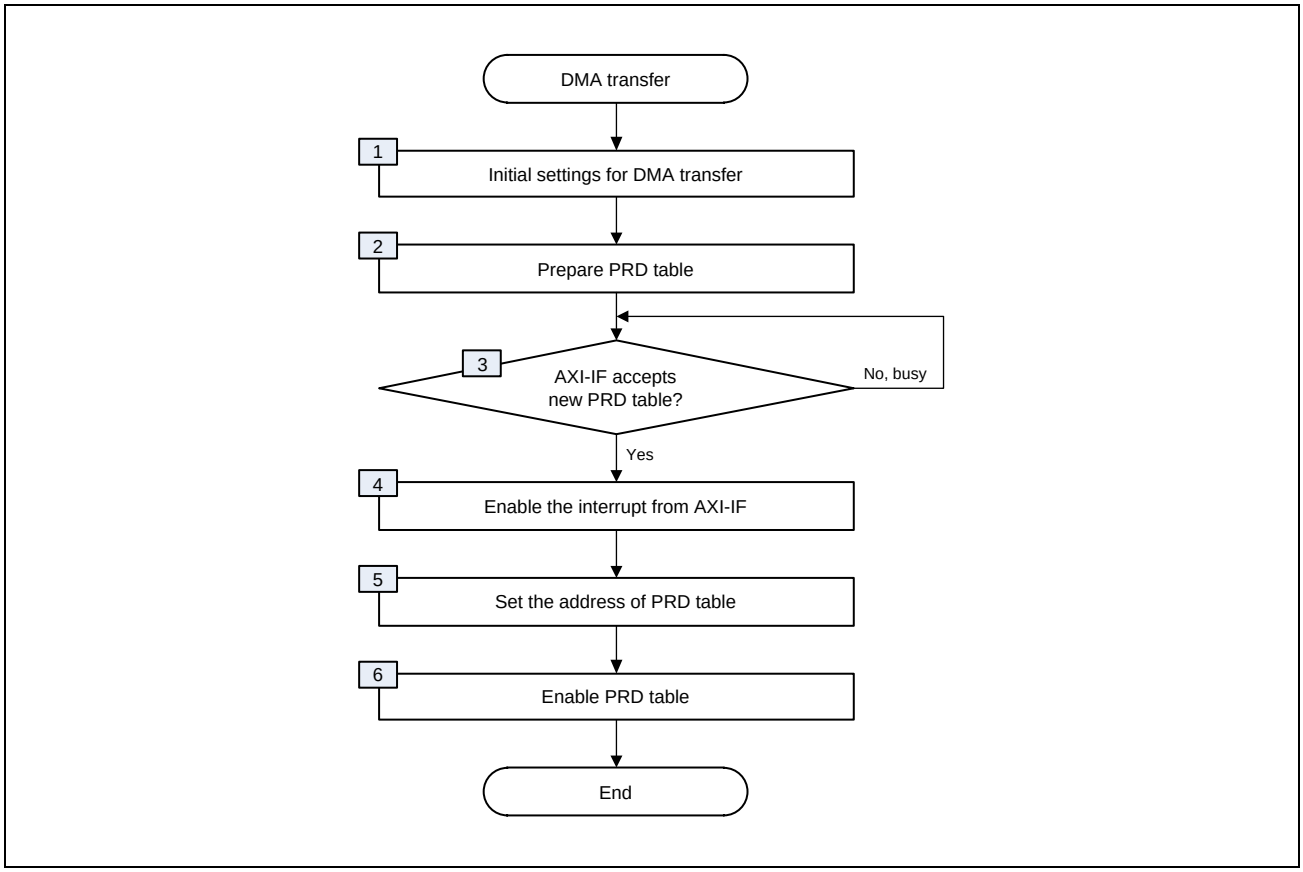


Figure 35.6-38 Transfer Setting Flow

(1) Initial settings for DMA transfer
Change the DMA transfers suspended to normal operation.
Since AXI-IF uses EPC_D_Pn_DATAEN[30:1] to see if the PIPE is ready for the transfer or not, Pn_CON.Pn_DATAIF_EN should be enabled.

- AXI_CON.MST_WAIT0 = 0
- Pn_CON.Pn_DATAIF_EN = 1

(2) Prepare PRD table
Prepare PRD table in system memory following the format defined in **Section 35.6.3.2, Physical Region Descriptor (PRD) Table**.

(3) Can AXI-IF accept new PRD table?
AXI-IF handles up to 4 PRD tables concurrently. If the number of PRD tables running in AXI-IF is less than 4, new PRD table can be set for AXI-IF. The “PRD table running” means here that PRD table is assigned to one of DMA_Ch0_PRD_ADRx register and DMA_Ch0_CONx.PRD_ENx is enabled for it.
If there is any DMA_Ch0_CONx in which PRD_ENx is disabled (= 0), new transfer can be assigned to it.
If there is no DMA_Ch0_CONx with PRD_ENx = 0, wait for the completion of one of PRD tables running.

(4) Enable interrupt from AXI-IF

Enable the assertion of an interrupt from AXI-IF if it is disabled, and clear the interrupt status registers. But the status register might have the interrupt status of completed transfer, and it is also possible that the concurrent transfer is finished and set its status in registers just when the software clears them for new transfer. Make sure not to clear statuses of other PIPE or other DMA_Ch0_CONx when clearing the status of PIPE and DMA_Ch0_CONx to be used. The bits in status register have “write 1 to clear” function, which means it is not cleared when writing 0. Write 1 just to the bit to be cleared.

- DMA_INT_STA.Pxx_DMACNG_STA = 1 (The status of the PIPE to be used is cleared)
- AXI_INT_STA.PRDENx_CLR_STA = 1 (The status of DMA_Ch0_CONx to be used is cleared)
- AXI_INT_STA.PRDERR0_x_STA = 1 (The error status of DMA_Ch0_CONx to be used is cleared)

After clearing the interrupt status, enable the interrupt for the PIPE and DMA_Ch0_CONx to be used.

- AXI_INT_ENA.DMA_INT_ENA = 1
- AXI_INT_ENA.PRDENx_CLR_ENA = 1
- AXI_INT_ENA.PRDERR0_x_STA = 1

(5) Set the address of PRD table

Set the address of PRD table generated at (2) in DMA_Ch0_PRD_ADRx register. If the transfer consists of some PRD tables, set the address of the first PRD table.

- DMA_Ch0_PRD_ADRx = the address of PRD table

(6) Enable PRD table

Set the information of PRD table to DMA_Ch0_CONx register, and enable it on DMA_CH0_CONx.PRD_ENx. The fields below can be set in one word access.

- DMA_CH0_CONx.PIPE_DIRx = the direction of the PIPE
- DMA_CH0_CONx.PIPE_NOx = the index of the PIPE
- DMA_CH0_CONx.PRD_ENx = 1

In case the transfer of new PRD table is expected to wait for the completion of one of the concurrent transfer and be executed after it, use DMA_CH0_CONx.EXTPRD_ENx. See **Section 35.6.4.4, AXI DMA Transfer Control** for details of DMA_CH0_CONx.EXTPRD_ENx.

- DMA_CH0_CONx.EXTPRD_NOx = the index of DMA_CH0_CONy which completion of transfer new PRD table is waiting for.
- DMA_CH0_CONx.EXTPRD_ENx = 1 (the use of EXTPRD_EN is enabled)

Note that EXTPRD_ENx is not cleared if PRD_ENy of DMA_CH0_CONy which completion is waited for is already 0. That is, EXTPRD_ENx cannot be used for DMA_CH0_CONy which has already cleared its enable bit (PRD_ENy). Make sure that PRD_ENy is still 1 and the related transfer is still being executed when EXTPRD_EN is associated. When PRD_ENy is already cleared to 0, do not use EXTPRD_EN. In that case, there is no need to wait for the completion of DMA_CH0_CONy since it has already been finished.

(2) Transfer Stop Process

Process to stop PRD Table that has Transfer process enabled is described in this section.

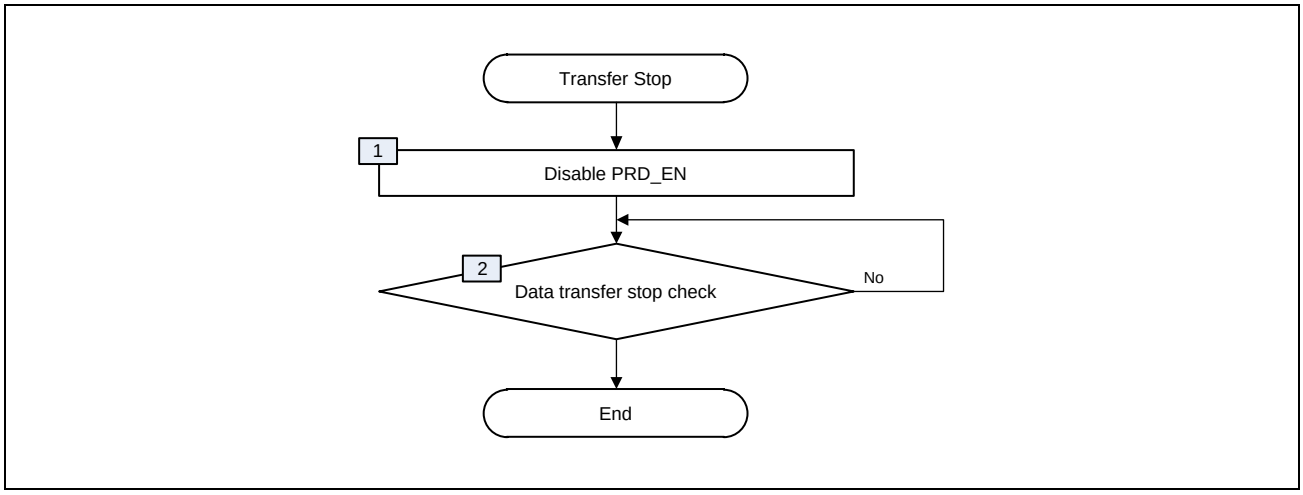


Figure 35.6-39 Transfer Stop Flow

(1) Disable PRD_EN
Set PRD Table to have Transfer Process suspended to “Stop DMA Transfer.”
Below is for the case to stop Transfer with PRD Table that was set in DMA_CH0_CONx

- DMA_CH0_CONx.PRD_ENx = 0b (Set to Stop DMA Transfer)

(2) Data transfer stop check
Wait the Transfer with the PRD Table that was requested to be stopped in (1) is stopped completely.
Number of PIPE being transferred can be checked by referencing a register provided below. Wait for the applicable status is cleared in case the register indicates Transfer in progress at the PIPE stop was requested in (1) Transfer.

- AXI_STA.DMA_TRANS0 = 0b (Stand-by)

or

- AXI_STA.DMA_PIPE0 = xxh (Other PIPEs than requested for stop shall be selected.)

Setting for PRD Table can be rewritten after it is confirmed that the applicable PRD Table is not in use.

35.6.5.8 Power Management

(1) Suspend in USB3.1 (Transition of State from U0 to U3)

The process to transit to U3 state of LTSSM in USB3.1 specification is described here.

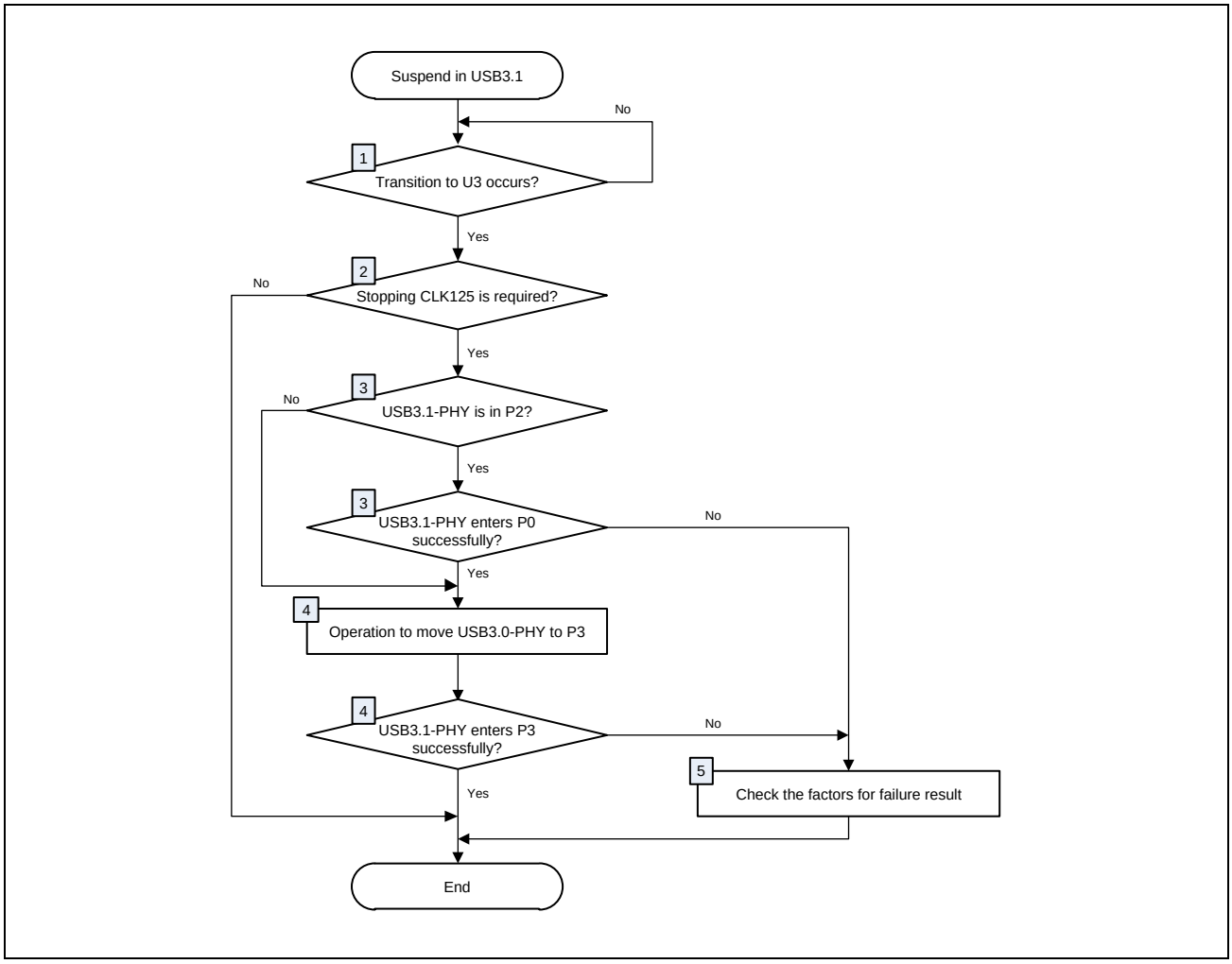


Figure 35.6-40 Suspend in USB3.1 Flow

(1) Transition to U3 is informed

It is defined that only a downstream port (host or hub) can initiated U3 entry and an upstream port cannot reject it in USB3.1 specification. The downstream port initiates U3 entry by sending LGO_U3.

When EPC receives LGO_U3, it accepts it and executes the transition to U3 inside. At this time, USB_INT_STA_1.B3_LNKCNG_STA is asserted since the change of the link status occurs. The current status of LTSSM can be known by seeing PORTSC.PLS[3:0].

Check whether the transition to U3 is requested or not when LTSSM is in U0 state and USB_INT_STA_1.B3_LNKCNG_STA is asserted. If LTSSM has changed to U3 state, the transition to U3 has been requested from downstream port.

- Interrupt due to USB_INT_STA_1.B3_LNKCNG_STA is generated
- Check whether PORTSC.PLS[3:0] shows U3 or not.

Note that there is another possibility that a disconnection or error occurs as the factor of the change of the link status. In such case, follow the flows noted in other sections.

After confirming the factor of the change, clear USB_INT_STA_1.B3_LNKCNG_STA. Then, proceed to (2).

- USB_INT_STA_1.B3_LNKCNG_STA = 1 (Clearing the event that the link has changed)

(2) Is stopping USB3.1-PHY clock required?
LTSSM in EPC has transited to U3 at (1), but USB3.1-PHY is in P0 or P2 state of USB3.1-PHY state since only P0 or P2 can be selected as the setting of USB30_CON.U3_POW_SEL[1:0]. Note the difference between U0/U1/U2/U3 and P0/P1/P2/P3. Ux is the power management states in LTSSM. Px is the power management states for USB3.1-PHY and the upper layer. USB30_CON.U3_POW_SEL[1:0] defines the PHY state in which USB3.1-PHY is placed when the transition to U3 is requested in LTSSM. P3 is defined as the state in which the clock is suspended. The reason why P3 is not selected as the setting of USB30_CON.U3_POW_SEL[1:0] is that it may cause issues if the clock from USB3.1-PHY is stopped suddenly.

If USB3.1-PHY is not required to be placed in P3 when the upper layer is in U3 state, no additional operation is required here. If it is required, proceed to (3).

(3) Is USB3.1-PHY placed in P2?
As noted above, P0 or P2 can be selected as USB3.1-PHY state on USB30_CON.U3_POW_SEL[1:0] when LTSSM of upper layer enters U3. If USB3.1-PHY is in P2 at present and expected to enter P3, it should be move to P0 once before it is operated to enter P3.

- USB30_CON.POW_SEL_WEN = 1
- USB30_CON.POW_SEL[2:0] = 110b (the transition from P2 to P0 is requested when LTSSM is in U3)

When the transition to P0 requested has been done, an interrupt due to the transition is asserted. Since there is no reason to fail in the transition, so USB3.1-PHY surely enters P0, but confirm the result of the transition.

- Interrupt due to the transition asserted
- Check whether USB_INT_STA_1.B3_PSSUCS_STA is asserted or not. If it is asserted, the transition has been done successfully. Clear it after the confirmation.
- If USB_INT_STA_1.B3_PSSUCS_STA is not asserted, check whether USB_INT_STA_1.B3_PSFAIL_STA is asserted or not. If it is asserted, the presumed factors are explained at (5).

If USB30_CON.U3_POW_SEL[1:0] = 00b (P0) and USB3.1-PHY is placed in P0 when LTSSM enters U3, this operation is not required.

Hence, USB3.1-PHY is P0 at present.

(4) Operation to move USB3.1-PHY to P3
Set USB30_CON.POWSEL[2:0] to place USB3.1-PHY in P3.

- USB30_CON.POW_SEL_WEN = 1
- USB30_CON.POWSEL[2:0] = 101b (the transition from P0 to P3 is requested when LTSSM is in U3)

When the transition to P3 requested has been done, an interrupt due to the transition is asserted. Since there is no reason to fail in the transition, so USB3.1-PHY surely enters P3, but confirm the result of the transition.

- Interrupt due to the transition asserted
- Check whether USB_INT_STA_1.B3_PSSUCS_STA is asserted or not. If it is asserted, the transition has been done successfully. Clear it after the confirmation.
- If USB_INT_STA_1.B3_PSSUCS_STA is not asserted, check whether USB_INT_STA_1.B3_PSFAIL_STA is asserted or not. If it is asserted, the presumed factors are explained at (5).

(5) Check the factors for failure result

If case the transition of power state noted here failed, the presumed factors are as follows.
(1) the disconnection has occurred and LTSSM transits to SS.Disabled.
(2) U3Wakeup LFPS from host has come and LTSSM has started the transition to U0.
(3) the warm reset from host has come

See the statuses below to know whether the factors above occur or not.

- USB_INT_STA_1.B3_DISABLE_STA = 1 (if (1) occurred)
- PORTSC.PLS[3:0] = 0h (if (2) occurred)
- USB_INT_STA_1.B3_WRMRST_STA = 1 (if (3) occurred)

If (1) occurs, see **Section 35.6.5.3(3), USB Disconnection** for the disconnection process.
If (2) occurs, see **Section 35.6.5.3(2), USB Connection** for the resume process from U3.
If (3) occurs, see **Section 35.6.5.3(4), Warm Reset Process** for the warm reset process.

In case the transition of power state failed but the factors above has not caused it, fatal error might occur in the system.

(2) Resume in USB3.1 (from U3 to U0: Initiated by Host)

The process for the transition to U0 initiated by host in USB3.1 is described here.

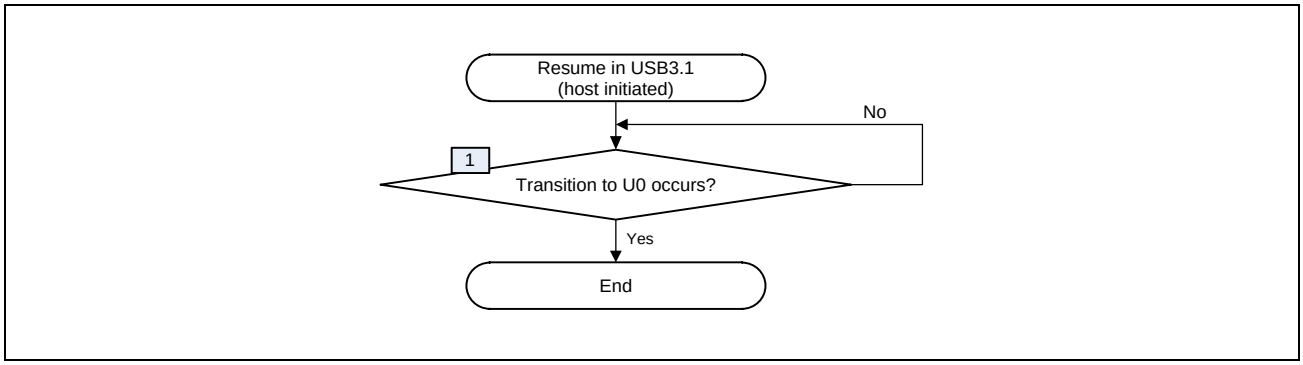


Figure 35.6-41 Resume in USB3.1 (Host Initiated) Flow

(1) Does the transition to U0 occur?

In case EPC is in U3 and receives U3Wakeup LFPS from host, it automatically responds to the LFPS and go back to U0. At this time, USB3.1-PHY is moved back to P0 as well.

The event is notified on the assertion of USB_INT_STA_1.B3_LNKCNG_STA. An interrupt due to the bit is asserted if enabled.

- Interrupt due to USB_INT_STA_1.B3_LNKCNG_STA is asserted, if enabled
- Check that USB_INT_STA_1.B3_LNKCNG_STA = 1
- Check that PORTSC.PLS[3:0] shows U0 (= 0h)

After the confirmation above, clear USB_INT_STA_1.B3_LNKCNG_STA.

- USB_INT_STA_1.B3_LNKCNG_STA = 1 (clearing the event of the link change)

If USB3.1-PHY is placed in P3 following the flow in **Section 35.6.5.8(1), Suspend in USB3.1 (Transition of State from U0 to U3)** and the clock from it is stopped in U3, the clock is also resumed as USB3.1-PHY goes back to P0. USB_INT_STA_1.B3_PLLWKUP_STA is asserted in that case. If it is asserted, clear it.

- USB_INT_STA_1.B3_PLLWKUP_STA = 1 (clearing the event of USB3.1 PLL Wakeup)

(3) Resume in USB3.1 (from U3 to U0: Initiated by Device)

The process for the transition to U0 initiated by device in USB3.1 is described here.

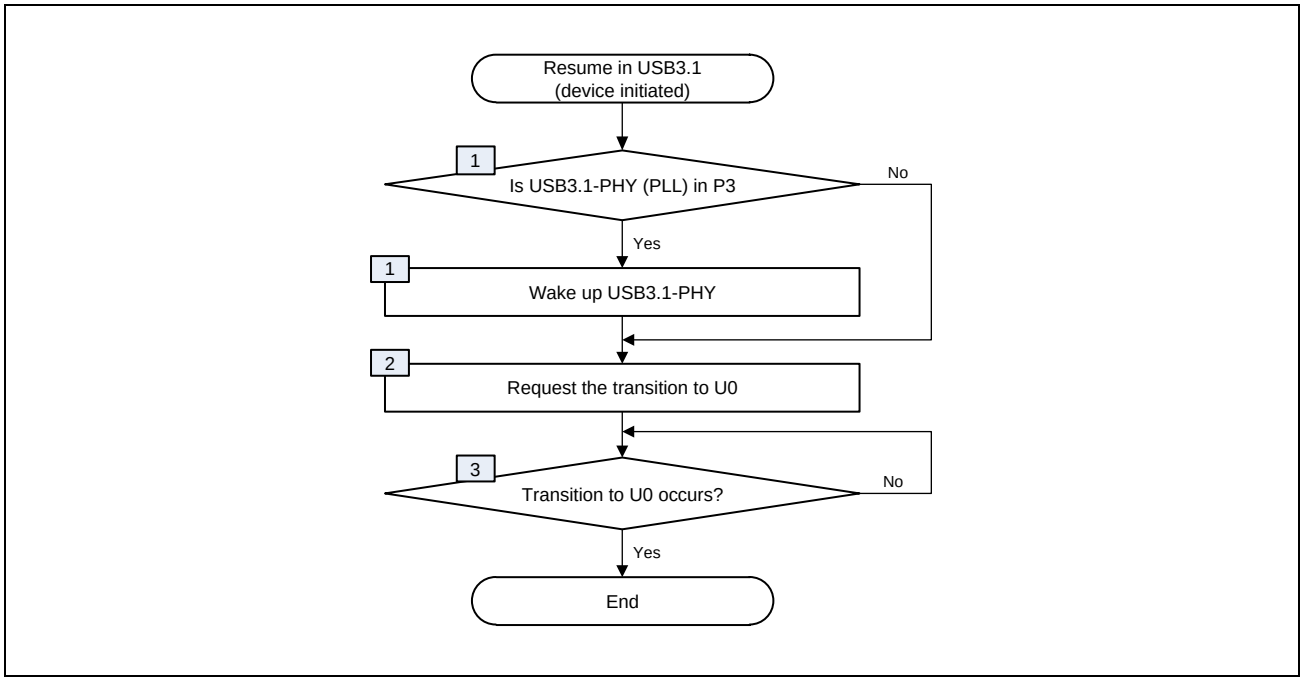


Figure 35.6-42 Resume in USB3.1 (Device Initiated) Flow

(1) Is USB3.1-PHY in P3?
If USB3.1-PHY is placed in P3 following the flow in **Section 35.6.5.8(1), Suspend in USB3.1 (Transition of State from U0 to U3)** and the clock from it is stopped in U3, it is required to wake up USB3.1-PHY since the clock from USB3.1-PHY should be provided for the operations here.
See **Section 35.6.5.8(6), USB3.1-PHY (PLL) Wakeup Process** for the process of wakeup of USB3.1-PHY.

If USB3.1-PHY is P0 or P2 and the clock from it is being provided, it is not required to wake up USB3.1-PHY.

(2) Request the transition to U0
Request the transition to U0 in LTSSM as follows.

- PORTSC.LWS = 1
- PORTSC.PLS[3:0] = 0h (U0 state is requested)

(3) Does the transition to U0 occur?
With the request to transit to U0, EPC asserts U3Wakeup LFPS to host. When host responds to the LFPS and LFPS handshake is established, EPC has transited to U0.
At that time, USB_INT_STA_1.B3_LNKCNG_STA is asserted and an interrupt due to it is caused if enabled.

- Interrupt due to USB_INT_STA_1.B3_LNKCNG_STA is asserted, if enabled
- Check that USB_INT_STA_1.B3_LNKCNG_STA = 1
- Check that PORTSC.PLS[3:0] shows U0 (= 0h)

After the confirmation above, clear USB_INT_STA_1.B3_LNKCNG_STA.

- USB_INT_STA_1.B3_LNKCNG_STA = 1 (Clearing the event of the link change)

(4) Function Suspend

The process for function suspend in USB3.1 is described here.

The function suspend is defined for SuperSpeed device and functions are placed into function suspend on the reception of Set Feature(FUNCTION_SUSPEND). Since function has one or more interfaces, what function is selected to be suspend is recognized by seeing what interface receives the request. If the function has multiple interfaces, the request comes to the first interface of the function.

Note that the specification defines about the function suspend as follows.

- A function may be placed into function suspend independently of other functions within the device.
- A device may be transitioned into device suspend regardless of the function suspend state of any function within the device.
- Function suspend state is retained while in divide suspend and throughout the device suspend entry and exit processes.

The definition of function depends on the specification of device.

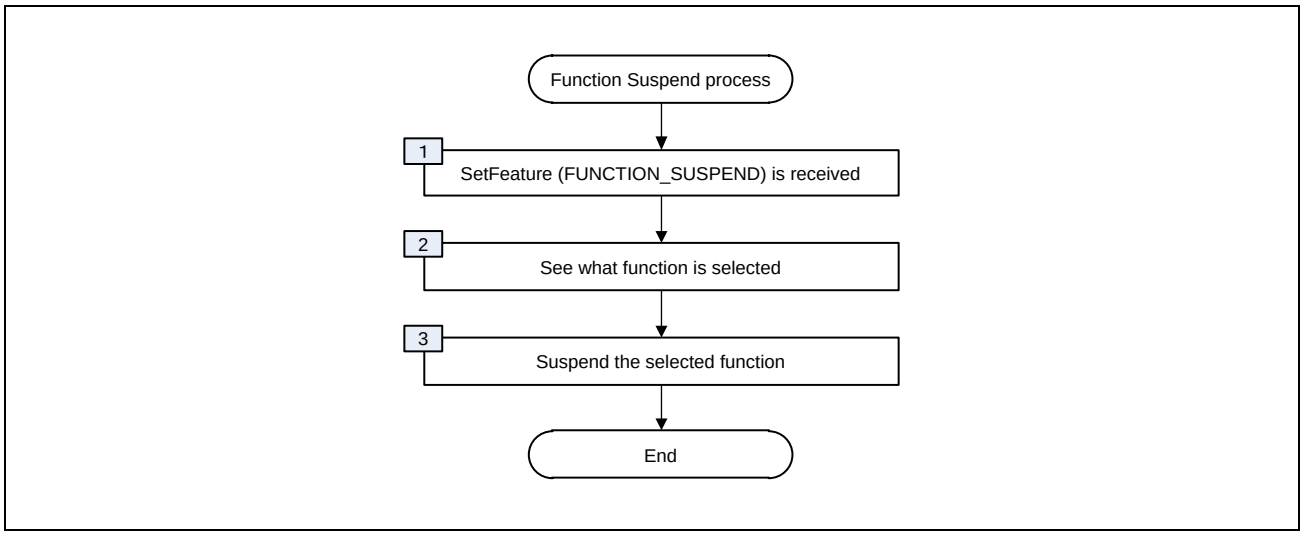


Figure 35.6-43 Function Suspend Process

(1) Set Feature(FUNCTION_SUSPEND) is received
In case Set Feature(FUNCTION_SUSPEND) comes, the function suspend is requested. The function suspend is requested only vie Set Feature(FUNCTION_SUSPEND).

(2) See what function is selected
See what function within the device is selected. The interface number of the function is specified in the lower byte of wIndex. If the function has multiple interfaces, the lower byte of wIndex shall be the first interface of the function.
Bit 0 in the upper byte of wIndex shows which of normal state (= 0) or suspended state (= 1) is requested. When bit 0 is 1 and the function has been enabled, the selected function is requested to suspend. When bit 0 is 0 and the function has been suspended, the selected function is requested to exit from suspended state.
Bit 1 in the upper byte for wIndex shows whether the function remote wakeup is enabled or not.

(3) Suspend the selected function
Suspend the function which is selected at (2).

If the function cannot be suspended, the device may be allowed to return STALL response to Set Feature(FUNCTION_SUSPEND).

(5) Function Remote Wakeup

The process of function remote wakeup is described here.

The function remote wakeup is defined for SS device and DEVICE_REMOTE_WAKEUP is not supported by SuperSpeed device.

As a function may be suspended independently of other functions, the link is still in U0 state even when one or more functions are suspended. In case the suspended function within the device requires to be woken up and the link is U0 state, the device simply sends Function Remote Wakeup Notification. In case the function is requesting the remote wake up but the link is in the low power state (U1, U2 or U3), resume the link to U0 state first and then sends Function Remote Wakeup Notification.

The function shows whether it supports the function remote wakeup or not in the response to Get Status from the interface which belongs to the function.

It is also required that Function Remote Wake is enabled to request the function remote wakeup from the device. Function Remote Wake is disabled (= 0) in the default state and set when Set Feature(FUNCTION_SUSPEND) is received and bit 1 of the upper byte of wIndex in setup data is 1. The current status of Function Remote Wake is shown in the response to GetStatus from the interface which belongs to the function.

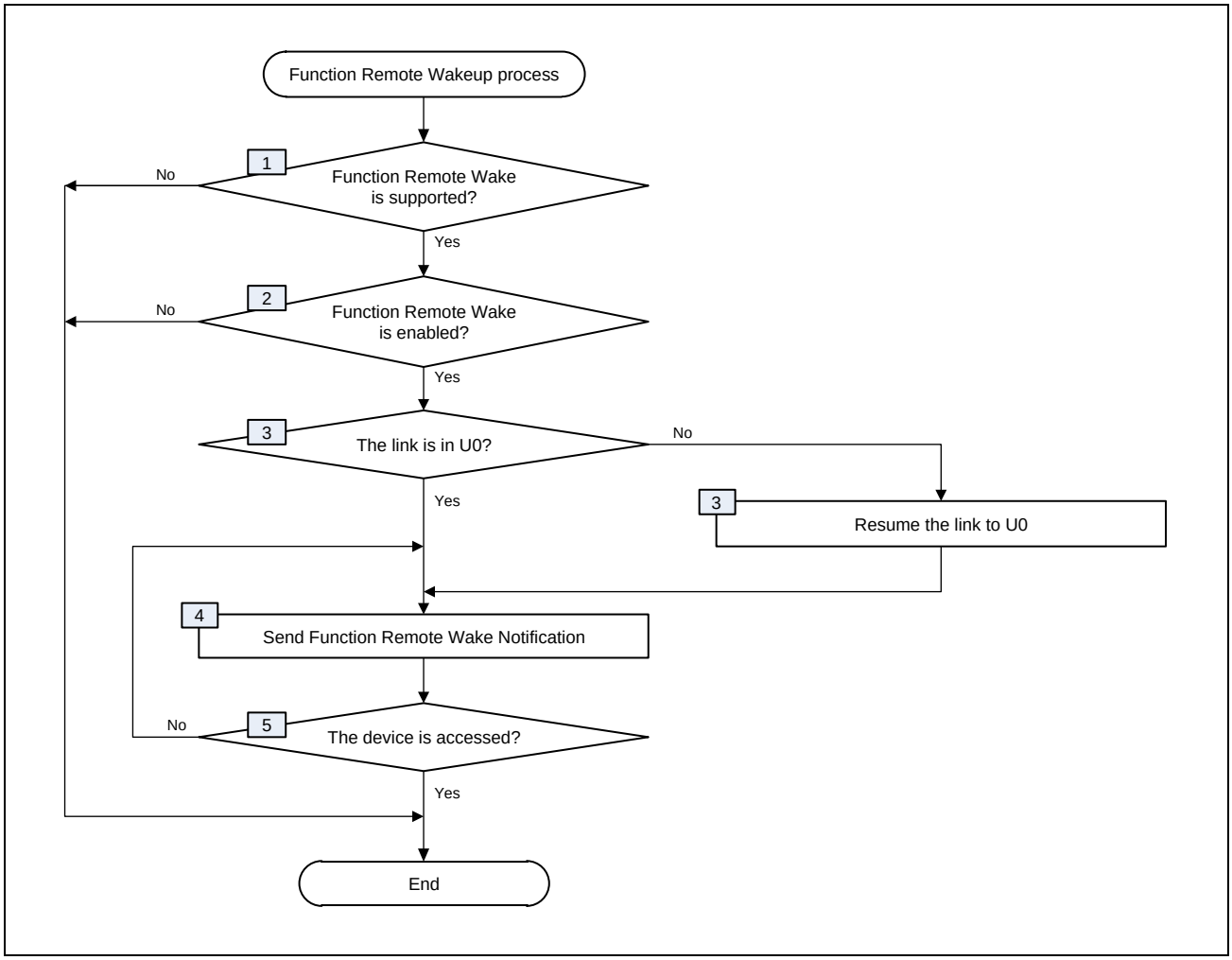


Figure 35.6-44 Function Remote Wakeup Process

(1) Is Function Remote Wake supported?
If the function within the device does not support Function Remote Wake, it cannot request the function remote wakeup. The function shows whether it supports Function Remote Wake or not in the response to Get Status from the interface which belongs to the function. See **Section 35.6.5.9(5), Get Status** for details.

(2) Is Function Remote Wake enabled?
If Function Remote Wake is disabled for the function within the device, it cannot request the function remote wakeup. The current status of Function Remote Wake is shown in the response to Get Status from the interface which belongs to the function. See **Section 35.6.5.9(5), Get Status** for details.

(3) The link is in U0 state?
To send Function Remote Wake Notification, the link is required to be in U0 state.
If USB3PERI is in U1 or U2 state, it automatically goes back to U0 state when Notification written in USB3_TP_DAT_x register is sent. Therefore, the software need not mind the link status except the case the link is U3. Proceed to (4).
If USB3PERI is in U3 state, it is required to exit from the state first. See **Section 35.6.5.8(3), Resume in USB3.1 (from U3 to U0: Initiated by Device)** for the process of resume in USB3.1.

(4) Send Function Remote Wake Notification
If the link is in U0 state, then send Function Remote Wake Notification.

- Write Function Remote Wake Notification to USB3_TPDAT_x registers
- USB30_CON.B3_TP_SEND = 1 (Notification in USB3_TPDAT_x registers is sent)

(5) Is the device accessed?
If tNotification (= 2500 ms) has passed and the device has not been accessed yet from the time Function Remote Wake Notification was sent, it is required to send Function Remote Wake Notification again. The device should send the notification until the function is resumed.
When Set Feature(FUNCTION_SUSPEND) with bit 0 = 1 in the upper byte of wIndex comes, the function is resumed.

(6) USB3.1-PHY (PLL) Wakeup Process

The process to wake up USB3.1-PHY (PLL) in case it is suspended is described here.

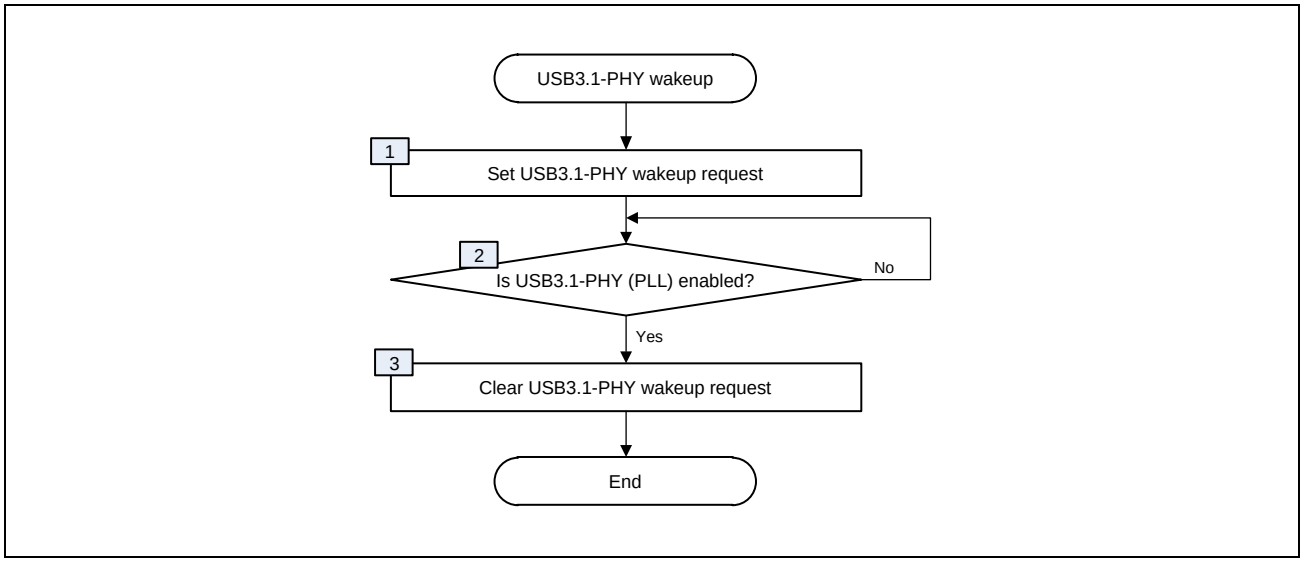


Figure 35.6-45 USB3.1-PHY (PLL) Wakeup Process Flow

(1) Set USB3.1-PHY wakeup request
There are 2 ways to request USB3.1-PHY to wake up.
The first way is to set USB30_CON.B3_PLLWAKE.

[In case register is used]

- USB30_CON.B3_PLLWAKE = 1

(2) Is USB3.1-PHY (PLL) enabled?
Responding to the wake up request at (1), USB3.1-PHY (PLL) becomes enabled.
At that time, USB_INT_STA_1.B3_PLLWKUP_STA is asserted and an interrupt due to it is generated if enabled.

- Interrupt due to USB_INT_STA_1.B3_PLLWKUP_STA is generated
- Check that USB_INT_STA_1.B3_PLLWKUP_STA = 1

After the confirmation above, clear USB_INT_STA_1.B3_PLLWKUP_STA.

- USB_INT_STA_1.B3_PLLWKUP_STA = 1 (Clearing the event of USB3.1 PLL Wakeup)

(3) Clear USB3.1-PHY wakeup request
After the resume of USB3.1-PHY is confirmed at (2), clear USB3.1-PHY wakeup request set in (1).

[In case register is used]

- USB30_CON.B3_PLLWAKE = 0

[In case input signal is used]

- B3_PLL_WAKEIN = 0

(7) Suspend in USB2.0

The process when the state transition to suspend in USB2.0 occurs is described here.

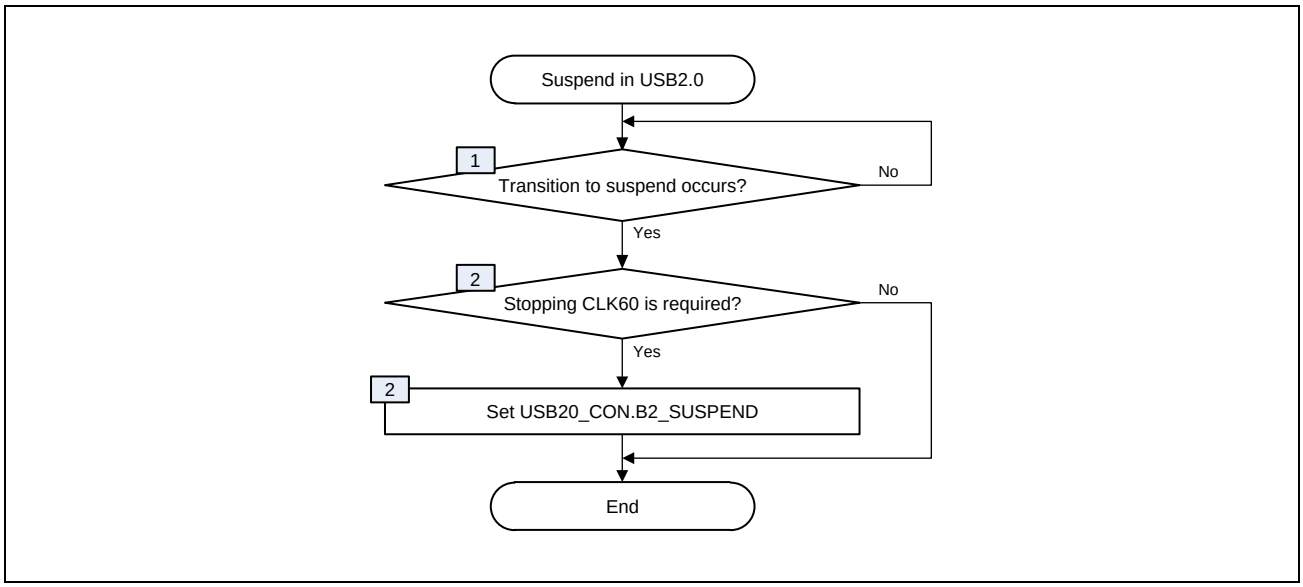


Figure 35.6-46 Suspend in USB2.0 Process Flow

(1) Does the transition to suspend occur?

In USB2.0 (HS/FS) host requests device to make a transition to suspended state by sending no signal to it for a certain period. Device transits to suspended state when it detects constant idle state on USB bus for more than 3.0 ms.

When EPC works as HS or FS device and finds constant idle state on USB bus and make the transition to suspended state, it asserts USB_INT_STA_1.B2_SPND_STA. An interrupt due to it is generated if enabled.

- Interrupt due to USB_INT_STA_1.B2_SPND_STA is generated, if enabled
- Check whether USB_INT_STA_1.B2_SPND_STA = 1 or not.

After the confirmation above, clear USB_INT_STA_1.B2_SPND_STA.

- USB_INT_STA_1.B2_SPND_STA = 1 (Clearing the event of entering USB2.0 suspension)

(2) Is stopping USB2.0-PHY clock required?

PLL in USB2.0-PHY is still running even when EPC enters the suspended state of USB2.0. In order to stop PLL in USB2.0-PHY, set USB20_CON.B2_SUSPEND

- USB20_CON.B2_SUSPEND = 1 (Clock from USB2.0-PHY is stopped)

If it is not required to stop the clock from USB2.0-PHY, no operation is needed here.

(8) Resume in USB2.0 (Initiated by Host)

The process to resume in USB2.0 initiated by host is described here.

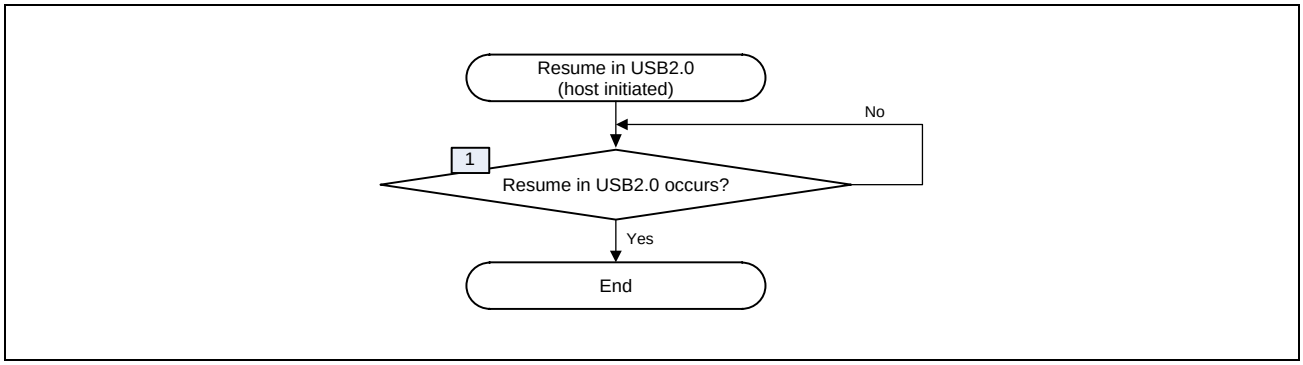


Figure 35.6-47 Resume in USB2.0 (Initiated by Host) Process Flow

(1) Does the resume in USB2.0 occur?

In case EPC is in suspended state and receives the resume signal from host, it responds to it end exits from the suspended state automatically.

At that time EPC asserts USB_INT_STA_1.B2_RSUM_STA or USB_INT_STA_1.B2_L1RSUM_STA depending on the low power state it stayed in. An interrupt due to them is generated if enabled.

- Interrupt due to USB_INT_STA_1.B2_RSUM_STA or USB_INT_STA_1.B2_L1RSUM_STA is generated, if enabled.
- Check whether USB_INT_STA_1.B2_RSUM_STA or USB_INT_STA_1.B2_L1RSUM_STA = 1 or not.

After the confirmation above, clear the status bit asserted.

- USB_INT_STA_1.B2_RSUM_STA = 1 (In case of resume from suspend)
- USB_INT_STA_1.B2_L1RSUM_STA = 1 (In case of resume from sleep)

If USB2.0 PLL is stopped in the suspend state, it is also resumed when EPC exits from the suspend state.

(9) Resume in USB2.0 (Initiated by Device)

The process to resume in USB2.0 initiated by device is described here.

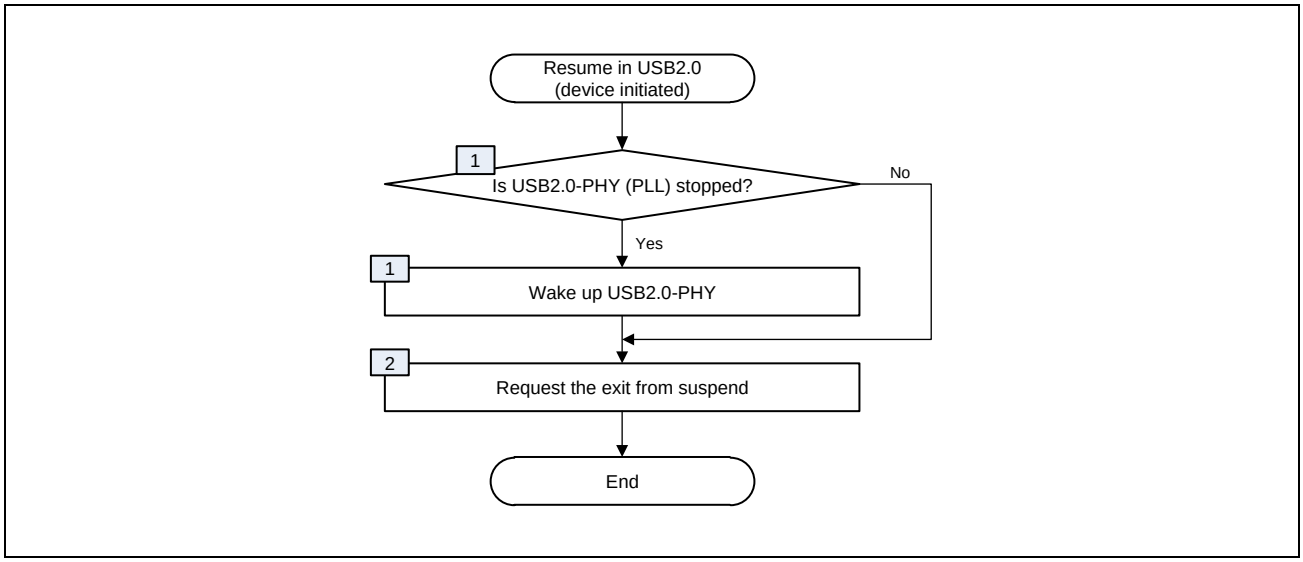


Figure 35.6-48 Resume in USB2.0 (Initiated by Device) Process Flow

(1) Is the clock from USB2.0-PHY stopped?
If the clock from USB2.0-PHY is stopped following the flow in **Section 35.6.5.8(7), Suspend in USB2.0**, it is required to wake up USB2.0-PHY since the clock form USB2.0-PHY should be provided for the operations here.
See **Section 35.6.5.8(10), USB2.0 PHY (PLL) Wakeup Process** for the process to wakeup of USB2.0-PHY.

(2) Request the exit from the suspended state
Request to exit from the suspended state by setting as follows.

- USB20_CON.B2_RSUM_IN = 1 (resume request)

If PLL in USB2.0-PHY is not stopped in suspended state, that is, if USB20_CON.B2_SUSPEND is not set to 1 in suspended state, USB_INT_STA_1.B2_RSUM_STA or USB_INT_STA_1.B2_L1RSUM_STA may be asserted when downstream port responds to the resume request and bus activity comes back.
But, if it is stopped, they are not asserted here because they are asserted when USB20_CON.B2_SUSPEND is cleared so they would have already been asserted at (1).
In either case host should responds to the resume request from the device and bus becomes active again, so the device is required only to wait for the resume of transfer.

(10) USB2.0 PHY (PLL) Wakeup Process

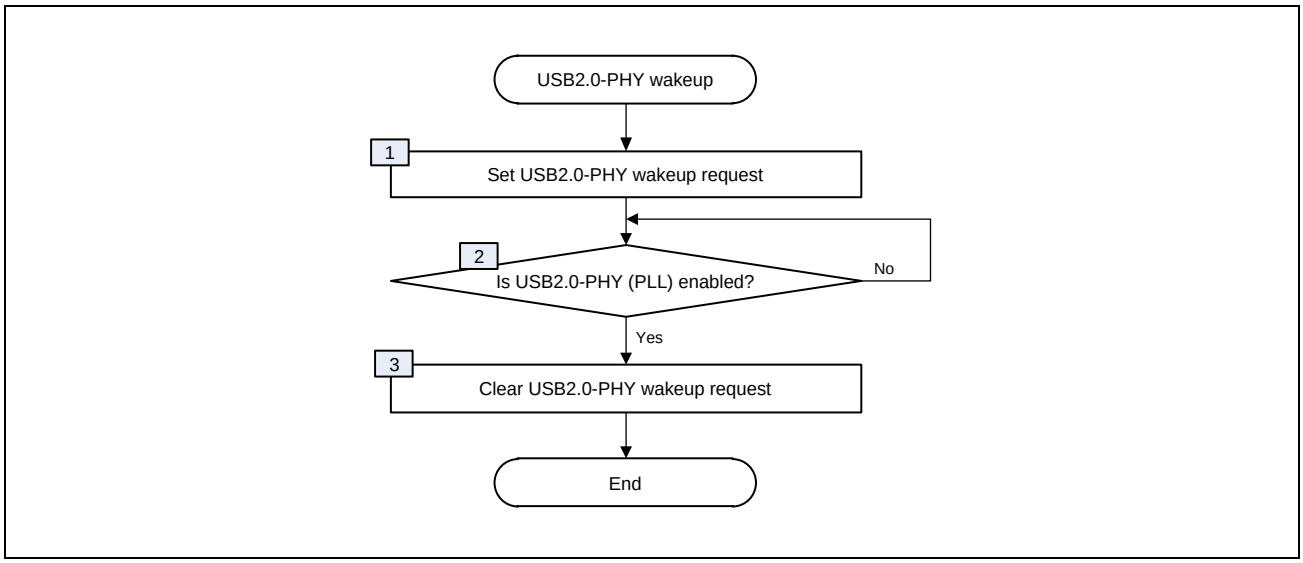


Figure 35.6-49 USB2.0-PHY (PLL) Wakeup Process Flow

(1) Set USB2.0-PHY wakeup request
There are 2 ways to request USB2.0-PHY to wake up.
The first way is to clear USB20_CON.B2_SUSPEND.

[In case register is used]

- USB20_CON.B2_SUSPEND = 0 (Clearing the value set in **Section 35.6.5.8(7), Suspend in USB2.0**)

(2) Is USB2.0-PHY (PLL) enabled?
Responding to the wake up request at (1), USB2.0-PHY (PLL) becomes enabled.
At that time, USB_INT_STA_1.B2_RSUM_STA is generated and an interrupt due to it is caused if enabled.

- Interrupt due to USB_INT_STA_1.B2_RSUM_STA is generated
- Check that USB_INT_STA_1.B2_RSUM_STA = 1

After the confirmation above, clear USB_INT_STA_1.B2_RSUM_STA.

- USB_INT_STA_1.B2_RSUM_STA = 1 (Clearing the event of USB2.0 PLL Wakeup)

If USB3PERI was in L1 state, USB_INT_STA_1.B2_L1RSUM_STA is asserted instead.

(3) Clear USB2.0-PHY wakeup request
After the resume of USB2.0-PHY is confirmed at (2), clear B2_PLL_WAKEIN input signal if used.
If USB20_CON.B2_SUSPEND is used to place USB2.0-PHY in suspended state, USB20_CON.B2_SUSPEND is automatically cleared.

[In case input signal is used]

- B2_PLL_WAKEIN = 0

(11) Process of Transition from U0 to U1/U2 in USB3.1 (Initiated by Device)

With the settings as follows, USB3PERI automatically controls the transition from U0 to U1/U2 by sending LGO_U1/LGO_U2 request or by responding to LGO_U1/LGO_U2 request from host.

- PORTPMSC.U1_TIMEOUT[15:0] = U1 timeout value defined by user
- PORTPMSC.U2_TIMEOUT[15:0] = U2 timeout value in received U2 Inactivity Timeout LMP
- SSIFCMD.SSIF_URES[1:0] = 00b (LAU responses to LGO_U1/LGO_U2 are allowed)
- SSIFCMD.SSIF_UREQ[1:0] = 00b (sending LGO_U1/LGO_U2 by timeout is allowed)

USB3PERI controls the exit from U1/U2 state when it has any available data to be transmitted in buffer or when host requests wakeup as well. No additional operation by the software is required for the cases.

But there might be a case the software requests the transition to U1/U2 state at any point it wants. The process for such case is described here. But note that U1 timeout value can be defined by user, so consider it first to change the value of PORTPMSC.U1_TIMEOUT[15:0] in case LGO_U1 is required to be sent.

The process of Sleep (U1/U2) transition in USB3.1 when the device initiates at any timing is explained. This process flow is for usage when the device initiates LGO_U1/LGO_U2 at any time, and the timer which determine the duration for no data on the bus may be set in PORTPMSC.U1_TIMEOUT. The device can issue LGO_U1 after the timeout of the timer.

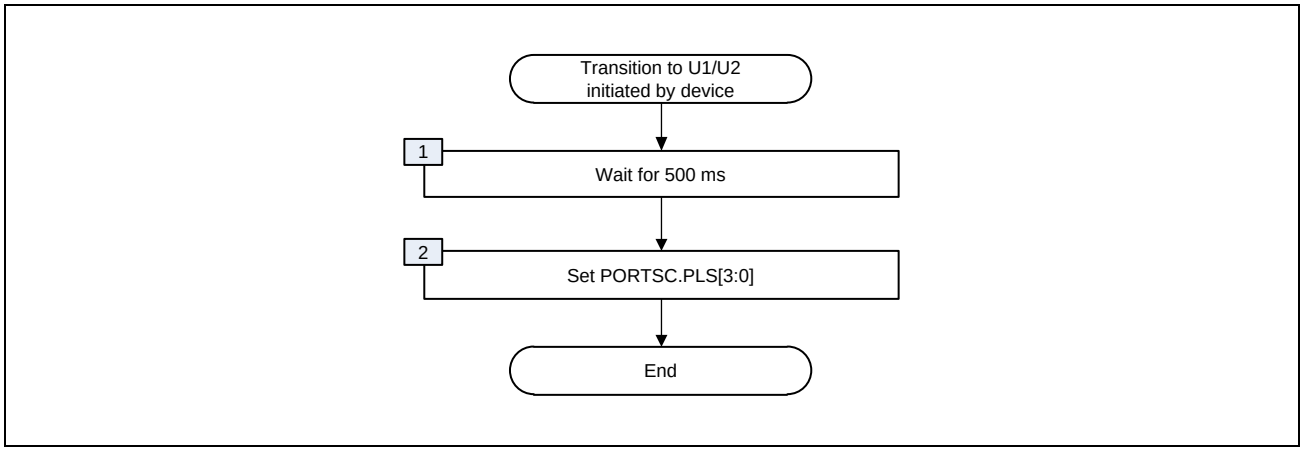


Figure 35.6-50 Transition to U1/U2 (Initiated by Device) Process Flow

(1) Wait for 500 ms

In C.3.2.2 and C3.2.3 of USB3.1 specification, it is defined that the link should be kept in U0 after device has sent ERDY until host sends a request in response to the ERDY or until tERDYtimeout (= 500 ms) occurs.

Since USB3PERI sends ERDY automatically depending on the status of buffer, so it might be difficult to know when it has sent ERDY exactly.

If the software does not assure when the last ERDY has been sent, wait for 500 ms from the point. If no response from host comes, it can request the transition to U1/U2 state. Note that USB3PERI might send ERDY again depending on the process of transfer if the response from host comes before the timeout.

If the software assures when the last ERDY has been sent and 500 ms has passed, it can request the transition to U1/U2 immediately. The triggers to send ERDY for USB3PERI are :

1) IN packet is written to buffer
2) Pn_CON.Pn_RES[1:0] is changed to normal response (= 01b)
3) Buffer for OUT endpoint was full once but becomes available

4) Buffer for OUT endpoint had the last packet of transfer (short packet or packet with PP = 0) but it has been transferred to system memory.

If these triggers has not occurred for 500 ms, it can be said that 500 ms has passed at least from the last ERDY the device has sent.

(2) Set PORTSC.PLS[3:0]

The software can request the transition to U1 or U2 by setting PORTSC.PLS[3:0]. It is also required to set SSIFCMD.SSIF_UDIR[1:0] to enable the function.

- SSIFCMD.SSIF_UDIR[1:0] = 00b (If only one of LGO_U1 or LGO_U2 is requested, unused bit does not require to be enabled.)
- PORTSC.PLS[3:0] = 1h (If the transition to U1 is requested)
  2h (If the transition to U2 is requested)

With the operations above, USB3PERI sends LGO_U1 or LGO_U2 to request the transition to U1 or U2. If host accepts it, the link makes a transition to the low power state.
When LTSSM in USB3PERI enters U1 or U2, USB_INT_STA_1.B3_LNKCNG_STA is asserted. An interrupt due to it is generated if enabled. PORTSC.PLS[3:0] shows the current state of LTSSM.

- Interrupt due to USB_INT_STA_1.B3_LNKCNG_STA is asserted
- Check that USB_INT_STA_1.B3_LNKCNG_STA = 1
- Check that PORTSC.PLS[3:0] shows the requested state (U1 or U2).

Note that PORTSC.PLS[3:0] might show another state if the link transits to U1/U2 but host requests the exit from the state soon.
If host does not accept the request, USB_INT_STA_1.B3_LNKCNG_STA is not asserted. In case the software cannot detect the assertion of the bit even when it waits for a certain time, it should consider the possibility that host rejected the request. The software can send the same request again, but host might intend new transfer, so the software had better the state of USB3PERI in U0 for the moment.

After the confirmation above, write 1 to USB_INT_STA_1.B3_LNKCNG_STA to clear.

- USB_INT_STA_1.B3_LNKCNG_STA = 1 (Clearing the event that the link status is changed)

35.6.5.9 Device Requests

This section describes the operations required for USB device requests.

(1) Clear Feature

This request is used to clear or disable a specific feature.

In case the recipient is device and the device works in SS, U1_ENABLE, U2_ENABLE, LTM_ENABLE and B3_NTF_HOST_REL are defined as feature selectors. But as B3_NTF_HOST_REL is defined for OTG, it is not used for device.

(a) When Clear Feature(U1_ENABLE) comes, disable the initiation of U1 entry of USB3PERI as follows. Note that U1_ENABLE enables or disables only the initiation of U1 entry but the device is still allowed to accept LGO_U1 from downstream port and enters U1 state regardless of the feature.

- SSIFCMD.SSIF_UDIR[0] = 1 (The initiation of LGO_U1 due to direct request is disabled.)
- SSIFCMD.SSIF_UREQ[0] = 1 (The initiation of LGO_U1 due to timeout is disabled.)

(b) When Clear Feature(U2_ENABLE) comes, disable the initiation of U2 entry of USB3PERI as follows. Note that U2_ENABLE enables or disables only the initiation of U2 entry but the device is still allowed to accept LGO_U2 from downstream port and enters U2 state regardless of the feature.

- SSIFCMD.SSIF_UDIR[1] = 1 (The initiation of LGO_U2 due to direct request is disabled.)
- SSIFCMD.SSIF_UREQ[1] = 1 (The initiation of LGO_U2 due to timeout is disabled.)

(c) When Clear Feature(LTM_ENABLE) comes, disable the transmission of LTM (Latency Tolerance Message). Note that SS device must support U1 and U2 features, but LTM feature is optional. SS device shows whether it supports LTM feature or not on LTM capable bit in SuperSpeed USB Device Capabilities Descriptor.

In case the recipient is device and the device works in HS or FS, DEVICE_REMOTE_WAKEUP and TEST_MODE are defined as feature selectors.

(d) When Clear Feature(DEVICE_REMOTE_WAKEUP) comes, disable the remote wakeup function of the device.

(e) When TEST_MODE feature is enabled, the device is in test mode. But it is defined that the power cycle is used for the device to exit from test mode and Clear Feature(TEST_MODE) does not clear the feature.

For FUNCTION_SUSPEND, Clear Feature is not used to change the feature. Only Set Feature(FUNCTION_SUSPEND) is used to change the feature.

In case the recipient is endpoint, ENDPOINT_HALT is defined as feature selector. All of SS, HS and FS devices support the feature.

(f) When Clear Feature(ENDPOINT_HALT) comes, it means the reset of Halt feature and the initialization of the endpoint.
At first, set Pn_CON.Pn_CLR and wait for Pn_CON.Pn_CLR to return to 0.

- Pn_CON.Pn_CLR = 1 (Initialization of the endpoint (pipe) is required.)
- Wait for Pn_CON.Pn_CLR = 0

After Pn_CON.Pn_CLR = 0, set enable bits below again.

- Pn_CON.Pn_EN = 1 (The endpoint (pipe) is enabled)
- In case of DMA Transfer, Pn_CON.Pn_DATAIF_EN = 1 (EPC_D_Pn_DATAEN[30:1] is enabled for the endpoint)

Then, set Pn_CON.Pn_RES[1:0] = 01b so that the endpoint responds in normal state.

- Pn_CON.Pn_RES[1:0] = 01b (Normal response)

It is not recommended that the endpoint 0 (PIPE0) supports function STALL for HS and FS device. It is also defined that SS device does not support the feature. If the device does not support Halt feature for the endpoint 0, it executes the control transfer of Clear Feature(ENDPOINT_HALT) for the endpoint 0 normally but can ignore the request.

It is noted in **Section 35.6.5.9(5), Get Status** how each feature is controlled as the status of the device.

(2) Get Configuration

This request returns the current device configuration value.

In case this request is received, return the current configuration value. It has been selected with Set Configuration. If not, return the initial value (= zero).

(3) Get Descriptor

This request returns the specified descriptor if the descriptor exists.

The length of transfer is specified in wLength of setup data. In case the size of the descriptor equals to or is smaller than the value in wLength, transmit all of the descriptor from the beginning to the end. In case the size of the descriptor is larger than the value in wLength, transmit a part of the descriptor from the beginning to the length specified in wLength.

Each packet transporting the descriptor should equal to or smaller than the max packet size defined for each speed mode (512byte for SS, 64byte for HS and 8/16/32/64byte for FS). If the size of the last packet equals to the max packet size defined, zero length packet should follow it.

(4) Get Interface

This request returns the selected alternate setting of the specified interface.

In case this request is received, return the current alternate setting of the interface. It has been selected with Set Interface. If not, return the initial value (= zero).

(5) Get Status

This request returns status for the specified recipient.

In case the recipient is device, the information returned for this request as SuperSpeed device is shown in **Figure 35.6-51**.

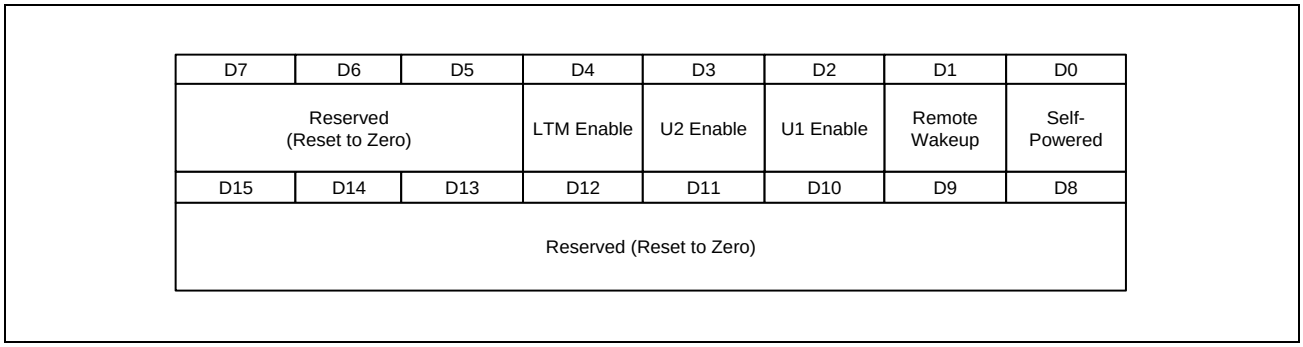


Figure 35.6-51 Information as SS Device in Case the Recipient is Device

D0: This bit shows whether the device is self-powered or not.

D1: This bit shows whether the device supports Remote Wakeup or not.
SuperSpeed device is defined to set this bit to 0 and use Function Remote Wakeup instead.

D2: This bit shows whether the device is currently enabled to initiate U1 entry or not. If this bit is 0, the device is disabled to initiate U1 entry. Regardless of whether this bit is set or not, the device can accept the request for U1 entry from the downstream port and enter U1 state.
This bit is set to 1 on the reception of Set Feature(U1_ENABLE) and set to 0 on the reception of Clear Feature(U1_ENABLE). This bit is reset to 0 when the device is reset.

D3: This bit shows whether the device is currently enabled to initiate U2 entry or not. If this bit is 0, the device is disabled to initiate U2 entry. Regardless of whether this bit is set or not, the device can accept the request for U2 entry from the downstream port and enter U2 state.
This bit is set to 1 on the reception of Set Feature(U2_ENABLE) and set to 0 on the reception of Clear Feature(U2_ENABLE). This bit is reset to 0 when the device is reset.

D4: This bit shows whether the device is currently enabled to send LTM (Latency Tolerance Message) or not. If this bit is 0, the device is disabled to send LTM.
This bit is set to 1 on the reception of Set Feature(LTM_ENABLE) and set to 0 on the reception of Clear Feature(LTM_ENABLE). This bit is reset to 0 when the device is reset.

In case the recipient is device, the information returned for this request as HighSpeed or FullSpeed device is shown in **Figure 35.6-52**.

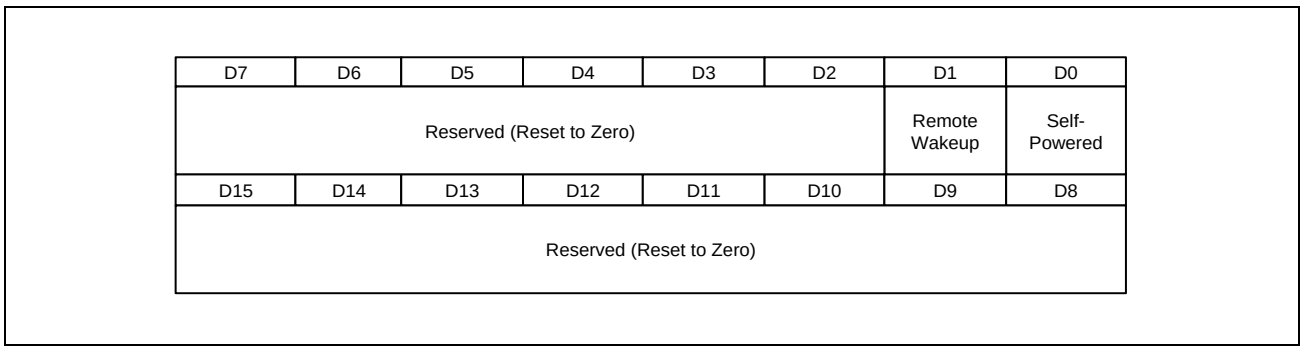


Figure 35.6-52 Information as HS/FS Device in Case the Recipient is Device

D0: This bit shows whether the device is self-powered or not.

D1: This bit shows whether the device supports Remote Wakeup or not.
The default value is 0. The value is modified on the reception of Set Feature(DEVICE_REMOTE_WAKEUP) or Clear Feature(DEVICE_REMOT_WAKEUP). When Set Feature(DEVICE_REMOTE_WAKEUP) is received, the status of this bit is changed to 1. When Clear Feature(DEVIE_REMOT_WAKEUP) is received, the status of this bit is changed to 0.
When this feature is enabled, device can request the remote wakeup in suspended state.
This bit is reset to 0 when the device is reset.

In case the recipient is interface, the information returned for this request as SuperSpeed device is shown in **Figure 35.6-53**.

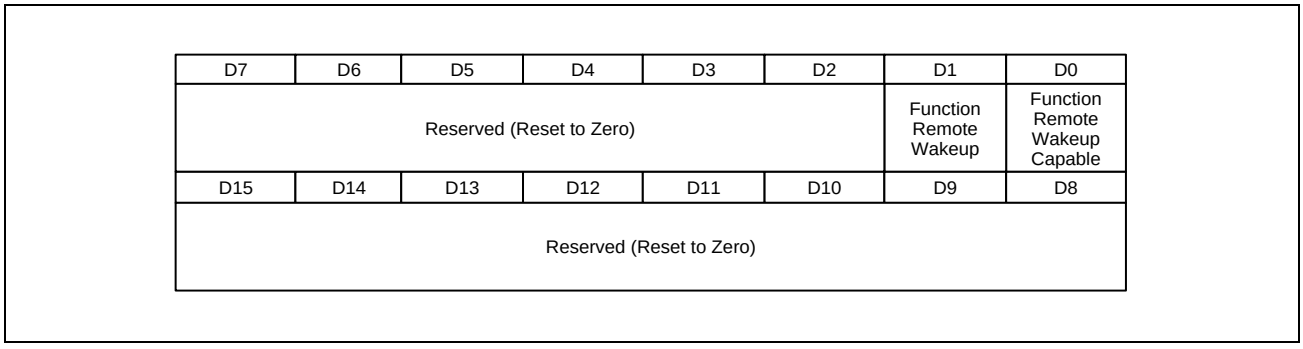


Figure 35.6-53 Information as SS Device in Case the Recipient is Interface

D0: This bit shows whether the interface supports Function Remote Wakeup Capable or not.
Note that Function Remote Wakeup function is used instead of Remote Wakeup function in SuperSpeed device. If the device does not support Function Remote Wakeup, it cannot request the remote wakeup in suspended state (U3).

D1: This bit shows whether the function is currently enabled to request the remote wakeup or not.
The definition of function depends on the specification of device.
The default value is 0. The value is modified on the reception of Set Feature(FUNCTION_SUSPEND). When Set Feature(FUNCTION_SUSPEND) is received and bit 1 in the upper byte of wIndex is 1, Function Remote Wake is enabled and the status of this bit is changed to 1. When Set Feature(FUNCTION_SUSPEND) is received and bit1

in the upper byte of wIndex is 0, Function Remote Wake is disabled and the status of this bit is changed to 0.
When this feature is enabled, device can request the remote wakeup for the suspended function.
This bit is reset to 0 when the device is reset.

In case the recipient is interface, the information returned for this request as HighSpeed or FullSpeed device is shown in **Figure 35.6-54**. All fields are reserved.

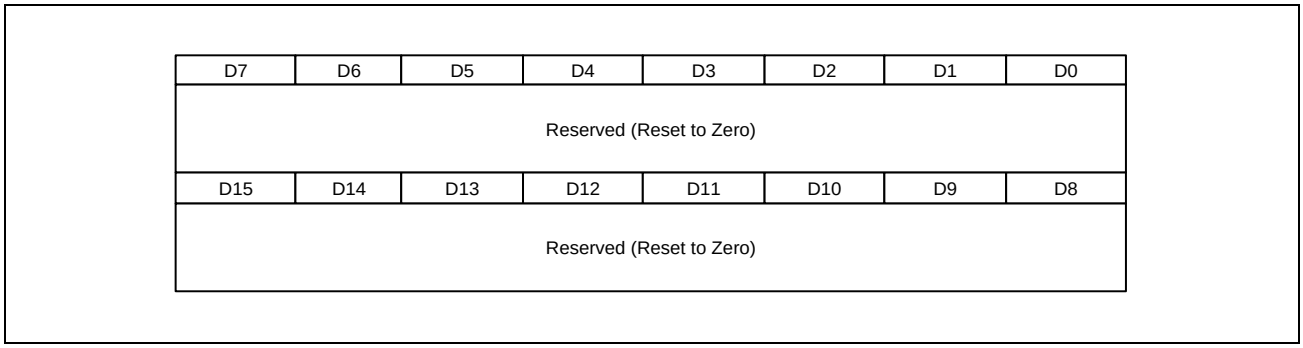


Figure 35.6-54 Information as HS/FS Device in Case the Recipient is Interface

In case the recipient is endpoint, the information returned for this request as SuperSpeed, HighSpeed or FullSpeed device is shown in **Figure 35.6-55**.

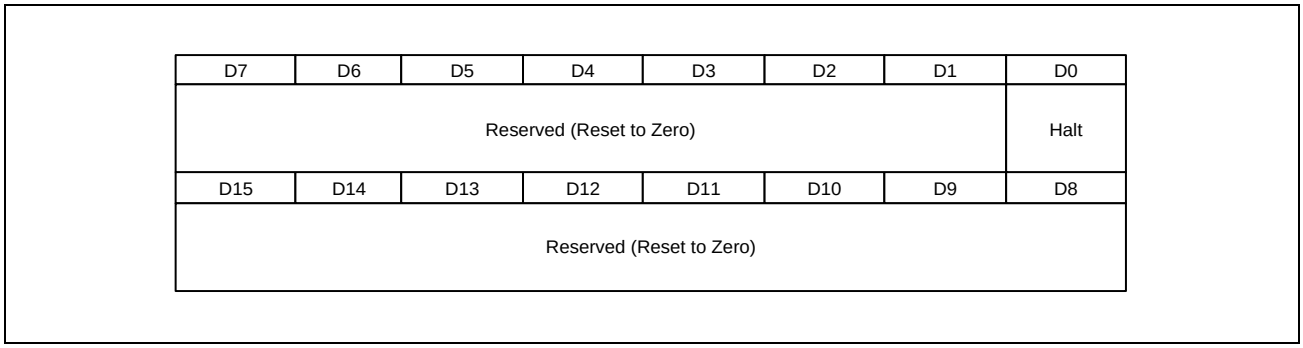


Figure 35.6-55 Information as SS/HS/FS Device in Case the Recipient is Endpoint

D0: This bit shows the current status of Halt feature of the endpoint. If the endpoint is currently halted, the Halt feature is set to 1.
The Halt feature is required to be implemented for all interrupt and bulk endpoints.
The Halt feature might be set due to the internal status of device (when unsupported request comes, for example), or it might be set by Set Feature(ENDPOINT_HALT).
During the feature is set to 1, the endpoint should return STALL response to any request. To return STALL response, set Pn_CON.Pn_RES[1:0] = 10b.

- Pn_CON.Pn_RES[1:0] = 10b (STALL response)

The Halt feature is cleared on the reception of ClearFeature(ENDPOINT_HALT), SetConfiguration and SetInterface. Note that the sequence number in SS and data toggle in HS/FS is initialized on those requests. The feature might be cleared due to the internal status of device (when the cause of error is removed, for example).
When the Halt feature is reset, the endpoint changed its status not to return STALL response. Set Pn_CON.Pn_RES[1:0] = 01b to request the endpoint to respond in the normal mode.

- Pn_CON.Pn_RES[1:0] = 01b (Normal response)

SS device does not support function STALL on control endpoint.

(6) Set Address

This request sets the device address for all future device accesses. The address is shown in wValue field of setup data.

In case this request is received, read the address in wValue field of setup data. But the device cannot update its address to the value given on Set Address until it completes the control transfer of Set Address, since it is defined in USB specification that stages after the initial setup packet assume the same device address as the setup packet.

Write the address given on Set Address to the field below before completing the status stage of the control transfer of Set Address. (That is, write the address to the field below, then P0_CON.P0_ST_RES[1:0] to normal response.)

The hardware of USB3PERI updates the field to new address after it completes the status stage of the control transfer of Set Address.

- USB_COM_CON.DEV_ADDR[6:0] = the value in wValue field of setup packet.

Set Address 0 has the special meaning to initialize the settings in the device. See Table 9-10 in USB3.1 specification.

(7) Set Configuration

This request sets the device configuration. The configuration value selected is shown in lower byte of wValue field of setup data.

The configuration value shall be zero or the value shown in the configuration descriptor.

(1) In case the configuration value matches the value shown in the configuration descriptor, do the operations as follows before the status stage of the control transfer is completed.

- Configure USB3PERI to follow the configuration selected.
- USB_COM_CON.CONF = 1 (USB3PERI is in configured state)

Remember the configuration value since Get Configuration might be requested later.
Then, complete the status stage of the control transfer by setting P0_CON.P0_ST_RES[1:0] = 01b (normal response).

(2) In case the configuration value is zero, it means that the device is requested to go back to address state. Do the operation as follows before the status stage of the control transfer is completed.

- USB_COM_CON.CONF = 0 (USB3PERI is not in configured state)

The buffer of each PIPE should be initialized as well. Do the operation noted in (f) of **Section 35.6.5.9(1), Clear Feature** for PIPEs those have been used in configured state.

Note that the clocks to Data-IN RAMs or Data-OUT RAM is suspended with the setting above. (They are suspended in unconfigured state.) In that case, the clocks to Register RAM and EP0 RAM are still running.
Remember the configuration value since Get Configuration might be requested later.
Then, complete the status stage of the control transfer by setting P0_CON.P0_ST_RES[1:0] = 01b (normal response).

(8) Set Descriptor

This request is optional and may be used to update existing descriptors or new descriptors may be added.

If this request is not defined in the specification of device or the class specification which the device supports, this request is not required to be implemented.

When SetDescriptor comes, update the specified descriptor.

(9) Set Feature

This request is used to set or enable a specific feature.

In case the recipient is device and the device works in SS, U1_ENABLE, U2_ENABLE, LTM_ENABLE and B3_NTF_HOST_REL are defined as feature selectors. But as B3_NTF_HOST_REL is defined for OTG, it is not used for device.

(a) When Set Feature(U1_ENABLE) comes, enable the initiation of U1 entry of USB3PERI as follows. Note that U1_ENABLE enables or disables only the initiation of U1 entry but the device is still allowed to accept LGO_U1 from the downstream port and enters U1 state regardless of the feature.

- SSIFCMD.SSIF_UDIR[0] = 0 (The initiation of LGO_U1 due to direct request is enabled.)
- SSIFCMD.SSIF_UREQ[0] = 0 (The initiation of LGO_U1 due to timeout is enabled.)
- PORTPMSC.U1_TIMEOUT = U1 timeout value defined by user

(b) When Set Feature(U2_ENABLE) comes, enable the initiation of U2 entry of USB3PERI as follows. Note that U2_ENABLE enables or disables only the initiation of U2 entry but the device is still allowed to accept LGO_U2 from the downstream port and enters U2 state regardless of the feature.

- SSIFCMD.SSIF_UDIR[1] = 0 (The initiation of LGO_U2 due to direct request is enabled.)
- SSIFCMD.SSIF_UREQ[1] = 0 (The initiation of LGO_U2 due to timeout is enabled.)
- PORTPMSC.U2_TIMEOUT = U2 timeout value in received U2 Inactivity Timeout LMP

(c) When Set Feature(LTM_ENABLE) comes, enable the transmission of LTM (Latency Tolerance Message). Note that SS device must support U1 and U2 features, but LTM feature is optional. SS device shows whether it supports LTM feature or not on LTM capable bit in SuperSpeed USB Device Capabilities Descriptor.

In case the recipient is device and the device works in HS or FS, DEVICE_REMOTE_WAKEUP and TEST_MODE are defined as feature selectors.

(d) When Clear Feature(DEVICE_REMOTE_WAKEUP) comes, enable the remote wakeup function of the device. When requesting the remote wakeup, see the flow in **Section 35.6.5.8(9), Resume in USB2.0 (Initiated by Device)**.

(e) When TEST_MODE feature is enabled, the device is in test mode. The upper byte of wIndex of setup data specifies test mode selector and it is defined in Table 9-7 of USB2.0 specification.
USB3PERI has the function for TEST_MODE with the setting of USB20_CON.B2_TSTMOD [2:0] and USB20_CON.B2_TSTMOD_EN. When Set Feature (TEST_MODE) comes, set USB20_CON.B2_TSTMOD[2:0] and USB20_CON.B2_TSTMOD_EN according to the test mode selector specified.

In case the recipient is interface and the device works in SS, FUNCTION_SUSPEND is defined as feature selector.

(f) The function within the device shows whether it supports Function Remote Wakeup function or not in Function Remote Wakeup Capable bit in **Figure 35.6-53**. When the function supports Function Remote Wake and Set Feature(FUNCTION_SUSPEND) is received and the bit 1 in the upper byte of wIndex is 1, enable Function Remote Wake. When the function supports Function Remote Wake and Set Feature(FUNCTION_SUSPEND) is received and the bit 1 in the upper byte of wIndex is 0, disable Function Remote Wake.
To request the function remote wakeup, See **Section 35.6.5.8(5), Function Remote Wakeup**.

In case the recipient is endpoint, ENDPOINT_HALT is defined as feature selector. All of SS, HS and FS devices support the feature.

(g) When Set Feature(ENDPOINT_HALT) comes, set Pn_CON.Pn_RES[1:0] = 10b to return STALL response from the endpoint.

- Pn_CON.Pn_RES[1:0] = 10b (STALL response)

Note that the state machine of Stream bulk transits to Disabled state by receiving Set Feature(ENDPOINT_HALT). If the endpoint works as the Stream bulk one, disable all transfers on the reception of Set Feature(ENDPOINT_HALT).

It is not recommended that the endpoint 0 supports function STALL for HS and FS device. It is also defined that SS device does not support the feature. If the device does not support Halt feature for the endpoint 0, it executes the control transfer of Set Feature(ENDPOINT_HALT) for the endpoint 0 normally but can ignore the request.

It is noted in **Section 35.6.5.9(5), Get Status** how each feature is controlled as the status of the device.

(10) Set Interface

This request allows host to select an alternate setting of the specified interface.

In case this request is received, configure USB3PERI to follow the configuration of interface selected.

- Configure USB3PERI to follow the configuration of interface selected

As Set Interface means the initialization of selected interface as well, it is recommended to initialize the PIPEs related to the interface using Pn_CON.Pn_CLR. The operations as follows are required for all PIPEs related to the interface.

- Pn_CON.Pn_CLR = 1 (Initialization of PIPE)
- Wait for Pn_CON.Pn_CLR returns to 0
- Pn_CON.Pn_EN = 1 (Enabling the PIPE again)
- In case of DMA Transfer, Pn_CON.Pn_DATAIF_EN = 1 (Enabling data interface for the PIPE again.)

Remember the alternate setting of the interface since Get Interface might be requested later.

(11) Set Isochronous Delay

This request informs the device of the delay from the time host transmits a packet to the time it is received by the device.

As USB3PERI does not support Isochronous transfer, so there is no function to use the value received on this request.

From the viewpoint of implementation the device can return STALL response in order to show it does not support this request, or can ignore the request although it responds correctly to the control transfer of this request.

(12) Set SEL

This request is valid when the device works in SS and sets both the U1 and U2 System Exit Latency and the U1 or U2 exit latency for all the links between a device and a root port on the host.

When Set SEL comes, update BELT (Best Effort Latency Tolerance) value referring the information provided on this request, if required.

(13) Synch Frame

This request is used to set and then report an endpoint’s synchronization frame.

As USB3PERI does not support Isochronous transfer, so there is no function to use the value received on this request.

From the viewpoint of implementation the device can return STALL response in order to show it does not support this request, or can ignore the request although it responds correctly to the control transfer of this request.

35.6.5.10 BOT Control

Bulk Only Transport (BOT) is defined as one of transfer methods in mass storage class. An example of BOT operation is described here.

(1) Overall

BOT consists of two bulk endpoints as its name suggests.

- Bulk OUT PIPE (for the reception of CBW or OUT data)
- Bulk IN PIPE (for the transmission of CSW or IN data)

In BOT protocol, Command Block Wrapper (CBW) is sent to request an operation in advance of IN or OUT data transfers, and Command Status Wrapper (CSW) is sent to notify the result of the operation after the IN or OUT data transfers. There are some commands which do not require the data transfers. For such command, only CBW and CSW are exchanged.

(2) BOT Assistance Mode

USB3PERI has BOT assistance mode. The mode is available when Pn_MOD.Pn_BOT is set to 1 for OUT PIPE in BOT.

In BOT assistance mode, USB3PERI notifies the reception of CBW by asserting Pn_INT_STA.Pn_CBW_STA. If an interrupt due to the bit is enabled, the interrupt is generated.

USB3PERI interprets the received packet as CBW when both of two conditions below are satisfied for the packet.

- The length of the packet is 31 bytes.
- The first 4 bytes of the packet (dCBWSignature) equals to 43425355h.

In this mode, Pn_CON.Pn_DATAIF_EN of the OUT PIPE that receives CBW is disabled (reset to 0) every time CBW (the packet which satisfies two conditions above) is received. As the result, CBW is not transferred through Data Interface or on AXI DMA transfer. Pn_CON.Pn_DATAIF_EN of IN PIPE is not changed.

CBW can be transferred through Data Interface or on AXI DMA transfer if Pn_CON.Pn_DATAIF_EN is set to 1 again, but it is recommended to read CBW through Pn_READ register because the software should read and decode it for BOT operation.

As CBW is a short packet in bulk transfer, the OUT PIPE in BOT enters flow control after the reception of CBW if it works as USB3.1 device. When CBW has been read through Pn_READ register (or when it has been transferred through Data Interface or on AXI DMA transfer), USB3PERI returns ERDY from the OUT PIPE automatically. But if OUT data transfer is requested, make sure to set Pn_CON.Pn_DATAIF_EN to 1 after CBW has been read or transferred.

If BOT assistance mode is not used (Pn_MOD.Pn_BOT = 0) for BOT transfer, the OUT PIPE in BOT does not distinguish CBW and CBW is transferred as one of short packets through Data Interface or on AXI DMA transfer. In that case Pn_CON.Pn_DATAIF_EN is not disabled and Pn_INT_STA.Pn_CBW_STA is not asserted on the reception of CBW.

(USB3PERI does not know that the packet is CBW.)

The software is required to find CBW in system memory (where the received packet is transferred to) when a short packet is received.

(3) BOT Process

It is assumed that BOT assistance mode in **Section 35.6.5.10(2), BOT Assistance Mode** and the flow of BOT process with the mode is described here.

Make sure to set Pn_MOD.Pn_BOT = 1.

As noted above, one bulk OUT PIPE and one bulk IN PIPE are required for BOT. For the settings of bulk OUT PIPE, see **Section 35.6.5.5(2), Bulk-OUT Process**. For the settings of bulk IN PIPE, see **Section 35.6.5.5(1), Bulk-IN Process**.

As the preparation of BOT, enable an interrupt due to Pn_INT_STA.Pn_CBW_STA of the OUT PIPE. That is, set Pn_INT_ENA.Pn_CBW_ENA of bulk OUT PIPE to 1.

- Pn_INT_ENA.Pn_CBW_ENA = 1 (Interrupt due to Pn_INT_STA.Pn_CBW_STA is enabled)

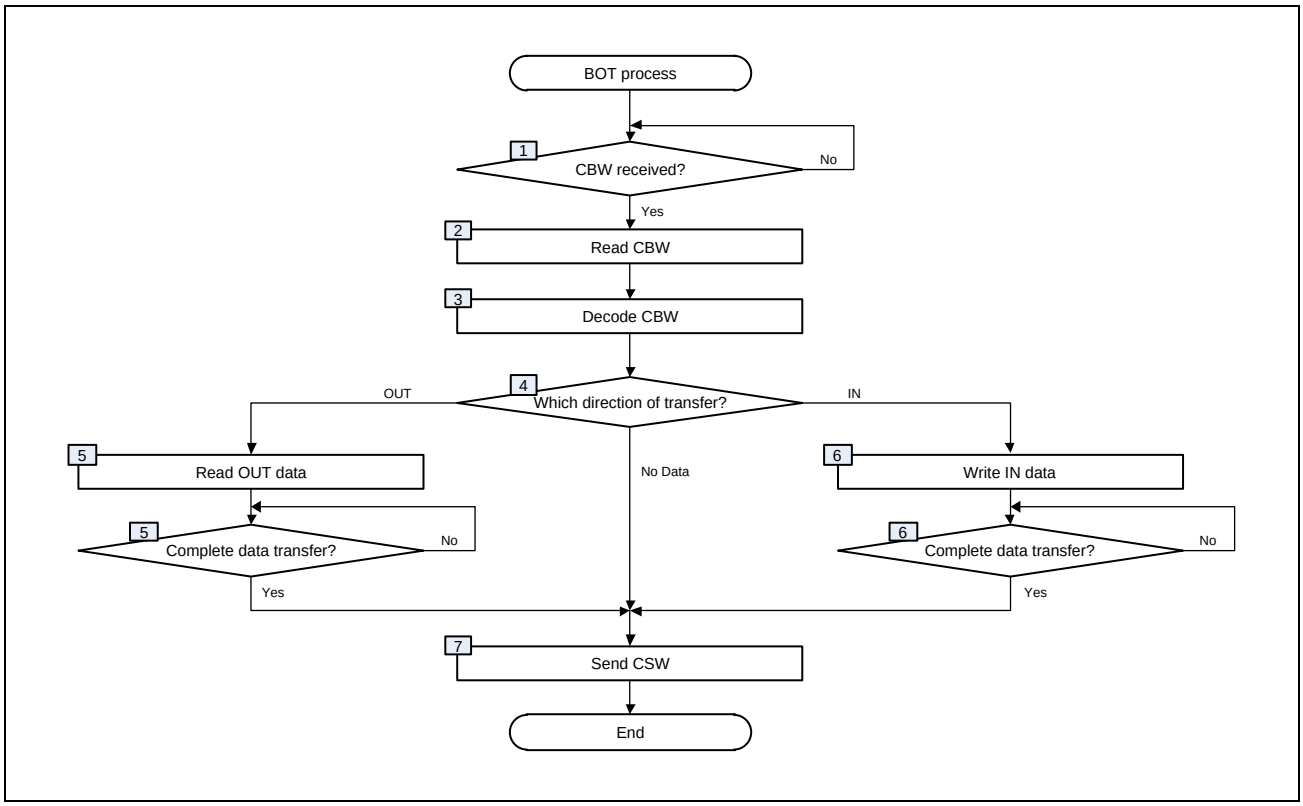


Figure 35.6-56 BOT Process Flow

(1) Is CBW received?
When CBW is received, Pn_INT_STA.Pn_CBW_STA is asserted and an interrupt due to it is generated.

- Interrupt due to Pn_INT_STA.Pn_CBW_STA is asserted
- Check that Pn_INT_STA.Pn_CBW_STA = 1

After the confirmation above, clear Pn_INT_STA.Pn_CBW_STA.

- Pn_INT_STA.Pn_CBW_STA = 1 (Clearing the event of the reception of CBW)

(2) Read CBW
Read CBW through Pn_READ register.

(3) Decode CBW
Decode the content of CBW which is read at (2).
If any operation other than data transfer is requested, do it here.

(4) Which direction of transfer is requested?
If OUT transfer is requested, proceed to (5).
If IN transfer is requested, proceed to (6).
If No data transfer is requested, proceed to (7).

(5) Read OUT data
It is assumed here that OUT data received is transferred through Data Interface or on AXI DMA transfer. Set Pn_CON.Pn_DATAIF_EN = 1 since it is reset to 0 at the reception of CBW.
For bulk OUT transfer, see **Section 35.6.5.5(2), Bulk-OUT Process**. If two or more packets are received, repeat the flow shown there.
Proceed to (7).

(6) Write IN data
It is assumed here that IN data to be transmitted is transferred through Data Interface or on AXI DMA transfer. Pn_CON.Pn_DATAIF_EN of IN PIPE is not changed on the reception of CBW.
For bulk IN transfer, see **Section 35.6.5.5(1), Bulk-IN Process**. If two or more packets are to be transmitted, repeat the flow shown there.
Proceed to (7).

(7) Send CSW
It is assumed here that the software prepares CSW and writes it through Pn_WRITE register.
Before writing CSW to the buffer of the IN PIPE, confirm that the buffer has available space.

- Check that Pn_STA.Pn_BUFSTS = 1 for bulk IN PIPE in order to confirm that the buffer for the PIPE is available.

If the buffer has available space for CSW, write CSW through Pn_WRITE register. Since the size of CSW is 13 bytes, the access to Pn_WRITE register is required 4 times. The last write word has only 1 valid byte.

- Write CSW to Pn_WRITE register. 4 write accesses are required for 13 bytes of CSW.

After CSW has been written to Pn_WRITE register, send CSW as follows. As only 32-bit access is allowed to the register, both fields should be set in one word access.

- Pn_CON.Pn_SEND = 1
- Pn_CON.Pn_BYTE_EN[1:0] = 01b (The last word has only 1 valid byte.)

35.6.5.11 The Others

(1) USB3.1 TP Send Flow

This operational flow is the way to send any USB3.1 TP data. It is used for the TP transmission such as Device Notification TP.

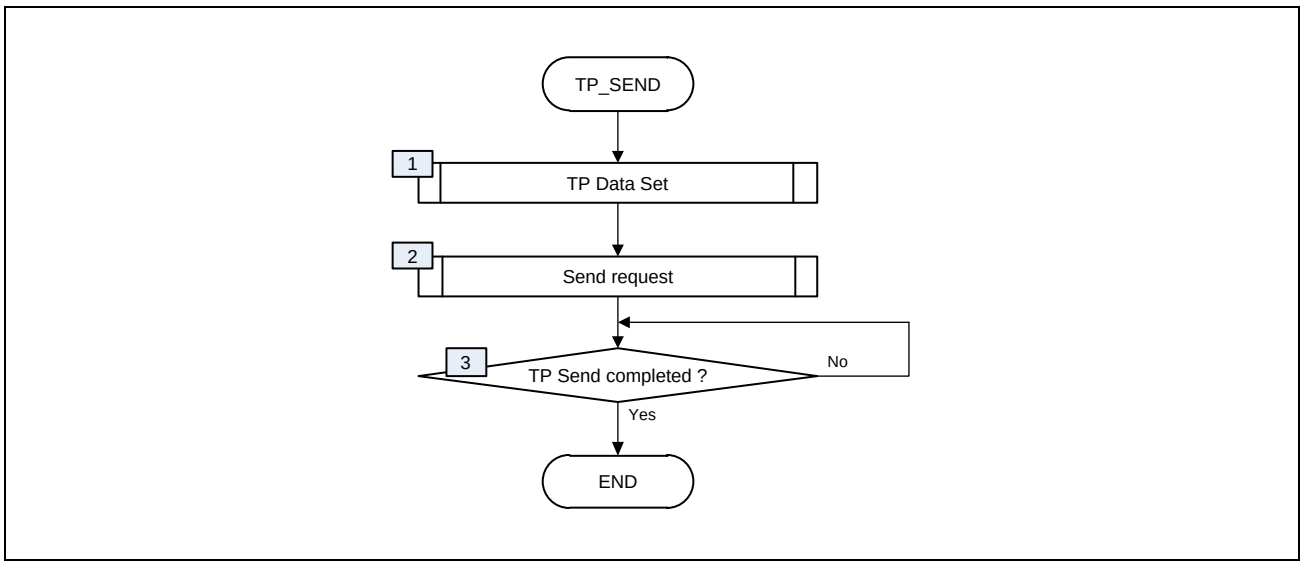


Figure 35.6-57 TP Send Flow

(1) TP Data set
Write TP Data that will be sent to Host on the EPC registers as below.

- USB3_TPDAT_0 = DWORD0 of TP
- USB3_TPDAT_1 = DWORD1 of TP
- USB3_TPDAT_2 = DWORD2 of TP

(2) Send request
Set the following register to make a request for transmission of TP data that was set in (1).

- USB_INT_ENA_1.B3_TPSUCS_ENA = 1 (Interrupt due to the success of TP transmission is enabled)
- USB30_CON.B3_TP_SEND = 1 (request for transmission TP)

(3) TP Send completed?
Check the status of completion on the bits below.

- Interrupt due to USB_INT_STA_1.B3_TPSUCS_STA is asserted
- Check whether USB_INT_STA_1.B3_TPSUCS_STA = 1 (transmission of TP is completed)
- Write 1 to the asserted bit to clear.

NOTE

If WarmReset or HotReset has been issued by Host when there is a request with B3_TP_SEND, TP may not be transmitted and interrupt due to B3_TPSUCS_STA may not assert.

35.6.6 Configuration of USB3PERI

It is described how to configure USB3PERI in this section.

35.6.6.1 Prohibitions of Register Access

(1) Prohibited Access During a Register is Used

P0_READ, P0_WRITE, Pn_READ and Pn_WRITE registers are used to read or write a packet to each PIPE through these register.

But as noted in the subsection of each register, it is prohibited to access to other Px_yyy registers before whole of a packet has been read or written through the register which is currently used. Px_yyy registers. The packet might not be read or written correctly otherwise.

It is also prohibited to change the targeted PIPE of Pn_yyy registers on PIPE_COM.PIPE_NUM[4:0] before read or write of a packet has been completed to the PIPE currently selected.

When P0_WRITE or Pn_WRITE register is used, it is required to send the packet which has been written by setting P0_CON.P0_SEND or Pn_CON.Pn_SEND before the access to other Px_yyy registers.

Make sure to complete read or write of a packet before the access to other Px_yyy registers, once it is started.

If Px_yyy register is read or written in an interrupt routine, it might violate the notation without awareness. To avoid the case, mask the interrupt related to the routine during read or write of a packet, or never access to Px_yyy registers in an interrupt service.

The lists of registers prohibited to access during P0_READ or Pn_READ register is used are as follows.

Prohibited to access during P0_READ register is used	P0_WRITE, Pn_READ, Pn_WRITE, Pn_STA, Pn_LNG, Pn_RSVPKT
Prohibited to access during Pn_READ register is used	P0_READ, P0_WRITE, P0_STA, P0_LNG, Pn_WRITE

The lists of registers prohibited to access during P0_WRITE or Pn_WRITE register is used are as follows.

Prohibited Registers for accessing in case of P0_WRITE	P0_READ, Pn_READ, Pn_WRITE, Pn_STA, Pn_LNG, Pn_RSVPKT
Prohibited Registers for accessing in case of Pn_WRITE	P0_READ, P0_WRITE, P0_STA, P0_LNG, Pn_READ

(2) Prohibited Access Depends on PIPE Direction

Some registers have a specified direction of transfer for use.

P0_READ, Pn_READ, P0_LNG and Pn_LNG are only used for OUT Transfer. So these registers are prohibited to access if direction of transfer is IN (Px_DIR = 1).

P0_WRITE and Pn_WRITE are only used for IN Transfer. So these registers prohibited to access if direction of transfer is OUT. (Px_DIR = 0)

The lists of registers prohibited to access in case of Px_MOD.Px_DIR = 1 (for IN Transfer) are as follows.

Prohibited Registers for accessing in case of P0_MOD.P0_DIR = 1	P0_READ, P0_LNG
Prohibited Registers for accessing in case of Pn_MOD.Pn_DIR = 1	Pn_READ, Pn_LNG

The lists of registers prohibited to access in case of Px_MOD.Px_DIR = 0 (for OUT Transfer) are as follows.

Prohibited Registers for accessing in case of P0_MOD.P0_DIR = 0	P0_WRITE
Prohibited Registers for accessing in case of Pn_MOD.Pn_DIR = 0	Pn_WRITE

35.7 USB Test Module (USB3TEST)

35.7.1 Features

This section mainly describes the USB test module (USB3TEST) which is connected between the USB3HOST and USB3PERI and the PHY module. The main functions of USB3TEST are as follows.

- Reset control
- Control of PHY input pins
- Monitoring of PHY output pins

Section 36 PCI Express 2.0 Interface (PCIe)

This section describes the functions of the PCI Express 2.0 interface (PCIe).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

36.1 Overview

This unit has a dual structure so that the device incorporating it can operate as a root complex or endpoint device, and includes a Type 0/1 Configuration Register for this purpose. Furthermore, it has an internal DMA controller. However, limitations imposed by the AXI place restrictions on some specifications of PCI Express functionality.

■ Unit Function Specifications

AXI Interface Specification

Little endian is only supported.

- Master interface
  - 1 port
  - Bus width: 64 bits
  - ID width: 4 bits (fixed value)
  - Interleave not supported
  - Burst type: Incremental (1 to 16 words, bursts of 4 or 8)
  - Byte-lane transfer and narrow transfer (8, 16, 32-bit lengths, only in 1 dword) are supported. Non-aligned (“unaligned”) transfer is not supported.
  - Allowable number of read/write requests: Variable (1 to 16)
  - Write interleave depth: 1
  - Protection (data/user/non-secure) can be set by using registers.
  - Access type: Normal only (exclusive or locked access not supported)

- Slave interface
  - 1 port
  - Bus width: 64 bits
  - ID width: Up to 8 bits
  - Burst type: Incremental (TYPE = INCR, LENGTH = 1 to 16, SIZE = 1/2/4/8 bytes)
  - Support for byte-lane transfer (only when valid bytes are consecutive), unaligned transfer, and narrow transfer (1, 2, and 4 bytes)
  - Number of read transactions which can be accepted: 1 to 8
    Number of write transactions which can be accepted: 1
  - Read data reordering depth: 1 to 8
    Write interleave depth: 1

- Required memory area: 16 KB or larger (variable)
- Protection is not distinguished (reception is possible even in the case of protection).
- Access type: Normal only (exclusive or locked access not supported)
- Cache signals (ARCACHE/AWCACHE) are only supported for bufferable bits for writing.

- DMAC
  - DMA method: Register control, descriptor control
  - Number of channels: 8
  - Allowable number of requests to be issued (the maximum total number: 8. When DMAC ch. 1 issues eight PCIe-MRd/MW requests, other channels cannot issue requests).

    PCIe MRd: Up to 8/ch PCIe MWr: 1/ch
    AXI Read: 1/ch AXI Write: 1/ch

PCI Express Specification（Compliant with the PCI Express Base Specification 4.0）

- PCI Express Gen1 (2.5 (GT/s))/Gen2 (5.0 (GT/s))
- Root Complex (RC) / Endpoint (EP) Applications, Type 0/1 Configuration Register
- Supports one lane (×1) or two lanes (x2)
- Data payload: up to 128 bytes; read request size: up to 512 bytes
- Virtual channels are not supported (only VC0 supported)
- Number of outstanding transfers: 1 to 8
- Dynamic control of speed up/down configuration
- Clock Power Management is not supported (P1.CPM, P2.CPM not supported)
- Power Management (ASPM supported)
- Error handling/logging (AER supported)
- Replay FIFO with ECC
- Internal Memory without parity
- Number of Support Functions: 2
- Number of DMAC channels: 8

The initial values of configuration registers for vendor ID, device ID, revision ID, class code, subsystem vendor ID, subsystem ID, and base address register mask are 0. Set appropriate values in the registers before the start of link up.

L1PM substates are not supported.

36.2 TOP Pins

36.2.1 Pin Functions

This section gives the list of top-level pins of this unit.

36.2.1.1 List of External Pins

Table 36.2-1 lists the external pins of the PCI.

Table 36.2-1 List of External Pins

Pin name	I/O	Function
PCRXD0P	Input	Serial data input for Lane0 (positive)
PCRXD0M	Input	Serial data input for Lane0 (negative)
PCRXD1P	Input	Serial data input for Lane1 (positive)
PCRXD1M	Input	Serial data input for Lane1 (negative)
PCTXD0P	Output	Serial data output for Lane0 (positive)
PCTXD0M	Output	Serial data outpu for Lane0 (negative)
PCTXD1P	Output	Serial data output for Lane1 (positive)
PCTXD1M	Output	Serial data output for Lane1 (negative)
PCREFCKP	Input	Reference clock input (positive) 100 MHz
PCREFCKM	Input	Reference clock input (negative) 100 MHz
PCREXT	Input	External reference resistor connection: 8.2kΩ ±1%
PCRSTOUTB	Output	Reset output

36.2.1.2 List of Internal Pins

Table 36.2-2 lists the internal pins of this unit.

Table 36.2-2 List of Internal Pins (1/2)

Pin name	I/O	Function
FLR_REQ[1:0]	Output	FLR request output
FLR_RESET[1:0]	Input	FLR input
INTX_EP_F0	Input	INTX interrupt signal input for Function #0 for Endpoint (Level signal input: 2 or more cycles of ACLK)
INTX_EP_F1	Input	INTX interrupt signal input for Function #1 for Endpoint (Level signal input: 2 or more cycles of ACLK)
UI_EXTMSI_VAL0	Input	MSI interrupt notification pin for Endpoint
UI_EXTMSI_VAL1	Input	MSI interrupt notification pin for Endpoint
UI_EXTMSI_VAL2	Input	MSI interrupt notification pin for Endpoint
UI_EXTMSI_VAL3	Input	MSI interrupt notification pin for Endpoint
UI_EXTMSI_VAL4	Input	MSI interrupt notification pin for Endpoint
UI_EXTMSI_VEC0 [4:0]	Input	MSI interrupt vector specification pin for Endpoint
UI_EXTMSI_VEC1 [4:0]	Input	MSI interrupt vector specification pin for Endpoint
UI_EXTMSI_VEC2 [4:0]	Input	MSI interrupt vector specification pin for Endpoint
UI_EXTMSI_VEC3 [4:0]	Input	MSI interrupt vector specification pin for Endpoint
UI_EXTMSI_VEC4 [4:0]	Input	MSI interrupt vector specification pin for Endpoint
UI_EXTMSI_FUNC0 [2:0]	Input	MSI interrupt function number specification pin for Endpoint
UI_EXTMSI_FUNC1 [2:0]	Input	MSI interrupt function number specification pin for Endpoint
UI_EXTMSI_FUNC2 [2:0]	Input	MSI interrupt function number specification pin for Endpoint
UI_EXTMSI_FUNC3 [2:0]	Input	MSI interrupt function number specification pin for Endpoint
UI_EXTMSI_FUNC4 [2:0]	Input	MSI interrupt function number specification pin for Endpoint
ALLOW_ENTER_L1	Input	ASPM L1 state permission setting input
PME_TIM	Input	Clock input for PM_PME Message for Endpoint
TURN_OFF_EVENT	Output	PME_Turn_Off Msg. Reception flag output for Endpoint
TURN_OFF_EVENT_ACK	Input	Acknowledge input for Endpoint
D3_EVENT_F0	Output	Non-D0 State transition request reception output for Function #0 for Endpoint
D3_EVENT_F1	Output	Non-D0 State transition request reception output for Function #1 for Endpoint
D3_EVENT_ACK_F0	Input	Acknowledgment input for Function # 0for Endpoint
D3_EVENT_ACK_F1	Input	Acknowledgment input for Function # 1for Endpoint
CFG_PMCSR_PME_STATUS_F0	Input	Power Management Event setting input for Function #0 for Endpoint
CFG_PMCSR_PME_STATUS_F1	Input	Power Management Event setting input for Function #1 for Endpoint
CFG_PMCSR_PME_STATUS_WRITECLEAR_F0	Output	PME_STATUS clear output for Function #0 for Endpoint
CFG_PMCSR_PME_STATUS_WRITECLEAR_F1	Output	PME_STATUS clear output for Function #1 for Endpoint
MODE_PORT	Input	Device Type setting 0b: Endpoint 1b: Root Complex
MODE_PORT_ENABLE_B	Input	Input for PHY OFF mode setting 1b: PHY OFF 0b: Normal operation

Table 36.2-3 List of Internal Pins (2/2)

Pin name	I/O	Function
ACLK	Input	System clock input
MAWID[3:0]	Output	AXI Master Interface Signals-Write Address Channel Write address ID tag output
MAWLEN[3:0]	Output	AXI Master Interface Signals-Write Address Channel Burst length output
MAWSIZE[2:0]	Output	AXI Master Interface Signals-Write Address Channel Burst size output
MAWBURST[1:0]	Output	AXI Master Interface Signals-Write Address Channel Burst type output (01b: Fixed output of incremental bursts)
MAWCACHE[3:0]	Output	AXI Master Interface Signals-Write Address Channel Cache type output
MBID[3:0]	Input	AXI Master Interface Signals-Write Response Channel Response ID tag input
MARID[3:0]	Output	AXI Master Interface Signals-Read Address Channel Read address ID tag output
MARLEN[3:0]	Output	AXI Master Interface Signals-Read Address Channel Burst length output
MARSIZE[2:0]	Output	AXI Master Interface Signals-Read Address Channel Burst size output
MARBURST[1:0]	Output	AXI Master Interface Signals-Read Address Channel Burst type output (01b: Fixed output of incremental bursts)
MRID[3:0]	Input	AXI Master Interface Signals-Read Data Channel Read ID tag input
SAWID[idlen-1:0] (idlen=8)	Input	AXI Slave Interface Signals-Write Address Channel Write address ID tag input
SAWLEN[3:0]	Input	AXI Slave Interface Signals-Write Address Channel Burst length input
SAWSIZE[2:0]	Input	AXI Slave Interface Signals-Write Address Channel Burst size input
SAWBURST[1:0]	Input	AXI Slave Interface Signals-Write Address Channel Burst type input
SAWVALID	Input	AXI Slave Interface Signals-Write Address Channel Valid signal input 1b: Valid 0b: Invalid
SAWREADY	Output	AXI Slave Interface Signals-Write Address Channel Ready signal input 1b: The slave is ready. 0b: The slave is being prepared.
SWID[idlen-1:0]	Input	AXI Slave Interface Signals-Write Data Channel Write ID tag input
SWSTRB[d/8-1:0]	Input	AXI Slave Interface Signals-Write Data Channel Write strobe input

36.3 Block Diagram

The figure below is a block diagram of the PCI.

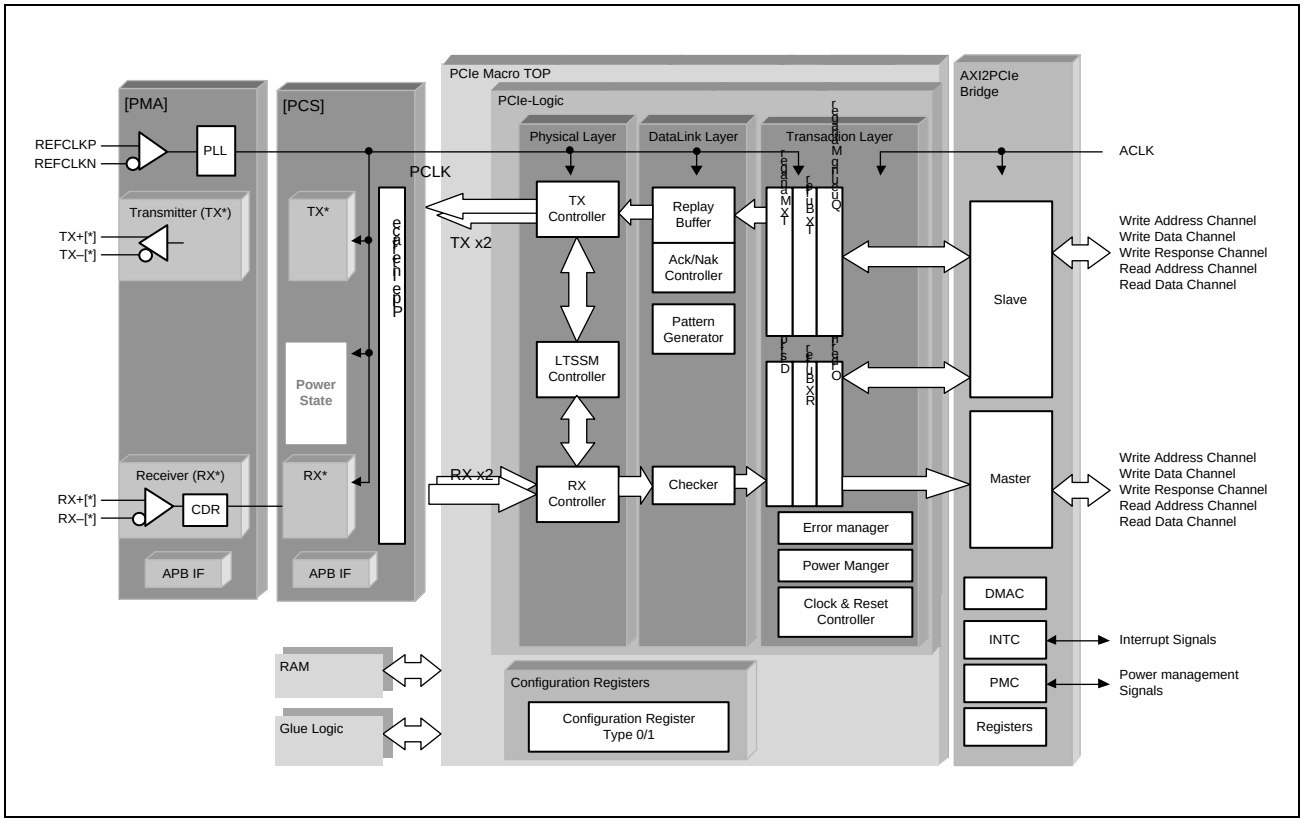


Figure 36.3-1 Block Diagram

36.3.1 Reset

A software reset by the register can be used for this unit. **Table 36.3-1** lists the software resets.

Table 36.3-1 List of Software Resets

Reset Name	Reset Control Register
RST_B	Reset Registers (offset:310h) bit 0
RST_GP_B	Reset Registers (offset:310h) bit 1
RST_RSM_B	Reset Registers (offset:310h) bit 2
RST_CFG_B	Reset Registers (offset:310h) bit 3
RST_LOAD_B	Reset Registers (offset:310h) bit 4
RST_PS_B	Reset Registers (offset:310h) bit 5
ARESETn (CPG)	Reset Control Register 3 bit 12

Note: In addition, there is a function level reset (FLR) which is only available in EP operation.

36.4 Register Descriptions (Root Complex Mode)

The following lists the registers incorporated in this unit.

For the register base address (<PCI_S0_REG_base>), see the section of Address Map.

CAUTION

The results of access to reserved bit areas, debug bit areas, and undefined areas are not guaranteed. The combination of reserved, debug, and undefined areas includes cases where the initial values will be non-zero, and the results of changes to such values are not guaranteed.

Registers with the HwInit attribute

Some registers with the RO attribute stated in the PCI Express Base Specification are writable at the time of initialization. When writing to these registers, CFG_HWINIT_EN (Permission Register (offset: 300h) bit[2]) must be set to 1b.

The following is the outline of categories of the register space within this unit.

AXI Bridge Registers	<PCI_S0_REG_base> + 0000h-1FFCh
Reserved	<PCI_S0_REG_base> + 2000h-5FFCh
PCI Express Configuration Registers (Type1)	<PCI_S0_REG_base> + 6000h-6FFCh
Reserved	<PCI_S0_REG_base> + 7000h-7FFCh

Access to the reserved spaces above is prohibited.

36.4.1 List of AXI Bridge Registers

The table below lists the AXI bridge registers. Unless specifically stated otherwise, byte, word, and double word access are all possible.

Table 36.4-1 AXI Bridge Registers (1/5)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
Reserved 00h to 7Ch				
00 to 7Ch	Reserved	—	—	—
Request Issuing 80h to FCh				
80h	Request Data Register 0	PCI_RC_REQDATA0	xxxx_xxxxh	32
84h	Request Data Register 1	PCI_RC_REQDATA1	xxxx_xxxxh	32
88h	Request Data Register 2	PCI_RC_REQDATA2	xxxx_xxxxh	32
8Ch	Request Receive Data Register	PCI_RC_REQRCVDAT	xxxx_xxxxh	32
90h	Request Address Register 1	PCI_RC_REQADR1	xxxx_xxxxh	32
94h	Request Address Register 2	PCI_RC_REQADR2	xxxx_xxxxh	32
98h	Request Byte Enable Register	PCI_RC_REQBE	0000_000Fh	32
9Ch	Request Issue Register	PCI_RC_REQISS	0000_0000h	32
A0h to FCh	Reserved	—	—	—
PCI Interruption 100h to 11Ch				
100h	MSI Receive Window Address Register	PCI_RC_MSIRCVWADR	0000_0000h	32
104h	Reserved	—	—	—
108h	MSI Receive Window Mask Register	PCI_RC_MSIRCVWMSK	0000_0003h	32
10Ch	Reserved	—	—	—
110h	PCI INTx Receive Interrupt Enable Register	PCI_RC_PINTRCVIE	0000_0000h	32
114h	PCI INTx Receive Interrupt Status Register	PCI_RC_PINTRCVIS	0000_0000h	32
118h	Debug	—	—	—
11Ch	Reserved	—	—	—
Message Interruption 120h to 13Ch				
120h	Message Receive Interrupt Enable Register	PCI_RC_MSGRCVIE	0000_0000h	32
124h	Message Receive Interrupt Status Register	PCI_RC_MSGRCVIS	0000_0000h	32
128h to 12Ch	Reserved	—	—	—
130h	Message Code Register	PCI_RC_MSGCODE	0000_0000h	32
134h	Message Data Register	PCI_RC_MSGDATA	0000_0000h	32
138h	Message Header 3rdDW Register	PCI_RC_MSGH3DW	0000_0000h	32
13Ch	Message Header 4thDW Register	PCI_RC_MSGH4DW	0000_0000h	32
Interrupt Table 140h to 1FCh				
140h	Interrupt Table Register	PCI_RC_INTTABLE	00xx_0000h	32
144h to 1FCh	Reserved	—	—	—
Error Event 200h to 2FCh				
200h	PCIe Event Interrupt Enable 0 Register	PCI_RC_PEIE0	0000_0000h	32
204h	PCIe Event Interrupt Status 0 Register	PCI_RC_PEIS0	0000_0000h	32
208h	PCIe Event Interrupt Enable 1 Register	PCI_RC_PEIE1	0000_0000h	32
20Ch	PCIe Event Interrupt Status 1 Register	PCI_RC_PEIS1	0000_0000h	32
210h	AXI Master Error Interrupt Enable Register	PCI_RC_AMEIE	0000_0000h	32
214h	AXI Master Error Interrupt Status Register	PCI_RC_AMEIS	0000_0000h	32
218h to 21Ch	Reserved	—	—	—

Table 36.4-1 AXI Bridge Registers (2/5)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
220h	AXI Slave Error Interrupt Enable 1 Register	PCI_RC_ASEIE1	0000_0000h	32
224h	AXI Slave Error Interrupt Status 1 Register	PCI_RC_ASEIS1	0000_0000h	32
228h to 22Ch	Debug	—	—	—
230h	AXI Slave Error Interrupt Status 3 Register	PCI_RC_ASEIS3	0000_0000h	32
234h to 244h	Debug	—	—	—
248h to 2FCh	Reserved	—	—	—
Unit Control 300h to 3FCh				
300h	Permission Register	PCI_RC_PERM	0000_0000h	32
304h to 30Ch	Reserved	—	—	—
310h	Reset Register	PCI_RC_RESET	0000_00xxh	32
314h	Mode Set 0 Register	PCI_RC_MSET0	2001_2000h	32
318h	Mode Set 1 Register	PCI_RC_MSET1	0000_33F2h	32
31Ch to 37Ch	Debug	—	—	—
380h	Mode Set 3 Register	PCI_RC_MSET3	0000_0000h	32
384h	Debug Output 1 Register	PCI_RC_DBGOUT1	0000_0000h	32
388h	Debug Output 2 Register	PCI_RC_DBGOUT2	0000_0000h	32
390h	Debug Input 0 Register	PCI_RC_DBGIN0	xxxx_xxxxh	32
394h to 3FCh	Reserved	—	—	—
400h	PCIe Core Mode Set 1 Register	PCI_RC_PCMSET1	07D0_00F2h	32
404h	PCIe Core Control 1 Register	PCI_RC_PCCTRL1	0000_0000h	32
408h	PCIe Core Status 1 Register	PCI_RC_PCSTAT1	000x_xxxxh	32
40Ch	Debug	—	—	—
410h	PCIe Core Control 2 Register	PCI_RC_PCCTRL2	003E_0000h	32
414h	PCIe Core Status 2 Register	PCI_RC_PCSTAT2	xxxx_xxxxh	32
418h to 428h	Debug	—	—	—
42Ch	PCIe Core Status 5 Register	PCI_RC_PCSTAT5	0000_0x00h	32
430h to 43Ch	Reserved	—	—	—
440h to 458h	Debug	—	—	—
45Ch to 46Ch	Reserved	—	—	—
470h	Debug	—	—	—
474h to 47Ch	Reserved	—	—	—
480h	Debug	—	—	—
484h to 49Ch	Reserved	—	—	—
4A0h to 4C0h	Debug	—	—	—
4C4h to 4CCh	Reserved	—	—	—
4D0h	DMA Interrupt Vector 0 Register	PCI_RC_DMAINTVEC0	0000_0000h	32
4D4h	DMA Interrupt Vector 1 Register	PCI_RC_DMAINTVEC1	0000_0000h	32
4D8h to 6FCh	Reserved	—	—	—
700h to 744h	Debug	—	—	—
748h to 7FCh	Reserved	—	—	—
DMAC Registers 800h to FFCh				
Common Control 800h to 8FCh				
800h	DMA Control Register	PCI_RC_DMACTRL	0000_0000h	32
804h	Reserved	—	—	—
808h	DMA Interrupt Enable Register	PCI_RC_DMAINTE	0000_0000h	32

Table 36.4-1 AXI Bridge Registers (3/5)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
80Ch	DMA Interrupt Status Register	PCI_RC_DMAINTS	0000_0000h	32
810h to 8FCh	Reserved	—	—	—
Channel Control 900h to 91Ch*1				
900h	DMA Channel Control Register 0	PCI_RC_DMACHCTL0	0000_0000h	32
904h	Reserved	—	—	—
908h	QUE Entry (Lower) Register 0	PCI_RC_QUEE0L	0000_0000h	32
90Ch	QUE Entry (Upper) Register 0	PCI_RC_QUEE0U	0000_0000h	32
910h to 91Ch	Reserved	—	—	—
DMA Setting 920h to 94Ch*1				
920h	DMA Descriptor Control (Descriptor 00h) Register 0	PCI_RC_DMADPCTL0	0000_0000h	32
924h	DMA Source Address (Descriptor 04h) Register 0	PCI_RC_DMASRCA0	0000_0000h	32
928h	DMA Destination Address (Descriptor 08h) Register 0	PCI_RC_DMADSTA0	0000_0000h	32
92Ch	DMA Size (Descriptor 0Ch) Register 0	PCI_RC_DMASIZE0	0000_0000h	32
930h	DMA PCIe Upper Address (Descriptor 10h) Register 0	PCI_RC_DMAPCIEUA0	0000_0000h	32
934h	DMA Transaction Control (Descriptor 14h) Register 0	PCI_RC_DMATCTL0	0000_0000h	32
938h	Reserved	—	—	—
93Ch	DMA Descriptor Link Pointer (Descriptor 1Ch) Register 0	PCI_RC_DMADPLP0	0000_0000h	32
940h to 94Ch	Reserved	—	—	—
DMA Status 950h to 99Ch*1				
950h	DMA Rest Size Register 0	PCI_RC_DMARESTSIZ0	0000_0000h	32
954h	AXI Request Address Register 0	PCI_RC_AREQA0	0000_0000h	32
958h	PCIe Request Address (Lower) Register 0	PCI_RC_PREQA0L	0000_0000h	32
95Ch	PCIe Request Address (Upper) Register 0	PCI_RC_PREQA0U	0000_0000h	32
960h	QUE Status Register 0	PCI_RC_QUESTA0	0000_0000h	32
964h	Reserved	—	—	—
968h	DMAC Error Status Register 0	PCI_RC_DMACESTA0	0000_0000h	32
96Ch to 99Ch	Reserved	—	—	—
PCI Express to AXI Access 1000h to 10FCh				
1000h	AXI Window Base 0 Register	PCI_RC_AWBASE0	0000_0000h	32
1004h	AXI Window Mask 0 Register	PCI_RC_AWMASK0	0000_0FFFh	32
1008h	AXI Destination 0 Register	PCI_RC_ADEST0	0000_0000h	32
100Ch	Reserved	—	—	—
1010h	AXI Window Base 1 Register	PCI_RC_AWBASE1	0000_0000h	32
1014h	AXI Window Mask 1 Register	PCI_RC_AWMASK1	0000_0FFFh	32
1018h	AXI Destination 1 Register	PCI_RC_ADEST1	0000_0000h	32
101Ch	Reserved	—	—	—
1020h	AXI Window Base 2 Register	PCI_RC_AWBASE2	0000_0000h	32
1024h	AXI Window Mask 2 Register	PCI_RC_AWMASK2	0000_0FFFh	32
1028h	AXI Destination 2 Register	PCI_RC_ADEST2	0000_0000h	32
102Ch	Reserved	—	—	—
1030h	AXI Window Base 3 Register	PCI_RC_AWBASE3	0000_0000h	32
1034h	AXI Window Mask 3 Register	PCI_RC_AWMASK3	0000_0FFFh	32
1038h	AXI Destination 3 Register	PCI_RC_ADEST3	0000_0000h	32
103Ch	Reserved	—	—	—

Table 36.4-1 AXI Bridge Registers (4/5)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
1040h	AXI Window Base 4 Register	PCI_RC_AWBASE4	0000_0000h	32
1044h	AXI Window Mask 4 Register	PCI_RC_AWMASK4	0000_0FFFh	32
1048h	AXI Destination 4 Register	PCI_RC_ADEST4	0000_0000h	32
104Ch	Reserved	—	—	—
1050h	AXI Window Base 5 Register	PCI_RC_AWBASE5	0000_0000h	32
1054h	AXI Window Mask 5 Register	PCI_RC_AWMASK5	0000_0FFFh	32
1058h	AXI Destination 5 Register	PCI_RC_ADEST5	0000_0000h	32
105Ch	Reserved	—	—	—
1060h	AXI Window Base 6 Register	PCI_RC_AWBASE6	0000_0000h	32
1064h	AXI Window Mask 6 Register	PCI_RC_AWMASK6	0000_0FFFh	32
1068h	AXI Destination 6 Register	PCI_RC_ADEST6	0000_0000h	32
106Ch	Reserved	—	—	—
1070h	AXI Window Base 7 Register	PCI_RC_AWBASE7	0000_0000h	32
1074h	AXI Window Mask 7 Register	PCI_RC_AWMASK7	0000_0FFFh	32
1078h	AXI Destination 7 Register	PCI_RC_ADEST7	0000_0000h	32
107Ch to 10FCh	Reserved	—	—	—
AXI to PCI Express Access 1100h to 11FCh				
1100h	PCIe Window Base 0 Register	PCI_RC_PWBASE0	0000_0000h	32
1104h	PCIe Window Mask 0 Register	PCI_RC_PWMASK0	0000_0FFFh	32
1108h	PCIe Destination 0 (Lower) Register	PCI_RC_PDESTLO0	0000_0000h	32
110Ch	PCIe Destination 0 (Upper) Register	PCI_RC_PDESTUP0	0000_0000h	32
1110h	PCIe Window Base 1 Register	PCI_RC_PWBASE1	0000_0000h	32
1114h	PCIe Window Mask 1 Register	PCI_RC_PWMASK1	0000_0FFFh	32
1118h	PCIe Destination 1 (Lower) Register	PCI_RC_PDESTLO1	0000_0000h	32
111Ch	PCIe Destination 1 (Upper) Register	PCI_RC_PDESTUP1	0000_0000h	32
1120h	PCIe Window Base 2 Register	PCI_RC_PWBASE2	0000_0000h	32
1124h	PCIe Window Mask 2 Register	PCI_RC_PWMASK2	0000_0FFFh	32
1128h	PCIe Destination 2 (Lower) Register	PCI_RC_PDESTLO2	0000_0000h	32
112Ch	PCIe Destination 2 (Upper) Register	PCI_RC_PDESTUP2	0000_0000h	32
1130h	PCIe Window Base 3 Register	PCI_RC_PWBASE3	0000_0000h	32
1134h	PCIe Window Mask 3 Register	PCI_RC_PWMASK3	0000_0FFFh	32
1138h	PCIe Destination 3 (Lower) Register	PCI_RC_PDESTLO3	0000_0000h	32
113Ch	PCIe Destination 3 (Upper) Register	PCI_RC_PDESTUP3	0000_0000h	32
1140h	PCIe Window Base 4 Register	PCI_RC_PWBASE4	0000_0000h	32
1144h	PCIe Window Mask 4 Register	PCI_RC_PWMASK4	0000_0FFFh	32
1148h	PCIe Destination 4 (Lower) Register	PCI_RC_PDESTLO4	0000_0000h	32
114Ch	PCIe Destination 4 (Upper) Register	PCI_RC_PDESTUP4	0000_0000h	32
1150h	PCIe Window Base 5 Register	PCI_RC_PWBASE5	0000_0000h	32
1154h	PCIe Window Mask 5 Register	PCI_RC_PWMASK5	0000_0FFFh	32
1158h	PCIe Destination 5 (Lower) Register	PCI_RC_PDESTLO5	0000_0000h	32
115Ch	PCIe Destination 5 (Upper) Register	PCI_RC_PDESTUP5	0000_0000h	32
1160h	PCIe Window Base 6 Register	PCI_RC_PWBASE6	0000_0000h	32
1164h	PCIe Window Mask 6 Register	PCI_RC_PWMASK6	0000_0FFFh	32
1168h	PCIe Destination 6 (Lower) Register	PCI_RC_PDESTLO6	0000_0000h	32
116Ch	PCIe Destination 6 (Upper) Register	PCI_RC_PDESTUP6	0000_0000h	32

Table 36.4-1 AXI Bridge Registers (5/5)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
1170h	PCIe Window Base 7 Register	PCI_RC_PWBASE7	0000_0000h	32
1174h	PCIe Window Mask 7 Register	PCI_RC_PWMASK7	0000_0FFFh	32
1178h	PCIe Destination 7 (Lower) Register	PCI_RC_PDESTLO7	0000_0000h	32
117Ch	PCIe Destination 7 (Upper) Register	PCI_RC_PDESTUP7	0000_0000h	32
1180h to 1FFCh	Reserved*2	—	—	—

Note: Debug: Registers for use in debugging by Renesas. Access to these registers may lead to a malfunction.
Reserved: Reserved registers. The results of access to these registers and operation of the core through such access are not guaranteed.

Note 1. The addresses listed in the above table are those for channel 0. These addresses should be read as the addresses for the other DMAC channels according to the table below.

Channel Offset Address	
offset + 000h	Channel 0
offset + 080h	Channel 1
offset + 100h	Channel 2
offset + 180h	Channel 3
offset + 200h	Channel 4
offset + 280h	Channel 5
offset + 300h	Channel 6
offset + 380h	Channel 7

Example)

Channel 0: DMA Descriptor Control Register (offset: 920h = 920h + 000h)
Channel 1: DMA Descriptor Control Register (offset: 9A0h = 920h + 080h)
Channel 2: DMA Descriptor Control Register (offset: A20h = 920h + 100h)
Channel 3: DMA Descriptor Control Register (offset: AA0h = 920h + 180h)
Channel 4: DMA Descriptor Control Register (offset: B20h = 920h + 200h)
Channel 5: DMA Descriptor Control Register (offset: BA0h = 920h + 280h)
Channel 6: DMA Descriptor Control Register (offset: C20h = 920h + 300h)
Channel 7: DMA Descriptor Control Register (offset: CA0h = 920h + 380h)

Note 2. Though the address range from 1200h to 13FCh includes the AXI bridge registers for endpoint, access to this area is prohibited (the address configuration of the AXI bridge registers does not vary whether operation is as a root complex or endpoint).

36.4.2 List of PCI Express Configuration Registers

36.4.2.1 Type 1 (for Root Complex)

The table below lists the PCI Express configuration registers.

Table 36.4-2 PCI Express Configuration Registers (1/3)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
Common Configuration Space				
6000h	Vendor and Device ID	PCI_RC_VID	Configurable value	32
6004h	Command and Status	PCI_RC_COM_STA	0010_0000h	32
6008h	Revision ID and Class Code	PCI_RC_RID_CC	Configurable value	32
600Ch	Cache Line and Header Type	PCI_RC_CL_HT	0001_0000h	32
Configuration Space				
6010h	Base Address Register 0	PCI_RC_BAR0	0000_0004h	32
6014h	Base Address Register 1	PCI_RC_BAR1	0000_0000h	32
6018h	Bus Number Register	PCI_RC_BNR	0000_0000h	32
601Ch	I/O Base/Limit and Secondary Status	PCI_RC_IOBL_SS	0000_0000h	32
6020h	Memory Base/Limit Register	PCI_RC_MEMBL	FFF0_FFF0h	32
6024h	Prefetchable Memory Base/Limit Register	PCI_RC_PMBL	0001_0001h	32
6028h	Prefetchable Base Upper 32bits Register	PCI_RC_PBUP32	0000_0000h	32
602Ch	Prefetchable Limit Upper 32bits Register	PCI_RC_PLUP32	0000_0000h	32
6030h	I/O Base/Limit Upper 16bits Register	PCI_RC_IOBLUP16	0000_0000h	32
6034h	Capability Pointer	PCI_RC_CP	0000_0040h	32
6038h	Expansion ROM Base Address	PCI_RC_EROMBA	0000_0000h	32
603Ch	Bridge Control and Interrupt	PCI_RC_BC_INT	0000_0000h	32
PCI Power Management Capability Structure				
6040h	PM Capabilities	PCI_RC_PMC	4803_6001h	32
6044h	PM Status/Control	PCI_RC_PMSC	0000_0008h	32
6048h to 605Ch	Reserved	—	—	—
PCI Express Capability Structure				
6060h	PCI Express Capability	PCI_RC_PCIEC	0042_0010h	32
6064h	Device Capabilities	PCI_RC_DEVC	0000_8000h	32
6068h	Device Control/Status	PCI_RC_DEVCS	0000_2010h	32
606Ch	Link Capabilities	PCI_RC_LINKC	0073_6C22h	32
6070h	Link Control/Status	PCI_RC_LINKCS	1000_0008h	32
6074h	Slot Capabilities	PCI_RC_SLOTC	0000_0000h	32
6078h	Slot Control/Status	PCI_RC_SLOTCS	0040_0000h	32
607Ch	Root Control/Capabilities	PCI_RC_ROOTCC	0000_0000h	32
6080h	Root Status	PCI_RC_ROOTS	0000_0000h	32
6084h	Device Capabilities 2	PCI_RC_DEVC2	0000_0012h	32
6088h	Device Control 2/Status 2	PCI_RC_DEVCS2	0000_0000h	32
608Ch	Link Capabilities 2	PCI_RC_LINKC2	0000_0006h	32
6090h	Link Control 2/Status 2	PCI_RC_LINCS2	0000_0002h	32
6094h	Slot Capabilities 2	PCI_RC_SLOTC2	0000_0000h	32

Table 36.4-2 PCI Express Configuration Registers (2/3)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
6098h	Slot Control 2/Status 2	PCI_RC_SLOTCS2	0000_0000h	32
609Ch	Reserved	—	—	—
Specific Registers				
60A0h	Base Address Register Mask 00 (Lower)	PCI_RC_BARMSK00L	0FFF_FFFFh *1	32
60A4h	Base Address Register Mask 00 (Upper)	PCI_RC_BARMSK00U	0000_0000h*1	32
60A8h	Base Address Register Mask 01 (Lower)	PCI_RC_BARMSK01L	0000_0000h	32
60ACh	Base Address Register Mask 01 (Upper)	PCI_RC_BARMSK01U	0000_0000h	32
60B0h	Base Address Register Mask 02 (Lower)	PCI_RC_BARMSK02L	0000_1FFFh	32
60B4h	Base Address Register Mask 02 (Upper)	PCI_RC_BARMSK02U	0000_0000h	32
60B8h to 60C4h	Debug	—	—	—
60C8h	Base Size 00/01	PCI_RC_BSIZE00_01	0000_0000h	32
60CCh	Base Size 02/03	PCI_RC_BSIZE02_03	0000_0000h	32
60D0h	Base Size 04/05	PCI_RC_BSIZE04_05	0000_0000h	32
60D4h	Base Size 06	PCI_RC_BSIZE06	0000_0000h	32
60D8h	Type Supported 00/01/02	PCI_RC_TSUPPORT00_01_02	0033_3333h	32
60DCh	Debug	—	—	—
60E0h to 60FCh	Reserved	—	—	—
Advanced Error Reporting (AER) Capability				
6100h	Advanced Error Reporting Capability	PCI_RC_ADVERC	1501_0001h	32
6104h	Uncorrectable Error Status Register	PCI_RC_UNCESTS	0000_0000h	32
6108h	Uncorrectable Error Mask Register	PCI_RC_UNCEMASK	0000_0000h	32
610Ch	Uncorrectable Error Severity Register	PCI_RC_UNCESVY	0046_2030h	32
6110h	Correctable Error Status Register	PCI_RC_CESTS	0000_0000h	32
6114h	Correctable Error Mask Register	PCI_RC_CEMASK	0000_2000h	32
6118h	Advanced Error Capabilities and Control Register	PCI_RC_ADVECC	0000_00A0h	32
611Ch	Header Log Register 0	PCI_RC_HLOG0	0000_0000h	32
6120h	Header Log Register 1	PCI_RC_HLOG1	0000_0000h	32
6124h	Header Log Register 2	PCI_RC_HLOG2	0000_0000h	32
6128h	Header Log Register 3	PCI_RC_HLOG3	0000_0000h	32
612Ch	Root Error Command	PCI_RC_ROOTEC	0000_0000h	32
6130h	Root Error Status	PCI_RC_ROOTES	0000_0000h	32
6134h	Error Source Identification Register	PCI_RC_ERRSI	0000_0000h	32
6138h to 614Ch	Reserved	—	—	—
Device Serial Number Capability				
6150h	Device Serial Number Extended Capability	PCI_RC_DEVSNEXTC	0001_0003h	32
6154h	Serial Number Register (Lower DW)	PCI_RC_SNL	0000_0000h	32
6158h	Serial Number Register (Upper DW)	PCI_RC_SNU	0000_0000h	32
615Ch	Reserved	—	—	—
6160h				
616Ch	Debug	—	—	—
6170h to 618Ch	Reserved	—	—	—
6190h				
6194h	Debug	—	—	—

Table 36.4-2 PCI Express Configuration Registers (3/3)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
6098h	Slot Control 2/Status 2	PCI_RC_SLOTCS2	0000_0000h	32
6198h to 6FFCh	Reserved	—	—	—

Note: “Specific Registers” refers to registers specific to this unit.

Note 1. Writing all 1b’s is recommended in the initial settings for operation as a root complex.

36.4.3 Register Descriptions (Root Complex Mode)

The function description of each register is given below.

36.4.3.1 AXI Bridge Registers

(1) Request Data Register m (PCI_RC_REQDATAm) (m = 0 to 2)

This register issues various requests.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0080h (m = 0)
<PCI_S0_REG_base> + 0084h (m = 1)
<PCI_S0_REG_base> + 0088h (m = 2)

Initial Value: xxxx_xxxxh

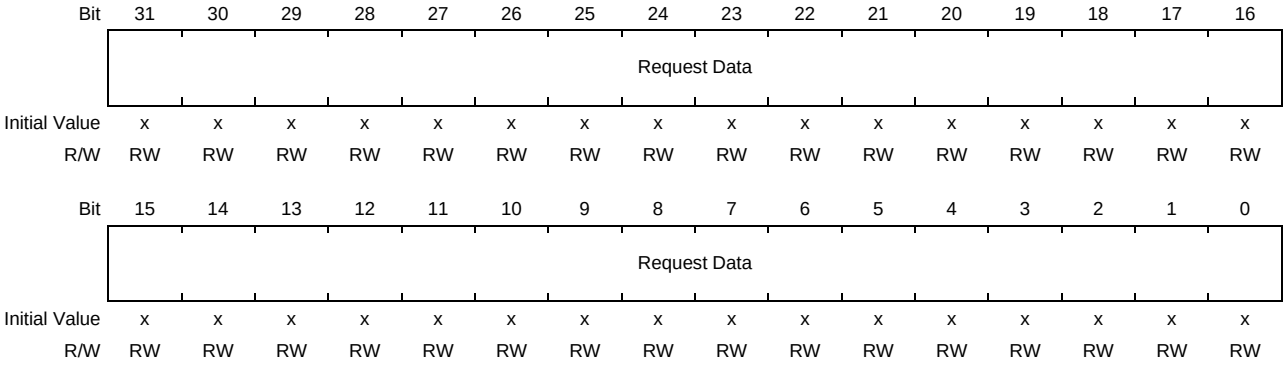


Table 36.4-3 PCI_RC_REQDATAm Register Contents

Bit Position	Bit Name	Description
31 to 0	Request Data	Set write data for issuing a request.

Table 36.4-4

	Request Data Register 0	Request Data Register 1	Request Data Register 2
Zero-Length Read Request	Invalid	Invalid	Invalid
Config Write	Invalid	Invalid	Write data
Config Read	Invalid	Invalid	Invalid
Message Request	3rd Header	4th Header	Invalid
Message Request with data payload	3rd Header	4th Header	Message data

Note: The bits should be set to 0 for the requests indicated as “Invalid”.

(2) Request Receive Data Register (PCI_RC_REQRCVDAT)

This register indicates the data read on reception of the completion response after issuing a read request.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 008Ch

Initial Value: xxxx_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Request Receive Data															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Request Receive Data															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-5 PCI_RC_REQRCVDAT Register Contents

Bit Position	Bit Name	Description
31 to 0	Request Receive Data	After issuing a read request, the data read on reception of the completion response are set in these bits. However, these bits are invalid for any kind of write request.

(3) Request Address Register 1 (PCI_RC_REQADR1)

This register issues requests.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0090h

Initial Value: xxxx_xxxxh

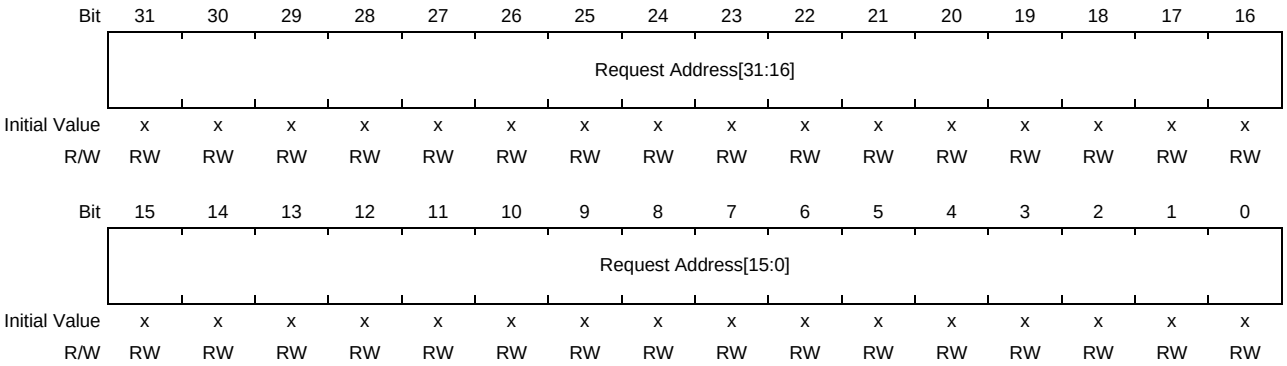


Table 36.4-6 PCI_RC_REQADR1 Register Contents

Bit Position	Bit Name	Description
31 to 0	Request Address [31:0]	Set the address and so forth for use in issuing requests.

Table 36.4-7

	[31:27]	[26:24]	[23:19]	[18:16]
Zero-Length Read Request	Address			
Config Write	Bus number		Reserved	Function number
Config Read	Bus number		Reserved	Function number
Message Request	Reserved	Routing type	Reserved	Reserved
Message Request with data payload	Reserved	Routing type	Reserved	Reserved

	[15:12]	[11:8]	[7:2]	[1:0]
Zero-Length Read Request	Address			Reserved
Config Write	Reserved	Ext. Reg. number	Register number	Reserved
Config Read	Reserved	Ext. Reg. number	Register number	Reserved
Message Request	Reserved	Reserved	Message code	
Message Request with data payload	Reserved	Reserved	Message code	

Note: The bits should be set to 0 for the requests indicated as “Reserved”.

(4) Request Address Register 2 (PCI_RC_REQADR2)

This register issues requests.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0094h

Initial Value: xxxx_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Request Address[63:48]															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Request Address[47:32]															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.4-8 PCI_RC_REQADR2 Register Contents

Bit Position	Bit Name	Description
31 to 0	Request Address [63:32]	Set the address and so forth for use in issuing requests.

Table 36.4-9

	[31:0]
Zero-Length Read Request	Address
Config Write	Invalid
Config Read	Invalid
Message Request	Invalid
Message Request with data payload	Invalid

Note: The bits should be set to 0 for the requests indicated as “Invalid”.

(5) Request Byte Enable Register (PCI_RC_REQBE)

This register specifies the 1st DW byte enable bit of the TLP header when issuing a request to PCIe.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0098h

Initial Value: 0000_000Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	Request Byte Enable			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 36.4-10 PCI_RC_REQBE Register Contents

Bit Position	Bit Name	Description
31 to 4	—	Reserved. These bits are read as 0b.
3 to 0	Request Byte Enable	Specify byte enabling in the issuing of IO/Cfg requests as required. Normally used with 1111b. 1b: Enable byte. 0b: Disable byte.

Table 36.4-11

	[3:0]
Zero-Length Read Request	0000b
Config Write	Random (Usually 1111b)
Config Read	Random (Usually 1111b)
Message Request	Invalid (1111b)
Message Request with data payload	Invalid (1111b)

(6) Request Issue Register (PCI_RC_REQISS)

This register is for setting up the issuing of requests to PCIe.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 009Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	Request Rejection	MOR CD PERR	MOR CH PERR	MOR EP ERR	MOR_STATUS		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	FUNC			TR Type				—	—	—	—	—	—	—	Request Issue
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	RW

Table 36.4-12 PCI_RC_REQISS Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b.
22	Request Rejection	Indicates that processing has been forcibly terminated in response to detection of the PCI Express transmission (TX) side being stopped or suspended. 0b: Normal state (a request is issued) 1b: Forced termination (rejection)
21	MOR CD PERR	Set to 1b if a data error occurs in the completion TLP for a non-posted request issued by this register. Not normally used. It is not updated at the time of a posted request.
20	MOR CH PERR	Set to 1b if a header error occurs in the completion TLP for a non-posted request issued by this register. Not normally used. It is not updated at the time of a posted request.
19	MOR EP ERR	Set to 1b if a poisoned completion TLP for a non-posted request issued by this register is received. Not normally used. It is not updated at the time of a posted request.
18 to 16	MOR_STATUS	Hold the MOR status in the completion TLP for a non-posted request issued by this register. It is not updated at the time of a posted request. 000b: Successful Completion (SC) 001b: Unsupported Request (UR) 010b: Configuration Request Retry Status (CRS) (not supported) 011b: Completion Timeout 100b: Completer Abort (CA) 101b: Unexpected Completion and mismatched type (Lock Completion response to non-Lock request) 110b: Reserved 111b: Overrun Completion length
15	—	Fixed to 0b.
14 to 12	FUNC	Set the function of requests.
11 to 8	TR Type	Set the request type (see **Table 36.4-13**).
7 to 1	—	Fixed to 0b.

Table 36.4-12 PCI_RC_REQISS Register Contents (2/2)

Bit Position	Bit Name	Description
0	Request Issue	When written: 1b: Issue a request. 0b: No operation When read: 1b: A request is being processed (indicating that the issued request is being processed). 0b: Issuing a request is acceptable (indicating that processing of the issued request has been completed).

Table 36.4-13

	TR Type		Device Type	
	[11:8]	Posted/Non-Posted	Root Complex	Endpoint
Zero-Length Read Request	0000b (0h)	Non-posted	Issuable	Issuable
Configuration Read Type0	0100b (4h)	Non-posted	Issuable	Issuing prohibited
Configuration Write Type0	0101b (5h)	Non-posted	Issuable	Issuing prohibited
Configuration Read Type1	0110b (6h)	Non-posted	Issuable	Issuing prohibited
Configuration Write Type1	0111b (7h)	Non-posted	Issuable	Issuing prohibited
Message Request	1000b (8h)	Posted	Issuable	Issuable
Message Request with data payload	1001b (9h)	Posted	Issuable	Issuable
	Others	—	Issuing prohibited	Issuing prohibited

(7) MSI Receive Window Address Register (PCI_RC_MSIRCVWADR)

This register sets the receive MSI memory area start address.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0100h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSI Receive Window Address[31:3]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSI Receive Window Address[31:3]													—	—	MSI Receive Window Enable
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	RW

Table 36.4-14 PCI_RC_MSIRCVWADR Register Contents

Bit Position	Bit Name	Description
31 to 3	MSI Receive Window Address [31:3]	The address should be aligned with the size set in the MSI Receive Mask bits. When a non-aligned address is set, the address bits for which the MSI Receive Window Mask bits have been set become 0. * To change this register, set the MSI Receive Window Enable bit to 0b.
2, 1	—	Reserved. These bits are read as 0b.
0	MSI Receive Window Enable	Enable the MSI receive window. 0b: Disable the window. 1b: Enable the window.

(8) MSI Receive Window Mask Register (PCI_RC_MSIRCVWMSK)

This register specifies the size of the area from the address set in the MSI Receive Window Address bits.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0108h

Initial Value: 0000_0003h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSI Receive Window Mask[31:2]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSI Receive Window Mask[31:2]														MSI Receive Window Mask[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R

Table 36.4-15 PCI_RC_MSIRCVWMSK Register Contents

Bit Position	Bit Name	Description
31 to 2	MSI Receive Window Mask[31:2]	Set the lower bits of the reserved area to 1b (min. 4-byte space; max. 4-Gbyte space). Example settings are as follows. 0h: 4-byte space 1b: 8-byte space 7fh: 2048-byte space *Note*: To change this register, set the MSI Receive Window Enable bit to 0b.
1, 0	MSI Receive Window Mask[1:0]	Fixed to 11b. The MSI Receive Window Mask [1:0] bits are always masked.

(9) PCI INTx Receive Interrupt Enable Register (PCI_RC_PINTRCVIE)

This register enables INTx_RC interrupts.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0110h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	MSI Receive Interrupt Enable	INTD Receive Interrupt Enable	INTC Receive Interrupt Enable	INTB Receive Interrupt Enable	INTA Receive Interrupt Enable
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW1	RW1	RW1	RW1	RW1

Table 36.4-16 PCI_RC_PINTRCVIE Register Contents

Bit Position	Bit Name	Description
31 to 5	—	Reserved. These bits are read as 0b.
4	MSI Receive Interrupt Enable	Permit INTMSI_RC in response to reception of an MSI. 0b: Disable 1b: Enable
3	INTD Receive Interrupt Enable	Permit INTD in response to reception of an MSI. 0b: Disable 1b: Enable
2	INTC Receive Interrupt Enable	Permit INTC in response to reception of an MSI 0b: Disable 1b: Enable
1	INTB Receive Interrupt Enable	Permit INTB in response to reception of an MSI. 0b: Disable 1b: Enable
0	INTA Receive Interrupt Enable	Permit INTA in response to reception of an MSI. 0b: Disable 1b: Enable

(10) PCI INTx Receive Interrupt Status Register (PCI_RC_PINTRCVIS)

This register indicates the INTx_RC interrupt factor. When Assert_INTx is received in response to a message request from PCIe, the corresponding bit in this register is set and interrupt INTx_RC is asserted. When Deassert_INTx is received in response to a message request, the corresponding bit in this register is cleared and interrupt INTx_RC is de-asserted. This register can be cleared by writing 1b by software. However, we do not recommend that software clears this interrupt bit on PCIe during normal operation. The fields of this register are set if each factor is detected, regardless of the setting of the PCI_INTx_Receive_Interrupt_Enable register for RC.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0114h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	MSI Receive Interrupt Status	INTD Receive Interrupt Status	INTC Receive Interrupt Status	INTB Receive Interrupt Status	INTA Receive Interrupt Status
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW1	RW1	RW1	RW1	RW1

Table 36.4-17 PCI_RC_PINTRCVIS Register Contents

Bit Position	Bit Name	Description
31 to 5	—	Reserved. These bits are read as 0b.
4	MSI Receive Interrupt Status	This bit is set when a memory write request is received from PCIe in the area for which the MSI receive window is set, an MSI is issued to the AXI as a write transaction, and a response to this is returned.
3	INTD Receive Interrupt Status	Set in response to reception of an assert INTD message. Cleared by Deassert INTD Message reception or by writing 1b.
2	INTC Receive Interrupt Status	Set in response to reception of an assert INTC message. Cleared in response to reception of a deassert INTC message or by writing 1b.
1	INTB Receive Interrupt Status	Set in response to reception of an assert INTB message. Cleared in response to reception of a deassert INTB message or by writing 1b.
0	INTA Receive Interrupt Status	Set in response to reception of an assert INTA message. Cleared in response to reception of a deassert INTA message or by writing 1b.

(11) Message Receive Interrupt Enable Register (PCI_RC_MSGRCVIE)

This register controls enabling of MSG_INT in response to the reception of message requests other than INTx and error-related messages.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0120h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	Message Receive Interrupt Enable	—	—	—	—	PM_Active_State_Nak Receive Interrupt Enable	PM_PME Receive Interrupt Enable	PME_Turn_Off Receive Interrupt Enable	PME_TO_Ack Receive Interrupt Enable
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	R	R	R	R	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-18 PCI_RC_MSGRCVIE Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24	Message Receive Interrupt Enable	Enables assertion of MSG_INT in response to reception of a message. 0b: Disable 1b: Enable
23 to 20	—	Reserved. These bits are read as 0b.
19	PM_Active_State_Nak Receive Interrupt Enable	Enables assertion of MSG_INT in response to reception of PM_Active_State_Nak. 0b: Disable 1b: Enable
18	PM_PME Receive Interrupt Enable	Enables assertion of MSG_INT in response to reception of PM_PME. 0b: Disable 1b: Enable
17	PME_Turn_Off Receive Interrupt Enable	Enables assertion of MSG_INT in response to reception of PME_Turn_Off. 0b: Disable 1b: Enable
16	PME_TO_Ack Receive Interrupt Enable	Enables assertion of MSG_INT in response to reception of PME_TO_Ack. 0b: Disable 1b: Enable
15 to 0	—	Fixed to 0b.

(12) Message Receive Interrupt Status Register (PCI_RC_MSGRCVIS)

This register is a status register that indicates the reception of message requests other than INTx and error-related messages. The value of this register is reflected in MSG_INT. Only the message code is used to judge the message type. The validity of routing and validity of Msg/MsgD selection are not verified. The corresponding message is considered to have been received.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0124h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	Message Receive Interrupt	—	—	—	—	PM_Active_State_Nak Receive Interrupt	PM_PME Receive Interrupt	PME_Turn_Off Receive Interrupt	PME_TO_Ack Receive Interrupt
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	R	R	R	R	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-19 PCI_RC_MSGRCVIS Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24	Message Receive Interrupt	Set in response to the reception of a message (regardless of the message type). It is cleared by writing 1b. Writing 0b has no effect.
23 to 20	—	Reserved. These bits are read as 0b.
19	PM_Active_State_Nak Receive Interrupt	Invalid due to RC.
18	PM_PME Receive Interrupt	Set in response to the reception of a PM_PME message. It is cleared by writing 1b. Writing 0b has no effect.
17	PME_Turn_Off Receive Interrupt	Invalid due to RC.
16	PME_TO_Ack Receive Interrupt	Set in response to the reception of a PME_TO_Ack message. It is cleared by writing 1b. Writing 0b has no effect.
15 to 0	—	Reserved. These bits are read as 0b.

(13) Message Code Register (PCI_RC_MSGCODE)

This register stores the code and routing of the last received message.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0130h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Message Code								Routing			—	—	—	—	Message Payload
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-20 PCI_RC_MSGCODE Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15 to 8	Message Code	Stores the code of the last received message.
7 to 5	Routing	Stores routing of the last received message.
4 to 1	—	Reserved. These bits are read as 0b.
0	Message Payload	Stores the presence or absence of the data payload of the last received message. 1b: MsgD (with payload) 0b: Msg (without payload)

Note: When a Power Management message (PME_TO_Ack Message, PME_Turn_Off Message, PM_PME Message, PM_Active_State_Nak Message) is received, this register is not written.

(14) Message Data Register (PCI_RC_MSGDATA)

This register stores the data of the last received message.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0134h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Message Data															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Message Data															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-21 PCI_RC_MSGDATA Register Contents

Bit Position	Bit Name	Description
31 to 0	Message Data	Stores the first DW data of the last received message. Updated only when MsgD (with data) is received, and retains previous data when Msg (without data) is received

Note: When a Power Management message (PME_TO_Ack Message, PME_Turn_Off Message, PM_PME Message, PM_Active_State_Nak Message) is received, this register is not written.

(15) Message Header 3rdDW Register (PCI_RC_MSGH3DW)

This register stores the header (the 3rd DW) of the last received message.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0138h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Message Header 3rd DW															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Message Header 3rd DW															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-22 PCI_RC_MSGH3DW Register Contents

Bit Position	Bit Name	Description
31 to 0	Message Header 3rd DW	Stores the header (the 3rd DW) of the last received message.

Note: When a Power Management message (PME_TO_Ack Message, PME_Turn_Off Message, PM_PME Message, PM_Active_State_Nak Message) is received, this register is not written.

(16) Message Header 4thDW Register (PCI_RC_MSGH4DW)

This register stores the header (the 4th DW) of the last received message.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 013Ch

Initial Value: 0000_0000h

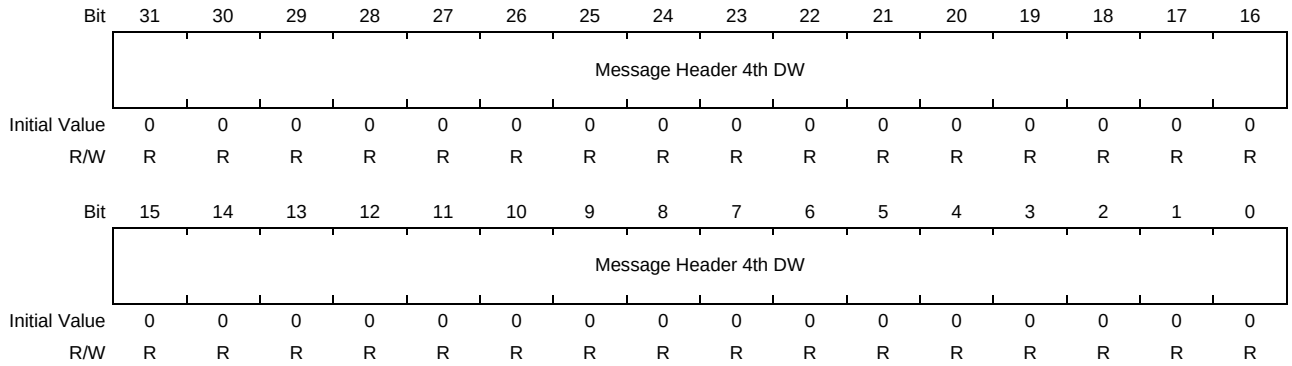


Table 36.4-23 PCI_RC_MSGH4DW Register Contents

Bit Position	Bit Name	Description
31 to 0	Message Header 4th DW	Stores the header (the 4th DW) of the last received message.

Note: When a Power Management message (PME_TO_Ack Message, PME_Turn_Off Message, PM_PME Message, PM_Active_State_Nak Message) is received, this register is not written.

(17) Interrupt Table Register (PCI_RC_INTTABLE)

The interrupt signal (active high) status of each category can be monitored in a list.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0140h

Initial Value: 00xx_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Debug															
Initial Value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Debug	—	—	—	Debug	AXI_ERR_INT	PCIE_EVT _INT	MSG_INT	—	—	—	INTMSI_RC	INTD_RC	INTC_RC	INTB_RC	INTA_RC
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-24 PCI_RC_INTTABLE Register Contents

Bit Position	Bit Name	Description
31 to 15	Debug	Debug register
14 to 12	—	Reserved. These bits are read as 0b.
11	Debug	Debug register
10	AXI_ERR_INT	Error interrupt monitor register
9	PCIE_EVT _INT	Event interrupt monitor register
8	MSG_INT	Message interrupt monitor register
7 to 5	—	Reserved. These bits are read as 0b.
4	INTMSI_RC	INT_MSI reception interrupt monitor register
3	INTD_RC	INTD_RC reception interrupt monitor register
2	INTC_RC	INTC_RC reception interrupt monitor register
1	INTB_RC	INTB_RC reception interrupt monitor register
0	INTA_RC	INTA_RC reception interrupt monitor register

Note: See the description of the terminal of the same name for details of the register.
Debug: Registers for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.

(18) PCIe Event Interrupt Enable 0 Register (PCI_RC_PEIE0)

This register enables interrupts of the various PCI Express event factors. This register enables writing to the PCIe Event Interrupt Status 0 Register (address: <PCI_S0_REG_base> + 0204h). See the description of this status register for details of the factors.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0200h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	UI_LINK_WIDTH_CHANG_DONE EN	UI_LINK_SPEED_CHANG_DONE EN	Request Done EN	—	—	Debug	CA EN	Debug		—	Debug				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	R	RW	RW	RW	RW	R	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Debug		—	RX_DLLP_PM_ENTER_L23 EN	Debug	ASPM L1 Rejected EN	DL_UpDown EN	—	Debug				—	—	—	Debug
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	R	RW	RW	RW	RW	R	RW	RW	RW	RW	R	R	R	RW

Table 36.4-25 PCI_RC_PEIE0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b.
30	UI_LINK_WIDTH_CHANGE_DONE EN	Up/Down configuration complete interrupt enable 0b: Disable 1b: Enable
29	UI_LINK_SPEED_CHANGE_DONE EN	Speed change complete interrupt enable 0b: Disable 1b: Enable
28	Request Done EN	Request complete interrupt enable 0b: Disable 1b: Enable
27, 26	—	Reserved. These bits are read as 0b.
25	Debug	Debug register
24	CA EN	CA (Completer Abort) interrupt enable 0b: Disable 1b: Enable
23, 22	Debug	Debug register
21	—	Reserved. This bit is read as 0b.
20 to 14	Debug	Debug register
13	—	Reserved. This bit is read as 0b.
12	RX_DLLP_PM_ENTER_L23 EN	RX_DLLP_PM_ENTER_L23 interrupt enable 0b: Disable 1b: Enable
11	Debug	Debug register

Table 36.4-25 PCI_RC_PEIE0 Register Contents (2/2)

Bit Position	Bit Name	Description
10	ASPM L1 Rejected EN	ASPM L1 Rejected interrupt enable 0b: Disable 1b: Enable
9	DL_UpDown EN	The DL state change interrupt enable 0b: Disable 1b: Enable
8	—	Reserved. This bit is read as 0b.
7 to 4	Debug	Debug register
3 to 1	—	Reserved. These bits are read as 0b.
0	Debug	Debug register

(19) PCIe Event Interrupt Status 0 Register (PCI_RC_PEIS0)

This register is a status register that indicates each PCI Express event. Set to 1b by the factor in the table. After checking the factor, write 1b to clear it.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0204h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	UI_LINK_WIDTH_CHANG_DONE	UI_LINK_SPEED_CHANG_DONE	Request Done	—	—	Debug	CA	Debug		—	Debug				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW1	RW1	RW1	R	R	RW1	RW1	RW1	RW1	R	RW1	RW1	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Debug		—	RX_DLLP_PM_TER_L23	Debug	ASPM L1 Rejected	DL_UpDown	—	Debug							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	RW1	R	RW1	RW1	RW1	RW1	R	RW1	RW1	RW1	RW1	R	R	R	RW1

Table 36.4-26 PCI_RC_PEIS0 Register Contents

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b.
30	UI_LINK_WIDTH_CHANGE_DONE	Indicates the completion of up/down configuration. It is cleared by writing 1b. Writing 0b has no effect.
29	UI_LINK_SPEED_CHANGE_DONE	Indicates the completion of a speed change. It is cleared by writing 1b. Writing 0b has no effect.
28	Request Done	Indicates the completion of the request. It is cleared by writing 1b. Writing 0b has no effect.
27, 26	—	Reserved. These bits are read as 0b.
25	Debug	Debug register
24	CA	Indicates a CA (completer abort) response to an other-party device. It is cleared by writing 1b. Writing 0b has no effect.
23, 22	Debug	Debug register
21	—	Reserved. This bit is read as 0b.
20 to 14	Debug	Debug register
13	—	Reserved. This bit is read as 0b.
12	RX_DLLP_PM_TER_L23	Indicates a transition to L2/L3 in power management control. It is cleared by writing 1b. Writing 0b has no effect.
11	Debug	Debug register
10	ASPM L1 Rejected	Indicates that a transition to ASPM L1 was rejected. It is cleared by writing 1b. Writing 0b has no effect.
9	DL_UpDown	If the DL_Down state is changed to the DL_UP state or the DL_Up state is changed to the DL_Down state, set to 1b. To check the DL_Down/DL_Up state, use the PCIe Core Status 1 Register (address: <PCI_S0_REG_base> + 0408h). It is cleared by writing 1b. Writing 0b has no effect.
8	—	Reserved. This bit is read as 0b.
7 to 0	Debug	Debug register

(20) PCIe Event Interrupt Enable 1 Register (PCI_RC_PEIE1)

This register enables parity error and ECC error interrupts. When each bit is set to valid, the value of each corresponding status bit of the PCIe event interrupt status 1 register (address: <PCI_S0_REG_base> + 020Ch) becomes valid.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0208h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXB_PARITY_ERR_EN	ERR_RPC_REPLAYFIFO_PERR_EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ERR_REPLAY_UPPER_CORRECTABLE_ERROR_EN	ERR_REPLAY_LOWER_CORRECTABLE_ERROR_EN	—	—	—	—	—	—	ERR_REPLAY_UPPER_UNCORRECTABLE_ERROR_EN	ERR_REPLAY_LOWER_UNCORRECTABLE_ERROR_EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	R	R	R	R	R	R	RW	RW

Table 36.4-27 PCI_RC_PEIE1 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 18	—	Reserved. These bits are read as 0b.
17	TXB_PARITY_ERR EN	Enables a TXB_PARITY_ERR interrupt. Enables notification of parity error interrupts in the Tx buffer mounted on the transaction layer. 0b: Disable 1b: Enable
16	ERR_RPC_REPLAYFIFO_PERR EN	Enables an ERR_RPC_REPLAYFIFO_PERR interrupt. Enables notification of parity error interrupts in the replay FIFO mounted on the data link layer. 0b: Disable 1b: Enable
15 to 10	—	Reserved. These bits are read as 0b.
9	ERR_REPLAY_UPPER_CORRECTABLE_ERROR EN	Enables an ERR_REPLAY_UPPER_CORRECTABLE_ERROR interrupt. Enables notification of ECC 1-bit error (correctable error) occurrence interrupts in the upper 64 bits of the data bus of the replay FIFO mounted on the data link layer. 0b: Disable 1b: Enable
8	ERR_REPLAY_LOWER_CORRECTABLE_ERROR EN	Enables an ERR_REPLAY_LOWER_CORRECTABLE_ERROR interrupt. Enables notification of ECC 1-bit error (correctable error) occurrence interrupts in the lower 64 bits of the data bus of the replay FIFO mounted on the data link layer. 0b: Disable 1b: Enable
7 to 2	—	Reserved. These bits are read as 0b.
1	ERR_REPLAY_UPPER_UNCORRECTABLE_ERROR EN	Enables an ERR_REPLAY_UPPER_CORRECTABLE_ERROR interrupt. Enables notification of ECC 2-bit or more error (uncorrectable error) occurrence interrupts in the upper 64 bits of the data bus of the replay FIFO mounted on the data link layer. 0b: Disable 1b: Enable

Table 36.4-27 PCI_RC_PEIE1 Register Contents (2/2)

Bit Position	Bit Name	Description
0	ERR_REPLAY_LOWER_UNCORRECTABLE_ERROR EN	Enables an ERR_REPLAY_LOWER_UNCORRECTABLE_ERROR interrupt. Enables notification of ECC 2-bit or more error (uncorrectable error) occurrence interrupts in the lower 64 bits of the data bus of the replay FIFO mounted on the data link layer. 0b: Disable 1b: Enable

(21) PCIe Event Interrupt Status 1 Register (PCI_RC_PEIS1)

This register is a status register that indicates parity error and ECC error interrupts. After checking the factor, write 1b to the corresponding bit clear it.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 020Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXB_PARITY_ERR	ERR_RPC_REPLAYFIFO_PERR
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ERR_REPLAY_UPPER_CORRECTABLE_ERROR	ERR_REPLAY_LOWER_CORRECTABLE_ERROR	—	—	—	—	—	—	ERR_REPLAY_UPPER_UNCORRECTABLE_ERROR	ERR_REPLAY_LOWER_UNCORRECTABLE_ERROR
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW1	RW1	R	R	R	R	R	R	RW1	RW1

Table 36.4-28 PCI_RC_PEIS1 Register Contents

Bit Position	Bit Name	Description
31 to 18	—	Reserved. These bits are read as 0b.
17	TXB_PARITY_ERR	TXB_PARITY_ERR interrupt. Notification of parity error interrupts in the Tx buffer mounted on the Transaction Layer. It is cleared by writing 1b. Writing 0b has no effect.
16	ERR_RPC_REPLAYFIFO_PERR	ERR_RPC_REPLAYFIFO_PERR interrupt. Notification of parity error interrupts in the replay FIFO mounted on the data link layer. It is cleared by writing 1b. Writing 0b has no effect.
15 to 10	—	Reserved. These bits are read as 0b.
9	ERR_REPLAY_UPPER_CORRECTABLE_ERROR	ERR_REPLAY_UPPER_CORRECTABLE_ERROR interrupt. Notification of ECC 1-bit error (correctable error) occurrence interrupts in the upper 64 bits of the data bus of the replay FIFO mounted on the data link layer. It is cleared by writing 1b. Writing 0b has no effect.
8	ERR_REPLAY_LOWER_CORRECTABLE_ERROR	ERR_REPLAY_LOWER_CORRECTABLE_ERROR interrupt. Notification of ECC 1-bit error (correctable error) occurrence interrupts in the lower 64 bits of the data bus of the replay FIFO mounted on the data link layer. It is cleared by writing 1b. Writing 0b has no effect.
7 to 2	—	Reserved. These bits are read as 0b.
1	ERR_REPLAY_UPPER_UNCORRECTABLE_ERROR	ERR_REPLAY_UPPER_CORRECTABLE_ERROR interrupt. Notification of ECC 2-bit error (correctable error) occurrence interrupts in the upper 64 bits of the data bus of the replay FIFO mounted on the data link layer. It is cleared by writing 1b. Writing 0b has no effect.
0	ERR_REPLAY_LOWER_UNCORRECTABLE_ERROR	ERR_REPLAY_LOWER_UNCORRECTABLE_ERROR interrupt. Notification of ECC 2-bit error (correctable error) occurrence interrupts in the lower 64 bits of the data bus of the replay FIFO mounted on the data link layer. It is cleared by writing 1b. Writing 0b has no effect.

(22) AXI Master Error Interrupt Enable Register (PCI_RC_AMEIE)

This register enables the AXI master error interrupt.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0210h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Write MSTERR INT EN[3:0]				—	—	—	—	Read MSTERR INT EN[3:0]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	R	R	R	R	RW	RW	RW	RW

Table 36.4-29 PCI_RC_AMEIE Register Contents

Bit Position	Bit Name	Description
31 to 12	—	Reserved. These bits are read as 0b.
11 to 8	Write MSTERR INT EN[3:0]	Enables a write MSTERR INT. Each of the corresponding bits is individually turned on/off. 0b: Disable 1b: Enable
7 to 4	—	Reserved. These bits are read as 0b.
3 to 0	Read MSTERR INT EN[3:0]	Enables a read MSTERR INT. Each of the corresponding bits is individually turned on/off. 0b: Disable 1b: Enable

(23) AXI Master Error Interrupt Status Register (PCI_RC_AMEIS)

This register indicates the AXI master error interrupt status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0214h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	Write ERR ID				—	—	—	—	Read ERR ID			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Write MSTERR INT EN[3:0]				—	—	—	—	Read MSTERR INT EN[3:0]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW1	RW1	RW1	RW1	R	R	R	R	RW1	RW1	RW1	RW1

Table 36.4-30 PCI_RC_AMEIS Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b.
27 to 24	Write ERR ID	Saves the ID on the first reception of DECERR or SLVERR. A new error ID can be saved when bits [11:8] are cleared. 0000b: Normal access.
23 to 20	—	Reserved. These bits are read as 0b.
19 to 16	Read ERR ID	Saves the ID on the first reception of DECERR or SLVERR. A new error ID can be saved when bits [3:0] are cleared. 0000b: Normal access.
15 to 12	—	Reserved. These bits are read as 0b.
11 to 8	Write MSTERR INT [3:0]	Indicates that an error was detected on the AXI master port. Only the first error detected is saved. A new error can be saved when bits [11:8] are cleared. Bit 11: Length error TEF does not match the length of the data transferred by the data channel. Bit 10: ID mismatch MAWID does not match MBID received by the response channel. Bit 9: DECERR is received. Bit 8: SLVERR is received. It is cleared by writing 1b. Writing 0b has no effect.
7 to 4	—	Reserved. These bits are read as 0b.
3 to 0	Read MSTERR INT [3:0]	Indicates that an error was detected on the AXI master port. Only the first error detected is saved. A new error can be saved when bits [3:0] are cleared. Bit 3: Length error TER does not match the length of the data transferred by the data channel. Bit 2: ID mismatch MARID does not match MRID received by the data channel. Bit 1: DECERR is received. Bit 0: SLVERR is received. It is cleared by writing 1b. Writing 0b has no effect.

(24) AXI Slave Error Interrupt Enable 1 Register (PCI_RC_ASEIE1)

This register enables the AXI slave error interrupt.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0220h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Write SLVERR INT EN[3:0]				—	—	—	—	—	—	Read SLVERR INT EN[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	R	R	R	R	R	R	RW	RW

Table 36.4-31 PCI_RC_ASEIE1 Register Contents

Bit Position	Bit Name	Description
31 to 12	—	Reserved. These bits are read as 0b.
11 to 8	Write SLVERR INT EN[3:0]	Enables a write MSTERR INT. Each of the corresponding bits is individually turned on/off. 0b: Disable 1b: Enable
7 to 2	—	Reserved. These bits are read as 0b.
1, 0	Read SLVERR INT EN[1:0]	Enables a read MSTERR INT. Each of the corresponding bits is individually turned on/off. 0b: Disable 1b: Enable

(25) AXI Slave Error Interrupt Status 1 Register (PCI_RC_ASEIS1)

This register indicates the AXI slave error interrupt status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0224h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Write SLVERR INT[3:0]				—	—	—	—	—	—	Read SLVERR INT[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW1	RW1	RW1	RW1	R	R	R	R	R	R	RW1	RW1

Table 36.4-32 PCI_RC_ASEIS1 Register Contents

Bit Position	Bit Name	Description
31 to 12	—	Reserved. These bits are read as 0b.
11 to 8	Write SLVERR INT [3:0]	Indicates that an unrecoverable error was detected on the AXI slave port (the response to the transaction is SLVERR). Bit 11: Burst length error SAWLEN does not match the burst length of the data received by the data channel. Bit 10: ID mismatch SAWID does not match SWID received by the data channel. Bit 9: Burst type invalid SAWBURST is 11b (undefined). When SAWBURST is 10b (wrapping) and the burst length is other than 2, 4, 8, and 16. Bit 8: Data size invalid SAWSIZE is 100b to 111b (greater than the AXI bus width or not supported). Each bit means the following. 0b: No error detected 1b: Error detected It is cleared by writing 1b. Writing 0b has no effect.
7 to 2	—	Reserved. These bits are read as 0b.
1, 0	Read SLVERR INT [1:0]	Indicates that an unrecoverable error was detected on the AXI slave port (the response to the transaction is SLVERR). Bit 1: Burst type invalid SAWBURST is 11b (undefined). When SAWBURST is 10b (wrapping) and the burst length is other than 2, 4, 8, and 16. Bit 0: Data size invalid SAWSIZE is 100b to 111b (greater than the AXI bus width or not supported). Each bit means the following. 0b: No error detected 1b: Error detected These bits are cleared by writing 1b. Writing 0b has no effect.

(26) AXI Slave Error Interrupt Status 3 Register (PCI_RC_ASEIS3)

This register indicates the AXI ID at the time of the first AXI slave error.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0230h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ERR ID															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR ID															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-33 PCI_RC_ASEIS3 Register Contents

Bit Position	Bit Name	Description
31 to 0	ERR ID	Saves the ID at the time of the first error of the AXI Slave Error Interrupt Status 1 register (address: 8503_0224h). Only the first error is saved. A new error ID can be saved when bits [11:8] and bits [1:0] of the AXI Slave Error Interrupt Status 1 register are cleared.

(27) Permission Register (PCI_RC_PERM)

This register controls access to the CFGU register.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0300h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	CFG_HWINIT_EN	Debug	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 36.4-34 PCI_RC_PERM Register Contents

Bit Position	Bit Name	Description
31 to 3	—	Reserved. These bits are read as 0b.
2	CFG_HWINIT_EN	Output to the CFG_HWINIT_EN pin. Used for register access control in CFGU.
1, 0	Debug	Debug register

(28) Reset Register (PCI_RC_RESET)

This register resets the PCIe core. Supplied to the internal core by OR with the pin of the same name. For details of each pin, see the terminal information. The write value is saved when accessed from the AXI side, but a low-level pulse is generated when the PCIe writes 0b. However, when the AXI has already written 0b, the signal remains at the low level. Writing 1b by the PCIe is ignored.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0310h

Initial Value: 0000_00xxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	force to D0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Debug				RST_PREG_B	RST_OUT_B	RST_PS_B	RST_LOAD_B	RST_CFG_B	RST_RSM_B	RST_GP_B	RST_B
Initial Value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.4-35 PCI_RC_RESET Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b.
16	force to D0	Forcibly shifts PM control to the D0 state after transmission of PME_TO_Ack. It is automatically cleared when PM control shifts to D0. Use of this bit is generally prohibited, as it can cause a mismatch with the power state of the entire system. 0b: No operation 1b: Shift to D0
15 to 12	—	Reserved. These bits are read as 0b.
11 to 8	Debug	(Fixed to 0000b.) Debug register
7	RST_PREG_B	Not used in this unit. The set value does not affect to unit operation. 0b: Reset 1b: Normal operation
6	RST_OUT_B	RST_OUT_B output 0b: Reset 1b: Normal operation
5	RST_PS_B	Reset the PCI Express core (PCLK domain) inside the unit. 0b: Reset 1b: Normal operation
4	RST_LOAD_B	Reset the configuration registers. Reset bits that have not been initialized by RST_LOAD_B. 0b: Reset 1b: Normal operation
3	RST_CFG_B	Reset the configuration registers. 0b: Reset 1b: Normal operation
2	RST_RSM_B	POWERGOOD-Reset AUX Power (AUX not supported)
1	RST_GP_B	Reset the PCI Express core (ACLK domain) inside the unit. 0b: Reset 1b: Normal operation

Table 36.4-35 PCI_RC_RESET Register Contents (2/2)

Bit Position	Bit Name	Description
0	RST_B	Reset the PCI Express core inside the unit. 0b: Reset 1b: Normal operation

(29) Mode Set 0 Register (PCI_RC_MSET0)

This register sets AXI mode.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0314h

Initial Value: 2001_2000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	AWPROT[2:0]			AWCACHE_L[3:0]				—	—	AWLOCK		AWCACHE_D[3:0]			
Initial Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	ARPROT			—	—	—	—	—	—	ARLOCK		ARCACHE			
Initial Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 36.4-36 PCI_RC_MSET0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b.
30 to 28	AWPROT[2:0]	Set the protection type in a transition from PCIe to AXI. These bits indicate whether the transaction protection level is “normal”, “privilege”, or “secure”, and whether the transaction is command access or data access. [2] 1b: Command access 0b: Data access [1] 1b: Non-secure access 0b: Secure access [0] 1b: Privilege access 0b: Normal access
27 to 24	AWCACHE_L[3:0]	Indicates the value of MAWCACHE[3:0] issued to AXI. This setting is issued when an AXI request containing the last byte is issued. * The recommended value is 0000b. [3] 1b: Write allocation enabled 0b: Write allocation disabled [2] 1b: Read allocation enabled 0b: Read allocation disabled [1] 1b: Cacheable 0b: Not cacheable [0] 1b: Bufferable 0b: Not bufferable.
23, 22	—	Reserved. These bits are read as 0b.
21, 20	AWLOCK	Lock type in a transition from PCIe to AXI. This signal provides information on the atomic nature of transfer. 00b: Normal access 01b: Exclusive access 10b: Lock access 11b: Reserved
19 to 16	AWCACHE_D[3:0]	Specifies the value of MAWCACHE[3:0] issued to AXI. This setting is issued when an AXI request other than the output condition of AWCACHE_L is issued. * The recommended value is 0001b. [3] 1b: Write allocation enabled 0b: Write allocation disabled [2] 1b: Read allocation enabled 0b: Read allocation disabled [1] 1b: Cacheable 0b: Not cacheable [0] 1b: Bufferable 0b: Not bufferable
15	—	Reserved. This bit is read as 0b.

Table 36.4-36 PCI_RC_MSET0 Register Contents (2/2)

Bit Position	Bit Name	Description
14 to 12	ARPROT[2:0]	Set the protection type in a transition from PCIe to AXI. These bits indicate whether the transaction protection level is “normal”, “privilege”, or “secure”, and whether the transaction is command access or data access. [2] 1b: Command access 0b: Data access [1] 1b: Non-secure access 0b: Secure access [0] 1b: Privilege access 0b: Normal access
11 to 6	—	Fixed to 0b.
5, 4	ARLOCK	Lock type in a transition from PCIe to AXI. This signal provides information on the atomic nature of transfer. 00b: Normal access 01b: Exclusive access 10b: Lock access 11b: Reserved
3 to 0	ARCACHE	Cache type in a transition from PCIe to AXI. These bits specifies “bufferable”, “cacheable”, “write-through”, “write-back”, or “allocation” as the attribute of the transaction.

(30) Mode Set 1 Register (PCI_RC_MSET1)

This register sets AXI mode.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0318h

Initial Value: 0000_33F2h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AXI Max Issue Write				AXI Max Issue Read				AXI Master Max Burst				—	—	RAM Parity Enable	PCIe Request Order
Initial Value	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	RW	RW

Table 36.4-37 PCI_RC_MSET1 Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15 to 12	AXI Max Issue Write	Sets the allowable number of write requests to be issued by an AXI master. Set the range that the interconnect can accept. 0h: Allowable number: 1 1h: Allowable number: 2 … Fh: Allowable number: 16
11 to 8	AXI Max Issue Read	Sets the allowable number of read requests to be issued by an AXI master. Set the range that the interconnect can accept. 0h: Allowable number: 1 1h: Allowable number: 12 … Fh: Allowable number: 16
7 to 4	AXI Master Max Burst	Sets the maximum burst length in AXI master operations.
3, 2	—	Reserved. These bits are read as 0b.
1	RAM Parity Enable	Enables or disables parity checking of the internal SRAM. The initial value is "enable" but is ignored for a unit not equipped with this function. 0b: Disable parity checking of the RAM. 1b: Enable parity checking of the RAM.
0	PCIe Request Order	The same AXI master issues read requests to PCIe without waiting for completion. Set 1b to strictly preserve the order of requests to the completer. 0b: Not waiting for completion. 1b: Waiting for completion.

(31) Mode Set 3 Register (PCI_RC_MSET3)

This register outputs the setting value as the ASPM L1 Idle Time bit.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0380h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	ASPM L1 Idle Time							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.4-38 PCI_RC_MSET3 Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved
7 to 0	ASPM L1 Idle Time	Sets the idle time for AXI transactions that will be checked by the unit during the transition to ASPM L1. 8 bits are set by these bits, and FFh is added to the lower 8 bits to form the idle time cycles. One condition for a transition to ASPM L1 is to confirm its idle time. 00h: 256 [ACLK] 01h: 512 [ACLK] … FFh: 65536 [ACLK]

(32) Debug Output 1 Register (PCI_RC_DBGOUT1)

This register is for debugging.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0384h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Debug															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Debug															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.4-39 PCI_RC_DBGOUT1 Register Contents

Bit Position	Bit Name	Description
31 to 0	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.

(33) Debug Output 2 Register (PCI_RC_DBGOUT2)

This register is for debugging.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0388h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Debug															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.4-40 PCI_RC_DBGOUT2 Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved
15 to 0	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.

(34) Debug Input 0 Register (PCI_RC_DBGIN0)

This register is for debugging.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0390h

Initial Value: xxxx_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	Debug			
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-41 PCI_RC_DBGIN0 Register Contents

Bit Position	Bit Name	Description
31 to 4	—	Reserved
3 to 0	Debug	This register is for use in debugging by Renesas. Do not use GPI [3:0]

(35) PCIe Core Mode Set 1 Register (PCI_RC_PCMSET1)

This register sets the operating mode of the PCI Express core.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0400h

Initial Value: 07D0_00F2h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	Debug		ASPM_L1_INTERVAL_TIME											
Initial Value	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	Debug		MODE_LINK_UPCONFIGURE_CAPABILITY_DISABLED	—	MODE_TXSWING	Debug						—	—	MODE_PORT	MODE_PORT_ENABLE_B
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0
R/W	R	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	R	R	RW	RW

Table 36.4-42 PCI_RC_PCMSET1 Register Contents (1/2)

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29, 28	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
27 to 16	ASPM_L1_INTERVAL_TIME	Sets the interval between ASM L1 requests. The PCIe base specification stipulates that ASML1 transition requests shall not be accepted continuously within 10 µs. To guard against this, set a timer value in this field. Make a setting such that the ACLK cycle x the set value is at least 10 µs. Setting in this product: When ACLK = 200 MHz (5 ns): 2000 (d) = 7D0 (h) = 0111_1101_0000
15	—	Fixed to 0b.
14, 13	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
12	MODE_LINK_UPCONFIGURE_CAPABILITY_DISABLED	Sets the Link Upconfigure Capability bit for a Training Sequence Ordered-set (TS-OS). 0b: Link Upconfigure Capability bit = 1b 1b: Link Upconfigure Capability bit = 0b (Gen1 × 1) When connecting to a Gen1 PCIe device, if this bit is not 0b, link-up may not be performed. In that case, change the bit to 0b by F/W.
11	—	Reserved. This bit is read as 0b.
10	MODE_TXSWING	Controls the amplitude of SerDes serial output. 0b: Full swing mode (initial value) 1b: Half swing mode
9 to 4	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
3, 2	—	Reserved. These bits are read as 0b.
1	MODE_PORT	Device type setting register. Be sure to fix it to “1b” before operation. 0b: Endpoint (setting prohibited) 1b: Root complex

Table 36.4-42 PCI_RC_PCMSET1 Register Contents (2/2)

Bit Position	Bit Name	Description
0	MODE_PORT_ENABLE_B	PHY disable setting register. It is fixed to 0b during normal operation. 0b: Normal operation 1b: PHY OFF

(36) PCIe Core Control 1 Register (PCI_RC_PCCTRL1)

This register controls power management and LTSSM (Link Training Sequence State Machine) state transitions.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0404h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BLB_RELAX_ORDERING_EN	—	—	—	Debug	—	UI_ENTER_L1S	Debug	RETURN_TO_L0	UI_RC_REJECT_ASPML1	Auto_PM_Active_State_Nak	UI_ENTER_L2	UI_ENTER_TXL0S
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	RW	R	R	R	RW	R	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	MODE_QUIESCE_GUARANTEE	UI_ENTER_TX_MODE_SRIS	MODE_EQ_AUTONOMOUS	MODE_EQ_PHASE23_ENABLE	MODE_RESET_EIEOS_INTERVALL0S	—	—	—	—	Debug			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	RW	RW	RW	RW	RW	R	R	R	R	RW	RW	RW	RW

Table 36.4-43 PCI_RC_PCCTRL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 29	—	Reserved. These bits are read as 0b.
28	BLB_RELAX_ORDERING_EN	Controls the RO bit of the request for transmission. 0b: The RO bit of the request TLP for transmission is always 0b (initial value). 1b: The RO bit of the request TLP for transmission can be set to 1b.
27 to 25	—	Reserved. These bits are read as 0b.
24	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
23	—	Reserved. This bit is read as 0b.
22	UI_ENTER_L1S	Enable transition to the L1 substate. 0b: Disable transition to the L1 substate (initial value). 1b: Enable transition to the L1 substate (setting prohibited).
21	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
20	RETURN_TO_L0	Controls the L1 or L2 state of RC mode to the L0 state (not normally used). 0b: Normal operation (initial value) 1b: Returns to the L0 state from the L1 or L2 state in RC mode. It is cleared automatically by confirming PMU_LINKSTATE [0] = 1.
19	UI_RC_REJECT_ASPML1	Rejects the transition to ASPM L1. 0b: Accepts the ASPM L1 transition request from the other-party EP device (initial value). 1b: Rejects the ASPM L1 transition request from the other-party EP device.
18	Auto PM_Active_State_Nak	PM_ActiveState_Nak Message transmit mode during ASPM L1 rejection. Set 1b to reject ASPM L1 in RC. This bit is cleared automatically by transmitting PM_ActiveState_Nak automatically. *Note*: Automatic transmission is allowed only once.
17	UI_ENTER_L2	Controls transition to L2 in RC mode. Set 1b for transition to the L2 state in RC mode. The PCIe core should be reset by the reset register control at the time of transition to the L2 state. This bit must be cleared to 0b after release from the reset following the return from the L2 state.

Table 36.4-43 PCI_RC_PCCTRL1 Register Contents (2/2)

Bit Position	Bit Name	Description
16	UI_ENTER_TXL0S	TxL0s transition control 0b: A transition to ASPM L0s is not initiated (initial value). 1b: A transition to ASPM L0s is initiated when the internal conditions are met.
15 to 13	—	Fixed to 0b.
12	MODE_QUIESCE_GUARANTEE	The Symbol6 bit 6 Quiesce Guarantee control bit of TS2OS 0b: Set TS2OS to 0b (initial value). 1b: Set TS2OS to 1b.
11	UI_ENTER_TXMODE_SRIS	Sets the clock tolerance compensation. 0b: SRNS (initial value) 1b: SRIS (not supported)
10	MODE_EQ_AUTONOMOUS	Reserved
9	MODE_EQ_PHASE23_ENABLE	Reserved
8	MODE_RESET_EIEOS_INTERVALL0S	Reserved
7 to 4	—	Reserved. These bits are read as 0b.
3 to 0	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.

(37) PCIe Core Status 1 Register (PCI_RC_PCSTAT1)

This register controls power management and LTSSM (Link Training Sequence State Machine) state transitions.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0408h

Initial Value: 000x_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	Debug				—	Debug			—	—	bme_down	Debug
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	LTSSM_STATE							PMU_LINKSTATE				—	Debug	STATE_VC0_NEGOTIATION_PENDING	DL_Down Status
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	0	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-44 PCI_RC_PCSTAT1 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b.
27 to 24	Debug	This register is for use in debugging by Renesas.
23	—	Reserved. This bit is read as 0b.
22 to 20	Debug	This register is for use in debugging by Renesas.
19, 18	—	Reserved. These bits are read as 0b.
17	bme_down	Indicates that the PCIe core transmission section cannot be used.
16	Debug	This register is for use in debugging by Renesas.
15	—	Reserved. This bit is read as 0b.
14 to 8	LTSSM_STATE	Indicates the states of the Link Training and Status State Machine in the link of the PCIe core. The following state is indicated by the upper 5 bits [14:10]. 000_xxb: Detect 001_xxb: Polling 010_xxb: Config 011_00b: Lo 011_01b: L1 011_1xb: L2 100_xxb: Recovery 101_xxb: Disable 110_xxb: Loopback
7 to 4	PMU_LINKSTATE	Monitors the L-state of the power management control section. 0100b: L1 state 1000b: L2 state
3	—	Reserved. This bit is read as 0b.
2	Debug	This register is for use in debugging by Renesas.
1	STATE_VC0_NEGOTIATION_PENDING	Monitors flow control initialization operation. When this bit is 1b, transactions should not be started by AXI. Confirm that this bit is 0b and DL_Down Status (bit [0]) is 0b. 0b: Indicates the completion of flow control initialization. 1b: Indicates that flow control initialization is not completed.

Table 36.4-44 PCI_RC_PCSTAT1 Register Contents (2/2)

Bit Position	Bit Name	Description
0	DL_down status	Indicates whether the PCIe core is in the DL_Down or DL_Up state. 0b: DL_Up state 1b: DL_Down state

(38) PCIe Core Control 2 Register (PCI_RC_PCCTRL2)

This register controls the link speed/width change in the PCI Express core.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0410h

Initial Value: 003E_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	UI_LINK_WIDTH_CHANGE_ENABLE[7:0]								MODE_NODEEMPHASIS[1:0]		MODE_PRESET_ENABLE[4:0]					UI_LINK_WIDTH_CHANGE_REQ
Initial Value	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	UI_LINK_SPEED_CHANGE		—	—	—	UI_LINK_CHANGE_AUTONOMOUS	—	—	—	UI_LINK_SPEED_CHANGE_REQ
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	R	R	R	RW	R	R	R	RW

Table 36.4-45 PCI_RC_PCCTRL2 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 24	UI_LINK_WIDTH_CHANGE_ENABLE [7:0]	Link width setting to be changed. When UI_LINK_WIDTH_CHANGE_REQ is asserted to request link width change, set to 1b to change to the corresponding lane. The LSB (bit [24]) corresponds to lane 0 and bit [25] corresponds to lane 1. Bits 31 to 26 are not supported.
23, 22	MODE_NODEEMPHASIS[1:0]	No de-emphasis mode setting pin during Gen1/Gen2 operation. [0]: During Gen1 operation 0b: Normal operation mode (initial value) 1b: No de-emphasis mode [1]: During Gen2 operation 0b: Normal operation mode (initial value) 1b: No de-emphasis mode
21 to 17	MODE_PRESET_ENABLE[4:0]	Reserved
16	UI_LINK_WIDTH_CHANGE_REQ	Link width change request control Set this bit to 1b to request that the link width be changed to the configuration of the bits [31:24] UI_LINK_WIDTHCHANGE_ENABLE field. Asserting during the L0 state transitions the Recovery state to the Configuration state, and a negotiation is performed with the other-party device. After confirming assertion of UI_LINK_WIDTH_CHANGE_DONE of PCIe Core Status 2 Register (address: <PCI_S0_REG_base> + 0414h) bit [29], set 1b0.
15 to 10	—	Reserved. These bits are read as 0b.
9, 8	UI_LINK_SPEED_CHANGE	Link speed setting Set the link speed. 00b: 2.5 GT/s 01b: 5.0 GT/s 10b: 8.0 GT/s (setting prohibited) 11b: 16.0 GT/s (setting prohibited)
7 to 5	—	Reserved. These bits are read as 0b.

Table 36.4-45 PCI_RC_PCCTRL2 Register Contents (2/2)

Bit Position	Bit Name	Description
4	UI_LINK_CHANGE_AUTONOMOUS	Reason for link width/speed change 0b: Reliability reason (Changes for reliability. Direction of decreasing bandwidth) 1b: Autonomous reason (Intentional change)
3 to 1	—	Reserved. These bits are read as 0b.
0	UI_LINK_SPEED_CHANGE_REQ	Link speed change request control Issues a request to change the link speed to the speed set in bit [8] UI_LINK_SPEED_CHANGE field. Asserting during the L0 state transitions the recovery state to the configuration state, and negotiation is performed with the other-party device. After confirming assertion of UI_LINK_SPEED_CHANGE_DONE of PCIe Core Status 2 Register (address: <PCI_S0_REG_base> + 0414h) bit [28], set 1b0.

(39) PCIe Core Status 2 Register (PCI_RC_PCSTAT2)

This register indicates the status of the link speed/width change in the PCI Express core.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0414h

Initial Value: xxxx_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	UI_LINK_WIDTH_CHANGE_DONE	UI_LINK_SPEED_CHANGE_DONE	—	—	—	STATE_UPCONFIGURE_CAPABLE	—	STATE_NEGOTIATED_LANE_END			—	STATE_NEGOTIATED_LANE_START		
Initial Value	0	0	x	x	0	0	0	x	0	x	x	x	0	0	x	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	STATE_RECEIVER_DETECTED[7:0]								STATE_DATA_RATE_IDENTIFIER_RECEIVED[7:0]							
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	0	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-46 PCI_RC_PCSTAT2 Register Contents (1/2)

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29	UI_LINK_WIDTH_CHANGE_DONE	Indicates the completion of link width change operation. Notifies the completion (1b) of a width change requested by setting UI_LINK_WIDTH_CHANGE_REQ of PCIe Core Control 2 Register (address: <PCI_S0_REG_base> + 0410h) bit [16]. It is set 0b by setting UI_LINK_WIDTH_CHANGE_REQ to 0b.
28	UI_LINK_SPEED_CHANGE_DONE	Notifies the completion (1b) of a speed change requested by setting. UI_LINK_SPEED_CHANGE_REQ of PCIe Core Control 2 Register (address: <PCI_S0_REG_base> + 0410h) bit [0]. It is set 0b by setting UI_LINK_SPEED_CHANGE_REQ to 0b.
27 to 25	—	Reserved. These bits are read as 0b.
24	STATE_UPCONFIGURE_CAPABLE	Indicates the Upconfigure Capable bit of the other-party device. Indicates that the other-party device supports changes in the direction to increase the link width. If this bit is 0b, after changing the link width, the original link width cannot be restored.
23	—	Reserved. This bit is read as 0b.
22 to 20	STATE_NEGOTIATED_LANE_END	During n lanes operation, indicates the position of a lane number (n = 1) (If n = 2, it means lane 1) after link negotiation with the other-party device. Used to check the current state of the operating lane before changing the link width. 000b: Lane 0 is the lane number (n - 1). 001b: Lane 1 is the lane number (n - 1). Others: Reserved
19	—	Reserved. This bit is read as 0b.
18 to 16	STATE_NEGOTIATED_LANE_START	During n lanes operation, indicates the position of lane number 0 after link negotiation with the other-party device. Used to check the current state of the operating lane before changing the link width. 000b: Lane 0 is the lane number 0. 001b: Lane 1 is the lane number 0. Others: Reserved

Table 36.4-46 PCI_RC_PCSTAT2 Register Contents (2/2)

Bit Position	Bit Name	Description
15 to 8	STATE_RECEIVER_DETECTED[7:0]	Indicates the connection status with the other-party device. The result of receiver detection is displayed. [0]: An other-party device was detected on lane 0. [1]: An other-party device was detected on lane 1. (Only x2 case) [2] to [7]: Reserved
7 to 0	STATE_DATA_RATE_IDENTIFIER_RECEIVED[7:0]	Indicates the link speed supported by the other-party device. Indicates the data rate Identifier field of TS-OS received from the other-party device. Bit 0: Reserved Bit 1: 2.5 GT/s data rate supported. Must be set to 1b. Bit 2: 5.0 GT/s data rate supported

(40) PCIe Core Status 5 Register (PCI_RC_PCSTAT5)

This register indicates the status in the PCI Express core.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 042Ch

Initial Value: 0000_0x00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Debug															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Debug															ORT_TRANSACTION_PENDING
Initial Value	0	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-47 PCI_RC_PCSTAT5 Register Contents

Bit Position	Bit Name	Description
31 to 1	Debug	This register is for use in debugging by Renesas.
0	ORT_TRANSACTION_PENDING	Indicates the presence of an outstanding request (not all completion responses corresponding to non-posted requests from the AXI side have not been received). Check this bit before requesting or enabling a transition to TxL0s/L1/L2 to ensure that no outstanding requests are present. 0b: No outstanding requests are present. 1b: Outstanding requests are present.

(41) DMA Interrupt Vector 0 Register (PCI_RC_DMAINTVEC0)

This register specifies the interrupt vectors for interrupt notification from AXI to PCIe (MSI) during DMA transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 04D0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	DMA_CH3_MSI_EN	DMA_CH3_vec					—	—	DMA_CH2_MSI_EN	DMA_CH2_vec				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DMA_CH1_MSI_EN	DMA_CH1_vec					—	—	DMA_CH0_MSI_EN	DMA_CH0_vec				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 36.4-48 PCI_RC_DMAINTVEC0 Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29	DMA_CH3_MSI_EN	DMA Ch3 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
28 to 24	DMA_CH3_vec	Specifies the MSI interrupt vector transmitted by DMAC ch. 3.
23, 22	—	Reserved. These bits are read as 0b.
21	DMA_CH2_MSI_EN	DMA Ch2 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
20 to 16	DMA_CH2_vec	Specifies the MSI interrupt vector transmitted by DMAC ch. 2.
15, 14	—	Reserved. These bits are read as 0b.
13	DMA_CH1_MSI_EN	DMA Ch1 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
12 to 8	DMA_CH1_vec	Specifies the MSI interrupt vector transmitted by DMAC ch. 1.
7, 6	—	Reserved. These bits are read as 0b.
5	DMA_CH0_MSI_EN	DMA Ch0 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
4 to 0	DMA_CH0_vec	Specifies the MSI interrupt vector transmitted by DMAC ch. 0.

Note: DMA_CHx_vec should be fixed to 0_0000b for the RC function.

(42) DMA Interrupt Vector 1 Register (PCI_RC_DMAINTVEC1)

This register specifies the interrupt vectors for interrupt notification from AXI to PCIe (MSI) during DMA transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 04D4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	DMA_CH7_MSI_EN	DMA_CH7_vec					—	—	DMA_CH6_MSI_EN	DMA_CH6_vec				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DMA_CH5_MSI_EN	DMA_CH5_vec					—	—	DMA_CH4_MSI_EN	DMA_CH4_vec				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 36.4-49 PCI_RC_DMAINTVEC1 Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29	DMA_CH7_MSI_EN	DMA Ch7 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
28 to 24	DMA_CH7_vec	Specifies the MSI interrupt vector transmitted by DMAC ch. 7.
23, 22	—	Reserved. These bits are read as 0b.
21	DMA_CH6_MSI_EN	DMA Ch6 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
20 to 16	DMA_CH6_vec	Specifies the MSI interrupt vector transmitted by DMAC ch. 6.
15, 14	—	Reserved. These bits are read as 0b.
13	DMA_CH5_MSI_EN	DMA Ch5 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
12 to 8	DMA_CH5_vec	Specifies the MSI interrupt vector transmitted by DMAC ch. 5.
7, 6	—	Reserved. These bits are read as 0b.
5	DMA_CH4_MSI_EN	DMA Ch4 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
4 to 0	DMA_CH4_vec	Specifies the MSI interrupt vector transmitted by DMAC ch. 4.

Note: DMA_CHx_vec should be fixed to 0_0000b for the RC function.

(43) DMA Control Register (PCI_RC_DMACTRL)

This register sets the maximum size of read requests which can be issued to the PCIe core as a DMAC function. Use the initial setting (128 bytes). This setting is common to all DMA channels.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0800h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	D_PMRS		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 36.4-50 PCI_RC_DMACTRL Register Contents

Bit Position	Bit Name	Description
31 to 3	—	Reserved. These bits are read as 0b.
2 to 0	D_PMRS	DMAC PCIe Max Read Request Size Sets the maximum size of read requests to be issued to PCIe by the DMAC. 000b: 128 bytes (initial value) 001b: 256 bytes 010b: 512 bytes (not supported) 011b: 1024 bytes (not supported) 100b: 2048 bytes (not supported) 101b: 4096 bytes (not supported) Others: Reserved (setting prohibited)

(44) DMA Interrupt Enable Register (PCI_RC_DMAINTE)

This register enables interrupts from the individual DMA channels.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0808h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CH7_ERR_EN	CH7_QUE_EMP_EN	CH7_STOP_EN	CH7_END_EN	CH6_ERR_EN	CH6_QUE_EMP_EN	CH6_STOP_EN	CH6_END_EN	CH5_ERR_EN	CH5_QUE_EMP_EN	CH5_STOP_EN	CH5_END_EN	CH4_ERR_EN	CH4_QUE_EMP_EN	CH4_STOP_EN	CH4_END_EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH3_ERR_EN	CH3_QUE_EMP_EN	CH3_STOP_EN	CH3_END_EN	CH2_ERR_EN	CH2_QUE_EMP_EN	CH2_STOP_EN	CH2_END_EN	CH1_ERR_EN	CH1_QUE_EMP_EN	CH1_STOP_EN	CH1_END_EN	CH0_ERR_EN	CH0_QUE_EMP_EN	CH0_STOP_EN	CH0_END_EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.4-51 PCI_RC_DMAINTE Register Contents (1/3)

Bit Position	Bit Name	Description
31	CH7_ERR_EN	CH7 Error Interrupt Enable 1b: Enable 0b: Disable
30	CH7_QUE_EMP_EN	CH7 Queue Empty Interrupt Enable 1b: Enable 0b: Disable
29	CH7_STOP_EN	CH7 Stop Interrupt Enable 1b: Enable 0b: Disable
28	CH7_END_EN	CH7 Completion Interrupt Enable 1b: Enable 0b: Disable
27	CH6_ERR_EN	CH6 Error Interrupt Enable 1b: Enable 0b: Disable
26	CH6_QUE_EMP_EN	CH6 Queue Empty Interrupt Enable 1b: Enable 0b: Disable
25	CH6_STOP_EN	CH6 Stop Interrupt Enable 1b: Enable 0b: Disable
24	CH6_END_EN	CH6 Completion Interrupt Enable 1b: Enable 0b: Disable
23	CH5_ERR_EN	CH5 Error Interrupt Enable 1b: Enable 0b: Disable
22	CH5_QUE_EMP_EN	CH5 Queue Empty Interrupt Enable 1b: Enable 0b: Disable

Table 36.4-51 PCI_RC_DMAINTE Register Contents (2/3)

Bit Position	Bit Name	Description
21	CH5_STOP_EN	CH5 Stop Interrupt Enable 1b: Enable 0b: Disable
20	CH5_END_EN	CH5 Completion Interrupt Enable 1b: Enable 0b: Disable
19	CH4_ERR_EN	CH4 Error Interrupt Enable 1b: Enable 0b: Disable
18	CH4_QUE_EMP_EN	CH4 Queue Empty Interrupt Enable 1b: Enable 0b: Disable
17	CH4_STOP_EN	CH4 Stop Interrupt Enable 1b: Enable 0b: Disable
16	CH4_END_EN	CH4 Completion Interrupt Enable 1b: Enable 0b: Disable
15	CH3_ERR_EN	CH3 Error Interrupt Enable 1b: Enable 0b: Disable
14	CH3_QUE_EMP_EN	CH3 Queue Empty Interrupt Enable 1b: Enable 0b: Disable
13	CH3_STOP_EN	CH3 Stop Interrupt Enable 1b: Enable 0b: Disable
12	CH3_END_EN	CH3 Completion Interrupt Enable 1b: Enable 0b: Disable
11	CH2_ERR_EN	CH2 Error Interrupt Enable 1b: Enable 0b: Disable
10	CH2_QUE_EMP_EN	CH2 Queue Empty Interrupt Enable 1b: Enable 0b: Disable
9	CH2_STOP_EN	CH2 Stop Interrupt Enable 1b: Enable 0b: Disable
8	CH2_END_EN	CH2 Completion Interrupt Enable 1b: Enable 0b: Disable
7	CH1_ERR_EN	CH1 Error Interrupt Enable 1b: Enable 0b: Disable
6	CH1_QUE_EMP_EN	CH1 Queue Empty Interrupt Enable 1b: Enable 0b: Disable
5	CH1_STOP_EN	CH1 Stop Interrupt Enable 1b: Enable 0b: Disable

Table 36.4-51 PCI_RC_DMAINTE Register Contents (3/3)

Bit Position	Bit Name	Description
4	CH1_END_EN	CH1 Completion Interrupt Enable 1b: Enable 0b: Disable
3	CH0_ERR_EN	CH0 Error Interrupt Enable 1b: Enable 0b: Disable
2	CH0_QUE_EMP_EN	CH0 Queue Empty Interrupt Enable 1b: Enable 0b: Disable
1	CH0_STOP_EN	CH0 Stop Interrupt Enable 1b: Enable 0b: Disable
0	CH0_END_EN	CH0 Completion Interrupt Enable 1b: Enable 0b: Disable

(45) DMA Interrupt Status Register (PCI_RC_DMAINTS)

This register indicates the state of interrupts from the individual DMA channels.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 080Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CH7_ERR	CH7_QUE_EMP	CH7_STOP	CH7_END	CH6_ERR	CH6_QUE_EMP	CH6_STOP	CH6_END	CH5_ERR	CH5_QUE_EMP	CH5_STOP	CH5_END	CH4_ERR	CH4_QUE_EMP	CH4_STOP	CH4_END
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH3_ERR	CH3_QUE_EMP	CH3_STOP	CH3_END	CH2_ERR	CH2_QUE_EMP	CH2_STOP	CH2_END	CH1_ERR	CH1_QUE_EMP	CH1_STOP	CH1_END	CH0_ERR	CH0_QUE_EMP	CH0_STOP	CH0_END
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1

Table 36.4-52 PCI_RC_DMAINTS Register Contents (1/3)

Bit Position	Bit Name	Description
31	CH7_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
30	CH7_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
29	CH7_STOP	Set when the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
28	CH7_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1 It is cleared by writing 1b. Writing 0b has no effect.
27	CH6_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
26	CH6_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
25	CH6_STOP	Set when the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
24	CH6_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1 It is cleared by writing 1b. Writing 0b has no effect.
23	CH5_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.

Table 36.4-52 PCI_RC_DMAINTS Register Contents (2/3)

Bit Position	Bit Name	Description
22	CH5_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
21	CH5_STOP	Set when the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
20	CH5_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1. It is cleared by writing 1b. Writing 0b has no effect.
19	CH4_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
18	CH4_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
17	CH4_STOP	Set when the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
16	CH4_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1 It is cleared by writing 1b. Writing 0b has no effect.
15	CH3_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
14	CH3_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
13	CH3_STOP	Set when the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
12	CH3_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1 It is cleared by writing 1b. Writing 0b has no effect.
11	CH2_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
10	CH2_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
9	CH2_STOP	Set if the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
8	CH2_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field set to 1 It is cleared by writing 1b. Writing 0b has no effect.

Table 36.4-52 PCI_RC_DMAINTS Register Contents (3/3)

Bit Position	Bit Name	Description
7	CH1_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
6	CH1_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
5	CH1_STOP	Set when the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
4	CH1_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field set to 1 It is cleared by writing 1b. Writing 0b has no effect.
3	CH0_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
2	CH0_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
1	CH0_STOP	Set when the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
0	CH0_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field set to 1 It is cleared by writing 1b. Writing 0b has no effect.

(46) DMA Channel Control Register m (PCI_RC_DMACHCTLm) (m = 0 to 7)

This register sets the control method for each DMA channel. Set either register type or descriptor type, not both.

- Setting QUE_EN = 1 and QUE_CLR = 1 is prohibited during register-type DMA transfer (TDMA_EN = 1).
- Setting RDMA_EN = 1 is prohibited during descriptor-type DMA transfer (QUE_EN = 1).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0900h (m = 0)
<PCI_S0_REG_base> + 0980h (m = 1)
<PCI_S0_REG_base> + 0A00h (m = 2)
<PCI_S0_REG_base> + 0A80h (m = 3)
<PCI_S0_REG_base> + 0B00h (m = 4)
<PCI_S0_REG_base> + 0B80h (m = 5)
<PCI_S0_REG_base> + 0C00h (m = 6)
<PCI_S0_REG_base> + 0C80h (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	QUE_CLR	—	—	—	—	—	—	QUE_EN	RDMA_EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	R	R	R	R	R	R	RW	RW

Table 36.4-53 PCI_RC_DMACHCTLm Register Contents

Bit Position	Bit Name	Description
31 to 9	—	Reserved. These bits are read as 0b.
8	QUE_CLR	Queue Clear The queue is cleared by writing 1b. The descriptor lists registered in the queue (those waiting for execution and the one currently being executed) are all cleared. The value read is always 0b. Writing 1b is prohibited when QUE_EN is set.
7 to 2	—	Reserved. These bits are read as 0b.
1	QUE_EN	Queue Enable Writing 1b to this bit enables the start of processing of descriptor lists registered in the descriptor queue and of DMA transfer (descriptor type). The bit is automatically cleared to 0b when DMA transfer is stopped (normally or abnormally). DMA transfer can also be stopped by writing 0b. However, it is only stopped after the completion of the request (from PCIe or AXI) currently being executed.
0	RDMA_EN	Register DMA Transfer Enable Writing 1b to this bit starts DMA transfer (register type) and transfer specified in the RDMA_SIZE bits proceeds. It is automatically cleared to 0b when DMA has ended in response to the completion of DMA transfer or the detection of an error. DMA transfer can also be stopped by writing 0b. However, it is only stopped after the completion of the request (from PCIe or AXI) currently being executed. 1b: Register-type DMA transfer is started. 0b: Register-type DMA transfer is stopped.

(47) QUE Entry (Lower) Register m (PCI_RC_QUEEmL) (m = 0 to 7)

This register sets the descriptor queue list. This setting value is registered as the DSA (DMA descriptor start address) of the queue list.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0908h (m = 0)
<PCI_S0_REG_base> + 0988h (m = 1)
<PCI_S0_REG_base> + 0A08h (m = 2)
<PCI_S0_REG_base> + 0A88h (m = 3)
<PCI_S0_REG_base> + 0B08h (m = 4)
<PCI_S0_REG_base> + 0B88h (m = 5)
<PCI_S0_REG_base> + 0C08h (m = 6)
<PCI_S0_REG_base> + 0C88h (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DSA[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSA[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R

Table 36.4-54 PCI_RC_QUEEmL Register Contents

Bit Position	Bit Name	Description
31 to 0	QUE_ENTRY (DSA) [31:00]	Register a descriptor list queue. This area becomes the DSA. Set the address where the first descriptor is stored. Since the setting is for 8-byte alignment, the lower 3 bits are fixed to 0b.

Note: When these bits are read, any of the following will be read depending on the state of DMA transfer.
DMA transfer is proceeding: The descriptor list being executed
DMA transfer is stopped (when QUE_EN has been automatically cleared): The last list to have been executed
DMA transfer is stopped (when QUE_EN has been cleared by software): The list that has been stopped (was being executed).

(48) QUE Entry (Upper) Register m (PCI_RC_QUEEmU) (m = 0 to 7)

This register sets the descriptor queue list. This setting value is registered as the EI (end interrupt), LS (list stop), and the label of the queue list. Register to the queue by writing to [31:24].

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 090Ch (m = 0)
<PCI_S0_REG_base> + 098Ch (m = 1)
<PCI_S0_REG_base> + 0A0Ch (m = 2)
<PCI_S0_REG_base> + 0A8Ch (m = 3)
<PCI_S0_REG_base> + 0B0Ch (m = 4)
<PCI_S0_REG_base> + 0B8Ch (m = 5)
<PCI_S0_REG_base> + 0C0Ch (m = 6)
<PCI_S0_REG_base> + 0C8Ch (m = 7)

Initial Value: 0000_0000h

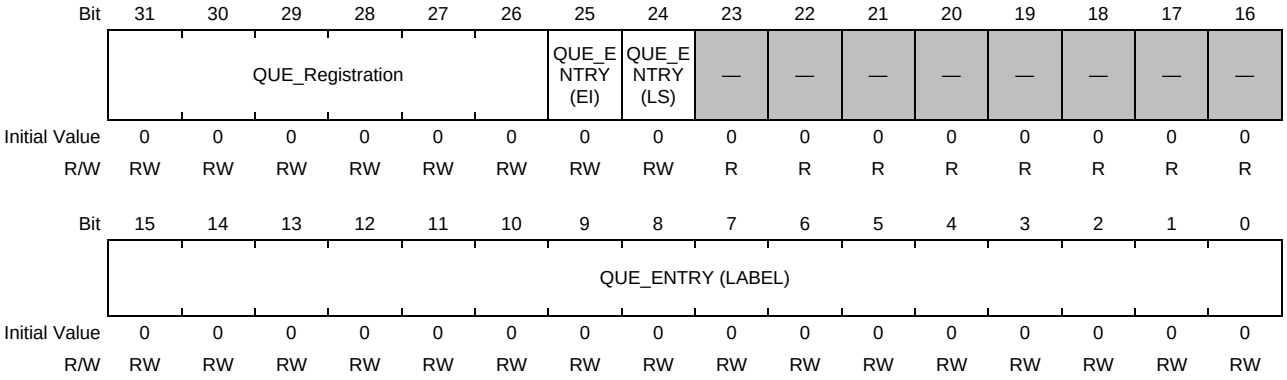


Table 36.4-55 PCI_RC_QUEEmU Register Contents

Bit Position	Bit Name	Description
31 to 26	QUE_Registration	Register to the queue by writing to [31:24]. The value read is always 0000_00b.
25	QUE_ENTRY (EI)	Specify whether to notify an interrupt (interrupt status CHx_END) when processing of the descriptor list is completed. 1b: Notify the interrupt. 0b: Does not notify the interrupt.
29	QUE_ENTRY (LS)	Specify whether to stop DMA transfer when processing of the descriptor list is completed. 1b: Stop DMA transfer. 0b: Does not stop DMA transfer.
23 to 16	—	Reserved. These bits are read as 0b.
15 to 0	QUE_ENTRY (LABEL)	This field represents the label of the list and there are no special rules for the setting procedures. The value can be set as desired.

Note: When these bits are read, any of the following will be read depending on the state of DMA transfer.
DMA transfer is proceeding: The descriptor list being executed
DMA transfer is stopped (when QUE_EN has been automatically cleared): The last list to have been executed
DMA transfer is stopped (when QUE_EN has been cleared by software): The list that has been stopped (was being executed).

(49) DMA Descriptor Control (Descriptor 00h) Register m (PCI_RC_DMADPCTLm) (m = 0 to 7)

This register indicates the field value at offset 00h in the descriptor table. Only effective when the descriptor-type DMA transfer is selected (the value read has no meaning in the case of register-type transfer).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0920h (m = 0)
<PCI_S0_REG_base> + 09A0h (m = 1)
<PCI_S0_REG_base> + 0A20h (m = 2)
<PCI_S0_REG_base> + 0AA0h (m = 3)
<PCI_S0_REG_base> + 0B20h (m = 4)
<PCI_S0_REG_base> + 0BA0h (m = 5)
<PCI_S0_REG_base> + 0C20h (m = 6)
<PCI_S0_REG_base> + 0CA0h (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DSCFM				—	WBD	LE	LV	D	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	STS															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-56 PCI_RC_DMADPCTLm Register Contents

Bit Position	Bit Name	Description
31 to 28	DSCFM	Indicates the DSCFM field value in the descriptor table being executed.
27	—	Reserved. This bit is read as 0b.
26	WBD	Indicates the WBD field value in the descriptor table being executed.
25	LE	Indicates the LE field value in the descriptor table being executed.
24	LV	Indicates the LV field value in the descriptor table being executed.
23	D	Indicates the D field value in the descriptor table being executed.
22 to 16	—	Reserved. These bits are read as 0b.
15 to 0	STS	Indicates the STS field value in the descriptor table being executed.

(50) DMA Source Address (Descriptor 04h) Register m (PCI_RC_DMASRCAm) (m = 0 to 7)

This register sets the start address of the source for DMA transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0924h (m = 0)
<PCI_S0_REG_base> + 09A4h (m = 1)
<PCI_S0_REG_base> + 0A24h (m = 2)
<PCI_S0_REG_base> + 0AA4h (m = 3)
<PCI_S0_REG_base> + 0B24h (m = 4)
<PCI_S0_REG_base> + 0BA4h (m = 5)
<PCI_S0_REG_base> + 0C24h (m = 6)
<PCI_S0_REG_base> + 0CA4h (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DMA_S_ADDR															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_S_ADDR															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R

Table 36.4-57 PCI_RC_DMASRCAm Register Contents

Bit Position	Bit Name	Description
31 to 0	DMA_S_ADDR	Sets the start address of the source for DMA transfer. Since the setting is for 8-byte alignment, the lower 3 bits are fixed to 0b.

Note: If the source address is for the PCIe space (DIR = 0), the PCIe request address is set in combination with the DMA PCIe upper address (descriptor 10h). When descriptor-type DMA transfer is to proceed, writing to these bits is prohibited and the value read indicates the value of the SA field in the descriptor table being executed.

(51) DMA Destination Address (Descriptor 08h) Register m (PCI_RC_DMADSTAm) (m = 0 to 7)

This register sets the start address of the destination for DMA transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0928h (m = 0)
<PCI_S0_REG_base> + 09A8h (m = 1)
<PCI_S0_REG_base> + 0A28h (m = 2)
<PCI_S0_REG_base> + 0AA8h (m = 3)
<PCI_S0_REG_base> + 0B28h (m = 4)
<PCI_S0_REG_base> + 0BA8h (m = 5)
<PCI_S0_REG_base> + 0C28h (m = 6)
<PCI_S0_REG_base> + 0CA8h (m = 7)

Initial Value: 0000_0000h

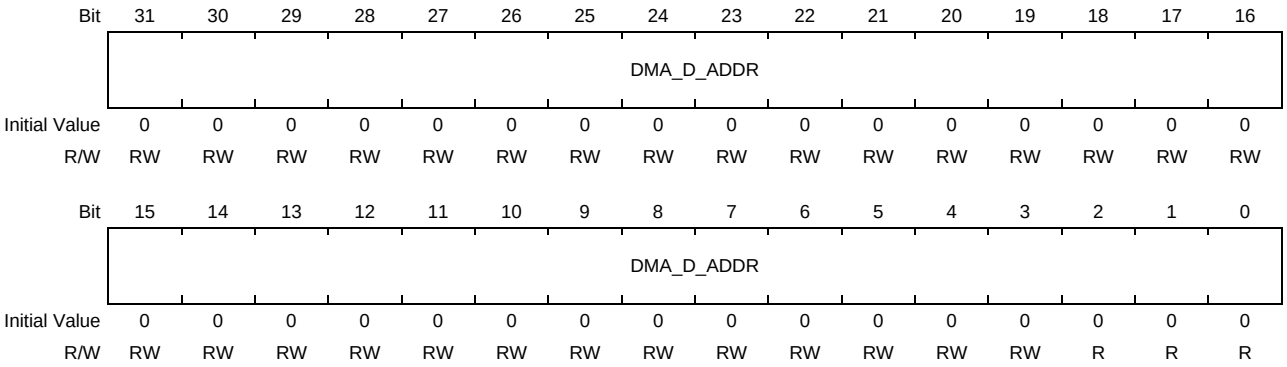


Table 36.4-58 PCI_RC_DMADSTAm Register Contents

Bit Position	Bit Name	Description
31 to 0	DMA_D_ADDR	Sets the start address of the destination for DMA transfer. Since the setting is for 8-byte alignment, the lower 3 bits are fixed to 0b.

Note: If the destination address is for the PCIe space (DIR = 0), the PCIe request address is set in combination with the DMA PCIe upper address (descriptor 10h). When descriptor-type DMA transfer is to proceed, writing to these bits is prohibited and the value read indicates the value of the DA field in the descriptor table being executed.

(52) DMA Size (Descriptor 0Ch) Register m (PCI_RC_DMASIZEm) (m = 0 to 7)

This register sets the number of bytes for DMA transfer. Reflects the field at offset 0Ch in the descriptor table.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 092Ch (m = 0)
<PCI_S0_REG_base> + 09ACh (m = 1)
<PCI_S0_REG_base> + 0A2Ch (m = 2)
<PCI_S0_REG_base> + 0AACh (m = 3)
<PCI_S0_REG_base> + 0B2Ch (m = 4)
<PCI_S0_REG_base> + 0BACh (m = 5)
<PCI_S0_REG_base> + 0C2Ch (m = 6)
<PCI_S0_REG_base> + 0CACh (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DMA_SIZE															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_SIZE															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R

Table 36.4-59 PCI_RC_DMASIZEm Register Contents

Bit Position	Bit Name	Description
31 to 0	DMA_SIZE	Sets the number of bytes for DMA transfer. Since the setting is for 8-byte alignment, the lower 3 bits are fixed to 0b.

Note: When descriptor-type DMA transfer is to proceed, writing to these bits is prohibited and the value read indicates the value of the SIZE field in the descriptor table being executed. The number of bytes for transfer when the setting is 0000_0000h is 1_0000_0000h.

(53) DMA PCIe Upper Address (Descriptor 10h) Register m (PCI_RC_DMAPCIEUAm) (m = 0 to 7)

This register sets the start address [63:32] for DMA transfer on the PCIe side.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0930h (m = 0)
<PCI_S0_REG_base> + 09B0h (m = 1)
<PCI_S0_REG_base> + 0A30h (m = 2)
<PCI_S0_REG_base> + 0AB0h (m = 3)
<PCI_S0_REG_base> + 0B30h (m = 4)
<PCI_S0_REG_base> + 0BB0h (m = 5)
<PCI_S0_REG_base> + 0C30h (m = 6)
<PCI_S0_REG_base> + 0CB0h (m = 7)

Initial Value: 0000_0000h

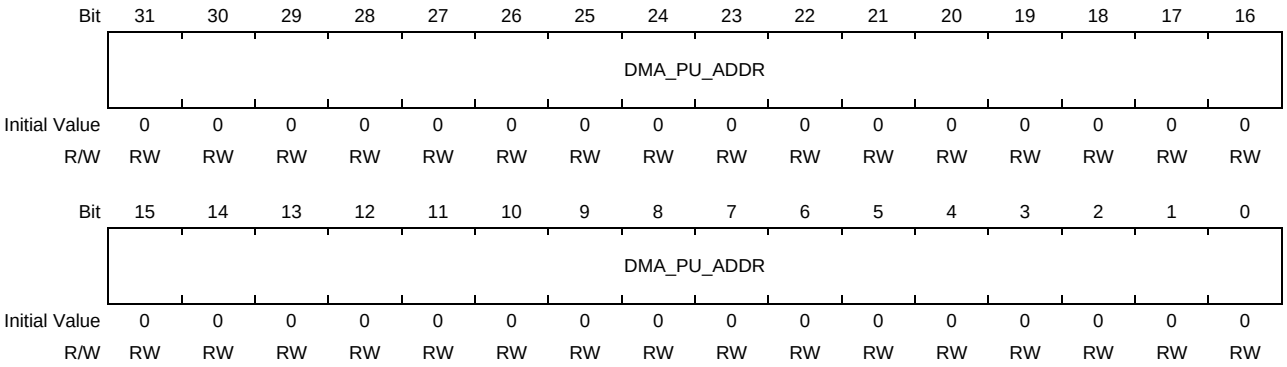


Table 36.4-60 PCI_RC_DMAPCIEUAm Register Contents

Bit Position	Bit Name	Description
31 to 0	DMA_PU_ADDR	Sets the start address [63:32] for DMA transfer on the PCIe side.

Note: When descriptor-type DMA transfer is to proceed, writing to these bits is prohibited and the value read indicates the value of the PUA field in the descriptor table being executed.

(54) DMA Transaction Control (Descriptor 14h) Register m (PCI_RC_DMATCTLm) (m = 0 to 7)

This register controls DMA transfer to the AXI side and PCIe side.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0934h (m = 0)
<PCI_S0_REG_base> + 09B4h (m = 1)
<PCI_S0_REG_base> + 0A34h (m = 2)
<PCI_S0_REG_base> + 0AB4h (m = 3)
<PCI_S0_REG_base> + 0B34h (m = 4)
<PCI_S0_REG_base> + 0BB4h (m = 5)
<PCI_S0_REG_base> + 0C34h (m = 6)
<PCI_S0_REG_base> + 0CB4h (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CCH_L[3:0]				CCH_D[3:0]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	DMA_TC			—	—	DMA_ATB[1:0]		—	DMA_FUN			—	—	—	DMA_DIR
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	R	RW	RW	R	RW	RW	RW	R	R	R	RW

Table 36.4-61 PCI_RC_DMATCTLm Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b.
23 to 20	CCH_L[3:0]	Indicates the value of A*CACHE[3:0] issued to AXI. This setting is issued when an AXI request containing the last byte is issued in transfer indicated by SIZE. The recommended value is 0000b. [3] 1b: Write allocation enabled 0b: Write allocation disabled [2] 1b: Read allocation enabled 0b: Read allocation disabled [1] 1b: Cacheable 0b: Not cacheable [0] 1b: Bufferable 0b: Not bufferable
19 to 16	CCH_D[3:0]	Specifies the value of A*CACHE[3:0] issued to AXI. This setting is issued when an AXI request other than the output condition of CCH_L is issued. When DIR = 0 (PCIe → AXI), the recommended value is 0001b. When DIR = 1 (AXI → PCIe), the recommended value is 0000b. [3] 1b: Write allocation enabled 0b: Write allocation disabled [2] 1b: Read allocation enabled 0b: Read allocation disabled [1] 1b: Cacheable 0b: Not cacheable [0] 1b: Bufferable 0b: Not bufferable
15	—	Reserved. This bit is read as 0b.
14 to 12	DMA_TC	The traffic class issued to PCIe. Indicates the traffic class value of the request issued to PCIe.
11, 10	—	Reserved. These bits are read as 0b.
9, 8	DMA_ATB[1:0]	The attribute issued to PCIe. Bit [1]: Relaxed ordering (non-supported function: Fixed to 0b) Bit [0]: No snoop (0b is recommended)
7	—	Reserved. This bit is read as 0b.
6 to 4	DMA_FUNC	Indicates the request function number issued to PCIe.
3 to1	—	Reserved. These bits are read as 0b.

Table 36.4-61 PCI_RC_DMATCTLm Register Contents (2/2)

Bit Position	Bit Name	Description
0	DMA_DIR	Sets the direction of DMA transfer. 1b: AXI → PCIe 0b: PCIe → AXI

Note: When descriptor-type DMA transfer is to proceed, writing to these bits is prohibited and the value read indicates the value of the CCH_L, CCH_D, TC, ATB, and DIR fields in the descriptor table being executed.

(55) DMA Descriptor Link Pointer (Descriptor 1Ch) Register m (PCI_RC_DMADPLPm) (m = 0 to 7)

This register indicates the field value at offset 1Ch in the descriptor table. Only effective when the descriptor-type DMA transfer is selected (the value read has no meaning in the case of register-type transfer).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 093Ch (m =0)
<PCI_S0_REG_base> + 09BCh (m = 1)
<PCI_S0_REG_base> + 0A3Ch (m = 2)
<PCI_S0_REG_base> + 0ABCh (m = 3)
<PCI_S0_REG_base> + 0B3Ch (m = 4)
<PCI_S0_REG_base> + 0BBCh (m = 5)
<PCI_S0_REG_base> + 0C3Ch (m = 6)
<PCI_S0_REG_base> + 0CBCh (m = 7)

Initial Value: 0000_0000h

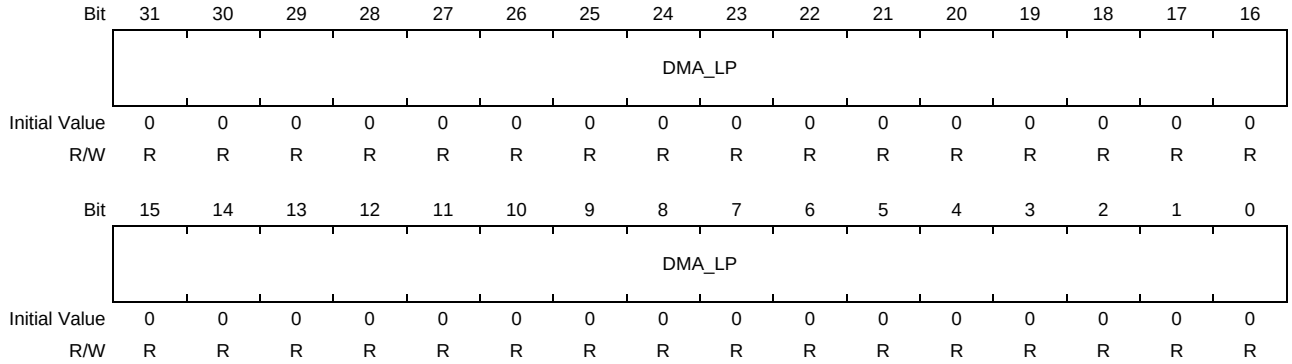


Table 36.4-62 PCI_RC_DMADPLPm Register Contents

Bit Position	Bit Name	Description
31 to 0	DMA_LP	Indicates the LP field value in the descriptor table being executed.

(56) DMA Rest Size Register m (PCI_RC_DMARESTSIZm) (m = 0 to 7)

This register indicates the number of bytes for which DMA transfer has not yet been completed.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0950h (m = 0)
<PCI_S0_REG_base> + 09D0h (m = 1)
<PCI_S0_REG_base> + 0A50h (m = 2)
<PCI_S0_REG_base> + 0AD0h (m = 3)
<PCI_S0_REG_base> + 0B50h (m = 4)
<PCI_S0_REG_base> + 0BD0h (m = 5)
<PCI_S0_REG_base> + 0C50h (m = 6)
<PCI_S0_REG_base> + 0CD0h (m = 7)

Initial Value: 0000_0000h

Table 36.4-63 PCI_RC_DMARESTSIZm Register Contents

Bit Position	Bit Name	Description
31 to 0	DMA_REST_SIZE	Indicates the number of bytes for which DMA transfer has not yet been completed (common to register-type and descriptor-type transfer).

(57) AXI Request Address Register m (PCI_RC_AREQAm) (m = 0 to 7)

This register indicates the address during AXI transfer that is in progress or for the most recently completed transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0954h (m = 0)
<PCI_S0_REG_base> + 09D4h (m = 1)
<PCI_S0_REG_base> + 0A54h (m = 2)
<PCI_S0_REG_base> + 0AD4h (m = 3)
<PCI_S0_REG_base> + 0B54h (m = 4)
<PCI_S0_REG_base> + 0BD4h (m = 5)
<PCI_S0_REG_base> + 0C54h (m = 6)
<PCI_S0_REG_base> + 0CD4h (m = 7)

Initial Value: 0000_0000h

Table 36.4-64 PCI_RC_AREQAm Register Contents

Bit Position	Bit Name	Description
31 to 0	AXI_REQ_ADDR	Indicates the address during AXI transfer that is in progress or for the most recently completed transfer (common to register type and descriptor type).

(58) PCIe Request Address (Lower) Register m (PCI_RC_PREQAmL) (m = 0 to 7)

This register indicates the lower 32 bits of the address during PCIe transfer that is in progress or for the most recently completed transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0958h (m = 0)
<PCI_S0_REG_base> + 09D8h (m = 1)
<PCI_S0_REG_base> + 0A58h (m = 2)
<PCI_S0_REG_base> + 0AD8h (m = 3)
<PCI_S0_REG_base> + 0B58h (m = 4)
<PCI_S0_REG_base> + 0BD8h (m = 5)
<PCI_S0_REG_base> + 0C58h (m = 6)
<PCI_S0_REG_base> + 0CD8h (m = 7)

Initial Value: 0000_0000h

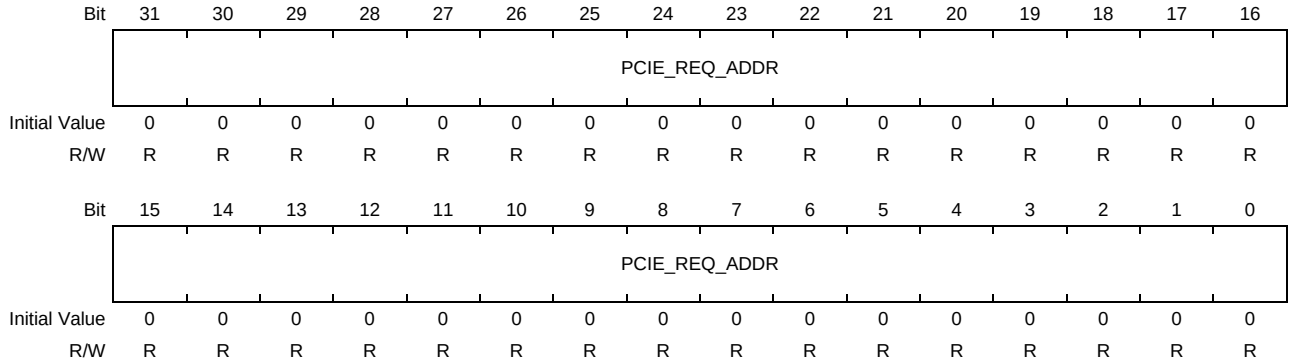


Table 36.4-65 PCI_RC_PREQAmL Register Contents

Bit Position	Bit Name	Description
31 to 0	PCIE_REQ_ADDR	Indicates the lower 32 bits of the address during PCIe transfer that is in progress or for the most recently completed transfer (common to register type and descriptor type).

(59) PCIe Request Address (Upper) Register m (PCI_RC_PREQAmU) (m = 0 to 7)

This register indicates the upper 32 bits of the address during PCIe transfer that is in progress or for the most recently completed transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 095Ch (m = 0)
<PCI_S0_REG_base> + 09DCh (m = 1)
<PCI_S0_REG_base> + 0A5Ch (m = 2)
<PCI_S0_REG_base> + 0ADCh (m = 3)
<PCI_S0_REG_base> + 0B5Ch (m = 4)
<PCI_S0_REG_base> + 0BDCh (m = 5)
<PCI_S0_REG_base> + 0C5Ch (m = 6)
<PCI_S0_REG_base> + 0CDCh (m = 7)

Initial Value: 0000_0000h

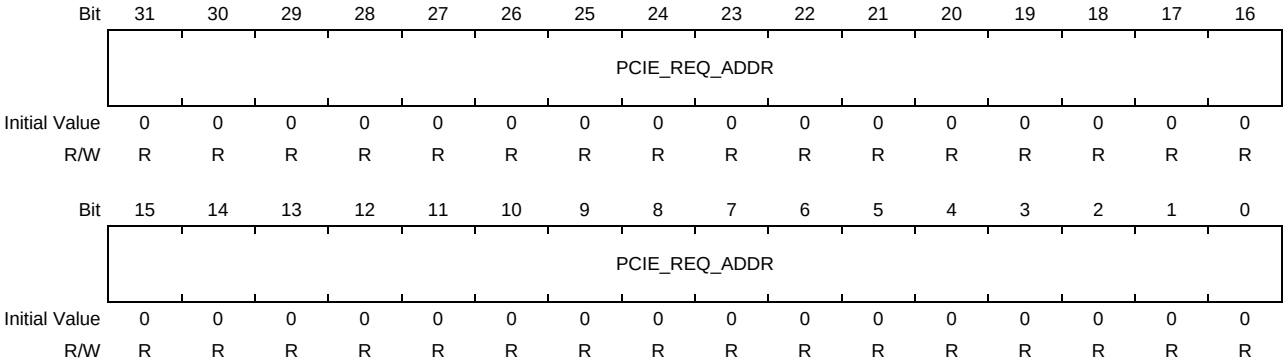


Table 36.4-66 PCI_RC_PREQAmU Register Contents

Bit Position	Bit Name	Description
31 to 0	PCIE_REQ_ADDR	Indicates the upper 32 bits of the address during PCIe transfer that is in progress or for the most recently completed transfer (common to register type and descriptor type).

(60) QUE Status Register m (PCI_RC_QUESTAm) (m = 0 to 7)

This register indicates the state of the descriptor queue.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0960h (m = 0)
<PCI_S0_REG_base> + 09E0h (m = 1)
<PCI_S0_REG_base> + 0A60h (m = 2)
<PCI_S0_REG_base> + 0AE0h (m = 3)
<PCI_S0_REG_base> + 0B60h (m = 4)
<PCI_S0_REG_base> + 0BE0h (m = 5)
<PCI_S0_REG_base> + 0C60h (m = 6)
<PCI_S0_REG_base> + 0CE0h (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	GO_LIST	LIST_NUM			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-67 PCI_RC_QUESTAm Register Contents

Bit Position	Bit Name	Description
31 to 5	—	Reserved. These bits are read as 0b.
4	GO_LIST	Indicates whether a descriptor list being executed is or is not present. 1b: Present 0b: Not present
3 to 0	LIST_NUM	Indicates the number of descriptor lists with which the queue for the given DMA channel has been loaded (any list currently being executed is not included). Attempts at making new entries in the queue while the value of this field is 8 (writing to the queue entry bits for the given channel) has no effect (will be ignored).

(61) DMAC Error Status Register m (PCI_RC_DMACESTAm) (m = 0 to 7)

This register indicates the error state of the DMAC.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0968h (m = 0)
<PCI_S0_REG_base> + 09E8h (m = 1)
<PCI_S0_REG_base> + 0A68h (m = 2)
<PCI_S0_REG_base> + 0AE8h (m = 3)
<PCI_S0_REG_base> + 0B68h (m = 4)
<PCI_S0_REG_base> + 0BE8h (m = 5)
<PCI_S0_REG_base> + 0C68h (m = 6)
<PCI_S0_REG_base> + 0CE8h (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	CFG_BM_DIS_EP	BME_SUP	BME_DOWN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	Debug	MOR_CD_PERR	MOR_CH_PERR	MOR_EP_PERR	MOR_STATUS			—	—	—	Debug		—	AXI_RESP	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-68 PCI_RC_DMACESTAm Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b.
18	CFG_BM_DIS_EP	Set when the unit is operating as an endpoint and the state of Bus Master Enable Off (configuration space 004h bit [2] = 0) is detected. The value is kept until CHm_ERR is cleared.
17	BME_SUP	Set when a suspend signal from PCIe is detected. The value is kept until CHm_ERR is cleared. This bit is only valid in endpoint mode.
16	BME_DOWN	Set when a stop signal from PCIe is detected. The value is kept until CHm_ERR is cleared.
15	—	Reserved. This bit is read as 0b.
14	Debug	Debug register
13	MOR_CD_PERR	Set when MOR_CD_PERR is detected. The value is kept until CHm_ERR is cleared.
12	MOR_CH_PERR	Set when MOR_CH_PERR is detected. The value is kept until CHm_ERR is cleared.
11	MOR_EP_ERR	Set when it is a poisoned completion. The value is kept until CHm_ERR is cleared.
10 to 8	MOR_STATUS	Indicates the MOR_STATUS value if MOR_STATUS is not 000b (success). The value is kept until CHm_ERR is cleared. 000b: Initial value 001b: Unsupported request 010b: CRS 011b: Completion timeout 100b: Completer abort 101b: Unexpected completion 110b: Reserved 111b: Mismatched length (length overrun)
7 to 5	—	Reserved. These bits are read as 0b.
4, 3	Debug	Debug register
2	—	Reserved. This bit is read as 0b.

Table 36.4-68 PCI_RC_DMACESTAm Register Contents (2/2)

Bit Position	Bit Name	Description
1, 0	AXI_RESP	Indicates a slave response in AXI Master transactions. This field is updated when CHm_ERR is set. The value is kept until CHm_ERR is cleared. 00b: Initial value. 01b: Reserved. 10b: SLVERR 11b: DECERR

(62) AXI Window Base m Register (PCI_RC_AWBASEm) (m = 0 to 7)

This register is for setting windows for address conversion in access from PCIe to AXI. It sets the base address on the PCI side. The areas are set on 4-Kbyte boundaries.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 1000h (m = 0)
<PCI_S0_REG_base> + 1010h (m = 1)
<PCI_S0_REG_base> + 1020h (m = 2)
<PCI_S0_REG_base> + 1030h (m = 3)
<PCI_S0_REG_base> + 1040h (m = 4)
<PCI_S0_REG_base> + 1050h (m = 5)
<PCI_S0_REG_base> + 1060h (m = 6)
<PCI_S0_REG_base> + 1070h (m = 7)

Initial Value: 0000_0000h

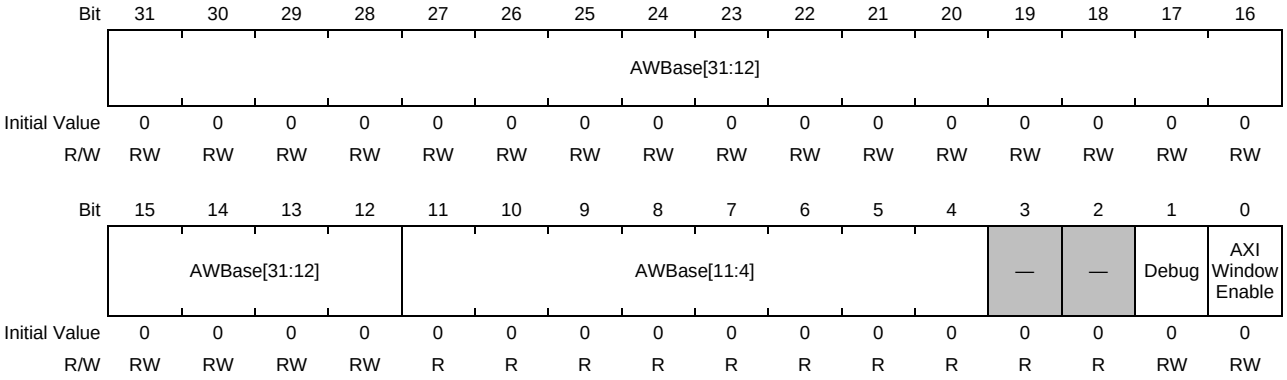


Table 36.4-69 PCI_RC_AWBASEm Register Contents

Bit Position	Bit Name	Description
31 to 12	AWBase[31:12]	Setting windows for address conversion in access from PCIe to AXI. The areas are set in 4-Kbyte boundaries.
11 to 4	AWBase[11:4]	Fixed to 0000_0000b.
3, 2	—	Reserved. These bits are read as 0b.
1	Debug	This register is for use in debugging by Renesas.
0	AXI Window Enable	Enable AXI windows. 0b: Disable windows. 1b: Enable windows.

(63) AXI Window Mask m Register (PCI_RC_AWMASKm) (m = 0 to 7)

This register is for setting windows for address conversion in access from PCIe to AXI. The window is set as the area corresponding to the number of set bits from the address set in the AWBase register. The area which can be set is 4K × 2^N bytes.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 1004h (m = 0)
<PCI_S0_REG_base> + 1014h (m = 1)
<PCI_S0_REG_base> + 1024h (m = 2)
<PCI_S0_REG_base> + 1034h (m = 3)
<PCI_S0_REG_base> + 1044h (m = 4)
<PCI_S0_REG_base> + 1054h (m = 5)
<PCI_S0_REG_base> + 1064h (m = 6)
<PCI_S0_REG_base> + 1074h (m = 7)

Initial Value: 0000_0FFFh

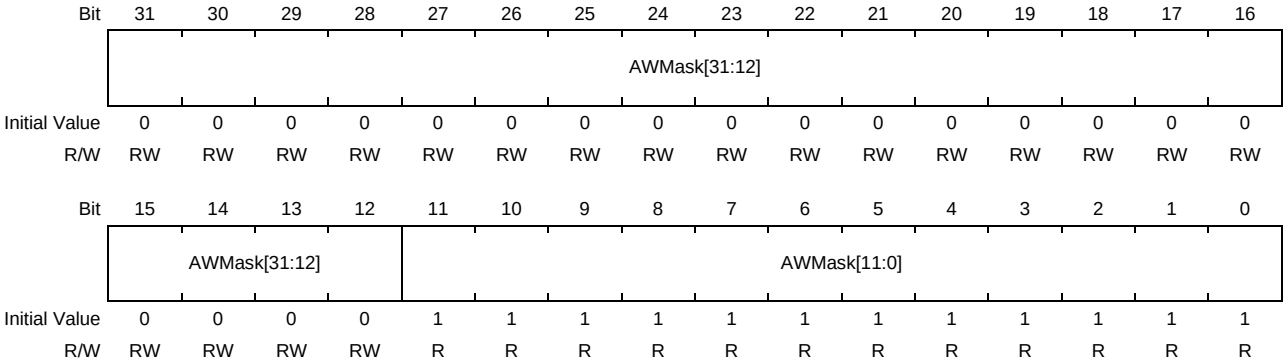


Table 36.4-70 PCI_RC_AWMASKm Register Contents

Bit Position	Bit Name	Description
31 to 12	AWMask[31:12]	The window is set as the area corresponding to the number of set bits from the address set in the AWBase register. Set 1b from the lowest-order bit. Accordingly, the area which can be set is 4K × 2^N bytes.
11 to 0	AWMask[11:4]	Fixed to 1111_1111_1111b.

(64) AXI Destination m Register (PCI_RC_ADESTm) (m = 0 to 7)

This register is for setting windows for address conversion in access from PCIe to AXI. The base address of the window in the address space on the AXI side is set. The areas are set on 4-Kbyte boundaries.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 1008h (m = 0)
<PCI_S0_REG_base> + 1018h (m = 1)
<PCI_S0_REG_base> + 1028h (m = 2)
<PCI_S0_REG_base> + 1038h (m = 3)
<PCI_S0_REG_base> + 1048h (m = 4)
<PCI_S0_REG_base> + 1058h (m = 5)
<PCI_S0_REG_base> + 1068h (m = 6)
<PCI_S0_REG_base> + 1078h (m = 7)

Initial Value: 0000_0000h

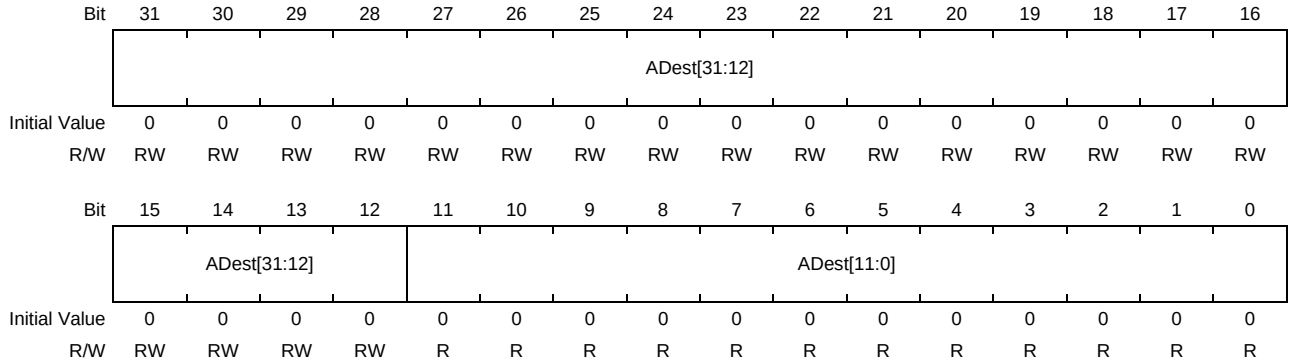


Table 36.4-71 PCI_RC_ADESTm Register Contents

Bit Position	Bit Name	Description
31 to 12	ADest[31:12]	The base address of the window in the address space on the AXI side is set. The areas are set on 4-Kbyte boundaries.
11 to 0	ADest[11:0]	Fixed to 0000_0000_0000b.

(65) PCIe Window Base m Register (PCI_RC_PWBASEm) (m = 0 to 7)

This register is for setting windows for address conversion in access from AXI to PCIe. It sets the base address on the AXI side. The areas are set on 4-Kbyte boundaries.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 1100h (m = 0)
<PCI_S0_REG_base> + 1110h (m = 1)
<PCI_S0_REG_base> + 1120h (m = 2)
<PCI_S0_REG_base> + 1130h (m = 3)
<PCI_S0_REG_base> + 1140h (m = 4)
<PCI_S0_REG_base> + 1150h (m = 5)
<PCI_S0_REG_base> + 1160h (m = 6)
<PCI_S0_REG_base> + 1170h (m = 7)

Initial Value: 0000_0000h

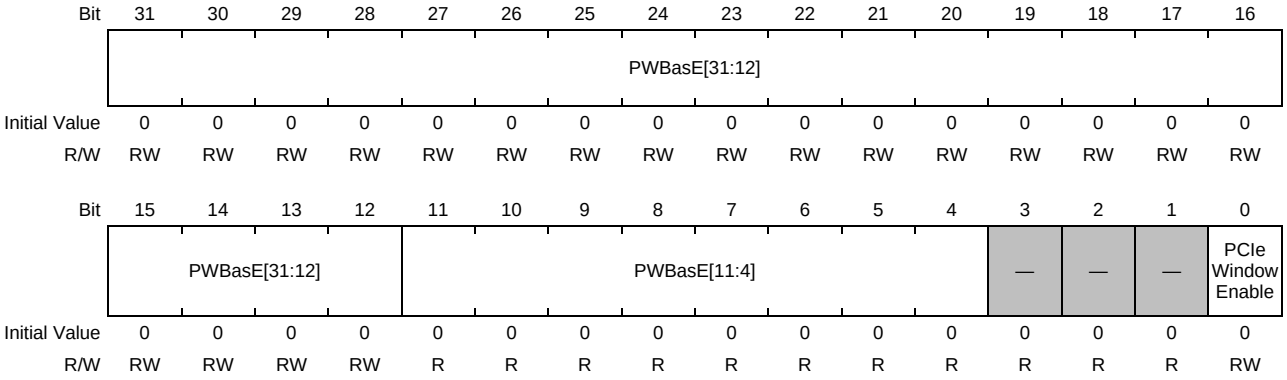


Table 36.4-72 PCI_RC_PWBASEm Register Contents

Bit Position	Bit Name	Description
31 to 12	PWBasE[31:12]	Setting windows for address conversion in access from AXI to PCIe. The areas are set in 4-Kbyte boundaries.
11 to 4	PWBasE[11:4]	Fixed to 0000_0000b.
3 to 1	—	Reserved. These bits are read as 0b.
0	PCIe Window Enable	Enable PCIe windows. 0b: Disable windows. 1b: Enable windows.

(66) PCIe Window Mask m Register (PCI_RC_PWMASKm) (m = 0 to 7)

This register is for setting windows for address conversion in access from AXI to PCIe. The window is set as the area corresponding to the number of set bits from the address set in the PWBase register.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 1104h (m = 0)
<PCI_S0_REG_base> + 1114h (m = 1)
<PCI_S0_REG_base> + 1124h (m = 2)
<PCI_S0_REG_base> + 1134h (m = 3)
<PCI_S0_REG_base> + 1144h (m = 4)
<PCI_S0_REG_base> + 1154h (m = 5)
<PCI_S0_REG_base> + 1164h (m = 6)
<PCI_S0_REG_base> + 1174h (m = 7)

Initial Value: 0000_0FFFh

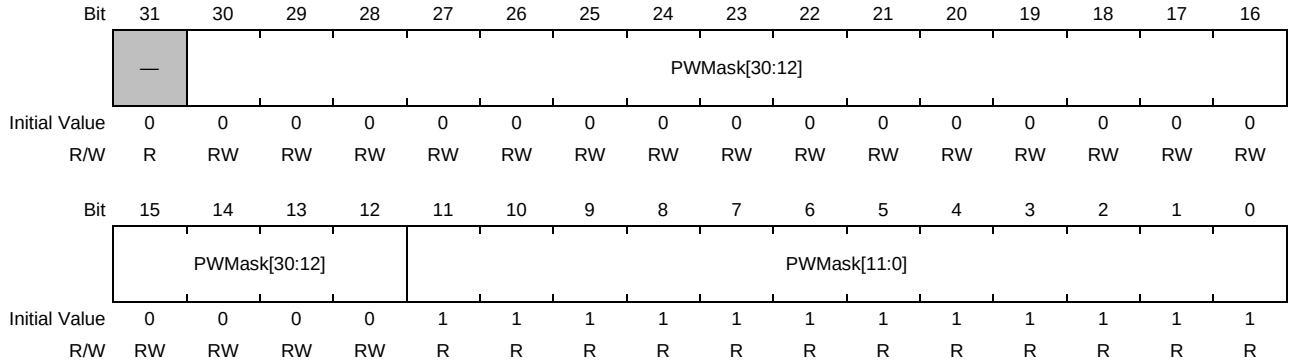


Table 36.4-73 PCI_RC_PWMASKm Register Contents

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b.
30 to 12	PWMask[30:12]	The window is set as the area corresponding to the number of set bits from the address set in the PWBase register. Set 1b from the lowest-order bit.
11 to 0	PWMask[11:0]	Fixed to 1111_1111_1111b.

(67) PCIe Destination m (Lower) Register (PCI_RC_PDESTLOm) (m = 0 to 7)

This register is for setting windows for address conversion in access from AXI to PCIe. The base address of the window in the address space on the AXI side is set. The areas are set on 4-Kbyte boundaries.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 1108h (m = 0)
<PCI_S0_REG_base> + 1118h (m = 1)
<PCI_S0_REG_base> + 1128h (m = 2)
<PCI_S0_REG_base> + 1138h (m = 3)
<PCI_S0_REG_base> + 1148h (m = 4)
<PCI_S0_REG_base> + 1158h (m = 5)
<PCI_S0_REG_base> + 1168h (m = 6)
<PCI_S0_REG_base> + 1178h (m = 7)

Initial Value: 0000_0000h

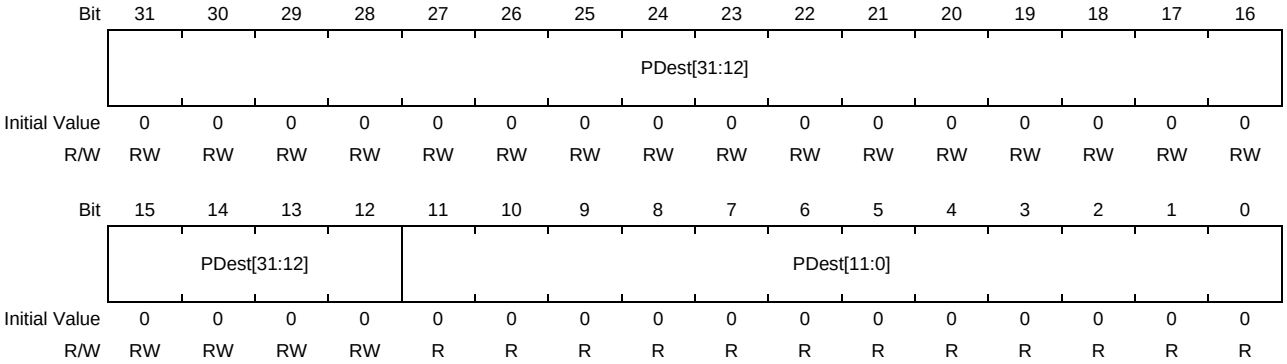


Table 36.4-74 PCI_RC_PDESTLOm Register Contents

Bit Position	Bit Name	Description
31 to 12	PDest[31:12]	The base address of the window in the address base on the AXI side is set. The areas are set on 4-Kbyte boundaries.
11 to 0	PDest[11:0]	Fixed to 0000_0000_0000b.

(68) PCIe Destination m (Upper) Register (PCI_RC_PDESTUPm) (m = 0 to 7)

This register is for setting windows for address conversion in access from AXI to PCIe. The base address of the window in the address space on the AXI side is set. The areas are set on 4-Kbyte boundaries.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 110Ch (m = 0)
<PCI_S0_REG_base> + 111Ch (m = 1)
<PCI_S0_REG_base> + 112Ch (m = 2)
<PCI_S0_REG_base> + 113Ch (m = 3)
<PCI_S0_REG_base> + 114Ch (m = 4)
<PCI_S0_REG_base> + 115Ch (m = 5)
<PCI_S0_REG_base> + 116Ch (m = 6)
<PCI_S0_REG_base> + 117Ch (m = 7)

Initial Value: 0000_0000h

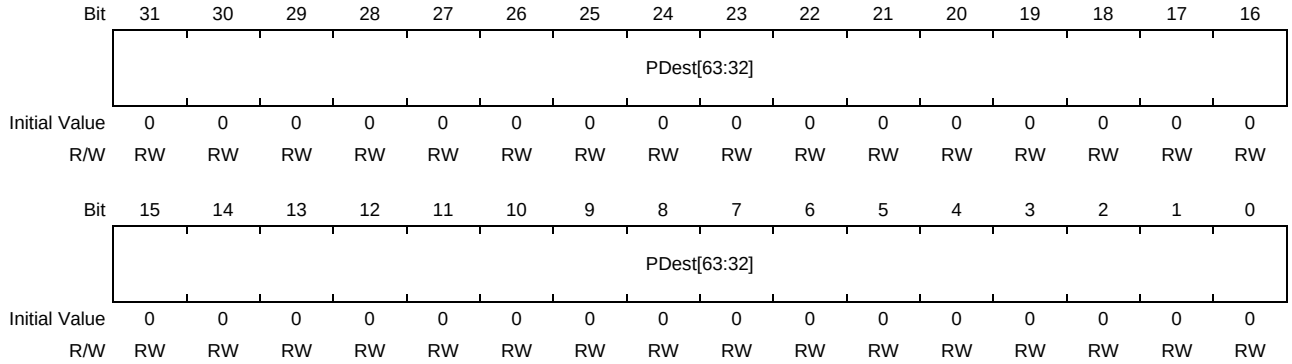


Table 36.4-75 PCI_RC_PDESTUPm Register Contents

Bit Position	Bit Name	Description
31 to 0	PDest[63:32]	The base address of the window in the address base on the AXI side is set. The areas are set on 4-Kbyte boundaries.

36.4.3.2 PCI Express Configuration Registers (Type1)

(1) Vendor and Device ID Register (PCI_RC_VID)

This register indicates the vendor and device ID. This register can be written during initialization.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6000h

Initial Value: Configurable Value

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Device ID															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Vendor ID															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-76 PCI_RC_VID Register Contents

Bit Position	Bit Name	Description
31 to 16	Device ID	Indicates the manufacturer. Set a fixed value.
15 to 0	Vendor ID	Used to identify devices manufactured by the manufacturer indicated by the vendor ID. Set a fixed value.

Table 36.4-77 Valid Reset Signal

Reset Signal	Device ID	Vendor ID
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		

(2) Command and Status Register (PCI_RC_COM_STA)

This register specifies the command and the status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6004h

Initial Value: 0010_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Detected Parity Error	Signaled System Error	Received Master Abort	Received Target Abort	Signaled Target Abort	DEVSEL Timing		Master Data Parity Error	—	—	—	Capabilities List	Interrupt Status	—	—	Immediate Readiness
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W	R	RW1	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	Interrupt Disable	—	SERR# Enable	—	Parity Error Response	—	—	—	Bus Master Enable	Memory Space Enable	IO Space Enable
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	R	RW	R	RW	R	R	R	RW	RW	R

Table 36.4-78 PCI_RC_COM_STA Register Contents (1/2)

Bit Position	Bit Name	Description
31	Detected Parity Error	Does not apply to root complex devices. Fixed to 0b.
30	Signaled System Error	Set to 1b when this unit has transmitted an ERR_FATAL or ERR_NONFATAL message while the SERR Enable bit is 1b.
29	Received Master Abort	Does not apply to root complex devices. Fixed to 0b.
28	Received Target Abort	Does not apply to root complex devices. Fixed to 0b.
27	Signaled Target Abort	Does not apply to root complex devices. Fixed to 0b.
26, 25	DEVSEL Timing	Reserved, Does not apply to PCI Express.
24	Master Data Parity Error	Does not apply to root complex devices. Fixed to 0b.
23 to 21	—	Reserved. These bits are read as 0b.
20	Capabilities List	Fixed to 1b because all PCI Express devices by definition have PCI Express capability.
19	Interrupt Status	Indicates the interrupt state of the device.
18, 17	—	Reserved. These bits are read as 0b.
16	Immediate Readiness	Fixed to 0b.
15 to 11	—	Reserved. These bits are read as 0b.
10	Interrupt Disable	Disables transmission of Assert_INTx messages. Not used for root complex devices.
9	—	Reserved. This bit is read as 0b.
8	SERR# Enable	When set to 1b, the root complex is notified of a non-fatal error or fatal error through a message transaction. *Note*: Even if this bit is not set, the root complex is notified of an error through a message transaction when the Error Reporting bit in the Device Control register of PCI Express Capability is set to 1b.
7	—	Reserved. This bit is read as 0b.

Table 36.4-78 PCI_RC_COM_STA Register Contents (2/2)

Bit Position	Bit Name	Description
6	Parity Error Response	Controls operation when a poisoned TLP is transmitted or received. *Note*: Errors are logged in the Detected Parity Error field of the Status register, the Device Status register of the PCI Express Capability, and the Uncorrectable Error Status register of the Advanced Error Reporting Capability, regardless of the setting of this bit.
5 to 3	—	Reserved. These bits are read as 0b.
2	Bus Master Enable	Controls whether to operate as a bus mater.
1	Memory Space Enable	Controls whether the device returns a response in the case of access to the memory space.
0	I/O Space Enable	Fixed to 0b. Access to the I/O space is not supported.

Table 36.4-79 Valid Reset Signal

Reset Signal	Signaled System Error	Capabilities List	Interrupt Status	Interrupt Disable	SERR# Enable	Parity Error Response
RST_LOAD_B						
RST_RSM_B						
RST_CFG_B	✓	✓	✓	✓	✓	✓

Reset Signal	Bus Master Enable	Memory Space Enable
RST_LOAD_B		
RST_RSM_B		
RST_CFG_B	✓	✓

(3) Revision ID and Class Code Register (PCI_RC_RID_CC)

This register indicates the revision ID and the class code.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6008h

Initial Value: Configurable Value

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Class Code															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Class Code								Revision ID							
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-80 PCI_RC_RID_CC Register Contents

Bit Position	Bit Name	Description
31 to 8	Class Code	Indicates information on the type and function of the device and their values are defined by the PCI special interest group (PCI-SIG) as follows. 31 to 24: Base class 23 to 16: Sub-class 15 to 8: Programming interface Set to the fixed value. The initial value can be set using parameters.
7 to 0	Revision ID	An 8-bit ID used to indicate the revision number of a specific device specified by its vendor and device IDs. Set the fixed value. The initial value can be set using parameters.

Table 36.4-81 Valid Reset Signal

Reset Signal	Class Code	Capabilities List
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		

(4) Cache Line and Header Type Register (PCI_RC_CL_HT)

This register indicates the cache line and the header type.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 600Ch

Initial Value: 0001_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BIST								Header Type							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Master Latency Timer								Cache Line Size							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.4-82 PCI_RC_CL_HT Register Contents

Bit Position	Bit Name	Description
31 to 24	BIST	Fixed to 00h because the BIST register function is not supported.
23 to 16	Header Type	Root complex: Fixed to 01h.
15 to 8	Master Latency Timer	Fixed to 00h because the Master Latency Timer register is not used for PCI Express.
7 to 0	Cache Line Size	Though these bits are implemented as a readable/writable field for legacy compatibility, the setting has no effect on this device.

Table 36.4-83 Valid Reset Signal

Reset Signal	Cache Line Size
RST_LOAD_B	
RST_RSM_B	
RST_CFG_B	✓

(5) Base Address Register 0 (PCI_RC_BAR0)

This register forms a 64-bit memory space in combination with Base Address Register 1 (BAR1).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6010h

Initial Value: 0000_0004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register 0															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register 0												Prefetch	Type	—	Memory Space Indicator
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	HwInit	R	R	R

Table 36.4-84 PCI_RC_BAR0 Register Contents

Bit Position	Bit Name	Description
31 to 4	Base Address Register 0	Indicates the base address. Some lower bits of this field are implemented as read-only bits that are fixed to 0b to suit the required size of the address block. Read-only bits of this unit can be set in Base Address Register Mask00 (Lower) (address: <PCI_S0_REG_base> + 60A0h).
3	Prefetch	0b: Disable 1b: Enable This register can be written during initialization.
2	Type	0b: 32-bit address 1b: 64-bit address. A 64-bit address is used. Fixed to 1b.
1	—	Reserved. This bit is read as 0b.
0	Memory Space Indicator	Indicates the memory space. Fixed to 0b.

Table 36.4-85 Valid Reset Signal

Reset Signal	Base Address Register 0	Prefetch
RST_LOAD_B		✓
RST_RSM_B		
RST_CFG_B	✓	

(6) Base Address Register 1 (PCI_RC_BAR1)

This register forms a 64-bit memory space in combination with Base Address Register 0 (BAR0).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6014h

Initial Value: 0000_0000h

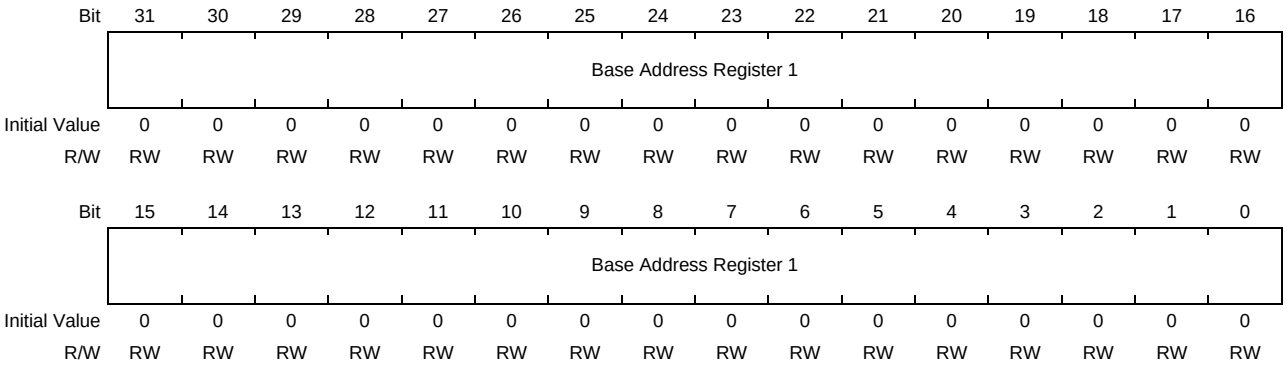


Table 36.4-86 PCI_RC_BAR1 Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register 1	Base Address Register 1 (64-bit Upper Address) Indicates the upper 32 bits of the base address.

Table 36.4-87 Valid Reset Signal

Reset Signal	Base Address Register 1
RST_LOAD_B	
RST_RSM_B	
RST_CFG_B	✓

(7) Capabilities Pointer Register (PCI_RC_CP)

This register indicates the I/O base, limit, and secondary status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6034h

Initial Value: 0000_0040h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Capability Pointer							
Initial Value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-88 PCI_RC_CP Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	Capability Pointer	Capability implementation start address. The PCI power management capability is implemented from 40h. This register can be written during initialization. The lower 2 bits are fixed to 00b (reserved) and cannot be written on the AXI side.

Table 36.4-89 Valid Reset Signal

Reset Signal	Capability Pointer [7:2]
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	

(8) Interrupt Register (PCI_RC_INT)

This register controls the bridge and enables the interrupt status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 603Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	Discard Timer SERR Enable	Discard Timer Status	Secondary Discard Timer	Primary Discard Timer	Fast Back-to-Back Enable	Secondary Bus Reset	Master Abort Mode	VGA 16bit Decode	VGA Enable	ISA Enable	SERR# Enable	Parity Error Response Enable
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	RW	R	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Interrupt Pin								Interrupt Line							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.4-90 PCI_RC_INT Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b.
27	Discard Timer SERR Enable	Reserved: Does not apply to PCI Express (fixed to 0b).
26	Discard Timer Status	Reserved: Does not apply to PCI Express (fixed to 0b).
25	Secondary Discard Timer	Reserved: Does not apply to PCI Express (fixed to 0b).
24	Primary Discard Timer	Reserved: Does not apply to PCI Express (fixed to 0b).
23	Fast Back-to-Back Enable	Reserved: Does not apply to PCI Express (fixed to 0b).
22	Secondary Bus Reset	The hot reset state is entered by writing 1b.
21	Master Abort Mode	Reserved: Does not apply to PCI Express.
20	VGA 16-bit Decode	The initial value is 0b. It is not used in this unit.
19	VGA Enable	The initial value is 0b. It is not used in this unit.
18	ISA Enable	The initial value is 0b. It is not used in this unit.
17	SERR# Enable	INT_SERR* interrupt pin notification is enabled by writing 1b.
16	Parity Error Response Enable	Writing 1b sets the Master Data Parity Error bit of the Secondary Status register when a poisoned TLP is received.
15 to 8	Interrupt Pin	Fixed to 00h. This register can be written during initialization.
7 to 0	Interrupt Line	Fixed to 00h.

Table 36.4-91 Valid Reset Signal

Reset Signal	Secondary Bus Reset	VGA 16-bit Decode	VGA Enable	ISA Enable	SERR# Enable	Parity Error Response Enable
RST_LOAD_B						
RST_RSM_B						
RST_CFG_B	✓	✓	✓	✓	✓	✓

Reset Signal	Interrupt Pin	Interrupt Line
RST_LOAD_B	✓	
RST_RSM_B		
RST_CFG_B		✓

(9) PM Capabilities Register (PCI_RC_PMC)

This register indicates various support information.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6040h

Initial Value: 4803_6001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PME Support					D2 Support	D1 Support	AUX_Current			DSI	Immediate_Readiness_on_Return_to_D0	PME Clock	Version		
Initial Value	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	1
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability ID							
Initial Value	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-92 PCI_RC_PMC Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 27	PME Support	Indicates whether each device state supports PME. This register can be written during initialization. xxxx_1b: Supports D0. xxx1_xb: Supports D1. xx1x_xb: Supports D2. x1xx_xb: Supports D3 hot. 1xxx_xb: Supports D3 cold (not supported).
26	D2 Support	Indicates whether to support the D2 power management state. This register can be written during initialization. 0b: Not supported 1b: Supported
25	D1 Support	Indicates whether to support the D1 power management state. This register can be written during initialization. 0b: Not supported 1b: Supported
24 to 22	AUX_Current	Indicates the 3.3Vaux auxiliary current (the maximum current that the auxiliary power source can supply). This register can be written during initialization. 111b: 375 mA 110b: 320 mA 101b: 250 mA 100b: 220 mA 011b: 160 mA 010b: 100 mA 001b: 55 mA 000b: 0 (self-powered) Reading these bits returns 000b (AUX is not supported).
21	Device Specific Initialization (DSI)	Indicates whether to use DSI (Device Specific Initialization). This register can be written during initialization. 0b: Not supported 1b: Supported

Table 36.4-92 PCI_RC_PMC Register Contents (2/2)

Bit Position	Bit Name	Description
20	Immediate_Readiness_on_Return_to_D0	Fixed to 0b.
19	PME Clock	Reserved: Does not apply to PCI Express.
18 to 16	Version	Fixed to 011b. PCI Power Management Interface Specification Rev.1.2
15 to 8	Next Capability Pointer	Indicates the PCI Express Capability start address.
7 to 0	Capability ID	Indicates the PCI Power Management Capability. Fixed to 01h.

Table 36.4-93 Valid Reset Signal

Reset Signal	PME Support	D2 Support	D1 Support	AUX_Current	DSI	Version
RST_LOAD_B	✓	✓	✓	✓	✓	✓
RST_RSM_B						
RST_CFG_B						

Reset Signal	Next Capability Pointer [7:2]
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	

(10) PM Status/Control Register (PCI_RC_PMSC)

This register indicates and controls the PME status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6044h

Initial Value: 0000_0008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Data								Bus Power/Clock Control Enable	B2/B3/Support	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PME Status	Data Scale		Data Select				PME Enable	—	—	—	—	No_Soft_Reset	—	PowerState	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W	RW1	R	R	R	R	R	R	RW	R	R	R	R	R	R	RW	RW

Table 36.4-94 PCI_RC_PMSC Register Contents

Bit Position	Bit Name	Description
31 to 24	Data	Not supported
23	Bus Power/Clock Control Enable	Not supported
22	B2/B3 Support	Not supported
21 to 16	—	Reserved. These bits are read as 0b.
15	PME Status	Indicates that a PME assertion factor has occurred. It is cleared by writing 1b. Writing 0b has no effect.
14, 13	Data Scale	Not supported
12 to 9	Data Select	Not supported
8	PME Enable	Controls the assertion of PME. When this bit is 1b, assertion of PME is enabled. At this time, PME is asserted when PME_status is set. PCI Express handles wake-up processing on links, and then asserts PME by sending a PM_PME message. *Note*: According to the value of PME support [4] (PME Support by D3cold), the specification is as follows: PME Support [4] = 1b Reset: RST_RSM_B PME Support [4] = 0b Reset: RST_CFG_B
7 to 4	—	Reserved. These bits are read as 0b.
3	No_Soft_Reset	Indicates that an internal reset is not initiated in the device in a power state transition from D3 hot to D0.
2	—	Reserved. This bit is read as 0b.
1, 0	PowerState	Sets the PCI device state. 00b: D0 (initial value) 01b: D1 (setting prohibited) 10b: D2 (setting prohibited) 11b: D3 hot

Table 36.4-95 Valid Reset Signal

Reset Signal	PME Enable	PowerState
RST_LOAD_B		
RST_RSM_B	✓	
RST_CFG_B		✓

(11) PCI Express Capability Register (PCI_RC_PCIEC)

This register indicates the PCIe capability.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6060h

Initial Value: 0042_0010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	Interrupt Message Number					Slot Implemented	Device/Port Type				Capability Version			
Initial Value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
R/W	R	R	R	R	R	R	R	HwInit	R	R	R	R	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability ID							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	R	R	R	R	R	R	R	R

Table 36.4-96 PCI_RC_PCIEC Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29 to 25	Interrupt Message Number	Fixed to 00_000b.
24	Slot Implemented	The value 1b indicates that the PCI Express link (down port) is connected to the slot. This register can be written during initialization.
23 to 20	Device/Port Type	Indicates that the device is a PCI Express root complex device. 0000b PCI Express Endpoint device 0001b Legacy PCI Express Endpoint device 0100b Root Port of PCI Express Root Complex (initial value) 0101b Upstream Port of PCI Express Switch 0110b Downstream Port of PCI Express Switch 0111b PCI Express-to-PCI/PCI-X Bridge 1000b PCI/PCI-X-to-PCI Express Bridge 1001b Root Complex Integrated Endpoint Device 1010b Root Complex Event Collector All other encodings are reserved.
19 to 16	Capability Version	Indicates the PCI Express Capability Structure version. Fixed to 0010b. This register can be written during initialization.
15 to 8	Next Capability Pointer	Indicates that a pointer to this capability list as the last list (fixed to 00h). The lower 2 bits [9:8] are fixed to 00b. This register can be written during initialization.
7 to 0	Capability ID	Indicates the PCI Express capability. Fixed to 10h.

Table 36.4-97 Valid Reset Signal

Reset Signal	Slot Implemented	Next Capability Pointer
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		

(12) Device Capabilities Register (PCI_RC_DEVC)

This register indicates the device capability.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6064h

Initial Value: 0000_8000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	Function Level Reset Capability	Captured Slot Power Limit Scale		Captured Slot Power Limit Value								—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Role-Based Error Reporting	—	—	—	Endpoint L1 Acceptable Latency			Endpoint L0s Acceptable Latency			Extended Tag Field Supported	Phantom Functions Supported		Max_Payload_Size Supported		
Initial Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-98 PCI_RC_DEVC Register Contents

Bit Position	Bit Name	Description
31 to 29	—	Reserved. These bits are read as 0b.
28	Function Level Reset Capability	Does not apply to root complex devices. Fixed to 0b.
27, 26	Captured Slot Power Limit Scale	Does not apply to root complex devices. Fixed to 00b.
25 to 18	Captured Slot Power Limit Value	Does not apply to root complex devices. Fixed to 00h.
17, 16	—	Reserved. These bits are read as 0b.
15	Role-Based Error Reporting	Set to 1b when error reporting (compliant with Rev 1.1 or later) is implemented. Fixed to 1b in this core.
14 to 12	—	Reserved. These bits are read as 0b.
11 to 9	Endpoint L1 Acceptable Latency	Does not apply to root complex devices. Fixed to 000b.
8 to 6	Endpoint L0s Acceptable Latency	Does not apply to root complex devices. Fixed to 000b.
5	Extended Tag Field Supported	0b: 5-bit tag field supported 1b: 8-bit tag field supported Fixed to 1b when 10-bit tags are used.
4, 3	Phantom Functions Supported	Phantom functions are not supported. Fixed to 00b.
2 to 0	Max_Payload_ Size Supported	000b: 128B max payload size (initial value) 001b: 256B max payload size 010b: 512B max payload size 011b: 1024B max payload size 100b: 2048B max payload size 101b: 4096B max payload size 110b: Reserved 111b: Reserved

Table 36.4-99 Valid Reset Signal

Reset Signal	Extended Tag Field Supported	Max_Payload_Size Support
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		

(13) Device Control/Status Register (PCI_RC_DEVCS)

This register controls the device and indicates the device status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6068h

Initial Value: 0000_2010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	Emergency Power Reduction Detected	Transaction Pending	AUX Power Detected	Unsupported Request Detected	Fatal Error Detected	Non-Fatal Error Detected	Correctable Error Detected
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW1	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Initiate Function Level Reset	Max_Read_Request_Size			Enable No Snoop	AUX Power PM Enable	Phantom Functions Enable	Extended Tag Field Enable	Max_Payload_Size			Enable Relaxed Ordering	Unsupported Request Reporting Enable	Fatal Error Reporting Enable	Non-Fatal Error Reporting Enable	Correctable Error Reporting Enable
Initial Value	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W	R	RW	RW	RW	R	RW	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.4-100 PCI_RC_DEVCS Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b.
22	Emergency Power Reduction Detected	Not supported. Fixed to 0b.
21	Transaction Pending	Does not apply to root complex devices. Fixed to 0b.
20	AUX Power Detected	Indicates that auxiliary power was detected (AUX is not supported).
19	Unsupported Request Detected	Indicates that an unsupported request error was detected. The value 1b indicates that the error was detected. It is cleared by writing 1b. Writing 0b has no effect.
18	Fatal Error Detected	Indicates that a fatal error was detected. The value 1b indicates that the error was detected. It is cleared by writing 1b. Writing 0b has no effect.
17	Non-Fatal Error Detected	Indicates that a non-fatal error was detected. The value 1b indicates that the error was detected. It is cleared by writing 1b. Writing 0b has no effect.
16	Correctable Error Detected	Indicates that a correctable error was detected. The value 1b indicates that the error was detected. It is cleared by writing 1b. Writing 0b has no effect.
15	Initiate Function Level Reset	A write of 1b initiates a function level reset to the Function. The value read by software from this bit is always 0b.
14 to 12	Max_Read_Request_Size	Sets the maximum read request size. 000b: 128-byte max read request size 001b: 256-byte max read request size 010b: 512-byte max read request size (initial value) 011b: 1024-byte max read request size 100b: 2048-byte max read request size 101b: 4096-byte max read request size 110b: Reserved 111b: Reserved
11	Enable No Snoop	This unit does not use No Snoop Attribute as a requester.

Table 36.4-100 PCI_RC_DEVCS Register Contents (2/2)

Bit Position	Bit Name	Description
10	Auxiliary (AUX) Power PM Enable	Sets whether to support auxiliary (AUX) power (AUX is not supported). 1b: Supported 0b: Not supported (initial value) When this bit is set to 1b, set AUX_Current (Power Management Capabilities register)
9	Phantom Functions Enable	Phantom functions are not supported. Fixed to 0b.
8	Extended Tag Field Enable	Extended tags are not supported. Only 5-bit tags are used.
7 to 5	Max_Payload_Size	Sets the maximum payload size. 000b: 128-byte max payload size (initial value) 001b: 256-byte max payload size 010b: 512-byte max payload size 011b: 1024-byte max payload size 100b: 2048-byte max payload size 101b: 4096-byte max payload size 110b: Reserved 111b: Reserved
4	Enable Relaxed Ordering	Sets whether to support relaxed ordering as a requester. 1b: Supported 0b: Not supported
3	Unsupported Request Reporting Enable	Controls the generation of ERR_NONFATAL and ERR_FATAL messages in response to the detection of unsupported requests. The value 1b enables generation of messages.
2	Fatal Error Reporting Enable	Controls the generation of ERR_FATAL messages. The value 1b enables generation of messages.
1	Non-Fatal Error Reporting Enable	Controls the generation of ERR_NONFATAL messages. The value 1b enables generation of messages.
0	Correctable Error Reporting Enable	Controls the generation of ERR_COR messages. The value 1b enables generation of messages.

Table 36.4-101 Valid Reset Signal

Reset Signal	Unsupported Request Detected	Fatal Error Detected	Non-Fatal Error Detected	Correctable Error Detected	Max_Read_Request_Size	AUX Power PM Enable
RST_LOAD_B						
RST_RSM_B						✓
RST_CFG_B	✓	✓	✓	✓	✓	

Reset Signal	Extended Tag Field Enable	Max_Payload_Size	Enable Relaxed Ordering	Unsupported Request Reporting Enable	Fatal Error Reporting Enable
RST_LOAD_B					
RST_RSM_B					
RST_CFG_B	✓	✓	✓	✓	✓

Reset Signal	Non-Fatal Error Reporting Enable	Correctable Error Reporting Enable
RST_LOAD_B		
RST_RSM_B		
RST_CFG_B	✓	✓

(14) Link Capabilities Register (PCI_RC_LINKC)

This register indicates the link capabilities. This register can be written during initialization.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 606Ch

Initial Value: 0073_6C22h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Port Number								—	ASPM Optionality Compliance	Link Bandwidth Notification Capability	Data Link Layer Link Active Reporting Capable	Surprise Down Error Reporting Capable	Clock Power Management	L1 Exit Latency	
Initial Value	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	L1 Exit Latency	L0s Exit Latency			Active State Power Management Support		Maximum Link Width						Supported Link Speed			
Initial Value	0	1	1	0	1	1	0	0	0	0	1	0	0	0	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-102 PCI_RC_LINKC Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 24	Port Number	Indicates the port number of the PCI Express link.
23	—	Reserved. This bit is read as 0b.
22	ASPM Optionality Compliance	Fixed to 1b.
21	Link Bandwidth Notification Capability	Indicates support for the Link Bandwidth Notification status and interrupt mechanisms.
20	Data Link Layer Link Active Reporting Capable	Indicates that reporting of the DL_Active state of the data link control and management state machine is supported.
19	Surprise Down Error Reporting Capable	Fixed to 0b. Detection and reporting of a surprise down error are not supported.
18	Clock Power Management	Does not apply to root complex devices. Fixed to 0b.
17 to 15	L1 Exit Latency	000b: Less than 1µs 001b: 1 µs to less than 2 µs 010b: 2 µs to less than 4 µs 011b: 4 µs to less than 8 µs 100b: 8 µs to less than 16 µs 101b: 16 µs to less than 32 µs 110b: 32 µs to 64 µs (initial value) 111b: More than 64 µs

Table 36.4-102 PCI_RC_LINKC Register Contents (2/2)

Bit Position	Bit Name	Description
14 to 12	L0s Exit Latency	000b: Less than 64 ns 001b: 64 ns to less than 128 ns 010b: 128 ns to less than 256 ns 011b: 256 ns to less than 512 ns 100b: 512 ns to less than 1 µs 101b: 1 µs to less than 2 µs 110b: 2 µs to 4 µs (initial value) 111b: More than 4 µs
11, 10	Active State Power Management (ASPM) Support	00b: Reserved 01b: L0s entry supported 10b: Reserved 11b: L0s and L1 entry supported (initial value)
9 to 4	Maximum Link Width	00_0000b: Reserved 00_0001b: ×1 00_0010b: ×2 (initial value) 00_0100b: ×4 (setting prohibited) 00_1000b: ×8 (setting prohibited) 00_1100b: ×12 (setting prohibited) 01_0000b: ×16 (setting prohibited) 10_0000b: ×32 (setting prohibited)
3 to 0	Supported Link Speed	0001b: 2.5 GT/s link speed supported 0010b: 5.0 GT/s and 2.5 GT/s link speeds supported (initial value) All other encodings are reserved.

Table 36.4-103 Valid Reset Signal

Reset Signal	ASPM Optionality Compliance	Link Bandwidth Notification Capability	Data Link Layer Link Active Reporting Capable	Surprise Down Error Reporting Capable	L1 Exit Latency	L0s Exit Latency
RST_LOAD_B	✓	✓	✓	✓	✓	✓
RST_RSM_B						
RST_CFG_B						

Reset Signal	Active State Power Management Support	Maximum Link Width	Supported Link Speed
RST_LOAD_B	✓	✓	✓
RST_RSM_B			
RST_CFG_B			

(15) Link Control/Status Register (PCI_RC_LINKCS)

This register controls the link and indicates the link status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6070h

Initial Value: 1000_0008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Link Autonomous Bandwidth Status	Link Bandwidth Management Status	Data Link Layer Link Active	Slot Clock Configuration	Link Training	—	Negotiated Link Width						Current Link Speed			
Initial Value	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	RW1	R	HwInit	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Link Autonomous Bandwidth Interrupt Enable	Link Bandwidth Management Interrupt Enable	Hardware Autonomous Width Disable	Enable Clock Power Management	Extended Synch	Common Clock Configuration	Retrain Link	Link Disable	Read Completion Boundary	—	Active State Power Management Control	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W	R	R	R	R	RW	RW	RW	R	RW	RW	RW	RW	R	R	RW	RW

Table 36.4-104 PCI_RC_LINKCS Register Contents (1/2)

Bit Position	Bit Name	Description
31	Link Autonomous Bandwidth Status	This bit is output when Link Autonomous Bandwidth Interrupt Enable is asserted. It is cleared by writing 1b. Writing 0b has no effect.
30	Link Bandwidth Management Status	This bit is output when Link Bandwidth Management Interrupt Enable is asserted. It is cleared by writing 1b. Writing 0b has no effect.
29	Data Link Layer Link Active	1b indicates that the data link layer is in the link-active state.
28	Slot Clock Configuration	Indicates that the common reference clock with the EP is in use. 0b: The reference clock for the connector is not in use. 1b: The reference clock for the connector is in use (initial value). This register can be written during initialization.
27	Link Training	Exit the configuration or recovery state to clear this bit. The value 1b indicates that the LTSSM of the physical layer is in the configuration state or recovery state.
26	—	Reserved. This bit is read as 0b.
25 to 20	Negotiated Link Width	Indicates the link width established as a result of negotiation. 00_0001b: ×1 00_0010b: ×2 00_0100b: ×4 00_1000b: ×8 00_1100b: ×12 01_0000b: ×16 10_0000b: ×32 All other encodings are reserved.

Table 36.4-104 PCI_RC_LINKCS Register Contents (2/2)

Bit Position	Bit Name	Description
19 to 16	Current Link Speed	0001b: 2.5GT/s PCI Express link 0010b: 5.0 GT/s PCI Express link 0011b: 8.0 GT/s PCI Express link 0100b: 16.0 GT/s PCI Express link 0000b during reset period.
15 to 12	—	Reserved. These bits are read as 0b.
11	Link Autonomous Bandwidth Interrupt Enable	Controls the generation of interrupts in response to the setting of the Link Autonomous Bandwidth Management Status bit (bit 31). 0b: Interrupts disabled (initial value) 1b: Interrupts enabled
10	Link Bandwidth Management Interrupt Enable	Controls the generation of interrupts in response to the setting of the Link Bandwidth Status bit (bi t30). 0b: Interrupts disabled (initial value) 1b: Interrupts enabled
9	Hardware Autonomous Width Disable	Disables a link width change. 0b: Link width change enabled (initial value) 1b: Link width change disabled
8	Enable Clock Power Management	Does not apply to root complex devices. Fixed to 0b.
7	Extended Synch	Set this bit to 1b to transmit 4096 FTS ordered sets at the time of a transition from L0s to L0. Also, 1024 TS1 ordered sets are transmitted at the beginning of the recovery state in a transition from L1 to L0. The initial value is 0b.
6	Common Clock Configuration	Sets whether a common reference clock is used. 0b: A non-common reference clock is supplied (initial value). 1b: A common reference clock is supplied.
5	Retrain Link	Setting this bit to 1b initiates link retraining by directing the LTSSM to the recovery state. The value read is always 0b.
4	Link Disable	Setting this bit to 1b forces the LTSSM to transition to the disabled state.
3	Read Completion Boundary (RCB)	0b: 64 bytes 1b: 128 bytes (initial value)
2	—	Reserved. This bit is read as 0b.
1, 0	Active State Power Management (ASPM) Control	Sets the level of permission for active-state power management. 00b: Disabled (initial value) 01b: L0s entry supported 10b: Reserved 11b: L0s and L1 entry supported

Table 36.4-105 Valid Reset Signal

Reset Signal	Link Autonomous Bandwidth Status	Link Bandwidth Management Status	Slot Clock Configuration	Link Autonomous Bandwidth Interrupt Enable	Link Bandwidth Management Interrupt Enable	Hardware Autonomous Width Disable
RST_LOAD_B			✓			
RST_RSM_B						
RST_CFG_B	✓	✓		✓	✓	✓

Reset Signal	Enable Clock Power Management	Extended Synch	Common Clock Configuration	Retrain Link	Link Disable	Active State Power Management Control
RST_LOAD_B						
RST_RSM_B						
RST_CFG_B	✓	✓	✓	✓		✓

(16) Device Capabilities 2 Register (PCI_RC_DEVC2)

This register indicates the device capability.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6084h

Initial Value: 0000_0012h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	Emergency Power Reduction Initialization Required	Emergency Power Reduction Supported		—	—	—	—	OBFF Supported		10-Bit Tag Requester Supported	10-Bit Tag Completer Supported
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	LTR Mechanism Supported	—	—	—	—	—	—	Completion Timeout Disable Supported	Completion Timeout Ranges Supported			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	HwInit	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-106 PCI_RC_DEVC2 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 27	—	Reserved. These bits are read as 0b.
26	Emergency Power Reduction Initialization Required	Emergency Power Reduction Initialization Required. Not supported. Fixed to 0b.
25, 24	Emergency Power Reduction Supported	Emergency Power Reduction Supported Not supported. Fixed to 0b.
23 to 20	—	Reserved. These bits are read as 0b.
19, 18	OBFF Supported	00b (not supported). This register can be written during initialization.
17	10-Bit Tag Requester Supported	10-Bit Tag (Requester) support. This register can be written during initialization. 0b: Not supported (initial value) 1b: Supported. Fixed to 0b.
16	10-Bit Tag Completer Supported	10-Bit Tag (Completer) support. This register can be written during initialization. 0b: Not supported (initial value) 1b: Supported.
15 to 12	—	Reserved. These bits are read as 0b.
11	LTR Mechanism Supported	Sets whether Latency Tolerance Reporting (LTR) is supported. This register can be written during initialization. 0b: Not supported 1b: Supported
10 to 5	—	Reserved. These bits are read as 0b.

Table 36.4-106 PCI_RC_DEVC2 Register Contents (2/2)

Bit Position	Bit Name	Description
4	Completion Timeout Disable Supported	Sets whether the completion timeout disable function is supported. This register can be written during initialization. 0b: Not Supported 1b: Supported
3 to 0	Completion Timeout Ranges Supported	Sets the completion timeout range. This register can be written during initialization. Range A: 50 µs to 10 ms Range B: 10 ms to 250 ms Range C: 250 ms to 4 s Range D: 4 s to 64 s The above 4 patterns are decided and the following combinations can be set. 0000b: Program setting. Not supported 0001b: Range A 0010b: Range B 0011b: Ranges A and B 0110b: Ranges B and C 0111b: Ranges A, B, and C 1110b: Ranges B, C and D 1111b: Ranges A, B, C, and D All other encodings are reserved. *Note*: Although the initial value described in the UM is 0010b, the initial value should be changed according to the installed system and device performance or indicate the initial value as a product request.

Table 36.4-107 Valid Reset Signal

Reset Signal	Emergency Power Reduction Initialization Required	Emergency Power Reduction Supported	OBFF Supported	10-Bit Tag Requester Supported	10-Bit Tag Completer Supported	LTR Mechanism Supported
RST_LOAD_B	✓	✓	✓	✓	✓	✓
RST_RSM_B						
RST_CFG_B						

Reset Signal	Completion Timeout Disable Supported	Completion Timeout Ranges Supported
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		

(17) Device Control 2/Status 2 Register (PCI_RC_DEVCS2)

This register controls the device and indicates the device status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6088h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	OBFF Enable		10-Bit Tag Requester Enable	Emergency Power Reduction	LTR Mechanism Enable	—	—	—	—	—	Completion Timeout Disable	Completion Timeout Value			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	R	R	R	R	R	RW	RW	RW	RW	RW

Table 36.4-108 PCI_RC_DEVCS2 Register Contents

Bit Position	Bit Name	Description
31 to 15	—	Reserved. These bits are read as 0b.
14, 13	OBFF Enable	00b (disabled) No changes allowed. *Note*: These bits are reserved when OBFF Supported = 00b.
12	10-Bit Tag Requester Enable	10-Bit Tag (Requester) enable 0b: Disable (initial value) 1b: Enable Fixed to 0b.
11	Emergency Power Reduction Request	Emergency Power Reduction Request Not supported. Fixed to 0b.
10	LTR Mechanism Enable	The LTR mechanism is enabled when this bit is set.
9 to 5	—	Reserved. These bits are read as 0b.
4	Completion Timeout Disable	The completion timeout disable function is enabled when this bit is set.
3 to 0	Completion Timeout Value	Sets the completion timeout range. 0000b: 10 ms to 50 ms (initial value) 0001b: 50 µs to 100 µs 0010b: 1 ms to 10 ms 0101b: 16 ms to 55 ms 0110b: 65 ms to 210 ms 1001b: 260 ms to 900 ms 1010b: 1 s to 3.5 s 1101b: 4 s to 13 s 1110b: 17 s to 64 s Others: Reserved (setting prohibited) *Note*: By the initial value 0000b, the time is set longer than the default lower limit of 50 usec in the Base Spec, but this takes into account the lower limit of 10 msec recommended by the Base Spec.

Table 36.4-109 Valid Reset Signal

Reset Signal	OBFF Enable	10-Bit Tag Requester Enable	LTR Mechanism Enable	Completion Timeout Disable	Completion Timeout Value
RST_LOAD_B					
RST_RSM_B					
RST_CFG_B	✓	✓	✓	✓	✓

(18) Link Capabilities 2 Register (PCI_RC_LINKC2)

This register indicates the link capabilities.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 608Ch

Initial Value: 0000_0006h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DRS Supported	—	—	—	—	—	—	Two Retimers Presence Detect Supported	Retimer Presence Detect Supported	Lower SKP OS Reception Supported Speeds Vector							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Lower SKP OS Generation Supported Speeds Vector							Crosslink Supported	Supported Link Speeds Vector[6:0]							—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	R

Table 36.4-110 PCI_RC_LINKC2 Register Contents

Bit Position	Bit Name	Description
31	DRS Supported	This function is not supported for this product. Fixed to 0b.
30 to 25	—	Reserved. These bits are read as 0b.
24	Two Retimers Presence Detect Supported	This function is not supported for this product. Fixed to 0b. This register can be written during initialization.
23	Retimer Presence Detect Supported	This function is not supported for this product. Fixed to 0b. This register can be written during initialization.
22 to 16	Lower SKP OS Reception Supported Speeds Vector	This function is not supported for this product. Fixed to 000_0000b. This register can be written during initialization.
15 to 9	Lower SKP OS Generation Supported Speeds Vector	This function is not supported for this product. Fixed to 0000_000b. This register can be written during initialization.
8	Crosslink supported	This function is not supported for this product. Fixed to 0b. This register can be written during initialization.
7 to 1	Supported Link Speeds Vector[6:0]	Indicates the supported link speed. This register can be written during initialization. Bit [0]: 2.5 GT/s Bit [1]: 5.0 GT/s Others: Reserved
0	—	Reserved. This bit is read as 0b.

Table 36.4-111 Valid Reset Signal

Reset Signal	Two Retimers Presence Detect Supported	Retimer Presence Detect Supported	Lower SKP OS Reception Supported Speeds Vector	Lower SKP OS Generation Supported Speeds Vector	Crosslink Supported	Supported Link Speeds Vector
RST_LOAD_B	✓	✓	✓	✓	✓	✓
RST_RSM_B						
RST_CFG_B						

(19) Link Control 2/Status 2 Register (PCI_RC_LINCS2)

This register controls the link and indicates the link status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6090h

Initial Value: 0000_0002h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DRS Message Received	Downstream Component Presence			—	—	Crosslink Resolution		Two Retimers Presence Detected	Retimer Presence Detected	Link Equalization Request	Equalization Phase 3 Successful	Equalization Phase 2 Successful	Equalization Phase 1 Successful	Equalization Complete	Current De-emphasis Level
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	RW1	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Compliance Preset/De-emphasis				Compliance SOS	Enter Modified Compliance	Transmit Margin			Selectable De-emphasis	Hardware Autonomous Speed Disable	Enter Compliance	Target Link Speed			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	HwInit	RW	RW	RW	RW	RW	RW

Table 36.4-112 PCI_RC_LINCS2 Register Contents (1/2)

Bit Position	Bit Name	Description
31	DRS Message Received	This function is not supported for this product. Fixed to 0b.
30 to 28	Downstream Component Presence	This function is not supported for this product. Fixed to 000b.
27, 26	—	Reserved. These bits are read as 0b.
25, 24	Crosslink Resolution	This function is not supported for this product. Fixed to 00b.
23	Two Retimers Presence Detect Supported	This function is not supported for this product. Fixed to 0b.
22	Retimer Presence Detect Supported	This function is not supported for this product. Fixed to 0b.
21	Link Equalization Request	This function is not supported for this product. Fixed to 0b.
20	Equalization Phase 3 Successful	This function is not supported for this product. Fixed to 0b.
19	Equalization Phase 2 Successful	This function is not supported for this product. Fixed to 0b.
18	Equalization Phase 1 Successful	This function is not supported for this product. Fixed to 0b.
17	Equalization Complete	This function is not supported for this product. Fixed to 0b.

Table 36.4-112 PCI_RC_LINCS2 Register Contents (2/2)

Bit Position	Bit Name	Description
16	Current De-emphasis Level	This is a status register indicating the de-emphasis level during Gen2 operation. 1b: −3.5 dB 0b: −6 dB (initial value) *Note*: The initial value after Gen2 linkup is 0b. However, 1b is indicated after Gen1 linkup, but this bit has no meaning in Gen1 and should be ignored.
15 to 12	Compliance Preset/De-emphasis	Sets the de-emphasis level during in the Polling.Compliance state. 0001b: −3.5 dB 0000b: −6 dB (initial value)
11	Compliance SOS	When this bit is set to 1b, the SKP ordered sets are inserted periodically during transmission of the compliance pattern.
10	Enter Modified Compliance	The configuration bit for transmission of the modified compliance pattern. 1b: Modified compliance pattern 0b: Compliance pattern (initial value)
9 to 7	Transmit Margin	Adjusts the voltage level. 000b: Normal operating range 001b to 111b: See the corresponding section of the Base Spec.
6	Selectable De-emphasis	The setting register for de-emphasis during RC Gen2 operation. This register can be written during initialization. 1b: −3.5 dB 0b: −6 dB
5	Hardware Autonomous Speed Disable	Controls a link speed change. 1b: Link speed change not supported (disabled) 0b: Link speed change supported (enabled)
4	Enter Compliance	Enables transition to compliance mode by setting 1b. The link speed at this time is the value set in the Target Link Speed field.
3 to 0	Target Link Speed	Sets the link speed value for indication to the other-party device during training. 0001b: 2.5 GT/s target link speed 0010b: 5.0 GT/s target link speed (initial value) 0011b: 8.0 GT/s target link speed (setting prohibited) 0100b: 16.0 GT/s target link speed (setting prohibited) All other encodings are reserved.

Table 36.4-113 Valid Reset Signal

Reset Signal	Link Equalization Request	Compliance Preset/De-emphasis	Compliance SOS	Enter Modified Compliance	Transmit Margin	Hardware Autonomous Speed Disable
RST_LOAD_B						
RST_RSM_B	✓	✓	✓	✓	✓	✓
RST_CFG_B						

Reset Signal	Enter Compliance	Target Link Speed
RST_LOAD_B		
RST_RSM_B	✓	✓
RST_CFG_B		

(20) Base Address Register Mask00 (Lower) (PCI_RC_BARMSK00L)

This register indicates mask information for Base Address Register 0 (BAR0).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60A0h

Initial Value: 0FFF_FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register Mask00 (Lower)															
Initial Value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register Mask00 (Lower)															
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-114 PCI_RC_BARMSK00L Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register Mask00 (Lower)	The mask register for Base Address Register 0 (BAR0). This register can be written during initialization. The initial value is decided by the configurable parameter.

Table 36.4-115 Valid Reset Signal

Reset Signal	Base Address Register Mask00 (Lower)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	

(21) Base Address Register Mask00 (Upper) (PCI_RC_BARMSK00U)

This register indicates mask information for Base Address Register 1 (BAR1).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60A4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register Mask00 (Upper)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register Mask00 (Upper)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-116 PCI_RC_BARMSK00U Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register Mask00 (Upper)	The mask register for Base Address Register 1 (BAR1). This register can be written during initialization. The initial value is decided by the configurable parameter.

Table 36.4-117 Valid Reset Signal

Reset Signal	Base Address Register Mask00 (Upper)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	

(22) Base Address Register Mask01 (Lower) (PCI_RC_BARMSK01L)

This register is not used.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60A8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register Mask01 (Lower)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register Mask01 (Lower)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-118 PCI_RC_BARMSK01L Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register Mask01 (Lower)	The mask register for Base Address Register 2 (BAR2). This register can be written during initialization. The initial value is decided by the configurable parameter.

Table 36.4-119 Valid Reset Signal

Reset Signal	Base Address Register Mask01 (Lower)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	

(23) Base Address Register Mask01 (Upper) (PCI_RC_BARMSK01U)

This register is not used.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60ACh

Initial Value: 0000_0000h

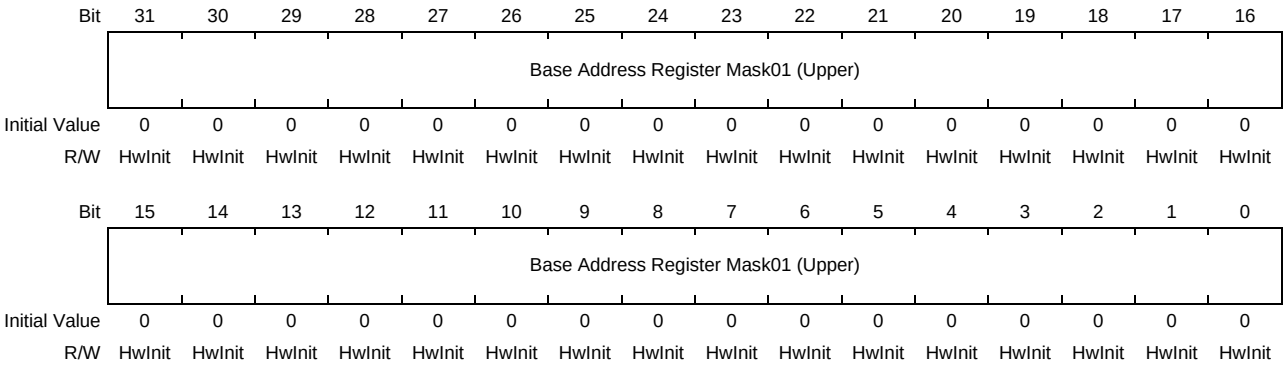


Table 36.4-120 PCI_RC_BARMSK01U Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register Mask01 (Upper)	The mask register for Base Address Register 3 (BAR3). This register can be written during initialization. The initial value is decided by the configurable parameter.

Table 36.4-121 Valid Reset Signal

Reset Signal	Base Address Register Mask01 (Upper)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	

(24) Base Address Register Mask02 (Lower) (PCI_RC_BARMSK02L)

This register is not used.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60B0h

Initial Value: 0000_1FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register Mask02 (Lower)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register Mask02 (Lower)															
Initial Value	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-122 PCI_RC_BARMSK02L Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register Mask02 (Lower)	The mask register for Base Address Register 4 (BAR4). This register can be written during initialization. The initial value is decided by the configurable parameter.

Table 36.4-123 Valid Reset Signal

Reset Signal	Base Address Register Mask02 (Lower)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	

(25) Base Address Register Mask02 (Upper) (PCI_RC_BARMSK02U)

This register is not used.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60B4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register Mask02 (Upper)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register Mask02 (Upper)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-124 PCI_RC_BARMSK02U Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register Mask02 (Upper)	The mask register for Base Address Register 5 (BAR5). This register can be written during initialization. The initial value is decided by the configurable parameter.

Table 36.4-125 Valid Reset Signal

Reset Signal	Base Address Register Mask01 (Upper)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	

(26) Base Size 00/01 Register (PCI_RC_BSIZE00_01)

This register sets the acceptable TLP size.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60C8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	Base Size 01									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Base Size 00									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-126 PCI_RC_BSIZE00_01 Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved. These bits are read as 0b.
25 to 16	Base Size 01	Fixed to 00_0000_0000b. Not used. This register can be written during initialization.
15 to 10	—	Reserved. These bits are read as 0b.
9 to 0	Base Size 00	Sets the size of the TLP (DW size) which can be accepted by Address Space 00 set by the Base Address Register and Base Address Mask Register. When a TLP with a packet length greater than the size set in these bits is received, even if it is smaller than the max payload size, a completer abort error (CA) is detected. Note that the initial value is 0_0000_0000b and this function is invalid in this case. This register can be written during initialization.

Table 36.4-127 Valid Reset Signal

Reset Signal	Base Size 01	Base Size 00
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		

(27) Base Size 02/03 Register (PCI_RC_BSIZE02_03)

This register is not used in root complex mode.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60CCh

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	Base Size 03									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Base Size 02									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-128 PCI_RC_BSIZE02_03 Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved. These bits are read as 0b.
25 to 16	Base Size 03	Fixed to 00_0000_0000b. Not used. This register can be written during initialization.
15 to 10	—	Reserved. These bits are read as 0b.
9 to 0	Base Size 02	Fixed to 00_0000_0000b. Not used. This register can be written during initialization.

Table 36.4-129 Valid Reset Signal

Reset Signal	Base Size 03	Base Size 02
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		

(28) Base Size 04/05 Register (PCI_RC_BSIZE04_05)

This register is not used in root complex mode.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60D0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	Base Size 05									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Base Size 04									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-130 PCI_RC_BSIZE04_05 Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved. These bits are read as 0b.
25 to 16	Base Size 05	Fixed to 00_0000_0000b. Not used. This register can be written during initialization.
15 to 10	—	Reserved. These bits are read as 0b.
9 to 0	Base Size 04	Fixed to 00_0000_0000b. Not used. This register can be written during initialization.

Table 36.4-131 Valid Reset Signal

Reset Signal	Base Size 05	Base Size 04
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		

(29) Base Size 06 Register (PCI_RC_BSIZE06)

This register is not used in root complex mode.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60D4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Base Size 06									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-132 PCI_RC_BSIZE06 Register Contents

Bit Position	Bit Name	Description
31 to 10	—	Reserved. These bits are read as 0b.
9 to 0	Base Size 06	Fixed to 00_0000_0000b. Not used. This register can be written during initialization.

Table 36.4-133 Valid Reset Signal

Reset Signal	Base Size 06
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	

(30) Type Supported 00/01/02 Register (PCI_RC_TSUPPORT00_01_02)

This register indicates the transaction type which can be supported by the memory space.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60D8h

Initial Value: 0033_3333h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Debug								Type Supported 02							
Initial Value	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1
R/W	R	R	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Type Supported 01								Type Supported 00[7:0]							
Initial Value	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-134 PCI_RC_TSUPPORT00_01_02 Register Contents

Bit Position	Bit Name	Description
31 to 24	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value (00h) may lead to a malfunction.
23 to 16	Type Supported 02	*Note*: Not used. This register can be written during initialization.
15 to 8	Type Supported 01	*Note*: Not used. This register can be written during initialization.
7 to 0	Type Supported 00[7:0]	Sets the transaction type which can be supported by space 00 (CFG_SPACE00_BASE). The meaning of each bit is indicated as follows. Bit 0: 32-bit memory read Bit 1: 64-bit memory read Bit 2: 32-bit memory read lock Bit 3: 64-bit memory read lock Bit 4: 32-bit memory write Bit 5: 64-bit memory write Bit 6: IO read Bit 7: IO write This register can be written during initialization.

Table 36.4-135 Valid Reset Signal

Reset Signal	Debug	Type Supported 02	Type Supported 01	Type Supported 00
RST_LOAD_B	✓	✓	✓	✓
RST_RSM_B				
RST_CFG_B				

(31) Advanced Error Reporting Capability Register (PCI_RC_ADVERC)

This register indicates the advanced error reporting capability.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6100h

Initial Value: 1501_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Next Capability Offset												Capability Version			
Initial Value	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	1
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCI Express Extended Capability ID															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-136 PCI_RC_ADVERC Register Contents

Bit Position	Bit Name	Description
31 to 20	Next Capability Offset	Indicates the start address of the device serial number capability. This register can be written during initialization.
19 to 16	Capability Version	Indicates the version number of the capability structure. Initial value: 0001b
15 to 0	PCI Express Extended Capability ID	Indicates the advanced error reporting capability. Initial value: 0001h

Table 36.4-137 Valid Reset Signal

Reset Signal	Next Capability Offset	Capability Version
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		

(32) Uncorrectable Error Status Register (PCI_RC_UNCESTS)

This register indicates the uncorrectable error status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6104h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	ACS Violation Status	Unsupported Request Error Status	ECRC Error Status	Malformed TLP Status	Receiver Overflow Status	Unexpected Completion Status
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW1	RW1	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Completer Abort Status	Completion Timeout Status	Flow Control Protocol Error Status	Poisoned TLP Received Status	—	—	—	—	—	—	Surprise Down Error Status	Data Link Protocol Error Status	—	—	—	Undefined
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	RW1	R	RW1	R	R	R	R	R	R	R	RW1	R	R	R	R

Table 36.4-138 PCI_RC_UNCESTS Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b.
21	ACS Violation Status	ACS is not supported. Fixed to 0b.
20	Unsupported Request Error Status	Indicates that an unsupported TLP was received. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
19	ECRC Error Status (Optional)	Indicates that an ECRC error was received. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
18	Malformed TLP Status	Indicates that a malformed TLP was received. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
17	Receiver Overflow Status (Optional)	Indicates that a TLP larger than the free credit in the receive buffer was received. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
16	Unexpected Completion Status	Indicates that a completion response was received but there is no record of transmission of the corresponding non-posted request (due to a mismatch with the transaction descriptor). It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
15	Completer Abort Status (Optional)	Indicates that the completion status returned a completion with Completer Abort (CA) status after the transmission of a non-posted request. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected

Table 36.4-138 PCI_RC_UNCESTS Register Contents (2/2)

Bit Position	Bit Name	Description
14	Completion Timeout Status	Indicates that the corresponding completion response was not received within the specified time after the transmission of a non-posted request. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
13	Flow Control Protocol Error Status (Optional)	Not implemented (fixed to 0b)
12	Poisoned TLP Received Status	Indicates that a poisoned TLP (which has a payload and the EP field of the header is 1b) was received. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
11 to 6	—	Reserved. These bits are read as 0b.
5	Surprise Down Error Status (Optional)	Not Implemented (fixed to 0b)
4	Data Link Protocol Error Status	Indicates that a sequence number error was detected in the data link layer. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
3 to 1	—	Reserved. These bits are read as 0b.
0	Undefined	Fixed to 0b.

Table 36.4-139 Valid Reset Signal

Reset Signal	Unsupported Request Error Status	ECRC Error Status	Malformed TLP Status	Receiver Overflow Status	Unexpected Completion Status	Completer Abort Status
RST_LOAD_B						
RST_RSM_B	✓	✓	✓	✓	✓	✓
RST_CFG_B						

Reset Signal	Completion Timeout Status	Poisoned TLP Received Status	Data Link Protocol Error Status
RST_LOAD_B			
RST_RSM_B	✓	✓	✓
RST_CFG_B			

(33) Uncorrectable Error Mask Register (PCI_RC_UNCEMASK)

This register masks the uncorrectable error status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6108h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	ACS Violation Mask	Unsupported Request Error Mask	ECRC Error Mask	Malformed TLP Mask	Receiver Overflow Mask	Unexpected Completion Mask
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Completer Abort Mask	Completion Timeout Mask	Flow Control Protocol Error Mask	Poisoned TLP Received Mask	—	—	—	—	—	—	Surprise Down Error Mask	Data Link Protocol Error Mask	—	—	—	Undefined
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	R	RW	R	R	R	R	R	R	R	RW	R	R	R	R

Table 36.4-140 PCI_RC_UNCEMASK Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b.
21	ACS Violation Mask	ACS is not supported. Fixed to 0b.
20	Unsupported Request Error Mask	Masks error notification to the root complex if an unsupported request error is detected. 0b: No masking 1b: Mask error message transmission, logging of the header in the Header Log register, and updating of the first error pointer.
19	ECRC Error Mask (Optional)	Masks error notification to the root complex if an ECRC error is detected. 0b: No masking 1b: Masking
18	Malformed TLP Mask	Masks error notification to the root complex if a malformed TLP error is detected. 0b: No masking 1b: Mask error message transmission, logging of the header in the Header Log register, and updating of the first error pointer.
17	Receiver Overflow Mask (Optional)	Masks error notification to the root complex if a receiver overflow error is detected. 0b: No masking 1b: Mask error message transmission and updating of the first error pointer.
16	Unexpected Completion Mask	Masks error notification to the root complex if an unexpected completion error is detected. 0b: No masking 1b: Mask error message transmission, logging of the header in the Header Log register, and updating of the first error pointer.
15	Completer Abort Mask (Optional)	Masks error notification to the root complex if a completer abort error is detected. 0b: No masking 1b: Mask error message transmission, logging of the header in the Header Log register, and updating of the first error pointer.
14	Completion Timeout Mask	Masks error notification to the root complex if a completion timeout error is detected. 0b: No masking 1b: Mask error message transmission and updating of the first error pointer.

Table 36.4-140 PCI_RC_UNCEMASK Register Contents (2/2)

Bit Position	Bit Name	Description
13	Flow Control Protocol Error Mask (Optional)	Not Implemented (fixed to 0b)
12	Poisoned TLP Received Mask	Masks error notification to the root complex if a poisoned TLP error is detected. 0b: No masking 1b: Mask error message transmission, logging of the header in the Header Log register, and updating of the first error pointer.
11 to 6	—	Reserved. These bits are read as 0b.
5	Surprise Down Error Mask (Optional)	Not Implemented (fixed to 0b)
4	Data Link Protocol Error Mask	Masks error notification to the root complex if a data link protocol error is detected. 0b: No masking 1b: Mask error message transmission and updating of the first error pointer.
3 to 1	—	Reserved. These bits are read as 0b.
0	Undefined	Fixed to 0b

Table 36.4-141 Valid Reset Signal

Reset Signal	Unsupported Request Error Mask	ECRC Error Mask	Malformed TLP Mask	Receiver Overflow Mask	Unexpected Completion Mask	Completer Abort Mask
RST_LOAD_B						
RST_RSM_B	✓	✓	✓	✓	✓	✓
RST_CFG_B						

Reset Signal	Completion Timeout Mask	Poisoned TLP Received Mask	Data Link Protocol Error Mask
RST_LOAD_B			
RST_RSM_B	✓	✓	✓
RST_CFG_B			

(34) Uncorrectable Error Severity Register (PCI_RC_UNCESVY)

This register sets the uncorrectable error severity.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 610Ch

Initial Value: 0046_2030h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	Debug	ACS Violation Severity	Unsupported Request Error Severity	ECRC Error Severity	Malformed TLP Severity	Receiver Overflow Severity	Unexpected Completion Severity
Initial Value	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0
R/W	R	R	R	R	R	R	R	R	R	HwInit	R	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Completer Abort Severity	Completion Timeout Severity	Flow Control Protocol Error Severity	Poisoned TLP Received Severity	—	—	—	—	—	—	Surprise Down Error Severity	Data Link Protocol Error Severity	—	—	—	Undefined
Initial Value	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0
R/W	RW	RW	R	RW	R	R	R	R	R	R	R	RW	R	R	R	R

Table 36.4-142 PCI_RC_UNCESVY Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b.
22	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction. This register can be written during initialization.
21	ACS Violation Severity	ACS is not supported. Fixed to 0b.
20	Unsupported Request Error Severity	Sets the severity of the error for detection of an unsupported request error. 0b: Non-fatal error 1b: Fatal error
19	ECRC Error Severity (Optional)	Sets the severity of the error for an ECRC error. 0b: Non-fatal error 1b: Fatal error
18	Malformed TLP Severity	Sets the severity of the error for a malformed TLP error. 0b: Non-fatal error 1b: Fatal error
17	Receiver Overflow Severity (Optional)	Sets the severity of the error for a receiver overflow error. 0b: Non-fatal error 1b: Fatal error
16	Unexpected Completion Severity	Sets the severity of the error for an unexpected completion error. 0b: Non-fatal error 1b: Fatal error
15	Completer Abort Severity (Optional)	Sets the severity of the error for a completer abort error. 0b: Non-fatal error 1b: Fatal error
14	Completion Timeout Severity	Sets the severity of the error for a completion timeout error. 0b: Non-fatal error 1b: Fatal error

Table 36.4-142 PCI_RC_UNCESVY Register Contents (2/2)

Bit Position	Bit Name	Description
13	Flow Control Protocol Error Severity (Optional)	Not Implemented (fixed to 0b)
12	Poisoned TLP Received Severity	Sets the severity of the error for a poisoned TLP error. 0b: Non-fatal error 1b: Fatal error
11 to 6	—	Reserved. These bits are read as 0b.
5	Surprise Down Error Severity (Optional)	Not Implemented (fixed to 0b)
4	Data Link Protocol Error Severity	Sets the severity of the error for a data link protocol error. 0b: Non-fatal error 1b: Fatal error
3 to 1	—	Reserved. These bits are read as 0b.
0	Undefined	Fixed to 0b.

Table 36.4-143 Valid Reset Signal

Reset Signal	Debug	Unsupported Request Error Severity	ECRC Error Severity	Malformed TLP Severity	Receiver Overflow Severity	Unexpected Completion Severity
RST_LOAD_B	✓					
RST_RSM_B		✓	✓	✓	✓	✓
RST_CFG_B						

Reset Signal	Completer Abort Severity	Completion Timeout Severity	Poisoned TLP Received Severity	Data Link Protocol Error Severity
RST_LOAD_B				
RST_RSM_B	✓	✓	✓	✓
RST_CFG_B				

(35) Correctable Error Status Register (PCI_RC_CESTS)

This register indicates the correctable error status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6110h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	Advisory Non-Fatal Error Status	Replay Timer Timeout Status	—	—	—	REPLAY_NUM Rollover Status	Bad DLLP Status	Bad TLP Status	—	—	—	—	—	Receiver Error Status
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW1	RW1	R	R	R	RW1	RW1	RW1	R	R	R	R	R	RW1

Table 36.4-144 PCI_RC_CESTS Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved. These bits are read as 0b.
13	Advisory Non-Fatal Error Status	Indicates that an advisory non-fatal error was detected. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
12	Replay Timer Timeout Status	Indicates that a timeout error has occurred when an Ack or Nak DLLP was not received within the specified time after the transmission of a TLP. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
11 to 9	—	Reserved. These bits are read as 0b.
8	REPLAY_NUM Rollover Status	Indicates that REPLAY_NUM has rolled over from 11b to 00b when replays occurred four times consecutively. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
7	Bad DLLP Status	Indicates that a CRC error of DLLP was detected. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
6	Bad TLP Status	Indicates that a CRC error or sequence number error was detected. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
5 to 1	—	Reserved. These bits are read as 0b.
0	Receiver Error Status (optional)	It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected

Table 36.4-145 Valid Reset Signal

Reset Signal	Advisory Non-Fatal Error Status	Replay Timer Timeout Status	REPLAY_NUM Rollover Status	Bad DLLP Status	Bad TLP Status	Receiver Error Status
RST_LOAD_B						
RST_RSM_B	✓	✓	✓	✓	✓	✓
RST_CFG_B						

(36) Correctable Error Mask Register (PCI_RC_CEMASK)

This register masks the correctable error status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6114h

Initial Value: 0000_2000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	Advisory Non-Fatal Error Mask	Replay Timer Timeout Mask	—	—	—	REPLAY_NUM Rollover Mask	Bad DLLP Mask	Bad TLP Mask	—	—	—	—	—	Receiver Error Mask
Initial Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW1	RW1	R	R	R	RW1	RW1	RW1	R	R	R	R	R	RW1

Table 36.4-146 PCI_RC_CEMASK Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved. These bits are read as 0b.
13	Advisory Non-Fatal Error Mask	Error notification is masked if an advisory non-fatal error is detected. 0b: No masking 1b: Masks advisory non-fatal error handling (masks updating of the first error pointer and logging of the header, and error message transmission).
12	Replay Timer Timeout Mask	Error notification is masked if a replay timer timeout error is detected. 0b: No masking 1b: Masks error message transmission.
11 to 9	—	Reserved. These bits are read as 0b.
8	REPLAY_NUM Rollover Mask	Error notification is masked if a REPLAY_NUM rollover error is detected. 0b: No masking 1b: Masks error message transmission.
7	Bad DLLP Mask	Error notification is masked if a bad DLLP error is detected. 0b: No masking 1b: Masks error message transmission.
6	Bad TLP Mask	Error notification is masked if a bad TLP error is detected. 0b: No masking 1b: Masks error message transmission.
5 to 1	—	Reserved. These bits are read as 0b.
0	Receiver Error Mask (optional)	0b: No masking 1b: Masks error message transmission.

Table 36.4-147 Valid Reset Signal

Reset Signal	Advisory Non-Fatal Error Mask	Replay Timer Timeout Mask	REPLAY_NUM Rollover Mask	Bad DLLP Mask	Bad TLP Mask	Receiver Error Mask
RST_LOAD_B						
RST_RSM_B	✓	✓	✓	✓	✓	✓
RST_CFG_B						

(37) Advanced Error Capabilities and Control Register (PCI_RC_ADVECC)

This register indicates and controls the advanced error capabilities.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6118h

Initial Value: 0000_00A0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ECRC Check Enable	ECRC Check Capable	ECRC Generation Enable	ECRC Generation Capable	First Error Pointer				
Initial Value	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	R	RW	R	R	R	R	R	R

Table 36.4-148 PCI_RC_ADVECC Register Contents

Bit Position	Bit Name	Description
31 to 9	—	Reserved. These bits are read as 0b.
8	ECRC Check Enable	Enables ECRC checking. 0b: Disable (initial value) 1b: Enable
7	ECRC Check Capable	Indicates whether ECRC checking is implemented. 0b: No ECRC checking 1b: ECRC checking is implemented (initial value).
6	ECRC Generation Enable	Enables ECRC generation. 0b: Disable (initial value) 1b: Enable
5	ECRC Generation Capable	Indicates whether ECRC generation is implemented. 0b: No ECRC generation 1b: ECRC generation is implemented (initial value).
4 to 0	First Error Pointer	Indicates the field value of the Uncorrectable Error Status register for the first uncorrectable error detection.

Note: The First Error Pointer bits [4:0] are reset by RST_GP_B.

Table 36.4-149 Valid Reset Signal

Reset Signal	ECRC Check Enable	ECRC Generation Enable
RST_LOAD_B		
RST_RSM_B	✓	✓
RST_CFG_B		

(38) Header Log Register 0 (PCI_RC_HLOG0)

This register indicates the header log.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 611Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Header of TLP associated with error 0															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Header of TLP associated with error 0															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-150 PCI_RC_HLOG0 Register Contents

Bit Position	Bit Name	Description
31 to 0	Header of TLP associated with error 0	Indicates the 1st DW of the header where the first uncorrectable error was detected.

(39) Header Log Register 1 (PCI_RC_HLOG1)

This register indicates the header log.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6120h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Header of TLP associated with error 1															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Header of TLP associated with error 1															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-151 PCI_RC_HLOG1 Register Contents

Bit Position	Bit Name	Description
31 to 0	Header of TLP associated with error 1	Indicates the 2nd DW of the header where the first uncorrectable error was detected.

(40) Header Log Register 2 (PCI_RC_HLOG2)

This register indicates the header log.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6124h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Header of TLP associated with error 2															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Header of TLP associated with error 2															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-152 PCI_RC_HLOG2 Register Contents

Bit Position	Bit Name	Description
31 to 0	Header of TLP associated with error 2	Indicates the 3rd DW of the header where the first uncorrectable error was detected.

(41) Header Log Register 3 (PCI_RC_HLOG3)

This register indicates the header log.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6128h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Header of TLP associated with error 3															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Header of TLP associated with error 3															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-153 PCI_RC_HLOG3 Register Contents

Bit Position	Bit Name	Description
31 to 0	Header of TLP associated with error 3	Indicates the 4th DW of the header where the first uncorrectable error was detected.

(42) Device Serial Number Extended Capability Register (PCI_RC_DEVSNEXTC)

This register specifies the device serial number extended capability.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6150h

Initial Value: 0001_0003h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Next Capability Offset												Capability Version			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCI Express Extended Capability ID															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.4-154 PCI_RC_DEVSNEXTC Register Contents

Bit Position	Bit Name	Description
31 to 20	Next Capability Offset	Indicates that this is the last item in the capability list. Fixed to 000h.
19 to 16	Capability Version	Indicates the version number of the capability structure. Initial value: 0001b. This register can be written during initialization.
15 to 0	PCI Express Extended Capability ID	Indicates the device serial number extended capability. Initial value: 0003h

Table 36.4-155 Valid Reset Signal

Reset Signal	Next Capability Offset	Capability Version
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		

(43) Serial Number Register (Lower DW) (PCI_RC_SNL)

This register specifies the serial number of the device.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6154h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PCI Express Device Serial Number (Lower DW)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCI Express Device Serial Number (Lower DW)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-156 PCI_RC_SNL Register Contents

Bit Position	Bit Name	Description
31 to 0	PCI Express Device Serial Number (Lower DW)	These are the lower-order 32 bits of a unique ID (EUI-64) of the IEEE specification. An EUI-64 consists of a 24-bit company ID and a 40-bit vendor-defined extension ID. This register can be written during initialization.

Table 36.4-157 Valid Reset Signal

Reset Signal	PCI Express Device Serial Number (Lower DW)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	

(44) Serial Number Register (Upper DW) (PCI_RC_SNU)

This register specifies the serial number of the device.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6158h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PCI Express Device Serial Number (Upper DW)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCI Express Device Serial Number (Upper DW)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit	HwInit

Table 36.4-158 PCI_RC_SNU Register Contents

Bit Position	Bit Name	Description
31 to 0	PCI Express Device Serial Number (Upper DW)	These are the higher-order 32 bits of a unique ID (EUI-64) of the IEEE specification. An EUI-64 consists of a 24-bit company ID and a 40-bit vendor-defined extension ID. This register can be written during initialization.

Table 36.4-159 Valid Reset Signal

Reset Signal	PCI Express Device Serial Number (Upper DW)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	

36.5 Register Descriptions (Endpoint Mode)

The following lists the registers incorporated in the unit.

For the register base address (<PCI_S0_REG_base>), see the section of Address Map.

CAUTION

The results of access to reserved bit areas, debug bit areas, and undefined areas are not guaranteed. The combination of reserved, debug, and undefined areas includes cases where the initial values will be non-zero, and the results of changes to such values are not guaranteed.

The following is the outline of categories of the register space within this unit.

AXI Bridge Registers	<PCI_S0_REG_base> + 0000h-1FFCh
Reserved	<PCI_S0_REG_base> + 2000h-5FFCh
PCI Express Configuration Registers (Type0)	<PCI_S0_REG_base> + 6000h-6FFCh (Function #0)
PCI Express Configuration Registers (Type0)	<PCI_S0_REG_base> + 7000h-7FFCh (Function #1)

Access to the reserved spaces above is prohibited.

36.5.1 List of AXI Bridge Registers

Unless specifically stated otherwise, byte, word, and double word access are all possible.

Access to registers is possible from the AXI-bus side and the PCIe-bus side. Attributes may vary with the register and the direction of access. In the case of registers for which attributes vary, attributes in the upper parts of the cells in the R/W column are for access from the PCIe-bus side and those in the lower parts are for access from the AXI-bus side. However, the cells are not divided into upper and lower parts in cases where access does not vary with the side proceeding with access.

Table 36.5-1 AXI Bridge Registers (1/6)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
Reserved 00h to 7Ch				
00 to 7Ch	Reserved	—	—	—
Request Issuing 80h to FCh				
80h	Request Data Register 0	PCI_EP_REQDATA0	xxxx_xxxxh	32
84h	Request Data Register 1	PCI_EP_REQDATA1	xxxx_xxxxh	32
88h	Request Data Register 2	PCI_EP_REQDATA2	xxxx_xxxxh	32
8Ch	Request Receive Data Register	PCI_EP_REQRCVDAT	xxxx_xxxxh	32
90h	Request Address Register 1	PCI_EP_REQADR1	xxxx_xxxxh	32
94h	Request Address Register 2	PCI_EP_REQADR2	xxxx_xxxxh	32
98h	Request Byte Enable Register	PCI_EP_REQBE	0000_000Fh	32
9Ch	Request Issue Register	PCI_EP_REQISS	0000_0000h	32
A0 to FCh	Reserved	—	—	—
PCI Interruption 100h to 11Ch				
100h to 114h	Reserved	—	—	—
118h	PCI INTx Out Status Register	PCI_EP_INTXOUTS	0000_0000h	32
11Ch	Reserved	—	—	—
Message Interruption 120h to 13Ch				
120h	Message Receive Interrupt Enable Register	PCI_EP_MSGRCVIE	0000_0000h	32
124h	Message Receive Interrupt Status Register	PCI_EP_MSGRCVIS	0000_0000h	32
128h to 12Ch	Reserved	—	—	—
130h	Message Code Register	PCI_EP_MSGCODE	0000_0000h	32
134h	Message Data Register	PCI_EP_MSGDATA	0000_0000h	32
138h	Message Header 3rdDW Register	PCI_EP_MSGH3DW	0000_0000h	32
13Ch	Message Header 4thDW Register	PCI_EP_MSGH4DW	0000_0000h	32
Interrupt Table 140h to 1FCh				
140h	Interrupt Table Register	PCI_EP_INTTABLE	00xx _0000h	32
144h to 1FCh	Reserved	—	—	—
Error Event 200h to 2FCh				
200h	PCIe Event Interrupt Enable 0 Register	PCI_EP_PEIE0	0000_0000h	32
204h	PCIe Event Interrupt Status 0 Register	PCI_EP_PEIS0	0000_0000h	32
208h	PCIe Event Interrupt Enable 1 Register	PCI_EP_PEIE1	0000_0000h	32
20Ch	PCIe Event Interrupt Status 1 Register	PCI_EP_PEIS1	0000_0000h	32
210h	AXI Master Error Interrupt Enable Register	PCI_EP_AMEIE	0000_0000h	32
214h	AXI Master Error Interrupt Status Register	PCI_EP_AMEIS	0000_0000h	32
218h to 21Ch	Reserved	—	—	—

Table 36.5-1 AXI Bridge Registers (2/6)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
220h	AXI Slave Error Interrupt Enable 1 Register	PCI_EP_ASEIE1	0000_0000h	32
224h	AXI Slave Error Interrupt Status 1 Register	PCI_EP_ASEIS1	0000_0000h	32
228h to 22Ch	Debug	—	—	—
230h	AXI Slave Error Interrupt Status 3 Register	PCI_EP_ASEIS3	0000_0000h	32
234h	Debug	—	—	—
238h to 23Ch	Reserved	—	—	—
240h	PCIe Event Interrupt Enable 2 Register	PCI_EP_PEIE2	0000_0000h	32
244h	PCIe Event Interrupt Status 2 Register	PCI_EP_PEIS2	0000_0000h	32
248h to 2FCh	Reserved	—	—	—
Unit Control 300h to 3FCh				
300h	Permission Register	PCI_EP_PERM	0000_0000h	32
304h to 30Ch	Reserved	—	—	—
310h	Reset Register	PCI_EP_RESET	0000_00xxh	32
314h	Mode Set 0 Register	PCI_EP_MSET0	2001_2000h	32
318h	Mode Set 1 Register	PCI_EP_MSET1	0000_33F2h	32
31Ch to 37Ch	Debug	—	—	—
380h	Mode Set 3 Register	PCI_EP_MSET3	0000_0000h	32
384h	Debug Output 1 Register	PCI_EP_DBGOUT1	0000_0000h	32
388h	Debug Output 2 Register	PCI_EP_DBGOUT2	0000_0000h	32
390h	Debug Input 0 Register	PCI_EP_DBGIN0	xxxx_xxxxh	32
394h to 3FCh	Reserved	—	—	—
400h	PCIe Core Mode Set 1 Register	PCI_EP_PCMSET1	07D0_00F2h	32
404h	PCIe Core Control 1 Register	PCI_EP_PCCTRL1	0000_0000h	32
408h	PCIe Core Status 1 Register	PCI_EP_PCSTAT1	0x0x_xxxxh	32
40Ch	Debug	—	—	—
410h	PCIe Core Control 2 Register	PCI_EP_PCCTRL2	003E_0000h	32
414h	PCIe Core Status 2 Register	PCI_EP_PCSTAT2	xxxx_xxxxh	32
418h to 428h	Debug	—	—	—
42Ch	PCIe Core Status 5 Register	PCI_EP_PCSTAT5	0000_0x00h	32
430h to 43Ch	Reserved	—	—	—
440h to 458h	Debug	—	—	—
45Ch to 46Ch	Reserved	—	—	—
470h	Debug	—	—	—
474h to 47Ch	Reserved	—	—	—
480h	Debug	—	—	—
484h to 4CCh	Reserved	—	—	—
4D0h	DMA Interrupt Vector 0 Register	PCI_EP_DMAINTVEC0	0000_0000h	32
4D4h	DMA Interrupt Vector 1 Register	PCI_EP_DMAINTVEC1	0000_0000h	32
4D8h to 6FCh	Reserved	—	—	—
700h to 7FCh	Debug	—	—	—
DMAC Registers 800h to FFCh				
Common Control 800h to 8FCh				
800h	DMA Control Register	PCI_EP_DMACTRL	0000_0000h	32
804h	Reserved	—	—	—
808h	DMA Interrupt Enable Register	PCI_EP_DMAINTE	0000_0000h	32

Table 36.5-1 AXI Bridge Registers (3/6)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
80Ch	DMA Interrupt Status Register	PCI_EP_DMAINTS	0000_0000h	32
810h to 8FCh	Reserved	—	—	—
Channel Control 900h to 91Ch*1				
900h	DMA Channel Control Register 0	PCI_EP_DMACHCTL0	0000_0000h	32
904h	Reserved	—	—	—
908h	QUE Entry (Lower) Register 0	PCI_EP_QUEE0L	0000_0000h	32
90Ch	QUE Entry (Upper) Register 0	PCI_EP_QUEE0U	0000_0000h	32
910h~91Ch	Reserved	—	—	—
DMA Setting 920h to 94Ch*1				
920h	DMA Descriptor Control (Descriptor 00h) Register 0	PCI_EP_DMADPCTL0	0000_0000h	32
924h	DMA Source Address (Descriptor 04h) Register 0	PCI_EP_DMASRCA0	0000_0000h	32
928h	DMA Destination Address (Descriptor 08h) Register 0	PCI_EP_DMADSTA0	0000_0000h	32
92Ch	DMA Size (Descriptor 0Ch) Register 0	PCI_EP_DMASIZE0	0000_0000h	32
930h	DMA PCIe Upper Address (Descriptor 10h) Register 0	PCI_EP_DMAPCIEUA0	0000_0000h	32
934h	DMA Transaction Control (Descriptor 14h) Register 0	PCI_EP_DMATCTL0	0000_0000h	32
938h	Reserved	—	—	—
93Ch	DMA Descriptor Link Pointer (Descriptor 1Ch) Register 0	PCI_EP_DMADPLP0	0000_0000h	32
940h to 94Ch	Reserved	—	—	—
DMA Status 950h to 99Ch*1				
950h	DMA Rest Size Register 0	PCI_EP_DMARESTSIZ0	0000_0000h	32
954h	AXI Request Address Register 0	PCI_EP_AREQA0	0000_0000h	32
958h	PCIe Request Address (Lower) Register 0	PCI_EP_PREQA0L	0000_0000h	32
95Ch	PCIe Request Address (Upper) Register 0	PCI_EP_PREQA0U	0000_0000h	32
960h	QUE Status Register 0	PCI_EP_QUESTA0	0000_0000h	32
964h	Reserved	—	—	—
968h	DMAC Error Status Register 0	PCI_EP_DMACESTA0	0000_0000h	32
96Ch to 99Ch	Reserved	—	—	—
PCI Express to AXI Access 1000h to 10FCh (Function #0)				
1000h	AXI Window Base 0 Register (Function #0)	PCI_EP_AWBASE0_F0	0000_0000h	32
1004h	AXI Window Mask 0 Register (Function #0)	PCI_EP_AWMASK0_F0	0000_0FFFh	32
1008h	AXI Destination 0 Register (Function #0)	PCI_EP_ADEST0_F0	0000_0000h	32
100Ch	Reserved	—	—	—
1010h	AXI Window Base 1 Register (Function #0)	PCI_EP_AWBASE1_F0	0000_0000h	32
1014h	AXI Window Mask 1 Register (Function #0)	PCI_EP_AWMASK1_F0	0000_0FFFh	32
1018h	AXI Destination 1 Register (Function #0)	PCI_EP_ADEST1_F0	0000_0000h	32
101Ch	Reserved	—	—	—
1020h	AXI Window Base 2 Register (Function #0)	PCI_EP_AWBASE2_F0	0000_0000h	32
1024h	AXI Window Mask 2 Register (Function #0)	PCI_EP_AWMASK2_F0	0000_0FFFh	32
1028h	AXI Destination 2 Register (Function #0)	PCI_EP_ADEST2_F0	0000_0000h	32
102Ch	Reserved	—	—	—
1030h	AXI Window Base 3 Register (Function #0)	PCI_EP_AWBASE3_F0	0000_0000h	32
1034h	AXI Window Mask 3 Register (Function #0)	PCI_EP_AWMASK3_F0	0000_0FFFh	32
1038h	AXI Destination 3 Register (Function #0)	PCI_EP_ADEST3_F0	0000_0000h	32
103Ch	Reserved	—	—	—

Table 36.5-1 AXI Bridge Registers (4/6)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
1040h	AXI Window Base 4 Register (Function #0)	PCI_EP_AWBASE4_F0	0000_0000h	32
1044h	AXI Window Mask 4 Register (Function #0)	PCI_EP_AWMASK4_F0	0000_0FFFh	32
1048h	AXI Destination 4 Register (Function #0)	PCI_EP_ADEST4_F0	0000_0000h	32
104Ch	Reserved	—	—	—
1050h	AXI Window Base 5 Register (Function #0)	PCI_EP_AWBASE5_F0	0000_0000h	32
1054h	AXI Window Mask 5 Register (Function #0)	PCI_EP_AWMASK5_F0	0000_0FFFh	32
1058h	AXI Destination 5 Register (Function #0)	PCI_EP_ADEST5_F0	0000_0000h	32
105Ch	Reserved	—	—	—
1060h	AXI Window Base 6 Register (Function #0)	PCI_EP_AWBASE6_F0	0000_0000h	32
1064h	AXI Window Mask 6 Register (Function #0)	PCI_EP_AWMASK6_F0	0000_0FFFh	32
1068h	AXI Destination 6 Register (Function #0)	PCI_EP_ADEST6_F0	0000_0000h	32
106Ch	Reserved	—	—	—
1070h	AXI Window Base 7 Register (Function #0)	PCI_EP_AWBASE7_F0	0000_0000h	32
1074h	AXI Window Mask 7 Register (Function #0)	PCI_EP_AWMASK7_F0	0000_0FFFh	32
1078h	AXI Destination 7 Register (Function #0)	PCI_EP_ADEST7_F0	0000_0000h	32
107Ch to 10FCh	Reserved	—	—	—
AXI to PCI Express Access 1100h to 11FCh (Function #0)				
1100h	PCIe Window Base 0 Register (Function #0)	PCI_EP_PWBASE0_F0	0000_0000h	32
1104h	PCIe Window Mask 0 Register (Function #0)	PCI_EP_PWMASK0_F0	0000_0FFFh	32
1108h	PCIe Destination 0 (Lower) Register (Function #0)	PCI_EP_PDESTLO0_F0	0000_0000h	32
110Ch	PCIe Destination 0 (Upper) Register (Function #0)	PCI_EP_PDESTUP0_F0	0000_0000h	32
1110h	PCIe Window Base 1 Register (Function #0)	PCI_EP_PWBASE1_F0	0000_0000h	32
1114h	PCIe Window Mask 1 Register (Function #0)	PCI_EP_PWMASK1_F0	0000_0FFFh	32
1118h	PCIe Destination 1 (Lower) Register (Function #0)	PCI_EP_PDESTLO1_F0	0000_0000h	32
111Ch	PCIe Destination 1 (Upper) Register (Function #0)	PCI_EP_PDESTUP1_F0	0000_0000h	32
1120h	PCIe Window Base 2 Register (Function #0)	PCI_EP_PWBASE2_F0	0000_0000h	32
1124h	PCIe Window Mask 2 Register (Function #0)	PCI_EP_PWMASK2_F0	0000_0FFFh	32
1128h	PCIe Destination 2 (Lower) Register (Function #0)	PCI_EP_PDESTLO2_F0	0000_0000h	32
112Ch	PCIe Destination 2 (Upper) Register (Function #0)	PCI_EP_PDESTUP2_F0	0000_0000h	32
1130h	PCIe Window Base 3 Register (Function #0)	PCI_EP_PWBASE3_F0	0000_0000h	32
1134h	PCIe Window Mask 3 Register (Function #0)	PCI_EP_PWMASK3_F0	0000_0FFFh	32
1138h	PCIe Destination 3 (Lower) Register (Function #0)	PCI_EP_PDESTLO3_F0	0000_0000h	32
113Ch	PCIe Destination 3 (Upper) Register (Function #0)	PCI_EP_PDESTUP3_F0	0000_0000h	32
1140h	PCIe Window Base 4 Register (Function #0)	PCI_EP_PWBASE4_F0	0000_0000h	32
1144h	PCIe Window Mask 4 Register (Function #0)	PCI_EP_PWMASK4_F0	0000_0FFFh	32
1148h	PCIe Destination 4 (Lower) Register (Function #0)	PCI_EP_PDESTLO4_F0	0000_0000h	32
114Ch	PCIe Destination 4 (Upper) Register (Function #0)	PCI_EP_PDESTUP4_F0	0000_0000h	32
1150h	PCIe Window Base 5 Register (Function #0)	PCI_EP_PWBASE5_F0	0000_0000h	32
1154h	PCIe Window Mask 5 Register (Function #0)	PCI_EP_PWMASK5_F0	0000_0FFFh	32
1158h	PCIe Destination 5 (Lower) Register (Function #0)	PCI_EP_PDESTLO5_F0	0000_0000h	32
115Ch	PCIe Destination 5 (Upper) Register (Function #0)	PCI_EP_PDESTUP5_F0	0000_0000h	32
1160h	PCIe Window Base 6 Register (Function #0)	PCI_EP_PWBASE6_F0	0000_0000h	32
1164h	PCIe Window Mask 6 Register (Function #0)	PCI_EP_PWMASK6_F0	0000_0FFFh	32
1168h	PCIe Destination 6 (Lower) Register (Function #0)	PCI_EP_PDESTLO6_F0	0000_0000h	32
116Ch	PCIe Destination 6 (Upper) Register (Function #0)	PCI_EP_PDESTUP6_F0	0000_0000h	32

Table 36.5-1 AXI Bridge Registers (5/6)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
1170h	PCIe Window Base 7 Register (Function #0)	PCI_EP_PWBASE7_F0	0000_0000h	32
1174h	PCIe Window Mask 7 Register (Function #0)	PCI_EP_PWMASK7_F0	0000_0FFFh	32
1178h	PCIe Destination 7 (Lower) Register (Function #0)	PCI_EP_PDESTLO7_F0	0000_0000h	32
117Ch	PCIe Destination 7 (Upper) Register (Function #0)	PCI_EP_PDESTUP7_F0	0000_0000h	32
1180h to 11FCh	Reserved	—	—	—
PCI Express to AXI Access 1200h to 12FCh (Function #1)*2				
1200h	AXI Window Base 0 Register (Function #1)	PCI_EP_AWBASE0_F1	0000_0000h	32
1204h	AXI Window Mask 0 Register (Function #1)	PCI_EP_AWMASK0_F1	0000_0FFFh	32
1208h	AXI Destination 0 Register (Function #1)	PCI_EP_ADEST0_F1	0000_0000h	32
120Ch	Reserved	—	—	—
1210h	AXI Window Base 1 Register (Function #1)	PCI_EP_AWBASE1_F1	0000_0000h	32
1214h	AXI Window Mask 1 Register (Function #1)	PCI_EP_AWMASK1_F1	0000_0FFFh	32
1218h	AXI Destination 1 Register (Function #1)	PCI_EP_ADEST1_F1	0000_0000h	32
121Ch	Reserved	—	—	—
1220h	AXI Window Base 2 Register (Function #1)	PCI_EP_AWBASE2_F1	0000_0000h	32
1224h	AXI Window Mask 2 Register (Function #1)	PCI_EP_AWMASK2_F1	0000_0FFFh	32
1228h	AXI Destination 2 Register (Function #1)	PCI_EP_ADEST2_F1	0000_0000h	32
122Ch	Reserved	—	—	—
1230h	AXI Window Base 3 Register (Function #1)	PCI_EP_AWBASE3_F1	0000_0000h	32
1234h	AXI Window Mask 3 Register (Function #1)	PCI_EP_AWMASK3_F1	0000_0FFFh	32
1238h	AXI Destination 3 Register (Function #1)	PCI_EP_ADEST3_F1	0000_0000h	32
123Ch	Reserved	—	—	—
1240h	AXI Window Base 4 Register (Function #1)	PCI_EP_AWBASE4_F1	0000_0000h	32
1244h	AXI Window Mask 4 Register (Function #1)	PCI_EP_AWMASK4_F1	0000_0FFFh	32
1248h	AXI Destination 4 Register (Function #1)	PCI_EP_ADEST4_F1	0000_0000h	32
124Ch	Reserved	—	—	—
1250h	AXI Window Base 5 Register (Function #1)	PCI_EP_AWBASE5_F1	0000_0000h	32
1254h	AXI Window Mask 5 Register (Function #1)	PCI_EP_AWMASK5_F1	0000_0FFFh	32
1258h	AXI Destination 5 Register (Function #1)	PCI_EP_ADEST5_F1	0000_0000h	32
125Ch	Reserved	—	—	—
1260h	AXI Window Base 6 Register (Function #1)	PCI_EP_AWBASE6_F1	0000_0000h	32
1264h	AXI Window Mask 6 Register (Function #1)	PCI_EP_AWMASK6_F1	0000_0FFFh	32
1268h	AXI Destination 6 Register (Function #1)	PCI_EP_ADEST6_F1	0000_0000h	32
126Ch	Reserved	—	—	—
1270h	AXI Window Base 7 Register (Function #1)	PCI_EP_AWBASE7_F1	0000_0000h	32
1274h	AXI Window Mask 7 Register (Function #1)	PCI_EP_AWMASK7_F1	0000_0FFFh	32
1278h	AXI Destination 7 Register (Function #1)	PCI_EP_ADEST7_F1	0000_0000h	32
127Ch to 12FCh	Reserved	—	—	—
AXI to PCI Express Access 1300h to 13FCh (Function #1)*2				
1300h	PCIe Window Base 0 Register (Function #1)	PCI_EP_PWBASE0_F1	0000_0000h	32
1304h	PCIe Window Mask 0 Register (Function #1)	PCI_EP_PWMASK0_F1	0000_0FFFh	32
1308h	PCIe Destination 0 (Lower) Register (Function #1)	PCI_EP_PDESTLO0_F1	0000_0000h	32
130Ch	PCIe Destination 0 (Upper) Register (Function #1)	PCI_EP_PDESTUP0_F1	0000_0000h	32
1310h	PCIe Window Base 1 Register (Function #1)	PCI_EP_PWBASE1_F1	0000_0000h	32
1314h	PCIe Window Mask 1 Register (Function #1)	PCI_EP_PWMASK1_F1	0000_0FFFh	32

Table 36.5-1 AXI Bridge Registers (6/6)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
1318h	PCIe Destination 1 (Lower) Register (Function #1)	PCI_EP_PDESTLO1_F1	0000_0000h	32
131Ch	PCIe Destination 1 (Upper) Register (Function #1)	PCI_EP_PDESTUP1_F1	0000_0000h	32
1320h	PCIe Window Base 2 Register (Function #1)	PCI_EP_PWBASE2_F1	0000_0000h	32
1324h	PCIe Window Mask 2 Register (Function #1)	PCI_EP_PWMASK2_F1	0000_0FFFh	32
1328h	PCIe Destination 2 (Lower) Register (Function #1)	PCI_EP_PDESTLO2_F1	0000_0000h	32
132Ch	PCIe Destination 2 (Upper) Register (Function #1)	PCI_EP_PDESTUP2_F1	0000_0000h	32
1330h	PCIe Window Base 3 Register (Function #1)	PCI_EP_PWBASE3_F1	0000_0000h	32
1334h	PCIe Window Mask 3 Register (Function #1)	PCI_EP_PWMASK3_F1	0000_0FFFh	32
1338h	PCIe Destination 3 (Lower) Register (Function #1)	PCI_EP_PDESTLO3_F1	0000_0000h	32
133Ch	PCIe Destination 3 (Upper) Register (Function #1)	PCI_EP_PDESTUP3_F1	0000_0000h	32
1340h	PCIe Window Base 4 Register (Function #1)	PCI_EP_PWBASE4_F1	0000_0000h	32
1344h	PCIe Window Mask 4 Register (Function #1)	PCI_EP_PWMASK4_F1	0000_0FFFh	32
1348h	PCIe Destination 4 (Lower) Register (Function #1)	PCI_EP_PDESTLO4_F1	0000_0000h	32
134Ch	PCIe Destination 4 (Upper) Register (Function #1)	PCI_EP_PDESTUP4_F1	0000_0000h	32
1350h	PCIe Window Base 5 Register (Function #1)	PCI_EP_PWBASE5_F1	0000_0000h	32
1354h	PCIe Window Mask 5 Register (Function #1)	PCI_EP_PWMASK5_F1	0000_0FFFh	32
1358h	PCIe Destination 5 (Lower) Register (Function #1)	PCI_EP_PDESTLO5_F1	0000_0000h	32
135Ch	PCIe Destination 5 (Upper) Register (Function #1)	PCI_EP_PDESTUP5_F1	0000_0000h	32
1360h	PCIe Window Base 6 Register (Function #1)	PCI_EP_PWBASE6_F1	0000_0000h	32
1364h	PCIe Window Mask 6 Register (Function #1)	PCI_EP_PWMASK6_F1	0000_0FFFh	32
1368h	PCIe Destination 6 (Lower) Register (Function #1)	PCI_EP_PDESTLO6_F1	0000_0000h	32
136Ch	PCIe Destination 6 (Upper) Register (Function #1)	PCI_EP_PDESTUP6_F1	0000_0000h	32
1370h	PCIe Window Base 7 Register (Function #1)	PCI_EP_PWBASE7_F1	0000_0000h	32
1374h	PCIe Window Mask 7 Register (Function #1)	PCI_EP_PWMASK7_F1	0000_0FFFh	32
1378h	PCIe Destination 7 (Lower) Register (Function #1)	PCI_EP_PDESTLO7_F1	0000_0000h	32
137Ch	PCIe Destination 7 (Upper) Register (Function #1)	PCI_EP_PDESTUP7_F1	0000_0000h	32
1380h to 1FFCh	Reserved	—	—	—

Note: Debug: Registers for use in debugging by Renesas. Access to these registers may lead to a malfunction.
Reserved: Reserved registers. The results of access to these registers and operation of the core through such access are not guaranteed.

Note 1. The addresses listed in the above table are those for channel 0. These addresses should be read as the addresses for the other DMAC channels according to the table below.

Channel Offset Address	
offset + 000h	Channel 0
offset + 080h	Channel 1
offset + 100h	Channel 2
offset + 180h	Channel 3
offset + 200h	Channel 4
offset + 280h	Channel 5
offset + 300h	Channel 6
offset + 380h	Channel 7

Example)

Channel 0: DMA Descriptor Control Register (offset: 920h = 920h + 000h)
Channel 1: DMA Descriptor Control Register (offset: 9A0h = 920h + 080h)
Channel 2: DMA Descriptor Control Register (offset: A20h = 920h + 100h)

Channel 3: DMA Descriptor Control Register (offset: AA0h = 920h + 180h)
Channel 4: DMA Descriptor Control Register (offset: B20h = 920h + 200h)
Channel 5: DMA Descriptor Control Register (offset: BA0h = 920h + 280h)
Channel 6: DMA Descriptor Control Register (offset: C20h = 920h + 300h)
Channel 7: DMA Descriptor Control Register (offset: CA0h = 920h + 380h)

Note 2. The register functions for function 1 is the same as those for function 0, so refer to the functions for function 0 for details of the register functions.

36.5.2 List of PCI Express Configuration Registers

36.5.2.1 Type 0 (for Endpoint)

Table 36.5-2 lists the PCI Express configuration registers (Type 0).

Table 36.5-2 PCI Express Configuration Registers (Type0) (1/5)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
Common Configuration Space				
6000h	Vendor and Device ID (Function #0)*1	PCI_EP_VID_F0	Configurable value	32
6004h	Command and Status (Function #0)	PCI_EP_COM_STA_F0	0010_0000h	32
6008h	Revision ID and Class Code (Function #0)*1	PCI_EP_RID_CC_F0	Configurable value	32
600Ch	Cache Line and Header Type (Function #0)	PCI_EP_CL_HT_F0	0080_0000h	32
Configuration Space				
6010h	Base Address Register 0 (Function #0)	PCI_EP_BAR0_F0	0000_0004h	32
6014h	Base Address Register 1 (Function #0)	PCI_EP_BAR1_F0	0000_0000h	32
6018h	Base Address Register 2 (Function #0)	PCI_EP_BAR2_F0	0000_0004h	32
601Ch	Base Address Register 3 (Function #0)	PCI_EP_BAR3_F0	0000_0000h	32
6020h	Base Address Register 4 (Function #0)	PCI_EP_BAR4_F0	0000_0004h	32
6024h	Base Address Register 5 (Function #0)	PCI_EP_BAR5_F0	0000_0000h	32
6028h	Reserved	—	—	—
602Ch	Subsystem ID (Function #0)*1	PCI_EP_SSID_F0	Configurable value	32
6030h	Reserved	—	—	—
6034h	Capabilities Pointer (Function #0)	PCI_EP_CP_F0	0000_0040h	32
6038h	Reserved	—	—	—
603Ch	Interrupt (Function #0)	PCI_EP_INT_F0	0000_0100h	32
PCI Power Management Capability Structure				
6040h	PM Capabilities (Function #0)	PCI_EP_PMC_F0	4803_E001h	32
6044h	PM Status/Control (Function #0)	PCI_EP_PMSC_F0	0000_0008h	32
6048h to 605Ch	Reserved	—	—	—
PCI Express Capability Structure				
6060h	PCI Express Capability (Function #0)	PCI_EP_PCIEC_F0	0002_0010h	32
6064h	Device Capabilities (Function #0)	PCI_EP_DEVC_F0	1000_8FC0h	32
6068h	Device Control/Status (Function #0)	PCI_EP_DEVCS_F0	0000_2010h	32
606Ch	Link Capabilities (Function #0)	PCI_EP_LINKC_F0	0043_6C22h	32
6070h	Link Control/Status (Function #0)	PCI_EP_LINKCS_F0	1000_0000h	32
6074h	Reserved	—	—	—
6078h	Reserved	—	—	—
607Ch	Reserved	—	—	—
6080h	Reserved	—	—	—
6084h	Device Capabilities 2 (Function #0)	PCI_EP_DEVC2_F0	0000_0012h	32
6088h	Device Control 2/Status 2 (Function #0)	PCI_EP_DEVCS2_F0	0000_0000h	32
608Ch	Link Capabilities 2 (Function #0)	PCI_EP_LINKC2_F0	0000_0006h	32
6090h	Link Control 2/Status 2 (Function #0)	PCI_EP_LINCS2_F0	0000_0002h	32

Table 36.5-2 PCI Express Configuration Registers (Type0) (2/5)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
6094h	Reserved	—	—	—
6098h	Reserved	—	—	—
609Ch	Reserved	—	—	—
Specific Registers				
60A0h	Base Address Register Mask00 (Lower) (Function #0)	PCI_EP_BARMSK00L_F0	0FFF_FFFFh	32
60A4h	Base Address Register Mask00 (Upper) (Function #0)	PCI_EP_BARMSK00U_F0	0000_0000h	32
60A8h	Base Address Register Mask01 (Lower) (Function #0)	PCI_EP_BARMSK01L_F0	0000_0000h	32
60ACh	Base Address Register Mask01 (Upper) (Function #0)	PCI_EP_BARMSK01U_F0	0000_0000h	32
60B0h	Base Address Register Mask02 (Lower) (Function #0)	PCI_EP_BARMSK02L_F0	0000_1FFFh	32
60B4h	Base Address Register Mask02 (Upper) (Function #0)	PCI_EP_BARMSK02U_F0	0000_0000h	32
60B8h to 60C4h	Debug	—	—	—
60C8h	Base Size 00/01 (Function #0)	PCI_EP_BSIZE00_01_F0	0000_0000h	32
60CCh	Base Size 02/03 (Function #0)	PCI_EP_BSIZE02_03_F0	0000_0000h	32
60D0h	Base Size 04/05 (Function #0)	PCI_EP_BSIZE04_05_F0	0000_0000h	32
60D4h	Base Size 06 (Function #0)	PCI_EP_BSIZE06_F0	0000_0000h	32
60D8h	Type Supported 00/01/02 (Function #0)	PCI_EP_TSUPPORT00_01_02_F0	0033_3333h	32
60DCh	Debug	—	—	—
MSI and MSI-X Capability Structure				
60E0h	MSI Capability (Function #0)	PCI_EP_MSICAP_F0	018A_6005h	32
60E4h	Message Address (Function #0)	PCI_EP_MSGADR_F0	0000_0000h	32
60E8h	Message Upper Address (Function #0)	PCI_EP_MSGUADR_F0	0000_0000h	32
60ECh	Message Data (Function #0)	PCI_EP_MSGDAT_F0	0000_0000h	32
60F0h	Mask Bits (Function #0)	PCI_EP_MSKBIT_F0	0000_0000h	32
60F4h	Pending Bits (Function #0)	PCI_EP_PENDBIT_F0	0000_0000h	32
60F8h to 60FCh	Reserved	—	—	—
Advanced Error Reporting (AER) Capability				
6100h	Advanced Error Reporting Capability (Function #0)	PCI_EP_ADVERC_F0	1501_0001h	32
6104h	Uncorrectable Error Status Register (Function #0)	PCI_EP_UNCESTS_F0	0000_0000h	32
6108h	Uncorrectable Error Mask Register (Function #0)	PCI_EP_UNCEMASK_F0	0000_0000h	32
610Ch	Uncorrectable Error Severity Register (Function #0)	PCI_EP_UNCESVY_F0	0046_2030h	32
6110h	Correctable Error Status Register (Function #0)	PCI_EP_CESTS_F0	0000_0000h	32
6114h	Correctable Error Mask Register (Function #0)	PCI_EP_CEMASK_F0	0000_2000h	32
6118h	Advanced Error Capabilities and Control Register (Function #0)	PCI_EP_ADVECC_F0	0000_00A0h	32
611Ch	Header Log Register 0 (Function #0)	PCI_EP_HLOG0_F0	0000_0000h	32
6120h	Header Log Register 1 (Function #0)	PCI_EP_HLOG1_F0	0000_0000h	32
6124h	Header Log Register 2 (Function #0)	PCI_EP_HLOG2_F0	0000_0000h	32
6128h	Header Log Register 3 (Function #0)	PCI_EP_HLOG3_F0	0000_0000h	32
612Ch to 614Ch	Reserved	—	—	—
Device Serial Number Capability				
6150h	Device Serial Number Extended Capability (Function #0)	PCI_EP_DEVSNEXTC_F0	0001_0003h	32
6154h	Serial Number Register (Lower DW) (Function #0)	PCI_EP_SNL_F0	0000_0000h	32
6158h	Serial Number Register (Upper DW) (Function #0)	PCI_EP_SNU_F0	0000_0000h	32

Table 36.5-2 PCI Express Configuration Registers (Type0) (3/5)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
615Ch	Reserved	—	—	—
6160h to 616Ch	Debug	—	—	—
6170h to 618Ch	Reserved	—	—	—
6190h to 6194h	Debug	—	—	—
6198h to 6FFCh	Reserved	—	—	—
Common Configuration Space				
7000h	Vendor and Device ID (Function #1)*1	PCI_EP_VID_F1	Configurable value	32
7004h	Command and Status (Function #1)	PCI_EP_COM_STA_F1	0010_0000h	32
7008h	Revision ID and Class Code (Function #1)*1	PCI_EP_RID_CC_F1	Configurable value	32
700Ch	Cache Line and Header Type (Function #1)	PCI_EP_CL_HT_F1	0080_0000h	32
Configuration Space				
7010h	Base Address Register 0 (Function #1)	PCI_EP_BAR0_F1	0000_0004h	32
7014h	Base Address Register 1 (Function #1)	PCI_EP_BAR1_F1	0000_0000h	32
7018h	Base Address Register 2 (Function #1)	PCI_EP_BAR2_F1	0000_0004h	32
701Ch	Base Address Register 3 (Function #1)	PCI_EP_BAR3_F1	0000_0000h	32
7020h	Base Address Register 4 (Function #1)	PCI_EP_BAR4_F1	0000_0004h	32
7024h	Base Address Register 5 (Function #1)	PCI_EP_BAR5_F1	0000_0000h	32
7028h	Reserved	—	—	—
702Ch	Subsystem ID (Function #1)*1	PCI_EP_SSID_F1	Configurable value	32
7030h	Reserved	—	—	—
7034h	Capabilities Pointer (Function #1)	PCI_EP_CP_F1	0000_0040h	32
7038h	Reserved	—	—	—
703Ch	Interrupt (Function #1)	PCI_EP_INT_F1	0000_0100h	32
PCI Power Management Capability Structure				
7040h	PM Capabilities (Function #1)	PCI_EP_PMC_F1	4803_E001h	32
7044h	PM Status/Control (Function #1)	PCI_EP_PMSC_F1	0000_0008h	32
7048h to 705Ch	Reserved	—	—	—
PCI Express Capability Structure				
7060h	PCI Express Capability (Function #1)	PCI_EP_PCIEC_F1	0002_0010h	32
7064h	Device Capabilities (Function #1)	PCI_EP_DEVC_F1	1000_8FC0h	32
7068h	Device Control/Status (Function #1)	PCI_EP_DEVCS_F1	0000_2010h	32
706Ch	Link Capabilities (Function #1)	PCI_EP_LINKC_F1	0043_6C22h	32
7070h	Link Control/Status (Function #1)	PCI_EP_LINKCS_F1	1000_0000h	32
7074h	Reserved	—	—	—
7078h	Reserved	—	—	—
707Ch	Reserved	—	—	—
7080h	Reserved	—	—	—
7084h	Device Capabilities 2 (Function #1)	PCI_EP_DEVC2_F1	0000_0012h	32
7088h	Device Control 2/Status 2 (Function #1)	PCI_EP_DEVCS2_F1	0000_0000h	32
708Ch	Link Capabilities 2 (Function #1)	PCI_EP_LINKC2_F1	0000_0006h	32
7090h	Link Control 2/Status 2 (Function #1)	PCI_EP_LINCS2_F1	0000_0002h	32
7094h	Reserved	—	—	—

Table 36.5-2 PCI Express Configuration Registers (Type0) (4/5)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
7098h	Reserved	—	—	—
709Ch	Reserved	—	—	—
Specific Registers				
70A0h	Base Address Register Mask00 (Lower) (Function #1)	PCI_EP_BARMSK00L_F1	0FFF_FFFFh	32
70A4h	Base Address Register Mask00 (Upper) (Function #1)	PCI_EP_BARMSK00U_F1	0000_0000h	32
70A8h	Base Address Register Mask01 (Lower) (Function #1)	PCI_EP_BARMSK01L_F1	0000_0000h	32
70ACh	Base Address Register Mask01 (Upper) (Function #1)	PCI_EP_BARMSK01U_F1	0000_0000h	32
70B0h	Base Address Register Mask02 (Lower) (Function #1)	PCI_EP_BARMSK02L_F1	0000_1FFFh	32
70B4h	Base Address Register Mask02 (Upper) (Function #1)	PCI_EP_BARMSK02U_F1	0000_0000h	32
70B8h to 70C4h	Debug	—	—	—
70C8h	Base Size 00/01 (Function #1)	PCI_EP_BSIZE00_01_F1	0000_0000h	32
70CCh	Base Size 02/03 (Function #1)	PCI_EP_BSIZE02_03_F1	0000_0000h	32
70D0h	Base Size 04/05 (Function #1)	PCI_EP_BSIZE04_05_F1	0000_0000h	32
70D4h	Base Size 06 (Function #1)	PCI_EP_BSIZE06_F1	0000_0000h	32
70D8h	Type Supported 00/01/02 (Function #1)	PCI_EP_TSUPPORT00_01_02_F1	0033_3333h	32
70DCh	Debug	—	—	—
MSI and MSI-X Capability Structure				
70E0h	MSI Capability (Function #1)	PCI_EP_MSICAP_F1	018A_6005h	32
70E4h	Message Address (Function #1)	PCI_EP_MSGADR_F1	0000_0000h	32
70E8h	Message Upper Address (Function #1)	PCI_EP_MSGUADR_F1	0000_0000h	32
70ECh	Message Data (Function #1)	PCI_EP_MSGDAT_F1	0000_0000h	32
70F0h	Mask Bits (Function #1)	PCI_EP_MSKBIT_F1	0000_0000h	32
70F4h	Pending Bits (Function #1)	PCI_EP_PENDBIT_F1	0000_0000h	32
70F8h to 70FCh	Reserved	—	—	—
Advanced Error Reporting (AER) Capability				
7100h	Advanced Error Reporting Capability (Function #1)	PCI_EP_ADVERC_F1	1501_0001h	32
7104h	Uncorrectable Error Status Register (Function #1)	PCI_EP_UNCESTS_F1	0000_0000h	32
7108h	Uncorrectable Error Mask Register (Function #1)	PCI_EP_UNCEMASK_F1	0000_0000h	32
710Ch	Uncorrectable Error Severity Register (Function #1)	PCI_EP_UNCESVY_F1	0046_2030h	32
7110h	Correctable Error Status Register (Function #1)	PCI_EP_CESTS_F1	0000_0000h	32
7114h	Correctable Error Mask Register (Function #1)	PCI_EP_CEMASK_F1	0000_2000h	32
7118h	Advanced Error Capabilities and Control Register (Function #1)	PCI_EP_ADVECC_F1	0000_00A0h	32
711Ch	Header Log Register 0 (Function #1)	PCI_EP_HLOG0_F1	0000_0000h	32
7120h	Header Log Register 1 (Function #1)	PCI_EP_HLOG1_F1	0000_0000h	32
7124h	Header Log Register 2 (Function #1)	PCI_EP_HLOG2_F1	0000_0000h	32
7128h	Header Log Register 3 (Function #1)	PCI_EP_HLOG3_F1	0000_0000h	32
712Ch to 714Ch	Reserved	—	—	—
Device Serial Number Capability				
7150h	Device Serial Number Extended Capability(Function #1)	PCI_EP_DEVSNEXTC_F1	0001_0003h	32
7154h	Serial Number Register (Lower DW) (Function #1)	PCI_EP_SNL_F1	0000_0000h	32
7158h	Serial Number Register (Upper DW) (Function #1)	PCI_EP_SNU_F1	0000_0000h	32
715Ch	Reserved	—	—	—

Table 36.5-2 PCI Express Configuration Registers (Type0) (5/5)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
7160h to 716Ch	Debug	—	—	—
7170h to 718Ch	Reserved	—	—	—
7190h to 7194h	Debug	—	—	—
7198h to 7FFCh	Reserved	—	—	—

Note: “Specific Registers” refer to the registers specific to this unit. They cannot be controlled from the root complex. When the values need to be changed from the initial values, they must be set from the CPU, etc. of the endpoint before the link is up.

Note 1. Set the initial value from the local CPU, etc.

36.5.3 Register Descriptions (Endpoint Mode)

36.5.3.1 AXI Bridge Registers

(1) Request Data Register m (PCI_EP_REQDATAm) (m = 0 to 2)

This register issues various requests. Write access to this register is only possible from AXI. In case of write access from PCIe, it returns a response and ends normally without writing data to this register. Read access is possible from both AXI and PCIe.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0080h (m = 0)
<PCI_S0_REG_base> + 0084h (m = 1)
<PCI_S0_REG_base> + 0088h (m = 2)

Initial Value: xxxx_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Request Data															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Request Data															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-3 PCI_EP_REQDATAm Register Contents

Bit Position	Bit Name	Description
31 to 0	Request Data	Set write data for issuing a request.

Table 36.5-4 Valid Reset Signal

	Request Data Register 0	Request Data Register 1	Request Data Register 2
Zero-Length Read Request	Invalid	Invalid	Invalid
Message Request	3rd header	4th header	Invalid
Message Request with data payload	3rd header	4th header	Message data

Note: The bits should be set to 0 for the requests indicated as “Invalid”.

(2) Request Receive Data Register (PCI_EP_REQRCVDAT)

This register indicates the data read on reception of the completion response after issuing a read request.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 008Ch

Initial Value: xxxx_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Request Receive Data															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Request Receive Data															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-5 PCI_EP_REQRCVDAT Register Contents

Bit Position	Bit Name	Description
31 to 0	Request Receive Data	After issuing a read request, the data read on reception of the completion response are set in these bits. However, these bits are invalid for any kind of write request.

(3) Request Address Register 1 (PCI_EP_REQADR1)

This register issues requests. Write access to this register is only possible from AXI. In case of write access from PCIe, it returns a response and ends normally without writing data to this register. Read access is possible from both AXI and PCIe.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0090h

Initial Value: xxxx_xxxxh

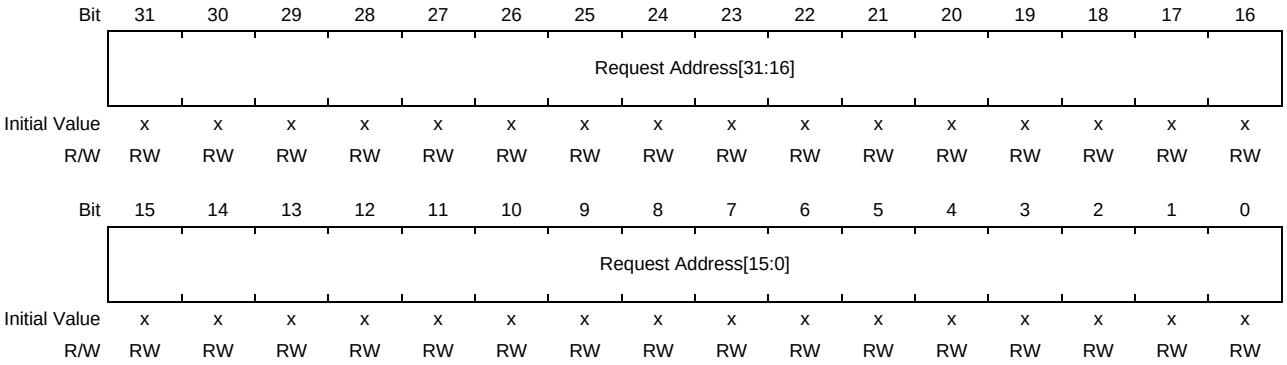


Table 36.5-6 PCI_EP_REQADR1 Register Contents

Bit Position	Bit Name	Description
31 to 0	Request Address [31:0]	Set the address for issuing a request.

Table 36.5-7 Valid Reset Signal

	[31:27]	[26:24]	[23:19]	[18:16]
Zero-Length Read Request	Address			
Message Request	Reserved	Routing Type	Reserved	Reserved
Message Request with data payload	Reserved	Routing Type	Reserved	Reserved

	[15:12]	[11:8]	[7:2]	[1:0]
Zero-Length Read Request	Address			Reserved
Message Request	Reserved	Reserved	Message Code	
Message Request with data payload	Reserved	Reserved	Message Code	

Note: The bits should be set to 0 for the requests indicated as “Reserved”.

(4) Request Address Register 2 (PCI_EP_REQADR2)

This register issues requests. Write access to this register is only possible from AXI. In case of write access from PCIe, it returns a response and ends normally without writing data to this register. Read access is possible from both AXI and PCIe.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0094h

Initial Value: xxxx_xxxxh

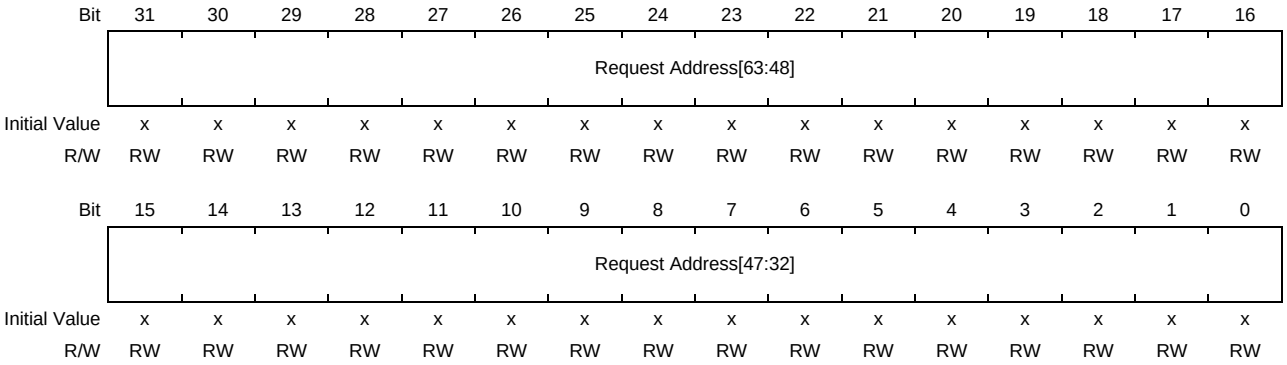


Table 36.5-8 PCI_EP_REQADR2 Register Contents

Bit Position	Bit Name	Description
31 to 0	Request Address [63:32]	Set the address for issuing a request.

Table 36.5-9 Valid Reset Signal

	[31:0]
Zero-Length Read Request	Address
Message Request	Invalid
Message Request with data payload	Invalid

Note: The bits should be set to 0 for the requests indicated as “Invalid”.

(5) Request Byte Enable Register (PCI_EP_REQBE)

This register specifies the first byte enable bit within the TLP header (1st DW byte) when issuing a request to PCIe. Write access to this register is only possible from AXI. In case of write access from PCIe, it returns a response and ends normally without writing data to this register. Read access is possible from both AXI and PCIe.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0098h

Initial Value: 0000_000Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	Request Byte Enable			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 36.5-10 PCI_EP_REQBE Register Contents

Bit Position	Bit Name	Description
31 to 4	—	Reserved. These bits are read as 0b.
3 to 0	Request Byte Enable	Specify byte enabling in the issuing of IO/Cfg requests as required. Usually, the setting should be 1111b. 1b: Enable byte. 0b: Disable byte.

Table 36.5-11 Valid Reset Signal

	[3:0]
Zero-Length Read Request	0000b
Message Request	Invalid (1111b)
Message Request with data payload	Invalid (1111b)

(6) Request Issue Register (PCI_EP_REQISS)

This register issues a request to PCIe. Write access to this register is only possible from AXI. In case of write access from PCIe, it returns a response and ends normally without writing data to this register. Read access is possible from both AXI and PCIe.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 009Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	Request Rejection	MOR CD PERR	MOR CH PERR	MOR EP ERR	MOR_STATUS		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	FUNC			TR Type				—	—	—	—	—	—	—	Request Issue
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	RW

Table 36.5-12 PCI_EP_REQISS Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b.
22	Request Rejection	Indicates that processing has been forcibly terminated in response to detection of the PCI Express transmission (TX) side being stopped or suspended. 0b: Normal state (a request is issued) 1b: Forced termination (rejection)
21	MOR CD PERR	Set to 1b if a data error occurs in the completion TLP for a non-posted request issued by this register. Not normally used. It is not updated at the time of a posted request.
20	MOR CH PERR	Set to 1b if a header error occurs in the completion TLP for a non-posted request issued by this register. Not normally used. It is not updated at the time of a posted request.
19	MOR EP ERR	Set to 1b if a poisoned completion TLP for a non-posted request issued by this register is received. Not normally used. It is not updated at the time of a posted request.
18 to 16	MOR_STATUS	Hold the MOR status in the completion TLP for a non-posted request issued by this register. It is not updated at the time of a posted request. 000b: Successful Completion (SC) 001b: Unsupported Request (UR) 010b: Configuration Request Retry Status (CRS) (not supported) 011b: Completion Timeout 100b: Completer Abort (CA) 101b: Unexpected Completion and mismatched type (Lock Completion respond to non-Lock Request) 110b: Reserved 111b: Overrun Completion length
15	—	Reserved. This bit is read as 0b.
14 to 12	FUNC	Set the function of requests.
11 to 8	TR Type	Set the request type (see **Table 36.5-13**).
7 to 1	—	Reserved. These bits are read as 0b.

Table 36.5-12 PCI_EP_REQISS Register Contents (2/2)

Bit Position	Bit Name	Description
0	Request Issue	When written: 1b: Issue a request. 0b: No operation When read: 1b: A request is being processed (indicating that the issued request is being processed). 0b: Issuing a new request is acceptable (indicating that the issued request has been completed).

Table 36.5-13 Valid Reset Signal

	TR Type		Device Type	
	[11:8]	Posted/Non-Posted	Root Complex	Endpoint
Zero-Length Read Request	0000b (0h)	Non-posted	Issuable	Issuable
Configuration Read Type0	0100b (4h)	Non-posted	Issuable	Issuing prohibited
Configuration Write Type0	0101b (5h)	Non-posted	Issuable	Issuing prohibited
Configuration Read Type1	0110b (6h)	Non-posted	Issuable	Issuing prohibited
Configuration Write Type1	0111b (7h)	Non-posted	Issuable	Issuing prohibited
Message Request	1000b (8h)	Posted	Issuable	Issuable
Message Request with data payload	1001b (9h)	Posted	Issuable	Issuable
	Others	—	Issuing prohibited	Issuing prohibited

(7) PCI INTx Out Status Register (PCI_EP_INTXOUTS)

This register can confirm the PCI INTx status issued by the unit with the interrupt input signal (INTX_EP_F*: active high). In addition, the value of this register is not reflected if the INTx message is asserted or deasserted by issuing a special request (prohibited operation). This register is only valid in endpoint mode.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0118h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	Debug					—	—	—	—	INTD Status	INTC Status	INTB Status	INTA Status
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-14 PCI_EP_INTXOUTS Register Contents

Bit Position	Bit Name	Description
31 to 13	—	Reserved. These bits are read as 0b.
12 to 8	Debug	Debug register
7 to 4	—	Reserved. These bits are read as 0b.
3	INTD Status	Set in response to transmission of an assert INTD message. Cleared in response to transmission of a de-assert INTD message. 0b: De-assert 1b: Assert
2	INTC Status	Set in response to transmission of an assert INTC message. Cleared in response to transmission of a de-assert INTC message. 0b: De-assert 1b: Assert
1	INTB Status	Set in response to transmission of an assert INTB message. Cleared in response to transmission of a de-assert INTB message. 0b: De-assert 1b: Assert
0	INTA Status	Set in response to transmission of an assert INTA message. Cleared in response to transmission of a de-assert INTA message. 0b: De-assert 1b: Assert

(8) Message Receive Interrupt Enable Register (PCI_EP_MSGRCVIE)

This register controls enabling of MSG_INT in response to the reception of message requests other than INTx and error-related messages.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0120h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	Message Receive Interrupt Enable	—	—	—	—	PM_Active_State_Nak Receive Interrupt Enable	PM_PME Receive Interrupt Enable	PME_Turn_Off Receive Interrupt Enable	PME_TO_Ack Receive Interrupt Enable
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	R	R	R	R	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-15 PCI_EP_MSGRCVIE Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24	Message Receive Interrupt Enable	Enables assertion of MSG_INT in response to reception of a message. 0b: Disabled 1b: Enabled
23 to 20	—	Reserved. These bits are read as 0b.
19	PM_Active_State_Nak Receive Interrupt Enable	Enables assertion of MSG_INT in response to reception of PM_Active_State_Nak. 0b: Disabled 1b: Enabled
18	PM_PME Receive Interrupt Enable	Enables assertion of MSG_INT in response to reception of PM_PME. EP is not supported. Fixed to 0b.
17	PME_Turn_Off Receive Interrupt Enable	Enables assertion of MSG_INT in response to reception of PME_Turn_Off. 0b: Disabled 1b: Enabled
16	PME_TO_Ack Receive Interrupt Enable	Enables assertion of MSG_INT in response to reception of PME_TO_Ack. EP is not supported. Fixed to 0b.
15 to 0	—	Reserved. These bits are read as 0b.

(9) Message Receive Interrupt Status Register (PCI_EP_MSGRCVIS)

This register is a status register that indicates the reception of message requests other than INTx and error-related messages. The value of this register is reflected in MSG_INT. Only the message code is used to decide the message type, and the corresponding message is assumed to have been received while the validity of the routing and the validity of the Msg/MsgD selection are not verified.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0124h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	Message Receive Interrupt	—	—	—	—	PM_Active_State_Nak Receive Interrupt	PM_PME Receive Interrupt	PME_Turn_Off Receive Interrupt	PME_TO_Ack Receive Interrupt
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	R	R	R	R	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-16 PCI_EP_MSGRCVIS Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24	Message Receive Interrupt	Set in response to the reception of a message (regardless of the message type). It is cleared by writing 1b. Writing 0b has no effect.
23 to 20	—	Reserved. These bits are read as 0b.
19	PM_Active_State_Nak Receive Interrupt	This bit is set in response to the reception of a PM_Active_State_Nak message.
18	PM_PME Receive Interrupt	EP is not supported.
17	PME_Turn_Off Receive Interrupt	Invalid due to RC.
16	PME_TO_Ack Receive Interrupt	EP is not supported.
15 to 0	—	Reserved. These bits are read as 0b.

(10) Message Code Register (PCI_EP_MSGCODE)

This register stores the code and routing of the last received message.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0130h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Message Code								Routing			—	—	—	—	Message Payload
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-17 PCI_EP_MSGCODE Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15 to 8	Message Code	Stores the code of the last received message.
7 to 5	Routing	Stores routing of the last received message.
4 to 1	—	Reserved. These bits are read as 0b.
0	Message Payload	Stores the presence or absence of the data payload of the last received message. 1b: MsgD (with payload) 0b: Msg (without payload)

Note: When a Power Management message (PME_TO_Ack Message, PME_Turn_Off Message, PM_PME Message, PM_Active_State_Nak Message) is received, this register is not written.

(11) Message Data Register (PCI_EP_MSGDATA)

This register stores the data of the last received message.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0134h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Message Data															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Message Data															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-18 PCI_EP_MSGDATA Register Contents

Bit Position	Bit Name	Description
31 to 0	Message Data	Stores the first DW data of the last received message. Only updated when MsgD (with data) is received and retains the previous data when Msg (without data) is received

Note: When a Power Management message (PME_TO_Ack Message, PME_Turn_Off Message, PM_PME Message, PM_Active_State_Nak Message) is received, this register is not written.

(12) Message Header 3rdDW Register (PCI_EP_MSGH3DW)

This register stores the header (3rd DW) of the last received message.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0138h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Message Header 3rd DW															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Message Header 3rd DW															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-19 PCI_EP_MSGH3DW Register Contents

Bit Position	Bit Name	Description
31 to 0	Message Header 3rd DW	Stores the header (3rd DW) of the last received message.

Note: When a Power Management message (PME_TO_Ack Message, PME_Turn_Off Message, PM_PME Message, PM_Active_State_Nak Message) is received, this register is not written.

(13) Message Header 4thDW Register (PCI_EP_MSGH4DW)

This register stores the header (4th DW) of the last received message.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 013Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Message Header 4th DW															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Message Header 4th DW															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-20 PCI_EP_MSGH4DW Register Contents

Bit Position	Bit Name	Description
31 to 0	Message Header 4th DW	Stores the header (4th DW) of the last received message.

Note: When a Power Management message (PME_TO_Ack Message, PME_Turn_Off Message, PM_PME Message, PM_Active_State_Nak Message) is received, this register is not written.

(14) Interrupt Table Register (PCI_EP_INTTABLE)

This register is an index of interrupt factors. The interrupt signal (active high) status of each category can be monitored in a list.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0140h

Initial Value: 00xx_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Debug															
Initial Value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Debug	—	—	—	Debug	AXI_ERR_INT	PCIE_EVT _INT	MSG_INT	—	—	—	Debug				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-21 PCI_EP_INTTABLE Register Contents

Bit Position	Bit Name	Description
31 to 15	Debug	Debug register
14 to 12	—	Reserved. These bits are read as 0b.
11	Debug	Debug register
10	AXI_ERR_INT	Error interrupt monitor register
9	PCIE_EVT _INT	Event interrupt monitor register
8	MSG_INT	Message interrupt monitor register
7 to 5	—	Reserved. These bits are read as 0b.
4 to 0	Debug	Debug register

Note: See the description of the terminal of the same name for details of the register.

(15) PCIe Event Interrupt Enable 0 Register (PCI_EP_PEIE0)

This register enables interrupts of the various PCI Express event factors. This register enables writing to the PCIe Event Interrupt Status 1 Register (address: <PCI_S0_REG_base> + 0204h).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0200h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	UI_LINK_WIDTH_CHANG_DONE EN	UI_LINK_SPEED_CHANG_DONE EN	Request Done EN	—	—	Debug	CA EN	Debug		—	Debug				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	R	RW	RW	RW	RW	R	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Debug		—	RX_DLLP_PM_ENTER_L23 EN	Debug	ASPM L1 Rejected EN	DL_UpDown EN	Debug					—	—	—	Debug
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	RW

Table 36.5-22 PCI_EP_PEIE0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b.
30	UI_LINK_WIDTH_CHANGE_DONE EN	Up/Down configuration complete interrupt enable 0b: Disabled 1b: Enabled
29	UI_LINK_SPEED_CHANGE_DONE EN	Speed change complete interrupt enable 0b: Disabled 1b: Enabled
28	Request Done EN	Request complete interrupt enable 0b: Disabled 1b: Enabled
27, 26	—	Reserved. These bits are read as 0b.
25	Debug	Debug register
24	CA EN	CA (completer abort) interrupt enable 0b: Disabled 1b: Enabled
23, 22	Debug	Debug register
21	—	Reserved. This bit is read as 0b.
20 to 14	Debug	Debug register
13	—	Reserved. This bit is read as 0b.
12	RX_DLLP_PM_ENTER_L23 EN	RX_DLLP_PM_ENTER_L23 interrupt enable 0b: Disabled 1b: Enabled
11	Debug	Debug register
10	ASPM L1 Rejected EN	ASPM L1 rejected interrupt enable 0b: Disabled 1b: Enabled

Table 36.5-22 PCI_EP_PEIE0 Register Contents (2/2)

Bit Position	Bit Name	Description
9	DL_UpDown EN	The DL state change interrupt enable 0b: Disabled 1b: Enabled
8 to 4	Debug	Debug register
3 to 1	—	Reserved. These bits are read as 0b.
0	Debug	Debug register

Note: Debug: Registers for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.

(16) PCIe Event Interrupt Status 0 Register (PCI_EP_PEIS0)

This register is a status register to indicate interrupts of the various PCI Express event factors. Set to 1b by the factor in the table. After checking the factor, write 1b to the corresponding bit to clear it.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0204h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	UI_LINK_WIDTH_CHANG_DONE	UI_LINK_SPEED_CHANG_DONE	Request Done	—	—	Debug	CA	Debug		—	Debug				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW1	RW1	RW1	R	R	RW1	RW1	RW1	RW1	R	RW1	RW1	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Debug		—	RX_DLLP_PM_TER_L23	Debug	ASPM L1 Rejected	DL_UpDown	Debug								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	RW1	R	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	R	R	R	RW1

Table 36.5-23 PCI_EP_PEIS0 Register Contents

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b.
30	UI_LINK_WIDTH_CHANGE_DONE	Indicates the completion of up/down configuration. It is cleared by writing 1b. Writing 0b has no effect.
29	UI_LINK_SPEED_CHANGE_DONE	Indicates the completion of a speed change. It is cleared by writing 1b. Writing 0b has no effect.
28	Request Done	Indicates the completion of a request. It is cleared by writing 1b. Writing 0b has no effect.
27, 26	—	Reserved. These bits are read as 0b.
25	Debug	Debug register
24	CA	Indicates the response to the other-party device by CA (completer abort). It is cleared by writing 1b. Writing 0b has no effect.
23, 22	Debug	Debug register
21	—	Fixed to 0b.
20 to 14	Debug	Debug register
13	—	Reserved. This bit is read as 0b.
12	RX_DLLP_PM_TER_L23	Indicates a transition of the power management control state to L2/L3. It is cleared by writing 1b. Writing 0b has no effect.
11	Debug	Debug register
10	ASPM L1 Rejected	Do not use (enable) this bit in Endpoint Mode.
9	DL_UpDown	If the DL_Down state is changed to the DL_UP state or the DL_Up state is changed to the DL_Down state, set to 1b. To check the DL_Down/DL_Up state, use the PCIe Core Status 1 Register (address: <PCI_S0_REG_base> + 0408h). It is cleared by writing 1b. Writing 0b has no effect.
8 to 0	Debug	Debug register

(17) PCIe Event Interrupt Enable 1 Register (PCI_EP_PEIE1)

This register enables parity error and ECC error interrupts. When each bit is set to valid, the value of each corresponding status bit of the PCIe event interrupt status 1 register (address: <PCI_S0_REG_base> + 020Ch) becomes valid.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0208h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXB_PARITY_ERR_EN	ERR_RPC_REPLAYFIFO_PERR_EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ERR_REPLAY_UPPER_CORRECTABLE_ERROR_EN	ERR_REPLAY_LOWER_CORRECTABLE_ERROR_EN	—	—	—	—	—	—	ERR_REPLAY_UPPER_UNCORRECTABLE_ERROR_EN	ERR_REPLAY_LOWER_UNCORRECTABLE_ERROR_EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	R	R	R	R	R	R	RW	RW

Table 36.5-24 PCI_EP_PEIE1 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 18	—	Reserved. These bits are read as 0b.
17	TXB_PARITY_ERR EN	Enables a TXB_PARITY_ERR interrupt. Enables notification of parity error interrupts in the Tx buffer mounted on the transaction layer. 0b: Disabled 1b: Enabled
16	ERR_RPC_REPLAYFIFO_PERR EN	Enables an ERR_RPC_REPLAYFIFO_PERR interrupt. Enables notification of parity error interrupts in the replay FIFO mounted on the data link layer. 0b: Disabled 1b: Enabled
15 to 10	—	Reserved. These bits are read as 0b.
9	ERR_REPLAY_UPPER_CORRECTABLE_ERROR EN	Enables an ERR_REPLAY_UPPER_CORRECTABLE_ERROR interrupt. Enables notification of ECC 1-bit error (correctable error) occurrence interrupts in the upper 64 bits of the data bus of the replay FIFO mounted on the data link layer. 0b: Disabled 1b: Enabled
8	ERR_REPLAY_LOWER_CORRECTABLE_ERROR EN	Enables an ERR_REPLAY_LOWER_CORRECTABLE_ERROR interrupt. Enables notification of ECC 1-bit error (correctable error) occurrence interrupts in the lower 64 bits of the data bus of the replay FIFO mounted on the data link layer. 0b: Disabled 1b: Enabled
7 to 2	—	Reserved. These bits are read as 0b.
1	ERR_REPLAY_UPPER_UNCORRECTABLE_ERROR EN	Enables an ERR_REPLAY_UPPER_CORRECTABLE_ERROR interrupt. Enables notification of ECC 2-bit or more error (uncorrectable error) occurrence interrupts in the upper 64 bits of the data bus of the replay FIFO mounted on the data link layer. 0b: Disabled 1b: Enabled

Table 36.5-24 PCI_EP_PEIE1 Register Contents (2/2)

Bit Position	Bit Name	Description
0	ERR_REPLAY_LOWER_UNCORRECTABLE_ERROR EN	Enables an ERR_REPLAY_LOWER_UNCORRECTABLE_ERROR interrupt. Enables notification of ECC 2-bit or more error (uncorrectable error) occurrence interrupts in the lower 64 bits of the data bus of the replay FIFO mounted on the data link layer. 0b: Disabled 1b: Enabled

(18) PCIe Event Interrupt Status 1 Register (PCI_EP_PEIS1)

This register is a status register that indicates parity error and ECC error interrupts. After checking the factor, write 1b to the corresponding bit to clear it.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 020Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TXB_PARITY_ERR	ERR_RPC_REPLAYFIFO_PERR
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ERR_REPLAY_UPPER_CORRECTABLE_ERROR	ERR_REPLAY_LOWER_CORRECTABLE_ERROR	—	—	—	—	—	—	ERR_REPLAY_UPPER_UNCORRECTABLE_ERROR	ERR_REPLAY_LOWER_UNCORRECTABLE_ERROR
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW1	RW1	R	R	R	R	R	R	RW1	RW1

Table 36.5-25 PCI_EP_PEIS1 Register Contents

Bit Position	Bit Name	Description
31 to 18	—	Reserved. These bits are read as 0b.
17	TXB_PARITY_ERR	TXB_PARITY_ERR interrupt. Notification of parity error interrupts in the Tx buffer mounted on the transaction layer. It is cleared by writing 1b. Writing 0b has no effect.
16	ERR_RPC_REPLAYFIFO_PERR	ERR_RPC_REPLAYFIFO_PERR interrupt. Notification of parity error interrupts in the replay FIFO mounted on the data link layer. It is cleared by writing 1b. Writing 0b has no effect.
15 to 10	—	Reserved. These bits are read as 0b.
9	ERR_REPLAY_UPPER_CORRECTABLE_ERROR	ERR_REPLAY_UPPER_CORRECTABLE_ERROR interrupt. Notification of ECC 1-bit error (correctable error) occurrence interrupts in the upper 64 bits of the data bus of the replay FIFO mounted on the data link layer. It is cleared by writing 1b. Writing 0b has no effect.
8	ERR_REPLAY_LOWER_CORRECTABLE_ERROR	ERR_REPLAY_LOWER_CORRECTABLE_ERROR interrupt. Notification of ECC 1-bit error (correctable error) occurrence interrupts in the lower 64 bits of the data bus of the replay FIFO mounted on the data link layer. It is cleared by writing 1b. Writing 0b has no effect.
7 to 2	—	Reserved. These bits are read as 0b.
1	ERR_REPLAY_UPPER_UNCORRECTABLE_ERROR	ERR_REPLAY_UPPER_CORRECTABLE_ERROR interrupt. Notification of ECC 2-bit or more error (uncorrectable error) occurrence interrupts in the upper 64 bits of the data bus of the replay FIFO mounted on the data link layer. It is cleared by writing 1b. Writing 0b has no effect.
0	ERR_REPLAY_LOWER_UNCORRECTABLE_ERROR	ERR_REPLAY_LOWER_UNCORRECTABLE_ERROR interrupt. Notification of ECC 2-bit or more error (uncorrectable error) occurrence interrupts in the lower 64 bits of the data bus of the replay FIFO mounted on the data link layer. It is cleared by writing 1b. Writing 0b has no effect.

(19) AXI Master Error Interrupt Enable Register (PCI_EP_AMEIE)

This register enables the AXI master error interrupt.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0210h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Write MSTERR INT EN[3:0]				—	—	—	—	Read MSTERR INT EN[3:0]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	R	R	R	R	RW	RW	RW	RW

Table 36.5-26 PCI_EP_AMEIE Register Contents

Bit Position	Bit Name	Description
31 to 12	—	Reserved. These bits are read as 0b.
11 to 8	Write MSTERR INT EN[3:0]	Enables a write MSTERR INT. Each of the corresponding bits is individually turned on/off. 0b: Disabled 1b: Enabled
7 to 4	—	Reserved. These bits are read as 0b.
3 to 0	Read MSTERR INT EN[3:0]	Enables a read MSTERR INT. Each of the corresponding bits is individually turned on/off. 0b: Disabled 1b: Enabled

(20) AXI Master Error Interrupt Status Register (PCI_EP_AMEIS)

This register indicates the AXI master error interrupt status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0214h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	Write ERR ID				—	—	—	—	Read ERR ID			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Write MSTERR INT EN[3:0]				—	—	—	—	Read MSTERR INT EN[3:0]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW1	RW1	RW1	RW1	R	R	R	R	RW1	RW1	RW1	RW1

Table 36.5-27 PCI_EP_AMEIS Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b.
27 to 24	Write ERR ID	Saves the ID on the first reception of DECERR or SLVERR. When bits [11:8] are cleared, a new error ID can be saved. 0000b: Normal access.
23 to 20	—	Reserved. These bits are read as 0b.
19 to 16	Read ERR ID	Saves the ID on the first reception of DECERR or SLVERR. When bits [3:0] are cleared, a new error ID can be saved. 0000b: Normal access.
15 to 12	—	Reserved. These bits are read as 0b.
11 to 8	Write MSTERR INT[3:0]	Indicates that an error was detected on the AXI master port. Only the first error detected is saved. When bits [11:8] are cleared, a new error can be saved. Bit 11: Length error TEF does not match the length of the data transferred by the data channel. Bit 10: ID mismatch MAWID does not match MBID received by the response channel. Bit 9: DECERR is received. Bit 8: SLVERR is received. These bits are cleared by writing 1b. Writing 0b has no effect.
7 to 4	—	Reserved. These bits are read as 0b.
3 to 0	Read MSTERR INT[3:0]	Indicates that an error was detected on the AXI master port. Only the first error detected is saved. When bits [3:0] are cleared, a new error can be saved. Bit 3: Length error TER does not match the length of the data transferred by the data channel. Bit 2: ID mismatch MARID does not match MRID received by data channel. Bit 1: DECERR is received. Bit 0: SLVERR is received. These bits are cleared by writing 1b. Writing 0b has no effect.

(21) AXI Slave Error Interrupt Enable 1 Register (PCI_EP_ASEIE1)

This register enables the AXI slave error interrupt.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0220h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Write SLVERR INT EN[3:0]				—	—	—	—	—	—	Read SLVERR INT EN[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	R	R	R	R	R	R	RW	RW

Table 36.5-28 PCI_EP_ASEIE1 Register Contents

Bit Position	Bit Name	Description
31 to 12	—	Reserved. These bits are read as 0b.
11 to 8	Write SLVERR INT EN[3:0]	Enables a write MSTERR INT. Each of the corresponding bits is individually turned on/off. 0b: Disabled 1b: Enabled
7 to 2	—	Reserved. These bits are read as 0b.
1, 0	Read SLVERR INT EN[1:0]	Enables a read MSTERR INT. Each of the corresponding bits is individually turned on/off. 0b: Disabled 1b: Enabled

(22) AXI Slave Error Interrupt Status 1 Register (PCI_EP_ASEIS1)

This register indicates the AXI slave error interrupt status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0224h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Write SLVERR INT[3:0]				—	—	—	—	—	—	Read SLVERR INT[1:0]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW1	RW1	RW1	RW1	R	R	R	R	R	R	RW1	RW1

Table 36.5-29 PCI_EP_ASEIS1 Register Contents

Bit Position	Bit Name	Description
31 to 12	—	Reserved. These bits are read as 0b.
11 to 8	Write SLVERR INT[3:0]	Indicates that an unrecoverable error was detected on the AXI slave port (the response to the transaction is SLVERR). Bit 11: Burst length error. SAWLEN does not match the burst length of the data received by the data channel. Bit 10: ID mismatch SAWID does not match SWID received by the data channel. Bit 9: Burst type invalid SAWBURST is 11b (undefined). When SAWBURST is 10b (wrapping) and the burst length is other than 2, 4, 8, and 16. Bit 8: Data size invalid. SAWSIZE is 100b to 111b (greater than the AXI bus width or not supported). Each bit means the following. 0b: No error detected 1b: Error detected These bits are cleared by writing 1b. Writing 0b has no effect.
7 to 2	—	Reserved. These bits are read as 0b.
1 to 0	Read SLVERR INT[1:0]	Indicates that an unrecoverable error was detected on the AXI slave port (the response to the transaction is SLVERR). Bit 1: Burst type invalid SAWBURST is 11b (undefined). When SAWBURST is 10b (wrapping) and the burst length is other than 2, 4, 8, and 16. Bit 0: Data size invalid SAWSIZE is 100b to 111b (greater than the AXI bus width or not supported) Each bit means the following. 0b: No error detected 1b: Error detected These bits are cleared by writing 1b. Writing 0b has no effect.

(23) AXI Slave Error Interrupt Status 3 Register (PCI_EP_ASEIS3)

This register indicates the AXI ID at the time of the first AXI slave error.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0230h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ERR ID															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR ID															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-30 PCI_EP_ASEIS3 Register Contents

Bit Position	Bit Name	Description
31 to 0	ERR ID	The ID at the time of the first error of the AXI Slave Error Interrupt Status 1 register (address: <PCI_S0_REG_base> + 0224h). Only the first error is saved. A new error ID can be saved when bits [11:8] and bits [1:0] of the AXI Slave Error Interrupt Status 1 register are cleared.

(24) PCIe Event Interrupt Enable 2 Register (PCI_EP_PEIE2)

This register enables interrupts of the various PCI Express event factors. This register enables writing to the PCIe Event Interrupt Status 2 Register (address: <PCI_S0_REG_base> + 0244h).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0240h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LTR_MECHANISM_EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D3_hot_err_EN								CFG_POWER_STATE_EN							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-31 PCI_EP_PEIE2 Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b.
16	LTR_MECHANISM_EN	Enables an interrupt for the CFG_LTR_MECHANISM change detection function.
15 to 8	D3_hot_err_EN	Enables a D3_hot_err status detection interrupt at the time of the D3_EVENT_ACK/TURN_OFF_EVENT_ACK assertion if a transition to the D3hot state (CFG_POWERSTATE! = 0) is detected or a PME_TURN_OFF message is received in the pending state of the completion (ORT_TRANSACTION_PENDING = 1). Bits [15:10] are not used. The lower 2 bits correspond to each function.
7 to 0	CFG_POWER_STATE_EN	Enables a D_STATE_OUT_Fx (x = Function no.) pin change detection function interrupt. Bits [7:2] are not used. The lower 2 bits correspond to each function.

(25) PCIe Event Interrupt Status 2 Register (PCI_EP_PEIS2)

This register indicates the state of various PCI Express events.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0244h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Debug								—	—	—	—	—	—	—	LTR_MECHANISM
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D3_hot_err								CFG_POWER_STATE							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1

Table 36.5-32 PCI_EP_PEIS2 Register Contents

Bit Position	Bit Name	Description
31 to 24	Debug	Register for debugging
23 to 17	—	Reserved. These bits are read as 0b.
16	LTR_MECHANISM	This bit indicates the detection of changes to CFG_LTR_MECHANISM.
15 to 8	D3_hot_err	These bits indicate the D3_hot_err status detection at the time of the D3_EVENT_ACK/TURN_OFF_EVENT_ACK assertion if a transition to the D3hot state (CFG_POWERSTATE! = 0) is detected or the PME_TURN_OFF message is received in the pending state of the completion (ORT_TRANSACTION_PENDING = 1). Bits [15:10] are not used. The lower 2 bits correspond to each function.
7 to 0	CFG_POWER_STATE	This bit indicates the detection of changes to the D_STATE_OUT_Fx (x = Function no.) pin. Bits [7:2] are not used. The lower 2 bits correspond to each function.

(26) Permission Register (PCI_EP_PERM)

This register controls access to the CFGU register.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0300h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	Debug		Stealth Enable
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 36.5-33 PCI_EP_PERM Register Contents

Bit Position	Bit Name	Description
31 to 3	—	Reserved. These bits are read as 0b.
2, 1	Debug	Debug register
0	Stealth Enable	Sets the stealth (invisible) function of the Bridge Register. The stealth function is to restrict access from the PCIe side for security. Write access to this bit from the PCIe side is invalid. The PCIe side cannot access the all Bridge Registers when this function is enabled. Returns 0 when read. 0b: Disable the stealth function. 1b: Enable the stealth function.

(27) Reset Register (PCI_EP_RESET)

This register resets the PCIe core. Supplied to the internal core by OR with the pin of the same name. For details of each pin, see the terminal information. The write value is saved when accessed from the AXI side, but a low-level pulse is generated when the PCIe writes 0b. However, when the AXI has already written 0b, the signal remains at the low level. Writing 1b by the PCIe is ignored.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0310h

Initial Value: 0000_00xxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	force to D0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Debug				RST_PREG_B	RST_OUT_B	RST_PS_B	RST_LOAD_B	RST_CFG_B	RST_RSM_B	RST_GP_B	RST_B
Initial Value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-34 PCI_EP_RESET Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b.
16	force to D0	Forcibly shifts PM control to the D0 state after transmission of PME_TO_Ack. It is automatically cleared when PM control shifts to D0. Use of this bit is generally prohibited, as it can cause a mismatch with the power state of the entire system. 0b: No operation 1b: Shift to D0
15 to 12	—	Reserved. These bits are read as 0b.
11 to 8	Debug	(Fixed to 0000b.) Debug register
7	RST_PREG_B	Not used in this unit. The set value does not affect unit operation. 0b: Reset 1b: Normal operation
6	RST_OUT_B	RST_OUT_B output 0b: Reset 1b: Normal operation
5	RST_PS_B	Reset the PCI Express core (PCLK domain) inside the unit. 0b: Reset 1b: Normal operation
4	RST_LOAD_B	Reset the configuration registers. Reset bits that have not been initialized by RST_LOAD_B. 0b: Reset 1b: Normal operation
3	RST_CFG_B	Reset the configuration registers. 0b: Reset 1b: Normal operation
2	RST_RSM_B	POWERGOOD-Reset AUX Power (AUX not supported)
1	RST_GP_B	Reset the PCI Express core (ACLK domain) inside the unit. 0b: Reset 1b: Normal operation

Table 36.5-34 PCI_EP_RESET Register Contents (2/2)

Bit Position	Bit Name	Description
0	RST_B	Reset the PCI Express core inside the unit. 0b: Reset 1b: Normal operation

(28) Mode Set 0 Register (PCI_EP_MSET0)

This register sets AXI mode.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0314h

Initial Value: 2001_2000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	AWPROT[2:0]			AWCACHE_L[3:0]				—	—	AWLOCK		AWCACHE_D[3:0]			
Initial Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	RW	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	ARPROT			—	—	—	—	—	—	ARLOCK		ARCACHE			
Initial Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 36.5-35 PCI_EP_MSET0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b.
30 to 28	AWPROT[2:0]	Set the protection type in a transition from PCIe to AXI. These bits indicate whether the transaction protection level is “normal”, “privilege”, or “secure”, and whether the transaction is command access or data access. [2] 1b: Command access 0b: Data access [1] 1b: Non-secure access 0b: Secure access [0] 1b: Privilege access 0b: Normal access
27 to 24	AWCACHE_L[3:0]	Indicates the value of MAWCACHE[3:0] issued to AXI. This setting is issued when an AXI request containing the last byte is issued. *Note*: The recommended value is 0000b. [3] 1b: Write allocation enabled 0b: Write allocation disabled [2] 1b: Read allocation enabled 0b: Read allocation disabled [1] 1b: Cacheable 0b: Not cacheable [0] 1b: Bufferable 0b: Not bufferable
23, 22	—	Reserved. These bits are read as 0b.
21, 20	AWLOCK	Lock type in a transition from PCIe to AXI. This signal provides information on the atomic nature of transfer. 00b: Normal access 01b: Exclusive access 10b: Lock access 11b: Reserved
19 to 16	AWCACHE_D[3:0]	Specifies the value of MAWCACHE[3:0] issued to AXI. This setting is issued when an AXI request other than the output condition of AWCACHE_L is issued. *Note*: The recommended value is 0001b. [3] 1b: Write allocation enabled 0b: Write allocation disabled [2] 1b: Read allocation enabled 0b: Read allocation disabled [1] 1b: Cacheable 0b: Not cacheable [0] 1b: Bufferable 0b: Not bufferable
15	—	Reserved. This bit is read as 0b.

Table 36.5-35 PCI_EP_MSET0 Register Contents (2/2)

Bit Position	Bit Name	Description
14 to 12	ARPROT[2:0]	Set the protection type in a transition from PCIe to AXI. These bits indicate whether the transaction protection level is “normal”, “privilege”, or “secure”, and whether the transaction is command access or data access. [2] 1b: Command access 0b: Data access [1] 1b: Non-secure access 0b: Secure access [0] 1b: Privilege access 0b: Normal access
11 to 6	—	Reserved. These bits are read as 0b.
5, 4	ARLOCK	Lock type in a transition from PCIe to AXI. This signal provides information on the atomic nature of transfer. 00b: Normal access 01b: Exclusive access 10b: Lock access 11b: Reserved
3 to 0	ARCACHE	Cache type in a transition from PCIe to AXI. These bits specify “bufferable”, “cacheable”, “write-through”, “write-back”, “allocation” as the attribute of the transaction.

(29) Mode Set 1 Register (PCI_EP_MSET1)

This register sets AXI mode.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0318h

Initial Value: 0000_33F2h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AXI Max Issue Write				AXI Max Issue Read				AXI Master Max Burst				—	—	RAM Parity Enable	PCIe Request Order
Initial Value	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	RW	RW

Table 36.5-36 PCI_EP_MSET1 Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15 to 12	AXI Max Issue Write	Sets the allowable number of write requests to be issued by an AXI master. Set the range that the interconnect can accept. 0h: Allowable number: 1 1h: Allowable number: 2 … Fh: Allowable number: 16
11 to 8	AXI Max Issue Read	Sets the allowable number of read requests to be issued by an AXI master. Set the range that the interconnect can accept. 0h: Allowable number: 1 1h: Allowable number: 2 … Fh: Allowable number: 16
7 to 4	AXI Master Max Burst	Set the maximum burst length in AXI master operations.
3, 2	—	Reserved. These bits are read as 0b.
1	RAM Parity Enable	Enables or disables parity checking of the internal SRAM. The initial value is "enable" but is ignored for units not equipped with this function. 0b: Disable parity checking of the RAM. 1b: Enable parity checking of the RAM.
0	PCIe Request Order	The same AXI master issues read requests to PCIe without waiting for completion. Set 1b to strictly preserve the order of requests to the completer. 0b: Not waiting for completion. 1b: Waiting for completion.

(30) Mode Set 3 Register (PCI_EP_MSET3)

This register outputs the setting value as the ASPM L1 Idle Time bit.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0380h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	ASPM L1 Idle Time							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-37 PCI_EP_MSET3 Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	ASPM L1 Idle Time	Sets the idle time for AXI transactions that will be checked by the unit during the transition to ASPM L1. 8 bits are set by these bits, and FFh is added to the lower 8 bits to form the idle time cycles. One condition for a transition to ASPM L1 is to confirm its idle time. 00h: 256 [ACLK]. 01h: 512 [ACLK] … FFh: 65536 [ACLK]

(31) Debug Output 1 Register (PCI_EP_DBGOUT1)

This register is for debugging.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0384h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Debug															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Debug															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-38 PCI_EP_DBGOUT1 Register Contents

Bit Position	Bit Name	Description
31 to 0	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.

(32) Debug Output 2 Register (PCI_EP_DBGOUT2)

This register is for debugging.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0388h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Debug															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-39 PCI_EP_DBGOUT2 Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved
15 to 0	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.

(33) Debug Input 0 Register (PCI_EP_DBGIN0)

This register is for debugging.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0390h

Initial Value: xxxx_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	Debug			
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-40 PCI_EP_DBGIN0 Register Contents

Bit Position	Bit Name	Description
31 to 4	—	Reserved
3 to 0	Debug	This register is for use in debugging by Renesas. Do not use GPI[3:0]

(34) PCIe Core Mode Set 1 Register (PCI_EP_PCMSET1)

This register sets the operating mode of the PCI Express core.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0400h

Initial Value: 07D0_00F2h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	Debug		ASPM_L1_INTERVAL_TIME											
Initial Value	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	Debug		MODE_LINK_UPCONFIGURE_CAPABILITY_DISABLED	—	MODE_TXSWING	Debug	MODE_SELECTABLE_DEEMPHASIS	Debug				—	—	MODE_PORT	MODE_PORT_ENABLE_B
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0
R/W	R	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	R	R	RW	RW

Table 36.5-41 PCI_EP_PCMSET1 Register Contents (1/2)

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29, 28	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
27 to 16	ASPM_L1_INTERVAL_TIME	Sets the interval between ASM L1 requests. The PCIe base specification stipulates that ASML1 transition requests shall not be accepted continuously within 10 µs. To guard against this, set a timer value in this field. Make a setting such that the ACLK cycle x set value is at least 10 µs. Example: When ACLK = 100 MHz (10 ns) : 1000 (d) = 3E8 (h) = 0011_1110_1000b When ACLK = 200 MHz (5 ns) : 2000 (d) = 7D0 (h) = 0111_1101_0000b When ACLK = 250 MHz (4 ns) : 2500 (d) = 9C4 (h) = 1001_1100_0100b When ACLK = 300 MHz (3.3 ns): 3000 (d) = BB8 (h) = 1011_1011_1000b • In the case of ACLK for 400 MHz or more, set the timer value for (1/16) the number of clocks the lower 4 bits light-shifted (round up) for the setting value of the above specifications. Example: When ACLK = 500 MHz (2 ns) : 5000 (d) = 1388 (h) ⇒ 139 (h) = 0001_0011_1001b When ACLK = 533 MHz (1.8 ns): 5556 (d) = 15B4 (h) ⇒ 15C(h) = 0001_0101_1100b
15	—	Reserved. This bit is read as 0b.
14, 13	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
12	MODE_LINK_UPCONFIGURE_CAPABILITY_DISABLED	Sets the Link Upconfigure Capability bit for a Training Sequence Ordered-set (TS-OS). 0b: Link Upconfigure Capability bit = 1b 1b: Link Upconfigure Capability bit = 0b (Gen1 × 1) When connecting to a Gen1 PCIe device, link-up cannot be performed unless this bit is 0b. In that case, change the bit to 0b by F/W.
11	—	Reserved. This bit is read as 0b.

Table 36.5-41 PCI_EP_PCMSET1 Register Contents (2/2)

Bit Position	Bit Name	Description
10	MODE_TXSWING	Controls the amplitude of SerDes serial output. 0b: Full swing mode (initial value) 1b: Half swing mode
9	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
8	MODE_SELECTABLE_DEEMPHASIS	De-emphasis mode in endpoint mode Sets the de-emphasis value for operation at 5.0 GT/s as an endpoint. The initial value is that of the select_deemphasis variable stated in the PCIe Base Spec. 0b: −6 dB (initial value) 1b: −3.5 dB
7 to 4	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
3, 2	—	Reserved. These bits are read as 0b.
1	MODE_PORT	Device type setting register. In normal operation, use the external pin settings for EP/RC settings. 0b: Endpoint 1b: Root complex
0	MODE_PORT_ENABLE_B	PHY disable setting register. It is fixed to 0b during normal operation. 0b: Normal operation 1b: PHY OFF

(35) PCIe Core Control 1 Register (PCI_EP_PCCTRL1)

This register controls power management and LTSSM (Link Training Sequence State Machine) state transitions.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0404h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BLB_RELAX_ORDERING_EN	—	—	—	Debug	—	UI_ENTER_L1S	Debug					UI_ENTER_TXL0S
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	RW	R	R	R	RW	R	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	MODE_QUIESCE_GUARANTEE	UI_ENTER_TXMODE_SRIS	MODE_EQ_AUTONOMOUS	MODE_EQ_PHASE23_ENABLE	MODE_RESET_EIEOS_INTERVALL0S	—	—	—	—	Debug			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	RW	RW	RW	RW	RW	R	R	R	R	RW	RW	RW	RW

Table 36.5-42 PCI_EP_PCCTRL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 29	—	Reserved. These bits are read as 0b.
28	BLB_RELAX_ORDERING_EN	Controls the transmission of read-only bits of a request. 0b: Transmits read-only bits of a request TLP set to 0b (initial value). 1b: Transmits read-only bits of a request TLP set to 1b.
27 to 25	—	Reserved. These bits are read as 0b.
24	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
23	—	Reserved. This bit is read as 0b.
22	UI_ENTER_L1S	Enable transition to the L1 substate. 0b: Disable transition to the L1 substate (initial value). 1b: Enable transition to the L1 substate (setting prohibited).
21 to 17	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
16	UI_ENTER_TXL0S	TxL0s transition control 0b: A transition to ASPM L0s is not initiated (initial value). 1b: A transition to ASPM L0s is initiated when the internal conditions are met.
15 to 13	—	Reserved. These bits are read as 0b.
12	MODE_QUIESCE_GUARANTEE	The Symbol6 bit 6 Quiesce Guarantee control bit of TS2OS 0b: Set TS2OS to 0b (initial value). 1b: Set TS2OS to 1b.
11	UI_ENTER_TXMODE_SRIS	Sets the clock tolerance compensation. 0b: SRNS (initial value) 1b: SRIS (not supported)
10	MODE_EQ_AUTONOMOUS	Reserved
9	MODE_EQ_PHASE23_ENABLE	Reserved
8	MODE_RESET_EIEOS_INTERVALL0S	Reserved

Table 36.5-42 PCI_EP_PCCTRL1 Register Contents (2/2)

Bit Position	Bit Name	Description
7 to 4	—	Reserved. These bits are read as 0b.
3 to 0	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.

(36) PCIe Core Status 1 Register (PCI_EP_PCSTAT1)

This register controls power management and LTSSM (Link Training Sequence State Machine) state transitions.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0408h

Initial Value: 0x0x_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	TURN_OFF_EVENT_ACK	TURN_OFF_EVENT	Debug		—	Debug			—	—	bme_down	Debug
Initial Value	0	0	0	0	x	0	0	0	0	0	0	0	0	0	x	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	LTSSM_STATE							PMU_LINKSTATE				—	Debug	STATE_VC0_NEGOTIATION_PENDING	DL_Down Status
Initial Value	0	x	x	x	x	x	x	x	x	x	x	x	0	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-43 PCI_EP_PCSTAT1 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b.
27	TURN_OFF_EVENT_ACK	Monitors the TURN_OFF_EVENT_ACK input signal.
26	TURN_OFF_EVENT	Monitors the TURN_OFF_EVENT output signal.
25, 24	Debug	This register is for use in debugging by Renesas.
23	—	Reserved. This bit is read as 0b.
22 to 20	Debug	This register is for use in debugging by Renesas.
19, 18	—	Reserved. These bits are read as 0b.
17	bme_down	Indicates that the PCIe core transmission section cannot be used.
16	Debug	This register is for use in debugging by Renesas.
15	—	Reserved. This bit is read as 0b.
14 to 8	LTSSM_STATE	Indicates the states of the Link Training and Status State Machine in the link of the PCIe core. The following state is indicated by the upper 5 bits [14:10]. 000_xxb: Detect 001_xxb: Polling 010_xxb: Config 011_00b: Lo 011_01b: L1 011_1xb: L2 100_xxb: Recovery 101_xxb: Disable 110_xxb: Loopback
7 to 4	PMU_LINKSTATE	Monitors the L-state of the power management control section. 0100b: L1 state 1000b: L2 state
3	—	Reserved. This bit is read as 0b.
2	Debug	This register is for use in debugging by Renesas.

Table 36.5-43 PCI_EP_PCSTAT1 Register Contents (2/2)

Bit Position	Bit Name	Description
1	STATE_VC0_NEGOTIATION_PENDING	Monitors flow control initialization operation. When this bit is 1b, transactions should not be started by AXI. Confirm that this bit is 0b and DL_Down Status (bit [0]) is 0b. 0b: Indicates the completion of flow control initialization. 1b: Indicates that flow control initialization is not completed.
0	DL_down status	Indicates whether the PCIe core is in the DL_Down or DL_Up state. 0b: DL_Up Status 1b: DL_Down Status

(37) PCIe Core Control 2 Register (PCI_EP_PCCTRL2)

This register controls the link speed/width change in the PCI Express core.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0410h

Initial Value: 003E_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	UI_LINK_WIDTH_CHANGE_ENABLE[7:0]								MODE_NODEEMPHASIS[1:0]		MODE_PRESET_ENABLE[4:0]					UI_LINK_WIDTH_CHANGE_REQ
Initial Value	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	UI_LINK_SPEED_CHANGE		—	—	—	UI_LINK_CHANGE_AUTONOMOUS	—	—	—	UI_LINK_SPEED_CHANGE_REQ
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	R	R	R	RW	R	R	R	RW

Table 36.5-44 PCI_EP_PCCTRL2 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 24	UI_LINK_WIDTH_CHANGE_ENABLE [7:0]	Link width setting to be changed. When UI_LINK_WIDTH_CHANGE_REQ is asserted to request a link width change, to 1b to change to the corresponding lane. The LSB (bit [24]) corresponds to lane 0 and bit [25] corresponds to lane 1. Bits 31 to 25 are not supported.
23, 22	MODE_NODEEMPHASIS[1:0]	No de-emphasis mode setting pin during Gen1/Gen2 operation. [0]: During Gen1 operation 0b: Normal operation mode (initial value) 1b: No de-emphasis mode [1]: During Gen2 operation 0b: Normal operation mode (initial value) 1b: No de-emphasis mode
21 to 17	MODE_PRESET_ENABLE[4:0]	Reserved
16	UI_LINK_WIDTH_CHANGE_REQ	Link width change request control Set this bit to 1b to request that the link width be changed to the configuration of the bits [31:24] UI_LINK_WIDTHCHANGE_ENABLE field. Asserting during the L0 state transitions the recovery state to the configuration state, and negotiation is performed with the other-party device. After confirming assertion of UI_LINK_WIDTH_CHANGE_DONE of PCIe Core Status 2 Register (address: <PCI_S0_REG_base> + 0414h) bit [29], set 1b0.
15 to 10	—	Reserved. These bits are read as 0b.
9, 8	UI_LINK_SPEED_CHANGE	Link speed setting Set the link speed. 00b: 2.5 GT/s 01b: 5.0 GT/s 10b: 8.0 GT/s (setting prohibited) 11b: 16.0 GT/s (setting prohibited)
7 to 5	—	Reserved. These bits are read as 0b.
4	UI_LINK_CHANGE_AUTONOMOUS	Reason for link width/speed change 0b: Reliability reason (Changes for reliability. Direction of decreasing bandwidth) 1b: Autonomous reason (Intentional change)

Table 36.5-44 PCI_EP_PCCTRL2 Register Contents (2/2)

Bit Position	Bit Name	Description
3 to 1	—	Reserved. These bits are read as 0b.
0	UI_LINK_SPEED_CHANGE_REQ	Link speed change request control Issues a request to change Link Speed to the speed set in the bit [8] UI_LINK_SPEED_CHANGE field. Asserting during the L0 state transitions the recovery state to the configuration state, and negotiation is performed with the other-party device. After confirming assertion of UI_LINK_SPEED_CHANGE_DONE of PCIe Core Status 2 Register (address: <PCI_S0_REG_base> + 0414h) bit [28], set 1b0.

(38) PCIe Core Status 2 Register (PCI_EP_PCSTAT2)

This register indicates the status of the link speed/width change in the PCI Express core.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0414h

Initial Value: xxxx_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	UI_LINK_WIDTH_CHANGE_DONE	UI_LINK_SPEED_CHANGE_DONE	—	—	—	STATE_UPCONFIGURE_CAPABLE	—	STATE_NEGOTIATED_LANE_END			—	STATE_NEGOTIATED_LANE_START		
Initial Value	0	0	x	x	0	0	0	x	0	x	x	x	0	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	STATE_RECEIVER_DETECTED[7:0]								STATE_DATA_RATE_IDENTIFIER_RECEIVED[7:0]							
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	0	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-45 PCI_EP_PCSTAT2 Register Contents (1/2)

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29	UI_LINK_WIDTH_CHANGE_DONE	Indicates the completion of link width change operation. Notifies the completion (1b) of a width change requested by setting UI_LINK_WIDTH_CHANGE_REQ of PCIe Core Control 2 Register (address: <PCI_S0_REG_base> + 0410h) bit [16]. It is set 0b by setting UI_LINK_WIDTH_CHANGE_REQ to 0b.
28	UI_LINK_SPEED_CHANGE_DONE	Notifies the completion (1b) of a speed change requested by setting UI_LINK_SPEED_CHANGE_REQ of PCIe Core Control 2 Register (address: <PCI_S0_REG_base> + 0410h) bit [0]. It is set 0b by setting UI_LINK_SPEED_CHANGE_REQ to 0b.
27 to 25	—	Reserved. These bits are read as 0b.
24	STATE_UPCONFIGURE_CAPABLE	Indicates the Upconfigure Capable bit of the other-party device. Indicates that the other-party device supports changes in the direction to increase the link width. If this bit is 0b, after changing the link width, the original link width cannot be restored.
23	—	Reserved. This bit is read as 0b.
22 to 20	STATE_NEGOTIATED_LANE_END	During n lanes operation, indicates the position of a lane number (n = 1) after link negotiation with the other-party device. Used to check the current state of the operating lane before changing the link width. 000b: Lane 0 is lane number (n - 1). 001b: Lane 1 is lane number (n - 1). Others: Reserved
19	—	Reserved. This bit is read as 0b.
18 to 16	STATE_NEGOTIATED_LANE_START	During n lanes operation, indicates the position of lane number 0 after link negotiation with the other-party device. Used to check the current state of the operating lane before changing the link width. 000b: Lane 0 is lane number 0. 001b: Lane 1 is lane number 0. Others: Reserved

Table 36.5-45 PCI_EP_PCSTAT2 Register Contents (2/2)

Bit Position	Bit Name	Description
15 to 8	STATE_RECEIVER_DETECTED[7:0]	Indicates the connection status with the other-party device. The result of receiver detection is displayed. [0]: An other-party device was detected on lane 0. [1]: An other-party device was detected on lane 1. (Only x2 case) [2] to [7]: Reserved
7 to 0	STATE_DATA_RATE_IDENTIFIER_RECEIVED[7:0]	Indicates the link speed supported by the other-party device. Indicates the data rate identifier field of TS-OS received from the other-party device. Bit 0: Reserved Bit 1: 2.5 GT/s data rate supported. Must be set to 1b. Bit 2: 5.0 GT/s data rate supported Bit 3: 8.0 GT/s data rate supported Bit 4: 16.0 GT/s data rate supported

(39) PCIe Core Status 5 Register (PCI_EP_PCSTAT5)

This register indicates the status in the PCI Express core.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 042Ch

Initial Value: 0000_0x00h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	suspend_bme								D3_EVENT							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D3_EVENT_ACK								ORT_TRANSACTION_PENDING							
Initial Value	0	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-46 PCI_EP_PCSTAT5 Register Contents

Bit Position	Bit Name	Description
31 to 24	suspend_bme	Indicates the state in which the use of the PCIe core transmitter for each function should be suspended. Reserved (fixed to 0) other than the lower 2 bits
23 to 16	D3_EVENT	Monitors the D3_EVENT signal for each function. Reserved (fixed to 0) other than the lower 2 bits
15 to 8	D3_EVENT_ACK	Monitors the D3_EVENT_ACK signal for each function. Reserved (fixed to 0) other than the lower 2 bits
7 to 0	ORT_TRANSACTION_PENDING	Indicates the presence of an outstanding request (not all completion responses corresponding to non-posted requests from the AXI side have not been received). Check this bit before requesting or enabling a transition to TxL0s/L1/L2 to ensure that no outstanding requests are present. 0b: No outstanding requests are present. 1b: Outstanding requests are present.

(40) DMA Interrupt Vector 0 Register (PCI_EP_DMAINTVEC0)

This register specifies the interrupt vectors for interrupt notification from AXI to PCIe (MSI) during DMA transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 04D0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	DMA_CH3_MSI_EN	DMA_CH3_vec					—	—	DMA_CH2_MSI_EN	DMA_CH2_vec				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DMA_CH1_MSI_EN	DMA_CH1_vec					—	—	DMA_CH0_MSI_EN	DMA_CH0_vec				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 36.5-47 PCI_EP_DMAINTVEC0 Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29	DMA_CH3_MSI_EN	DMA Ch3 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
28 to 24	DMA_CH3_vec	Specifies MSI interrupt vector transmitted by DMAC ch. 3.
23, 22	—	Reserved. These bits are read as 0b.
21	DMA_CH2_MSI_EN	DMA Ch2 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
20 to 16	DMA_CH2_vec	Specifies MSI interrupt vector transmitted by DMAC ch. 2.
15, 14	—	Reserved. These bits are read as 0b.
13	DMA_CH1_MSI_EN	DMA Ch1 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
12 to 8	DMA_CH1_vec	Specifies MSI interrupt vector transmitted by DMAC ch. 1.
7, 6	—	Reserved. These bits are read as 0b.
5	DMA_CH0_MSI_EN	DMA Ch0 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
4 to 0	DMA_CH0_vec	Specifies the MSI interrupt vector transmitted by DMAC ch. 0.

(41) DMA Interrupt Vector 1 Register (PCI_EP_DMAINTVEC1)

This register specifies interrupt vectors for interrupt notification from AXI to PCIe (MSI) during DMA transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 04D4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	DMA_CH7_MSI_EN	DMA_CH7_vec					—	—	DMA_CH6_MSI_EN	DMA_CH6_vec				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DMA_CH5_MSI_EN	DMA_CH5_vec					—	—	DMA_CH4_MSI_EN	DMA_CH4_vec				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 36.5-48 PCI_EP_DMAINTVEC1 Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29	DMA_CH7_MSI_EN	DMA Ch7 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
28 to 24	DMA_CH7_vec	Specifies MSI interrupt vector transmitted by DMAC ch. 7.
23, 22	—	Reserved. These bits are read as 0b.
21	DMA_CH6_MSI_EN	DMA Ch6 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
20 to 16	DMA_CH6_vec	Specifies MSI interrupt vector transmitted by DMAC ch. 6.
15, 14	—	Reserved. These bits are read as 0b.
13	DMA_CH5_MSI_EN	DMA Ch5 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
12 to 8	DMA_CH5_vec	Specifies MSI interrupt vector transmitted by DMAC ch. 5.
7, 6	—	Reserved. These bits are read as 0b.
5	DMA_CH4_MSI_EN	DMA Ch4 MSI Enable 0b: MSI is not used (DMA interrupt notification by the DMA_INT pin). 1b: MSI is used. For the RC function, MSI transmission is prohibited, so fix this bit to 0b.
4 to 0	DMA_CH4_vec	Specifies MSI interrupt vector transmitted by DMAC ch. 4.

(42) DMAC Control Register (PCI_EP_DMACTRL)

This register sets the maximum size of read requests which can be issued to the PCIe Core as a DMAC function. Use the initial setting (128-byte). This setting is common to all DMA channels.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0800h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	D_PMRS		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 36.5-49 PCI_EP_DMACTRL Register Contents

Bit Position	Bit Name	Description
31 to 3	—	Reserved. These bits are read as 0b.
2 to 0	D_PMRS	DMAC PCIe Max Read Request Size Sets the maximum size of read requests to be issued to PCIe by the DMAC. 000b: 128 bytes (initial value) 001b: 256 bytes 010b: 512 bytes (not supported) 011b: 1024 bytes (not supported) 100b: 2048 bytes (not supported) 101b: 4096 bytes (not supported) Others: Reserved (setting prohibited)

(43) DMAC Interrupt Enable Register (PCI_EP_DMAINTE)

This register enables interrupts from the individual DMA channels.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0808h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CH7_ERR_EN	CH7_QUE_EMP_EN	CH7_STOP_EN	CH7_END_EN	CH6_ERR_EN	CH6_QUE_EMP_EN	CH6_STOP_EN	CH6_END_EN	CH5_ERR_EN	CH5_QUE_EMP_EN	CH5_STOP_EN	CH5_END_EN	CH4_ERR_EN	CH4_QUE_EMP_EN	CH4_STOP_EN	CH4_END_EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH3_ERR_EN	CH3_QUE_EMP_EN	CH3_STOP_EN	CH3_END_EN	CH2_ERR_EN	CH2_QUE_EMP_EN	CH2_STOP_EN	CH2_END_EN	CH1_ERR_EN	CH1_QUE_EMP_EN	CH1_STOP_EN	CH1_END_EN	CH0_ERR_EN	CH0_QUE_EMP_EN	CH0_STOP_EN	CH0_END_EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-50 PCI_EP_DMAINTE Register Contents (1/3)

Bit Position	Bit Name	Description
31	CH7_ERR_EN	CH7 Error interrupt Enable 1b: Enabled 0b: Disabled
30	CH7_QUE_EMP_EN	CH7 Que Empty interrupt Enable 1b: Enabled 0b: Disabled
29	CH7_STOP_EN	CH7 Stop interrupt Enable 1b: Enabled 0b: Disabled
28	CH7_END_EN	CH7 Completion interrupt Enable 1b: Enabled 0b: Disabled
27	CH6_ERR_EN	CH6 Error interrupt Enable 1b: Enabled 0b: Disabled
26	CH6_QUE_EMP_EN	CH6 Que Empty interrupt Enable 1b: Enabled 0b: Disabled
25	CH6_STOP_EN	CH6 Stop interrupt Enable 1b: Enabled 0b: Disabled
24	CH6_END_EN	CH6 Completion interrupt Enable 1b: Enabled 0b: Disabled
23	CH5_ERR_EN	CH5 Error interrupt Enable 1b: Enabled 0b: Disabled
22	CH5_QUE_EMP_EN	CH5 Que Empty interrupt Enable 1b: Enabled 0b: Disabled

Table 36.5-50 PCI_EP_DMAINTE Register Contents (2/3)

Bit Position	Bit Name	Description
21	CH5_STOP_EN	CH5 Stop Interrupt Enable 1b: Enabled 0b: Disabled
20	CH5_END_EN	CH5 Completion Interrupt Enable 1b: Enabled 0b: Disabled
19	CH4_ERR_EN	CH4 Error Interrupt Enable 1b: Enabled 0b: Disabled
18	CH4_QUE_EMP_EN	CH4 Que Empty Interrupt Enable 1b: Enabled 0b: Disabled
17	CH4_STOP_EN	CH4 Stop Interrupt Enable 1b: Enabled 0b: Disabled
16	CH4_END_EN	CH4 Completion Interrupt Enable 1b: Enabled 0b: Disabled
15	CH3_ERR_EN	CH3 Error Interrupt Enable 1b: Enabled 0b: Disabled
14	CH3_QUE_EMP_EN	CH3 Que Empty Interrupt Enable 1b: Enabled 0b: Disabled
13	CH3_STOP_EN	CH3 Stop Interrupt Enable 1b: Enabled 0b: Disabled
12	CH3_END_EN	CH3 Completion Interrupt Enable 1b: Enabled 0b: Disabled
11	CH2_ERR_EN	CH2 Error Interrupt Enable 1b: Enabled 0b: Disabled
10	CH2_QUE_EMP_EN	CH2 Que Empty Interrupt Enable 1b: Enabled 0b: Disabled
9	CH2_STOP_EN	CH2 Stop Interrupt Enable 1b: Enabled 0b: Disabled
8	CH2_END_EN	CH2 Completion Interrupt Enable 1b: Enabled 0b: Disabled
7	CH1_ERR_EN	CH1 Error Interrupt Enable 1b: Enabled 0b: Disabled
6	CH1_QUE_EMP_EN	CH1 Que Empty Interrupt Enable 1b: Enabled 0b: Disabled
5	CH1_STOP_EN	CH1 Stop Interrupt Enable 1b: Enabled 0b: Disabled

Table 36.5-50 PCI_EP_DMAINTE Register Contents (3/3)

Bit Position	Bit Name	Description
4	CH1_END_EN	CH1 Completion Interrupt Enable 1b: Enabled 0b: Disabled
3	CH0_ERR_EN	CH0 Error Interrupt Enable 1b: Enabled 0b: Disabled
2	CH0_QUE_EMP_EN	CH0 Que Empty Interrupt Enable 1b: Enabled 0b: Disabled
1	CH0_STOP_EN	CH0 Stop Interrupt Enable 1b: Enabled 0b: Disabled
0	CH0_END_EN	CH0 Completion Interrupt Enable 1b: Enabled 0b: Disabled

(44) DMAC Interrupt Status Register (PCI_EP_DMAINTS)

This register indicates the state of interrupts from the individual DMA channels.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 080Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CH7_ERR	CH7_QUE_EMP	CH7_STOP	CH7_END	CH6_ERR	CH6_QUE_EMP	CH6_STOP	CH6_END	CH5_ERR	CH5_QUE_EMP	CH5_STOP	CH5_END	CH4_ERR	CH4_QUE_EMP	CH4_STOP	CH4_END
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH3_ERR	CH3_QUE_EMP	CH3_STOP	CH3_END	CH2_ERR	CH2_QUE_EMP	CH2_STOP	CH2_END	CH1_ERR	CH1_QUE_EMP	CH1_STOP	CH1_END	CH0_ERR	CH0_QUE_EMP	CH0_STOP	CH0_END
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1	RW1

Table 36.5-51 PCI_EP_DMAINTS Register Contents (1/3)

Bit Position	Bit Name	Description
31	CH7_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
30	CH7_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
29	CH7_STOP	Set if DMAC suspended on the way. DMAC suspend in the following case. RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
28	CH7_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1b It is cleared by writing 1b. Writing 0b has no effect.
27	CH6_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
26	CH6_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
25	CH6_STOP	Set when the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
24	CH6_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following state. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1b It is cleared by writing 1b. Writing 0b has no effect.
23	CH5_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.

Table 36.5-51 PCI_EP_DMAINTS Register Contents (2/3)

Bit Position	Bit Name	Description
22	CH5_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
21	CH5_STOP	Set the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
20	CH5_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1b It is cleared by writing 1b. Writing 0b has no effect.
19	CH4_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
18	CH4_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
17	CH4_STOP	Set the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
16	CH4_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1b It is cleared by writing 1b. Writing 0b has no effect.
15	CH3_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
14	CH3_QUE_EMP	Set a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
13	CH3_STOP	Set when the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
12	CH3_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1b It is cleared by writing 1b. Writing 0b has no effect.
11	CH2_ERR	Sets when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
10	CH2_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
9	CH2_STOP	Set when the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.

Table 36.5-51 PCI_EP_DMAINTS Register Contents (3/3)

Bit Position	Bit Name	Description
8	CH2_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1b It is cleared by writing 1b. Writing 0b has no effect.
7	CH1_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
6	CH1_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
5	CH1_STOP	Set when the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
4	CH1_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1b It is cleared by writing 1b. Writing 0b has no effect.
3	CH0_ERR	Set when an error has occurred during DMA transfer. It is cleared by writing 1b. Writing 0b has no effect.
2	CH0_QUE_EMP	Set when a list is removed from the descriptor queue (and is moved to become the descriptor list for execution) and this leads to the queue being empty. It is cleared by writing 1b. Writing 0b has no effect.
1	CH0_STOP	Set when the DMAC is stopped while in progress. The DMAC is stopped in the following case: RDMA_EN or QUE_EN was cleared to 0b by software during DMA transfer and processing for the request being issued was ended. It is cleared by writing 1b. Writing 0b has no effect.
0	CH0_END	Set when transfer through the DMAC is completed normally. Successful completion indicates the following states. • Transfer of the amount of data indicated by DMA_SIZE is completed. • End of the descriptor list for which the EI field is set to 1b It is cleared by writing 1b. Writing 0b has no effect.

(45) DMA Channel Control Register m (PCI_EP_DMACHCTLm) (m = 0 to 7)

This register sets the control method for each DMA channel. Set either register type or descriptor type, not both.

- Setting QUE_EN = 1b and QUE_CLR = 1b is prohibited during register-type DMA transfer (TDMA_EN = 1b).
- Setting RDMA_EN = 1b is prohibited during descriptor-type DMA transfer (QUE_EN = 1b).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0900h (m = 0)
<PCI_S0_REG_base> + 0980h (m = 1)
<PCI_S0_REG_base> + 0A00h (m = 2)
<PCI_S0_REG_base> + 0A80h (m = 3)
<PCI_S0_REG_base> + 0B00h (m = 4)
<PCI_S0_REG_base> + 0B80h (m = 5)
<PCI_S0_REG_base> + 0C00h (m = 6)
<PCI_S0_REG_base> + 0C80h (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	QUE_CLR	—	—	—	—	—	—	QUE_EN	RDMA_EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	R	R	R	R	R	R	RW	RW

Table 36.5-52 PCI_EP_DMACHCTLm Register Contents

Bit Position	Bit Name	Description
31 to 9	—	Reserved. These bits are read as 0b.
8	QUE_CLR	Queue Clear The queue is cleared by writing 1b. The descriptor lists registered in the queue (those waiting for execution and the one currently being executed) are all cleared. Do not clear them during DMA execution. The value read is always 0b. Writing 1b is prohibited when QUE_EN is set.
7 to 2	—	Reserved. These bits are read as 0b.
1	QUE_EN	Queue Enable Writing 1b to this bit enables the start of processing of descriptor lists registered in the descriptor queue and of DMA transfer (descriptor type). The bit is automatically cleared to 0b when DMA transfer is stopped (normally or abnormally). DMA transfer can also be stopped by writing 0b. However, it is only stopped after the completion of the request (from PCIe or AXI) currently being executed.
0	RDMA_EN	Register method DMA transfer Enable Writing 1b to this bit starts DMA transfer (register type) and transfer specified in the RDMA_SIZE bits proceeds. It is automatically cleared to 0b when DMA has ended in response to the completion of DMA transfer or the detection of an error. DMA transfer can also be stopped by writing 0b. However, it is only stopped after the completion of the request (from PCIe or AXI) currently being executed. 1b: Register-type DMA transfer is started. 0b: Register-type DMA transfer is stopped.

(46) QUE Entry (Lower) Register m (PCI_EP_QUEEmL) (m = 0 to 7)

This register sets the descriptor queue list. This setting value is registered as the DSA (DMA descriptor start address) of the queue list.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0908h (m = 0)
<PCI_S0_REG_base> + 0988h (m = 1)
<PCI_S0_REG_base> + 0A08h (m = 2)
<PCI_S0_REG_base> + 0A88h (m = 3)
<PCI_S0_REG_base> + 0B08h (m = 4)
<PCI_S0_REG_base> + 0B88h (m = 5)
<PCI_S0_REG_base> + 0C08h (m = 6)
<PCI_S0_REG_base> + 0C88h (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DSA[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSA[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R

Table 36.5-53 PCI_EP_QUEEmL Register Contents

Bit Position	Bit Name	Description
31 to 0	QUE_ENTRY (DSA[31:00])	Register a descriptor list queue. This area becomes the DSA. Set the address where the first descriptor is stored. Since the setting is for 8-byte alignment, the lower 3 bits are fixed to 0b.

Note: When these bits are read, any of the following will be read depending on the state of DMA transfer.
DMA transfer is proceeding: The descriptor list being executed
DMA transfer is stopped (when QUE_EN has been automatically cleared): The last list to have been executed
DMA transfer is stopped (when QUE_EN has been cleared by software): The list that has been stopped (was being executed).

(47) QUE Entry (Upper) Register m (PCI_EP_QUEE0U) (m = 0 to 7)

This register sets the descriptor queue list. This setting value is registered as the EI (end interrupt), LS (list stop), and the label of the queue list. Register to the queue by writing to [31:24].

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 090Ch (m = 0)
<PCI_S0_REG_base> + 098Ch (m = 1)
<PCI_S0_REG_base> + 0A0Ch (m = 2)
<PCI_S0_REG_base> + 0A8Ch (m = 3)
<PCI_S0_REG_base> + 0B0Ch (m = 4)
<PCI_S0_REG_base> + 0B8Ch (m = 5)
<PCI_S0_REG_base> + 0C0Ch (m = 6)
<PCI_S0_REG_base> + 0C8Ch (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	QUE_Registration						QUE_ENTRY (EI)	QUE_ENTRY (LS)	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	QUE_ENTRY (LABEL)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-54 PCI_EP_QUEE0U Register Contents

Bit Position	Bit Name	Description
31 to 26	QUE_Registration	Register to the queue by writing to [31:24]. The value read is always 0000_00b.
25	QUE_ENTRY (EI)	Specify whether to notify an interrupt (interrupt status CHx_END) when the processing of the descriptor list is completed. 1b: Notify the interrupt. 0b: Notify no interrupt.
24	QUE_ENTRY (LS)	Specify whether to stop DMA transfer when the processing of the descriptor list is completed. 1b: Stop DMA transfer. 0b: Does not stop DMA transfer.
23 to 16	—	Reserved. These bits are read as 0b.
15 to 0	QUE_ENTRY (LABEL)	This field represents the label of the list and there are no special rules for the setting procedures. The value can be set as desired.

Note: When these bits are read, any of the following will be read depending on the state of DMA transfer.
DMA transfer is proceeding: The descriptor list being executed
DMA transfer is stopped (when QUE_EN has been automatically cleared): The last list to have been executed
DMA transfer is stopped (when QUE_EN has been cleared by software): The list that has been stopped (was being executed).

(48) DMA Descriptor Control (Descriptor 00h) Register m (PCI_EP_DMADPCTLm) (m = 0 to 7)

This register indicates the field value at offset 00h in the descriptor table. Only effective when the descriptor-type DMA transfer is selected (the value read has no meaning in the case of register-type transfer).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0920h (m = 0)
<PCI_S0_REG_base> + 09A0h (m = 1)
<PCI_S0_REG_base> + 0A20h (m = 2)
<PCI_S0_REG_base> + 0AA0h (m = 3)
<PCI_S0_REG_base> + 0B20h (m = 4)
<PCI_S0_REG_base> + 0BA0h (m = 5)
<PCI_S0_REG_base> + 0C20h (m = 6)
<PCI_S0_REG_base> + 0CA0h (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DSCFM				—	WBD	LE	LV	D	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	STS															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-55 PCI_EP_DMADPCTLm Register Contents

Bit Position	Bit Name	Description
31 to 28	DSCFM	Indicates the DSCFM field value in the descriptor table being executed.
27	—	Reserved. This bit is read as 0b.
26	WBD	Indicates the WBD field value in the descriptor table being executed.
25	LE	Indicates the LE field value in the descriptor table being executed.
24	LV	Indicates the LV field value in the descriptor table being executed.
23	D	Indicates the D field value in the descriptor table being executed.
22 to 16	—	Reserved. These bits are read as 0b.
15 to 0	STS	Indicates the STS field value in the descriptor table being executed.

(49) DMA Source Address (Descriptor 04h) Register m (PCI_EP_DMASRCAm) (m = 0 to 7)

This register sets the start address of the source for DMA transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0924h (m = 0)
<PCI_S0_REG_base> + 09A4h (m = 1)
<PCI_S0_REG_base> + 0A24h (m = 2)
<PCI_S0_REG_base> + 0AA4h (m = 3)
<PCI_S0_REG_base> + 0B24h (m = 4)
<PCI_S0_REG_base> + 0BA4h (m = 5)
<PCI_S0_REG_base> + 0C24h (m = 6)
<PCI_S0_REG_base> + 0CA4h (m = 7)

Initial Value: 0000_0000h

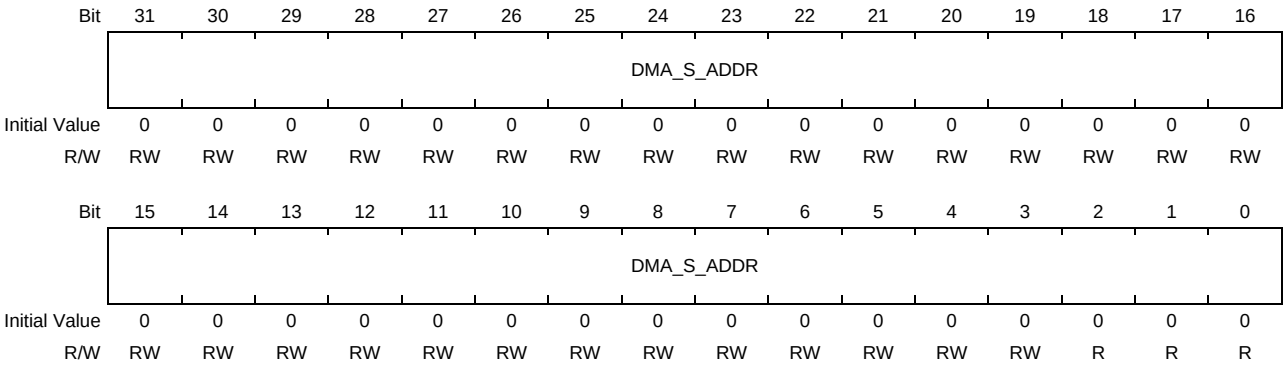


Table 36.5-56 PCI_EP_DMASRCAm Register Contents

Bit Position	Bit Name	Description
31 to 0	DMA_S_ADDR	Sets the start address of the source for DMA transfer. Since the setting is for 8-byte alignment, the lower 3 bits are fixed to 0b.

Note: If the source address is for the PCIe space (DIR = 0b), the PCIe request address is set in combination with the DMA PCIe upper address (descriptor 10h). When descriptor-type DMA transfer is to proceed, writing to these bits is prohibited and the value read indicates the value of the SA field in the descriptor table being executed.

(50) DMA Destination Address (Descriptor 08h) Register m (PCI_EP_DMADSTAm) (m = 0 to 7)

This register sets the start address of the destination for DMA transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0928h (m = 0)
<PCI_S0_REG_base> + 09A8h (m = 1)
<PCI_S0_REG_base> + 0A28h (m = 2)
<PCI_S0_REG_base> + 0AA8h (m = 3)
<PCI_S0_REG_base> + 0B28h (m = 4)
<PCI_S0_REG_base> + 0BA8h (m = 5)
<PCI_S0_REG_base> + 0C28h (m = 6)
<PCI_S0_REG_base> + 0CA8h (m = 7)

Initial Value: 0000_0000h

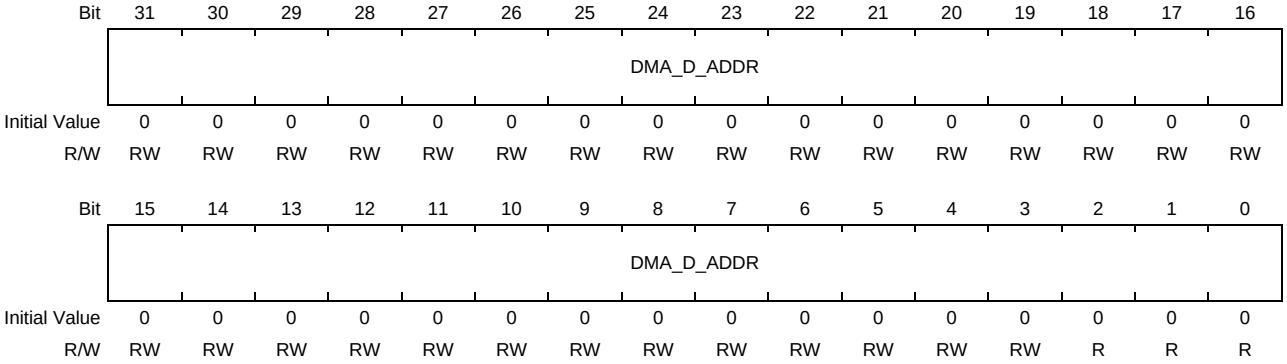


Table 36.5-57 PCI_EP_DMADSTAm Register Contents

Bit Position	Bit Name	Description
31 to 0	DMA_D_ADDR	Sets the start address of the destination for DMA transfer. Since the setting is for 8-byte alignment, the lower 3 bits are fixed to 0b.

Note: If the destination address is for the PCIe space (DIR = 0b), the PCIe request address is set in combination with the DMA PCIe upper address (descriptor 10h). When descriptor-type DMA transfer is to proceed, writing to these bits is prohibited and the value read indicates the value of the DA field in the descriptor table being executed.

(51) DMA Size (Descriptor 0Ch) Register m (PCI_EP_DMASIZEm) (m = 0 to 7)

This register sets the number of bytes for DMA transfer. Reflects the field at offset 0Ch in the descriptor table.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 092Ch (m = 0)
<PCI_S0_REG_base> + 09ACh (m = 1)
<PCI_S0_REG_base> + 0A2Ch (m = 2)
<PCI_S0_REG_base> + 0AACh (m = 3)
<PCI_S0_REG_base> + 0B2Ch (m = 4)
<PCI_S0_REG_base> + 0BACh (m = 5)
<PCI_S0_REG_base> + 0C2Ch (m = 6)
<PCI_S0_REG_base> + 0CACh (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DMA_SIZE															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA_SIZE															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R

Table 36.5-58 PCI_EP_DMASIZEm Register Contents

Bit Position	Bit Name	Description
31 to 0	DMA_SIZE	Sets the number of bytes for DMA transfer. Since the setting is for 8-byte alignment, the lower 3 bits are fixed to 0b.

Note: When descriptor-type DMA transfer is to proceed, writing to these bits is prohibited and the value read indicates the value of the SIZE field in the descriptor table being executed. The number of bytes for transfer when the setting is 0000_0000h is 1_0000_0000h.

(52) DMA PCIe Upper Address (Descriptor 10h) Register m (PCI_EP_DMAPCIEUAm) (m = 0 to 7)

This register sets the start address [63:32] for DMA transfer on the PCIe side.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0930h (m = 0)
<PCI_S0_REG_base> + 09B0h (m = 1)
<PCI_S0_REG_base> + 0A30h (m = 2)
<PCI_S0_REG_base> + 0AB0h (m = 3)
<PCI_S0_REG_base> + 0B30h (m = 4)
<PCI_S0_REG_base> + 0BB0h (m = 5)
<PCI_S0_REG_base> + 0C30h (m = 6)
<PCI_S0_REG_base> + 0CB0h (m = 7)

Initial Value: 0000_0000h

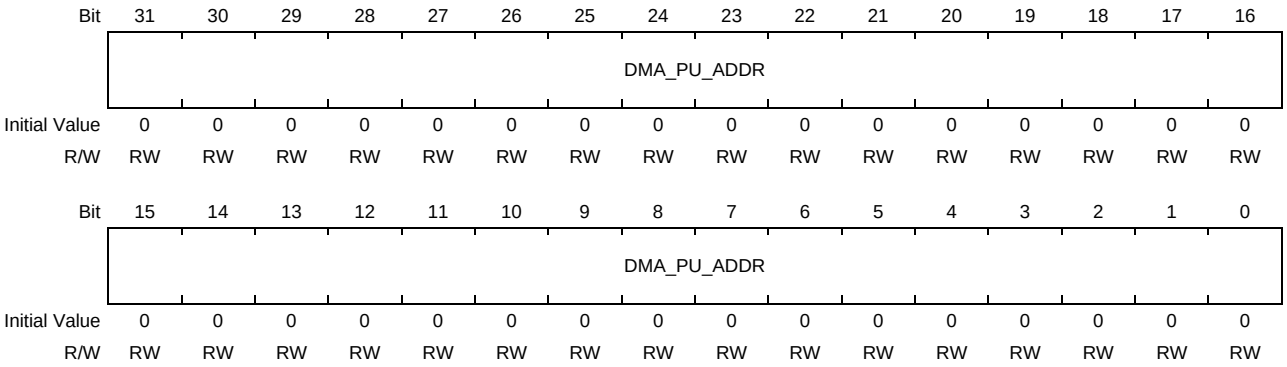


Table 36.5-59 PCI_EP_DMAPCIEUAm Register Contents

Bit Position	Bit Name	Description
31 to 0	DMA_PU_ADDR	Sets the start address [63:32] for DMA transfer on the PCIe side.

Note: When descriptor-type DMA transfer is to proceed, writing to these bits is prohibited and the value read indicates the value of the PUA field in the descriptor table being executed.

(53) DMA Transaction Control (Descriptor 14h) Register m (PCI_EP_DMATCTLm) (m = 0 to 7)

This register controls DMA transfer to the AXI side and PCIe side.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0934h (m = 0)
<PCI_S0_REG_base> + 09B4h (m = 1)
<PCI_S0_REG_base> + 0A34h (m = 2)
<PCI_S0_REG_base> + 0AB4h (m = 3)
<PCI_S0_REG_base> + 0B34h (m = 4)
<PCI_S0_REG_base> + 0BB4h (m = 5)
<PCI_S0_REG_base> + 0C34h (m = 6)
<PCI_S0_REG_base> + 0CB4h (m = 7)

Initial Value: 0000_0000h

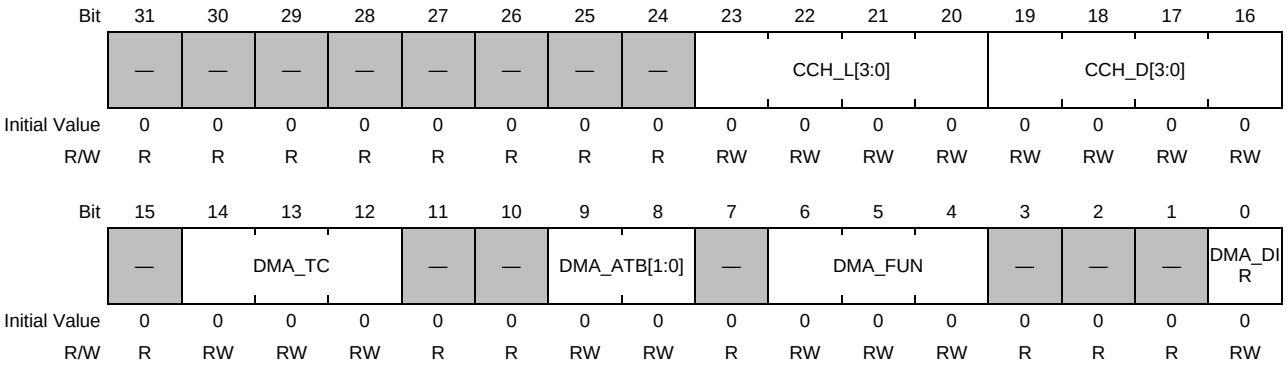


Table 36.5-60 PCI_EP_DMATCTLm Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b.
23 to 20	CCH_L[3:0]	Indicates the value of A*CACHE[3:0] issued to AXI. This setting is issued when an AXI request containing the last byte is issued in transfer indicated by SIZE. The recommended value is 0000b. [3] 1b: Write allocation enabled 0b: Write allocation disabled [2] 1b: Read allocation enabled 0b: Read allocation disabled [1] 1b: Cacheable 0b: Not cacheable [0] 1b: Bufferable 0b: Not bufferable
19 to 16	CCH_D[3:0]	Specifies the value of A*CACHE[3:0] issued to AXI. This setting is issued when an AXI request other than the output condition of CCH_L is issued. When DIR = 0b (PCIe → AXI), the recommended value is 0001b. When DIR = 1b (AXI → PCIe), the recommended value is 0000b. [3] 1b: Write assignable. 0b: No write assignment [2] 1b: Read assignable. 0b: No read assignment [1] 1b: Cacheable. 0b: Not Cacheable. [0] 1b: Bufferable. 0b: Not Bufferable
15	—	Reserved. This bit is read as 0b.
14 to 12	DMA_TC	The traffic class issued to PCIe. Indicates the traffic class value of the request issued to PCIe.
11, 10	—	Reserved. These bits are read as 0b.
9, 8	DMA_ATB[1:0]	The attribute issued to PCIe. Bit [1]: Relaxed Ordering (non-supported function: Fixed to 0b.) Bit [0]: No snoop (0b is recommended)
7	—	Reserved. This bit is read as 0b.
6 to 4	DMA_FUNC	Indicates the request function number issued to PCIe.
3 to1	—	Reserved. These bits are read as 0b.

Table 36.5-60 PCI_EP_DMATCTLm Register Contents (2/2)

Bit Position	Bit Name	Description
0	DMA_DIR	Sets the direction of DMA transfer. 1b: AXI → PCIe 0b: PCIe → AXI

Note: When descriptor-type DMA transfer is to proceed, writing to these bits is prohibited and the value read indicates the value of the CCH_L, CCH_D, TC, ATB, and DIR fields in the descriptor table being executed.

(54) DMA Descriptor Link Pointer (Descriptor 1Ch) Register m (PCI_EP_DMADPLPm) (m = 0 to 7)

This register indicates the field value at offset 1Ch in the descriptor table. Only effective when descriptor-type DMA transfer is selected (the value read has no meaning in the case of register-type transfer).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 093Ch (m = 0)
<PCI_S0_REG_base> + 09BCh (m = 1)
<PCI_S0_REG_base> + 0A3Ch (m = 2)
<PCI_S0_REG_base> + 0ABCh (m = 3)
<PCI_S0_REG_base> + 0B3Ch (m = 4)
<PCI_S0_REG_base> + 0BBCh (m = 5)
<PCI_S0_REG_base> + 0C3Ch (m = 6)
<PCI_S0_REG_base> + 0CBCh (m = 7)

Initial Value: 0000_0000h

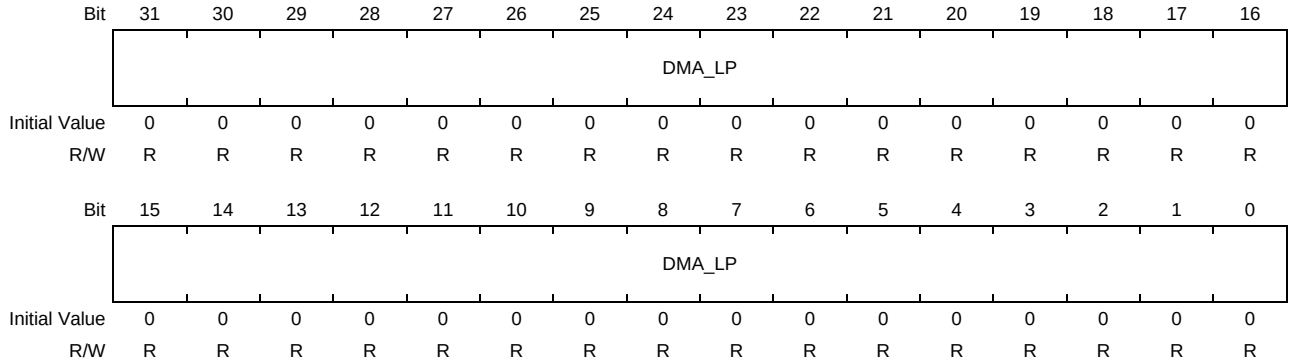


Table 36.5-61 PCI_EP_DMADPLPm Register Contents

Bit Position	Bit Name	Description
31 to 0	DMA_LP	Indicates the LP field value in the descriptor table being executed.

(55) DMA Rest Size Register m (PCI_EP_DMARESTSIZm) (m = 0 to 7)

This register indicates the number of bytes for which DMA transfer has not yet been completed.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0950h (m = 0)
<PCI_S0_REG_base> + 09D0h (m = 1)
<PCI_S0_REG_base> + 0A50h (m = 2)
<PCI_S0_REG_base> + 0AD0h (m = 3)
<PCI_S0_REG_base> + 0B50h (m = 4)
<PCI_S0_REG_base> + 0BD0h (m = 5)
<PCI_S0_REG_base> + 0C50h (m = 6)
<PCI_S0_REG_base> + 0CD0h (m = 7)

Initial Value: 0000_0000h

Table 36.5-62 PCI_EP_DMARESTSIZm Register Contents

Bit Position	Bit Name	Description
31 to 0	DMA_REST_SIZE	Indicates the number of bytes for which DMA transfer has not yet been completed (common to register-type and descriptor-type transfer).

(56) AXI Request Address Register m (PCI_EP_AREQAm) (m = 0 to 7)

This register indicates the address during AXI transfer that is in progress or for the most recently completed transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0954h (m = 0)
<PCI_S0_REG_base> + 09D4h (m = 1)
<PCI_S0_REG_base> + 0A54h (m = 2)
<PCI_S0_REG_base> + 0AD4h (m = 3)
<PCI_S0_REG_base> + 0B54h (m = 4)
<PCI_S0_REG_base> + 0BD4h (m = 5)
<PCI_S0_REG_base> + 0C54h (m = 6)
<PCI_S0_REG_base> + 0CD4h (m = 7)

Initial Value: 0000_0000h

Table 36.5-63 PCI_EP_AREQAm Register Contents

Bit Position	Bit Name	Description
31 to 0	AXI_REQ_ADDR	Indicates the address during AXI transfer that is in progress or for the most recently completed transfer (common to register type and descriptor type).

(57) PCIe Request Address (Lower) Register m (PCI_EP_PREQAmL) (m = 0 to 7)

This register indicates the lower 32 bits of the address during PCIe transfer that is in progress or for the most recently completed transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0958h (m = 0)
<PCI_S0_REG_base> + 09D8h (m = 1)
<PCI_S0_REG_base> + 0A58h (m = 2)
<PCI_S0_REG_base> + 0AD8h (m = 3)
<PCI_S0_REG_base> + 0B58h (m = 4)
<PCI_S0_REG_base> + 0BD8h (m = 5)
<PCI_S0_REG_base> + 0C58h (m = 6)
<PCI_S0_REG_base> + 0CD8h (m = 7)

Initial Value: 0000_0000h

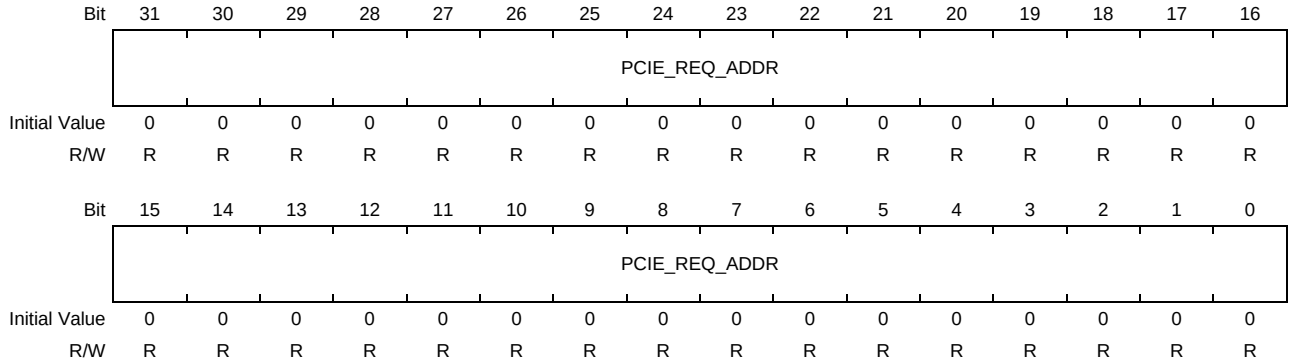


Table 36.5-64 PCI_EP_PREQAmL Register Contents

Bit Position	Bit Name	Description
31 to 0	PCIE_REQ_ADDR	Indicates the lower 32 bits of the address during PCIe transfer that is in progress or for the most recently completed transfer (common to register type and descriptor type).

(58) PCIe Request Address (Upper) Register m (PCI_EP_PREQAmU) (m = 0 to 7)

This register indicates the upper 32 bits of the address during PCIe transfer that is in progress or for the most recently completed transfer.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 095Ch (m = 0)
<PCI_S0_REG_base> + 09DCh (m = 1)
<PCI_S0_REG_base> + 0A5Ch (m = 2)
<PCI_S0_REG_base> + 0ADCh (m = 3)
<PCI_S0_REG_base> + 0B5Ch (m = 4)
<PCI_S0_REG_base> + 0BDCh (m = 5)
<PCI_S0_REG_base> + 0C5Ch (m = 6)
<PCI_S0_REG_base> + 0CDCh (m = 7)

Initial Value: 0000_0000h

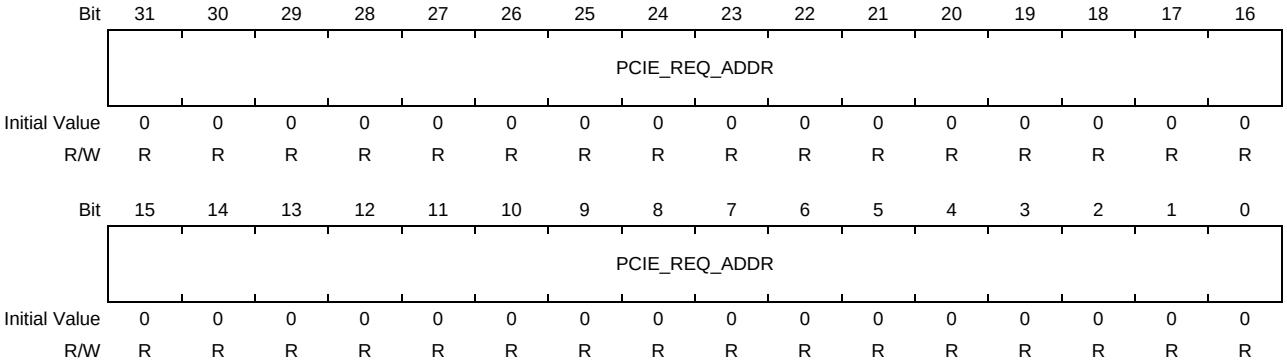


Table 36.5-65 PCI_EP_PREQAmU Register Contents

Bit Position	Bit Name	Description
31 to 0	PCIE_REQ_ADDR	Indicates the upper 32 bits of the address during PCIe transfer that is in progress or for the most recently completed transfer (common to register type and descriptor type).

(59) QUE Status Register m (PCI_EP_QUESTAm) (m = 0 to 7)

This register indicates the state of the descriptor queue.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0960h (m = 0)
<PCI_S0_REG_base> + 09E0h (m = 1)
<PCI_S0_REG_base> + 0A60h (m = 2)
<PCI_S0_REG_base> + 0AE0h (m = 3)
<PCI_S0_REG_base> + 0B60h (m = 4)
<PCI_S0_REG_base> + 0BE0h (m = 5)
<PCI_S0_REG_base> + 0C60h (m = 6)
<PCI_S0_REG_base> + 0CE0h (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	GO_LIST	LIST_NUM			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-66 PCI_EP_QUESTAm Register Contents

Bit Position	Bit Name	Description
31 to 5	—	Reserved. These bits are read as 0b.
4	GO_LIST	Indicates whether a descriptor list being executed is or is not present. 1b: Present 0b: Not present
3 to 0	LIST_NUM	Indicates the number of descriptor lists with which the queue for the given DMA channel has been loaded (any list currently being executed is not included). Attempts at making new entries in the queue while the value of this field is 8 (writing to the queue entry bits for the given channel) has no effect (will be ignored).

(60) DMAC Error Status Register m (PCI_EP_DMACESTAm) (m = 0 to 7)

This register indicates the error state of the DMAC.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 0968h (m = 0)
<PCI_S0_REG_base> + 09E8h (m = 1)
<PCI_S0_REG_base> + 0A68h (m = 2)
<PCI_S0_REG_base> + 0AE8h (m = 3)
<PCI_S0_REG_base> + 0B68h (m = 4)
<PCI_S0_REG_base> + 0BE8h (m = 5)
<PCI_S0_REG_base> + 0C68h (m = 6)
<PCI_S0_REG_base> + 0CE8h (m = 7)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	CFG_BM_DIS_EP	BME_SUP	BME_DOWN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	Debug	MOR_CD_PERR	MOR_CH_PERR	MOR_EP_PERR	MOR_STATUS			—	—	—	Debug		—	AXI_RESP	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-67 PCI_EP_DMACESTAm Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b.
18	CFG_BM_DIS_EP	Set when the macro is operating as an endpoint and the state of Bus Master Enable Off (configuration space 004h bit [2] = 0b) is detected. The value is kept until CHm_ERR is cleared.
17	BME_SUP	Set as a setting factor of CHm_ERR when a suspend signal from PCIe is detected. The value is kept until CHm_ERR is cleared. This bit is only valid in endpoint mode.
16	BME_DOWN	Set as a setting factor of CHm_ERR when a stop signal from PCIe is detected. The value is kept until CHm_ERR is cleared.
15	—	Reserved. This bit is read as 0b.
14	Debug	Debug register
13	MOR_CD_PERR	Set as a setting factor of CHm_ERR when MOR_CD_PERR is detected. The value is kept until CHm_ERR is cleared.
12	MOR_CH_PERR	Set as a setting factor of CHm_ERR when MOR_CH_PERR is detected. The value is kept until CHm_ERR is cleared.
11	MOR_EP_ERR	Set as a setting factor of CHm_ERR when it is a poisoned completion. The value is kept until CHm_ERR is cleared.

Table 36.5-67 PCI_EP_DMACESTAm Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	MOR_STATUS	Indicates the MOR_STATUS value as a setting factor of CHm_ERR if MOR_STATUS is not 000b (success). The value is kept until CHm_ERR is cleared. 000b: Initial value 001b: Unsupported request 010b: CRS 011b: Completion timeout 100b: Completer abort 101b: Unexpected completion 110b: Reserved 111b: Mismatched length (length overrun)
7 to 5	—	Reserved. These bits are read as 0b.
4, 3	Debug	Debug register
2	—	Reserved. This bit is read as 0b.
1, 0	AXI_RESP	Indicates a slave response in AXI master transactions. This field is updated when CHx_ERR is set. The value is kept until the bit is cleared. 00b: Initial value. 01b: Reserved 10b: SLVERR 11b: DECERR

(61) AXI Window Base m Register (Function #n) (PCI_EP_AWBASEm_Fn) (m = 0 to 7, n = 0, 1)

This register is for setting windows for address conversion in access from PCIe to AXI. It sets the base address on the PCI side. The areas are set on 4-Kbyte boundaries.

Access Size: 32 bits

Address(es):
<PCI_S0_REG_base> + 1000h (m = 0, Funtion#0)
<PCI_S0_REG_base> + 1010h (m = 1, Funtion#0)
<PCI_S0_REG_base> + 1020h (m = 2, Funtion#0)
<PCI_S0_REG_base> + 1030h (m = 3, Funtion#0)
<PCI_S0_REG_base> + 1040h (m = 4, Funtion#0)
<PCI_S0_REG_base> + 1050h (m = 5, Funtion#0)
<PCI_S0_REG_base> + 1060h (m = 6, Funtion#0)
<PCI_S0_REG_base> + 1070h (m = 7, Funtion#0)
<PCI_S0_REG_base> + 1200h (m = 0, Funtion#1)
<PCI_S0_REG_base> + 1210h (m = 1, Funtion#1)
<PCI_S0_REG_base> + 1220h (m = 2, Funtion#1)
<PCI_S0_REG_base> + 1230h (m = 3, Funtion#1)
<PCI_S0_REG_base> + 1240h (m = 4, Funtion#1)
<PCI_S0_REG_base> + 1250h (m = 5, Funtion#1)
<PCI_S0_REG_base> + 1260h (m = 6, Funtion#1)
<PCI_S0_REG_base> + 1270h (m = 7, Funtion#1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	AWBase[31:12]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AWBase[31:12]				AWBase[11:4]								—	—	Debug	AXI Window Enable
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	R	R	R	R	R	R	R	R	R	R	RW	RW

Table 36.5-68 PCI_EP_AWBASEm_Fn Register Contents

Bit Position	Bit Name	Description
31 to 12	AWBase[31:12]	Setting windows for address conversion in access from PCIe to AXI. The areas are set in 4-Kbyte boundaries.
11 to 4	AWBase[11:4]	Fixed to 0000_0000b.
3, 2	—	Reserved. These bits are read as 0b.
1	Debug	This register is for use in debugging by Renesas.
0	AXI Window Enable	Enable AXI windows. 0b: Disable windows. 1b: Enable windows.

(62) AXI Window Mask m Register (Function #n) (PCI_EP_AWMASKm_Fn) (m = 0 to 7, n = 0, 1)

This register is for setting windows for address conversion in access from PCIe to AXI. The window is set as the area corresponding to the number of set bits from the address set in the AWBase register. The area which can be set is 4K × 2^N bytes.

Access Size: 32 bits

Address(es):
<PCI_S0_REG_base> + 1004h (m = 0, Funtion#0)
<PCI_S0_REG_base> + 1014h (m = 1, Funtion#0)
<PCI_S0_REG_base> + 1024h (m = 2, Funtion#0)
<PCI_S0_REG_base> + 1034h (m = 3, Funtion#0)
<PCI_S0_REG_base> + 1044h (m = 4, Funtion#0)
<PCI_S0_REG_base> + 1054h (m = 5, Funtion#0)
<PCI_S0_REG_base> + 1064h (m = 6, Funtion#0)
<PCI_S0_REG_base> + 1074h (m = 7, Funtion#0)
<PCI_S0_REG_base> + 1204h (m = 0, Funtion#1)
<PCI_S0_REG_base> + 1214h (m = 1, Funtion#1)
<PCI_S0_REG_base> + 1224h (m = 2, Funtion#1)
<PCI_S0_REG_base> + 1234h (m = 3, Funtion#1)
<PCI_S0_REG_base> + 1244h (m = 4, Funtion#1)
<PCI_S0_REG_base> + 1254h (m = 5, Funtion#1)
<PCI_S0_REG_base> + 1264h (m = 6, Funtion#1)
<PCI_S0_REG_base> + 1274h (m = 7, Funtion#1)

Initial Value: 0000_0FFFh

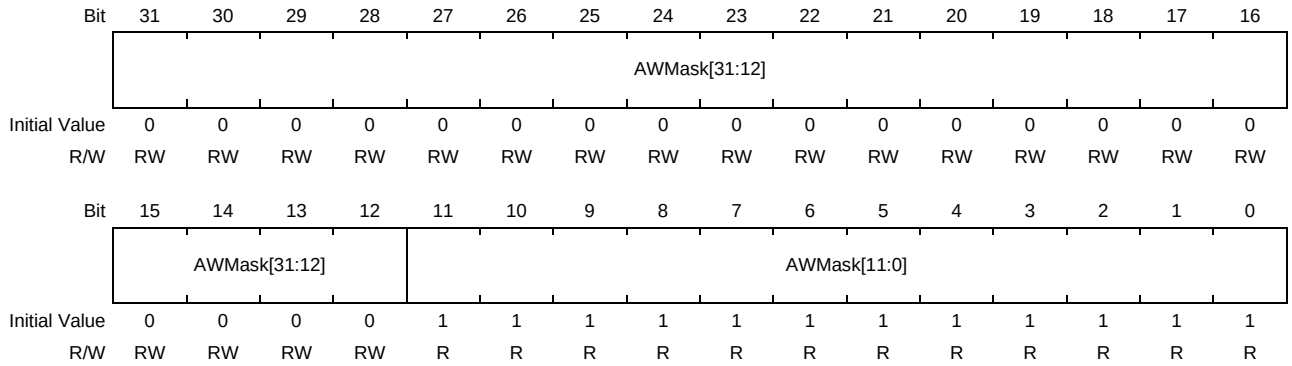


Table 36.5-69 PCI_EP_AWMASKm_Fn Register Contents

Bit Position	Bit Name	Description
31 to 12	AWMask[31:12]	The window is set as the area corresponding to the number of set bits from the address set in the AWBase register. Set 1b from the lowest-order bit. Accordingly, the area which can be set is 4K × 2^N bytes.
11 to 0	AWMask[11:0]	Fixed to 1111_1111_1111b.

(63) AXI Destination m Register (Function #n) (PCI_EP_ADESTm_Fn) (m = 0 to 7, n = 0, 1)

This register is for setting windows for address conversion in access from PCIe to AXI. It sets the base address on the AXI side. The areas are set on 4-Kbyte boundaries.

Access Size: 32 bits

Address(es):
<PCI_S0_REG_base> + 1008h (m = 0, Funtion#0)
<PCI_S0_REG_base> + 1018h (m = 1, Funtion#0)
<PCI_S0_REG_base> + 1028h (m = 2, Funtion#0)
<PCI_S0_REG_base> + 1038h (m = 3, Funtion#0)
<PCI_S0_REG_base> + 1048h (m = 4, Funtion#0)
<PCI_S0_REG_base> + 1058h (m = 5, Funtion#0)
<PCI_S0_REG_base> + 1068h (m = 6, Funtion#0)
<PCI_S0_REG_base> + 1078h (m = 7, Funtion#0)
<PCI_S0_REG_base> + 1208h (m = 0, Funtion#1)
<PCI_S0_REG_base> + 1218h (m = 1, Funtion#1)
<PCI_S0_REG_base> + 1228h (m = 2, Funtion#1)
<PCI_S0_REG_base> + 1238h (m = 3, Funtion#1)
<PCI_S0_REG_base> + 1248h (m = 4, Funtion#1)
<PCI_S0_REG_base> + 1258h (m = 5, Funtion#1)
<PCI_S0_REG_base> + 1268h (m = 6, Funtion#1)
<PCI_S0_REG_base> + 1278h (m = 7, Funtion#1)

Initial Value: 0000_0000h

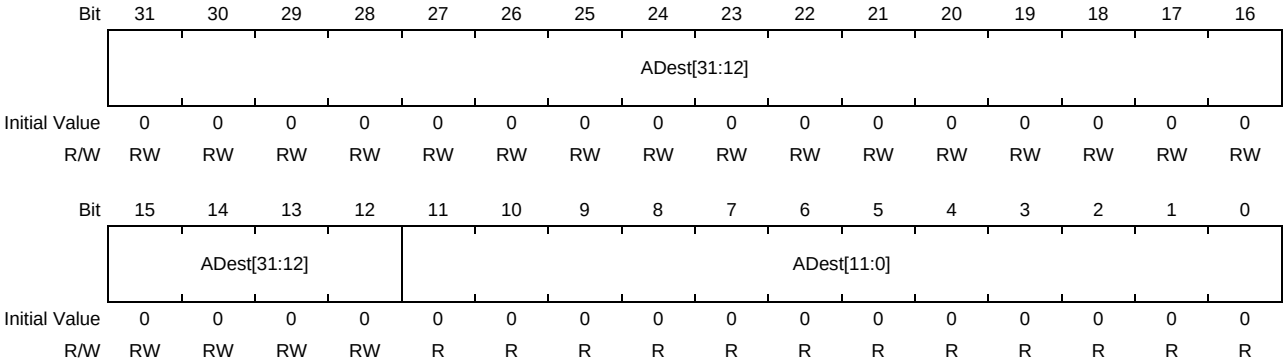


Table 36.5-70 PCI_EP_ADESTm_Fn Register Contents

Bit Position	Bit Name	Description
31 to 12	ADest[31:12]	Sets the base address on the AXI side. The areas are set on 4-Kbyte boundaries.
11 to 0	ADest[11:0]	Fixed to 0000_0000_0000b.

(64) PCIe Window Base m Register (Function #n) (PCI_EP_PWBASEm_Fn) (m = 0 to 7, n = 0, 1)

This register is for setting windows for address conversion in access from AXI to PCIe. It sets the base address on the AXI side. The areas are set on 4-Kbyte boundaries.

Access Size: 32 bits

Address(es):
<PCI_S0_REG_base> + 1100h (m = 0, Funtion#0)
<PCI_S0_REG_base> + 1110h (m = 1, Funtion#0)
<PCI_S0_REG_base> + 1120h (m = 2, Funtion#0)
<PCI_S0_REG_base> + 1130h (m = 3, Funtion#0)
<PCI_S0_REG_base> + 1140h (m = 4, Funtion#0)
<PCI_S0_REG_base> + 1150h (m = 5, Funtion#0)
<PCI_S0_REG_base> + 1160h (m = 6, Funtion#0)
<PCI_S0_REG_base> + 1170h (m = 7, Funtion#0)
<PCI_S0_REG_base> + 1300h (m = 0, Funtion#1)
<PCI_S0_REG_base> + 1310h (m = 1, Funtion#1)
<PCI_S0_REG_base> + 1320h (m = 2, Funtion#1)
<PCI_S0_REG_base> + 1330h (m = 3, Funtion#1)
<PCI_S0_REG_base> + 1340h (m = 4, Funtion#1)
<PCI_S0_REG_base> + 1350h (m = 5, Funtion#1)
<PCI_S0_REG_base> + 1360h (m = 6, Funtion#1)
<PCI_S0_REG_base> + 1370h (m = 7, Funtion#1)

Initial Value: 0000_0000h

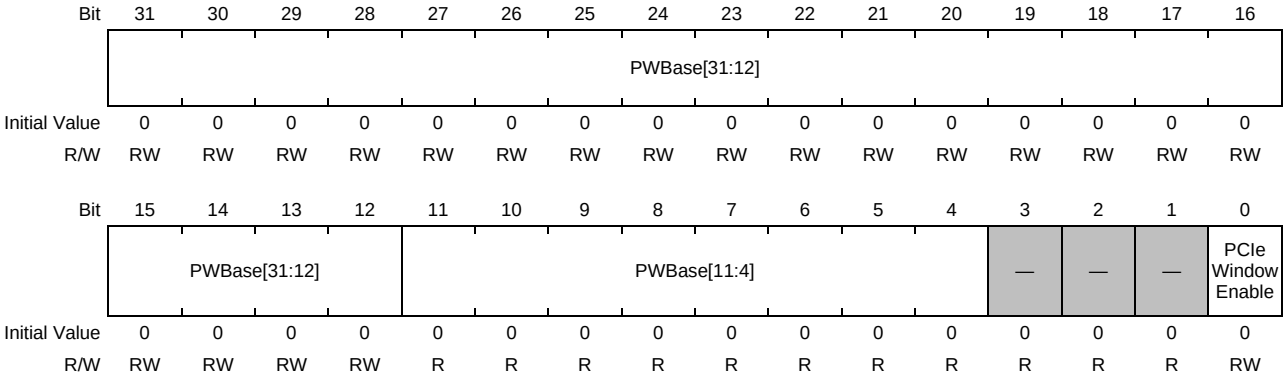


Table 36.5-71 PCI_EP_PWBASEm_Fn Register Contents

Bit Position	Bit Name	Description
31 to 12	PWBase[31:12]	Setting windows for address conversion in access from AXI to PCIe. The areas are set on 4-Kbyte boundaries.
11 to 4	PWBase[11:4]	Fixed to 0000_0000b.
3 to 1	—	Reserved. These bits are read as 0b.
0	PCIe Window Enable	Enable PCIe windows. 0b: Disable windows. 1b: Enable windows.

(65) PCIe Window Mask m Register (Function #n) (PCI_EP_PWMASKm_Fn) (m = 0 to 7, n = 0, 1)

This register is for setting windows for address conversion in access from AXI to PCIe. The window is set as the area corresponding to the number of set bits from the address set in the PWBase register.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 1104h (m = 0, Funtion#0)
<PCI_S0_REG_base> + 1114h (m = 1, Funtion#0)
<PCI_S0_REG_base> + 1124h (m = 2, Funtion#0)
<PCI_S0_REG_base> + 1134h (m = 3, Funtion#0)
<PCI_S0_REG_base> + 1144h (m = 4, Funtion#0)
<PCI_S0_REG_base> + 1154h (m = 5, Funtion#0)
<PCI_S0_REG_base> + 1164h (m = 6, Funtion#0)
<PCI_S0_REG_base> + 1174h (m = 7, Funtion#0)
<PCI_S0_REG_base> + 1304h (m = 0, Funtion#1)
<PCI_S0_REG_base> + 1314h (m = 1, Funtion#1)
<PCI_S0_REG_base> + 1324h (m = 2, Funtion#1)
<PCI_S0_REG_base> + 1334h (m = 3, Funtion#1)
<PCI_S0_REG_base> + 1344h (m = 4, Funtion#1)
<PCI_S0_REG_base> + 1354h (m = 5, Funtion#1)
<PCI_S0_REG_base> + 1364h (m = 6, Funtion#1)
<PCI_S0_REG_base> + 1374h (m = 7, Funtion#1)

Initial Value: 0000_0FFFh

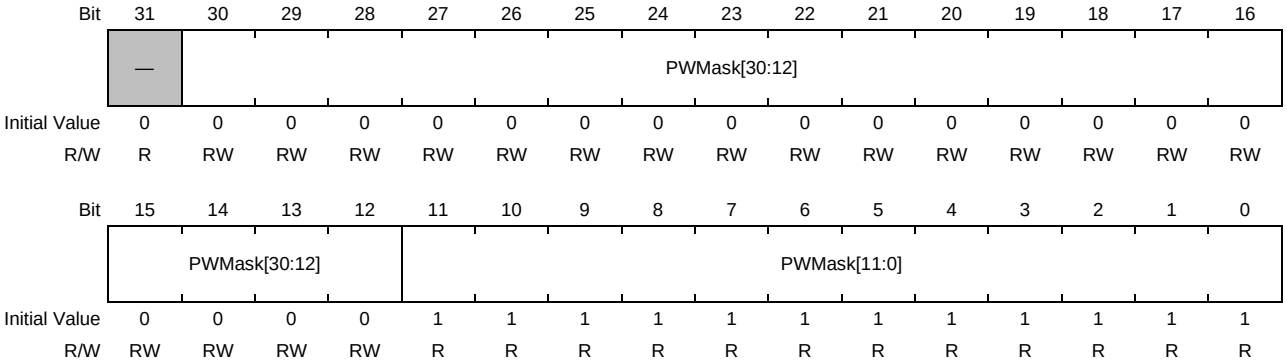


Table 36.5-72 PCI_EP_PWMASKm_Fn Register Contents

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b.
30 to 12	PWMask[30:12]	The window is set as the area corresponding to the number of set bits from the address set in the PWBase register. Set 1b from the lowest-order bit.
11 to 0	PWMask[11:0]	Fixed to 1111_1111_1111b.

(66) PCIe Destination m (Lower) Register (Function #n) (PCI_EP_PDESTLOm_Fn) (m = 0 to 7, n = 0, 1)

This register is for setting windows for address conversion in access from AXI to PCIe. It sets the base address on the PCIe side. The areas are set on 4-Kbyte boundaries.

Access Size: 32 bits

Address(es):
<PCI_S0_REG_base> + 1108h (m = 0, Funtion#0)
<PCI_S0_REG_base> + 1118h (m = 1, Funtion#0)
<PCI_S0_REG_base> + 1128h (m = 2, Funtion#0)
<PCI_S0_REG_base> + 1138h (m = 3, Funtion#0)
<PCI_S0_REG_base> + 1148h (m = 4, Funtion#0)
<PCI_S0_REG_base> + 1158h (m = 5, Funtion#0)
<PCI_S0_REG_base> + 1168h (m = 6, Funtion#0)
<PCI_S0_REG_base> + 1178h (m = 7, Funtion#0)
<PCI_S0_REG_base> + 1308h (m = 0, Funtion#1)
<PCI_S0_REG_base> + 1318h (m = 1, Funtion#1)
<PCI_S0_REG_base> + 1328h (m = 2, Funtion#1)
<PCI_S0_REG_base> + 1338h (m = 3, Funtion#1)
<PCI_S0_REG_base> + 1348h (m = 4, Funtion#1)
<PCI_S0_REG_base> + 1358h (m = 5, Funtion#1)
<PCI_S0_REG_base> + 1368h (m = 6, Funtion#1)
<PCI_S0_REG_base> + 1378h (m = 7, Funtion#1)

Initial Value: 0000_0000h

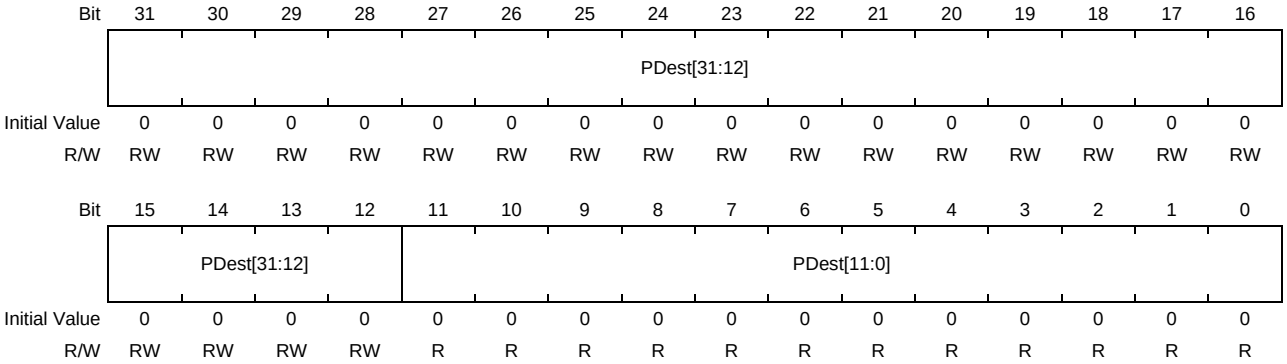


Table 36.5-73 PCI_EP_PDESTLOm_Fn Register Contents

Bit Position	Bit Name	Description
31 to 12	PDest[31:12]	Sets the base address on the PCIe side. The areas are set on 4-Kbyte boundaries.
11 to 0	PDest[11:0]	Fixed to 0000_0000_0000b.

(67) PCIe Destination m (Upper) Register (Function #n) (PCI_EP_PDESTUPm_Fn) (m = 0 to 7, n = 0, 1)

This register is for setting windows for address conversion in access from AXI to PCIe. It sets the base address on the PCIe side. The areas are set on 4-Kbyte boundaries.

Access Size: 32 bits

Address(es):
<PCI_S0_REG_base> + 110Ch (m = 0, Funtion#0)
<PCI_S0_REG_base> + 111Ch (m = 1, Funtion#0)
<PCI_S0_REG_base> + 112Ch (m = 2, Funtion#0)
<PCI_S0_REG_base> + 113Ch (m = 3, Funtion#0)
<PCI_S0_REG_base> + 114Ch (m = 4, Funtion#0)
<PCI_S0_REG_base> + 115Ch (m = 5, Funtion#0)
<PCI_S0_REG_base> + 116Ch (m = 6, Funtion#0)
<PCI_S0_REG_base> + 117Ch (m = 7, Funtion#0)
<PCI_S0_REG_base> + 130Ch (m = 0, Funtion#1)
<PCI_S0_REG_base> + 131Ch (m = 1, Funtion#1)
<PCI_S0_REG_base> + 132Ch (m = 2, Funtion#1)
<PCI_S0_REG_base> + 133Ch (m = 3, Funtion#1)
<PCI_S0_REG_base> + 134Ch (m = 4, Funtion#1)
<PCI_S0_REG_base> + 135Ch (m = 5, Funtion#1)
<PCI_S0_REG_base> + 136Ch (m = 6, Funtion#1)
<PCI_S0_REG_base> + 137Ch (m = 7, Funtion#1)

Initial Value: 0000_0000h

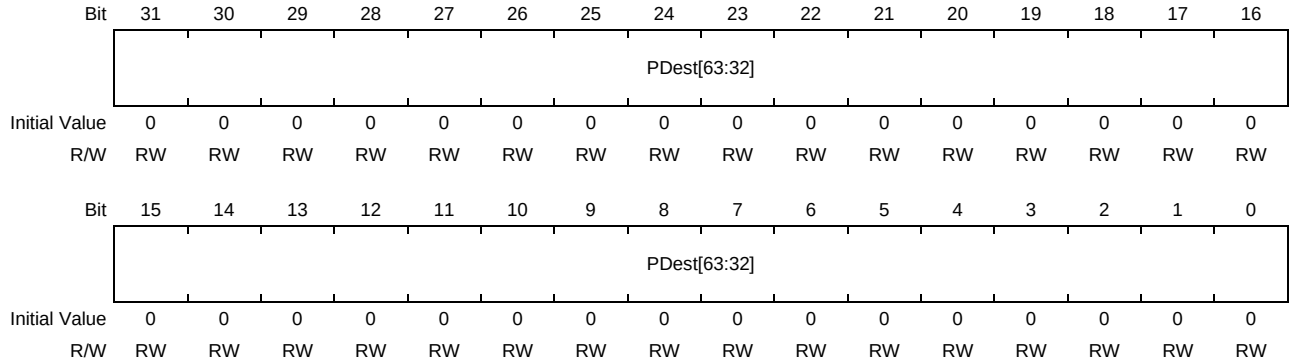


Table 36.5-74 PCI_EP_PDESTUPm_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	PDest[63:32]	Sets the base address on the PCIe side. The areas are set on 4-Kbyte boundaries.

36.5.3.2 PCI Express Configuration Registers (Type0)

(1) Vendor and Device ID (Function #n) Register (PCI_EP_VID_Fn) (n = 0, 1)

This register indicates the vendor and device ID.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6000h (Function #0)
<PCI_S0_REG_base> + 7000h (Function #1)

Initial Value: Configurable Value

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Device ID															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Vendor ID															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-75 PCI_EP_VID_Fn Register Contents

Bit Position	Bit Name	Description
31 to 16	Device ID	Indicates the manufacturer. Set a fixed value.
15 to 0	Vendor ID	Used to identify devices manufactured by the manufacturer indicated by the vendor ID. Set a fixed value.

Table 36.5-76 Valid Reset Signal

Reset Signal	Device ID	Vendor ID
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		
FLR		

(2) Command and Status (Function #n) (PCI_EP_COM_STA_Fn) (n = 0, 1)

This register specifies the command and the status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6004h (Function #0)
<PCI_S0_REG_base> + 7004h (Function #1)

Initial Value: 0010_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Detected Parity Error	Signaled System Error	Received Master Abort	Received Target Abort	Signaled Target Abort	DEVSEL Timing		Master Data Parity Error	Fast Back-to-Back Transaction Capable	—	66MHz Capable	Capabilities List	Interrupt Status	—	—	Immediate Readiness
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	R	R	RW	R	R	R	R	R	R	R	R
R/W (PCIe)	RW1	RW1	RW1	RW1	RW1	R	R	RW1	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	Interrupt Disable	Fast Back-to-Back Transaction Enable	SERR# Enable	IDSEL Stepping/Wait Cycle Control	Parity Error Response	VGA Palette Snoop	Memory Write and Invalidate	Special Cycle Enable	Bus Master Enable	Memory Space Enable	IO Space Enable
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	RW	R	RW	R	RW	R	R	R	RW	RW	R
R/W (PCIe)	R	R	R	R	R	RW	R	RW	R	RW	R	R	R	RW	RW	R

Table 36.5-77 PCI_EP_COM_STA_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31	Detected Parity Error	Set to 1b when a poisoned TLP is received regardless of the setting of the Parity Error Response bit. It is cleared by writing 1b during PCIe access. Writing 0b has no effect.
30	Signaled System Error	Set to 1b when this unit has transmitted an ERR_FATAL or ERR_NONFATAL message while the SERR Enable bit is 1b. It is cleared by writing 1b during PCIe access. Writing 0b has no effect.
29	Received Master Abort	Set to 1b when a received Completion Status field indicates the completion of an unsupported request. It is cleared by writing 1b during PCIe access. Writing 0b has no effect.
28	Received Target Abort	Set to 1b when a received Completion Status field indicates the completer abortion state. It is cleared by writing 1b during PCIe access. Writing 0b has no effect.
27	Signaled Target Abort	Set to 1b when the Completion Status field indicated the completer abortion state at the time of transmission for completion. It is cleared by writing 1b during PCIe access. Writing 0b has no effect.
26, 25	DEVSEL Timing	Reserved. Does not apply to PCI Express. (Fixed to 00b.)
24	Master Data Parity Error	Set to 1b when the setting of the Parity Error Response bit becomes 1b and either of the following two conditions is satisfied. – The requester (BME) having received a poisoned completion TLP – The Requester (BME) having transmitted a poisoned write request TLP This bit is not set to 1b if the Parity Error Response bit is 0b. It is cleared by writing 1b during PCIe access. Writing 0b has no effect.
23	Fast Back-to-Back Transaction Capable	Reserved. Does not apply to PCI Express (fixed to 0b).
22	—	Reserved. This bit is read as 0b.
21	66MHz Capable	Reserved. Does not apply to PCI Express (fixed to 0b).

Table 36.5-77 PCI_EP_COM_STA_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
20	Capabilities List	This bit is fixed to 1b because all PCI Express devices by definition have PCI Express capability.
19	Interrupt Status	Indicates the interrupt state of the device.
18, 17	—	Reserved. These bits are read as 0b.
16	Immediate Readiness	Fixed to 0b.
15 to 11	—	Reserved. These bits are read as 0b.
10	Interrupt Disable	Disables transmission of Assert_INTx messages. Assert_INTx messages cannot be transmitted when the setting is 1b. If this bit is set to 1b while an Assert_INTx message has been transmitted, a Deassert_INTx message must be transmitted.
9	Fast Back-to-Back Transaction Enable	Reserved. Does not apply to PCI Express (fixed to 0b).
8	SERR# Enable	When set to 1b, the root complex is notified of a non-fatal error or fatal error through a message transaction. *Note*: Even if this bit is not set, the root complex is notified of an error through a message transaction when the Error Reporting bit in the Device Control register of PCI Express Capability is set to 1b.
7	IDSEL Stepping / Wait Cycle Control	Reserved. Does not apply to PCI Express (fixed to 0b).
6	Parity Error Response	Controls operation when a poisoned TLP is transmitted or received. *Note*: Errors are logged in the Detected Parity Error field of the Status register, the Device Status register of the PCI Express Capability, and the Uncorrectable Error Status register of the Advanced Error Reporting Capability, regardless of the setting of this bit.
5	VGA Palette Snoop	Reserved. Does not apply to PCI Express (fixed to 0b).
4	Memory Write and Invalidate	Reserved. Does not apply to PCI Express (fixed to 0b).
3	Special Cycle Enable	Reserved. Does not apply to PCI Express (fixed to 0b).
2	Bus Master Enable	Controls whether to operate as a bus master.
1	Memory Space Enable	Controls whether the device returns a response in the case of access to the memory space.
0	I/O Space Enable	Controls whether the device returns a response in the case of access to the I/O space.

Table 36.5-78 Valid Reset Signal

Reset Signal	Detected Parity Error	Signaled System Error	Received Master Abort	Received Target Abort	Signaled Target Abort	Master Data Parity Error
RST_LOAD_B						
RST_RSM_B						
RST_CFG_B	✓	✓	✓	✓	✓	✓
FLR	✓	✓	✓	✓	✓	✓

Reset Signal	Interrupt Disable	SERR# Enable	Parity Error Response	Bus Master Enable	Memory Space Enable
RST_LOAD_B					
RST_RSM_B					
RST_CFG_B	✓	✓	✓	✓	✓
FLR	✓	✓	✓	✓	✓

(3) Revision ID and Class Code (Function #n) (PCI_EP_RID_CC_Fn) (n = 0, 1)

This register indicates the revision ID and the class code.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6008h (Function #0)
<PCI_S0_REG_base> + 7008h (Function #1)

Initial Value: Configurable Value

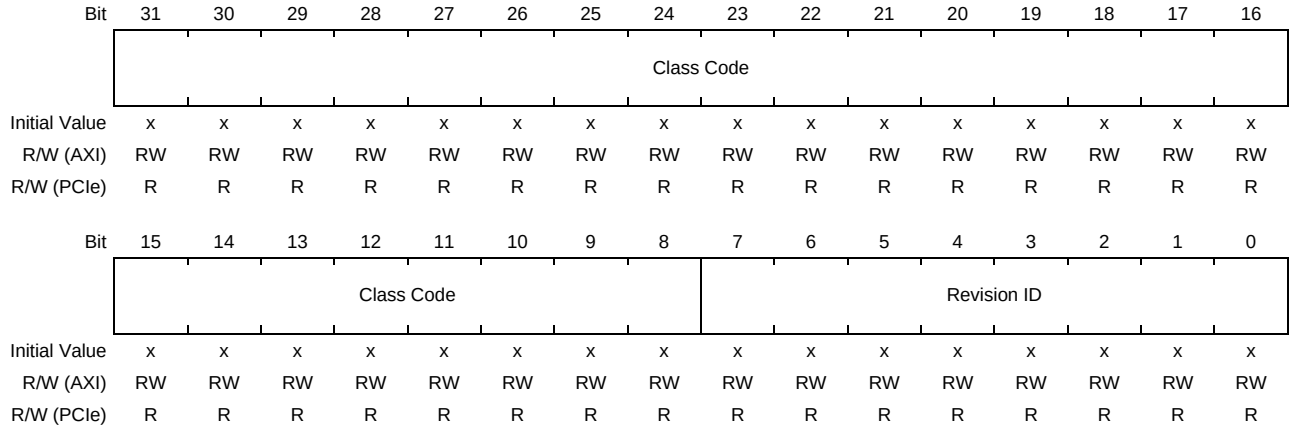


Table 36.5-79 PCI_EP_RID_CC_Fn Register Contents

Bit Position	Bit Name	Description
31 to 8	Class Code	Indicates information on the type and function of the device and their values are defined by the PCI special interest group (PCI-SIG) as follows. 31 to 24: Base class 23 to 16: Sub-class 15 to 8: Programming interface
7 to 0	Revision ID	An 8-bit ID used to indicate the revision number of a specific device specified by its vendor and device IDs. Set a fixed value.

Table 36.5-80 Valid Reset Signal

Reset Signal	Class Code	Capabilities List
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		
FLR		

(4) Cache Line and Header Type (Function #n) (PCI_EP_CL_HT) (n = 0 to 1)

This register indicates the cache line size and the header type.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 600Ch (Function #0)
<PCI_S0_REG_base> + 700Ch (Function #1)

Initial Value: 0080_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BIST								Header Type							
Initial Value	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Master Latency Timer								Cache Line Size							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-81 PCI_EP_CL_HT Register Contents

Bit Position	Bit Name	Description
31 to 24	BIST	Reserved. Does not apply to PCI Express (fixed to 00h).
23 to 16	Header Type	Multi-Function Device bit = 1b (fixed to 80h)
15 to 8	Master Latency Timer	Reserved. Does not apply to PCI Express (fixed to 00h).
7 to 0	Cache Line Size	Though these bits are implemented as a readable/writable field for legacy compatibility, the setting has no effect on this device.

Table 36.5-82 Valid Reset Signal

Reset Signal	Cache Line Size
RST_LOAD_B	
RST_RSM_B	
RST_CFG_B	✓
FLR	✓

(5) Base Address Register 0 (Function #n) (PCI_EP_BAR0_Fn) (n = 0, 1)

This register forms a 64-bit memory space in combination with Base Address Register 1 (BAR1).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6010h (Function #0)
<PCI_S0_REG_base> + 7010h (Function #1)

Initial Value: 0000_0004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register 0															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register 0												Prefetch	Type	—	Memory Space Indicator
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R

Table 36.5-83 PCI_EP_BAR0_Fn Register Contents

Bit Position	Bit Name	Description
31 to 4	Base Address Register 0	Indicates the base address. Some lower bits of this field are implemented as read-only bits that are fixed to 0b to suit the required size of the address block. Read-only bits of this unit can be set in Base Address Register Mask00 (Lower) (address: <PCI_S0_REG_base> + 60A0h).
3	Prefetch	0b: Disabled 1b: Enabled
2	Type	0b: 32-bit address 1b: 64-bit address A 64-bit address is used. Fixed to 1b.
1	—	Reserved. This bit is read as 0b.
0	Memory Space Indicator	Indicates the memory space. Fixed to 0b.

Table 36.5-84 Valid Reset Signal

Reset Signal	Base Address Register 0	Prefetch	Type	Memory Space Indicator
RST_LOAD_B		✓	✓	✓
RST_RSM_B				
RST_CFG_B	✓			
FLR	✓			

(6) Base Address Register 1 (Function #n) (PCI_EP_BAR1_Fn) (n = 0, 1)

This register forms a 64-bit memory space in combination with Base Address Register 0 (BAR0).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6014h (Function #0)
<PCI_S0_REG_base> + 7014h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register 1															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register 1															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-85 PCI_EP_BAR1_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register 1	Base Address Register 1 (64-bit Upper Address) Indicates the upper 32 bits of the base address. Read-only bits of this unit can be set in Base Address Register Mask00 (Upper) (address: <PCI_S0_REG_base> + 60A4h).

Table 36.5-86 Valid Reset Signal

Reset Signal	Base Address Register 1
RST_LOAD_B	
RST_RSM_B	
RST_CFG_B	✓
FLR	✓

(7) Base Address Register 2 (Function #n) (PCI_EP_BAR2_Fn) (n = 0, 1)

This register forms a 64-bit memory space in combination with Base Address Register 3 (BAR3).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6018h (Function #0)
<PCI_S0_REG_base> + 7018h (Function #1)

Initial Value: 0000_0004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register 2															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register 2												Prefetch	Type	—	Memory Space Indicator
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R

Table 36.5-87 PCI_EP_BAR2_Fn Register Contents

Bit Position	Bit Name	Description
31 to 4	Base Address Register 2	Indicates the base address. Some lower bits of this field are implemented as read-only bits that are fixed to 0b to suit the required size of the address block. Read-only bits of this unit can be set in Base Address Register Mask01 (Lower) (address: <PCI_S0_REG_base> + 60A8h).
3	Prefetch	0b: Disabled 1b: Enabled
2	Type	0b: 32-bit address 1b: 64-bit address A 64-bit address is used. Fixed to 1b.
1	—	Reserved. This bit is read as 0b.
0	Memory Space Indicator	Indicates the memory space. Fixed to 0b.

Table 36.5-88 Valid Reset Signal

Reset Signal	Base Address Register 2	Prefetch	Type	Memory Space Indicator
RST_LOAD_B		✓	✓	✓
RST_RSM_B				
RST_CFG_B	✓			
FLR	✓			

(8) Base Address Register 3 (Function #n) (PCI_EP_BAR3_Fn) (n = 0, 1)

This register forms a 64-bit memory space in combination with Base Address Register 2 (BAR2).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 601Ch (Function #0)
<PCI_S0_REG_base> + 701Ch (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register 3															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register 3															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-89 PCI_EP_BAR3_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register 3	Indicates the base address. Some lower bits of this field are implemented as read-only bits that are fixed to 0b to suit the required size of the address block. Read-only bits of this unit can be set in Base Address Register Mask01 (Upper) (address: <PCI_S0_REG_base> + 60ACh).

Table 36.5-90 Valid Reset Signal

Reset Signal	Base Address Register 3
RST_LOAD_B	
RST_RSM_B	
RST_CFG_B	✓
FLR	✓

(9) Base Address Register 4 (Function #n) (PCI_EP_BAR4_Fn) (n = 0, 1)

This register forms a 64-bit memory space in combination with Base Address Register 5 (BAR5).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6020h (Function #0)
<PCI_S0_REG_base> + 7020h (Function #1)

Initial Value: 0000_0004h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register 4															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register 4												Prefetch	Type	—	Memory Space Indicator
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R

Table 36.5-91 PCI_EP_BAR4_Fn Register Contents

Bit Position	Bit Name	Description
31 to 4	Base Address Register 4	Indicates the base address. Some lower bits of this field are implemented as read-only bits that are fixed to 0b to suit the required size of the address block. Read-only bits of this unit can be set in Base Address Register Mask02 (Lower) (address: <PCI_S0_REG_base> + 60B0h).
3	Prefetch	0b: Disabled 1b: Enabled
2	Type	0b: 32-bit address 1b: 64-bit address A 64-bit address is used. Fixed to 1b.
1	—	Reserved. This bit is read as 0b.
0	Memory Space Indicator	Indicates the memory space. Fixed to 0b.

Table 36.5-92 Valid Reset Signal

Reset Signal	Base Address Register 4	Prefetch	Type	Memory Space Indicator
RST_LOAD_B		✓	✓	✓
RST_RSM_B				
RST_CFG_B	✓			
FLR	✓			

(10) Base Address Register 5 (Function #n) (PCI_EP_BAR5_Fn) (n = 0, 1)

This register forms a 64-bit memory space in combination with Base Address Register 4 (BAR4).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6024h (Function #0)
<PCI_S0_REG_base> + 7024h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register 5															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register 5															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-93 PCI_EP_BAR5_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register 5	Indicates the base address. Some lower bits of this field are implemented as read-only bits that are fixed to 0b to suit the required size of the address block. Read-only bits of this unit can be set in Base Address Register Mask02 (Upper) (address: <PCI_S0_REG_base> + 60B4h).

Table 36.5-94 Valid Reset Signal

Reset Signal	Base Address Register 5
RST_LOAD_B	
RST_RSM_B	
RST_CFG_B	✓
FLR	✓

(11) Subsystem ID (Function #n) (PCI_EP_SSID_Fn) (n = 0, 1)

This register indicates the subsystem ID.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 602Ch (Function #0)
<PCI_S0_REG_base> + 702Ch (Function #1)

Initial Value: Configurable Value

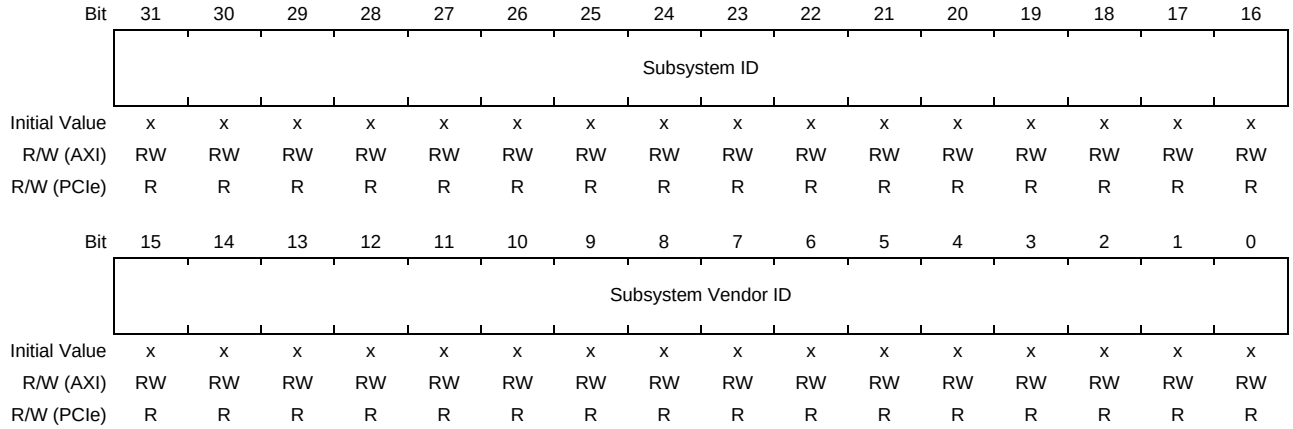


Table 36.5-95 PCI_EP_SSID_Fn Register Contents

Bit Position	Bit Name	Description
31 to 16	Subsystem ID	A 16-bit ID for use in identifying the subsystem made by the manufacturer which is specified by the subsystem vendor ID.
15 to 0	Subsystem Vendor ID	A 16-bit ID indicating the manufacturer of an add-in card or subsystem that incorporates this device. Set a fixed value.

(12) Capabilities Pointer (Function #n) (PCI_EP_CP_Fn) (n = 0, 1)

This register indicates start address for implementing the capability.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6034h (Function #0)
<PCI_S0_REG_base> + 7034h (Function #1)

Initial Value: 0000_0040h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Capability Pointer							
Initial Value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-96 PCI_EP_CP_Fn Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	Capabilities Pointer	Capability implementation start address 40h. The PCI power management capability is implemented from address 40h.

(13) Interrupt Register (Function #n) (PCI_EP_INT_Fn) (n = 0, 1)

This register assigns an interrupt to the terminal.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 603Ch (Function #0)
<PCI_S0_REG_base> + 703Ch (Function #1)

Initial Value: 0000_0100h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Max_Lat								Min_Gnt							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Interrupt Pin								Interrupt Line							
Initial Value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-97 PCI_EP_INT_Fn Register Contents

Bit Position	Bit Name	Description
31 to 24	Max_Lat	Reserved. Does not apply to PCI Express.
23 to 16	Min_Gnt	Reserved. Does not apply to PCI Express.
15 to 8	Interrupt Pin	Specifies the message issued from the INTX_EP_F * pin. 01h: Assert_INTA# (initial value) 02h: Assert_INTB# 03h: Assert_INTC# 04h: Assert_INTD# 05h-FFh: (Reserved)
7 to 0	Interrupt Line	Specifies which interrupt line of the system is connected to the interrupt output of the device. The system initialization program sets the value, and the device driver and OS read the value as required. The register is for use by software; there is no interaction between device operation and this register value.

Table 36.5-98 Valid Reset Signal

Reset Signal	Interrupt Pin	Interrupt Line
RST_LOAD_B	✓	
RST_RSM_B		
RST_CFG_B		✓
FLR		✓

(14) PM Capabilities (Function #n) (PCI_EP_PMC_Fn) (n = 0, 1)

This register indicates various support information.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6040h (Function #0)
<PCI_S0_REG_base> + 7040h (Function #1)

Initial Value: 4803_E001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PME Support					D2 Support	D1 Support	AUX_Current			DSI	Immediate_Readiness_on_Return_to_D0	PME Clock	Version		
Initial Value	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	1
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability ID							
Initial Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-99 PCI_EP_PMC_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 27	PME Support	Indicates whether PME is supported in each device state. xxxx_1b: Supports D0. xxx1_xb: Supports D1. xx1x_xb: Supports D2. x1xx_xb: Supports D3hot. 1xxx_xb: Supports D3cold (not supported).
26	D2 Support	Indicates whether the D2 power management state is supported. 0b: Not supported 1b: Supported
25	D1 Support	Indicates whether the D1 power management state is supported. 0b: Not supported 1b: Supported
24 to 22	AUX_Current	Indicates the 3.3 Vaux auxiliary current (the maximum current provided by auxiliary power). 111b: 375 mA 110b: 320 mA 101b: 250 mA 100b: 220 mA 011b: 160 mA 010b: 100 mA 001b: 55 mA 000b: 0 (self-powered) The reading returns 000b (AUX is not supported).
21	Device Specific Initialization (DSI)	Indicates whether to use DSI (Device Specific Initialization). 0b: Not supported 1b: Supported
20	Immediate_Readiness_on_Return_to_D0	Fixed to 0b.

Table 36.5-99 PCI_EP_PMC_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
19	PME Clock	Reserved. Does not apply to PCI Express
18 to 16	Version	Fixed to 011b. PCI Power Management Interface Specification Rev.1.2
15 to 8	Next Capability Pointer	Indicates the PCI Express Capability start address.
7 to 0	Capability ID	Indicates the PCI Power Management Capability. Fixed to 01h.

Table 36.5-100 Valid Reset Signal

Reset Signal	PME Support	D2 Support	D1 Support	AUX_Current	DSI	Version
RST_LOAD_B	✓	✓	✓	✓	✓	✓
RST_RSM_B						
RST_CFG_B						
FLR						

(15) PM Status/Control (Function #n) (PCI_EP_PMSC_Fn) (n = 0, 1)

This register indicates and controls the PME status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6044h (Function #0)
<PCI_S0_REG_base> + 7044h (Function #1)

Initial Value: 0000_0008h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Data								Bus Power/Clock Control Enable	B2/B3/Support	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PME Status	Data Scale		Data Select				PME Enable	—	—	—	—	No_Soft_Reset	—	PowerState	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W (AXI)	RW1	R	R	R	R	R	R	RW	R	R	R	R	R	R	RW	RW
R/W (PCIe)	RW1	R	R	R	R	R	R	RW	R	R	R	R	R	R	RW	RW

Table 36.5-101 PCI_EP_PMSC_Fn Register Contents

Bit Position	Bit Name	Description
31 to 24	Data	Not supported
23	Bus Power/Clock Control Enable	Not supported
22	B2/B3 Support	Not supported
21 to 16	—	Reserved. These bits are read as 0b.
15	PME Status	Indicates that a PME assertion factor has occurred. It is cleared by writing 1b. Writing 0b has no effect.
14, 13	Data Scale	Not supported
12 to 9	Data Select	Not supported
8	PME Enable	Controls PME assertion. For 1b, PME assertion is enabled. At this time, PME is asserted if PME_status is set. PCI Express handles wake-up processing on links and then transmits a PM_PME message to assert PME. *Note*: According to the value of PME support [4] (PME Support by D3cold), the specification is as follows: PME Support [4] = 1b Reset: RST_RSM_B PME Support [4] = 0b Reset: RST_CFG_B
7 to 4	—	Reserved. These bits are read as 0b.
3	No_Soft_Reset	Indicate that in a power state transition from D3hot to D0, an internal reset is not initiated in the device.
2	—	Reserved. This bit is read as 0b.
1, 0	PowerState	Sets the PCI device state. 00b: D0 (initial value) 01b: D1 (setting prohibited) 10b: D2 (setting prohibited) 11b: D3hot

Table 36.5-102 Valid Reset Signal

Reset Signal	PME Enable	PowerState
RST_LOAD_B		
RST_RSM_B	✓	
RST_CFG_B		✓
FLR	✓	✓

(16) PCI Express Capability (Function #n) (PCI_EP_PCIEC_Fn) (n = 0, 1)

This register indicates the PCIe capability.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6060h (Function #0)
<PCI_S0_REG_base> + 7060h (Function #1)

Initial Value: 0002_0010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	Undefined	Interrupt Message Number					Slot Implemented	Device/Port Type				Capability Version			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W (AXI)	R	R	RW	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability I							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-103 PCI_EP_PCIEC_Fn Register Contents

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b.
30	Undefined	Fixed to 0b.
29 to 25	Interrupt Message Number	Indicates the MSI vector used in the interrupt message associated with any status bit in this capability structure.
24	Slot Implemented	Does not apply to endpoint devices. Fixed to 0b.
23 to 20	Device/Port Type	Indicates a native PCI Express Endpoint device. 0000b PCI Express Endpoint device (initial value) 0001b Legacy PCI Express Endpoint device 0100b Root Port of PCI Express Root Complex 0101b Upstream Port of PCI Express Switch 0110b Downstream Port of PCI Express Switch 0111b PCI Express-to-PCI/PCI-X Bridge 1000b PCI/PCI-X-to-PCI Express Bridge 1001b Root Complex Integrated Endpoint Device 1010b Root Complex Event Collector All other encodings are reserved.
19 to 16	Capability Version	Indicates the PCI Express Capability Structure version. Fixed to 0001b.
15 to 8	Next Capability Pointer	Indicates that this is the last item in the capability list. Fixed to 00h.
7 to 0	Capability ID	Indicates PCI Express capability. Fixed to 10h.

Table 36.5-104 Valid Reset Signal

Reset Signal	Interrupt Message Number	Device/Port Type	Capability Version
RST_LOAD_B	✓	✓	✓
RST_RSM_B			
RST_CFG_B			
FLR			

(17) Device Capabilities (Function #n) (PCI_EP_DEVC_Fn) (n = 0, 1)

This register indicates the device capability.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6064h (Function #0)
<PCI_S0_REG_base> + 7064h (Function #1)

Initial Value: 1000_8FC0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	Function Level Reset Capability	Captured Slot Power Limit Scale		Captured Slot Power Limit Value								—	—
Initial Value	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Role-Based Error Reporting	Undefined			Endpoint L1 Acceptable Latency			Endpoint L0s Acceptable Latency			Extended Tag Field Supported	Phantom Functions Supported		Max_Payload_Size Supported		
Initial Value	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-105 PCI_EP_DEVC_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 29	—	Reserved. These bits are read as 0b.
28	Function Level Reset Capability	Set when the function level reset function is implemented.
27, 26	Captured Slot Power Limit Scale	Indicates the scale of the Captured Slot Power Limit value. Set by the received Set_Slot_Power_Limit Message.
25 to 18	Captured Slot Power Limit Value	Indicates the Slot Power Limit (Watt) value. Set by the received Set_Slot_Power_Limit message.
17, 16	—	Reserved. These bits are read as 0b.
15	Role-Based Error Reporting	Sets 1b when the Error Reporting function (Rev 1.1 or later compliant) is implemented. Fixed to 1b for the PCI Express Base Spec.1 or later.
14 to 12	Undefined	Fixed to 0b.
11 to 9	Endpoint L1 Acceptable Latency	000b: Max 1 µs 001b: Max 2 µs 010b: Max 4 µs 011b: Max 8 µs 100b: Max 16 µs 101b: Max 32 µs 110b: Max 64 µs 111b: No limit (initial value)

Table 36.5-105 PCI_EP_DEVC_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
8 to 6	Endpoint L0s Acceptable Latency	000b: Max 64 ns 001b: Max 128 ns 010b: Max 256 ns 011b: Max 512 ns 100b: Max 1 µs 101b: Max 2 µs 110b: Max 4 µs 111b: No limit (initial value)
5	Extended Tag Field Supported	Extended Tag support. 0b: 5-bit Tag field supported 1b: 8-bit Tag field supported
4, 3	Phantom Functions Supported	Phantom Function is not supported. Fixed to 00b.
2 to 0	Max_Payload_ Size Supported	000b: 128 B max payload size (initial value) 001b: 256 B max payload size 010b: 512 B max payload size 011b: 1024 B max payload size 100b: 2048 B max payload size 101b: 4096 B max payload size 110b: Reserved 111b: Reserved

Table 36.5-106 Valid Reset Signal

Reset Signal	Function Level Reset Capability	Captured Slot Power Limit Scale	Captured Slot Power Limit Value	Endpoint L1 Acceptable Latency	Endpoint L0s Acceptable Latency	Extended Tag Field Supported
RST_LOAD_B	✓			✓	✓	✓
RST_RSM_B						
RST_CFG_B		✓	✓			

Reset Signal	Max_Payload_Size Supported
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	

(18) Device Control/Status (Function #n) (PCI_EP_DEVCS_Fn) (n = 0, 1)

This register controls the device and indicates the device status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6068h (Function #0)
<PCI_S0_REG_base> + 7068h (Function #1)

Initial Value: 0000_2010h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	Emergency Power Reduction Detected	Transaction Pending	AUX Power Detected	Unsupported Request Detected	Fatal Error Detected	Non-Fatal Error Detected	Correctable Error Detected
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	RW1	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Initiate Function Level Reset	Max_Read_Request_Size			Enable No Snoop	AUX Power PM Enable	Phantom Functions Enable	Extended Tag Field Enable	Max_Payload_Size			Enable Relaxed Ordering	Unsupported Request Reporting Enable	Fatal Error Reporting Enable	Non-Fatal Error Reporting Enable	Correctable Error Reporting Enable
Initial Value	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	R	RW	R	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	R	RW	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-107 PCI_EP_DEVCS_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b.
22	Emergency Power Reduction Detected	Not supported. Fixed to 0b.
21	Transaction Pending	Indicates that the transaction is pending because no completion has been received for the transmitted non-posted request. 1b indicates pending.
20	AUX Power Detected	Indicates that auxiliary power was detected (AUX is not supported).
19	Unsupported Request Detected	Indicates that an unsupported request error was detected. 1b indicates that an error was detected. It is cleared by writing 1b during PCIe access, writing 0b has no effect.
18	Fatal Error Detected	Indicates that a fatal error was detected. 1b indicates that an error was detected. It is cleared by writing 1b. Writing 0b has no effect.
17	Non-Fatal Error Detected	Indicates that a non-fatal error was detected. 1b indicates that an error was detected. It is cleared by writing 1b during PCIe access, writing 0b has no effect.
16	Correctable Error Detected	Indicates that a correctable error was detected. 1b indicates that an error was detected. It is cleared by writing 1b during PCIe access, writing 0b has no effect.
15	Initiate Function Level Reset	A write of 1b initiates a function level reset to the Function. The value read by software from this bit is always 0b.

Table 36.5-107 PCI_EP_DEVCS_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
14 to 12	Max_Read_Request_Size	Sets Max_Read_Request_Size. 000b: 128-byte max read request size 001b: 256-byte max read request size 010b: 512-byte max read request size (initial value) 011b: 1024-byte max read request size 100b: 2048-byte max read request size 101b: 4096-byte max read request size 110b: Reserved 111b: Reserved
11	Enable No Snoop	This macro does not use No Snoop Attribute as a requester.
10	Auxiliary (AUX) Power PM Enable	Sets whether to use auxiliary (AUX) power (AUX unsupported).
9	Phantom Functions Enable	Phantom functions are not supported. Fixed to 0b.
8	Extended Tag Field Enable	Extended tags are not supported. Only 5-bit tags are used.
7 to 5	Max_Payload_Size	Sets Max_Payload_Size. 000b: 128-byte max payload size (initial value) 001b: 256-byte max payload size 010b: 512-byte max payload size 011b: 1024-byte max payload size 100b: 2048-byte max payload size 101b: 4096-byte max payload size 110b: Reserved 111b: Reserved
4	Enable Relaxed Ordering	Sets whether to use Snoop Attribute as a requester. 1b: Supported 0b: Not supported
3	Unsupported Request Reporting Enable	Controls the generation of ERR_NONFATAL and ERR_FATAL messages in response to the detection of unsupported requests. 1b enables Message generation.
2	Fatal Error Reporting Enable	Controls the generation of ERR_FATAL messages. 1b enables message generation.
1	Non-Fatal Error Reporting Enable	Controls the generation of ERR_NONFATAL messages. 1b enables message generation.
0	Correctable Error Reporting Enable	Controls the generation of ERR_COR messages. 1b enables message generation.

Table 36.5-108 Valid Reset Signal

Reset Signal	Unsupported Request Detected	Fatal Error Detected	Non-Fatal Error Detected	Correctable Error Detected	Initiate Function Level Reset	Max_Read_Request_Size
RST_LOAD_B						
RST_RSM_B						
RST_CFG_B	✓	✓	✓	✓	✓	✓
FLR	✓	✓	✓	✓		✓

Reset Signal	AUX Power PM Enable	Extended Tag Field Enable	Max_Payload_Size	Enable Relaxed Ordering	Unsupported Request Reporting Enable	Fatal Error Reporting Enable
RST_LOAD_B						
RST_RSM_B	✓					
RST_CFG_B		✓	✓	✓	✓	✓
FLR				✓	✓	✓

Reset Signal	Non-Fatal Error Reporting Enable	Correctable Error Reporting Enable
RST_LOAD_B		
RST_RSM_B		
RST_CFG_B	✓	✓
FLR	✓	✓

(19) Link Capabilities (Function #n) (PCI_EP_LINKC_Fn) (n = 0, 1)

This register indicates the link capabilities.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 606Ch (Function #0)
<PCI_S0_REG_base> + 706Ch (Function #1)

Initial Value: 0043_6C22h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Port Number								—	ASPM Optionality Compliance	Link Bandwidth Notification Capability	Data Link Layer Link Active Reporting Capable	Surprise Down Error Reporting Capable	Clock Power Management	L1 Exit Latency	
Initial Value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	R	RW	R	R	R	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	L1 Exit Latency	L0s Exit Latency			Active State Power Management Support		Maximum Link Width						Max Link Speed			
Initial Value	0	1	1	0	1	1	0	0	0	0	1	0	0	0	1	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-109 PCI_EP_LINKC_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 24	Port Number	Indicates the port number of the PCI Express link.
23	—	Reserved. This bit is read as 0b.
22	ASPM Optionality Compliance	Fixed to 1b.
21	Link Bandwidth Notification Capability	Does not apply to endpoint devices. Fixed to 0b.
20	Data Link Layer Link Active Reporting Capable	Does not apply to endpoint devices. Fixed to 0b.
19	Surprise Down Error Reporting Capable	Does not apply to endpoint devices. Fixed to 0b.
18	Clock Power Management	Indicates whether the CLKREQ# mechanism is supported for L1 and l2/L3 ready. 0b: CLKREQ# mechanism is not supported. 1b: CLKREQ# mechanism is supported.
17 to 15	L1 Exit Latency	000b: Less than 1µs 001b: 1 µs to less than 2 µs 010b: 2 µs to less than 4 µs 011b: 4 µs to less than 8 µs 100b: 8 µs to less than 16 µs 101b: 16 µs to less than 32 µs 110b: 32 µs to 64 µs (initial value) 111b: More than 64 µs

Table 36.5-109 PCI_EP_LINKC_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
14 to 12	L0s Exit Latency	000b: Less than 64 ns 001b: 64 ns to less than 128 ns 010b: 128 ns to less than 256 ns 011b: 256 ns to less than 512 ns 100b: 512 ns to less than 1 µs 101b: 1 µs to less than 2 µs 110b: 2 µs to 4 µs (initial value) 111b: More than 4 µs
11, 10	Active State Power Management (ASPM) Support	00b: No ASPM Support 01b: L0s supported 10b: L0s supported 11b: L0s and L1 supported (initial value)
9 to 4	Maximum Link Width	00_0000b: Reserved 00_0001b: ×1 00_0010b: ×2 (initial value) 00_0100b: ×4 (setting prohibited) 00_1000b: ×8 (setting prohibited) 00_1100b: ×12 (setting prohibited) 01_0000b: ×16 (setting prohibited) 10_0000b: ×32 (setting prohibited)
3 to 0	Max Link Speed	0001b: 2.5 GT/s link speed supported 0010b: 5.0 GT/s and 2.5 GT/s link speeds supported (initial value) All other encodings are reserved.

Table 36.5-110 Valid Reset Signal

Reset Signal	ASPM Optionality Compliance	Clock Power Management	L1 Exit Latency	L0s Exit Latency	Active State Power Management Support	Maximum Link Width
RST_LOAD_B	✓	✓	✓	✓	✓	✓
RST_RSM_B						
RST_CFG_B						
FLR						

Reset Signal	Max Link Speed
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	
FLR	

(20) Link Control/Status (Function #n) (PCI_EP_LINKCS_Fn) (n = 0, 1)

This register controls the link and indicates the link status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6070h (Function #0)
<PCI_S0_REG_base> + 7070h (Function #1)

Initial Value: 1000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Link Autonomous Bandwidth Status	Link Bandwidth Management Status	Data Link Layer Link Active	Slot Clock Configuration	Link Training	—	Negotiated Link Width						Current Link Speed			
Initial Value	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	RW	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Link Autonomous Bandwidth Interrupt Enable	Link Bandwidth Management Interrupt Enable	Hardware Autonomous Width Disable	Enable Clock Power Management	Extended Synch	Common Clock Configuration	Retrain Link	Link Disable	Read Completion Boundary	—	Active State Power Management Control	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	RW	RW	RW	RW	R	R	RW	R	RW	RW
R/W (PCIe)	R	R	R	R	R	R	RW	RW	RW	RW	R	R	RW	R	RW	RW

Table 36.5-111 PCI_EP_LINKCS_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31	Link Autonomous Bandwidth Status	Does not apply to endpoint devices. Fixed to 0b.
30	Link Bandwidth Management Status	Does not apply to endpoint devices. Fixed to 0b.
29	Data Link Layer Link Active	1b indicates that the data link layer is in the link active state.
28	Slot Clock Configuration	Indicates whether to use the reference clock supplied to the connector when using this unit as an add-in card. 0b: Does not use the reference clock for the connector. 1b: Use the reference clock for the connector (initial value).
27	Link Training	Does not apply to endpoint devices. Fixed to 0b.
26	—	Reserved. This bit is read as 0b.
25 to 20	Negotiated Link Width	Indicates the link width established as a result of negotiation. 00_0001b: ×1 00_0010b: ×2 00_0100b: ×4 00_1000b: ×8 00_1100b: ×12 01_0000b: ×16 10_0000b: ×32 All other encodings are reserved.

Table 36.5-111 PCI_EP_LINKCS_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
19 to 16	Current Link Speed	0001b: 2.5GT/s PCI Express Link 0010b: 5.0 GT/s PCI Express Link 0011b: Setting prohibited 0100b: Setting prohibited 0000b during reset period.
15 to 12	—	Reserved. These bits are read as 0b.
11	Link Autonomous Bandwidth Interrupt Enable	Does not apply to endpoint devices. Fixed to 0b.
10	Link Bandwidth Management Interrupt Enable	Does not apply to endpoint devices. Fixed to 0b.
9	Hardware Autonomous Width Disable	Disables a link width change. 0b: Link width change enabled (initial value) 1b: Link width change disabled
8	Enable Clock Power Management	Enable/Disable CLKREQ# mechanism for L1 and L2/L3 ready,
7	Extended Synch	Set to 1b to transmit 4096 FTS ordered sets at the time of a transition from L0s to L0. Also, 1024 TS1 ordered sets are transmitted at the beginning of the recovery state in a transition from L1 to L0. The initial value is 0b.
6	Common Clock Configuration	Sets whether a common reference clock is used for remote nodes. 0b: A non-common reference clock is supplied (initial value). 1b: A common reference clock is supplied.
5	Retrain Link	Does not apply to endpoint devices. Fixed to 0b.
4	Link Disable	Does not apply to endpoint devices. Fixed to 0b.
3	Read Completion Boundary (RCB)	0b: 64 bytes 1b: 128 bytes (initial value)
2	—	Reserved. This bit is read as 0b.
1, 0	Active State Power Management (ASPM) Control	Sets the level of permission for active-state power management. 00b: Disabled (initial value) 01b: L0s entry supported 10b: Reserved 11b: L0s and L1 entry supported

Table 36.5-112 Valid Reset Signal

Reset Signal	Slot Clock Configuration	Hardware Autonomous Width Disable	Enable Clock Power Management	Extended Synch	Common Clock Configuration	Read Completion Boundary
RST_LOAD_B	✓					
RST_RSM_B						
RST_CFG_B		✓	✓	✓	✓	✓
FLR						

Reset Signal	Active State Power Management Control
RST_LOAD_B	
RST_RSM_B	
RST_CFG_B	✓
FLR	

(21) Device Capabilities 2 (Function #n) (PCI_EP_DEVC2_Fn) (n = 0, 1)

This register indicates the device capability.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6084h (Function #0)
<PCI_S0_REG_base> + 7084h (Function #1)

Initial Value: 0000_0012h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	Emergency Power Reduction Initialization Required	Emergency Power Reduction Supported		—	—	—	—	OBFF Supported		10-Bit Tag Requester Supported	10-Bit Tag Completer Supported
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	LTR Mechanism Supported	—	—	—	—	—	—	Completion Timeout Disable Supported	Completion Timeout Ranges Supported			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
R/W (AXI)	R	R	R	R	RW	R	R	R	R	R	R	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-113 PCI_EP_DEVC2_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 27	—	Reserved. These bits are read as 0b.
26	Emergency Power Reduction Initialization Required	Emergency Power Reduction Initialization Required. Not supported. Fixed to 0b.
25, 24	Emergency Power Reduction Supported	Emergency Power Reduction Supported Not supported. Fixed to 0b.
23 to 20	—	Reserved. These bits are read as 0b.
19, 18	OBFF Supported	00b (not supported). No changes allowed
17	10-Bit Tag Requester Supported	10-Bit Tag (Requester) support 0b: Not supported (initial value) 1b: Supported Fixed to 0b.
16	10-Bit Tag Completer Supported	10-Bit Tag (Completer) support 0b: Not supported (initial value) 1b: Supported
15 to 12	—	Reserved. These bits are read as 0b.
11	LTR Mechanism Supported	Sets whether Latency Tolerance Reporting (LTR) is supported. 0b: Not Supported 1b: Supported
10 to 5	—	Reserved. These bits are read as 0b.

Table 36.5-113 PCI_EP_DEVC2_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
4	Completion Timeout Disable Supported	Sets whether the completion timeout disable function is supported. 0b: Not Supported 1b: Supported
3 to 0	Completion Timeout Ranges Supported	Sets the completion timeout range. Range A: 50 µs to 10 ms Range B: 10 ms to 250 ms Range C: 250 ms to 4 s Range D: 4 s to 64 s The above 4 patterns are decided and the following combinations can be set. 0001b: Range A 0010b: Range B 0011b: Ranges A and B 0110b: Ranges B and C 0111b: Ranges A, B, and C 1110b: Ranges B, C and D 1111b: Ranges A, B, C, and D All other encodings are reserved. *Note*: Though initial value described in the UM is 0010b, the initial value should be changed according to the installed system and device performance or indicate the initial value as a product request.

Table 36.5-114 Valid Reset Signal

Reset Signal	OBFF Supported	10-Bit Tag Requester Supported	10-Bit Tag Completer Supported	LTR Mechanism Supported	Completion Timeout Disable Supported	Completion Timeout Ranges Supported
RST_LOAD_B	✓	✓	✓	✓	✓	✓
RST_RSM_B						
RST_CFG_B						
FLR						

(22) Device Control 2/Status 2 (Function #n) (PCI_EP_DEVCS2_Fn) (n = 0, 1)

This register controls device and indicates the device status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6088h (Function #0)
<PCI_S0_REG_base> + 7088h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	OBFF Enable		10-Bit Tag Requester Enable	Emergency Power Reduction	LTR Mechanism Enable	—	—	—	—	—	Completion Timeout Disable	Completion Timeout Value			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	RW	RW	RW	R	RW	R	R	R	R	R	RW	RW	RW	RW	RW
R/W (PCIe)	R	RW	RW	RW	R	RW	R	R	R	R	R	RW	RW	RW	RW	RW

Table 36.5-115 PCI_EP_DEVCS2_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 15	—	Reserved. These bits are read as 0b.
14, 13	OBFF Enable	00b (disabled) No changes allowed. *Note*: These bits are reserved when OBFF Supported = 00b.
12	10-Bit Tag Requester Enable	10-Bit Tag (Requester) enable 0b: Disabled (initial value) 1b: Enabled Not supported. Fixed to 0b.
11	Emergency Power Reduction Request	Emergency Power Reduction Request Not supported. Fixed to 0b.
10	LTR Mechanism Enable	The LTR mechanism is enabled when this bit is set. *Note*: This bit is reserved for Function #1.
9 to 5	—	Reserved. These bits are read as 0b.
4	Completion Timeout Disable	The completion timeout disable function is enabled when this bit is set.

Table 36.5-115 PCI_EP_DEVCS2_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
3 to 0	Completion Timeout Value	Sets Completion Timeout Range. 0000b: 10 ms to 50 ms (initial value) 0001b: 50 µs to 100 µs 0010b: 1 ms to 10 ms 0101b: 16 ms to 55 ms 0110b: 65 ms to 210 ms 1001b: 260 ms to 900 ms 1010b: 1 s to 3.5 s 1101b: 4 s to 13 s 1110b: 17 s to 64 s Others: Reserved (setting prohibited) *Note*: By the initial value 0000b, the time is set longer than the default 50 usec lower limit of Base Spec, but this takes into account the lower limit of 10 msec recommended by Base Spec.

Table 36.5-116 Valid Reset Signal

Reset Signal	OBFF Enable	10-Bit Tag Requester Enable	LTR Mechanism Enable	Completion Timeout Disable	Completion Timeout Value
RST_LOAD_B					
RST_RSM_B					
RST_CFG_B	✓	✓	✓	✓	✓
FLR	✓	✓	✓	✓	✓

(23) Link Capabilities 2 (Function #n) (PCI_EP_LINKC2_Fn) (n = 0, 1)

This register indicates the link capabilities.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 608Ch (Function #0)
<PCI_S0_REG_base> + 708Ch (Function #1)

Initial Value: 0000_0006h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DRS Supported	—	—	—	—	—	—	Two Retimers Presence Detect Supported	Retimer Presence Detect Supported	Lower SKP OS Reception Supported Speeds Vector							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Lower SKP OS Generation Supported Speeds Vector							Crosslink Supported	Supported Link Speeds Vector[6:0]							—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-117 PCI_EP_LINKC2_Fn Register Contents

Bit Position	Bit Name	Description
31	DRS Supported	This function is not supported for this product. Fixed to 0b.
30 to 25	—	Reserved. These bits are read as 0b.
24	Two Retimers Presence Detect Supported	This function is not supported for this product. Fixed to 0b.
23	Retimer Presence Detect Supported	This function is not supported for this product. Fixed to 0b.
22 to 16	Lower SKP OS Reception Supported Speeds Vector	This function is not supported for this product. Fixed to 000_0000b. *Note*: Each function should have the same value.
15 to 9	Lower SKP OS Generation Supported Speeds Vector	This function is not supported for this product. Fixed to 0000_000b. *Note*: Each function should have the same value.
8	Crosslink supported	This function is not supported for this product. Fixed to 0b.
7 to 1	Supported Link Speeds Vector[6:0]	Indicates the supported link speed. Bit [0[: 2.5 GT/s Bit [1]: 5.0 GT/s Others: Reserved
0	—	Reserved. This bit is read as 0b.

Table 36.5-118 Valid Reset Signal

Reset Signal	Two Retimers Presence Detect Supported	Retimer Presence Detect Supported	Lower SKP OS Reception Supported Speeds Vector	Lower SKP OS Generation Supported Speeds Vector	Supported Link Speeds Vector
RST_LOAD_B	✓	✓	✓	✓	✓
RST_RSM_B					
RST_CFG_B					
FLR					

(24) Link Control 2/Status 2 (Function #n) (PCI_EP_LINCS2_Fn) (n = 0, 1)

This register controls the link and indicates the link status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6090h (Function #0)
<PCI_S0_REG_base> + 7090h (Function #1)

Initial Value: 0000_0002h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DRS Message Received	Downstream Component Presence			—	—	Crosslink Resolution		Two Retimers Presence Detected	Retimer Presence Detected	Link Equalization Request	Equalization Phase 3 Successful	Equalization Phase 2 Successful	Equalization Phase 1 Successful	Equalization Complete	Current De-emphasis Level
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	RW	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	RW1	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Compliance Preset/De-emphasis				Compliance SOS	Enter Modified Compliance	Transmit Margin			Selectable De-emphasis	Hardware Autonomous Speed Disable	Enter Compliance	Target Link Speed			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW

Table 36.5-119 PCI_EP_LINCS2_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31	DRS Message Received	This function is not supported for this product. Fixed to 0b.
30 to 28	Downstream Component Presence	This function is not supported for this product. Fixed to 000b.
27, 26	—	Reserved. These bits are read as 0b.
25, 24	Crosslink Resolution	This function is not supported for this product. Fixed to 00b.
23	Two Retimers Presence Detect Supported	This function is not supported for this product. Fixed to 0b.
22	Retimer Presence Detect Supported	This function is not supported for this product. Fixed to 0b.
21	Link Equalization Request	This function is not supported for this product. Fixed to 0b.
20	Equalization Phase 3 Successful	This function is not supported for this product. Fixed to 0b.
19	Equalization Phase 2 Successful	This function is not supported for this product. Fixed to 0b.
18	Equalization Phase 1 Successful	This function is not supported for this product. Fixed to 0b.
17	Equalization Complete	This function is not supported for this product. Fixed to 0b.

Table 36.5-119 PCI_EP_LINCS2_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
16	Current De-emphasis Level	This is a status register indicating the de-emphasis level during Gen2 operation. 1b: −3.5 dB 0b: −6 dB (initial value) *Note*: The initial value after Gen2 linkup is 0b. However, 1b is indicated after Gen1 linkup, but this bit has no meaning in Gen1 and should be ignored.
15 to 12	Compliance Preset/De-emphasis	Sets the de-emphasis level during Polling.Compliance state. 0001b: −3.5 dB 0000b: −6 dB (initial value) *Note*: Reserved for Function #1.
11	Compliance SOS	When this bit is set to 1b, the SKP ordered sets are inserted periodically during transmission of the compliance pattern. *Note*: Reserved for Function #1.
10	Enter Modified Compliance	The configuration bit for transmission of the modified compliance pattern. *Note*: Reserved for Function #1.
9 to 7	Transmit Margin	Adjusts the voltage level. 000b: Normal operating range 001b to 111b: See the corresponding section of the Base Spec. *Note*: Reserved for Function #1.
6	Selectable De-emphasis	Does not applied to endpoint devices. Fixed to 0b.
5	Hardware Autonomous Speed Disable	Controls a link speed change. 1b: Link speed change not supported (disabled) 0b: Link speed change supported (enabled) *Note*: Reserved for Function #1.
4	Enter Compliance	Enables transition to compliance mode by setting 1b. The link speed value at this time is the value set in the Target Link Speed field. *Note*: Reserved for Function #1.
3 to 0	Target Link Speed	Sets the link speed value for indication to the other-party device during training. 0001b: 2.5 GT/s target link speed 0010b: 5.0 GT/s target link speed (initial value) 0011b: 8.0 GT/s target link speed (setting prohibited) 0100b: 16.0 GT/s Target link speed (setting prohibited) All other encodings are reserved *Note*: Reserved for Function #1.

Table 36.5-120 Valid Reset Signal

Reset Signal	Link Equalization Request	Compliance Preset/De-emphasis	Compliance SOS	Enter Modified Compliance	Transmit Margin	Hardware Autonomous Speed Disable
RST_LOAD_B						
RST_RSM_B	✓	✓	✓	✓	✓	✓
RST_CFG_B						
FLR						

Reset Signal	Enter Compliance	Target Link Speed
RST_LOAD_B		
RST_RSM_B	✓	✓
RST_CFG_B		
FLR		

(25) Base Address Register Mask00 (Lower) (Function #n) (PCI_EP_BARMSK00L_Fn) (n = 0, 1)

This register indicates mask information for Base Address Register 0 (BAR0).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60A0h (Function #0)
<PCI_S0_REG_base> + 70A0h (Function #1)

Initial Value: 0FFF_FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register Mask00 (Lower)															
Initial Value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register Mask00 (Lower)															
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-121 PCI_EP_BARMSK00L_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register Mask00 (Lower)	The mask register for Base Address Register 0 (BAR0). The initial value is decided by the configurable parameter.

Table 36.5-122 Valid Reset Signal

Reset Signal	Base Address Register Mask00 (Lower)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	
FLR	

(26) Base Address Register Mask00 (Upper) (Function #n) (PCI_EP_BARMSK00U_Fn) (n = 0, 1)

This register indicates mask information for Base Address Register 1 (BAR1).

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60A4h (Function #0)
<PCI_S0_REG_base> + 70A4h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register Mask00 (Upper)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register Mask00 (Upper)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-123 PCI_EP_BARMSK00U_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register Mask00 (Upper)	The mask register for Base Address Register 1 (BAR1). The initial value is decided by the configurable parameter.

Table 36.5-124 Valid Reset Signal

Reset Signal	Base Address Register Mask00 (Upper)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	
FLR	

(27) Base Address Register Mask01 (Lower) (Function #n) (PCI_EP_BARMSK01L_Fn) (n = 0, 1)

This register is not used.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60A8h (Function #0)
<PCI_S0_REG_base> + 70A8h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register Mask01 (Lower)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register Mask01 (Lower)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-125 PCI_EP_BARMSK01L_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register Mask01 (Lower)	The mask register for Base Address Register 2 (BAR2). The initial value is decided by the configurable parameter.

Table 36.5-126 Valid Reset Signal

Reset Signal	Base Address Register Mask01 (Lower)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	
FLR	

(28) Base Address Register Mask01 (Upper) (Function #n) (PCI_EP_BARMSK01U_Fn) (n = 0, 1)

This register is not used.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60ACh (Function #0)
<PCI_S0_REG_base> + 70ACh (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register Mask01 (Upper)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register Mask01 (Upper)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-127 PCI_EP_BARMSK01U_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register Mask01 (Upper)	The mask register for Base Address Register 3 (BAR3). The initial value is decided by the configurable parameter.

Table 36.5-128 Valid Reset Signal

Reset Signal	Base Address Register Mask01 (Lower)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	
FLR	

(29) Base Address Register Mask02 (Lower) (Function #n) (PCI_EP_BARMSK02L_Fn) (n = 0, 1)

This register is not used.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60B0h (Function #0)
<PCI_S0_REG_base> + 70B0h (Function #1)

Initial Value: 0000_1FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register Mask02 (Lower)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register Mask02 (Lower)															
Initial Value	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-129 PCI_EP_BARMSK02L_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register Mask02 (Lower)	The mask register for Base Address Register 4 (BAR4). The initial value is decided by the configurable parameter.

Table 36.5-130 Valid Reset Signal

Reset Signal	Base Address Register Mask02 (Lower)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	
FLR	

(30) Base Address Register Mask02 (Upper) (Function #n) (PCI_EP_BARMSK02U_Fn) (n = 0, 1)

This register is not used.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60B4h (Function #0)
<PCI_S0_REG_base> + 70B4h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Base Address Register Mask02 (Upper)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Base Address Register Mask02 (Upper)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-131 PCI_EP_BARMSK02U_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Base Address Register Mask02 (Upper)	The mask register for Base Address Register 5 (BAR5). The initial value is decided by the configurable parameter.

Table 36.5-132 Valid Reset Signal

Reset Signal	Base Address Register Mask01 (Upper)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	
FLR	

(31) Base Size 00/01 (Function #n) (PCI_EP_BSIZE00_01_Fn) (n = 0, 1)

This register sets the acceptable TLP size.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60C8h (Function #0)
<PCI_S0_REG_base> + 70C8h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	Base Size 01									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Base Size 00									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-133 PCI_EP_BSIZE00_01_Fn Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved. These bits are read as 0b.
25 to 16	Base Size 01	Sets the size of TLP (DW Size) accepted by Address Space xx set by Base Address Register and Base Address Mask Register. When a TLP with a packet length greater than the size set in these bits is received, even if it is smaller than the max payload size, a completer abort error (CA) is detected. Note that the initial value is 00_0000_0000b and this function is invalid in this case.
15 to 10	—	Reserved. These bits are read as 0b.
9 to 0	Base Size 00	Sets the size of TLP (DW Size) accepted by Address Space xx set by Base Address Register and Base Address Mask Register. When a TLP with a packet length greater than the size set in these bits is received, even if it is smaller than the max payload size, a completer abort error (CA) is detected. Note that the initial value is 00_0000_0000b and this function is invalid in this case.

Table 36.5-134 Valid Reset Signal

Reset Signal	Base Size 01	Base Size 00
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		
FLR		

(32) Base Size 02/03 (Function #n) (PCI_EP_BSIZE02_03_Fn) (n = 0, 1)

This register sets the acceptable TLP size.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60CCh (Function #0)
<PCI_S0_REG_base> + 70CCh (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	Base Size 03									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Base Size 02									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-135 PCI_EP_BSIZE02_03_Fn Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved. These bits are read as 0b.
25 to 16	Base Size 03	Sets the size of TLP (DW Size) accepted by Address Space xx set by Base Address Register and Base Address Mask Register. When a TLP with a packet length greater than the size set in these bits is received, even if it is smaller than the max payload size, a completer abort error (CA) is detected. Note that the initial value is 00_0000_0000b and this function is invalid in this case.
15 to 10	—	Reserved. These bits are read as 0b.
9 to 0	Base Size 02	Sets the size of TLP (DW Size) accepted by Address Space xx set by Base Address Register and Base Address Mask Register. When a TLP with a packet length greater than the size set in these bits is received, even if it is smaller than the max payload size, a completer abort error (CA) is detected. Note that the initial value is 00_0000_0000b and this function is invalid in this case.

Table 36.5-136 Valid Reset Signal

Reset Signal	Base Size 03	Base Size 02
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		
FLR		

(33) Base Size 04/05 (Function #n) (PCI_EP_BSIZE04_05_Fn) (n = 0, 1)

This register sets the acceptable TLP size.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60D0h (Function #0)
<PCI_S0_REG_base> + 70D0h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	Base Size 05									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Base Size 04									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-137 PCI_EP_BSIZE04_05_Fn Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved. These bits are read as 0b.
25 to 16	Base Size 05	Sets the size of TLP (DW Size) accepted by Address Space 05 set by Base Address Register and Base Address Mask Register. When a TLP with a packet length greater than the size set in these bits is received, even if it is smaller than the max payload size, a completer abort error (CA) is detected. Note that the initial value is 00_0000_0000b and this function is invalid in this case.
15 to 10	—	Reserved. These bits are read as 0b.
9 to 0	Base Size 04	Sets the size of TLP (DW Size) accepted by Address Space 04 set by Base Address Register and Base Address Mask Register. When a TLP with a packet length greater than the size set in these bits is received, even if it is smaller than the max payload size, a completer abort error (CA) is detected. Note that the initial value is 00_0000_0000b and this function is invalid in this case.

Table 36.5-138 Valid Reset Signal

Reset Signal	Base Size 05	Base Size 04
RST_LOAD_B	✓	✓
RST_RSM_B		
RST_CFG_B		
FLR		

(34) Base Size 06 (Function #n) (PCI_EP_BSIZE06_Fn) (n = 0, 1)

This register sets the acceptable TLP size.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60D4h (Function #0)
<PCI_S0_REG_base> + 70D4h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Base Size 06									
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-139 PCI_EP_BSIZE06_Fn Register Contents

Bit Position	Bit Name	Description
31 to 10	—	Reserved. These bits are read as 0b.
9 to 0	Base Size 06	Sets the size of TLP (DW Size) accepted by Address Space 06 set by Base Address Register and Base Address Mask Register. When a TLP with a packet length greater than the size set in these bits is received, even if it is smaller than the max payload size, a completer abort error (CA) is detected. Note that the initial value is 00_0000_0000b and this function is invalid in this case.

Table 36.5-140 Valid Reset Signal

Reset Signal	Base Size 06
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	
FLR	

(35) Type Supported 00/01/02 (Function #n) (PCI_EP_TSUPPORT00_01_02_Fn) (n = 0, 1)

This register indicates the transaction type which can be supported by the memory space.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60D8h (Function #0)
<PCI_S0_REG_base> + 70D9h (Function #1)

Initial Value: 0033_3333h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Debug								Type Supported 02							
Initial Value	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Type Supported 01								Type Supported 00[7:0]							
Initial Value	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-141 PCI_EP_TSUPPORT00_01_02_Fn Register Contents

Bit Position	Bit Name	Description
31 to 24	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
23 to 16	Type Supported 02	Sets the transaction type which can be supported by Space02 (CFG_SPACE02_BASE). The meaning of each bit is indicated as follows
15 to 8	Type Supported 01	Sets the transaction type which can be supported by Space01 (CFG_SPACE01_BASE). The meaning of each bit is indicated as follows
7 to 0	Type Supported 00[7:0]	Sets the transaction type which can be supported by Space00 (CFG_SPACE00_BASE). The meaning of each bit is indicated as follows

Note: Bit 0: 32-bit memory read
Bit 1: 64-bit memory read
Bit 2: 32-bit memory read lock
Bit 3: 64-bit memory read lock
Bit 4: 32-bit memory write
Bit 5: 64-bit memory write
Bit 6: IO read
Bit 7: IO write

Table 36.5-142 Valid Reset Signal

Reset Signal	Debug	Type Supported 02	Type Supported 01	Type Supported 00
RST_LOAD_B	✓	✓	✓	✓
RST_RSM_B				
RST_CFG_B				
FLR				

(36) MSI Capability (Function #n) (PCI_EP_MSICAP_Fn) (n = 0, 1)

This register specifies the MSI Capability.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60E0h (Function #0)
<PCI_S0_REG_base> + 70E0h (Function #1)

Initial Value: 018A_6005h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	Extended Message Data Enable	Extended Message Data Capable	Per-vector masking capable	64bit Address Capable	Multiple Message Enable			Multiple Message Capable			MSI Enable
Initial Value	0	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	RW	RW	RW	R	R	R	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	RW	RW	RW	R	R	R	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability ID							
Initial Value	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-143 PCI_EP_MSICAP_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 27	—	Reserved. These bits are read as 0b.
26	Extended Message Data Enable	Not supported. Fixed to 0b.
25	Extended Message Data Capable	Not supported. Fixed to 0b.
24	Per-vector masking capable	Indicates that MSI per-vector masking is supported.
23	64bit Address Capable	Indicates that a 64-bit address MSI message can be generated. Fixed to 1b.
22 to 20	Multiple Message Enable	Enables generation of multiple messages and sets the number. 101b (32) can be set as a software setting because 101b is specified in the Multiple Message Capable field. 000b: 1 (initial value) 001b: 2 010b: 4 011b: 8 100b: 16 101b: 32 110b: Reserved 111b: Reserved
19 to 17	Multiple Message Capable	000b: 1 001b: 2 010b: 4 011b: 8 100b: 16 101b: 32 (initial value) 110b: Reserved 111b: Reserved
16	MSI Enable	Enables generation of MSI messages. Enables generation at 1b.

Table 36.5-143 PCI_EP_MSICAP_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
15 to 8	Next Capability Pointer	Indicates the start address of the PCI Express capability. Initial value: 60h
7 to 0	Capability ID	Indicates the MSI capability. Fixed to 05h.

Table 36.5-144 Valid Reset Signal

Reset Signal	Multiple Message Enable	MSI Enable
RST_LOAD_B		
RST_RSM_B		
RST_CFG_B	✓	✓
FLR	✓	✓

(37) Message Address (Function #n) (PCI_EP_MSGADR_Fn) (n = 0, 1)

This register sets the destination address of MSI messages.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60E4h (Function #0)
<PCI_S0_REG_base> + 70E4h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Message Address															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Message Address														—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R

Table 36.5-145 PCI_EP_MSGADR_Fn Register Contents

Bit Position	Bit Name	Description
31 to 2	Message Address	Sets the destination address bits [31:2] of MSI messages.
1, 0	—	Reserved. These bits are read as 0b.

Table 36.5-146 Valid Reset Signal

Reset Signal	Message Address
RST_LOAD_B	
RST_RSM_B	
RST_CFG_B	✓
FLR	✓

(38) Message Upper Address (Function #n) (PCI_EP_MSGUADR_Fn) (n = 0, 1)

This register sets the upper destination address of MSI messages.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60E8h (Function #0)
<PCI_S0_REG_base> + 70E8h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Message Upper Address															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Message Upper Address															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-147 PCI_EP_MSGUADR_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Mask Bits	Setting the bit to 1b masks the transmission of messages as vectors.

Table 36.5-148 Valid Reset Signal

Reset Signal	Mask Bits
RST_LOAD_B	
RST_RSM_B	
RST_CFG_B	✓
FLR	✓

(39) Message Data (Function #n) (PCI_EP_MSGDAT_Fn) (n = 0, 1)

This register sets the upper destination address of MSI messages.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60ECh (Function #0)
<PCI_S0_REG_base> + 70ECh (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Extended Message Data															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Message Data															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-149 PCI_EP_MSGDAT_Fn Register Contents

Bit Position	Bit Name	Description
31 to 16	Extended Message Data	Not supported. Fixed to 0000h.
15 to 0	Message Data	Set data to be set in MSI messages. When the Multiple Message Enable field is 011b (8), the function (AXI) can change the lower 3 bits of message data and notify the system of 8 vectors as message data. Similarly, when the value is 010b (4), the function (AXI) can change the lower 2 bits to notify 4 vectors. When the value is 001b (2), the function (AXI) can change the lower 1 bit to notify 2 vectors. When it is 000b (1), the function (AXI) can notify only 1 vector. *Note*: The invalid upper bits of the function specification data (for example, in the case of above Multiple Message Enable setting 4, the upper bits except the lower 2 bits changed by Function) should specify 0b.

Table 36.5-150 Valid Reset Signal

Reset Signal	Message Data
RST_LOAD_B	
RST_RSM_B	
RST_CFG_B	✓
FLR	✓

(40) Mask Bits (Function #n) (PCI_EP_MSKBIT_Fn) (n = 0, 1)

This register masks the transmission of messages as vectors.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60F0h (Function #0)
<PCI_S0_REG_base> + 70F0h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Mask Bits															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Mask Bits															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 36.5-151 PCI_EP_MSKBIT_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Mask Bits	1b masks the transmission of messages as vectors.

(41) Pending Bits (Function #n) (PCI_EP_PENDBIT_Fn) (n = 0, 1)

This register indicates the pending state of an MSI message for the given function.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 60F4h (Function #0)
<PCI_S0_REG_base> + 70F4h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Pending Bits															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Pending Bits															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-152 PCI_EP_PENDBIT_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Pending Bits	Indicates the pending state of an MSI message for the given function.

(42) Advanced Error Reporting Capability (Function #n) (PCI_EP_ADVERC_Fn) (n = 0, 1)

This register indicates the advanced error reporting capability.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6100h (Function #0)
<PCI_S0_REG_base> + 7100h (Function #1)

Initial Value: 1501_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Next Capability Offset												Capability Version			
Initial Value	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	1
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCI Express Extended Capability ID															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-153 PCI_EP_ADVERC_Fn Register Contents

Bit Position	Bit Name	Description
31 to 20	Next Capability Offset	Indicates the start address of the device serial number capability. This register can be written during initialization. The lower 2 bits are fixed to 00b
19 to 16	Capability Version	Indicates the version number of the capability structure. Initial value: 0001b.
15 to 0	PCI Express Extended Capability ID	Indicates the advanced error reporting capability. Initial value: 0001h.

Table 36.5-154 Valid Reset Signal

Reset Signal	Capability Version
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	
FLR	

(43) Uncorrectable Error Status Register (Function #n) (PCI_EP_UNCESTS_Fn) (n = 0, 1)

This register indicates the uncorrectable error status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6104h (Function #0)
<PCI_S0_REG_base> + 7104h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	ACS Violation Status	Unsupported Request Error Status	ECRC Error Status	Malformed TLP Status	Receiver Overflow Status	Unexpected Completion Status
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	RW1	RW1	RW1	RW1	RW1
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	RW1	RW1	RW1	RW1	RW1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Completer Abort Status	Completion Timeout Status	Flow Control Protocol Error Status	Poisoned TLP Received Status	—	—	—	—	—	—	Surprise Down Error Status	Data Link Protocol Error Status	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW1	RW1	R	RW1	R	R	R	R	R	R	R	RW1	R	R	R	R
R/W (PCIe)	RW1	RW1	R	RW1	R	R	R	R	R	R	R	RW1	R	R	R	R

Table 36.5-155 PCI_EP_UNCESTS_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b.
21	ACS Violation Status	ACS is not supported. Fixed to 0b.
20	Unsupported Request Error Status	Indicates that an unsupported TLP was received. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
19	ECRC Error Status (Optional)	Indicates that an ECRC error was received. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
18	Malformed TLP Status	Indicates that a malformed TLP was received. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected. 1b: Error detected
17	Receiver Overflow Status (Optional)	Indicates that a TLP larger than the free credit in the receive buffer was received. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
16	Unexpected Completion Status	Indicates that a completion response was received but there is no record of transmission of the corresponding non-posted request (due to a mismatch with the transaction descriptor). It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected

Table 36.5-155 PCI_EP_UNCESTS_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
15	Completer Abort Status (Optional)	Indicates that the completion status returned a completion with Completer Abort (CA) status after the transmission of a non-posted request. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
14	Completion Timeout Status	Indicates that the corresponding completion response was not received within the specified time after the transmission of a non-posted request. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
13	Flow Control Protocol Error Status (Optional)	Not Implemented (fixed to 0b)
12	Poisoned TLP Received Status	Indicates that a poisoned TLP (which has a payload and the EP field of header is 1b) was received. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
11 to 6	—	Reserved. These bits are read as 0b.
5	Surprise Down Error Status (Optional)	Not Implemented (fixed to 0b)
4	Data Link Protocol Error Status	Indicates that a sequence number error was detected in the data link layer. It is cleared by writing 1b. Writing 0b has no effect. 0b: No error detected 1b: Error detected
3 to 0	—	Reserved. These bits are read as 0b.

Table 36.5-156 Valid Reset Signal

Reset Signal	Unsupported Request Error Status	ECRC Error Status	Malformed TLP Status	Receiver Overflow Status	Unexpected Completion Status	Completer Abort Status
RST_LOAD_B						
RST_RSM_B	✓	✓	✓	✓	✓	✓
RST_CFG_B						
FLR						

Reset Signal	Completion Timeout Status	Poisoned TLP Received Status	Data Link Protocol Error Status
RST_LOAD_B			
RST_RSM_B	✓	✓	✓
RST_CFG_B			
FLR			

(44) Uncorrectable Error Mask Register (Function #n) (PCI_EP_UNCEMASK_Fn) (n = 0, 1)

This register masks the uncorrectable error status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6108h (Function #0)
<PCI_S0_REG_base> + 7108h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	ACS Violation Mask	Unsupported Request Error Mask	ECRC Error Mask	Malformed TLP Mask	Receiver Overflow Mask	Unexpected Completion Mask
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Completer Abort Mask	Completion Timeout Mask	Flow Control Protocol Error Mask	Poisoned TLP Received Mask	—	—	—	—	—	—	Surprise Down Error Mask	Data Link Protocol Error Mask	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	R	RW	R	R	R	R	R	R	R	RW	R	R	R	R
R/W (PCIe)	RW	RW	R	RW	R	R	R	R	R	R	R	RW	R	R	R	R

Table 36.5-157 PCI_EP_UNCEMASK_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b.
21	ACS Violation Mask	ACS is not supported. Fixed to 0b.
20	Unsupported Request Error Mask	Masks error notification to the root complex if an unsupported request error is detected. 0b: No masking 1b: Mask error message transmission, logging of the header in the Header Log register, and updating of the first error pointer.
19	ECRC Error Mask (Optional)	Masks error notification to the root complex if an ECRC error is detected. 0b: No masking 1b: Masking
18	Malformed TLP Mask	Masks error notification to the root complex if a malformed TLP error is detected. 0b: No masking 1b: Mask error message transmission, logging of the header in the Header Log register, and updating of the first error pointer.
17	Receiver Overflow Mask (Optional)	Masks error notification to the root complex if a receiver overflow error is detected. 0b: No masking 1b: Mask error message transmission and updating of the first error pointer.
16	Unexpected Completion Mask	Masks error notification to the root complex if an unexpected completion error is detected. 0b: No masking 1b: Mask error message transmission, logging of the header in the Header Log register, and updating of the first error pointer.
15	Completer Abort Mask (Optional)	Masks error notification to the root complex if a completer abort error is detected. 0b: No masking 1b: Mask error message transmission, logging of the header in the Header Log register, and updating of the first error pointer.

Table 36.5-157 PCI_EP_UNCEMASK_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
14	Completion Timeout Mask	Masks error notification to the root complex if a completion timeout error is detected. 0b: No masking 1b: Mask error message transmission and updating of the first error pointer.
13	Flow Control Protocol Error Mask (Optional)	Not Implemented (fixed to 0b)
12	Poisoned TLP Received Mask	Masks error notification to the root complex if a poisoned TLP error is detected. 0b: No masking 1b: Mask error message transmission, logging of the header in the Header Log register, and updating of the first error pointer.
11 to 6	—	Reserved. These bits are read as 0b.
5	Surprise Down Error Mask (Optional)	Not Implemented (fixed to 0b)
4	Data Link Protocol Error Mask	Masks error notification to the root complex if a data link protocol error is detected. 0b: No masking 1b: Mask error message transmission and updating of the first error pointer.
3 to 0	—	Reserved. These bits are read as 0b.

Table 36.5-158 Valid Reset Signal

Reset Signal	Unsupported Request Error Mask	ECRC Error Mask	Malformed TLP Mask	Receiver Overflow Mask	Unexpected Completion Mask	Completer Abort Mask
RST_LOAD_B						
RST_RSM_B	✓	✓	✓	✓	✓	✓
RST_CFG_B						
FLR						

Reset Signal	Completion Timeout Mask	Poisoned TLP Received Mask	Data Link Protocol Error Mask
RST_LOAD_B			
RST_RSM_B	✓	✓	✓
RST_CFG_B			
FLR			

(45) Uncorrectable Error Severity Register (Function #n) (PCI_EP_UNCESVY_Fn) (n = 0, 1)

This register sets the uncorrectable error severity.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 610Ch (Function #0)
<PCI_S0_REG_base> + 710Ch (Function #1)

Initial Value: 0046_2030h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	Debug	ACS Violation Severity	Unsupported Request Error Severity	ECRC Error Severity	Malformed TLP Severity	Receiver Overflow Severity	Unexpected Completion Severity
Initial Value	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	RW	R	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Completer Abort Severity	Completion Timeout Severity	Flow Control Protocol Error Severity	Poisoned TLP Received Severity	—	—	—	—	—	—	Surprise Down Error Severity	Data Link Protocol Error Severity	—	—	—	—
Initial Value	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0
R/W (AXI)	RW	RW	R	RW	R	R	R	R	R	R	R	RW	R	R	R	R
R/W (PCIe)	RW	RW	R	RW	R	R	R	R	R	R	R	RW	R	R	R	R

Table 36.5-159 PCI_EP_UNCESVY_Fn Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b.
22	Debug	This register is for use in debugging by Renesas. Note that a change from the initial value may lead to a malfunction.
21	ACS Violation Severity	ACS is not supported. Fixed to 0b.
20	Unsupported Request Error Severity	Sets the severity of the error for detection of an unsupported request error. 0b: Non-fatal error 1b: Fatal error
19	ECRC Error Severity (Optional)	Sets the severity of the error for an ECRC Error. 0b: Non-fatal error 1b: Fatal error
18	Malformed TLP Severity	Sets the severity of the error for a malformed TLP error. 0b: Non-fatal error 1b: Fatal error
17	Receiver Overflow Severity (Optional)	Sets the severity of the error for a receiver overflow error. 0b: Non-fatal error 1b: Fatal error
16	Unexpected Completion Severity	Sets the severity of the error for an unexpected completion error. 0b: Non-fatal error 1b: Fatal error
15	Completer Abort Severity (Optional)	Sets the severity of the error for a completer abort error. 0b: Non-fatal error 1b: Fatal error
14	Completion Timeout Severity	Sets the severity of the error for a completion timeout error. 0b: Non-fatal error 1b: Fatal error

Table 36.5-159 PCI_EP_UNCESVY_Fn Register Contents (2/2)

Bit Position	Bit Name	Description
13	Flow Control Protocol Error Severity (Optional)	Not Implemented (fixed to 0b)
12	Poisoned TLP Received Severity	Sets the severity of the error for a poisoned TLP error. 0b: Non-fatal error 1b: Fatal error
11 to 6	—	Reserved. These bits are read as 0b.
5	Surprise Down Error Severity (Optional)	Not Implemented (fixed to 0b)
4	Data Link Protocol Error Severity	Sets the severity of the error for a data link protocol error. 0b: Non-fatal error 1b: Fatal error
3 to 0	—	Reserved. These bits are read as 0b.

Table 36.5-160 Valid Reset Signal

Reset Signal	Debug	Unsupported Request Error Severity	ECRC Error Severity	Malformed TLP Severity	Receiver Overflow Severity	Unexpected Completion Severity
RST_LOAD_B	✓					
RST_RSM_B		✓	✓	✓	✓	✓
RST_CFG_B						
FLR						

Reset Signal	Completer Abort Severity	Completion Timeout Severity	Poisoned TLP Received Severity	Data Link Protocol Error Severity
RST_LOAD_B				
RST_RSM_B	✓	✓	✓	✓
RST_CFG_B				
FLR				

(46) Correctable Error Status Register (Function #n) (PCI_EP_CESTS_Fn) (n = 0, 1)

This register indicates the correctable error status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6110h (Function #0)
<PCI_S0_REG_base> + 7110h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	Advisory Non-Fatal Error Status	Replay Timer Timeout Status	—	—	—	REPLAY_NUM Rollover Status	Bad DLLP Status	Bad TLP Status	—	—	—	—	—	Receiver Error Status
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	RW1	RW1	R	R	R	RW1	RW1	RW1	R	R	R	R	R	RW1

Table 36.5-161 PCI_EP_CESTS_Fn Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved. These bits are read as 0b.
13	Advisory Non-Fatal Error Status	Indicates that an advisory non-fatal error was detected. It is cleared by writing 1b during pcie. Writing 0b has no effect. 0b: No error detected 1b: Error detected
12	Replay Timer Timeout Status	Indicates that a timeout error has occurred when an Ack or Nak DLLP was not received within the specified time after the transmission of a TLP. It is cleared by writing 1b during pcie. Writing 0b has no effect. 0b: No error detected 1b: Error detected
11 to 9	—	Reserved. These bits are read as 0b.
8	REPLAY_NUM Rollover Status	Indicates that REPLAY_NUM has rolled over from 11b to 00b when replays occurred four times consecutively. It is cleared by writing 1b during pcie. Writing 0b has no effect. 0b: No error detected 1b: Error detected
7	Bad DLLP Status	Indicates that a CRC error of DLLP was detected. It is cleared by writing 1b during pcie. Writing 0b has no effect. 0b: No error detected 1b: Error detected
6	Bad TLP Status	Indicates that a CRC error or a sequence number error was detected. It is cleared by writing 1b during pcie. Writing 0b has no effect. 0b: No error detected 1b: Error detected
5 to 1	—	Reserved. These bits are read as 0b.
0	Receiver Error Status (optional)	It is cleared by writing 1b during pcie. Writing 0b has no effect. 0b: No error detected 1b: Error detected

Table 36.5-162 Valid Reset Signal

Reset Signal	Advisory Non-Fatal Error Status	Replay Timer Timeout Status	REPLAY_NUM Rollover Status	Bad DLLP Status	Bad TLP Status	Receiver Error Status
RST_LOAD_B						
RST_RSM_B	✓	✓	✓	✓	✓	✓
RST_CFG_B						
FLR						

(47) Correctable Error Mask Register (Function #n) (PCI_EP_CEMASK_Fn) (n = 0, 1)

This register masks the correctable error status.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6114h (Function #0)
<PCI_S0_REG_base> + 7114h (Function #1)

Initial Value: 0000_2000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	Advisory Non-Fatal Error Mask	Replay Timer Timeout Mask	—	—	—	REPLAY_NUM Rollover Mask	Bad DLLP Mask	Bad TLP Mask	—	—	—	—	—	Receiver Error Mask
Initial Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	RW	RW	R	R	R	RW	RW	RW	R	R	R	R	R	RW
R/W (PCIe)	R	R	RW	RW	R	R	R	RW	RW	RW	R	R	R	R	R	RW

Table 36.5-163 PCI_EP_CEMASK_Fn Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved. These bits are read as 0b.
13	Advisory Non-Fatal Error Mask	Error notification is masked if an advisory non-fatal error is detected. 0b: No masking 1b: Masks advisory non-fatal error handling (masks updating of the first error pointer and logging of the header, and error message transmission).
12	Replay Timer Timeout Mask	Error notification is masked if a replay timer timeout error is detected. 0b: No masking 1b: Masks error message transmission.
11 to 9	—	Reserved. These bits are read as 0b.
8	REPLAY_NUM Rollover Mask	Error notification is masked if a REPLAY_NUM rollover error is detected. 0b: No masking 1b: Masks error message transmission.
7	Bad DLLP Mask	Error notification is masked if a bad DLLP error is detected. 0b: No masking 1b: Masks error message transmission.
6	Bad TLP Mask	Error notification is masked if a bad TLP error is detected. 0b: No masking 1b: Masks error message transmission.
5 to 1	—	Reserved. These bits are read as 0b.
0	Receiver Error Mask (optional)	0b: No masking 1b: Masks error message transmission.

Table 36.5-164 Valid Reset Signal

Reset Signal	Advisory Non-Fatal Error Mask	Replay Timer Timeout Mask	REPLAY_NUM Rollover Mask	Bad DLLP Mask	Bad TLP Mask	Receiver Error Mask
RST_LOAD_B						
RST_RSM_B	✓	✓	✓	✓	✓	✓
RST_CFG_B						
FLR						

(48) Advanced Error Capabilities and Control Register (Function #n) (PCI_EP_ADVECC_Fn) (n = 0, 1)

This register indicates and controls the advanced error capabilities.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6118h (Function #0)
<PCI_S0_REG_base> + 7118h (Function #1)

Initial Value: 0000_00A0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ECRC Check Enable	ECRC Check Capable	ECRC Generation Enable	ECRC Generation Capable	First Error Pointer				
Initial Value	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	RW	R	RW	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	RW	R	RW	R	R	R	R	R	R

Table 36.5-165 PCI_EP_ADVECC_Fn Register Contents

Bit Position	Bit Name	Description
31 to 9	—	Reserved. These bits are read as 0b.
8	ECRC Check Enable	Enables ECRC checking. 0b: Disabled (initial value) 1b: Enabled
7	ECRC Check Capable	Indicates whether ECRC checking is implemented. 0b: No ECRC checking 1b: ECRC checking is implemented (initial value).
6	ECRC Generation Enable	Enables ECRC generation. 0b: Disabled (initial value) 1b: Enabled
5	ECRC Generation Capable	Indicates whether ECRC generation is implemented. 0b: No ECRC generation 1b: ECRC generation is implemented (initial value).
4 to 0	First Error Pointer	Indicates the filed value of the Uncorrectable Error Status register for the first uncorrectable error detection.

Note: First Error Pointer bits [4:0] are reset by RST_GP_B.

Table 36.5-166 Valid Reset Signal

Reset Signal	ECRC Check Enable	ECRC Generation Enable
RST_LOAD_B		
RST_RSM_B	✓	✓
RST_CFG_B		
FLR		

(49) Header Log Register 0 (Function #n) (PCI_EP_HLOG0_Fn) (n = 0, 1)

This register indicates the header log.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 611Ch (Function #0)
<PCI_S0_REG_base> + 711Ch (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Header of TLP associated with error 0															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Header of TLP associated with error 0															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-167 PCI_EP_HLOG0_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Header of TLP associated with error 0	Indicates the 1st DW of the header where the first uncorrectable error was detected.

(50) Header Log Register 1 (Function #n) (PCI_EP_HLOG1_Fn) (n = 0, 1)

This register indicates the header log.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6120h (Function #0)
<PCI_S0_REG_base> + 7120h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Header of TLP associated with error 1															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Header of TLP associated with error 1															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-168 PCI_EP_HLOG1_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Header of TLP associated with error 1	Indicates the 2nd DW of the header where the first uncorrectable error was detected.

(51) Header Log Register 2 (Function #n) (PCI_EP_HLOG2_Fn) (n = 0, 1)

This register indicates the header log.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6124h (Function #0)
<PCI_S0_REG_base> + 7124h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Header of TLP associated with error 2															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Header of TLP associated with error 2															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-169 PCI_EP_HLOG2_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Header of TLP associated with error 2	Indicates the 3rd DW of the header where the first uncorrectable error was detected.

(52) Header Log Register 3 (Function #n) (PCI_EP_HLOG3_Fn) (n = 0, 1)

This register indicates the header log.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6128h (Function #0)
<PCI_S0_REG_base> + 7128h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Header of TLP associated with error 3															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Header of TLP associated with error 3															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-170 PCI_EP_HLOG3_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	Header of TLP associated with error 3	Indicates the 4th DW of the header where the first uncorrectable error was detected.

(53) Device Serial Number Extended Capability Register (Function #n) (PCI_EP_DEVSNEXTC_Fn) (n = 0, 1)

This register specifies the device serial number extended capability.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6150h (Function #0)
<PCI_S0_REG_base> + 7150h (Function #1)

Initial Value: 0001_0003h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Next Capability Offset												Capability Version			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCI Express Extended Capability ID															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W (AXI)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-171 PCI_EP_DEVSNEXTC_Fn Register Contents

Bit Position	Bit Name	Description
31 to 20	Next Capability Offset	Indicates that this is the last item in the capability list. Fixed to 000h.
19 to 16	Capability Version	Indicates the version number of the capability structure. Initial value: 0001b.
15 to 0	PCI Express Extended Capability ID	Indicates the device serial number extended capability. Initial value: 0003h

Table 36.5-172 Valid Reset Signal

Reset Signal	Capability Version
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	
FLR	

(54) Serial Number Register (Lower DW) (Function #n) (PCI_EP_SNL_Fn) (n = 0, 1)

This register specifies the serial number of the device.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6154h (Function #0)
<PCI_S0_REG_base> + 7154h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PCI Express Device Serial Number (Lower DW)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCI Express Device Serial Number (Lower DW)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-173 PCI_EP_SNL_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	PCI Express Device Serial Number (Lower DW)	These are the lower-order 32 bits of a unique ID (EUI-64) of the IEEE specification. An EUI-64 consists of a 24-bit company ID and a 40-bit vendor-defined extension ID.

Note: The value of the PCI Express device serial number of the lower-order and the higher-order bits should be the same for all functions.

Table 36.5-174 Valid Reset Signal

Reset Signal	PCI Express Device Serial Number (Lower DW)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	
FLR	

(55) Serial Number Register (Upper DW) (Function #n) (PCI_EP_SNU_Fn) (n = 0, 1)

This register specifies the serial number of the device.

Access Size: 32 bits

Address(es): <PCI_S0_REG_base> + 6158h (Function #0)
<PCI_S0_REG_base> + 7158h (Function #1)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PCI Express Device Serial Number (Upper DW)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCI Express Device Serial Number (Upper DW)															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W (AXI)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
R/W (PCIe)	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 36.5-175 PCI_EP_SNU_Fn Register Contents

Bit Position	Bit Name	Description
31 to 0	PCI Express Device Serial Number (Upper DW)	These are the higher-order 32 bits of a unique ID (EUI-64) of the IEEE specification. An EUI-64 consists of a 24-bit company ID and a 40-bit vendor-defined extension ID.

Note: The value of the PCI Express device serial number of the lower-order and the higher-order bits should be the same for all functions.

Table 36.5-176 Valid Reset Signal

Reset Signal	PCI Express Device Serial Number (Upper DW)
RST_LOAD_B	✓
RST_RSM_B	
RST_CFG_B	
FLR	

36.6 PHY Register Descriptions

For more information, contact a Renesas Electronics sales representative.

36.7 Functional Description

36.7.1 PCIe Core Functions

The functional description of the unit is given below.

This unit is configured based on the Base Spec 4.0. For the detailed specification, refer to the Base Spec 4.0. This section mainly describes the parts specific to Renesas Electronics.

36.7.2 Issuing of PCIe Requests and Register Access (by AXI)

The following gives functional description on access to the PCI Express core by the AXI bus.

36.7.2.1 PCIe Requests which can be Issued (Supported Commands for TX)

Requests to be issued via pcie windows

MRd: Memory Read Request

MWr: Memory Write Request

Requests to be issued by the registers

MRd: Zero-Length Memory Read Request

CfgRd0: Configuration Read Type 0

CfgWr0: Configuration Write Type 0

CfgRd1: Configuration Read Type 1

CfgWr1: Configuration Write Type 1

Msg: Message Request

MsgD: Message Request with data payload

Unsupported requests (issuance prohibited)

IORd: I/O Read Request

IOWr: I/O Write Request

MRdLk: Memory Read Request-Locked

CplDLk: Completion for Locked Memory Read

CAUTION

If non-posted request with data (CfgWr0/CfgWr1/IOWr) which should not be transmitted is issued inadvertently in EPS mode, an MRd (non-posted request without data) which can be normally transmitted in EP mode may not also be transmitted after that.

36.7.2.2 Register Access

1) Internal register read/write

2) Configuration register read/write

The following restrictions apply to access to the configuration registers.

- Byte-lane transfer is only acceptable if the transfer consists of consecutive valid bytes.
- If the valid bytes are not consecutive, only values which are no greater than 32 bits (1 dword) and do not span the dword alignment are acceptable.

  Example) A value which can represent a dword TLP for PCIe

36.7.2.3 Issuing Memory Requests

Access from the AXI side is converted into a PCIe request and then issued. Up to eight windows can be allocated. Note that only incremental bursts and fixed bursts (of 1 beat) are acceptable. Wrapping bursts and fixed bursts (of 2 or more beats) are prohibited. If these prohibited bursts are received, the unit operates as follows.

- Although the response will in general be “OKAY” (except in cases that involved a protocol error of the AXI), this is beyond the scope of guaranteed operation.
- Unexpected requests may be issued to the PCIe bus.
- Unexpected registers may be modified.

To maintain the order between memory writing and memory reading, only issue next transactions after the reception of responses to writing. Buffering is not available in the issuing of memory write requests. (Refer to the description of AWCACHE* of Mode Set 0 Register (offset: 314h).)

(1) Memory Write Transaction from the AXI

A write transaction from the AXI via a window is converted into a MWr command and then issued.

- Number of write transactions which can be accepted at a time: 1
- Write data are held in an internal buffer.
- The order between memory write transactions is preserved (with the exception of transactions for messages and configuration).
- The order of memory write and other transactions is not preserved (a preceding memory read may be overtaken).
- To preserve the order between memory writing and memory reading or of Msg and MsgD, make sure that a next transaction is only issued after a response is returned. Buffering is not available in the issuing of memory write requests.
- Writing does not proceed if the PCI power state is not D0.
- Transactions where all bits of WSTRB are 0 during a burst return an “OKAY” response, but the written data are not reflected.
- Memory requests are not issued after an acknowledgement for PME_Turn_Off Message reception/Non-D0 State transition request reception has been asserted (Precautions: Only for Endpoint mode).

(2) Memory Read Transaction from the AXI

A read transaction from the AXI via a window is converted into an MRd command and then issued.

- Number of read transactions which can be accepted at a time: 1 to 8
- Read data are held in an internal buffer to preserve the order of transactions with the same ID.
- To preserve the order of memory read transactions from a given master ID, the system can also wait until the indicator of completion of a preceding read transaction is returned. The method of waiting is selectable as either of the above by the setting of an internal register as listed in the table below.

PCIe Request Order*1	Method of Waiting	Performance	Severity of Order
0 (initial value)	Data read are held in an internal buffer.	✓	—
1	Have the system wait for a read request to be issued.	—	✓

Note 1. The order can be set by using the PCIe Request Order bit (bit [0]) of Mode Set 1 Register (offset: 318h).

- The order of memory read transactions from a different master ID is not preserved.
- The order of memory read and other transactions is not preserved.
- To preserve the order between memory reading and memory writing, make sure that a next transaction is only issued after a response is returned. Buffering is not available in the issuing of memory write requests.
- MRdLk requests are not supported and therefore cannot be issued.
- Reading does not proceed if the PCI power state is not D0.
- Memory requests are not issued after an acknowledgement for PME_Turn_Off Message reception/Non-D0 State transition request reception has been asserted (Precautions: Only for Endpoint mode).

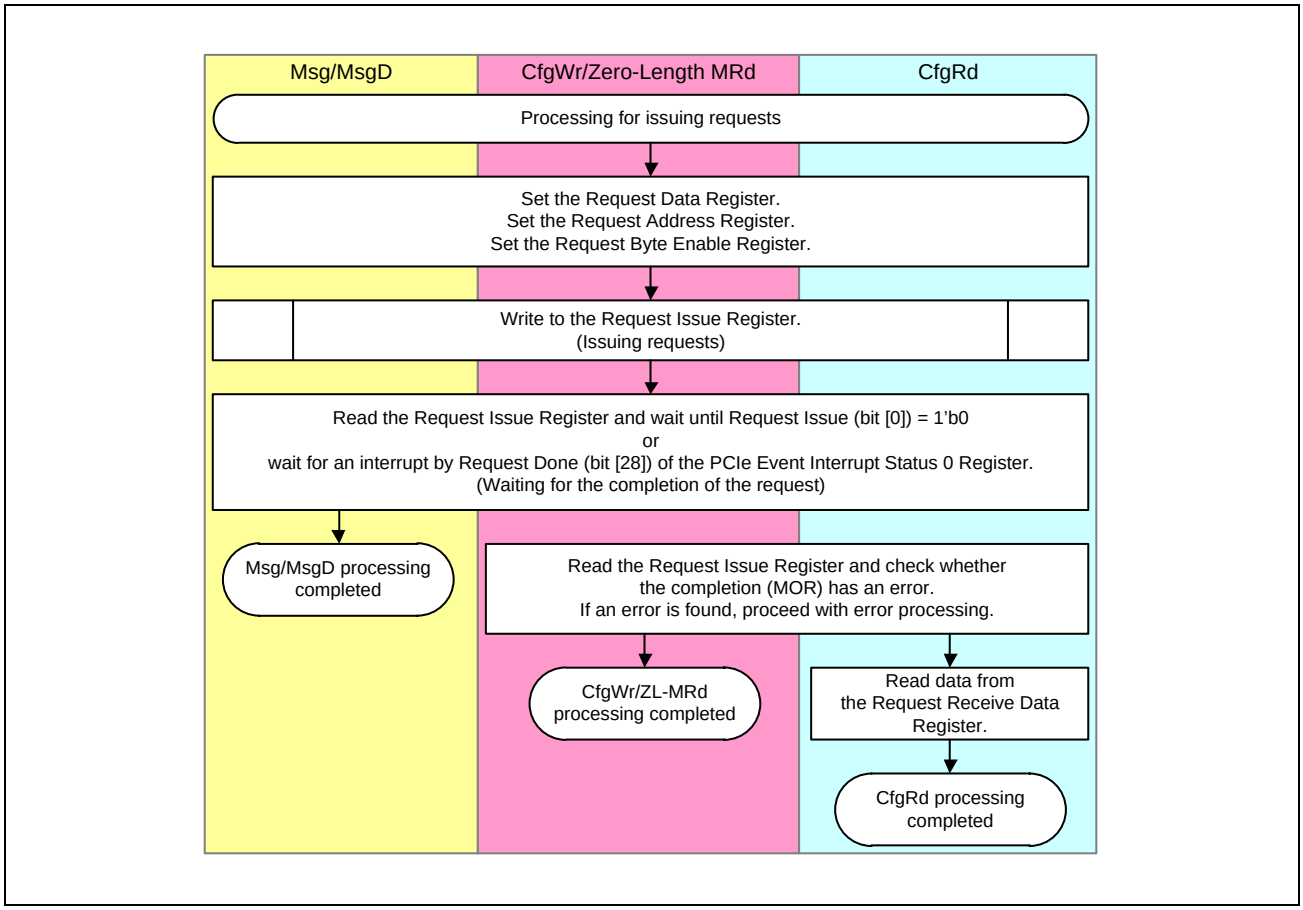
36.7.2.4 Issuing Special Requests

The following requests can be issued by controlling the internal registers.

- Configuration Read
- Configuration Write
- Zero-Length Memory Read Request
- Message Request
- Message Request with data payload

The internal registers are only writable from the AXI side. Attempted writing from the PCIe side is ignored and the write operation returns an “OKAY” response, but the written data are not reflected.

The figure below shows the flow of issuing requests by the registers.



(1) Issuing Message Requests

A message request is automatically issued by setting the Request Issue bit (bit [0]) of the Request Issue Register after access to an internal register through the AXI slave interface and setting a destination in Request Address Register 1.

(a) Flow of Issuing Message Requests

An example of the flow of issuing message requests is described below.

1. Set a destination in Request Address Register 1.

   Bits [31:27]: Reserved — Fixed to 0_0000b.

   Bits [26:24]: Routing Type — Specify the message routing.

   Bits [23:8]: Reserved — Fixed to 0000h.

   Bits [7:0]: Message CodeSpecify the message code.

2. Set the 3rd header in Request Data Register 1 as required.
3. Set the 4th header in Request Data Register 2 as required.
4. For MsgD, set write data in Request Data Register 3 (not required in the case of Msg).
5. Message requests are automatically issued by setting the Request Issue bit (bit [0]) of the Request Issue Register to 1b (the TR type bits (bits [11:8]) of the Request Issue Register are used to set Msg/MsgD).
6. Read the Request Issue Register and wait (polling) or wait for an interrupt of Request Done (bit [28]) of PCIe Event Interrupt Status 0 Register until the Request Issue bit (bit [0]) is set to 0b, wait for the request to end.

(b) Notes when Issuing Message Requests

Points to note when issuing message requests are described below.

- INTx and error type messages are automatically issued. They do not require issuing as message requests by the user (prohibited).
- Set message headers appropriately.
- A value to be set in a message header must be 0 except when sending a vendor defined message.

(2) Issuing Zero-Length Read Requests

A zero-length read request is automatically issued by setting a destination in Request Address Register 1 after access to an internal register through the AXI slave interface and setting the Request Issue bit (bit [0]) of the Request Issue Register.

(a) Flow of Issuing Zero-Length Read Requests

An example of the flow of issuing zero-length read requests is described below.

1. Set a destination in Request Address Register 1.

   Bits [31:2]: Address Set the address.

   Bits [1:0]: Reserved Fixed to 00b.

2. Set a destination in Request Address Register 1.

   Bits [64:32]: Address Set the address.

3. Set Byte Enable (0000b) in Request Byte Enable Register.
4. Zero-length read requests are automatically issued by setting the Request Issue bit (bit[0]) of the Request Issue Register to 1b (the TR type bits (bits [11:8]) of the Request Issue Register are used to set zero-length read).
5. Read the Request Issue Register and wait (polling) or wait for an interrupt of Request Done (bit [28]) of PCIe Event Interrupt Status 0 Register until the Request Issue bit (bit [0]) is set to 0b, wait for the request to end.

36.7.3 Initiation of AXI Transactions and Register Access (by PCIe)

The following gives functional description on access to the AXI bus by the PCI Express core.

36.7.3.1 PCIe Requests which can be Received (Supported Commands for RX)

MRd: Memory Read Request

MWr: Memory Write Request

CfgRd0: Configuration Read Type 0

CfgWr0: Configuration Write Type 0

Msg: Message Request

MsgD: Message Request with data payload

Cpl: Completion

CplD: Completion with Data

The following requests are not supported.

MRdLk: Memory Read Request-Locked

IORd: I/O Read Request

IOWr: I/O Write Request

CplLK: Completion for Locked Memory Read without Data

CplDLk: Completion for Locked Memory Read

CfgRd1: Configuration Read Type 1

CfgWr1: Configuration Write Type 1

AtomicOP is not supported.

36.7.3.2 Initiation of AXI Transactions

Access from the PCIe side is converted into an AXI transaction and then issued. Up to eight windows can be allocated.

To avoid a read-after-write (RAW) hazard, only issue a next memory write request following reception of the completion TLP for the previous one.

Table 36.7-1 AXI Transaction from PCIe Request

PCIe Request	AXI Burst Type	AXI Bus Size	Division
MWr/MRd	Incremental	64	Yes
		32	No
IOWr/IORd	Unsupported request		
MRdLk	Unsupported request		

(1) Memory Write Transaction from the PCIe

- Allowable number of write requests to be issued: Variable (the value is set by the AXI Max Issue Write bits (bits [15:12]) of Mode Set 1 Register).
- Write data are not held in an internal buffer (buffering within the PCIe core).
- The order between memory write transactions is preserved.
- The order of memory writing and memory reading is not preserved.
- To preserve the order between memory writing and memory reading, make sure that a next request is only issued after a completion TLP is returned.
- AWCACHE and AWPROT can be set by using Mode Set 0 Register.
- In cases of contention between DMA transfer (from PCIe to AXI) and memory write transaction, requests are accepted in turn in round-robin fashion.

(2) Memory Read Transaction from the PCIe

- Allowable number of read requests to be issued: Variable (the value is set by the AXI Max Issue Read bits (bits [11:8]) of Mode Set 1 Register).
- Since the PCI specification requires dword-aligned memory addresses in transfer, invalid byte lanes may be read. If an AXI slave as a read destination has a register or FIFO buffer which has been cleared by being read, the transaction may be non-compliant.
- Data read are held in an internal buffer.
- The order between memory read operations is preserved.
- A preceding memory write is not overtaken.
  Data read are held in an internal buffer until a preceding memory write is completed.
  When a zero-length read request is received, an “OKAY” response is returned, but the written data are not reflected and a completion TLP is transmitted after waiting for the completion of the preceding memory write.
  Data read are held in an internal buffer until a preceding memory write is completed.
- ARCACHE can be set by using Mode Set 0 Register.
- In cases of contention between DMA transfer (from AXI to PCIe) and memory read transaction, requests are accepted in turn in round-robin fashion.

36.7.3.3 Narrow Transfer

Narrow transfer to be initiated by the AXI transfer only supports the following AXI transactions.

- MAxBURST = INCR
- MAxSIZE = 0h to 2h (8 bits / 16 bits / 32 bits)
- MAxLEN = 0h (1 beat)

The following restrictions apply to TLPs from the PCIe module in narrow transfer.

- The length is 1 dword.
- The First Byte Enable bit only supports the following.
  - MAxSIZE = 0h (8 bits): 1000b / 0100b / 0010b / 0001b
  - MAxSIZE = 1h (16 bits): 1100b / 0011b
  - MAxSIZE = 2h (32 bits): 1111b

36.7.4 DMAC Functions

This section explains functions of the DMAC within the unit. Control by registers and by descriptors are both supported as methods of DMA control. The method of control is independently selected per channel.

36.7.4.1 Register-Type Transfer

DMA transfer from AXI to PCIe or vice versa is handled by software making register settings. The table below lists the DMAC registers for execution of register-type DMA transfer.

Table 36.7-2 Registers Related to Register-Type DMA Transfer

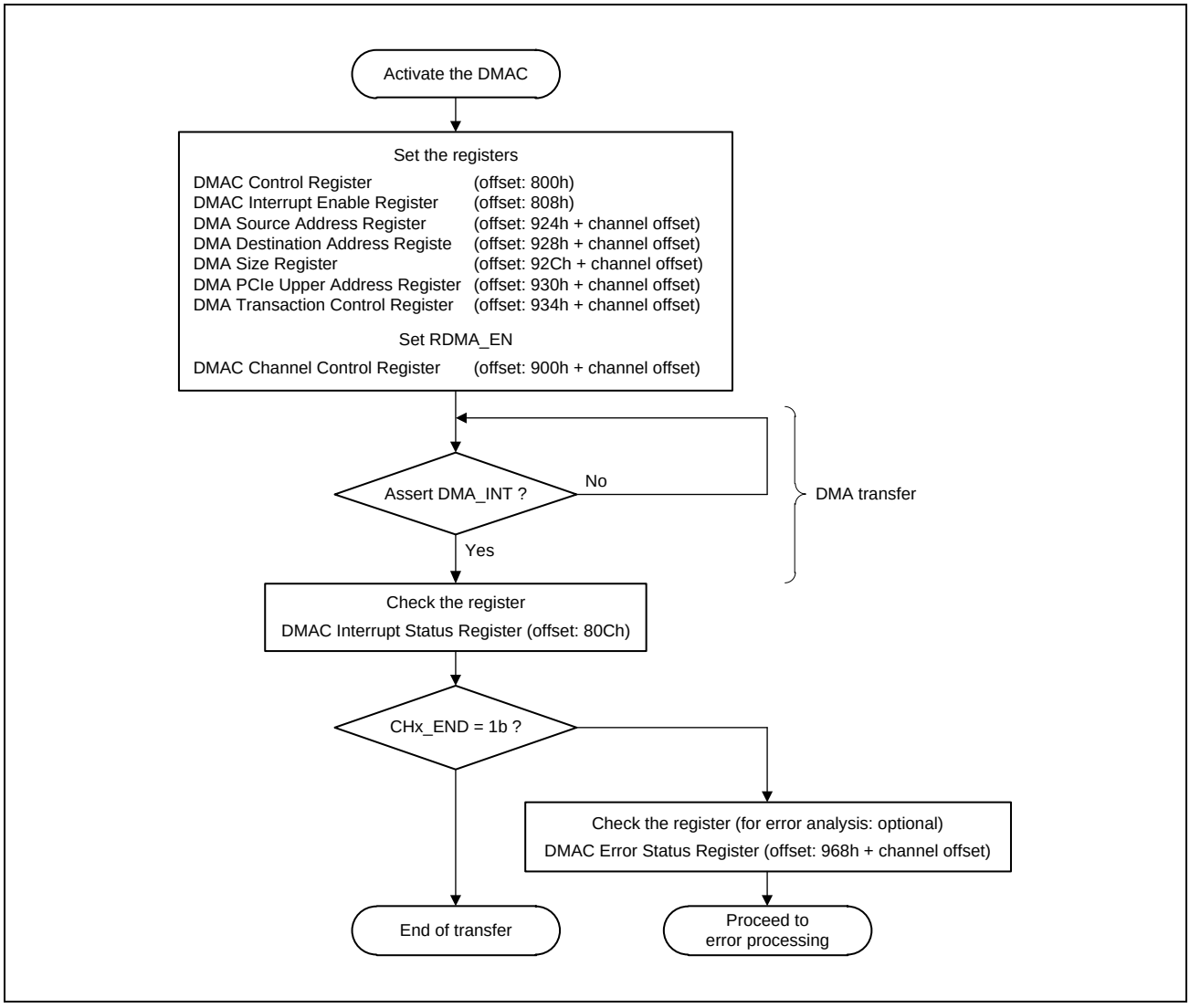
Common Control	
800h	DMAC Control Register
808h	DMAC Interrupt Enable Register
80Ch	DMAC Interrupt Status Register
Channel Control	
900h + channel offset	DMA Channel Control Register m
DMA Setting	
924h + channel offset	DMA Source Address Register m
928h + channel offset	DMA Destination Address Register m
92Ch + channel offset	DMA Size Register m
930h + channel offset	DMA PCIe Upper Address Register m
934h + channel offset	DMA Transaction Control Register m
DMA Status	
950h + channel offset	DMA Rest Size Register m
954h + channel offset	AXI Request Address Register m
958h + channel offset	PCIe Request Address(Lower) Register m
95Ch + channel offset	PCIe Request Address(Upper) Register m
968h + channel offset	DMAC Error Status Register m

(1) Flow of Operations

The following describes the procedures for settings to activate and stop the DMAC in the case of register-type transfer.

(a) Activation and Normal Operation

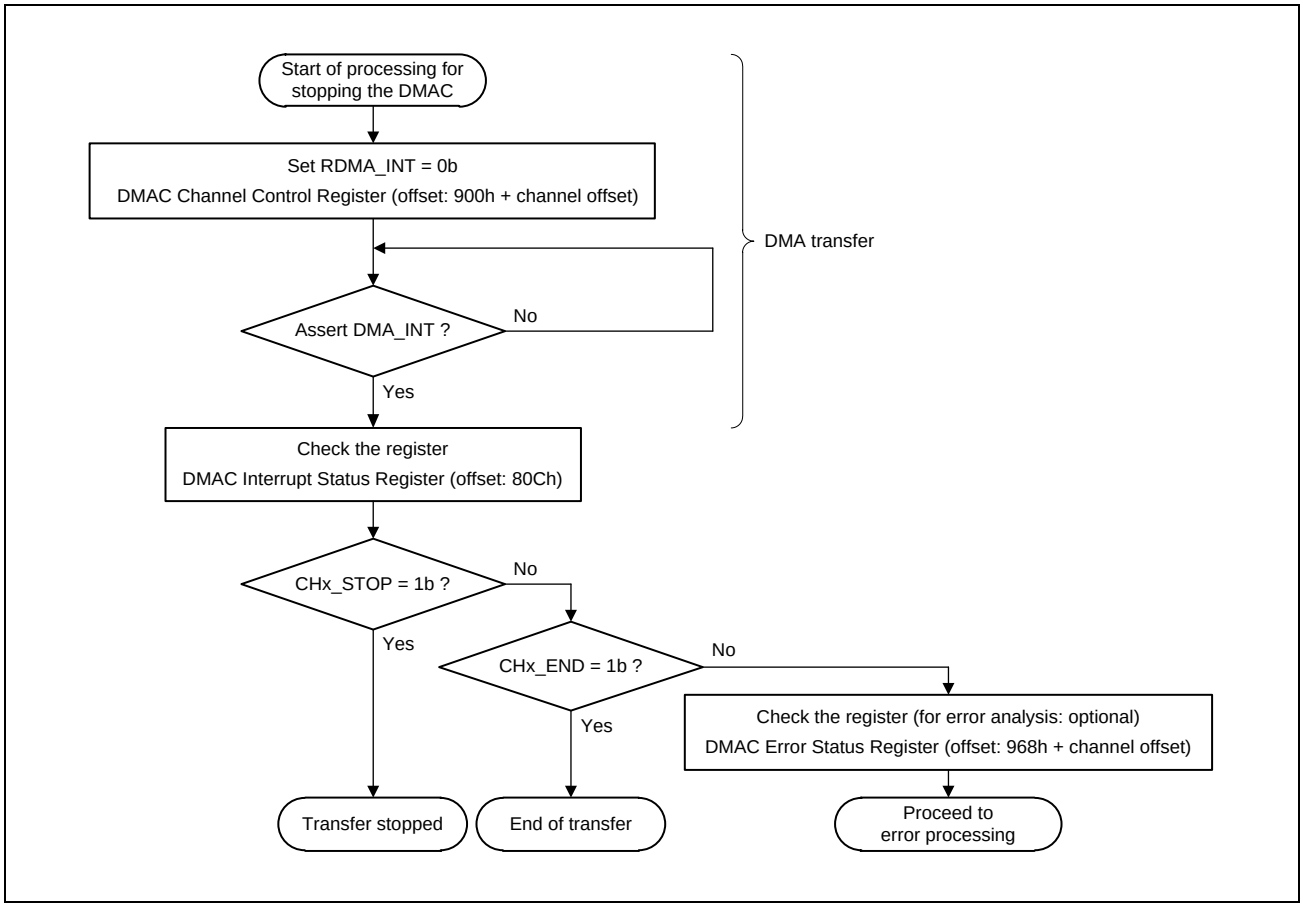
Before activating the DMAC, set the PCIe and AXI windows. After that, set the registers of the DMAC to start the DMAC.



(b) Stopping DMA Transfer

The following describes the procedure for settings to stop DMA transfer under software control.

- DMA transfer can be stopped by writing 0b to the RDMA_EN (register type DMA control enable) bit (bit [0]) of the DMAC channel control register (offset: 900h + channel offset).
- Following the detection of RDMA_EN being 0b, the unit waits for the completion of any request which has already been issued before asserting the interrupt signal (DMA_INT).
- After waiting for the assertion of DMA_INT, poll the CHx_STOP bit of the DMA Interrupt Status Register (offset: 80Ch) to check that its value is 1b.
- This indicates that DMA transfer has been stopped. If the CHx_STOP bit is 0b, check the CHx_END bit for the given channel in the same register.
- If a last request is still being executed when RDMA_EN is set to 0b, the CHx_END bit indicates the completion of DMA transfer as in normal operation.
- The address to which transfer was most recently completed before it was stopped and the remaining number of bytes for transfer can be checked by reading the DMA Status registers (offset: 950h + channel offset to 95Ch + channel offset) for the given channel.

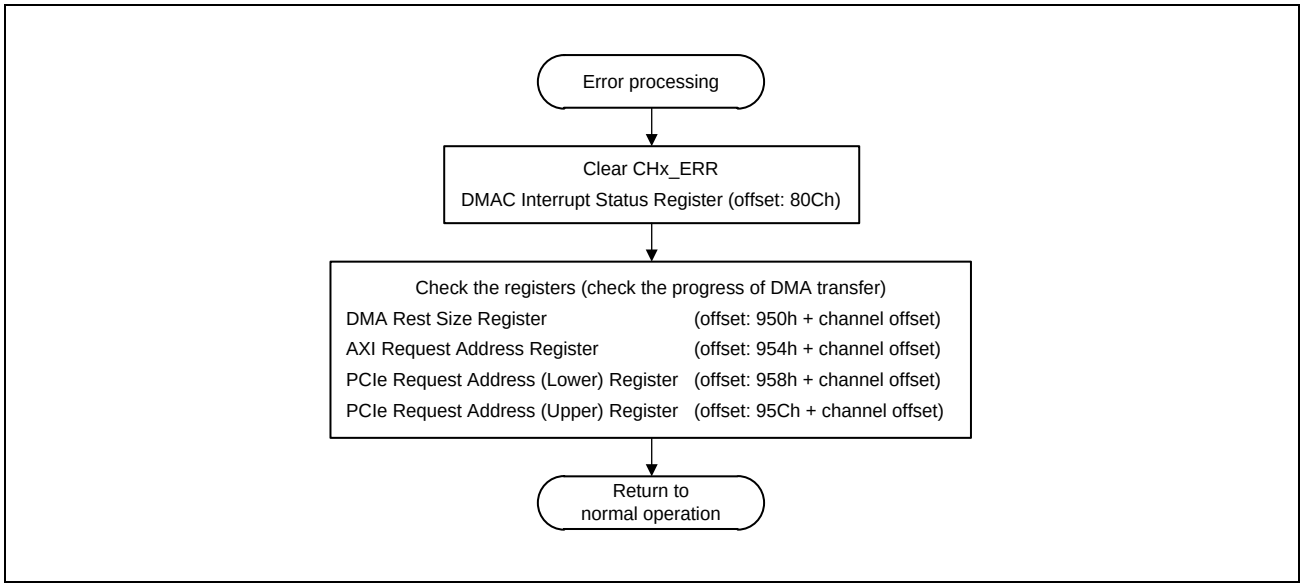


(c) Error Processing

If an error is detected in the AXI bus or a PCIe link while DMA transfer is in progress, the DMA_INT interrupt signal is asserted.

Check the channel where the error was found (CHx_ERR = 1b) by using the DMAC Interrupt Status Register (offset: 80Ch) and also the type of error by using the DMAC Error Status Register (offset: 968h + channel offset) as required.

Clear the CHx_ERR bit that is currently set in the DMAC interrupt status register (offset: 80Ch) by writing 0b to it and check the address to which transfer was most recently completed before it was stopped and the remaining number of bytes for transfer by reading the DMA Status registers (offset: 950h + channel offset to 95Ch + channel offset) for the given channel.



36.7.4.2 Descriptor-Type Transfer

Consecutive DMA transfer is achieved by sequentially reading descriptors which indicate parameters of DMA transfer. Descriptors are allocated to the AXI memory space and the descriptor lists indicate the addresses where the descriptors start. This DMAC has a queue for storing multiple descriptor lists and these descriptor lists are written by software. The first list loaded in the queue is executed after being moved to become the descriptor list for execution following the detection of the condition for starting DMA transfer (the DMAC retains up to nine lists, including the one currently being executed).

Descriptors can have a chained configuration; execution of a descriptor list ends on detection of the last descriptor, and if the queue has a next list, execution of the next descriptor follows.

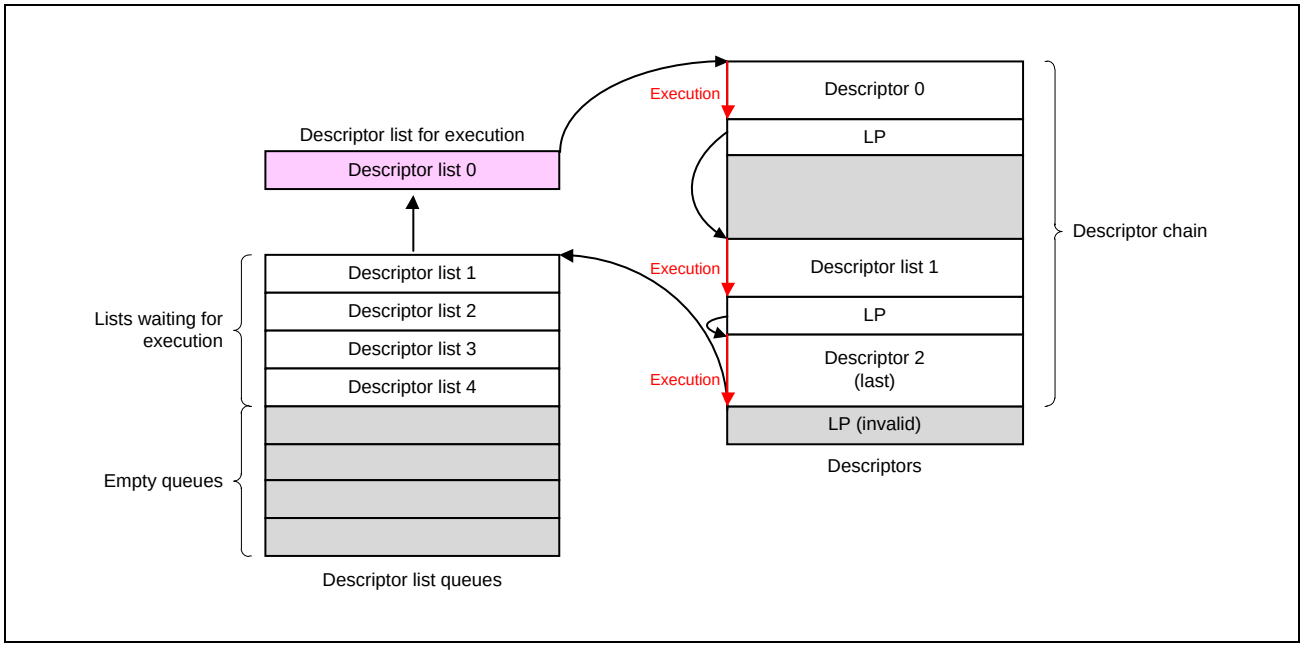


Figure 36.7-1 Descriptor Chain

The table below lists the DMAC registers for execution of descriptor-type DMA transfer.

Table 36.7-3 Registers Related to Descriptor-Type DMA Transfer

Common Control	
800h	DMAC Control Register
808h	DMAC Interrupt Enable Register
80Ch	DMAC Interrupt Status Register
Channel Control	
900h + channel offset	DMA Channel Control Register
908h + channel offset	QUE Entry (Lower) Register
90Ch + channel offset	QUE Entry (Upper) Register
DMA Setting	
920h + channel offset	DMA Descriptor Control (Descriptor 00h) Register m
924h + channel offset	DMA Source Address (Descriptor 04h) Register m
928h + channel offset	DMA Destination Address (Descriptor 08h) Register m
92Ch + channel offset	DMA Size (Descriptor 0Ch) Register m
930h + channel offset	DMA PCIe Upper Address (Descriptor 10h) Register m
934h + channel offset	DMA Transaction Control (Descriptor 14h) Register m
93Ch + channel offset	DMA Descriptor Link Pointer (Descriptor 1Ch) Register m
DMA Status	
950h + channel offset	DMA Rest Size Register m
954h + channel offset	AXI Request Address Register m
958h + channel offset	PCIe Request Address(Lower) Register m
95Ch + channel offset	PCIe Request Address(Upper) Register m
960h + channel offset	QUE Status Register m
968h + channel offset	DMAC Error Status Register m

(1) Descriptor List Queues

The DMAC has queues for storing descriptor lists for each of the channels. The number of FIFO queue stages is eight, so it can hold up to eight descriptor list entries (not including the one currently being executed).

Software places descriptor list entries in the queue. The descriptor lists to be entered are set by the combination of the QUE_ENTRY (upper) register and the QUE_ENTRY (lower) register in 64-bit (or 8-byte) units.

Since the target registers are also accessible in 8-bit units, making the settings in byte units through multiple accesses is also possible. A descriptor list entry is placed in the queue at the time when the QUE_ENTRY (upper) bits [31:24] are written. When making the settings and entering lists in the queue, take care with the order of register access (values written to the QUE_ENTRY (upper) bits [31:26] will not affect the register values and settings because they are read-only bits).

When the DMAC detects the presence of a list which has been entered in the queue, the first list entry is moved to become the pointer to the next descriptor for execution and DMA transfer starts.

(2) Descriptor List Format

The table below is the format of a descriptor list.

Table 36.7-4 Descriptor List Format

Offset	Byte 3			Byte 2	Byte 1	Byte 0
00h	DSA					
04h	Reserved	EI	LS	Reserved	LABEL	

Field Name	Description
DSA[31:0]	Descriptor start address for DMA. This field indicates the address where the first descriptor to be executed is stored. Since the setting is for 8-byte alignment and allocation of a single descriptor (00h to 1Ch) to straddle a 4-K boundary is prohibited, the 5 lower-order bits [4:0] are fixed to 0b.
EI	End Interrupt bit. This bit indicates whether an interrupt (Interrupt Status CHx_END of the DMAC Interrupt Status Register (offset: 80Ch)) is or is not conveyed when processing of this descriptor list is completed. 1b: The interrupt is conveyed. 0b: The interrupt is not conveyed.
LS	List Stop bit. This bit indicates whether DMA transfer is or is not to be stopped on completion of processing for this descriptor list entry. 1b: Stopped 0b: Not stopped On completion of the list in which the setting of this bit is 1b, the QUE_EN bit of the DMA control register is cleared.
LABEL[15:0]	This field represents the label of the list. There are no special rules for the setting procedures. The value can be set as desired.

Operations by the settings of the EI and LS bits following the completion of the descriptor list are as follows.

Table 36.7-5 Details of the EI/LS Bits

EI	LS	Description
0b	0b	No interrupt. DMA transfer is not stopped. If the queue has a next list, execution of the next descriptor follows.
0b	1b	No interrupt. DMA transfer is stopped (QUE_EN is cleared).
1b	0b	Interrupt (DMAC Interrupt Status Register (Offset: 80Ch), Interrupt Status CHx_END) is present. DMA transfer is not stopped. If the queue has a next list, execution of the next descriptor follows.
1b	1b	Interrupt (DMAC Interrupt Status Register (Offset: 80Ch), Interrupt Status CHx_END) is present. DMA transfer is stopped (QUE_EN is cleared).

(3) Descriptor Format

The table below is the format of descriptors.

Table 36.7-6 Descriptor List Format

Offset	Byte 3								Byte 2								Byte 1								Byte 0							
00h	DSCFM				WBD	LE	LV		D	—	—	—	—	—	—	—	STS (not used)															
04h	SA																															
08h	DA																															
0Ch	SIZE																															
10h	PUA																															
14h	—	—	—	—	—	—	—	—	CCH_L				CCH_D				—	TC			—	—	ATB		—	FUNC				—	—	—	DIR
18h	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
1Ch	LP																															

Field Name	Description
DSCFM[3:0]	The Descriptor Format field specifies the format of descriptors. This DMAC only supports 0001b. Do not set any other value.
WBD	Write Back Disable bit Indicates whether the DMAC writes 0b back to the LV bit when DMA transfer specified by a single descriptor is completed. 1b: The LV bit is not written back. 0b: The LV bit is written back.
LE	List End bit Indicates the end of the current descriptor chain. 1b: The current descriptor is the last of the chain. 0b: The current descriptor is not the last of the chain.
LV	Link Valid bit Indicates that the descriptor is valid. When DMA transfer is completed, the DMAC writes 0b back to this bit. When DMA transfer ends due to an error, write-back does not proceed. 1b: The descriptor is valid (DMA transfer specified by the descriptor is not completed). 0b: The descriptor is not valid (DMA transfer specified by the descriptor is completed).
D	Descriptor error bit Indicates a descriptor access error. If LV = 0 when the descriptor is read, the DMAC writes 1b back to the LV bit. When a descriptor error occurs, if the setting of the LE bit is 0 (indicating that the current descriptor is not the last of the chain), the DMAC continues transfer in accord with the descriptor the LP bits indicate. 1b: A descriptor access error occurred. 0b: No error
STS[15:0]	This field has no effect when DSCFM = 0001b. The DMAC does not use this field.
SA[31:0]	The Source Address field indicates the address of the source data for transfer. Since the setting is for 8-byte alignment, do not set a value other than the 3 lower-order bits ([2:0]).
DA[31:0]	The Destination Address field indicates the destination address. Since the setting is for 8-byte alignment, do not set a value other than the 3 lower-order bits ([2:0]).
SIZE[31:0]	This field indicates the number of bytes for transfer. Since the setting is for 8-byte alignment, do not set a value other than the 3 lower-order bits ([2:0]).
PUA[63:32]	The PCIe Upper Address field indicates the higher-order part ([63:32]) of the address in the PCL2 memory space. In the case of DMA transfer from PCIe to AXI (DIR = 0b), this field indicates the source address; in the case of DMA transfer from AXI to PCIe (DIR = 1b), it indicates the destination address.

Field Name	Description
CCH_L[3:0]	This field indicates the value of A*CACHE[3:0] to be issued through the AXI. The value of CCH_L[3:0] is output when an AXI request including the last byte is issued in transfer specified in the SIZE bits. Bit [3]: Write allocation Bit [2]: Read allocation Bit [1]: Cache enabled Bit [0]: Buffer enabled The recommend value is 0000b regardless of whether DIR is 0 or 1.
CCH_D[3:0]	This field indicates the value of A*CACHE[3:0] to be issued through the AXI. The value of CCH_D[3:0] is output when an AXI request other than the condition for the output of CCH_L[3:0] is issued. Bit [3]: Write allocation Bit [2]: Read allocation Bit [1]: Cache enabled Bit [0]: Buffer enabled The recommended value is 0001b when DIR = 0b (PCIe → AXI) and 0000b when DIR = 1b (AXI → PCIe).
TC[2:0]	This field specifies the value of the traffic class of the request to be issued through the PCIe interface. The value must be fixed to 000b.
ATB[1:0]	This field indicates the value of the attribute to be issued through the PCIe interface. Bit [1]: Relaxed ordering Bit [0]: No-snoop If neither relaxed ordering nor no-snoop is used, this field should be set to 00b (recommended).
FUNC[2:0]	This field specifies the function number of the request to be issued through the PCIe interface.
DIR	This bit indicates the direction of data transfer. 1b: AXI → PCIe 0b: PCIe → AXI
LP[31:0]	This field indicates the address where a next descriptor is stored. Since the setting is for 8-byte alignment, do not set a value other than the 3 lower-order bits ([2:0]).

The conditions where the descriptor is written back after the descriptor is read, the timings, and the corresponding bits are listed below.

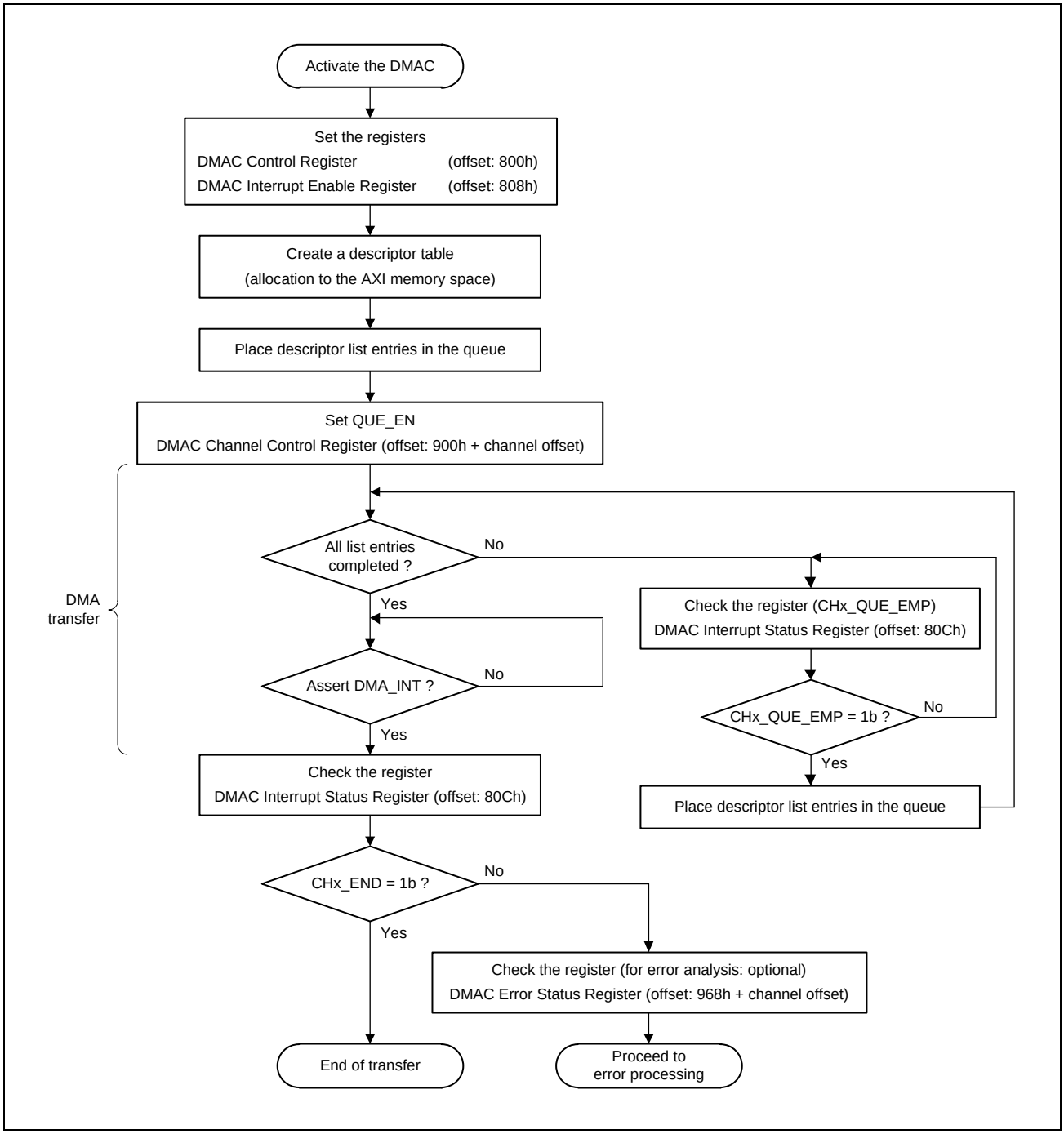
Condition	Timing	Corresponding Bit and Value
WBD = 0b && LV = 1b	After DMA transfer specified by the descriptor is completed	LV = 0b
WBD = (1b or 0b) && LV = 0b	After the descriptor is read (DMA transfer does not proceed)	D = 1b
WBD = 1b && LV = 1b	Write-back does not proceed.	—

(4) Flow of Operations

The following describes the procedures for settings to activate and stop the DMAC in the case of descriptor-type transfer.

(a) Activation and Normal Operation

Before activating the DMAC, set the PCIe and AXI windows. After that, set the registers of the DMAC to start the DMAC.

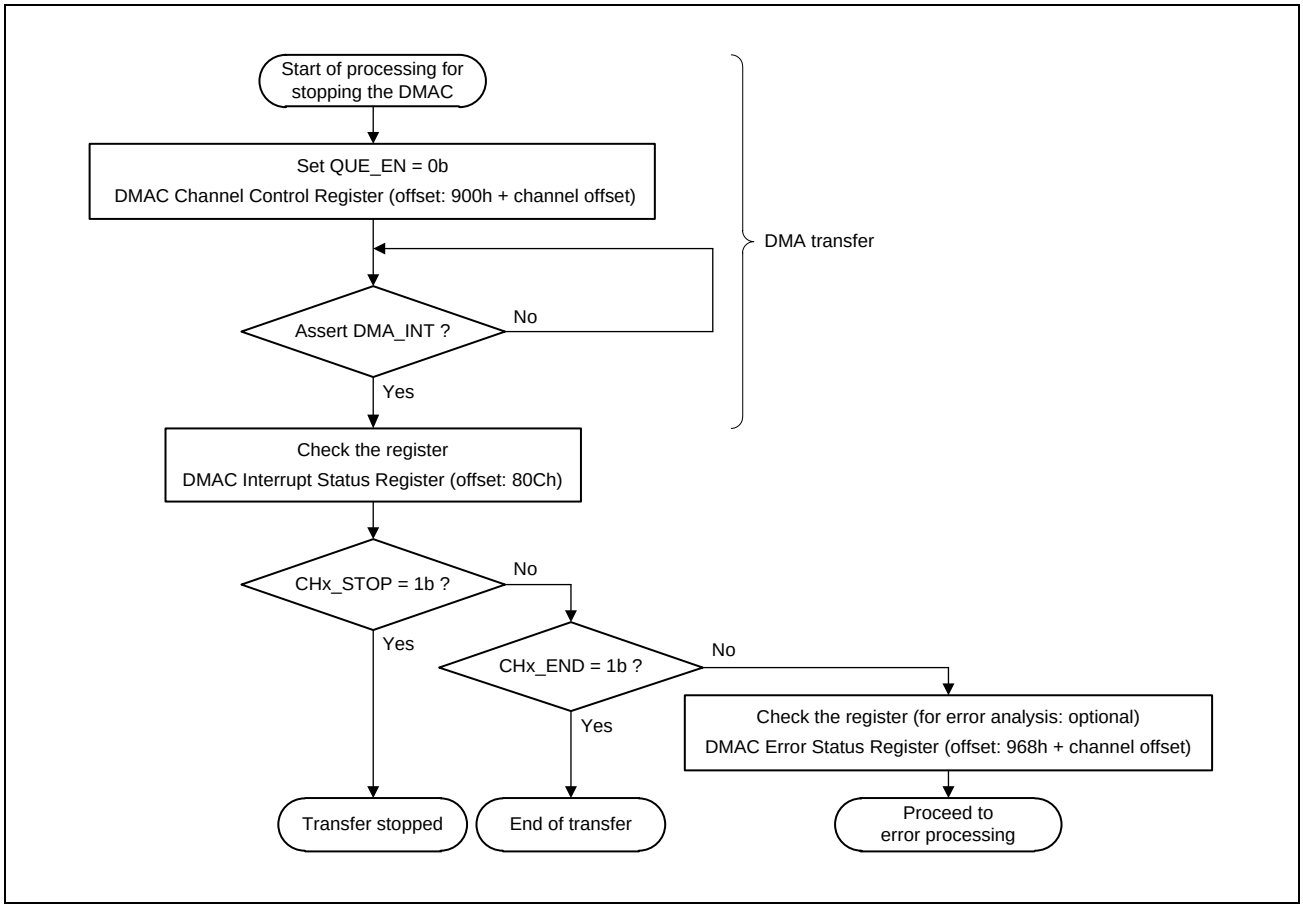


(b) Stopping DMA Transfer

The following describes the procedure for settings to stop DMA transfer under software control.

DMA transfer can be stopped by writing 0b to the QUE_EN (queue enable) bit (bit [1]) of the DMAC channel control register (offset: 900h + channel offset). Following the detection of QUE_EN being 0b, the unit waits for the completion of any request which has already been issued before asserting the interrupt signal (DMA_INT). After waiting for the assertion of DMA_INT, poll the CHx_STOP bit of the DMA interrupt status register (offset: 80Ch) to check that its value is 1b. This indicates that DMA transfer has been stopped. If the CHx_STOP bit is 0b, check the CHx_END bit for the given channel in the same register. If a last request is still being executed when QUE_EN is set to 0b, the CHx_END bit indicates the completion of DMA transfer as in normal operation.

The address to which transfer was most recently completed before it was stopped and the remaining number of bytes for transfer can be checked by reading the DMA status registers (offset: 950h + channel offset to 95Ch + channel offset) for the given channel.

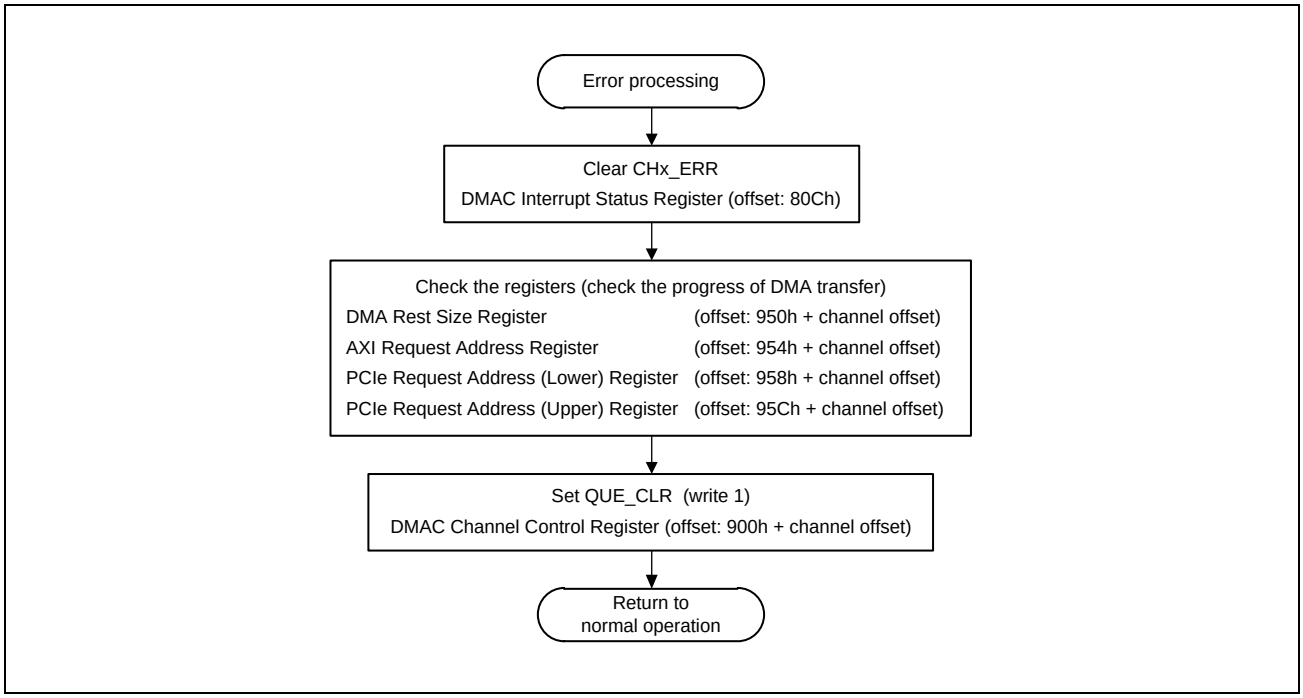


(c) Error Processing

If an error is detected in the AXI bus or a PCIe link while DMA transfer is in progress, the DMA_INT interrupt signal is asserted. Check the channel where the error was found (CHx_ERR = 1b) by using the DMAC interrupt status register and also the type of error by using the DMAC error status register (offset: 968h + channel offset) as required.

Clear the CHx_ERR bit that is currently set in the DMAC interrupt status register (offset: 80Ch) to 0b by writing to it. The address to which transfer was most recently completed before it was stopped and the remaining number of bytes for transfer can be checked by reading the DMA status registers (offset: 950h + channel offset to 95Ch + channel offset) for the given channel.

Based on that information, setting the registers as described in **Section 36.7.3.2(4)(a) Activation and Normal Operation** and create a descriptor table again. At this time, write 1b to the QUE_CLR bit (bit [8]) of the DMAC channel control register (offset: 900h + channel offset). Writing 1b to it leads to clearing of the queue. The descriptor lists registered in the queue (those waiting for execution and the one currently being executed) are all cleared.



36.7.4.3 Method of Transfer

This section describes the issuing of requests to the AXI or PCIe and data transfer in the case of DMA transfer. In either direction of transfer (from AXI to PCIe or vice versa), a request is issued to the reading side. After confirming the completion of preparation (reception) of the data to be read, a request is issued to the writing side for data transfer.

(1) DMA Transfer from PCIe to AXI

An MRd is issued to the PCIe module and an AXI write request is transferred following the reception of CplD from the PCIe. MRd requests corresponding to the number of outstanding transfers can be issued regardless of the reception of CplD. The received CplD (read data) is stored in the data buffer (RAM) once and then transferred by the DMAC to the AXI.

(2) DMA Transfer from AXI to PCIe

After the DMAC is activated, a read request (address channel) is issued to the AXI. The reception of data for reading from the given AXI slave starts and an MWr is issued to the PCIe. Data are repeatedly transferred until the completion of DMA data transfer corresponding to the amount of data set in the DMA Size bits.

36.7.4.4 Inter-Channel Arbitration

The DMAC arbitrates the following three types of request between channels.

1) PCIe Read Request
2) AXI Read Request
3) AXI Write Request

PCIe write requests do not require arbitration because data read over the AXI are returned one by one.

In the case of arbitration on the AXI side, not only requests for DMA data, but also reading and writing of descriptor data are subject to arbitration (each channel has a single source of requests for arbitration since a channel will not output a descriptor and request for data at the same time).

(1) Method of Arbitration

An MRd is issued to the PCIe module and an AXI write request is transferred following the reception of CplD from the PCIe. MRd requests corresponding to the number of outstanding transfers (eight) can be issued regardless of the reception of CplD. The received CplD (read data) is stored in the data buffer (RAM) once and then transferred by the DMAC to the AXI.

Arbitration for each type of request 1) to 3) above proceeds in round-robin fashion. A channel for which execution has just been completed is given the lowest priority and each channel which had a lower priority than that channel is raised by one rank in the order of priority.

The initial order of priority is ch. 0 > ch. 1 > ch. 2 > ch. 3 > ch. 4 > ch. 5 > ch. 6 > ch. 7.

The order of priority is changed every time a single request is completed.

There are two types of request for the AXI, requests for DMA data and requests for descriptors, but they are not distinguished for purposes of arbitration.

36.7.4.5 DMA Completed Interrupt

The DMAC has interrupt functions. It supports two types of interrupt source: one set is for normal operation and the other is for errors. For details, see **Section 36.7.6.5, DMA Interrupt**.

36.7.5 Reception of PCIe Commands

36.7.5.1 Reception of MSIs (Root Complex)

Reception of a memory write request in the MSI (message-signaled interrupt) reception area is judged to be an MSI. At this time, the request is forwarded to the AXI as a write transaction and the MSI Receive Interrupt Status bit (bit [4]) of the PCI INTx Receive Interrupt Status Register (offset: 114h) is automatically set at the same time. If the MSI Receive Interrupt Enable bit (bit [4]) of the PCI INTx Receive Interrupt Enable Register (offset: 110h) has been set, the interrupt signal (INTMSI_RC) is asserted. If the request is identified as an MSI due to the interrupt source, software can pinpoint the source by reading data in memory.

The conditions for judging a request to be an MSI

When all of the following conditions are satisfied, a request is judged to be an MSI.

(1) The request is a memory write request.

(2) The request is entered for any area within an AXI window.

(3) The address of an MWr from the PCIe interface must be within the area set by the MSI Reception Window Address register and the MSI Reception Window Mask register.
If a memory read request is received in the MSI reception area, the request is not judged to be an MSI so an interrupt is not generated.

(4) The length of memory write requests is 1 dword.

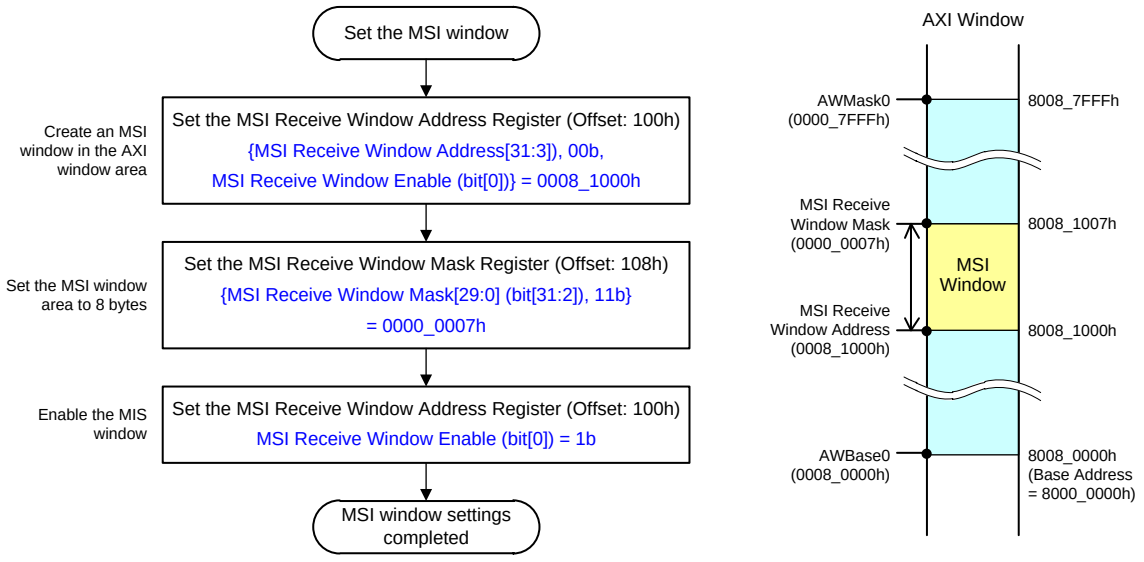
Notes on the MSI

(1) When a response to the MSI write transaction is returned, this unit judges execution of the MSI to have been completed and asserts an interrupt signal. Depending on the system, however, the MSI memory write transaction may not be completed due to the latency over the AXI to the actual memory even if the interrupt signal is asserted. To avoid this problem, buffering of AXI write transactions must be disabled (MAWCACHE[0] = 0b) at the time an MSI is issued.
For MAWCACHE[3:1], the setting of AWCACHE_L (bits [27:24]) of Mode Set 0 Register is used.

(2) If an MSI is received, the MSI write transaction is executed when MAWID[3:0] = 0001b. This is required for the unit to recognize the reception of the response to the MSI and for assertion of INTMSI_RC.

36.7.5.2 Setting the MSI Window

To enable MSI interrupts, the MSI window must be set. **Figure 36.7-2** shows example settings. The MSI window can be allocated within any AXI window.



Note: The values assigned in the figure (values in blue) are examples.

Figure 36.7-2 Settings for the MSI Window

36.7.5.3 Reception of an Interrupt in Respone to a Message Request (Root Complex)

When Assert_INTx is received in response to an Msg request from the PCIe interface, the corresponding interrupt bit (bits [3] to [0]) is set in the PCI INTx Receive Interrupt Status Register (offset: 114h) and an interrupt (INTx_RC) is asserted. When Deassert_INTx is received in response to a message request, the corresponding interrupt register (bit) is cleared and INTx_RC is de-asserted. The PCI INTx Receive Interrupt Status Register (offset: 114h) can be cleared by writing to it (RW1C) by software. In the PCIe, however, we do not recommend using software to clear an interrupt bit which has been set in response to an Msg in normal operation.

36.7.5.4 Reception of Message Requests

When a message is received through the PCIe interface, the relevant information is stored in the following registers.

Table 36.7-7 Message Related Registers

	Related Register
Message Code/Routing	Message Code Register (Offset: 130h)
Message Data	Message Data Register (Offset: 134h)
Message 3rd Header	Message Header 3rdDW Register (Offset: 138h)
Message 4th Header	Message Header 4thDW Register (Offset: 13Ch)

The corresponding bit in the Message Receive Interrupt Status Register is set at the same time as the reception of the following messages, and this is indicated by an interrupt.

Received Message		Corresponding Bit in Message Receive Interrupt Status Register
Type of Message	Message Code	
PM_Active_State_Nak	0001_0100	Bit [19]
PM_PME	0001_1000	Bit [18]
PME_Turn_Off	0001_1001	Bit [17]
PME_TO_Ack	0001_1011	Bit [16]

In the reception of PM messages other than the above, the relevant information is not written to the registers listed in **Table 36.7-7**.

- Unsupported messages:
  - Unlock
  - Vendor Defined Type 0
  - Vendor Defined Type 1

36.7.6 Interrupt

This unit prepares the output of interrupt signals in the ways stated below. The states of all interrupt signals are indicated at a glance in the Interrupt Table Register.

36.7.6.1 Error and Event Interrupt Notification

Table 36.7-8 Error/Event Interrupt Outputs

Interrupt Source Name	Active	Attribute	Description
DMA_INT	High	Level	DMA-related event
PCIE_EVT_INT	High	Level	PCIe-related event
MSG_INT	High	Level	Reception of messages
AXI_ERR_INT	High	Level	AXI-related error

Interrupt Output Related Status Registers

DMA_INT: DMAC Interrupt Status Register (Offset: 80Ch)
DMAC Error Status Register (Offset: 968h / + Channel Offset)

PCIE_EVT_INT: PCIe Event Interrupt Status 0 Register (Offset: 204h)
PCIe Event Interrupt Status 1 Register (Offset: 20Ch)
PCIe Event Interrupt Status 2 Register (Offset: 244h)

MSG_INT: Message Receive Interrupt Status Register (Offset: 124h)

AXI_ERR_INT: AXI Master Error Interrupt Status Register (Offset: 214h)
AXI Slave Error Interrupt Status 1 Register (Offset: 224h)

(1) Unit-Internal RAM Parity Error Interrupt Notification

The detection of parity errors in the internal RAM of this unit is indicated by the output of interrupt signals in the ways described below. The type of parity error detecting RAM can be confirmed from the corresponding register bit. A breakdown of the device is a possibility.

PCIE_EVT_INT: PCIe Event Interrupt Status 0 Register (Offset: 204h)
PCIe Event Interrupt Status 1 Register (Offset: 20Ch)

DMA_INT: DMAC Interrupt Status Register (Offset: 80Ch)
DMAC Error Status Register (Offset: 968h / + Channel Offset)

CAUTION

A RAM parity function is not available because it is not implemented in this core.

36.7.6.2 INTx/MSI Interrupt Notification (Root Complex)

Table 36.7-9 INTx/MSI Interrupt Outputs

Interrupt Source Name	Active	Attribute	Description
INTA_RC	High	Level	Set in response to the reception of an assert INTA message and cleared in response to the reception of a deassert INTA message.
INTB_RC	High	Level	Set in response to the reception of an assert INTB message and cleared in response to the reception of a deassert INTB message.
INTC_RC	High	Level	Set in response to the reception of an assert INTC message and cleared in response to the reception of a deassert INTC message.
INTD_RC	High	Level	Set in response to the reception of an assert INTD message and cleared in response to the reception of a deassert INTD message.
INTMSI_RC	High	Level	Set when a memory write request comes from the PCIe to the area set in the MSI reception window.
INT_LINK_BANDWIDTH	High	Level	Set when the link width has been changed.
INT_PM_PME	High	Level	Set in response to the reception of PME event notification (PM_PME message).
INT_SERR_COR/ INT_SERR_NONFATAL/ INT_SERR_FATAL	High	Level	Set in response to the reception of a correctable error message, non-fatal error message, or fatal error message.

36.7.6.3 Issuing INTx/MSI Interrupts (Endpoint)

An endpoint indicates two types of interrupt to the root complex.

(1) Legacy interrupt (Assert INTx Message/Deassert INTx Message)

- Issuing INTx Msg specified by an interrupt register by controlling an interrupt input signal (INTX_EP_F*) (recommended)
- Issuing Assert INTx and Deassert INTx messages through the issuing of special requests.

(2) MSI

- Issuing an MSI by generating a memory write transaction directly.

The MSI Enable bit in the MSI Capability Register (PCIe configuration Register) can be used to switch exclusive operation of two interrupts on or off.

To issue a legacy interrupt, the Interrupt Disable bit in the Command and Status Register (PCIe Configuration Register) must be cleared.

Furthermore, if writing proceeds in a power state other than D0 or a PME_TURN_OFF message is received, or if FLR_REQ is received, Deassert INTx Msg is automatically generated in response to the corresponding function asserting an INTx, and all active interrupts are withdrawn without waiting for the PME_Turn_Off Message reception/Non-D0 State transition request reception acknowledge/FLR_RESET response. However, when multiple functions share an INTx, the logical OR of the signals from the sharing functions is taken, a Deassert INTx Msg is generated, and the interrupts are withdrawn. If INTX_EP_F0/F1 is being asserted at the time of returning to the D0 state once more or an FLR sequence is completed (indicated by the de-assertion of FLR_REQ), Assert INTx is generated again in response.

Table 36.7-10 INTx/MSI Interrupt Inputs

Interrupt Factor Name	Active	Attribute	Description
INTX_EP_F0	High	Level	This is the trigger for Assert INTx and Deassert INTx messages.
INTX_EP_F1	High	Level	

[Related registers]

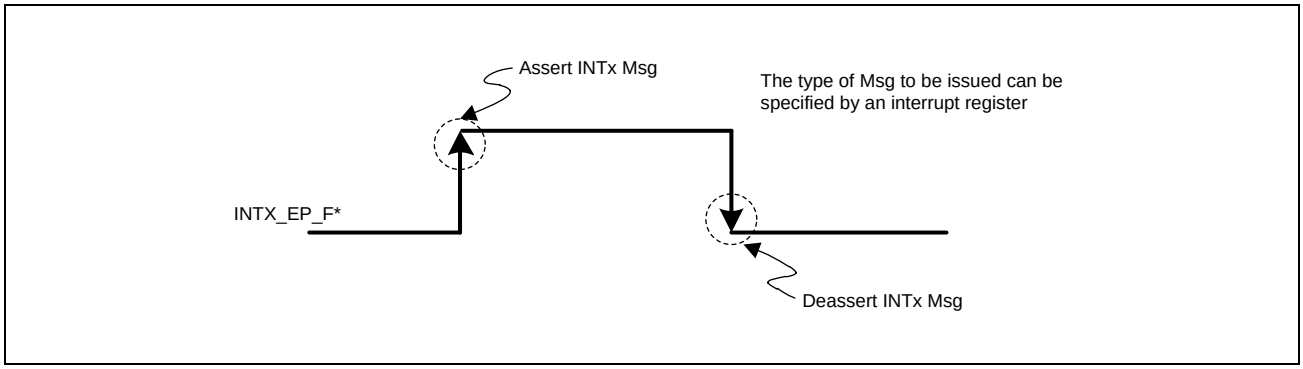
PCI INTx Out Status Register (Offset: 118h)

(1) Issuing a Legacy PCI INTx Emulation Interrupt (when MSI Enable = 0b)

A legacy PCI INTx emulation interrupt is issued by controlling INTX_EP_F*.

The type of Assert INTx and Deassert INTx Msg to be issued by controlling an interrupt signal is specified by an interrupt register provided for each of the functions. Assert INTx Msg is issued by setting INTX_EP_F* to 1, and Deassert INTx Msg is issued by clearing INTX_EP_F* to 0.

Make sure that a interrupt signal successfully arrives on the receiving side following the de-assertion of an interrupt signal. After completion of processing for an interrupt from a given source, negating the signal is recommended.



Changing the allocation of the legacy interrupt lines is possible by changing the interrupt register setting of the configuration register. If the same interrupt is shared by multiple functions, the logical OR of INTX_EP_F0 and INTX_EP_F1 is taken to issue an interrupt.

(2) MSI Transmission by Interupt Input (when MSI Enable = 1b)

Five inputs are used in specifying the interrupt (MSI). In the same way, each interrupt indication has its corresponding specified interrupt vector.

Table 36.7-11 External Interrupt Notification

Interrupt Notification Name	I/O	Note
UI_EXTMSI_VAL0/1/2/3/4	I	Interrupt notification
UI_EXTMSI_VEC0/1/2/3/4 [4:0]	I	Interrupt vector specification
UI_EXTMSI_FUNC0/1/2/3/4 [4:0]	I	Interrupt function number specification

Note: Multiple Message Enable in the Base Spec.: Implemented as a specification that supports 32 (5 bits).
Multiple Message Enable on the RC side: Support for 32 is also required.

CAUTION

Take care that the specified vector value does not impose a related restriction on the Multiple Message Enable register. For example, if the number set for Multiple Message Enable is 4, the two lower-order bits within the value set for the Message Data are overwritten by the value specified for the UI_EXTMSI_VEC[*] bits, and at that time, specify the value 0 for the higher-order bits that are not overwritten by UI_EXTMSI_VEC[*] bits. Convey interrupts in the state where the vector value and function number have been specified.

(3) Flow of Asserting MSI Enable

The following is the flow of asserting the MSI Enable field (bit 16) of the MSI Capability register.

1. Negate all INTx_EP_F0/F1 (processing by the endpoint).
2. Wait until the Interrupt Status field (bit 19) of the Command and Status register becomes 0b (confirm that the device is not in the waiting state for INTx interrupt messages).
   (Processing by the root complex: CfgRd)
3. Write 1b to the MSI Enable field (bit 16) of the MSI Capability register.
   (Processing by the root complex: CfgWr)

36.7.6.4 Root Complex Interrupt Notification

When this unit is in the root complex configuration, it has the following interrupt sources.

- INT_LINK_BAND_WIDTH
- INT_PM_PME
- INT_SERR
- INT_SERR_COR
- INT_SERR_FATAL
- INT_SERR_NONFATAL

(1) Interrupt due to the Change to the Link Bandwidth (INT_LINK_BAND_WIDTH)

This interrupt source is conveyed in response to the change to the bandwidth in link negotiation of PCI Express.

Note that this interrupt source is enabled when the root complex in use and it is fixed to “0: Low” when the endpoint is in use.

This interrupt source is only enabled when the Link Bandwidth Notification Capability bit (bit 21) of the Link Capabilities register (offset: 60Ch) is set to 1b. This interrupt signal can also be disabled by setting the Link Bandwidth Notification Capability bit to 0b even in operation as the root complex.

If the Link Bandwidth Notification Capability bit (bit 21) is set to 1b, the Link Bandwidth Management Status bit (bit 30) and the Link Autonomous Bandwidth Status bit (bit 31) in the Link Status register (offset 70h) serve as a source of the interrupt. These bits are set to 1b when the bandwidth is changed.

Whether to enable this interrupt source corresponds to the respective states of the Link Bandwidth Management Interrupt Enable bit (bit 10) and the Link Autonomous Bandwidth Interrupt Enable (bit 11) of the Link Control register (offset: 70h).

[Related Registers]

Offset	Bit	Description
PCI Express Capability Structure: Link Control / Status		
06Ch	21	Link Bandwidth Notification Capability
070h	10	Link Bandwidth Management Interrupt Enable
	11	Link Autonomous Bandwidth Interrupt Enable
	30	Link Bandwidth Management Status
	31	Link Autonomous Bandwidth Status

(2) PM-PME Reception Interrupt (INT_PM_PME)

This interrupt source is conveyed when the notification of a PME event (PM_PME message) is received from the other-party device.

Note that this interrupt source is enabled when the root complex in use and it is fixed to “0: Low” when the endpoint is in use.

This interrupt source is only conveyed when the PME Interrupt Enable bit (bit 3) of the Root Control/Capabilities Register (offset: 7Ch) is set to 1b. This interrupt source is not conveyed when the PME Interrupt Enable bit (bit 3) is set to 0b.

Note that the reception state of the received PM_PME message and the ID information, etc. are stored in the Root Status Register (offset: 80h) regardless of the setting of the PME Interrupt Enable bit mentioned above.

[Related Registers]

Offset	Bit	Description
PCI Express Capability Structure: Root Control Capabilities		
07Ch	3	PME Interrupt Enable
PCI Express Capability Structure: Root Status		
080h	15:0	PME Requester ID
	16	PME Status
	17	PME Pending

(3) System Error Interrupt (INT_SERR_xxx)

This interrupt is conveyed when a correctable error message, non-fatal error message, or fatal error message is received.

INT_SERR: The system error notification mentioned in the Base Spec. is obtained as the logical OR of the following three signals.

INT_SERR_COR: System Error on Correctable Error

INT_SERR_FATAL: System Error on Fatal Error

INT_SERR_NONFATAL: System Error on Non-Fatal Error

These interrupt sources are enabled when the root complex is in use and these are fixed to “0: Low” when the endpoint is in use.

(a) Correctable Error Interrupt (INT_SERR_COR)

To proceed with interrupt control due to a correctable error, set the interrupt enable bits of the following registers to 1b.

No.	Offset	Bit	Description
1	PCI Compatible Configuration: Bridge Control and Interrupt		
	03Ch	17	SERR# Enable
2	PCI Express Capability Structure: Device Control		
	068h	0	Correctable Error Reporting Enable
3	Advanced Error Reporting (AER) Capability: Root Error Command		
	12Ch	0	Correctable Error Reporting Enable

<Interrupt Source>

(1) ERR_COR Message Reception

If an ERR_COR message is received from the other-party device (endpoint), the INT_SERR_COR interrupt will be asserted. The following status register will be set at the same time.

Offset	Bit	Description
Advanced Error Reporting (AER) Capability: Root Error Status		
130h	0	ERR_COR Received

Note: If the Enable bits in no. 1, 2, and 3 are not set, the interrupt source will not be generated.
If the Enable bits in no. 1 and 2 are not set, writing will be masked.

(2) Correctable Error Detection

Any of the following correctable errors being detected within the unit will be written to the corresponding status register.

Error	Offset	Bit	Description
	Advanced Error Reporting (AER) Capability: Correctable Error Status		
8B10B Decode Error 8B10B RD Error	110h	0	Receiver Error Status
Bad TLP		6	Bad TLP Status
Bad DLLP		7	Bad DLLP Status
REPLAY_NUM Roll over		8	REPLAY_NUM Rollover Status
Replay Timer Timeout		12	Replay Timer Timeout Status
Advisory Non-Fatal Error		13	Advisory Non-Fatal Error Status

Note: If the Mask bit (Correctable Error Mask Register: Offset 114h) corresponding to each bit is set (masked), the corresponding error will not be detected and the interrupt source will not be generated.

At the same time, the INT_SERR_COR interrupt will be generated and the following status registers will be set to 1b.

Offset	Bit	Description
PCI Express Capability Structure: Device Status		
068h	16	Correctable Error Detect
Advanced Error Reporting (AER) Capability : Root Error Status		
130h	0	ERR_COR Received

Note: If the Enable bit in no. 2 is not set, the interrupt source will not be generated.
If the Enable bit in no. 2 is not set, writing to the Root Error Status Register will be masked.

If the Correctable Error Reporting Enable bit listed in no. 3 is not set, the source due to (1) and (2) stated above will be generated and INT_SERR_COR will not be asserted even if writing to the Root Error Register has proceeded.

(b) Fatal Error Interrupt (INT_SERR_FATAL)

To proceed with interrupt control due to a fatal error, set the interrupt enable bits of the following registers to 1b.

No.	Offset	Bit	Description
1	PCI Compatible Configuration: Bridge Control and Interrupt		
	03Ch	17	SERR# Enable
2	PCI Express Capability Structure: Device Control		
	068h	2	Fatal Error Reporting Enable
3	Common Configuration Space: Command and Status		
	004h	8	SERR# Enable
4	Advanced Error Reporting (AER) Capability: Root Error Command		
	12Ch	2	Fatal Error Reporting Enable

<Interrupt Source>

(1) ERR_FATAL Message Reception

If an ERR_FATAL message is received from the other-party device (endpoint), the INT_SERR_FATAL interrupt will be asserted (if the Enable bits in no.1 and 2 or no.3 and 4 are not set, the interrupt source will not be generated). The following status registers will be set at the same time.

Offset	Bit	Description	Remarks
Type1 Configuration Space: Secondary Status			*1
01Ch	30	Received System Error	
Common Configuration Space: Status Register			*2
004h	30	Signaled System Error	
Advanced Error Reporting (AER) Capability: Root Error Status			*3
130h	6	Fatal Error Message Received	

Note 1. Writing to this status register proceeds at the point a message is received regardless of the settings of the Enable bits.

Note 2. If the Enable bits in no. 1 and 2 are not set, writing will be masked.

Note 3. If the Enable bit in no. 1, 2, or 3 is not set, writing will be masked.

(2) Fatal Error Detection

Any of the following fatal errors being detected within the unit will be written to the corresponding status register.

Error	Offset	Bit	Description
	Advanced Error Reporting (AER) Capability: Uncorrectable Error Status		
Data Link Protocol Error	104h	4	Data Link Protocol Error Status
Poisoned TLP		12	Poisoned TLP Status
Completion Timeout		14	Completion Timeout Status
Completer Abort		15	Completer Abort Status
Unexpected Completion		16	Unexpected Completion Status
Receiver Overflow		17	Receiver Overflow Status
Malformed TLP		18	Malformed TLP Status
ECRC Error		19	ECRC Error Status
Unsupported Request		20	Unsupported Request Error Status

Note: If the Mask bit (Uncorrectable Error Mask Register: Offset 108h) corresponding to each bit is set (masked), the corresponding error will not be detected and the interrupt source will not be generated.
Also, the setting of the corresponding Severity bit (Uncorrectable Error Severity: Offset 10Ch) must be 1b (Fatal).

The INT_SERR_FATAL interrupt will be generated at the same time (if the Enable bits in no. 2 or no.3 and 4 are not set, the interrupt source will not be generated). The following status registers will be set at the same time.

Offset	Bit	Description	Remarks
PCI Express Capability Structure: Device Status			
068h	18	Fatal Error Detect	
Common Configuration Space: Status Register			*1
004h	30	Signaled System Error	
Advanced Error Reporting (AER) Capability: Root Error Status			*2
130h	6	Fatal Error Message Received	

Note 1. If the Enable bit in no. 3 is not set, writing will be masked.

Note 2. If the Enable bit in no. 2 or 3 is not set, writing will be masked.

If the Fatal Error Reporting Enable bit listed in no. 4 is not set, the source due to (1) and (2) stated above will be generated and INT_SERR_FATAL will not be generated even if writing to the Root Error Status Register has proceeded.

(c) Non-Fatal Error Interrupt (INT_SERR_NONFATAL)

To proceed with interrupt control due to a non-fatal error, set the interrupt enable bits of the following registers to 1b.

No.	Offset	Bit	Description
1	PCI Compatible Configuration: Bridge Control and Interrupt		
	03Ch	17	SERR# Enable
2	PCI Express Capability Structure: Device Control		
	068h	1	Non-Fatal Error Reporting Enable
3	Common Configuration Space: Command and Status		
	004h	8	SERR# Enable
4	Advanced Error Reporting (AER) Capability: Root Error Command		
	12Ch	1	Non-Fatal Error Reporting Enable

<Interrupt Source>

(1) ERR_FATAL Message Reception

If an ERR_NONFATAL message is received from the other-party device (endpoint), the INT_SERR_NONFATAL interrupt will be generated (if the Enable bits in no.1 and 2 or no.3 and 4 are not set, the interrupt source will not be generated). The following status registers will be set at the same time.

Offset	Bit	Description	Remarks
Type1 Configuration Space: Secondary Status			*1
01Ch	30	Received System Error	
Common Configuration Space: Status Register			*2
004h	30	Signaled System Error	
Advanced Error Reporting (AER) Capability: Root Error Status			*3
130h	5	Non-Fatal Error Message Received	

Note 1. Writing to this status register proceeds at the point a message is received regardless of the settings of the Enable bits.

Note 2. If the Enable bits in no. 1 and 3 are not set, writing will be masked.

Note 3. If the Enable bit in no. 1, 2, or 3 is not set, writing will be masked.

(2) Non-Fatal Error Detection

Any of the following non-fatal errors being detected within the unit will be written to the corresponding status register.

Error	Offset	Bit	Description
	Advanced Error Reporting (AER) Capability: Uncorrectable Error Status		
Data Link Protocol Error	104h	4	Data Link Protocol Error Status
Poisoned TLP		12	Poisoned TLP Status
Completion Timeout		14	Completion Timeout Status
Completer Abort		15	Completer Abort Status
Unexpected Completion		16	Unexpected Completion Status
Receiver Overflow		17	Receiver Overflow Status
Malformed TLP		18	Malformed TLP Status
ECRC Error		19	ECRC Error Status
Unsupported Request		20	Unsupported Request Error Status

Note: If the Mask bit (Uncorrectable Error Mask Register: Offset 108h) corresponding to each bit is set (masked), the corresponding error will not be detected and the interrupt source will not be generated.
Also, the setting of the corresponding Severity bit (Uncorrectable Error Severity: Offset 10Ch) must be 0b (Non-fatal).

The INT_SERR_NONFATAL interrupt will be generated at the same time (if the Enable bits in no. 2 or no.3 and 4 are not set, the interrupt source will not be generated). The following status registers will be set at the same time.

Offset	Bit	Description	Remarks
PCI Express Capability Structure: Device Status			*1
068h	17	Non-Fatal Error Detect	
Common Configuration Space : Status Register			*1
004h	30	Signaled System Error	
Advanced Error Reporting (AER) Capability: Root Error Status			*2
130h	5	Non-Fatal Error Message Received	

Note 1. If the Enable bit in no. 3 is not set, writing will be masked.

Note 2. If the Enable bit in no. 2 or 3 is not set, writing will be masked.

If the Non-Fatal Error Reporting Enable bit listed in no. 4 is not set, the source due to (1) and (2) stated above will be generated and INT_SERR_NONFATAL will not be generated even if writing to the Root Error Status Register has proceeded.

36.7.6.5 DMA Interrupt

The DMAC has interrupt functions. It supports two types of interrupt source: one set is for normal operation and the other is for errors. Use the DMAC Interrupt Enable Register to select the interrupt sources and control masking. DMA interrupt notification includes notification by DMA_INT in the direction of the AXI bus (local bus direction) and notification by issuing an MSI to an other-party RC.

On completion of DMA transfer, either conveying a DMA_INT interrupt or transmitting an MSI to the RC, but not both, is selected per-channel by a register setting (transmitting an MSI is prohibited in RC mode).

The DMA_CH*_MSI_EN bits of the DMA Interrupt Vector 0 Register and the DMA Interrupt Vector 1 Register are used to switch the setting (“*” corresponds to the channel number of a given DMA and per-channel control is possible). If an MSI is to be issued, the value of its traffic class (TC) bits is fixed to 0. The vector value can be specified by using the DMA_CH*_vec bits of these registers.

CAUTION

Take care that the specified vector value does not impose a related restriction on the Multiple Message Enable register. For example, if the number set for Multiple Message Enable is 4, the two lower-order bits within the value set for the Message Data are overwritten by the value specified for the DMA_CH*_vec bits, and at that time, specify the value 0b for the higher-order bits that are not overwritten by DMA_CH*_vec bits.

36.7.7 Power Management (Root Complex Mode)

36.7.7.1 PCI Power Management（PCI-PM）

An endpoint is placed in non-D0 (the D3 hot state) by changing the setting of the Power State field register of the endpoint by the root complex., which causes a transition of the link state of both RC and EP to L1.

This unit does not support the AUX power supply function. D3 cold is not supported. Implementing the L2 function goes to implementation of L2/L3 ready.

(1) Flow of Transition to the L2/L3 Ready State (RC)

< For transition via PCIPM L1 >

1. A root complex (RC) issues a config write to change the D-state of an endpoint (EP) to D3 (D3 hot).
2. The RC is automatically placed in L1 by automatic response of the other-party EC.
3. The RC transmits a PME_Turn_Off message.
4. Confirm the reception of a PME_TO_Ack Message from the EP by reading the value of the PME_TO_Ack Receive Interrupt bit (bit 16) in the Message Receive Interrupt Status Register of the RC.
5. Set UI_ENTER_L2 of PCIe Core Control 1 Registers to 1b.
6. Confirm the transition to the L2/L3 ready state by reading the value of the LTSSM_STATE bits (bits [14:8]) in the PCIe Core Status 1 Register (5 higher-order bits [14:10] = 0111xb: L2).

< For direct transition to the L2/L3 ready state >

Steps 3 to 6 above apply.

(2) Flow of Return from the L2/L3 Ready State (RC)

< Return from the L2/L3 ready state by the RC >

1. Assert the following reset signals.

   RST_B, RST_GP_B, RST_PS_B, RST_CFG_B
2. Deassert the reset signals at a desired time and wait for return to L0 (wait for linkup).
3. If the link is not up, repeat steps 1 and 2.

< Return from the L2/L3 ready state by the EP >

1. Wait for the reception of a beacon by the EP. Read the LINKDN bit (0204h, bit 9) in the PCIe Event Interrupt Status register regularly to check whether ELECTRICAL_IDLE_BROKEN has been generated.
2. Assert the following reset signals.

   RST_B, RST_GP_B, RST_PS_B, RST_CFG_B
3. Deassert the reset signals at a desired time, clear UI_ENTER_L2 of PCIe Core Control 1 Registers to 0b, and wait for it to return to L0 (wait for linkup).
4. If the link is not up, repeat steps 2 and 3.

36.7.7.2 Active State Power Management (ASPM)

The ASPM L0s and L1 states can be used by the setting of the Active State PM Control bits (bits [1:0]) in the Link Control/Status Register (PCIe Configuration Register: 6070h).

ASPM L0s: The module is automatically placed in the ASPM L0s state following setting of the Active State PM Control bits to 01b or 11b. When to initiate a transition to this state is determined by judgment of the idle state by the PCIe core.

ASPM L1: An RC is placed in the ASPM L1 state in response a request for transition to the ASPM L1 state from an EP following setting of the Active State PM Control bit to 11b. When to initiate a transition to this state is determined by judgment of the idle state by the PCIe core.
A transition to the ASPM L1 state is enabled by setting the UI_RC_REJECT_ASPM_L1 bit (bit [19]) of the PCIe Core Control 1 Register (offset: 404h) to 0b. To reject a transition to the ASPM L1 state on the RC side, set the UI_RC_REJECT_ASPM_L1 bit to 1b.

Return to the L0 state from the L1 state:

Resuming access from the AXI master side:

Return to the L0 state is initiated in response to the other-party PCIe device resuming access.

Resuming access from the AXI slave side:

The AXI can be returned to the L0 state in response to the AXI starting access to a PCIe device. Access to an AXI configuration register also returns the AXI to the L0 state.

36.7.8 Power Management (Endpoint Mode)

36.7.8.1 PCI Power Management (PCI-PM)

The endpoint unit can be placed in the D3 hot state by changing the setting of the Power State field register by the root complex. A PME_Turn_Off message can be received even after the transition to the D3 state. The turning-off procedure described below starts in such cases.

D0: This is a full-power state in which no restrictions apply. The link state is basically L0. However, if the ASPM generates a source for a transition, the latter takes priority.

D3hot: The link state basically changes to L1. By changing the value of the Power State bits of the PM Status/Control register in response to the reception of CfgWr, the unit sets D3_EVENT to 1 when a transition to the non-D0 state is requested per function, and issues Deassert_INTx in response to the assertion of any of the INTx signals. The EP should set D3_EVENT_ACK to 1 after preparation for low power consumption. After D3_EVEMT_ACK is set to 1, issuing of the AXI transaction to the PCIe is prohibited.(this does not apply to access to internal registers which include the configuration register).

This unit does not support the AUX power supply function. D3 cold is not supported. Implementing the L2 function goes to implementation of L2/L3 ready.

(1) Flow of Transition to the L2/L3 Ready State (EP)

< For transition via PCIPM L1 >

1. The D-state of an endpoint (EP) is changed to D3 (D3 hot) in response to the reception of a config write from a root complex (RC).
2. Check that D3_EVENT has been set to 1, and clear D3_EVENT_ACK to 0 after setting it to 1.
3. A transition to the L1 state is automatically initiated.
4. The EC receives a PME_Turn_Off message from the RC.
5. Check that TURN_OFF_EVENT has been set to 1, and clear TURN_OFF_EVENT_ACK to 0 after setting it to 1.
6. A transition to the L2/L3 ready state is automatically initiated.

< For direct transition to the L2/L3 ready state >

Steps 4 to 6 above apply.

(2) Flow of Return from the L2/L3 Ready State (EP)

< Return from to the L2/L3 ready state by the RC >

1. Wait for an Electrical Idle exit from the RC.
2. After that, follow the instruction by the RC to return to L0 (the following is an example).
   - Example 2-1. Follow the instruction by the RC to reset the EP (assert RST_B, RST_GP_B, RST_PS_B, and RST_CFG_B).
   - Example 2-2. Follow the instruction by the RC to release the EP from the reset state at a desired time.
   - Example 2-3. Return to L0.

< Return from to the L2/L3 ready state by the EP >

1. Check that the value of the LTSSM_STATE bits (bits [14:8]) in the PCIe Core Status 1 Register is 3Ah.

   Note: As a criterion for judgment at this time, checking the value read from this register requires consecutively checking the above value several times. Since the value of the LTSSM bits is checked by direct reference to the internal circuit state information, an undefined state value may be read depending on the timing of the operation for transition. To make sure that the current state is the L2 idle state, we recommend checking the state by access more than once. Only check all seven bits of LTSSM_STATE (bits [14:8]) of the PCIe Core Status 1 Register at this time in the flow of return.

2. Assert the Power Management Event setting input pin to 1b.
3. Assert RST_B (the EP transmits a beacon).
4. After that, follow the instruction by the RC to return to L0 (the following is an example).
   - Example 4-1. The RC detects the reception of a beacon from the EP and initiates return to L0 on the RC side.
   - Example 4-2. Follow the instruction by the RC to reset the EP (assert RST_B, RST_GP_B, and RST_PS_B, RST_CFG_B).
   - Example 4-3. Follow the instruction by the RC to release the EP from the reset state at a desired time.
   - Example 4-4. Return to L0.

36.7.8.2 Active State Power Management (ASPM)

The ASPM L0 and L1 states can be used by setting the Active State PM Control bits (bits [1:0]) of the Link Control/Status Register (PCIe Configuration Register: 6070h).

Permit a transition to ASPM L1 by setting ALLOW_ENTER_L1 to 1.

The ASPM L1 Idle Time bits of the registers must be set in advance to suit the AXI bus specifications (the range of settings is for from 256 to 65536 cycles of ACLK). If transfer does not proceed for the time set in the ASPM L1 Idle Time bits within the unit, the module is automatically placed in the ASPM L1 state.

ASPM L0s: A transition to the ASPM L0s state is automatically initiated by setting the Active State PM Control bits to 01b or 11b. When to initiate a transition to this state is determined by judgment of the idle state by the PCIe core, so your operation will not be especially required.

A transition to L0s can be controlled by setting the UI_ENTER_TXL0S bit (bit [16]) of the PCIe Core Control 1 Register.

ASPM L1: A transition to the ASPM L1 state can be initiated by setting the Active State PM Control bits to 10b or 11b. When to initiate a transition to this state is determined by judgment of the idle state by the PCIe core. A transition to the L1 state is enabled by setting ALLOW_ENTER_L1 to 1.

Return from the L1 state to the L0 state

Resuming access from the AXI master side:

Return to the L0 state is initiated in response to the other-party PCIe device resuming access.

Resuming access from the AXI slave side:

The AXI can be returned to the L0 state in response to the AXI starting access to a PCIe device. Access to an AXI configuration register also returns the AXI to the L0 state.

(1) ASPM L1 Idle Time Setting

The Mode Set 3 registers (offset: 380h) are defined as the ASPM L1 Idle Time registers. These registers are used to set the counter for monitoring the state of the AXI bus or internal transactions in terms of remaining activity when this unit is placed in the ASPM L1 state. The counter monitors whether the AXI bus and transactions within this unit are idle based on one of the following settings and uses this as the condition for triggering the transition to the ASPM L1 state.

"ASPM L1 Idle Time[7:0]" = 00h: 256 cycles of ACLK
"ASPM L1 Idle Time[7:0]" = 01h: 512 cycles of ACLK
:
"ASPM L1 Idle Time[7:0]" = FFh: 65536 cycles of ACLK

36.7.9 Error Processing

Two error reporting paradigms are defined for PCI Express: baseline error reporting capability, which is the minimal requirement, and advanced error reporting (AER) capability, which can provide greater stability, as an optional error reporting facility. Our unit supports both error reporting functions.

36.7.9.1 Error Classification

PCI Express errors are of two types, correctable and uncorrectable. Uncorrectable errors are further classified into two types, non-fatal and fatal.

Error Type	Description
Correctable Error	An error which cannot be recovered by hardware
Uncorrectable Error (Non-Fatal)	An error which causes a particular transaction in PCI Express to be unreliable (but the PCI Express link itself is functional).
Uncorrectable Error (Fatal)	An error which causes the PCI Express link itself to be unreliable

In operation as a root complex, the above types of error are indicated by the individual interrupt names.

- INT_SERR_COR
- INT_SERR_NONFATAL
- INT_SERR_FATAL

36.7.9.2 Error Checking Mechanism

(1) Physical Layer Error List

The following type of error is to be detected in the physical layer.

- Receiver Error

(2) Data Link Layer Error List

The following type of error is to be detected in the link layer.

- Bad TLP Error
- Bad DLLP Error
- REPLAY_NUM Rollover
- Replay Timer Timeout
- Receiver Overflow Error

(3) Transaction Layer Error List

The following type of error is to be detected in the transaction layer.

- Completion Timeout
- Completer Abort
- Unsupported Request
- Unexpected Completion
- Malformed TLP
- Poisoned TLP

CAUTION

The specifications of the receiver error detection function in each LTSSM state are as listed below.

LTSSM State	Unit Specification	Base Spec Specifications
Configuration	Support	Gen1/Gen2 (Must)
Recovery	Non-Support	Option
L0	Support	Must
Disabled	Support	Option
Hot Reset	Support	Option

36.7.9.3 Error Message

The PCI Express Base Specification defines error messages as one of the mechanisms for notifying the system or another device of an error when it is detected by a PCI Express agent.

Error Message	Description
ERR_COR	Used when a correctable error is detected
ERR_NONFATAL	Used when a non-fatal, uncorrectable error is detected
ERR_FATAL	Used when a fatal, uncorrectable error is detected

Advisory Non-Fatal Error

The PCI Express Base Specification states that when a PCI Express agent as the detecting agent detects a non-fatal error, it handles the error as an advisory non-fatal error whether it does or does not support AER. In handling a non-fatal error as an advisory non-fatal error, the agent sends an ERR_COR message instead of an ERR_NONFATAL message and sends an advisory notification to the software. At this time, the advisory non-fatal error status bit of the correctable error status register is set to indicate the error state. Note that subsequent setting of the first error pointer register, logging of the header, and message transmission only proceed if the Advisory Non-Fatal Error Mask bit of the Correctable Error Mask Register is clear (no masking). They do not proceed if the bit is set.

The error cases which are handled as advisory non-fatal errors are as follows.

- Reception of unsupported non-posted requests
- Reception of a non-posted request with a completer abort completion response
- Reception of an unexpected completion
- Reception of a poisoned TLP (this is not handled as an advisory non-fatal error in this core)
- Detection of a completion timeout (this is not handled as an advisory non-fatal error in this core)

This unit may merge multiple error messages with the same ID. This would occur when multiple errors are detected during the wait for the unit to be ready for the transmission of messages after an error condition is detected. However, messages will not always be merged in such cases.

36.8 Operation

36.8.1 Setting Up

Set the internal registers of the unit including the configuration registers.

This section explains the procedure for setting up until the PCI Express link is up (the module is ready for data transfer).

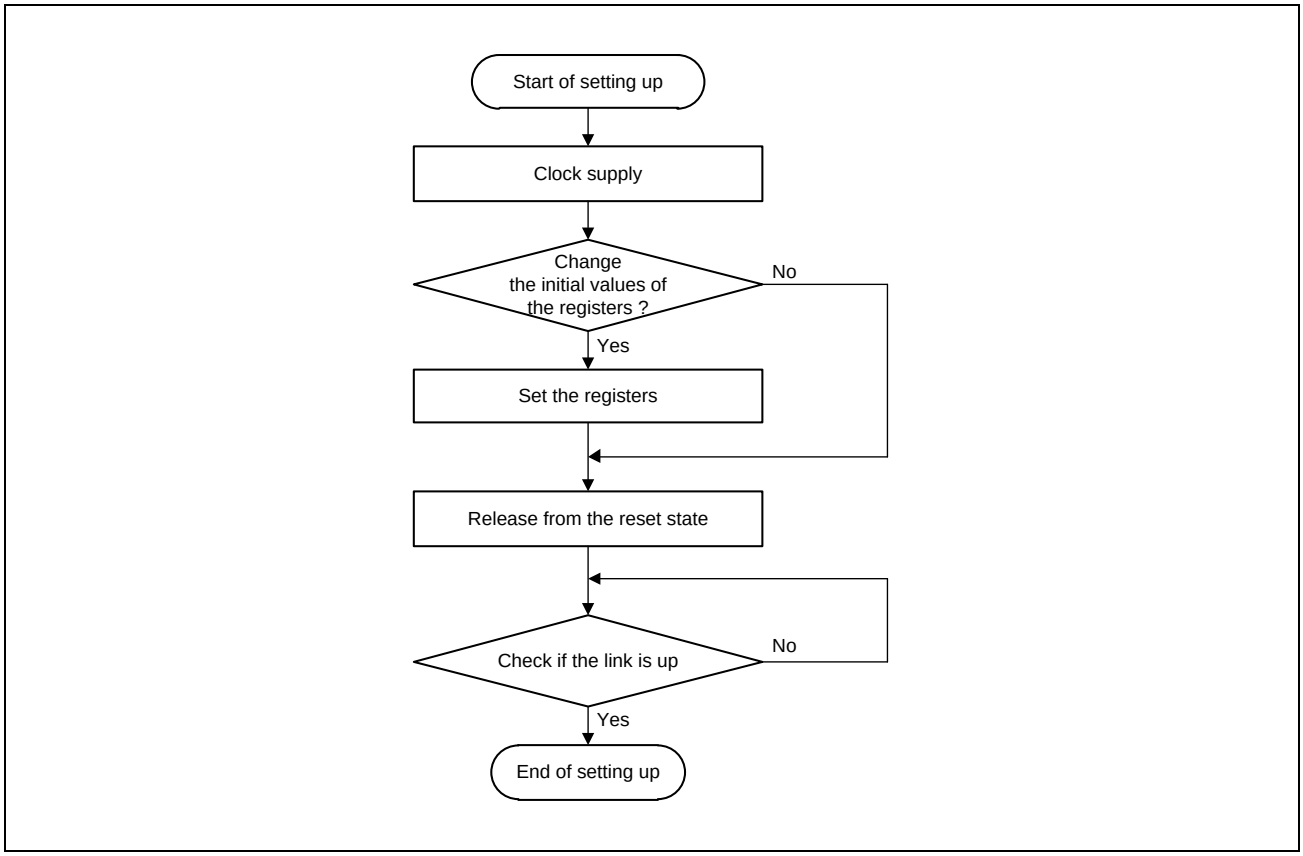


Figure 36.8-1 Setting Up

36.8.1.1 Changing the Initial Values of the Registers

Of the internal registers, the initial values of the configuration registers can be changed via the AXI slave interface.

1) AXI Bridge Registers

De-asserting ARESETn following supply of CLK allows access to these registers. In the case of resetting of the PCIe core, write to the registers while the reset signal is being asserted.

2) PCIe Configuration Register

De-asserting ARESETn following supply of CLK allows access to these registers. Of the reset signals of the PCIe core, those related to the configuration register must be de-asserted.

(1) Setting the Initial Values of the Registers

The initial values of the registers listed below are 0. Set appropriate values in the registers before the start of link up.

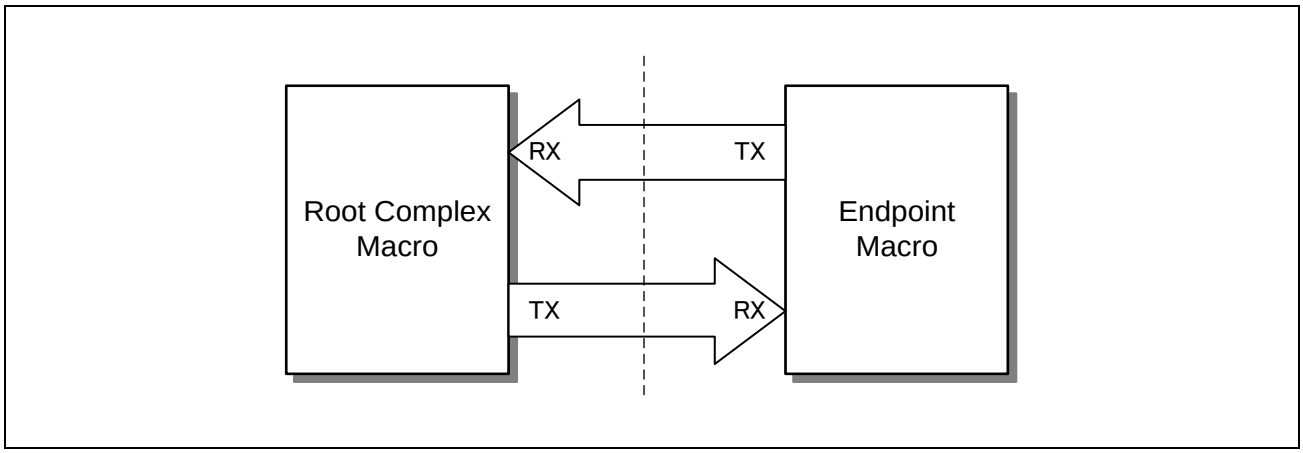
- Device ID
- Vendor ID
- Class Code (base class/sub-class/programming interface)
- Revision ID
- Subsystem ID
- Subsystem Vendor ID

36.8.1.2 De-asserting the Reset

In this unit, software reset control by the register is possible.

De-asserting of the reset of the core (the reset register in the case of register control) automatically starts operations such as receiver detection and the training sequence with the other-party device.

Note that our unit requires a wait of at least 5 ms from power-on to de-assertion of the reset.



Check that link negotiation with the other party has been completed and the link with the unit is up.

36.8.1.3 Checking if the Link is Up

Checking if the link is up can be done through either of the following methods. This is usually done by the root complex.

1) Polling

Have the CPU of the chip poll the DL_Down Status bit (bit [0]) of the PCIe core Status 1 Register in AXI bridge registers until the value of the bit is 0 (indicating the DL_Up state).

2) Interrupt

After assertion of the PCIE_EVT_INT pin of the interrupt signal, check the interrupt source by reading the DL_UpDown bit (bit [9]) in the PCIe Event Interrupt Status 0 register in AXI Bridge Registers. After that, check that the DL_Down Status bit (bit [0]) of the PCIe Core Status 1 Register is 0 (indicating the DL_Up state)

The settings above make the unit ready for transfer with the other party device.

However, data transfer such as reading or writing memory is not yet possible in this state. This requires subsequent window settings.

36.8.2 Setting the Windows (Root Complex Mode)

When using the window settings in the root complex configuration, the recommended settings in the BAR and BAR Mask registers are “BAR: All 0s” and “BAR Mask: All 1s”.

36.8.3 Setting the Windows (Endpoint Mode)

All PCI Express commands are issued via the set memory spaces or register spaces. After making the window settings and the configuration register settings, data such as PCIe MRd and MWr can be transferred. All PCI Express commands are issued via the set memory spaces or register spaces. After making the window settings and the configuration register settings, data can be transferred in response to PCIe MRd and MWr requests and so on.

36.8.3.1 BAR Specification (Two-Function Configuration)

Our unit has functionality for dividing the 64-bit memory space into window spaces for AXI access. Windows for access from PCIe to AXI and from AXI to PCIe are respectively referred to as AXI windows and PCI windows.

The AXI Bridge Registers (unit-specific registers) are accessible regardless of the function being used.

The 64-bit memory spaces must be set exclusively of each other and have no overlaps.

Set the AXI window spaces such that they do not overlap.

Table 36.8-1 Example BAR Settings (64 bits × 3, Function = 2)

Function	BAR (Memory Space)	AXI Window	Note
Function #0	64-bit memory space (1) {BAR1, BAR0}	AXI #0	
		AXI #1	
		AXI #2	
		AXI #3	
	64-bit memory space (2) {BAR3, BAR2}	AXI #4	
		AXI #5	
		AXI #6	
		AXI #7	
	64-bit memory space (3) {BAR5, BAR4}	—	AXI Bridge Registers
Function #1	64-bit memory space (1) {BAR1, BAR0}	AXI #0	
		AXI #1	
		AXI #2	
		AXI #3	
		AXI #4	
		AXI #5	
		AXI #6	
		AXI #7	
	64-bit memory space (2) {BAR3, BAR2}	—	Not allocated
	64-bit memory space (3) {BAR5, BAR4}	—	AXI Bridge Registers

Remarks BAR: Abbreviation of Base Address Register

Note: The address spaces are invalid when the corresponding BAR values are all 0s.
The BAR settings are required for each function.

The base addresses of the 64-bit memory spaces (1), (2), and (3) above are set by using the following configuration registers.

64-bit memory space (1): Configuration registers {BAR1, BAR0}
64-bit memory space (2): Configuration registers {BAR3, BAR2}
64-bit memory space (3): Configuration registers {BAR5, BAR4}

CAUTION

- Up to eight AXI windows can be set by dividing the 64-bit memory space (1).
- Up to eight AXI windows can be set by dividing the 64-bit memory space (2).
- The number of AXI windows allocated to each of the BAR areas is as follows.
  64-bit memory space (1): 64-bit memory space (2) = 8:0 or 4:4;
  Select either of the above settings. Note that all of the allocated AXI windows do not need to be used effectively.
- The 64-bit memory space (3) is dedicated for access to the AXI Bridge Registers.
- The base addresses of each of the AXI windows are limited within the 4-Gbyte space from the BAR base address.

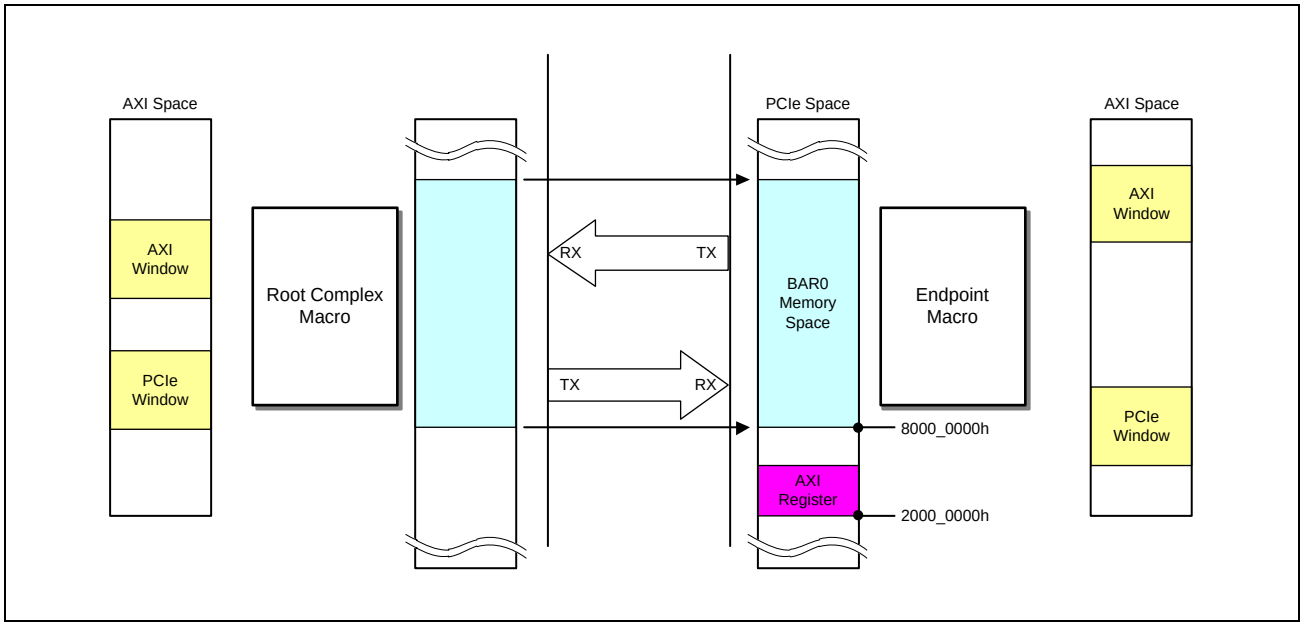
36.8.3.2 Setting the AXI Windows

In operation as an endpoint device, the AXI windows can be set in the following two ways.

1. The root complex issuing memory read and memory write requests.
2. Setting from the CPU of the endpoint under software control.

The following shows the procedure for making the settings by method 1.

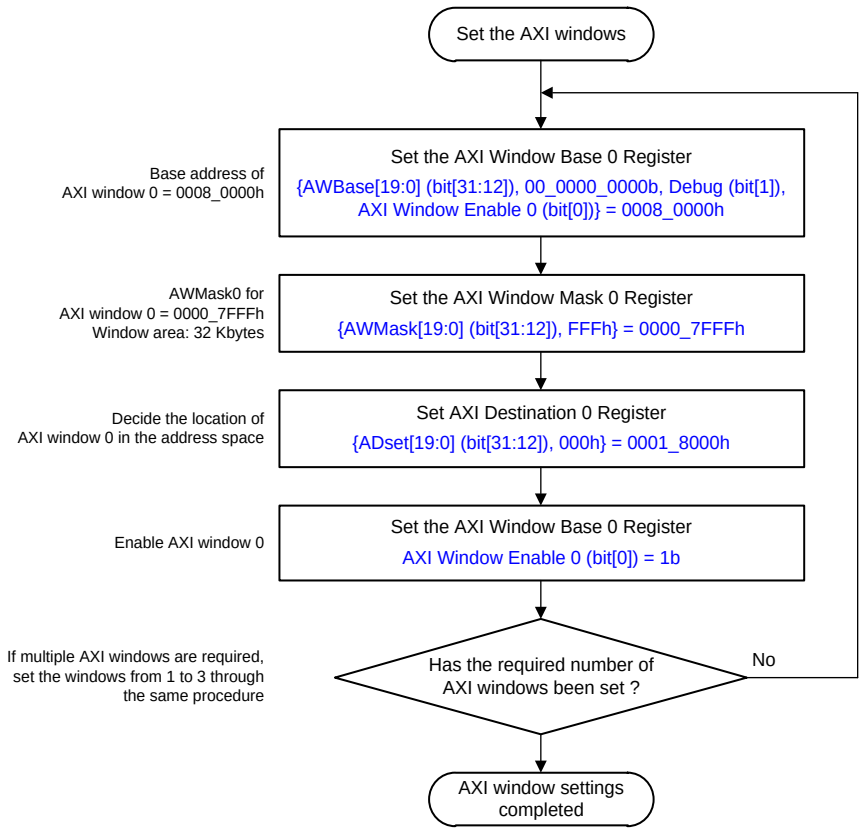
Set the AXI windows on the endpoint side by issuing memory read (MRd) and memory write (MWr) requests to the AXI Bridge Register access space set in the previous section.



Data transfer is possible when setting of the windows is completed and the Bus Master Enable bit and the Memory Space Enable bit of the given configuration register are set to the enabled state.

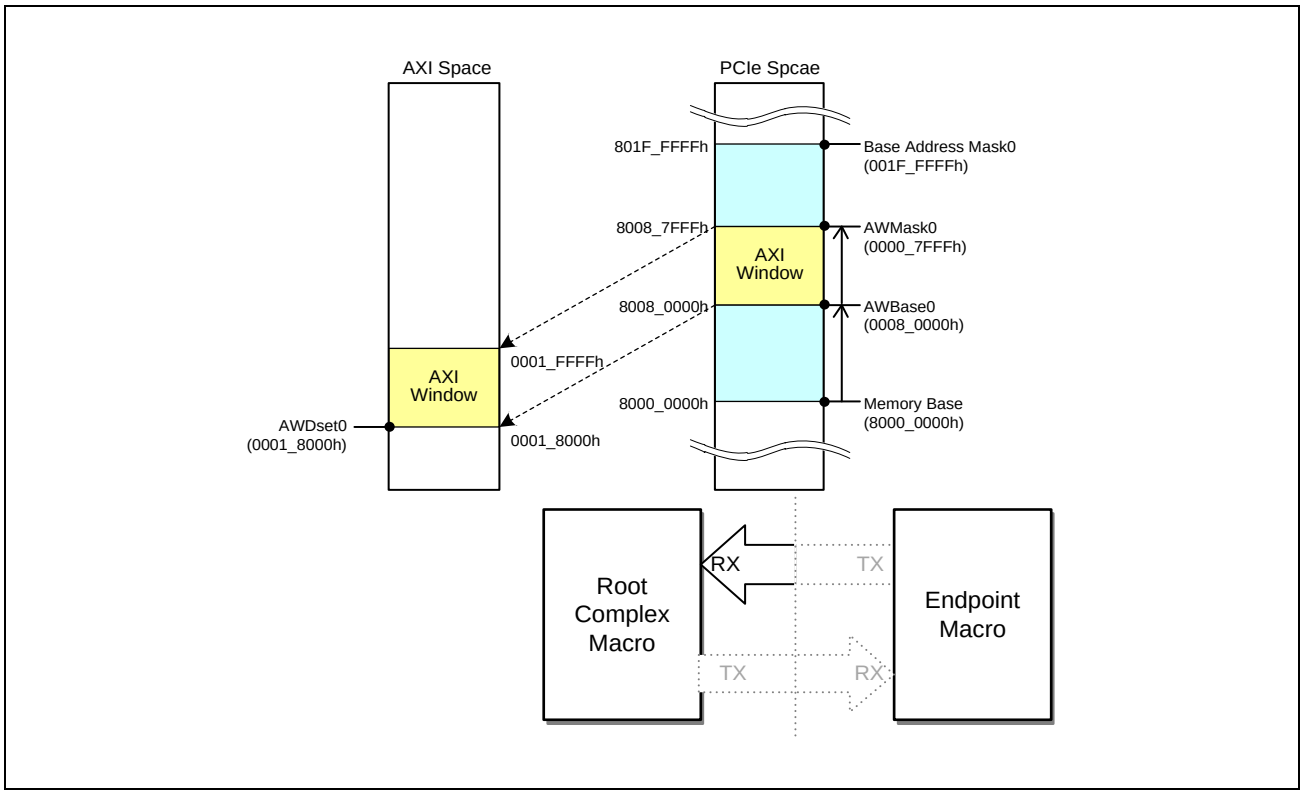
The following shows the procedure for making the settings by method 2.

The AXI windows can be set by write access to the registers through the AXI slave interface.



Note: The values assigned in the figure (values in blue) are examples.

Figure 36.8-2 Example Settings of the AXI Windows



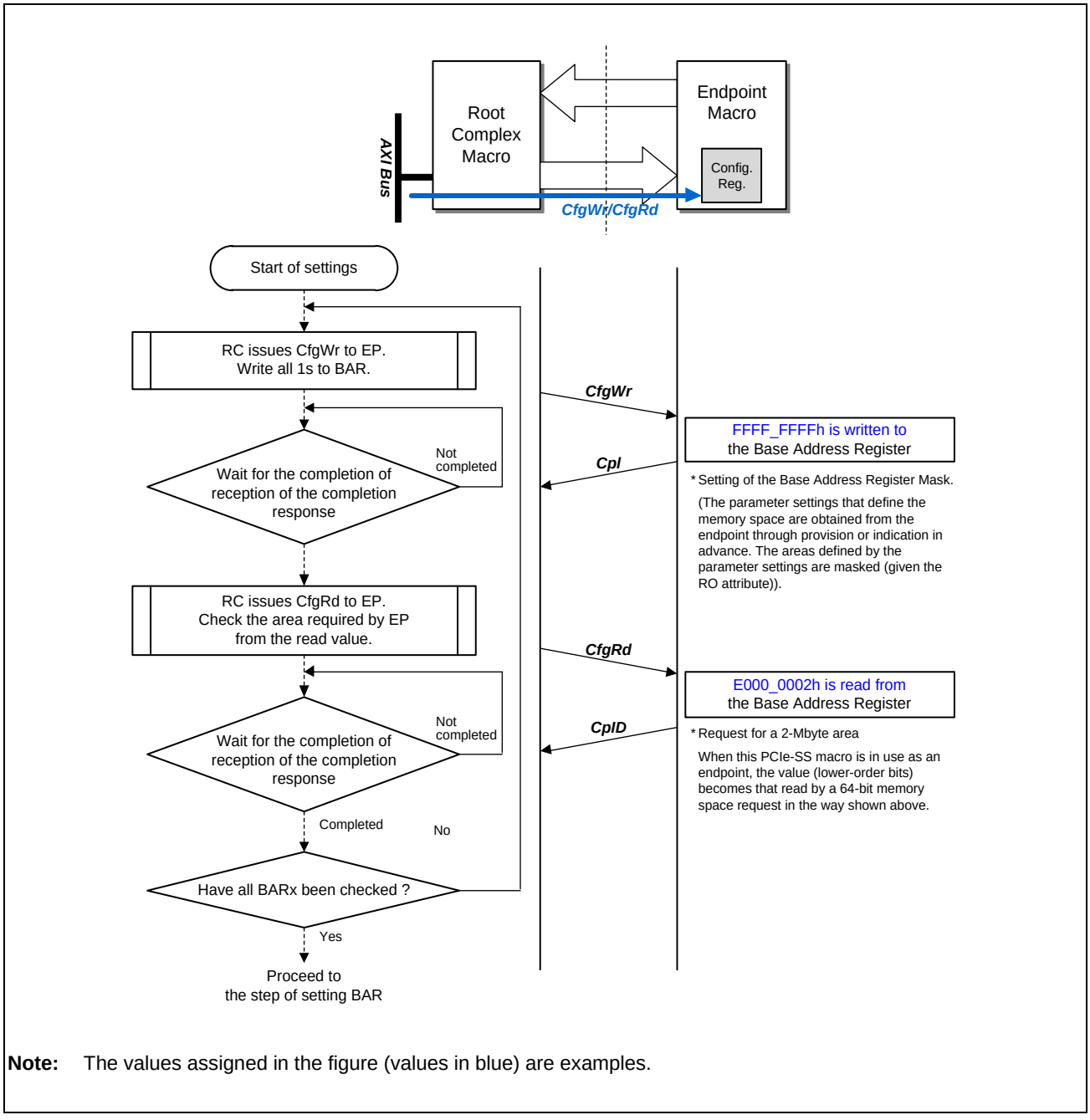
At this time, three address space settings, namely the AXI address space for the root complex device, the AXI address space for the endpoint device, and the PCI address space between the root complex and the endpoint, must be consistent within the system. If they are not, data cannot be transferred. Take care with the settings.

36.8.3.3 Setting the PCIe Address Space

A PC or similar system recognizes information on the areas of the memory space which are required by other-party endpoint devices by access to the configuration registers of the endpoints through software processing by the CPU on the root-complex side. In the case of embedded systems, etc., the areas required by the other-party devices will generally be known in advance, so this processing is not usually required.

The following is an example procedure for setting of the PCIe memory space for an other-party endpoint by the root complex.

Configuration requests are made to be issued to the other-party endpoint devices by register access through the AXI slave interface.



Note: The values assigned in the figure (values in blue) are examples.

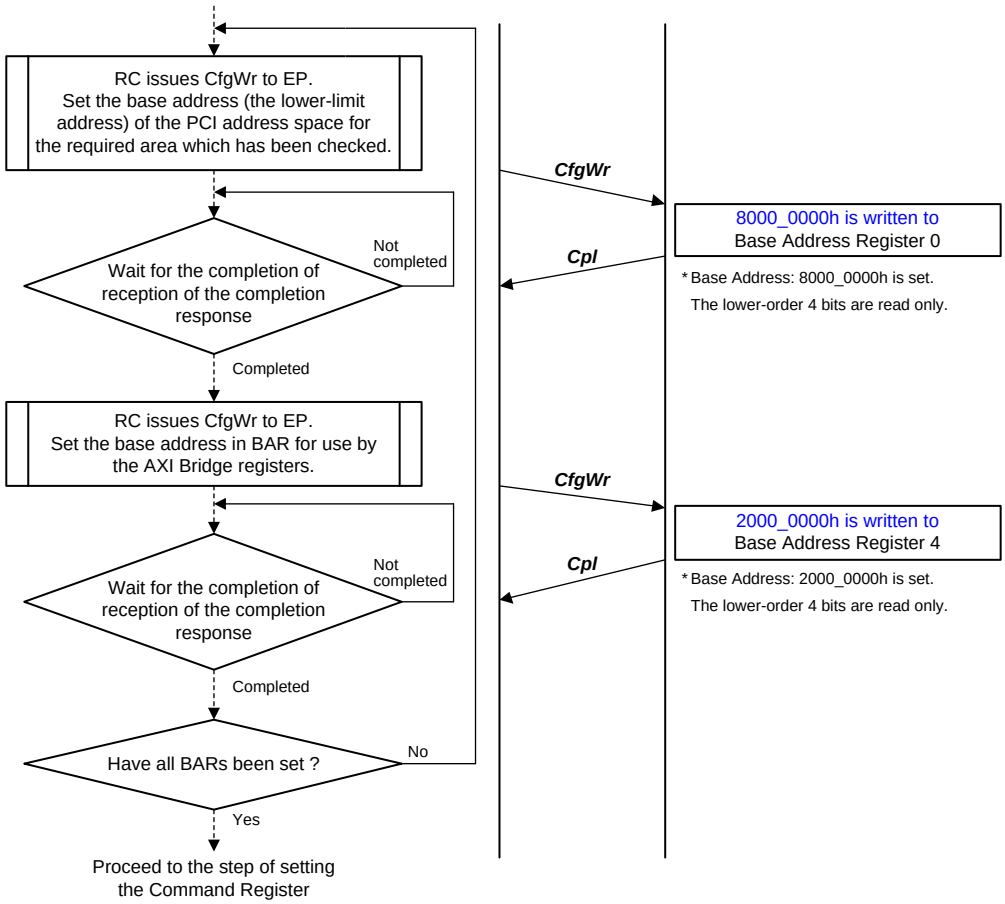
Figure 36.8-3 Example Settings for the PCIe Address Space

After issuing a configuration write request for writing all 1s (FFFF_FFFFh), a configuration read request is issued and if the result of reading is all 0s (0000_0000h), the given base address register (BAR) is judged to be reserved and the corresponding space is considered to be unused.

From the result of reading, software on the root complex side writes the base address (the lower-limit address) of the PCI address space to be allocated to the endpoint device by issuing a configuration write request.*[1] At this time, setting of a BAR for which the area requested by the endpoint device was found to be reserved and thus unused is not required.

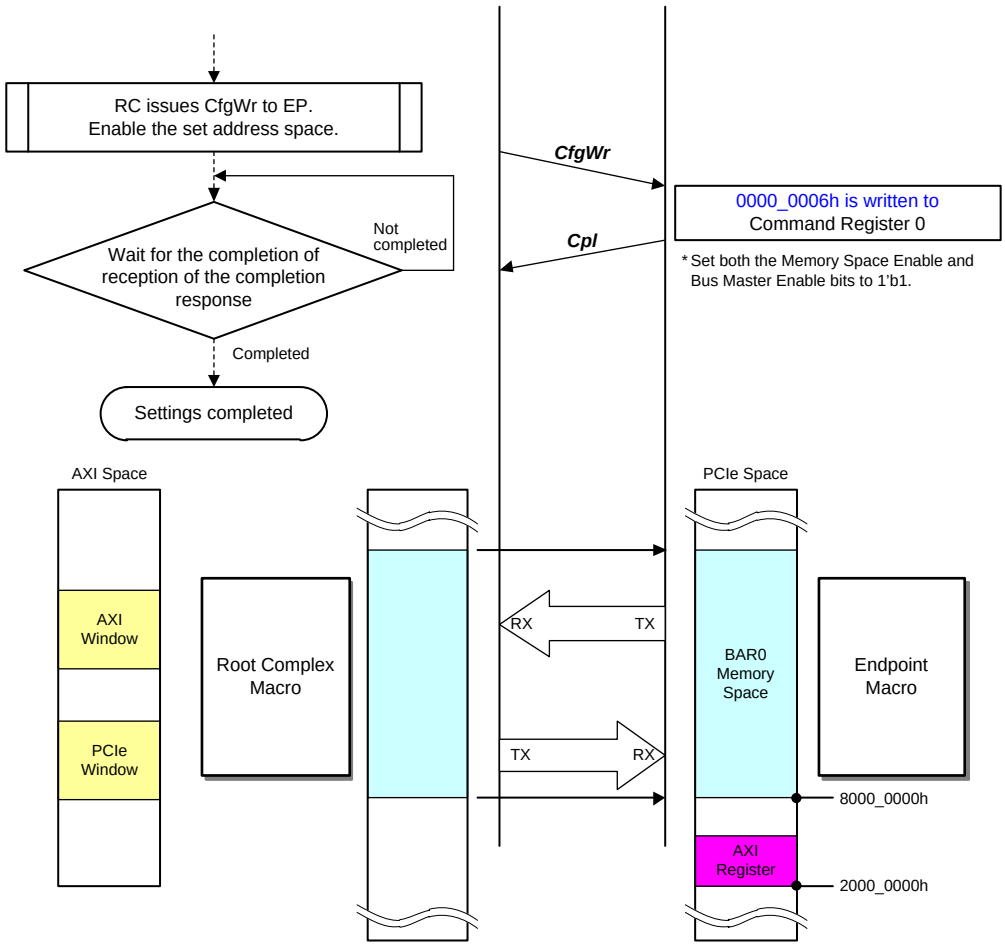
Also, if an address space which includes the other party has been prepared in advance, the above confirmation is not required. Set the base address directly.

Note 1. Setting a base address register to all 0s is prohibited.



Note: The values assigned in the figure (values in blue) are examples.

The completion of settings for the PCIe address space means that the root complex is ready for data transfer to the corresponding endpoint. Finally, set the Bus Master Enable bit and the Memory Space Enable bit of the given command register to enable the memory space.



Note: The values assigned in the figure (values in blue) are examples.

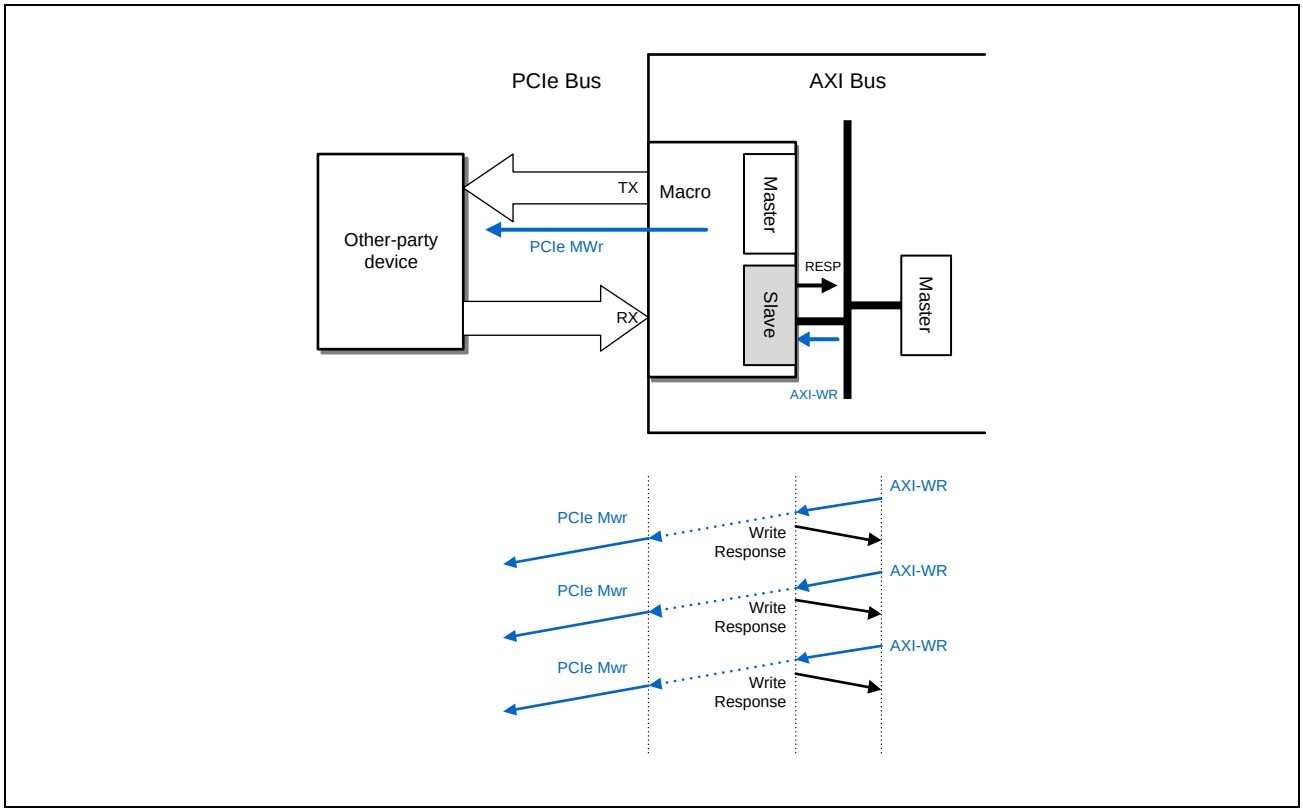
36.8.4 Data Transfer

This unit has one port each for master and slave operation as an AXI interface. For PCIe requests which can be issued through the master and slave ports, see **Section 36.7.2, Issuing of PCIe Requests and Register Access (by AXI)** and **Section 36.7.3, Initiation of AXI Transactions and Register Access (by PCIe)**.

The focus of this explanation is on normal memory data transfer.

36.8.4.1 PCIe MWr (when the AXI Slave is in Use)

A write transaction from the AXI bus (AXI-WR) via a window set as a PCIe window is converted into an MWr command (PCIe MWr) and then issued. If a PCIe MWr request is to be issued through the AXI interface slave port of the unit by using a DMAC, etc. external to the unit, the number of write transactions which can be accepted at a time is one, so the operation is as follows.



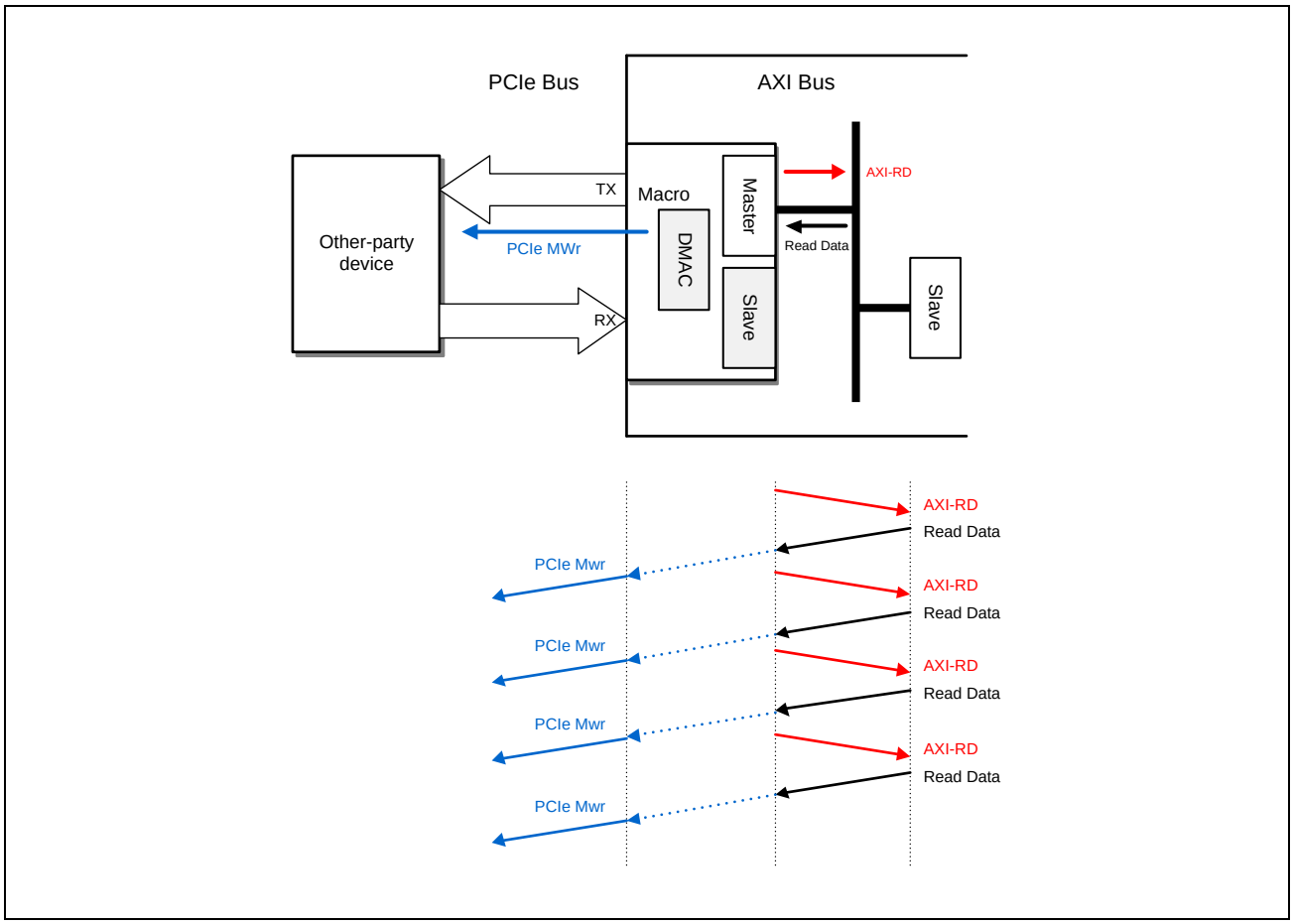
1. A write transaction from the AXI bus is issued through the AXI slave interface (write address channel, write data channel).
2. The transaction is converted into a PCIe MWr command and data are transferred to the other-party device via the PCIe bus.
3. After a wait for a response from the AXI slave interface (write response channel), a next AXI write transaction is issued.

A write response is issued after writing data to the transmission buffer (SRAM) within the unit. If this transmission buffer is full, the unit receives as much data as it can capture and then places the READY signal at the low level. Accordingly, the AXI bus may be placed in the hold state during transfer.

Since this depends not only on the specifications of the PCIe module (the number of lanes, rate, maximum payload size, etc.) but also on the size of the transmission buffer, the size of the reception buffer of the other-party device, and the external system configuration (the time for access to the external DRAM, etc.), care should be taken when considering the system configuration in general.

36.8.4.2 PCIe MWr (when the DMAC is in Use)

If a PCIe MWr request is to be issued through the AXI master port by using the DMAC within the unit, the number of requests which can be read by the internal DMAC is one transaction per channel, so the operation is as follows.



1. An AXI read (AXI-RD) request is issued through the AXI master interface (read address channel).
2. After the AXI master interface (read data channel) receives read data, this is converted into a PCIe MWr command and data are transferred to the other-party device via the PCIe bus.
3. Following the completion of the reception of read data, a next AXI-RD is issued.
4. The above steps are repeated until transfer of all bytes set in the DMA Size bits is completed.

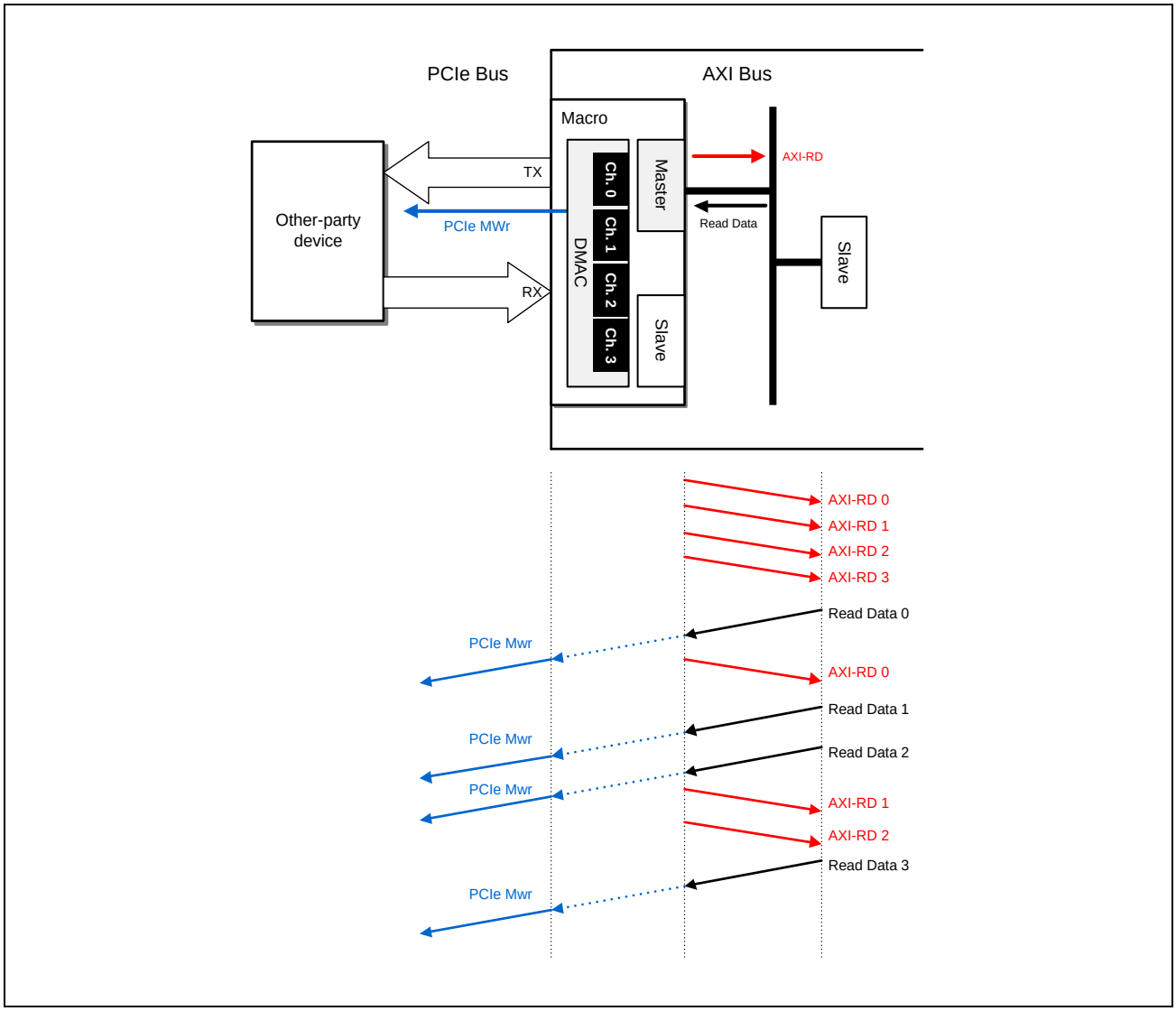
The read data channel checks that the data that have been read are valid and indicates the readiness of the data for reception. Even when the transmission buffer (SRAM) within the unit is full, the unit issues read requests through the read address channel. Also, it receives as much data as it can capture and places subsequent data in the non-receivable state. Accordingly, depending on the state of the transmission buffer, data may not be transferred regardless of a request having been issued, or the AXI bus may be placed in the hold state during transfer. This lengthens the period of waiting for data that have been read, leading to the deterioration of transfer performance as well as the deterioration of overall system performance.

Likewise, contention with write access by the slave interface and contention in write access between channels may decrease performance in transfer.

Since this depends not only on the specifications of the PCIe module (the number of lanes, rate, maximum payload size, etc.) but also on the size of the transmission buffer, the size of the reception buffer of the other-party device, and the

external system configuration (the time for access to the external DRAM, etc.), care should be taken when considering the system configuration in general.

The following is an example where the number of requests which can be read by the AXI master interfaced through four DMAC channels is 4.



1. An AXI read (AXI-RD0: DMAC ch. 0) request is issued through the AXI master interface (read address channel).
2. Since the number of requests which can be read by the unit = 4, AXI read requests are subsequently issued through DMAC ch. 1, ch. 2, and ch. 3.

   Note: No order of priority applies to the issuing of requests through these channels.

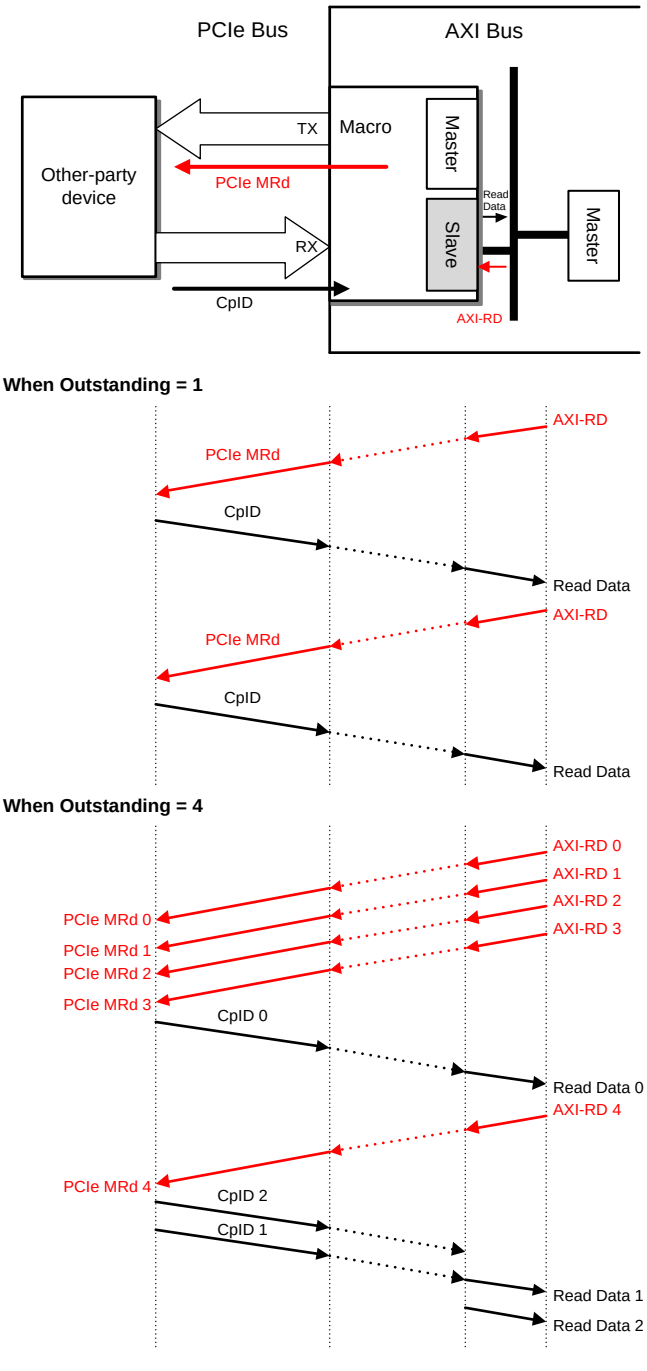
3. Following the completion of the reception of data read in response to the read request through ch. 0, ch. 0 is able to issue a next AXI-RD0.
4. The above steps are repeated until transfer of all bytes set in the DMA Size bits for each channel is completed.

Configuring data transfer as described above allows increased performance, although such a configuration complicates software control.

36.8.4.3 PCIe MRd (when the AXI Slave is in Use)

In usage as an AXI slave, memory read requests (PCIe MRd) are issued to the PCIe interface, a completion (CplD) is received from the PCIe interface, and an AXI write transfer (AXI-WR) is initiated (this unit supports eight outstanding transfers). Therefore, only the number of PCIe MRd requests that corresponds to this set number of outstanding transfers can be issued first, regardless of the reception of CplD. The received CplDs are stored in a data buffer (RAM) and then transferred through the AXI bus.

If a PCIe MRd is issued through the AXI interface slave port of the unit, the number of read requests which can be accepted by the AXI slave at a time = 1 to 8 corresponding to the PCIe section.



When outstanding = 1

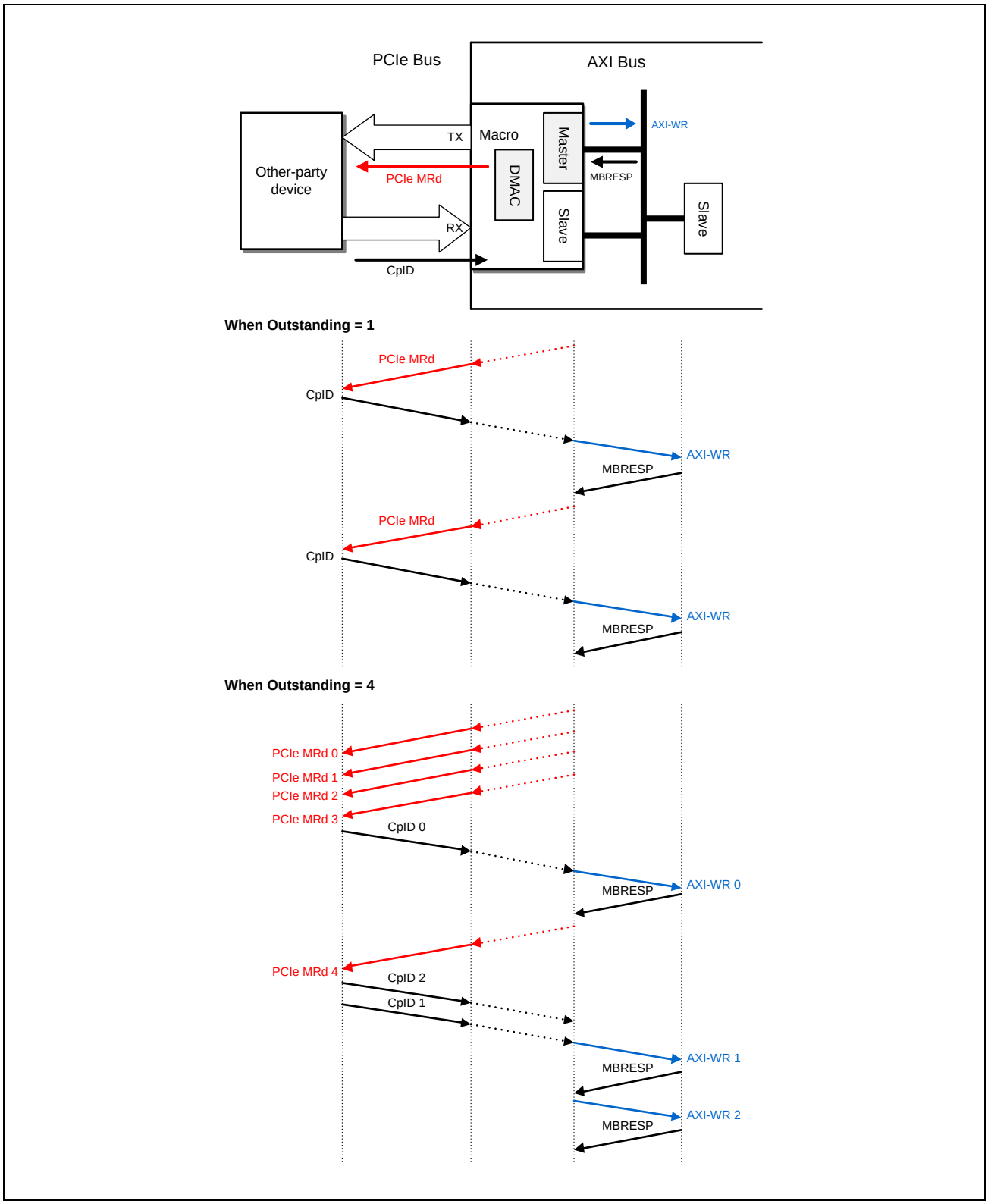
1. An AXI read transaction is issued through the AXI slave interface (read address channel).
2. A transaction is converted into a PCIe MRd command and the request for data reading is issued to the other-party device via the PCIe bus.
3. CplD is received from the other-party device and an AXI read response is issued through the AXI slave interface (read data channel).
4. Steps 1 to 3 are repeated.

When outstanding = 4

1. An AXI read transaction is issued through the AXI slave interface (read address channel).
2. A transaction is converted into a PCIe MRd command and the request for data reading is issued to the other-party device via the PCIe bus.
   Steps 1 and 2 can be repeated until up to four consecutive requests have been issued.
3. CplD is received from the other-party device and an AXI read response is issued through the AXI slave interface (read data channel).
   At this time, the PCIe module can operate with out-of-order transactions, so the order of CplDs from the other-party device may not be preserved. The unit also includes a buffer to support in-order transactions with the AXI bus. If this is used and the CplD for a preceding PCIe MRd is never returned, however, the next request cannot be issued and performance deteriorates accordingly.
   After that, steps 1 to 3 are repeated.

36.8.4.4 PCIe MRd (when the DMAC is in Use)

If a PCIe MRd request is to be issued by using the DMAC within the unit, the overall number of requests is also 1 to 8 when the DMAC is incorporated depending on the number of outstanding transfers.



1. Activate the internal DMAC through the AXI slave interface or from an other-party device.

When outstanding = 1

2. The DMAC issues a read request and this is converted to a PCIe MRd command within the unit. The request for data reading is issued to the other-party device via the PCIe bus.
3. CplD is received from the other-party device and an AXI write transaction is issued through the AXI master interface (write address channel, write data channel).
4. Following the completion of the AXI write transfer, a next request is issued.
5. Steps 2 to 4 are repeated until transfer of all bytes set in the DMA Size bits is complete

When outstanding = 4

2. The DMAC issues a read request and this is converted to a PCIe MRd command within the unit. The request for data reading is issued to the other-party device via the PCIe bus. Up to four consecutive requests can be issued.
3. CplD is received from the other-party device and an AXI write transaction is issued through the AXI master interface (write address channel, write data channel).
   At this time, the PCIe module can operate with out-of-order transactions, so the order of CplDs from the other-party device may not be preserved. The unit also includes a buffer to support in-order transactions with the AXI bus. If this is used and the CplD for a preceding PCIe MRd is never returned, however, the next request cannot be issued and performance deteriorates accordingly.
4. Following the completion of the AXI write transfer, a next request is issued.
5. Steps 2 to 4 are repeated until transfer of all bytes set in the DMA Size bits is completed.

36.8.5 PCIe Initialization Procedure

36.8.5.1 Initialization Procedure

(1) Root Complex Mode

For more information, contact a Renesas Electronics sales representative.

(2) Endpoint Mode

For more information, contact a Renesas Electronics sales representative.

36.8.5.2 Setting of Waveform Adjustment Register

For more information, contact a Renesas Electronics sales representative.

36.9 Points for Caution and Restrictions

36.9.1 Points for Caution and Prohibited Items in the Issuing of Requests

The following describes the restrictions in the issuing of various requests.

(1) Prohibition of fixed bursts of 2 or more beats

Fixed bursts for 2 or more beats are prohibited. If an attempt to use these is made, an OKAY response is returned to the AXI bus, but this may lead to issuing of the unexpected requests to the PCIe side, or unexpected register access which will change register values, and so on.

(2) Points for caution in the issuing of special requests

The requests listed below are issued by access to the internal registers. The registers are only accessible from the AXI side and writing to them while requests are being processed is prohibited. Attempted access from the PCIe side will be ignored.

[Special Requests]
- Zero-Length Memory Read Request
- Configuration Read
- Configuration Write
- Message Request
- Message Request with data payload

CAUTION: Do not issue a special request for which issuing of the request is prohibited. Operation is not guaranteed if this is done.

36.9.2 Ordering Specifications of Received Non-Posted and Posted Requests

In the specifications of this unit, a non-posted request is not overtaken by a posted request on the receiving side.

Requests received from another party are output to the higher-level bus in the order of reception.

36.9.3 Caution when Changing the Speed Spontaneously by the EP Unit

Follow the procedure below. The following control bits are present in the PCI Core Control 2 Register and PCI Core Status 2 Register among the AXI-Bridge registers.

1. Wait until the home node is placed in the L0 state.
2. Read the value of the STATE_DATA_RATE_IDENTIFIER_RECEIVED bit to check the supported speed of the other-party node.
3. If the home node supports the speed to which the other-party node wants to change, set the UI_LINK_SPEED_CHANGE[1:0] bits and assert the UI_LINK_SPEED_CHANGE_REQ bit.
4. Wait for the UI_LINK_SPEED_CHANGE_DONE bit to be asserted (wait for the completion).

CAUTION: UI_LINK_SPEED_CHANGE_REQ is retained until UI_LINK_SPEED_CHANGE_DONE is asserted. It should be de-asserted after checking the assertion of UI_LINK_SPEED_CHANGE_DONE.

36.9.4 Error Processing of Unsupported Requests

The following describes the flow of processing for error reporting and error logging.

(1) Access that straddles a 4-KB boundary

Data transfer to a memory space which straddles a 4-KB boundary cannot proceed (this is stipulated by the PCI Express Base Specification). In our unit, the reception of a memory write or read request for a memory space which straddles a 4-KB boundary is handled as a malformed TLP.

(2) RCB violations

The PCI Express Base Specification states that error processing in response to violations of the read completion boundary (RCB) is optional. The PCIe module of this LSI chip does not support the detection of RCB violations at the time of the reception of completion responses. Support for this function should be handled by the user logic.

(3) Error processing in response to byte enable fields

The PCI Express Base Specification states that error processing in response to Byte Enable fields is optional. Our unit does not support the detection of errors in the form of violations of Byte Enable rules. Support for this function should be handled by the user logic.

(4) Request that extends beyond the base address boundary

This core does not detect a request that starts within the range set in the Base Address Register but extends beyond the boundary from the base address as an error. Such a request should be handled by the user logic

(5) Processing when a TPL that is ready to be transferred by the transmitter is a malformed TLP

Even if malformation of a TLP that is ready to be transferred by the transmitter is detected, due to the detection of parity errors when it is read from the FIFO buffer and so on, this unit does not suspend the transmission of such a TLP. Received malformed TLPs must be handled appropriately by other-party devices.

36.9.5 Processing on Reception of the Message

The following lists the messages to be detected as a silent drop or UR on reception of the given message.

Table 36.9-1 Operations on Message Reception

Received Message	Root Complex	Endpoint
Assert_INTx	Normal processing	Silent Drop
Deassert_INTx	Normal processing	Silent Drop
ERR_COR	Normal processing	Silent Drop
ERR_NONFATAL	Normal processing	Silent Drop
ERR_FATAL	Normal processing	Silent Drop
UNLOCK	Silent Drop	Silent Drop
Set_Slot_Power_Limit	Silent Drop	Normal processing
Vendor_Defined_Type0	UR	UR
Vendor_Defined_Type1	Silent Drop	Silent Drop
Ignore	Silent Drop	Silent Drop
LTR	UR	UR
OBFF	UR	UR
PM_PME	Normal processing	Silent Drop
PME_TO_Ack	Normal processing	Silent Drop
PM_Active_State_Nak	Silent Drop	Normal processing
PME_Turn_Off	Silent Drop	Normal processing
PTM_Request	UR	UR
PTM_Response	UR	UR
PTM_ResponseD	UR	UR
Invalidate_Request	Silent Drop	UR
Invalidate_Completion	Normal processing	Silent Drop
Page_Request	UR	UR
Page_Response	UR	UR

Note: Silent Drop: Normal completion, data are not reflected
UR: Unsupported Request

36.9.6 Other Points for Caution

(1) Access after the de-assertion of the reset signal

When a cycle of writing starts before the value of the SAWREADY bit has become 1b following the de-assertion of the reset signal, access in the second and subsequent cycles produces slave errors.

After the reset signal has been de-asserted, do not assert the SAWVALID signal until SAWREADY has become 1.

(2) Point for caution at times of register writing

In some cases of writing 2DW or more and skipping over with the use of byte enable to a register from the AXI side, writing might not proceed as expected.

Using a pin reset or register reset from the AXI side as a non-consecutive SWSTRB, restricts writing to no more than 1DW (32 bits).

(3) Point for caution on register reading

In the case of reading a register from the AXI side, values read from invalid byte lanes are from undefined outputs (meaningless garbage data).

(4) Generation of unexpected correctable errors

A correctable error may be detected at the time of EIOS reception following low power state transitions of this unit such as from L0s to L1. If this happens, processing to send a message or assert an interrupt flag signal is to proceed. Take care on this point and respond appropriately so that a correctable error is not handled as a fatal error (a mask setting by a register to switch the notification of unexpected correctable errors off is recommended).

(5) Reset interval in transitions from a hot reset to detection in RC mode

In generations of PCI Express after Gen1, at the time of transitions from a hot reset to detection in accord with the operating rate, the base specification prescribes securing a 1-ms waiting interval for changes to the rate, so secure a reset interval of 1 ms.

Section 37 Ethernet MAC Interface (ETHER)

This section describes the functions of the Ethernet MAC interface (ETHER).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

37.1 Overview

The EthernetAVB-IF includes an Ethernet controller (MAC) that conforms to the definition of the MAC (Media Access Control) layer for Ethernet in the IEEE 802.3 standard.

When connected with a physical-layer LSI chip (PHY-LSI) that complies with the standard, the MAC is able to transmit and receive Ethernet (IEEE 802.3) frames. The MAC has a single MAC layer interface.

The EthernetAVB-IF has a dedicated direct memory access controller (AVB-DMAC) for transferring transmitted Ethernet frames to and received Ethernet frames from respective storage areas in the User RAM (URAM) at high speed.

The AVB-DMAC is compliant with the following three standards formulated for IEEE 802.1BA: the IEEE 802.1AS timing and synchronization protocol, the IEEE 802.1Qav real-time transfer, and the IEEE 802.1Qat stream reservation protocol.

In this section, URAM refers to the local RAM and external memory for the SoC.

37.1.1 Features

Table 37.1-1 lists the specifications of the EthernetAVB-IF module.

Table 37.1-1 Specifications (Functions)

Item	Description
Protocol	Flow control conforming with the IEEE 802.3x standard
Data transmission and reception	Transmission and reception of Ethernet (IEEE 802.3) frames
Transfer speed	Supports transfer at 100 and 1000 Mbps
Mode	Full-duplex mode
Interface	Supports the GMII (Gigabit Media Independent Interface), MII
Summary of the EthernetAVB-IF function	• An intelligent frame separation DMAC (AVB-DMAC) conforming with the following standards stipulated for IEEE 802.1BA: IEEE 802.1AS (time synchronization protocol), IEEE 802.1Qav (real-time transfer), IEEE 1722 (AVTP presentation timestamp), IEEE 802.1Qat is supported by software. • Descriptor management system Identification and sorting of frame data, and extraction and gathering of valid data Controllable interrupt frequency (reducing the load on the CPU)
Transmit/Receive FIFO	For transmission: 16 Kbytes For reception: 8 Kbytes
Magic Packet™	Detection of Magic Packets™*1

Note 1. Magic Packet™ is a trademark of Advanced Micro Devices, Inc.

Section 38 IIC Bus Interface (IIC)

This section describes the functions of the IIC bus interface (IIC).

38.1 Functional Overview

This section describes the functions of the IIC bus interface (IIC).

The IIC has a total of four channels from ch. 0 to ch. 3. Of those, ch. 1 and to ch. 3 are for use with the ISP support package, so using registers related to those channels is prohibited.

38.1.1 Features

- This interface uses two lines, the serial clock (SCL) and the serial data bus (SDA), to transfer data to and from multiple devices.
- The data length is 8 bits.
  (However, one bit of the ACK signal is attached after the 8-bit data.)
- This interface conforms to the IIC bus format (THE I2C-BUS SPECIFICATION VERSION 2.1 issued by Philips Semiconductors in January 2000). (However, it does not support the high speed mode: 3400 kbits/s.)
- Supports the standard mode (maximum transfer rate: 100 kbits/s) and the fast mode (maximum transfer rate: 400 kbits/s).
- The input clock consists of a single PCLK.
- The “High” level width and “Low” level width of the serial clock (SCL) can be set.
- The bus line status can be used to determine “start condition” and “stop condition”.
- The double buffers allow data to be sent and received continuously.

38.1.2 Connection Configuration

Figure 38.1-1 shows the connection configuration of the IIC.

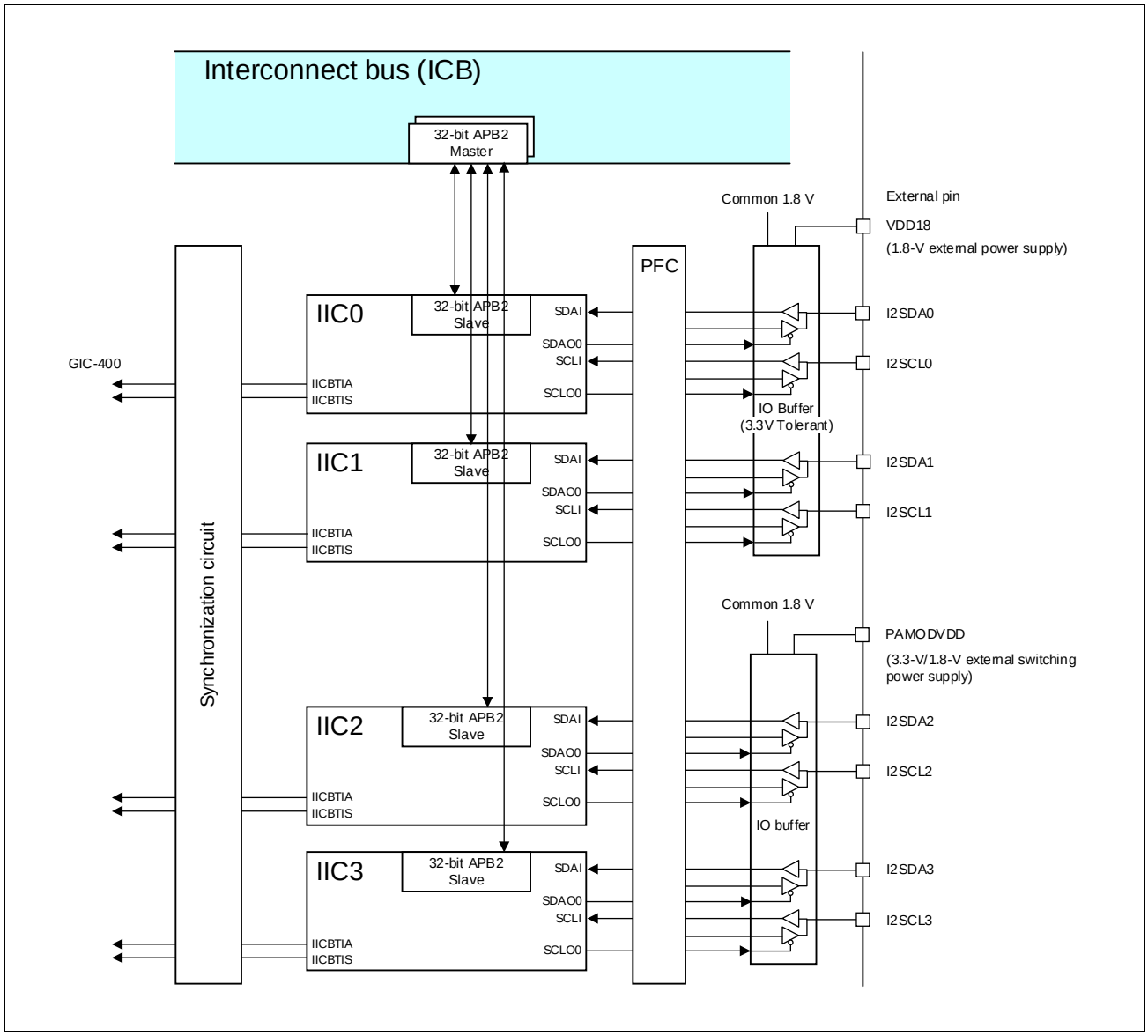


Figure 38.1-1 Connection Configuration

38.2 Block Diagram

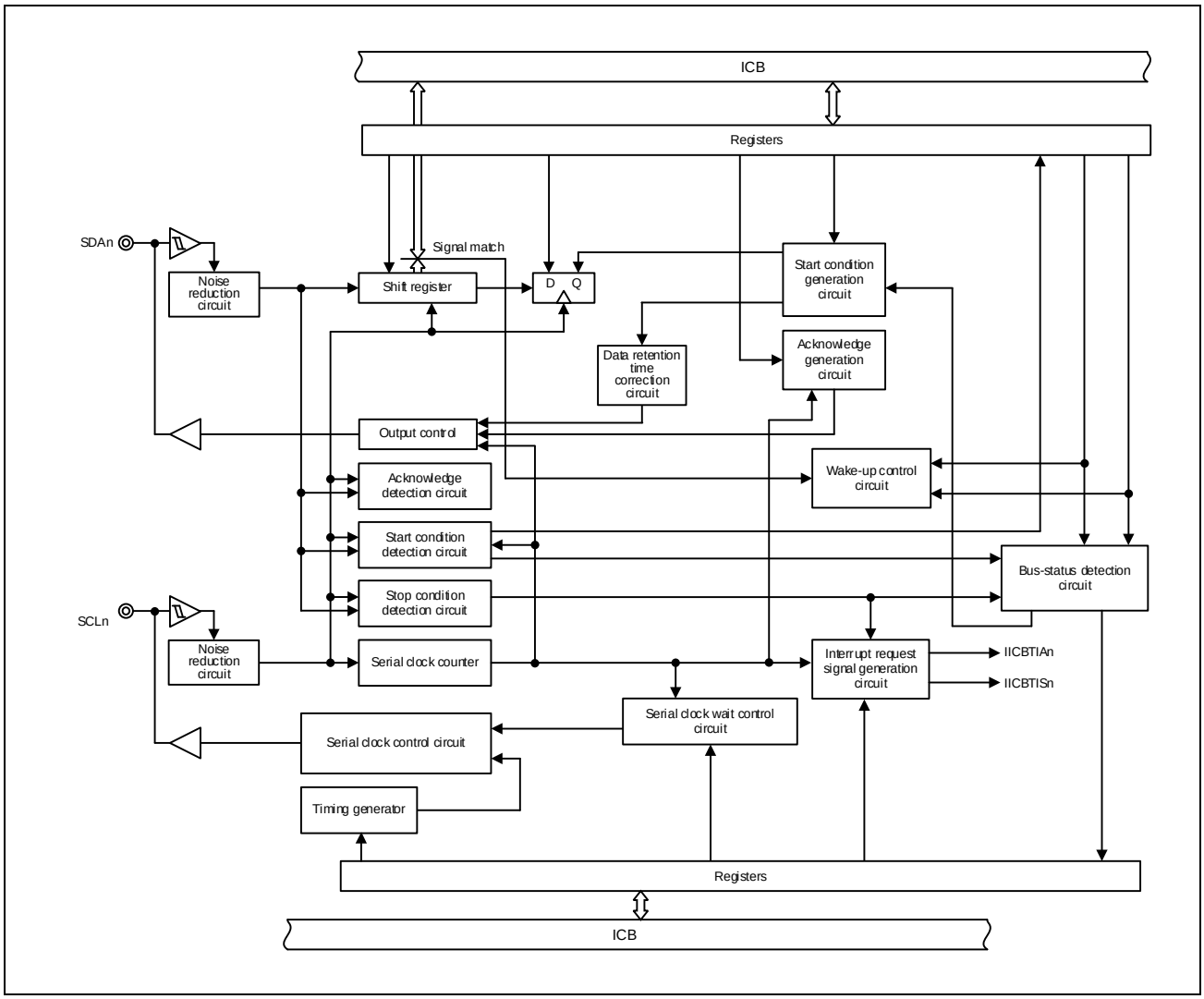


Figure 38.2-1 Block Diagram

38.3 Pin Functions

38.3.1 List of Internal Pins

Table 38.3-1 lists the internal pins of the IIC.

Table 38.3-1 List of Internal Pins

Classification	Pin name	I/O	Function
IIC bus pin	SCLI	Input	Serial clock input
	SDAI	Input	Serial data input
	SCLO0	Output	Serial clock output When the operation is stopped (IICB0 Control Register 0: IICB0IICE = 0b), “High” level is output.
	SDAO0	Output	Serial data output When the operation is stopped, “High” level is output.
Interrupt pin	IICBTIA	Output	Data transmission/reception interrupt output The signal is generated when transmitting and receiving addresses and data. The interrupt is a pulse of one clock cycle width in PCLK.
	IICBTIS	Output	Status interrupt output This signal is generated by arbitration loss, NACK reception, or detection of a stop condition. The interrupt is a pulse of one clock cycle width in PCLK.

38.4 Register Description

38.4.1 Base Addresses of Registers

For the base addresses of the registers (< IIC0_S0_base>, < IIC1_S0_base>, < IIC2_S0_base>, < IIC3_S0_base>), see the Address Map section.

38.4.2 List of Registers

Table 38.4-1 is a list of registers.

Table 38.4-1 List of Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
00h	IICB data register	IICm_IICB0DAT	0000_0000h	32
04h	IICB slave address register	IICm_IICB0SVA	0000_0000h	32
08h	IICB control register 0	IICm_IICB0CTL0	0000_0000h	32
0Ch	IICB trigger register	IICm_IICB0TRG	0000_0000h	32
10h	IICB status register 0	IICm_IICB0STR0	0000_0000h	32
14h	IICB status register 1	IICm_IICB0STR1	0000_0000h	32
18h	IICB status clear register	IICm_IICB0STRC	0000_0000h	32
20h	IICB control register 1	IICm_IICB0CTL1	0000_0000h	32
24h	IICB low-level width setting register	IICm_IICB0WL	0000_03FFh	32
28h	IICB high-level width setting register	IICm_IICB0WH	0000_03FFh	32
2Ch	IICB emulation read register	IICm_IICB0EDAT	0000_0000h	32
30h	IICBS shift register	IICm_IICB0DATS	0000_0000h	32

Note: (m = 0 to 3)

38.5 Register Descriptions

The function description of each register is given below.

The prefix (IICm_) of the register names is omitted in the register descriptions and the field descriptions in this section.

38.5.1 IICB Data Register (IICm_IICB0DAT) (m = 0 to 3)

The IICB0DAT register is used to send and receive transfer data.

This register is also initialized by changing the IICB0CTL0.IICB0IICE bit from 1 to 0 and the IICB0CTL0.IICB0IICE bit from 0 to 1.

Note 1: To become a master in single transfer mode or continuous transfer mode, set the IICB0TRG.IICB0STT bit = 1 and then write to the IICB0DAT register only once to transfer the address and communication direction.

Note 2: When transferring data in single transfer mode, writing to the IICB0DAT register in the communication state excluding the wait period is prohibited.

Note 3: When transferring data in continuous transfer mode, write to the IICB0DAT register only once for each IICBTIA0 interrupt request signal.

Note 4: Do not read the IICB0DAT register during transmission. Similarly, do not write to the IICB0DAT register during a receive operation.

Access Size: 32 bits

Address(es): <IIC0_S0_base> + 0000h
<IIC1_S0_base> + 0000h
<IIC2_S0_base> + 0000h
<IIC3_S0_base> + 0000h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IICB0DAT[7:0]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 38.5-1 IICm_IICB0DAT Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.

Table 38.5-1 IICm_IICB0DAT Register Contents (2/2)

Bit Position	Bit Name	Description
7 to 0	IICB0DAT[7:0]	During reception, the received data is retained. During transmission, the transmission data is written. The wait state is released by accessing the IICB0DAT register. • Single transfer mode: – When writing to the IICB0DAT register • Continuous transfer mode: – When writing to the IICB0DAT register – When the IICB0DAT register is read when it is not waiting due to NACK reception in the wait state during data transfer

38.5.2 IICB Slave Address Register (IICm_IICB0SVA) (m = 0 to 3)

The IICB0SVA register stores the IICB0 bus slave address.

Note: Writing to IICB0SVA is prohibited when IICB0CTL0.IICB0IICE = 1.

Access Size: 32 bits

Address(es): <IIC0_S0_base> + 0004h
<IIC1_S0_base> + 0004h
<IIC2_S0_base> + 0004h
<IIC3_S0_base> + 0004h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IICB0SVA[7:1]							—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 38.5-2 IICm_IICB0SVA Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 1	IICB0SVA[7:1]	Stores the IICB bus slave address. By comparing the received address with the IICB0SVA register, address match or address mismatch is judged. If the received address matches the IICB0SVA register, the IICB0STRn.IICB0SSCO bit is set to 1b.
0	—	Reserved. This bit is read as 0b. The write value should always be 0b.

38.5.3 IICB Control Register 0 (IICm_IICB0CTL0) (m = 0 to 3)

The IICB0CTL0 register controls the operation of this unit.

Access Size: 32 bits

Address(es): <IIC0_S0_base> + 0008h
<IIC1_S0_base> + 0008h
<IIC2_S0_base> + 0008h
<IIC3_S0_base> + 0008h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IICB0IICE	—	—	IICB0MDTX1	IICB0MDTX0	IICB0SLSI	IICB0SLWT	IICB0SLAC
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 38.5-3 IICm_IICB0CTL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7	IICB0IICE	Specifies whether to enable or disable the operation of this unit. 0b: Disable 1b: Enable The following registers are synchronously reset by changing the IICB0CTL0.IICB0IICE bit from 1b to 0b or the IICB0CTL0.IICB0IICE bit from 0b to 1b. • IICB0DAT, IICB0STR0 register When the IICB0CTL0.IICB0IICE bit = 0b, the SCLm, SDAm pins are in a high impedance state.
6, 5	—	Reserved. These bits are read as 0b. The write value should always be 0b.
4	IICB0MDTX1	Specifies the transfer mode when extension code is detected in the slave. 0b: Single transfer mode: Each transfer enters a wait state according to the setting of the IICB0CTL0.IICB0SLWT bit. 1b: Continuous transfer mode: Transfer that allows continuous communication without entering the wait state by reading or writing to the IICB0DAT register each time a data transmission/reception interrupt request signal (IICBTIA) is generated. *Note*: Rewriting is enabled only when the IICB0CTL0.IICB0IICE bit = 0b.
3	IICB0MDTX0	Specifies the transfer mode when the address matches between the master and slave. 0b: Single transfer mode 1b: Continuous transfer mode *Note*: Rewriting is enabled only when the IICB0CTL0.IICB0IICE bit = 0b.

Table 38.5-3 IICm_IICB0CTL0 Register Contents (2/2)

Bit Position	Bit Name	Description
2	IICB0SLSI	Specifies whether or not to generate a status interrupt request signal (IICBTIS) when a stop condition is detected. 0b: Disable IICBTIS signal generation when stop condition is detected. 1b: Enables IICBTIS signal generation when stop condition is detected. Set IICB0CTL0.IICB0SLSI bit = 1b when communicating under any of the following conditions. • When communicating as a master with the communication reservation function enabled. • When participating in communication as a slave. • When there is a possibility of losing arbitration (when operating as a master in a multi-master environment)
1	IICB0SLWT	Controls the timing of wait and interrupt request generation. 0b: Transition to wait state and interrupt request generation at the falling edge of the 8th clock during single transfer. 1b: Transition to wait state and interrupt request generation at the falling edge of the 9th clock during single transfer. The IICB0CTL0.IICB0SLWT bit controls the transition to wait and interrupt request generation at the 8th and 9th clock timing during data transfer. During address transfer, regardless of the IICB0CTL0.IICB0SLWT bit setting, the transition to wait and interrupt request generation conditions are as follows. • When single transfer mode: [*Master*] Generates a data transmission/reception interrupt request signal (IICBTIA) when the falling edge of the 9th clock is detected, and enters the wait state. [*Slave*] When the addresses match, the IICBTIA signal is generated when the falling edge of the 9th clock is detected, and a wait state is entered. If the addresses do not match, the IICBTIA signal is not generated and the wait state is not entered. • When continuous transfer mode: In continuous transfer mode, the wait timing does not affect the setting of the IICB0CTL0.IICB0SLWT bit. – Reception: Wait state at falling edge of 8th clock – Transmission: Wait state at falling edge of 9th clock *Note*: In single transfer mode, rewriting is enabled only when the IICB0CTL0.IICB0IICE bit = 0b or during the wait period.
0	IICB0SLAC	Control acknowledgement. 0b: Disable [*Master*] Acknowledge is not generated during data reception (SDAm pin is in high impedance state). [*Slave*] Acknowledge is not generated during data transfer with the matching address (SDAm pin is in high impedance state). 1b: Enable [*Master*] Acknowledgment during data reception is generated (SDAm pins are low level). [*Slave*] Generates an acknowledge during data transfer with the same address (SDAm pins are low level). In slave mode, if the address matches, an acknowledge during address transfer is generated regardless of the value of the IICB0CTL0.IICB0SLAC bit (SDAm pin is low level). An acknowledge is not always generated when data is transmitted or communication is not participated (SDAm pin is in a high impedance state).

38.5.4 IICB Trigger Register (IICm_IICB0TRG) (m=0 to 3)

The IICB0TRG register is used to set the trigger for this unit.

Access Size: 32 bits

Address(es): <IIC0_S0_base> + 000Ch
<IIC1_S0_base> + 000Ch
<IIC2_S0_base> + 000Ch
<IIC3_S0_base> + 000Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	IICB0LRET	IICB0WRET	IICB0STT	IICB0SPT
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 38.5-4 IICm_IICB0TRG Register Contents (1/3)

Bit Position	Bit Name	Description
31 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3	IICB0LRET	Communication evacuation trigger bit 0b: The read value is always 0b, and writing 0b is ignored. 1b: Evacuates from current communication and enters standby mode. Cleared automatically after execution. When IICB0TRG.IICB0LRET bit = 1b, the following is performed. • Set SCLm, SDAm to high impedance state (communication standby state). • The IICB0SSMS, IICB0SSDR, IICB0SSWT, IICB0SSEX, IICB0SSC0, IICB0SSTR, IICB0SSAC, IICB0SSRS, and IICB0SSST bits in the IICB0STR0 register are cleared. • If the IICB0TRG.IICB0STT bit = 1b (preparation for start condition Issuance) or IICB0TRG.IICB0SPT bit = 1b (preparation for issuance of stop condition) is set, generation of start and stop conditions is stopped. When the communication is saved in the communication reservation state, the communication reservation state is released. To use the master, set the IICB0TRG.IICB0STT bit to 1b again. *Note*: If IICB0TRG.IICB0LRET bit = 1b is set during master operation (IICB0STR0.IICB0SSMS bit = 1b), the bus is released. Since the serial clock is not output, mismatch occurs in the communication on the slave side.
2	IICB0WRET	Trigger bit to release wait state 0b: Do not release wait 1b: Release wait and resume communication. Automatically cleared after execution. If the wait is canceled by setting IICB0TRG.IICB0WRET bit = 1b during the 9th clock wait period, set IICB0STR0.IICB0SSTR bit = 0b and set SDAm = high impedance. As a result, the external master is ready to issue a stop condition or start condition. When not in the wait state (IICB0STR0.IICB0SSWT bit = 0b), setting 1b has no effect. In addition to the IICB0TRG.IICB0WRET bit = 1b, there are other wait release conditions.

Table 38.5-4 IICm_IICB0TRG Register Contents (2/3)

Bit Position	Bit Name	Description
1	IICB0STT	Start condition trigger bit 0b: No start condition is generated. 1b: Start condition is generated (It is automatically cleared after setting 1b). The IICB0TRG.IICB0STT bit can be set to 1b under the following conditions. Master status (IICB0STR0.IICB0SSMS bit = 1b) • Single transfer mode: – 9th clock wait period (both address transfer and data transfer). – When data is received, set IICB0CTL0.IICB0SLAC bit = 0b, and can be set only after the end of reception is communicated to the slave. • Continuous transfer mode: – During the wait period for the 9th clock of address transfer. – During Sending data. – When data is received, set IICB0CTL0.IICB0SLAC bit = 0b, and can be set only after the end of reception is communicated to the slave. *Note*: To generate the start condition, after cancelling wait, if the 9th clock is in wait, otherwise after the falling edge of the 9th clock is detected, secure SCLm low level width period and set SDAm and SCLm to high level. After waiting for start condition setup time, set SDAm to low level. Slave state or communication standby state (IICB0STR0.IICB0SSMS bit = 0b) • IICB0STR0.IICB0SSBS bit = 0b (bus released state) After the bus free time elapses, start condition is generated by changing SDAm from high level to low level (in this case, SCLm output high level). After that, secure the start condition hold time and set SCLm = low level. • IICB0STR0.IICB0SSBS bit = 1b (bus communication status) This state indicates that this unit is not the master and communication is performed on the bus. – When communication reservation function is enabled (IICB0CTL1.IICB0SLRS bit = 0b): After the bus is released (stop condition is detected), a start condition is generated after the bus free time is secured. However, even if the bus free time has not elapsed, if a start condition is detected, SDAm is set to low level immediately without waiting for the bus free time. – When the communication reservation function is disabled (IICB0CTL1.IICB0SLRS bit = 1b): The ICB0STR0.IICB0STCF bit is set to 1b and no start condition is generated. *Note*: Slave state or communication standby state is the operation with the IICB0STR0.IICB0SSBS bit value when the IICB0TRG0.IICB0STT bit = 0b is set. Even if the IICB0TRG0.IICB0STT bit is set to 1b after confirming the IICB0STR0.IICB0SSBS bit value by register read, the IICB0STR0.IICB0SSBS bit value may be different from the confirmed value. Start condition generation processing is started by setting the IICB0TRG.IICB0STT bit = 1b, but if the following conditions are detected, start condition generation processing is stopped and start condition generation will not be performed. • IICB0CTL0.IICB0IICE bit = 0b write • IICB0TRG.IICB0LRET bit = 1b write • Arbitration loss detection • IICB0TRG.IICB0STT bit operating as master in continuous transfer mode = IICB0TRG.IICB0SPT bit = 1b write after 1b write • When IICB0TRG.IICB0STT bit = 1b write and IICB0TRG.IICB0SPT bit = 1b write operating as master in continuous transfer mode are performed during the same data transfer period (In this case, IICB0TRG.IICB0STT bit = 1b write is enabled).

Table 38.5-4 IICm_IICB0TRG Register Contents (3/3)

Bit Position	Bit Name	Description
1	*<Continued from the previous page>*	*Note 1.* When start is enabled in the initial communication state (IICB0CTL1.IICB0SLSE bit = 1b), if the IICB0TRG.IICB0STT bit is set to 1b, a start condition is generated regardless of the bus status. If other communication is being performed at this time, the communication may be destroyed. *Note 2.* Simultaneous setting with the IICB0TRG.IICB0SPT bit is prohibited.
0	IICB0SPT	Stop condition trigger 0b: Stop condition is not generated. 1b: Generate a stop condition (automatically clear after setting 1b). The IICB0TRG.IICB0SPT bit can be set to 1b under the following conditions during communication as a master. • Single transfer mode: – 9th clock wait period (both address transfer and data transfer). – When data is received, set IICB0CTL0.IICB0SLAC bit = 0b, and can be set only after the end of reception is communicated to the slave. • Continuous transfer mode: It is permitted to set the IICB0TRG.IICB0SPT bit to 1b in the following states. – During the wait period for the 9th clock of address transfer. – During sending data. – NACK (IICB0STR0.IICB0SSAC bit = 0b) is received during the wait period of the 9th clock for data reception. The stop condition can be generated by the following procedure. In the wait state, after releasing the wait, SCLm are released with SDAm = low level output, and wait for SCLm = high level and SDAm = low level. Then, after tSU: STO time elapses, SDAm are set to high level. By setting the IICB0TRG.IICB0SPT bit = 1b, stop condition generation processing is started, but when the following conditions are detected, stop condition generation processing is stopped and stop condition generation will not be performed. • IICB0CTL0.IICB0IICE bit = 0b write • IICB0TRG.IICB0LRET bit = 1b write • Stop condition detection • Arbitration loss detection • IICB0TRG.IICB0SPT bit operating as master in continuous transfer mode = IICB0TRG.IICB0STT bit = 1b write *Note 1.* Setting 1b to the IICB0TRG.IICB0SPT bit is prohibited when in slave mode (IICB0STR0.IICB0SSMS bit = 0b). *Note 2.* Simultaneous setting with the IICB0TRG.IICB0STT bit is prohibited.

38.5.5 IICB Status Register 0 (IICm_IICB0STR0) (m=0 to 3)

The IICB0STR0 register indicates the status of this unit and the bus.

When the IICB0CTL0.IICB0IICE bit = 0b, write operation is also possible.

This register is also initialized by changing the IICB0CTL0.IICB0IICE bit from 1 to 0 and the IICB0CTL0.IICB0IICE bit from 0 to 1.

Access Size: 32 bits

Address(es): <IIC0_S0_base> + 0010h
<IIC1_S0_base> + 0010h
<IIC2_S0_base> + 0010h
<IIC3_S0_base> + 0010h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IICB0SSMS	—	IICB0SSDR	IICB0SSWT	IICB0SSEX	IICB0SSCO	IICB0SSTR	IICB0SSAC	IICB0SSRS	IICB0SSBS	IICB0SSST	IICB0SSSP	—	—	IICB0STCF	IICB0ALDF
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 38.5-5 IICm_IICB0STR0 Register Contents (1/6)

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15	IICB0SSMS	Master status check flag 0b: Not master state 1b: Master state <Set condition> • When a start condition is detected after writing IICB0TRG.IICB0STT bit = 1b. <Clear conditions> • When writing IICB0TRG.IICB0LRET bit = 1b. • When a stop condition is detected. • When arbitration loss is detected. If the set condition and clear condition overlap, the clear condition takes precedence.
14	—	Reserved. This bit is read as 0b.

Table 38.5-5 IICm_IICB0STR0 Register Contents (2/6)

Bit Position	Bit Name	Description
13	IICB0SSDR	IICB0DAT register status flag 0b: No unprocessed data remains in the IICB0DAT register. 1b: Unprocessed data remains in the IICB0DAT register. During receive operation: The received data remains unread in the IICB0DAT register. During transmission: Data written to the IICB0DAT register is not transferred to the shift register. *Note*: In single transfer mode or continuous transfer mode, this bit is never set. This is because in single transfer mode (transmission), writing to the IICB0DAT register is permitted only during the wait period. <Set conditions> ● The IICB0DAT register being written when IICB0STR0.IICB0SSWT bit = 0b during address transfer and data transfer (When writing data to the IICB0DAT register in the master mode, 1 is not set even if the IICB0STR0.IICB0SSWT bit = 0b because it is transferred directly to the shift register). ● At the falling edge of the 9th clock when the address coincides with the slave. ● When the IICB0CTL0.IICB0SLWT bit = 0b and single mode reception, at the falling edge of the 8th clock during data reception. ● In continuous transfer mode (receive), at the falling edge of the 8th clock regardless of the value of the IICB0CTL0.IICB0SLWT bit. ● When IICB0CTL0.IICB0SLWT bit = 1b, at the falling edge of the 9th clock during data reception. <Clear conditions> Clear condition that takes precedence over set condition. ● When writing 1 to the IICB0TRG.IICB0LRET bit. ● When arbitration loss is detected. ● At the falling edge of the 9th clock during address transfer by the master. ● When the IICB0CTL0.IICB0SLWT bit = 0b and continuous transmission, the falling edge of the 8th clock during data transmission. ● When IICB0CTL0.IICB0SLWT bit = 1b and continuous transmission, at the falling edge of the 9th clock during data transmission. Clear condition that prioritizes set condition (in continuous transfer mode (transmission)). ● When reading the IICB0DAT register when there is no unstored received data in the IICB0DAT register in the shift register.

Table 38.5-5 IICm_IICB0STR0 Register Contents (3/6)

Bit Position	Bit Name	Description
12	IICB0SSWT	Wait status flag 0b: No wait state 1b: Wait state <Set conditions> • When single transfer mode – Common to master and slave When the falling edge of the 8th clock is detected when the IICB0CTL0.IICB0SLWT bit = 0b during data transfer. When the falling edge of the 9th clock is detected when the IICB0CTL0.IICB0SLWT bit = 1b during data transfer. – Master IICB0TRG.IICB0STT bit = Master (IICB0STR0.IICB0SSMS bit = 1b) after 1b write, no write access to IICB0DAT register, and first falling edge of SCLm is detected. When the falling edge of the 9th clock is detected during address transfer. – Slave When the falling edge of the 9th clock is detected during an address match. • When continuous transfer mode – Common to master slaves during data transfer • During data transmission, when data to be transmitted next is not written. The IICB0CTL0.IICB0SLWT bit = 0b, when the IICB0STR0.IICB0SSDR bit = 0b at the falling edge of the 8th clock during data transmission. The IICB0CTL0.IICB0SLWT bit = 1b, when the IICB0STR0.IICB0SSDR bit = 0b at the falling edge of the 9th clock during data transmission. • When data is being received and the previous received data has not been read. The IICB0CTL0.IICB0SLWT bit = 0b, when the IICB0CTL0.IICB0SSDR bit = 1b at the falling edge of the 8th clock during data reception. The IICB0CTL0.IICB0SLWT bit = 1b, when the IICB0STR0.IICB0SSDR bit = 1b at the falling edge of the 9th clock during data reception. When NACK is detected (However, if IICB0TRG.IICB0STT bit = 1b or IICB0TRG.IICB0SPT bit = 1b was not written during master operation). – Master during address transfer period • The IICB0TRG.IICB0STT bit = Master (IICB0STR0.IICB0SSMS bit = 1b) after 1b write, no write access to IICB0DAT register, and the first falling edge of SCLm is detected. • When NACK is detected (However, the IICB0TRG.IICB0STT bit = 1b or the IICB0TRG.IICB0SPT bit = 1b if there was no write). – Slave during address transfer period • When the falling edge of the 9th clock while the IICB0STR0.IICB0SSTR bit = 0b is detected during an address match. • When NACK is detected. <Clear conditions> • Clear condition that takes precedence over the set condition – When writing IICB0TRG.IICB0LRET bit = 1b. – When writing IICB0TRG.IICB0STT bit = 1b in master operation and continuous transfer mode. – When writing IICB0TRG.IICB0SPT bit = 1b in master operation and continuous transfer mode. – IICB0DAT register write when transmitting in continuous transfer mode. – When waiting for the 8th clock, when reading IICB0DAT register when receiving in continuous transfer mode. – When waiting for the 9th clock, when reading the IICB0DAT register when receiving and acknowledging (ACK) in continuous transfer mode.

Table 38.5-5 IICm_IICB0STR0 Register Contents (4/6)

Bit Position	Bit Name	Description
12	*<Continue to previous page>*	• Clear condition that set condition has priority – When writing IICB0TRG.IICB0WRET bit = 1b. – When writing IICB0TRG.IICB0STT bit = 1b in master transfer and single transfer mode. – When writing IICB0TRG.IICB0SPT bit = 1b in master transfer and single transfer mode. – IICB0DAT register write when receiving in single transfer mode. *Note*: When canceling wait period by writing the IICB0TRG.IICB0WRET bit = 1b during the 9th clock wait period, the IICB0STR0.IICB0SSTR bit is cleared (0) and the bus is released (Set both SCLm and SDAm to high impedance state).
11	IICB0SSEX	Extended code reception detection flag 0b: Not received 1b: Received <Set condition> • When the falling edge of the 8th clock is detected during address transfer when the upper 4 bits of the received address data are 0000b or 1111b. <Clear conditions> • When IICB0TRG.IICB0LRET bit = 1b is written. • When a stop condition is detected. • When a start condition is detected. *Note*: Processing after an interrupt when the extension codes match depends on the data following the extension code, and therefore depends on the software processing.
10	IICB0SSCO	Detection flag for the address that matches the IICB0SVA register 0b: Not detected 1b: Detection <Set condition> • When the falling edge of the 8th clock is detected during the transfer of the address whose received address matches the IICB0SVA register. <Clear conditions> • When IICB0TRG.IICB0LRET bit = 1b is written. • When a stop condition is detected. • When a start condition is detected.
9	IICB0SSTR	Data transmission status detection flag to the serial data bus 0b: Not sending 1b: Sending <Set conditions> • Master – When a start condition is detected after writing IICB0TRG.IICB0STT bit = 1b. • Slave – When the falling edge of the 8th clock after receiving 1 in the R / W bit of the address transfer with the address match is detected. <Clear conditions> • Common to Master / Slave – When writing IICB0TRG.IICB0WRET bit = 1b. – When stop condition is detected. – IICB0TRG.IICB0WRET bit = 1b write during wait period of 9th clock. • Master – When the falling edge of the 8th clock after receiving 1 in the mode bit indicating R / W is detected. – When arbitration loss is detected. • Slave – When detecting a start (restart) condition.

Table 38.5-5 IICm_IICB0STR0 Register Contents (5/6)

Bit Position	Bit Name	Description
8	IICB0SSAC	Acknowledge (ACK) detection flag 0b: Acknowledge not detected 1b: Acknowledge is detected <Set condition> • When the falling edge of SCL is detected when low level is received in ACK bit while participating in communication. <Clear conditions> • When writing IICB0TRG.IICB0LRET bit = 1b. • When the rising edge of SCLm is detected. *Note*: The value of the IICB0STR0.IICB0SSAC bit changes regardless of whether an interrupt has occurred.
7	IICB0SSRS	Communication reservation status flag 0b: Not communication reservation state 1b: Communication reservation status <Set condition> • When the communication reservation function is enabled (IICB0CTL1.IICB0SLRS bit = 0b) and the IICB0TRG.IICB0STT bit is set to 1b during bus communication not operating as a master. <Clear conditions> • When writing IICB0TRG.IICB0LRET bit = 1b. • IICB0STR0.IICB0SSMS bit = 1b.
6	IICB0SSBS	Bus status flag 0b: Bus released state or communication initial state when IICB0CTL1.IICB0SLSE bit = 1b 1b: Bus communication state or communication initial state when IICB0CTL1.IICB0SLSE bit = 0b <Set conditions> • When a start condition is detected. • When writing IICB0CTL0.IICB0IICE bit = 1b with IICB0CTL1.IICB0SLSE bit = 0b. <Clear condition> • When a stop condition is detected. *Note*: The IICB0STR0.IICB0SSBS bit operates regardless of participation or non-participation in communication.
5	IICB0SSST	Start condition detection flag 0b: Not detected 1b: Detected <Set condition> • When a start condition is detected. <Clear conditions> • When writing IICB0TRG.IICB0LRET bit = 1b. • When a stop condition is detected. • When the rising edge of SCLm is detected after address transfer is completed. *Note*: The IICB0STR0.IICB0SSST bit operates regardless of participation or non-participation in communication.

Table 38.5-5 IICm_IICB0STR0 Register Contents (6/6)

Bit Position	Bit Name	Description
4	IICB0SSSP	Stop condition detection flag 0b: Not detected 1b: Detected <Set condition> • When a stop condition is detected. <Clear condition> • When the first falling edge of SCLm is detected after the start condition is detected. *Note*: The IICB0STR0.IICB0SSSP bit operates regardless of participation or non-participation in communication.
3, 2	—	Reserved. These bits are read as 0b.
1	IICB0STCF	IICB0TRG.IICB0STT bit clear flag 0b: Do not clear 1b: When a start condition cannot be issued, IICB0TRG.IICB0STT bit is cleared <Set condition> • When the IICB0TRG.IICB0STT bit is set to 1b during bus communication not operating as a master in the communication reservation function disabled state (IICB0CTL1.IICB0SLRS bit = 1b). <Clear condition> • IICB0STRC.IICB0CLSF bit = 1b write. *Note*: Even if the bus is released in the external bus state, this unit does not recognize that the bus is released (IICB0STR0.IICB0SSBS bit = 1b). If the communication reservation function is disabled, IICB0TRG.IICB0STT bit = IICB0STR0 The .IICB0STCF bit is set 1b.
0	IICB0ALDF	Arbitration loss detection flag 0b : Do not detect 1b: Loss of arbitration <Set condition> • When arbitration loss is detected. <Clearing condition> • IICB0STRC.IICB0CLAF bit = 1 write. If the set condition and clear condition are detected at the same time, the set condition has priority. When arbitration loss is detected, the IICB0STR0.IICB0SSMS and IICB0STR0.IICB0SSTR bits are cleared to 0b (SCLm and SDAm are set to the high impedance state and the bus is released). *Note*: If the IICB0STR0.IICB0ALDF bit is set 1b due to arbitration loss, the IICBTIA interrupt request signal or IICBTIS interrupt request signal is generated. When IICB0STR0.IICB0ALDF bit = 1 is confirmed by the interrupt request signal, clear IICB0STR0.IICB0ALDF bit with IICB0STRC.IICB0CLAF bit. If the IICB0STR0.IICB0ALDF bit is not cleared and 1b remains in the IICB0STR0.IICB0ALDF bit, the IICBTIS interrupt request signal is generated when the interrupt timing occurs even during unrelated communication.

38.5.6 IICB Status Register 1 (IICm_IICB0STR1) (m = 0 to 3)

The IICB0STR1 register indicates the serial bus status.

Note: Even in the loop back mode (IICB0CTL1.IICB0MDLB bit = 1b), the external serial clock signal (SCLm) and serial transmission/reception data signal (SDAm) are read.

Access Size: 32 bits

Address(es): <IIC0_S0_base> + 0014h
<IIC1_S0_base> + 0014h
<IIC2_S0_base> + 0014h
<IIC3_S0_base> + 0014h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IICB0SSCL	IICB0SSDA
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 38.5-6 IICm_IICB0STR1 Register Contents

Bit Position	Bit Name	Description
32 to 2	—	Reserved. These bits are read as 0b.
1	IICB0SSCL	Indicates the pin level status of the SCLm pin (input). 0b: SCLm pin (input) is at the low level. 1b: SCLm pin (input) is at the high level.
0	IICB0SSDA	Indicates the pin level status of the SDAm pin (input). 0b: SDAm pin (input) is at the low level. 1b: SDAm pin (input) is at the high level.

38.5.7 IICB Status Clear Register (IICm_IICB0STRC) (m = 0 to 3)

The IICB0STRC register clears the IICB0STCF bit and IICB0ALDF bit of the IICB0STR0 register.

Access Size: 32 bits

Address(es): <IIC0_S0_base> + 0018h
<IIC1_S0_base> + 0018h
<IIC2_S0_base> + 0018h
<IIC3_S0_base> + 0018h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IICB0CLSF	IICB0CLAF
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 38.5-7 IICm_IICB0STRC Register Contents

Bit Position	Bit Name	Description
31 to 2	—	Reserved. These bits are read as 0b. The write value should always be 0b.
1	IICB0CLSF	Clear bit of IICB0STR0.IICB0STCF bit 0b: No clear 1b: Clear *Note*: IICB0STRC.IICB0CLSF bit is set to 0b when read after data is set.
0	IICB0CLAF	Clear bit of IICB0STR0.IICB0ALDF bit 0b: No clear 1b: Clear *Note*: IICB0STRC.IICB0CLAF bit is set to 0b when read after data is set. *Note*: If writing 1b to the IICB0STRC.IICB0CLAF bit and the set condition of the IICB0STR0.IICB0ALDF bit occur simultaneously, the set condition of the IICB0STR0.IICB0ALDF bit is valid.

38.5.8 IICB Control Register 1 (IICm_IICB0CTL1) (m = 0 to 3)

The IICB0CTL1 register controls the operation of this unit.

Note: Writing to the IICB0CTL1 register when the IICB0CTL0.IICB0IICE bit = 1b is prohibited.

Access Size: 32 bits

Address(es): <IIC0_S0_base> + 0020h
<IIC1_S0_base> + 0020h
<IIC2_S0_base> + 0020h
<IIC3_S0_base> + 0020h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IICB0MDSC	IICB0LGDF[2:0]			IICB0MDLB	—	IICB0SLSE	IICB0SLRS
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 38.5-8 IICm_IICB0CTL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7	IICB0MDSC	Specify the operation mode of this unit. 0b: Standard mode (SCL clock frequency: Max. 100 kHz) 1b: High-speed mode (SCL clock frequency: Max. 400 kHz)
6 to 4	IICB0LGDF[2:0]	Specify the digital filter sampling period. The digital filter can be used only in the high-speed mode. 000b: Digital filter not used SCLm and SDAm that do not pass through the digital filter are used inside this unit. The digital filter circuit stops operating. Others: Using digital filter SCLm and SDAm that have passed through the digital filter inside this unit are used. When using a digital filter, set the IICB0CTL1.IICB0LGDF[2:0] bits as follow. Table 38.5-8-1

IICB0CTL1.IICB0LGDF[2:0] Bit	Frequency
001b	Minimum frequency ≤ PCLK ≤ 20 MHz
010b	20 MHz < PCLK ≤ 40 MHz
011b	40 MHz < PCLK ≤ 60 MHz
100b	60 MHz < PCLK ≤ 80 MHz
101b	80 MHz < PCLK ≤ 100 MHz
110b, 111b	Setting prohibited

Table 38.5-8 IICm_IICB0CTL1 Register Contents (2/2)

Bit Position	Bit Name	Description
		The following is a list of minimum frequencies for each setting (See **Table 38.5-8-2)**. Table 38.5-8-2 Operation Mode (IICB0CTL1.IICB0MDSC bit) / Filter Not Used (IICB0CTL1.IICB0LGDF[2: 0] bits = 000) / Use Filter (IICB0CTL1.IICB0LGDF[2: 0] bits ≠ 000) Standard mode 0b / 1.0 MHz / Do not use High speed mode 1b / 3.5 MHz / 4.0 MHz
3	IICB0MDLB	Specifies the loop back mode. 0b: Do not loop back 1b: Loop back By setting the IICB0CTL1.IICB0MDLB bit to 1b, the output serial clock signal (SCLm) and serial transmission/reception data signal (SDAm) are loopback, use as input serial clock signal (SCLm) and serial transmit/receive data signal (SDAm). The serial clock signal and serial transmission/reception data signal immediately before output are used as the serial clock signal and serial transmission/reception data signal to be returned. When the IICB0CTL1.IICB0MDLB bit = 1b, SCLm and SDAm are all at the high level.
2	—	Reserved. This bit is read as 0b. The write value should always be 0b.
1	IICB0SLSE	Specifies enabling or disabling of start condition issuance in the initial communication state. 0b: Start condition issuance disabled in the initial communication state 1b: Start condition issuance enabled in the initial communication state By setting the IICB0CTL1.IICB0SLSE bit to 1b, a start condition can be issued by setting the IICB0TRG.IICB0STT bit = 1b in the initial communication state (After the IICB0CTL0.IICB0IICE bit = 1b is set until the stop condition is detected). The IICB0CTL1.IICB0SLSE bit is automatically cleared even if 0b is not written when a start condition is detected. *Note*: Set the IICB0CTL1.IICB0SLSE bit to 0b when participating in other communications unpunctually. If the IICB0TRG.IICB0STT bit is set to 1b after setting the IICB0CTL1.IICB0SLSE bit to 1b while other communications is being performed, other communication may be destroyed.
0	IICB0SLRS	Specify enabling or disabling of the communication reservation function. 0b: Communication reservation function enabled If the IICB0CTL1.IICB0SLRS bit is 0b (clear) and this unit is not operating as a master and the bus is in use, setting the IICB0TRG.IICB0STT bit to 1b sets the communication reservation status. By checking the IICB0STR0.IICB0SSRS bit, it can be confirmed whether it is in the communication reserved state. 1b: Communication reservation function disabled If this unit is not participating in communication as a master and the IICB0TRG.IICB0STT bit is set to 1b while the bus is in use, the IICB0STR0.IICB0STCF bit = 1b and communication is not reserved.

38.5.9 IICB Low-level Width Setting Register (IICm_IICB0WL) (m = 0 to 3)

The IICB0WL register sets the low level width of the serial clock signal (SCLm).

Note: Writing to the IICB0WL register is prohibited when the IICB0CTL0.IICB0IICE bit = 1b.

Access Size: 32 bits

Address(es): <IIC0_S0_base> + 0024h
<IIC1_S0_base> + 0024h
<IIC2_S0_base> + 0024h
<IIC3_S0_base> + 0024h

Initial Value: 0000_03FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IICB0WL[9:0]									
Initial Value	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 38.5-9 IICm_IICB0WL Register Contents

Bit Position	Bit Name	Description
31 to 10	—	Reserved These bits are read as 0b. The write value should always be 0b.
9 to 0	IICB0WL[9:0]	Specify the t_{LOW} (SCLm clock low level width) section of the IIC bus standard. The value of the IICB0WL register is used to determine the serial output timing for other IIC bus standards.

38.5.10 IICB High-level Width Setting Register (IICm_IICB0WH) (m = 0 to 3)

The IICB0WH register sets the high level width of the serial clock signal (SCLm).

Note: Writing to the IICB0WH register is prohibited when the IICB0CTL0.IICB0IICE bit = 1b.

Access Size: 32 bits

Address(es): <IIC0_S0_base> + 0028h
<IIC1_S0_base> + 0028h
<IIC2_S0_base> + 0028h
<IIC3_S0_base> + 0028h

Initial Value: 0000_03FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IICB0WH[9:0]									
Initial Value	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 38.5-10 IICm_IICB0WH Register Contents

Bit Position	Bit Name	Description
31 to 10	—	Reserved. These bits are read as 0b. The write value should always be 0b.
9 to 0	IICB0WH[9:0]	Specify the HIGH (high level width of SCLm clock) interval of IIC bus standard. The value of the IICB0WH register is used to determine the serial output timing for other IIC bus standards.

38.5.10.1 Setting the Transfer Clock by the IICB0WL and IIVB0WH Registers

The values of the IICB0WL and IICB0WH registers are used to generate various timings in the IIC bus specifications.

(1) Setting the transfer clock on the master side

$$\text{Transfer clock (Hz)} = \frac{\text{PCLK}}{\text{IICB0WL} + \text{IICB0WH}} + \text{PCLK}\,(t_R + t_F)$$

At this time, the appropriate settings of IICB0WL and IICB0WH are as follows.
(All decimal points are rounded up.)

- In high-speed mode

  IICB0WL = (0.52/Transfer clock) × PCLK
  IICB0WH = (0.48/Transfer clock − t_R − t_F) × PCLK

- In standard mode

  IICB0WL = (0.47/Transfer clock) × PCLK
  IICB0WH = (0.53/Transfer clock − t_R − t_F) × PCLK

Note: Make sure that the data hold time does not exceed 0.9 [µs] in high-speed mode and 3.45 [µs] in standard mode.

NOTES

1. The data hold time is as follows depending on the setting of IICWL: Data hold time = IICB0WL[9:2]/PCLK.
2. When performing communications at 400 kbit/s in high-speed mode with PCLK = 100 MHz and tR/tF as 0, the settings are as follows.
   IICB0WL = 82h
   IICB0WH = 78h

(2) Setting IICB0WL and IICB0WH on the slave side

(All decimal points are rounded up.)

- In high-speed mode

  IICB0WL = 1.3 μs × PCLK IICB0WH = (1.2 μs − t_R − t_F) × PCLK

- In standard mode

  IICB0WL = 4.7 μs × PCLK IICB0WH = (5.3 μs − t_R − t_F) × PCLK

NOTES

— IICB0WL: IICB low-level width setting register
— IICB0WH: IICB high-level width setting register
— t_F: SDAn and SCLn signal falling time
— t_R: SDAn and SCLn signal rising time
— PCLK: Clock frequency supplied to this macro
— f_{CLK}: SCL clock frequency

38.5.11 IICB Emulation Read Register (IICm_IICB0EDAT) (m = 0 to 3)

The IICB0EDAT register is used to read the value of the IICB0DAT register.

This register is also initialized by changing the IICB0CTL0.IICB0IICE bit from 1b to 0b and the IICB0CTL0.IICB0IICE bit from 0b to 1b.

Access Size: 32 bits

Address(es): <IIC0_S0_base> + 002Ch
<IIC1_S0_base> + 002Ch
<IIC2_S0_base> + 002Ch
<IIC3_S0_base> + 002Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IICB0EDAT[7:0]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 38.5-11 IICm_IICB0EDAT Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	IICB0EDAT[7:0]	Indicates the value of IICB0DAT.IICB0DAT[7:0]. Reading the IICB0EDAT register does not affect the receive operation.

38.5.12 IICB Shift Register (IICm_IICB0DATS) (m = 0 to 3)

The IICB0DATS register is used to read the value of the shift register that stores transfer data.

Access Size: 32 bits

Address(es): <IIC0_S0_base> + 0030h
<IIC1_S0_base> + 0030h
<IIC2_S0_base> + 0030h
<IIC3_S0_base> + 0030h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IICB0DATS [7:0]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 38.5-12 IICm_IICB0DATS Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	IICB0DATS [7:0]	Indicates the value of the shift register that stores the transfer data. *Note*: The shift register is a register that holds the data received from SDAI during reception and shifts the data transferred from the IICB0DAT register during transmission.

38.6 Operation

This IIC bus is used for master and slave operations through the IIC bus.

This IIC bus is a serial bus for multiple masters. It has a clocked serial I/C format with the function for bus configuration so that communications with multiple devices can proceed with the two signal lines, the serial clock (SCL) and serial data bus (SDA). Therefore, when configuring the serial bus with multiple microcontrollers and peripheral ICs, reducing the number of ports to be used and wirings on the board is possible.

The master is able to output a start condition, slave address, data, and stop condition to a slave.

The slave automatically detects these received data by hardware. This function makes it possible to simplify the IIC bus control section in the application program.

In the IIC bus, the serial clock pin (SCL) and serial data bus pin (SDA) are open-drain outputs, so the serial clock line and serial data bus line require pull-up resistors.

The prefix (IICm_) of the register names is omitted in this and subsequent sections.

38.6.1 IIC Bus Functions

For the functions of the IIC bus, refer to THE I2C-BUS SPECIFICATION VERSION 2.1 issued by Philips Semiconductors in January 2000.

The following describes the functions of the IIC Bus.

38.6.1.1 Communications Mode

Standard mode (transfer speed: up to 100 kbits/s) and fast mode (transfer speed: up to 400 kbits/s) are supported. High-speed mode (transfer speed: up to 3400 kbits/s) is not supported.

38.6.1.2 Automatic Detection of Serial Data

A start condition, slave address, data, and stop condition on the serial data bus are automatically detected.

38.6.1.3 Chip Selection by Address

By transmitting the slave address or extension code in master operation, the specific slave address connected to the IIC bus can be selected for communications.

38.6.1.4 Wakeup Function

In slave operation, an interrupt only occurs when the received address matches the value of the slave address register (SVA0) and the extension code is received. Accordingly, the CPU other than the selected slave on the IIC bus can operate regardless of serial communications.

38.6.1.5 Acknowlege (ACK) Control

In master/slave operation, an acknowledge signal to check the normal execution of serial communications can be controlled.

38.6.1.6 Wait (WAIT) Control

A wait signal to notify the wait state can be controlled.

38.6.1.7 Arbitration Control

When multiple masters generate a start condition at the same time, the IIC bus is able to compare the level on the serial data bus (SDA) pin after the adjustment of synchronization with the serial clock (SCL) to finally select the master.

38.6.1.8 Continuous Transfer

When ACK for the transmitted data is received at the low level, the data can be transmitted continuously.

In addition, ACK for the received data is transmitted at the low level, the data can be received continuously.

38.6.2 Definition of the IIC Bus

The following describes the serial data communications format of the IIC bus and the meaning of the signals to be used.

The figure below shows the timing of transfer of a “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition”, which are generated on the serial data bus of the IIC bus.

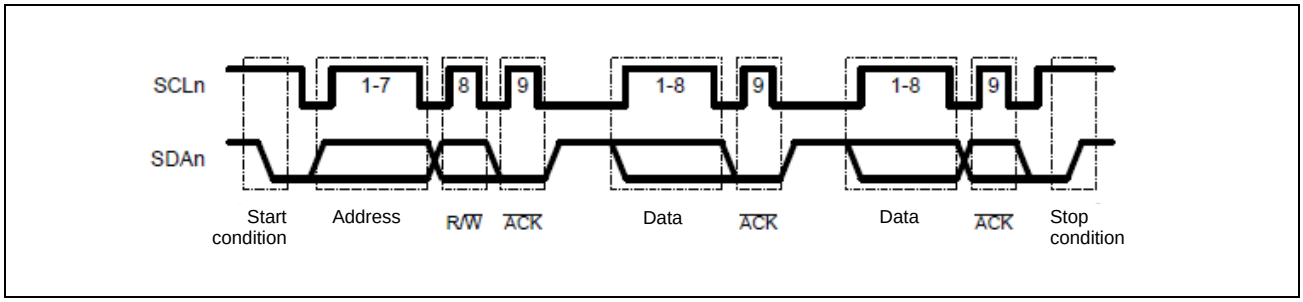


Figure 38.6-1 IIC Serial Data Transfer Timing

The start condition, slave address, and stop condition are generated by the master. An acknowledge ($\overline{ACK}$) can be generated by either the master or slave (it is usually generated by the receiver of 8-bit data).

The serial clock (SCLm) is continuously output by the master. The slave is able to extend the low-level period of the SCLm pin and insert a wait.

38.6.2.1 Start Condition

A start condition is met when the SDAm pin changes from the high to the low level while the SCLm pin is at the high level. A start condition is generated when the master starts serial transfer to the slave. When the IIC is used as a slave, the start condition can be detected.

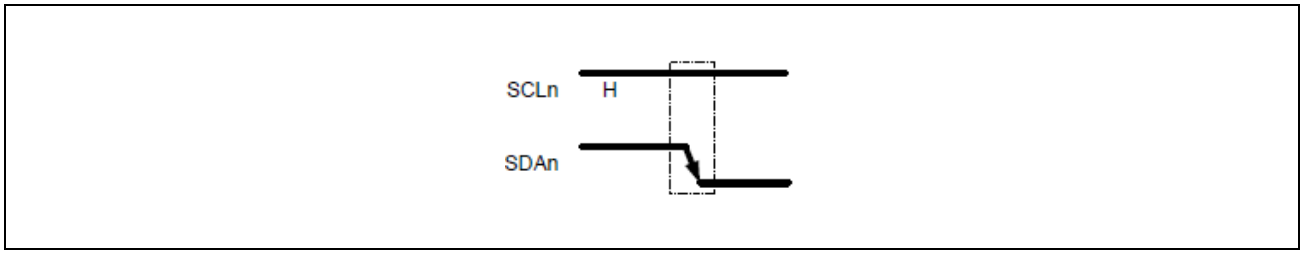


Figure 38.6-2 Start Condition

38.6.2.2 Address

7-bit data following the start condition are defined as an address.

An address is a 7-bit data segment that is output in order for the master to select the specific slave from among multiple slaves that are connected to the bus lines. Accordingly, all slaves on the bus lines must have different addresses.

A slave checks whether the 7-bit data matches its own address. At this time, matching with its own address means that this slave is selected, and after that it communicates with the master until the master generates a start condition or stop condition.

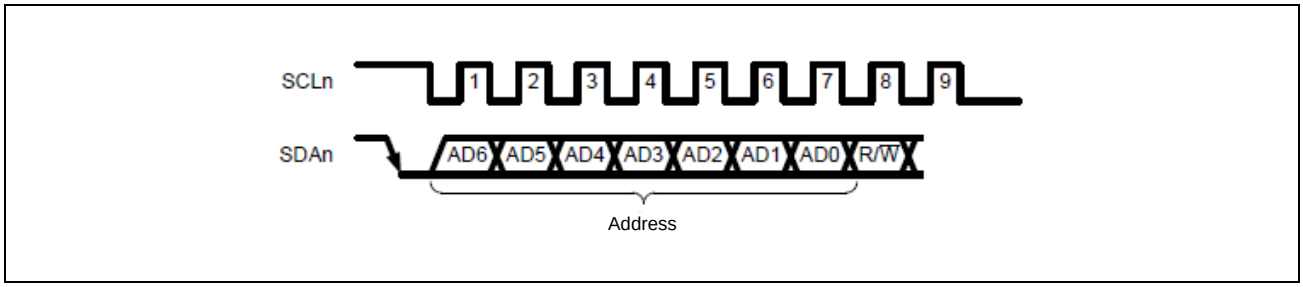


Figure 38.6-3 Address

38.6.2.3 Extention Code

When the higher-order four bits of the address are 0000 or 1111, these bits are called extension code. **Table 38.6-1** lists the definitions of bits as extension code.

Table 38.6-1 Extension Code Bit Definitions

Slave Address	R/W Bit	Description
0000 000b	0b	General call address
0000 000b	1b	Start byte
0000 001b	x	CBUS address
0000 010b	x	Address reserved for a different bus format
0000 011b	x	Reserved for future use
0000 1xxb	x	HS mode master code*1
1111 0xxb	x	10-bit slave address specification
1111 1xxb	x	Reserved for future use

Note 1. HS mode cannot be used in this unit.

Note 2. x : Don't care

38.6.2.4 Transfer Direction Specification

The master transmits 1-bit data to specify the transfer direction following the 7 address bits. The value of this transfer direction specification bit being 0b indicates that the master transmits data to the slave. The value 1b indicates that the master receives data from the slave.

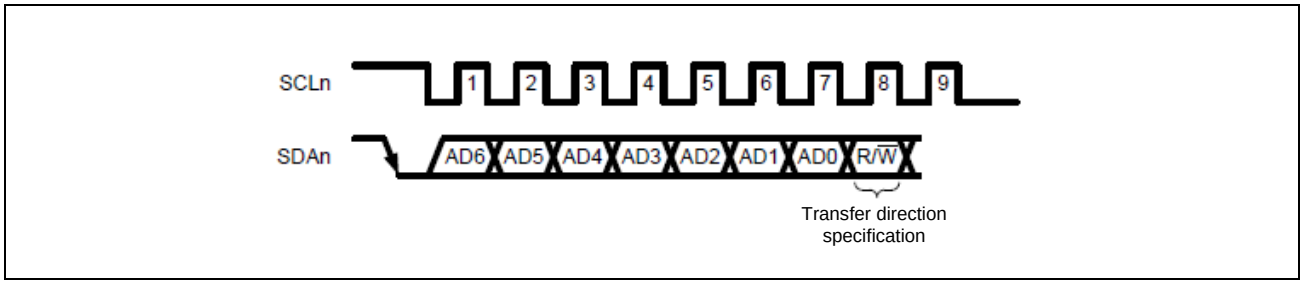


Figure 38.6-4 Transfer Direction Specification

38.6.2.5 Acknowledge

1-bit data following the transfer direction bit (R/$\overline{W}$) for address transfer and 1-bit data following 8-bit data are defined as acknowledge.

The acknowledge allows checking the state of serial data in the transmitter and receiver. The acknowledge being returned at the low level is called ($\overline{ACK}$), which indicates normal end. The acknowledge being returned at the high level is called (NACK), which indicates abnormal end.

The receiver returns an acknowledge every time it receives 8-bit data.

The transmitter usually receives an acknowledge following the transmission of 8-bit data. When ($\overline{ACK}$) is returned from the receiver, the transmitter recognizes that reception has proceeded correctly and continues processing.

When the master receives the last of data in reception, it does not return an acknowledge but generates a stop condition.

When the slave returns (NACK) in reception, the master generates a stop condition or restart condition to stop transmission. If (NACK) is returned, the following causes can be considered:

1) Reception has not proceeded correctly.
2) Reception of the last of data has ended.
3) The receiver specified by the address is not present.

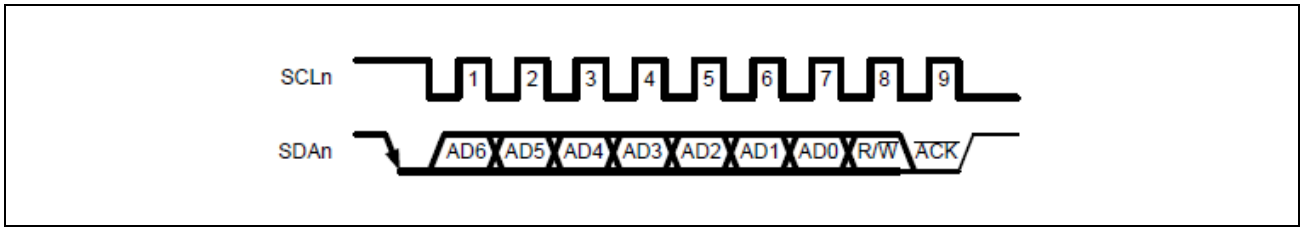


Figure 38.6-5 Acknowledge ($\overline{ACK}$)

38.6.2.6 Data

Bits, except for 9 bits following the start condition (address (7 bits), R/$\overline{W}$ (1 bit), and acknowledge (1 bit)) and the acknowledge, are defined as data.

If a 10-bit address is specified with the use of the extension code, 8-bit data following address transfer are used as the address (second address).

38.6.2.7 Stop Condition

A stop condition is met when the SDAm pin changes from the low to the high level while the SCLm pin is at the high level.

A stop condition is generated when the master has completed serial transfer to the slave.

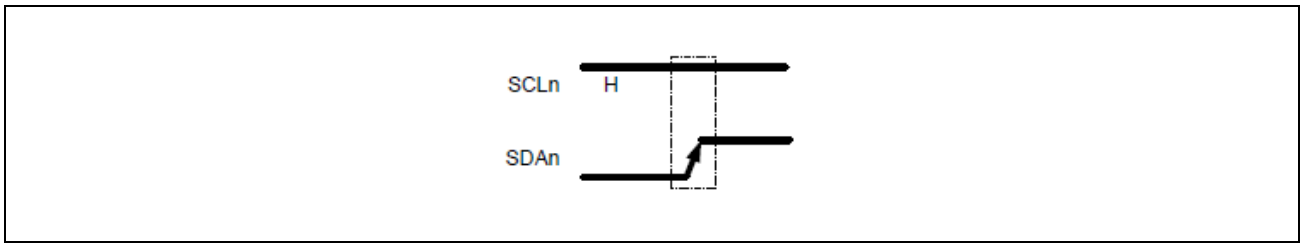


Figure 38.6-6 Stop Condition

38.6.2.8 Wait

A wait notifies the other party that the master or slave is preparing to transmit or receive data (i.e., in the wait state).

By driving the SCLm pin to the low level, the other party is notified of the wait state. When both the master and slave are released from the wait state, a next data transfer can be started.

(a) When the master enters the wait state in the 9th clock cycle and the slave enters the wait state in the 8th clock cycle (master: for transmission, slave: for reception)

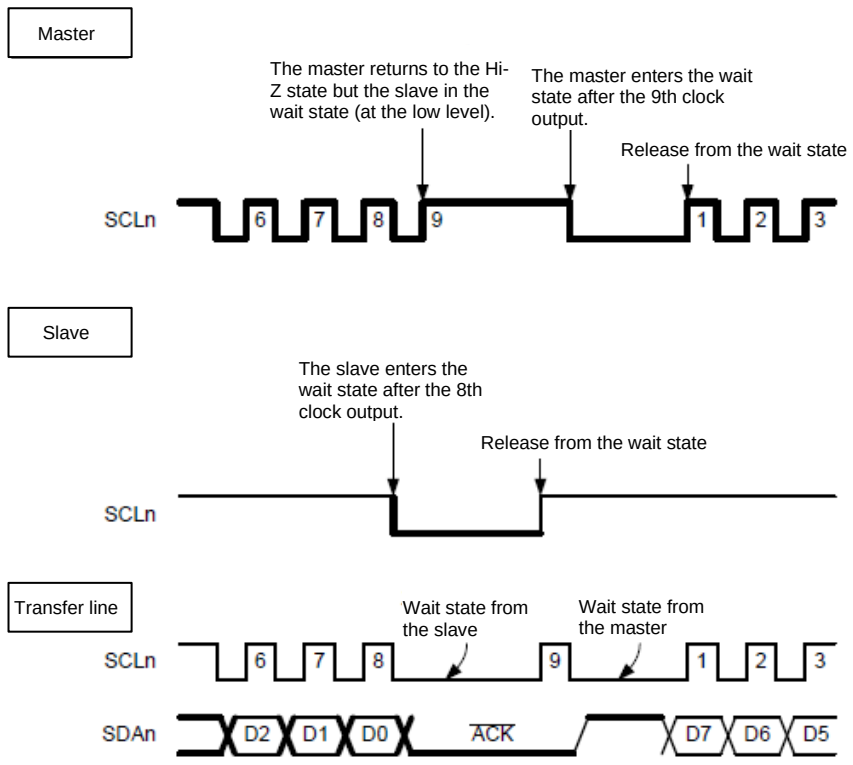


Figure 38.6-7 Wait (1/2)

(b) When both the master and slave enter the wait state in the 9th clock cycle (master: for transmission, slave: for reception)

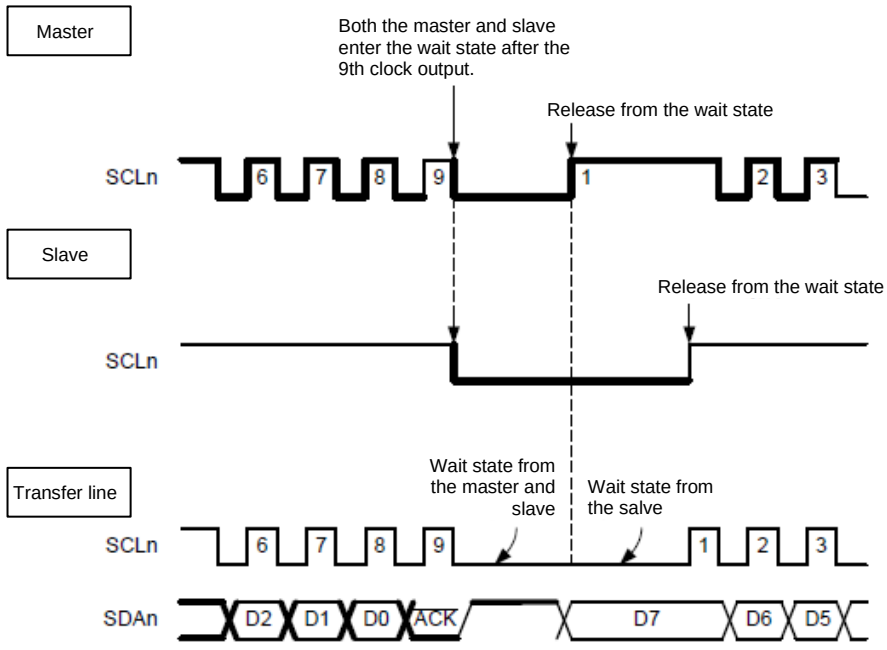


Figure 38.6-7 Wait (2/2)

38.6.2.9 Arbitration

When multiple masters generate a start condition at the same time, master communications proceed while adjusting the clock cycles until the data differ from one another. The following describes an example where two masters generate a start condition at the same time and arbitration occurs.

Here, suppose that a master that outputs the high level to the SDAm line (master 1) and a master that outputs the low level to the SDAm line (master 2) are present when the SCLm line is at the low level.

In this case, communications by the mater that has output the low level to the SDAm line are given priority and communications are not permitted for the master that has output the high level to the SDAm line.

Such procedure is called arbitration and the state in which communications are not permitted is called arbitration loss.

The master that has lost in arbitration releases the bus by placing both the SCLm and SDAm lines in the high-impedance state at the time it lost in arbitration.

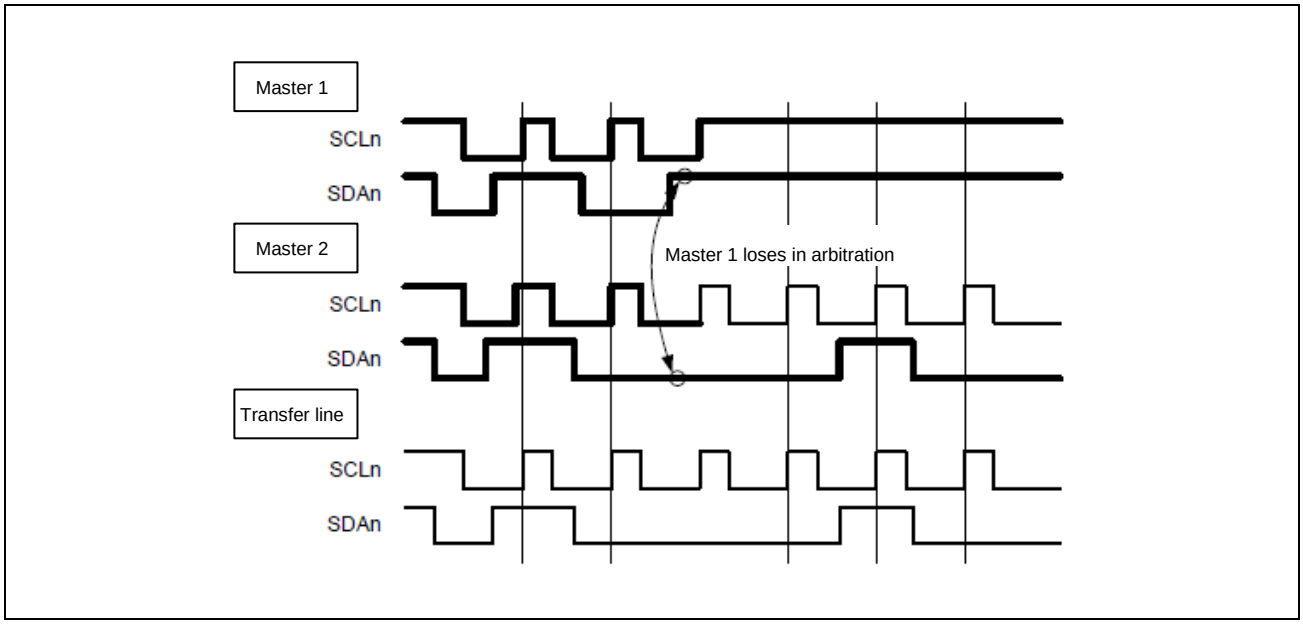


Figure 38.6-8 Example Timing of Arbitration

38.6.3 Operations for Communications

This unit supports single transfer mode and continuous transfer mode as the transfer mode.

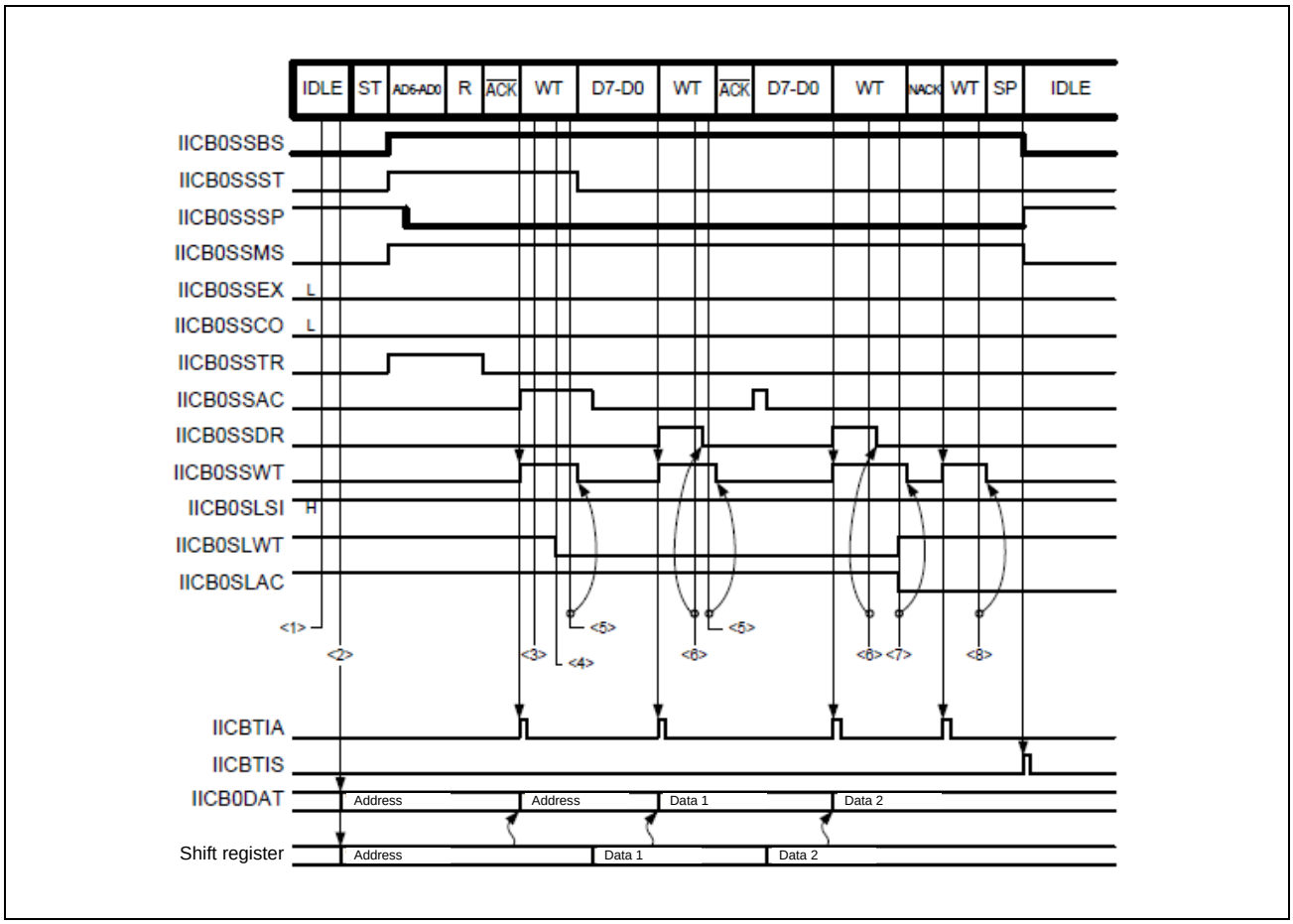
The transfer mode when the address matches between the master and slave is selected by the IICB0CTL0.IICB0MDTX0 bit, and the transfer mode when the extension code is detected by the slave is selected by the IICB0CTL0.IICB0MDTX1 bit.

38.6.3.1 Single Transfer Mode

In single transfer mode, a data transmission/reception interrupt request signal (IICBTIA) is generated to place the IIC in the wait state with the timing set in the IICB0CTL0.IICB0SLWT bit and data to be transferred are processed during this wait period.

Operations for each processing are described below.

(1) Example of Communications in Single Transfer Mode (Master Reception)



<1> Start condition output

Set the IICB0TRG.IICB0STT bit to 1.

<2> Address and transfer direction specification output

Set the combination of the slave's address and transfer direction as 8 bits in the IICB0DAT register.

<3> Checking the acknowledge result

Check the result by reading the IICB0STR0.IICB0SSAC bit in response to the IICBTIA interrupt.

<4> Wait timing setting

In data reception, clear the IICB0CTL0.IICB0SLWT bit to 0b to place the IIC in the wait state on the rising edge of the 8th clock cycle.

<5> Data reception

Set the IICB0TRG.IICB0WRET bit to 1b during the wait period to release the wait state and start reception.

<6> Loading received data

Read the received data from the IICB0DAT register in response to the IICBTIA interrupt.

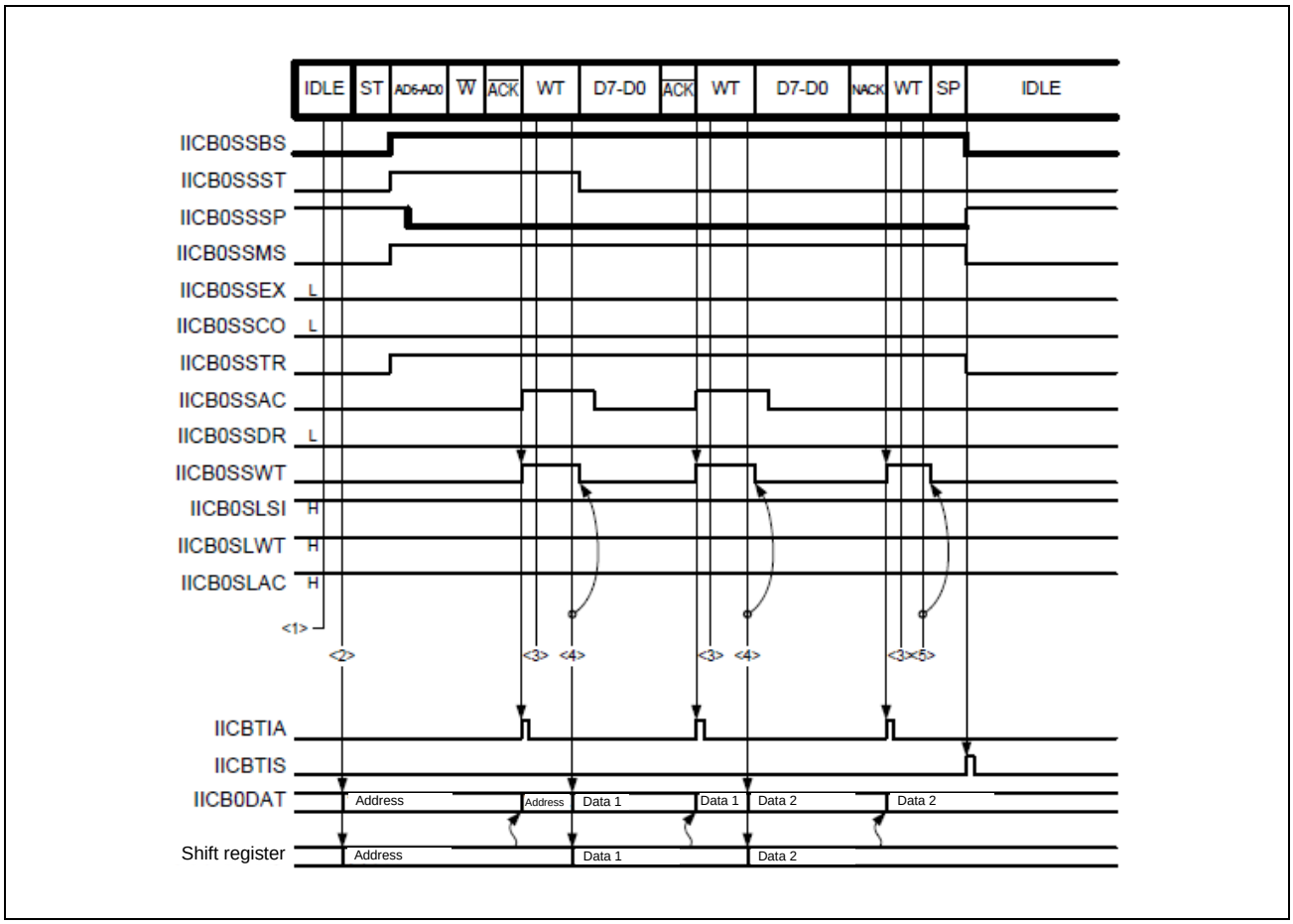
<7> Data reception completion processing

- Set the IICB0CTL0.IICB0SLWT bit to 1 and the IICB0CTL0.IICB0SLAC bit to 0b during the wait period.
- After that, set the IICB0TRG.IICB0WRET bit to 1b to release the wait state. An acknowledge is not generated and the transmitter is notified of the end of the data.

<8> Stop condition output

Set the IICB0TRG.IICB0SPT bit to 1b.

(2) Example of Communications in Single Transfer Mode (Master Transmission)



<1> Start condition output

Set the IICB0TRG.IICB0STT bit to 1b.

<2> Address and transfer direction specification output

Set the combination of the slave's address and transfer direction as 8 bits in the IICB0DAT register.

<3> Checking the acknowledge result

Check the result by reading the IICB0STR0.IICB0SSAC bit in response to the IICBTIA interrupt.

<4> Data transmission

Set the data for transmission in the IICB0DAT register during the wait period to release the wait state and start transmission.

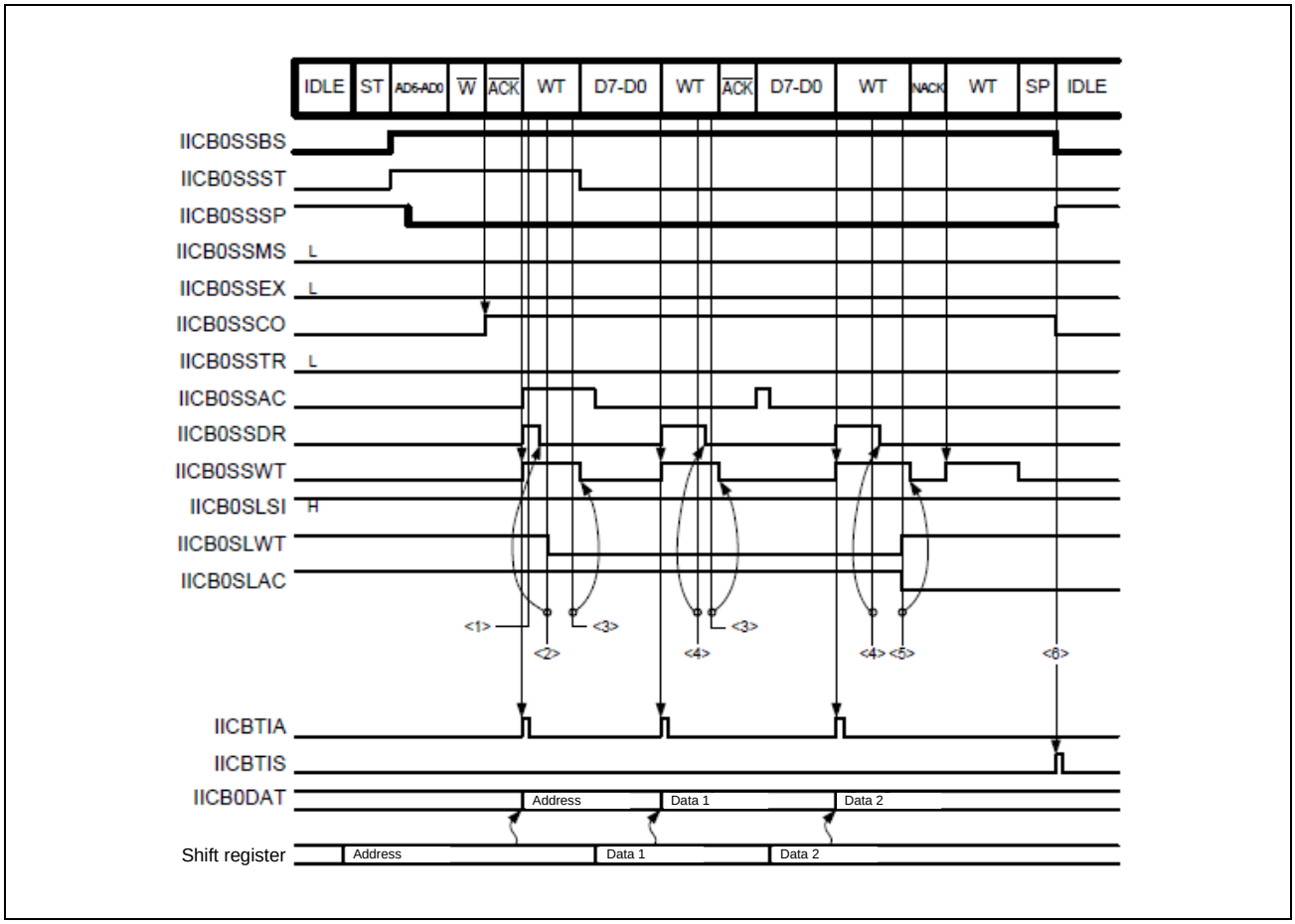
<5> Stop condition output

Set the IICB0TRG.IICB0SPT bit to 1b.

NOTE

In data transmission, set the IICB0CTL0.IICB0SLWT bit to 1 to place the IIC in the wait state on the falling edge of the 9th clock cycle.

(3) Example of Communications in Single Transfer Mode (Slave Reception)



<1> Checking the operating mode in slave operation

- Check the operating mode in response to the IICBTIA interrupt.
- Check the address transfer, address match, and that operation is for reception by reading the IICB0STR0.IICB0SSST, IICB0STR0.IICB0SSCO, and IICB0STR0.IICB0SSTR bits.
- Read the IICB0DAT register (empty reading).

<2> Wait timing setting

In data reception, clear the IICB0CTL0.IICB0SLWT bit to 0 to place the IIC in the wait state on the falling edge of the 8th clock cycle.

<3> Data reception

Set the IICB0TRG.IICB0WRET bit to 1b during the wait period to release the wait state and start reception.

<4> Loading received data

Read the received data from the IICB0DAT register in response to the IICBTIA interrupt.

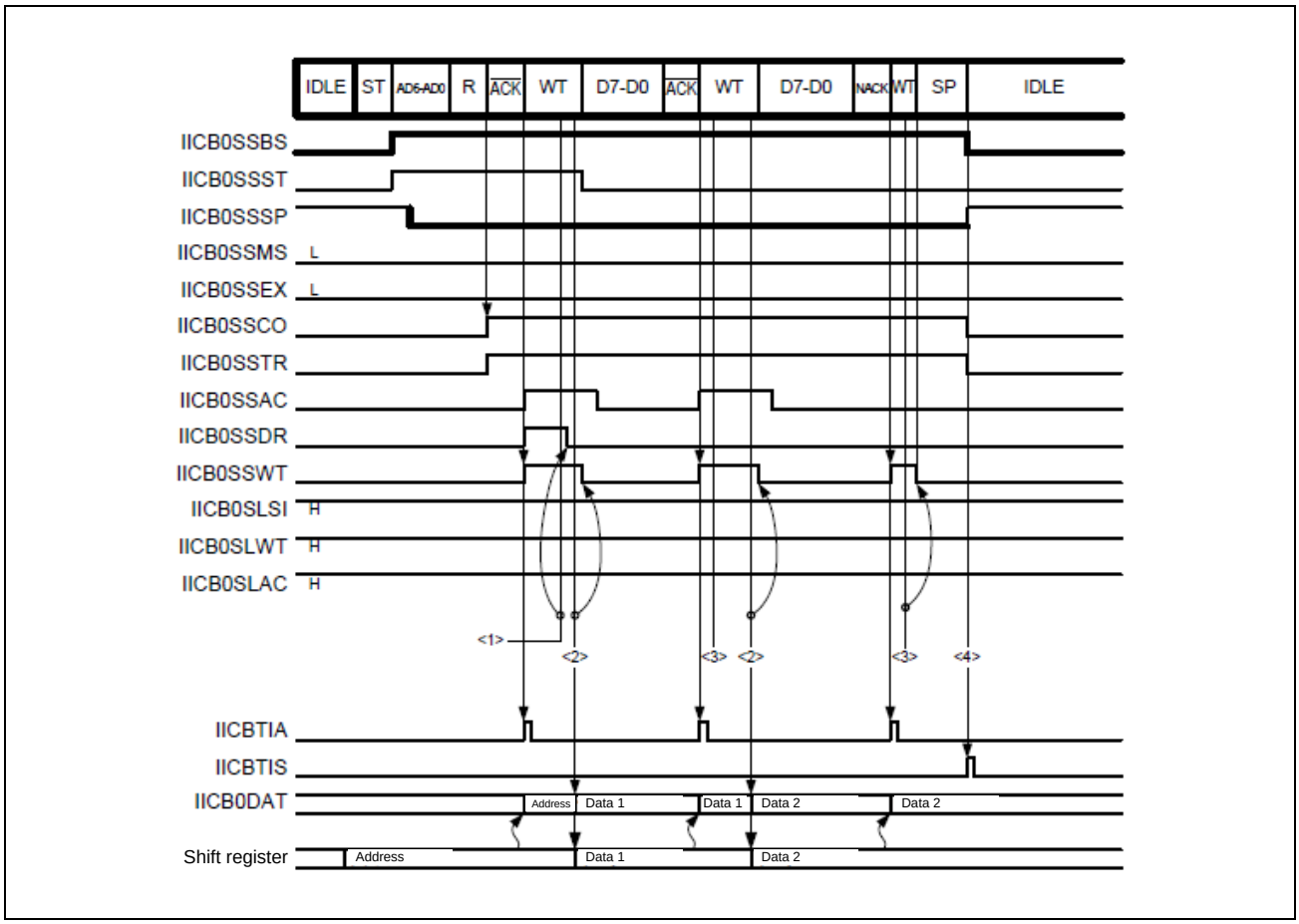
<5> Data reception completion processing

- Set the IICB0CTL0.IICB0SLWT bit to 1b and the IICB0CTL0.IICB0SLAC bit to 0b during the wait period.
- After that, set the IICB0TRG.IICB0WRET bit to 1b to release the wait state. An acknowledge is not generated and the transmitter is notified of the end of the data.

<6> Stop condition detection

A stop condition is detected in response to the IICBTIS interrupt.

(4) Example of Communications in Single Transfer Mode (Slave Transmission)



<1> Checking the operating mode in slave operation

- Check the operating mode in response to the IICBTIA interrupt.
- Check the address transfer, address match, and that operation is for transmission by reading the IICB0STR0.IICB0SSST, IICB0STR0.IICB0SSCO, and IICB0STR0.IICB0SSTR bits.
- Read the IICB0DAT register (empty reading).

<2> Data transmission

Set the data for transmission in the IICB0DAT register during the wait period to release the wait state and start transmission.

<3> Checking the acknowledge result

Check the result by reading the IICB0STR0.IICB0SSAC bit in response to the IICBTIA interrupt.

If an acknowledge is not generated, the transmission is judged to have been completed, and the IIC is released from the wait state by setting the IICB0TRG.IICB0WRET bit to 1b.

<4> Stop condition detection

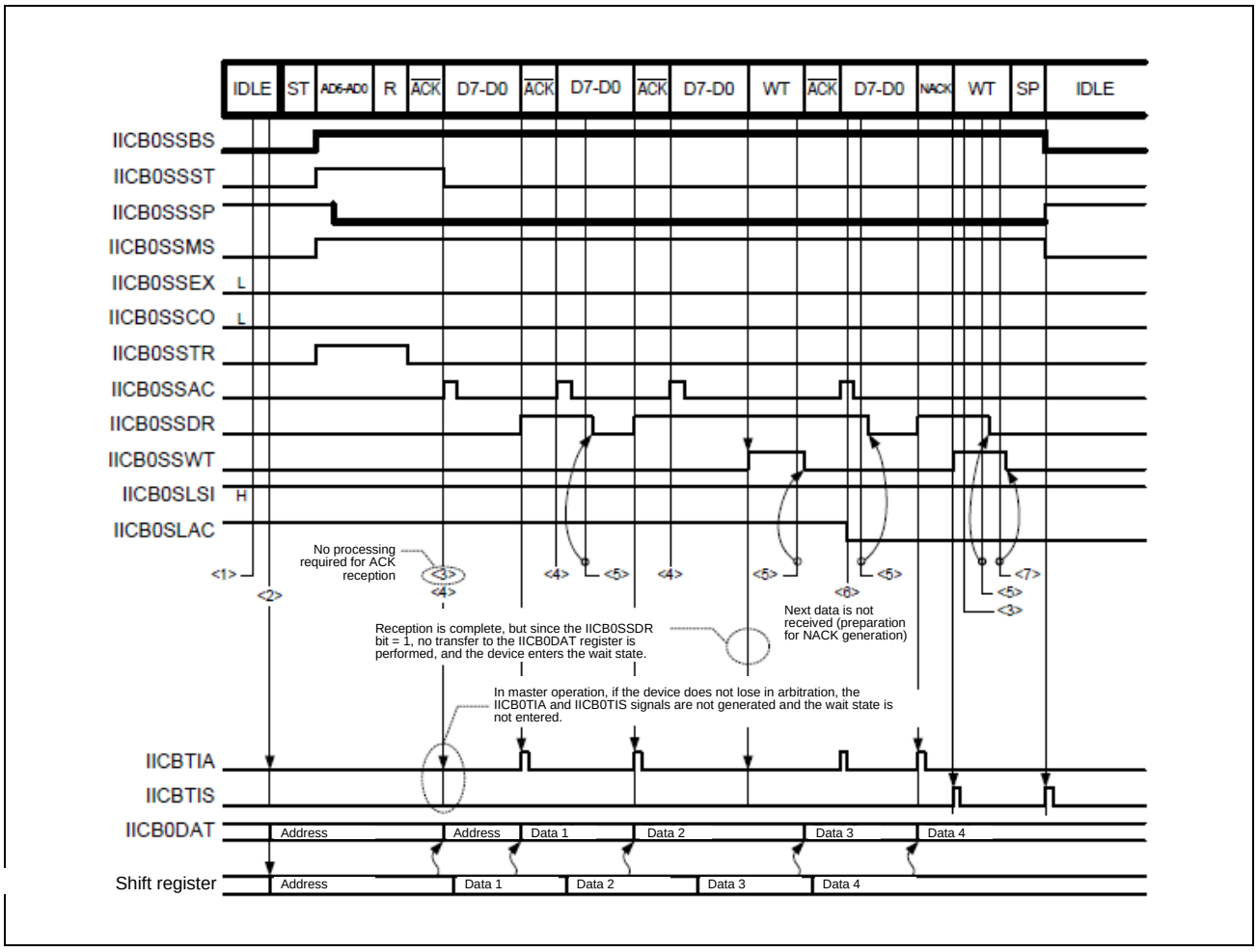
A stop condition is detected in response to the IICBTIS interrupt.

38.6.3.2 Continuous Transfer Mode

In continuous transfer mode, data can be transferred continuously without the IIC being placed in the wait state by reading from or writing to the IICB0DAT register every time a data transmission/reception interrupt request signal (IICBTIA) is generated.

Operations for each processing are described below.

(1) Example of Communicaitons in Continuous Transfer Mode (Master Reception)



<1> Start condition output

Set the IICB0TRG.IICB0STT bit to 1b.

<2> Address and transfer direction specification output

Set the combination of the slave's address and transfer direction as 8 bits in the IICB0DAT register.

<3> Checking the acknowledge result

The IICBTIS interrupt only occurs when the slave does not return the acknowledge.

Check the result by reading the IICB0STR0.IICB0SSAC bit.

<4> Checking the acknowledge result

If the IICB0DAT register has no unread data by the time reception starts, the IIC is not placed in the wait state and reception starts.

<5> Loading received data

Read the received data from the IICB0DAT register in response to the IICBTIA interrupt.

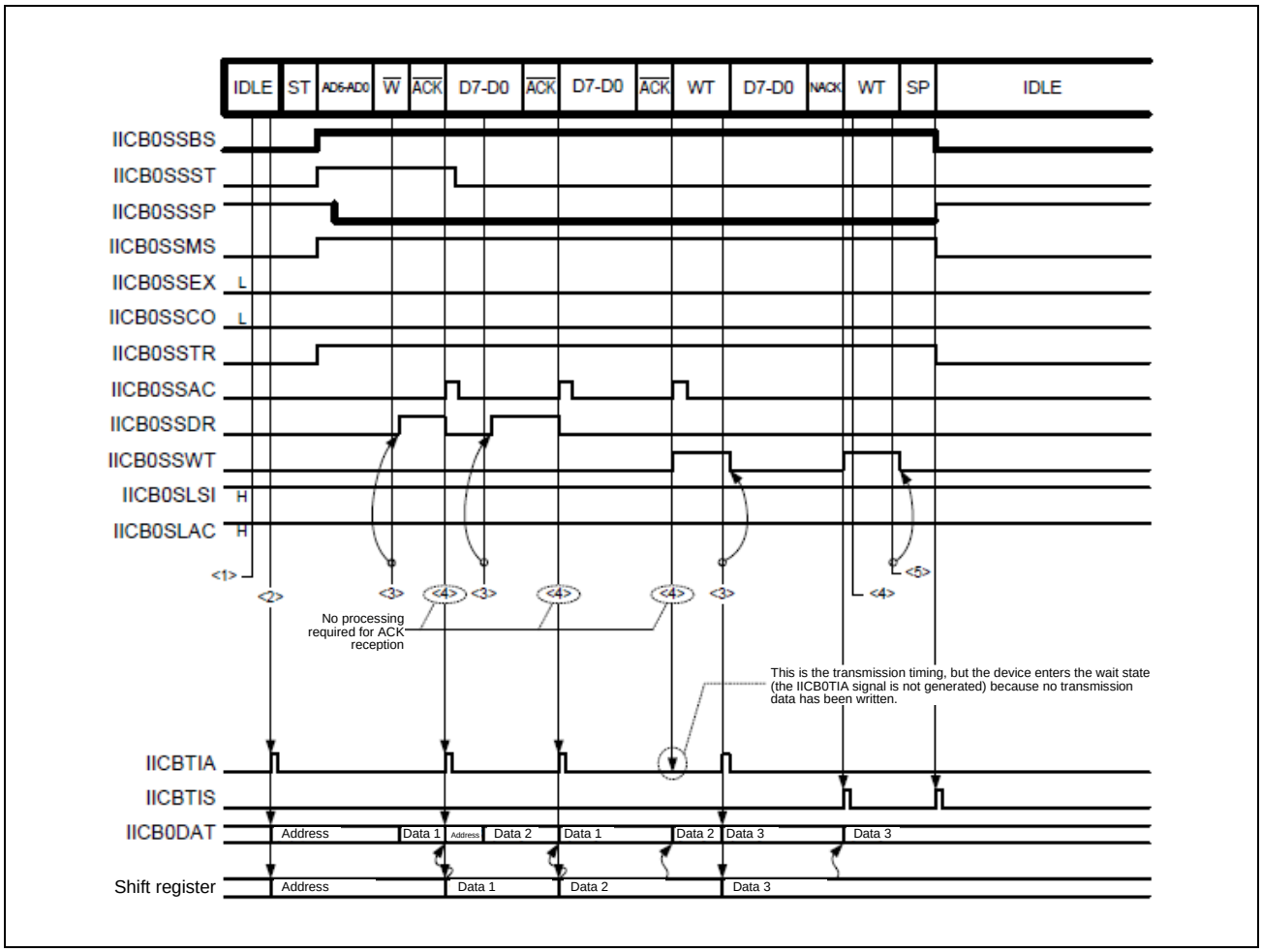
<6> Data reception completion processing

By clearing the IICB0CTL0.IICB0SLAC bit to 0b before reading the previous received data before the final received data, a next acknowledge is not generated and the transmitter is notified of the end of the data.

<7> Stop condition output

Set the IICB0TRG.IICB0SPT bit to 1b.

(2) Example of Comunications in Continuous Transfer Mode (Maaster Transmission)



<1> Start condition output

Set the IICB0TRG.IICB0STT bit to 1b.

<2> Address and transfer direction specification output

Set the combination of the slave's address and transfer direction as 8 bits in the IICB0DAT register.

<3> Data transmission

Set the data for transmission in the IICB0DAT register in response to the IICBTIA interrupt.

<4> Checking the acknowledge result

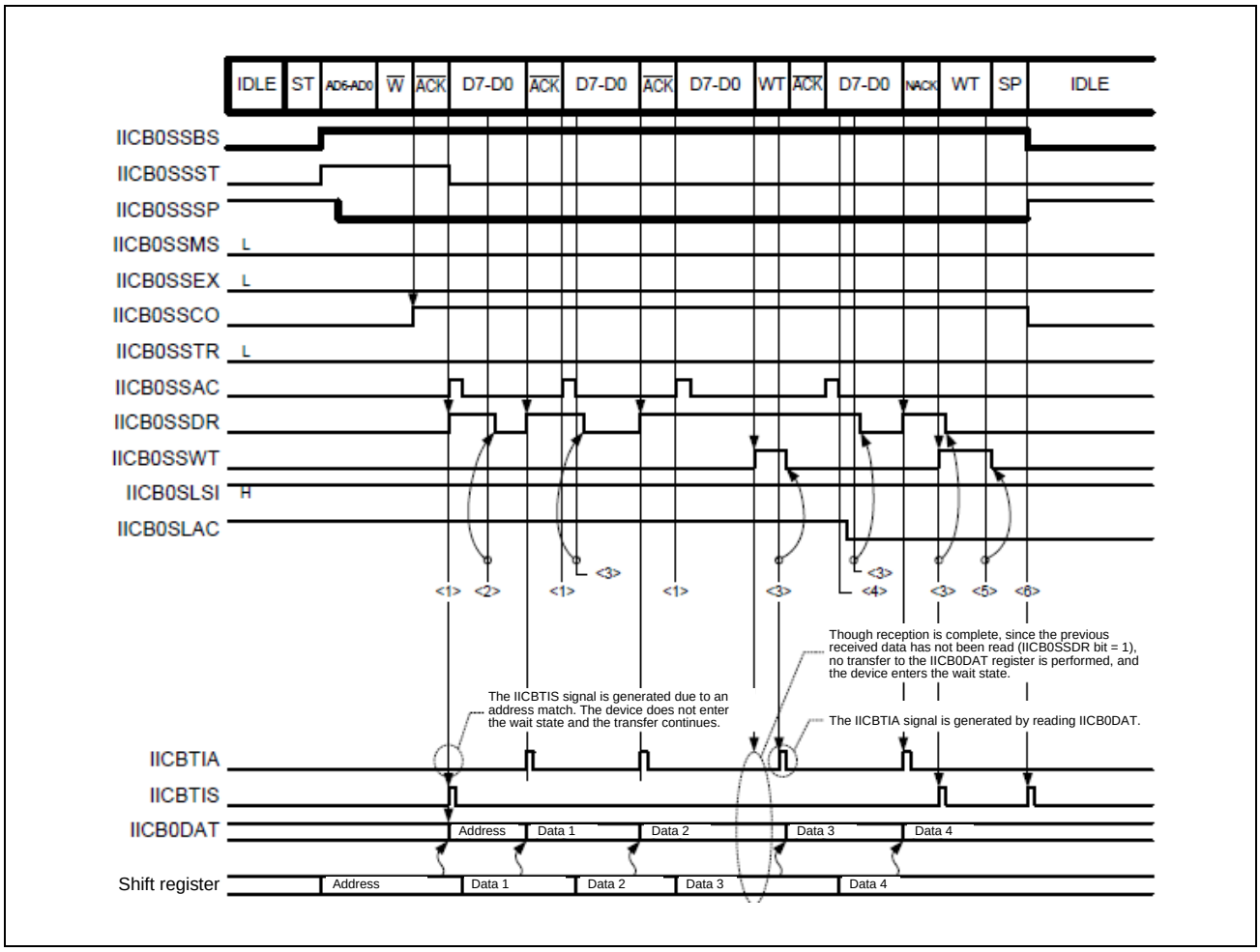
The IICBTIS interrupt only occurs when the slave does not return the acknowledge.

Check the result by reading the IICB0STR0.IICB0SSAC bit.

<5> Stop condition output

Set the IICB0TRG.IICB0SPT bit to 1b.

(3) Example of Communications in Continuous Transfer Mode (Slave Reception)



<1> Data reception

If the IICB0DAT register has no unread data by the time reception starts, the IIC is not placed in the wait state and reception starts.

<2> Checking the operating mode in slave operation

- Check the operating mode in response to the IICBTIS interrupt.
- Check the address transfer, address match, and that operation is for reception by reading the IICB0STR0.IICB0SSST, IICB0STR0.IICB0SSCO, and IICB0STR0.IICB0SSTR bits.
- Read the IICB0DAT register (empty reading).

<3> Loading received data

Read the received data from the IICB0DAT register in response to the IICBTIA interrupt.

<4> Data reception completion processing (1)

By clearing the IICB0CTL0.IICB0SLAC bit to 0b before reading the previous received data before the final received data, a next acknowledge is not generated and the transmitter is notified of the end of the data.

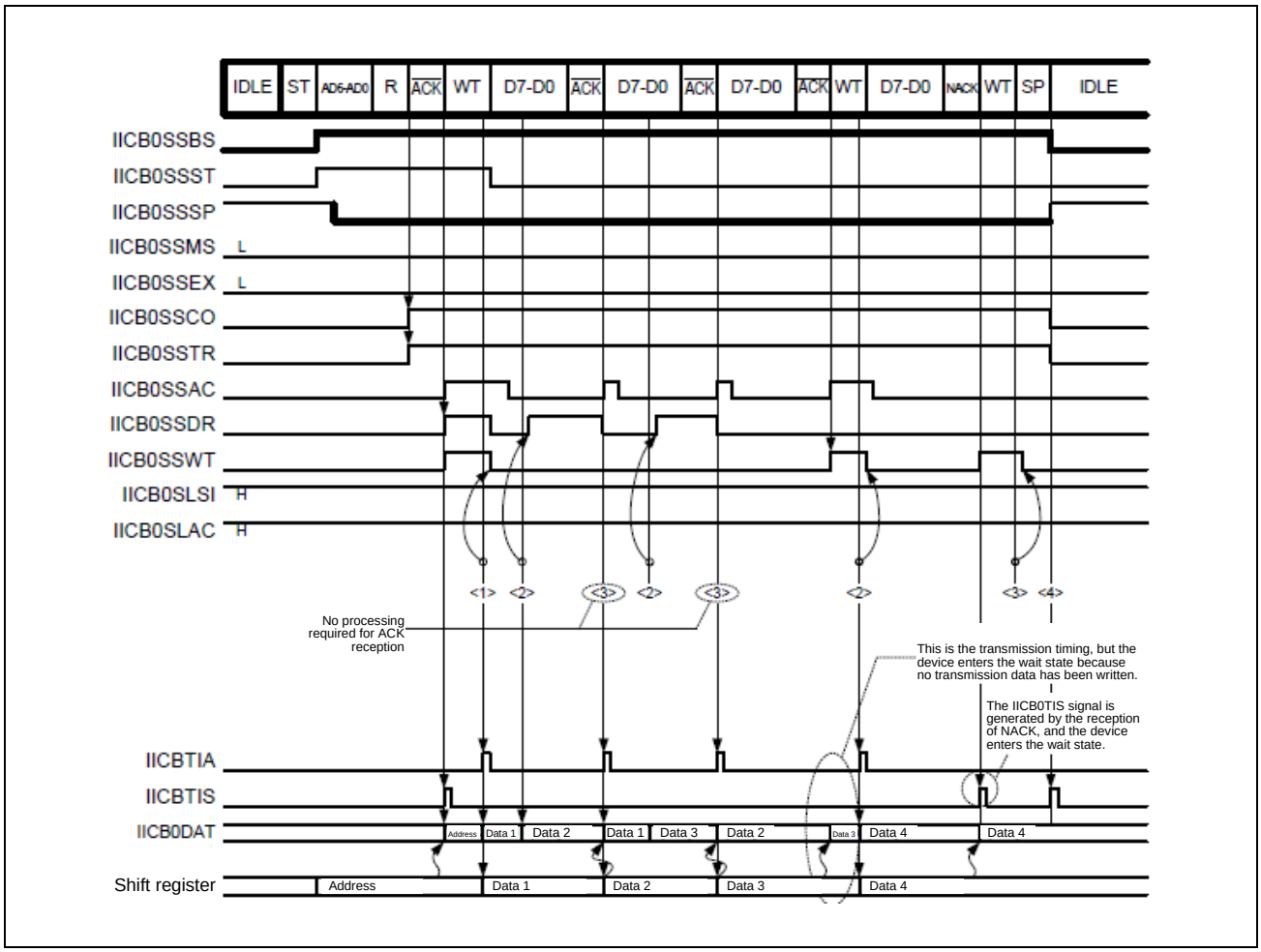
<5> Data reception completion processing (2)

The IICBTIS interrupt only occurs when the slave does not return the acknowledge.
The IIC is released from the wait state by setting the IICB0TRG.IICB0WRET bit to 1b.

<6> Stop condition detection

A stop condition is detected in response to the IICBTIS interrupt.

(4) Slave Transmission in Continuous Transfer Mode



<1> Checking the operating mode in slave operation

- Check the operating mode in response to the IICBTIS interrupt.
- Check the address transfer, address match, and that operation is for transmission by reading the IICB0STR0.IICB0SSST, IICB0STR0.IICB0SSCO, and IICB0STR0.IICB0SSTR bits.
- After reading the IICB0DAT register (empty reading), set the first data for transmission in the IICB0DAT register.

<2> Data transmission

Set the data for transmission in the IICB0DAT register in response to the IICBTIA interrupt.

<3> Checking the acknowledge result

The IICBTIS interrupt only occurs when the slave does not return the acknowledge.

Check the result by reading the IICB0STR0.IICB0SSAC bit.

If an acknowledge is not generated, the transmission is judged to have been completed, and the IIC is released from the wait state by setting the IICB0TRG.IICB0WRET bit to 1b.

<4> Stop condition detection

A stop condition is detected in response to the IICBTIS interrupt.

38.6.3.3 Processing of Final Data in Continuous Transfer Mode

The following describes operations for processing of final data when operation is in continuous transfer mode in the case of transmission and reception, respectively.

(1) Processing of Final Data in Reception

While operation is for reception, write 0b to ICB0SLAC before reading the previous received data before the final received data (reading IICB0DAT).

When the falling edge of the 8th clock cycle of SCLI is detected, the IIC judges whether the data received in the previous communications have been read.

If the data have been read, the IIC transmits the ACK bit in accord with the value of the IICB0SLAC bit at this time (on detection of the falling edge of the 8th clock cycle of SCLI) and is placed in the wait state if the data have not been read. When the data have been read from the IICB0DAT register, the IIC transmits the ACK bit in accord with the value of the IICB0SLAC bit.

Figure 38.6-9 is a timing chart of the example of final data processing in the case of reception.

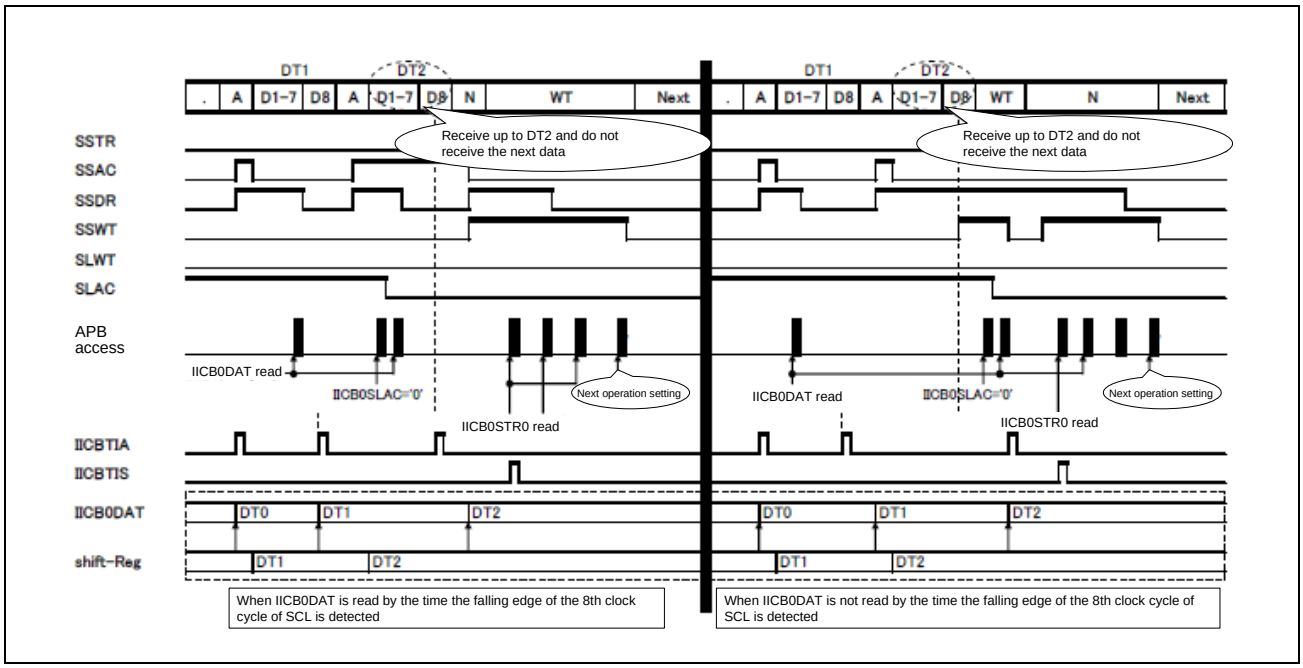


Figure 38.6-9 Processing of Final Data in Reception

(2) Processing of Final Data in Transmission

During the transmission operation, processing of final data differs in master operation and slave operation. The following describes operations for processing of final data in the case of master operation and slave operation.

< In master operation >

In master operation, a restart or stop condition is issued after the completion of transmission of the final data by writing 1b to IICB0STT or IICB0SPT after the IICBTIA interrupt following writing of the final data (with the timing of *1 in **Figure 38.6-10** when a restart or stop condition is set).

Even when writing of 1b to IICB0STT or IICB0SPT is delayed, the IIC is placed in the wait state (if data have not been written to IICB0DAT), so IICB0STT and IICB0SPT can be set to 1b. If 1b is written to IICB0STT at this time, subsequent writing to IICB0DAT is possible.

Figure 38.6-10 shows the operations for final data processing in the case of master operation.

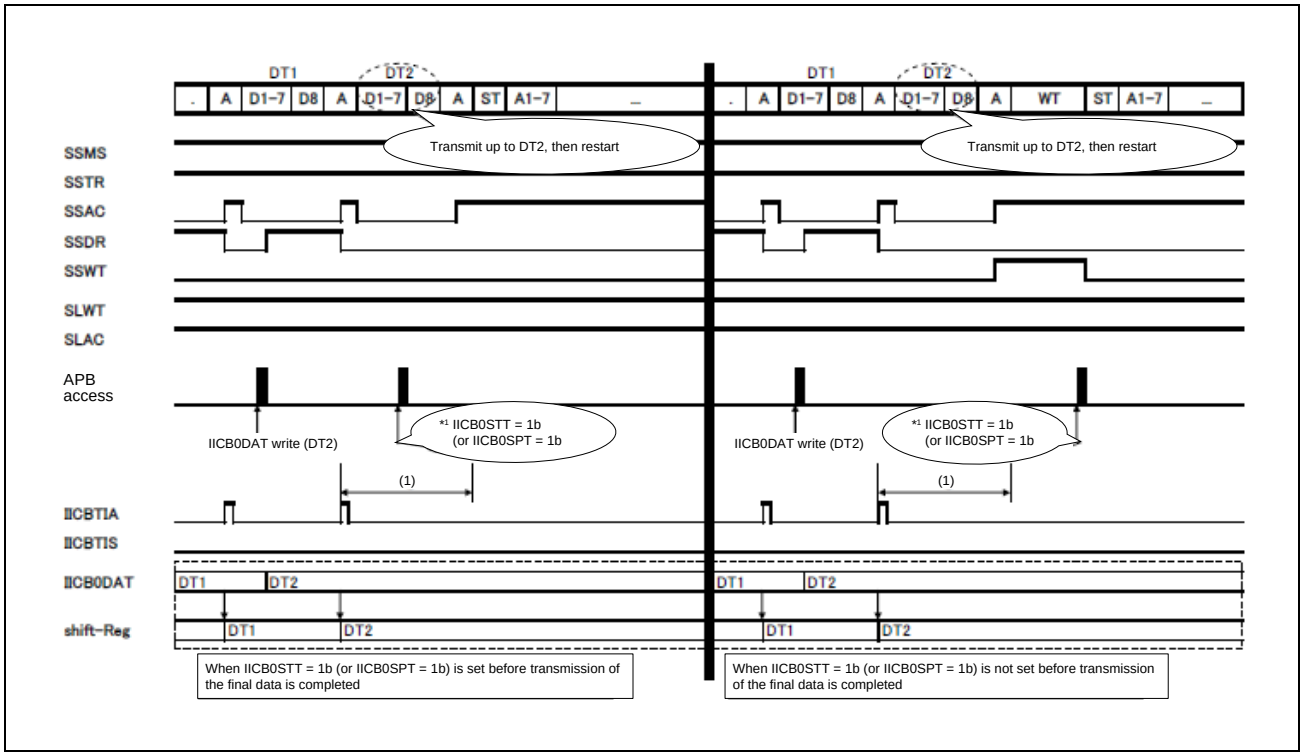


Figure 38.6-10 Operations for Final Data Processing in Transmission (IICB0SSMS = 1b & Continuous Transfer Mode)

When both writing 1 to IICB0STT and writing 1b to IICB0SPT proceed in the interval (1) in **Figure 38.6-10**, the subsequent setting is enabled and the previous setting is disabled.

Similarly, writing to IICB0DAT before writing 1b to IICB0STT (or to IICB0SPT) is ignored in the interval (1). The data written to IICB0DAT after 1b has been written to IICB0STT are transmitted as the data following the output of a start condition (the address).

< In slave operation >

In slave operation, the (external) master determines the final data. Accordingly, the data must always be transmitted (written to IICB0DAT) when ACK is received by the (external) master.

CAUTION

Even if there are no data for transmission, write any data to IICB0DAT. If writing to IICB0DAT does not proceed, bus communications may be stopped because the unit retains its state while in the wait state.

38.6.3.4 Arbitration

When multiple masters generate a start condition at the same time, master communications proceed while adjusting the clock cycles until the data differ from one another. **Figure 38.6-11** shows an example where two masters output a start condition at the same time and arbitration occurs.

Here, suppose that a master which outputs the high level to the SDA line (master 1) and a master which outputs the low level to the SDA line (master 2) are present when the SCL line is at the low level.

In this case, communications by the master which outputs the low level to the SDA line (master 2) are given priority, and communications are not permitted for the master which outputs the high level to the SDA line (master 1). Such procedure is called arbitration and the state where communications are not permitted is called arbitration loss.

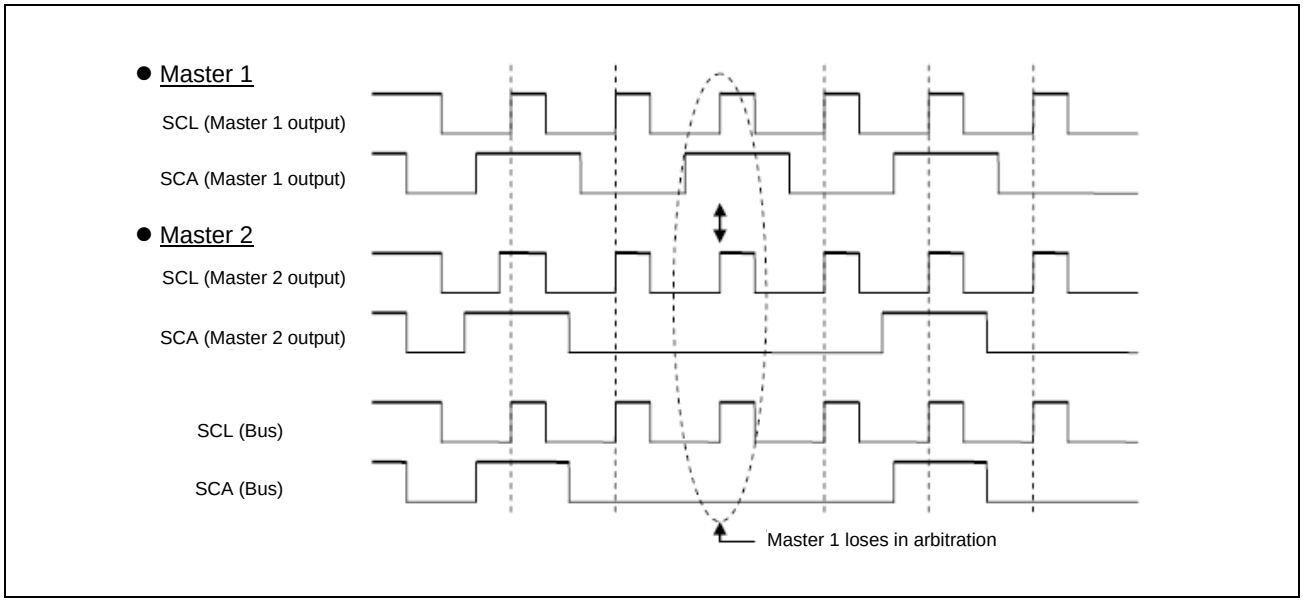


Figure 38.6-11 Example of Arbitration Loss

When this unit detects an arbitration loss in the master, it drives SCLm and SDAm to the high level respectively to place the slave in the standby state, and sets the IICB0STR0.IICB0ALDF bit to 1b at the time a status interrupt request signal (IICBTIS) is subsequently generated.

(1) State when Arbitration Occurs

The following describes the states in which arbitration occurs in master operation (the IICB0STR0.IICB0SSMS bit = 1b).

1) Address transmission is in progress.
2) Transmission of R/W bits for address transfer is in progress.
3) Transmission of the extension code is in progress.
4) Transmission of R/$\overline{W}$ bits for extension code transfer is in progress.
5) Data transmission is in progress.
6) Transmission of the $\overline{ACK}$ bit after data reception is in progress.
7) The start condition is detected while address transfer or data transfer is in progress.

8) The stop condition is detected while address transfer or data transfer is in progress.

9) The SDAm pin remains at the low level though generation of a restart condition is attempted.

10) The SDAm pin remains at the low level though generation of a stop condition is attempted.

11) A falling edge of the SCLm pin is detected though generation of a restart condition is attempted.

(2) Arbitration Checking Period and Judging Arbitration Loss

The following describes the states from (1) to (11) described in **Section 38.6.3.4(1), State when Arbitration Occurs**.

In (1) to (6), SDAO and SDAI are compared when a rising edge of SCLI is detected, and if SDAO = “H” & SDAI = “L”, this is judged to be an arbitration loss.

In (7), arbitration is checked all through the period while IICB0SSMS = 1b. In the checking period, detection of the start condition that is not output by itself is judged to be an arbitration loss.

In (8), arbitration is checked all through the period while IICB0SSMS = 1b. In the checking period, detection of the stop condition that is not output by itself is judged to be an arbitration loss.

Figure 38.6-12 shows the checking range from (1) to (8).

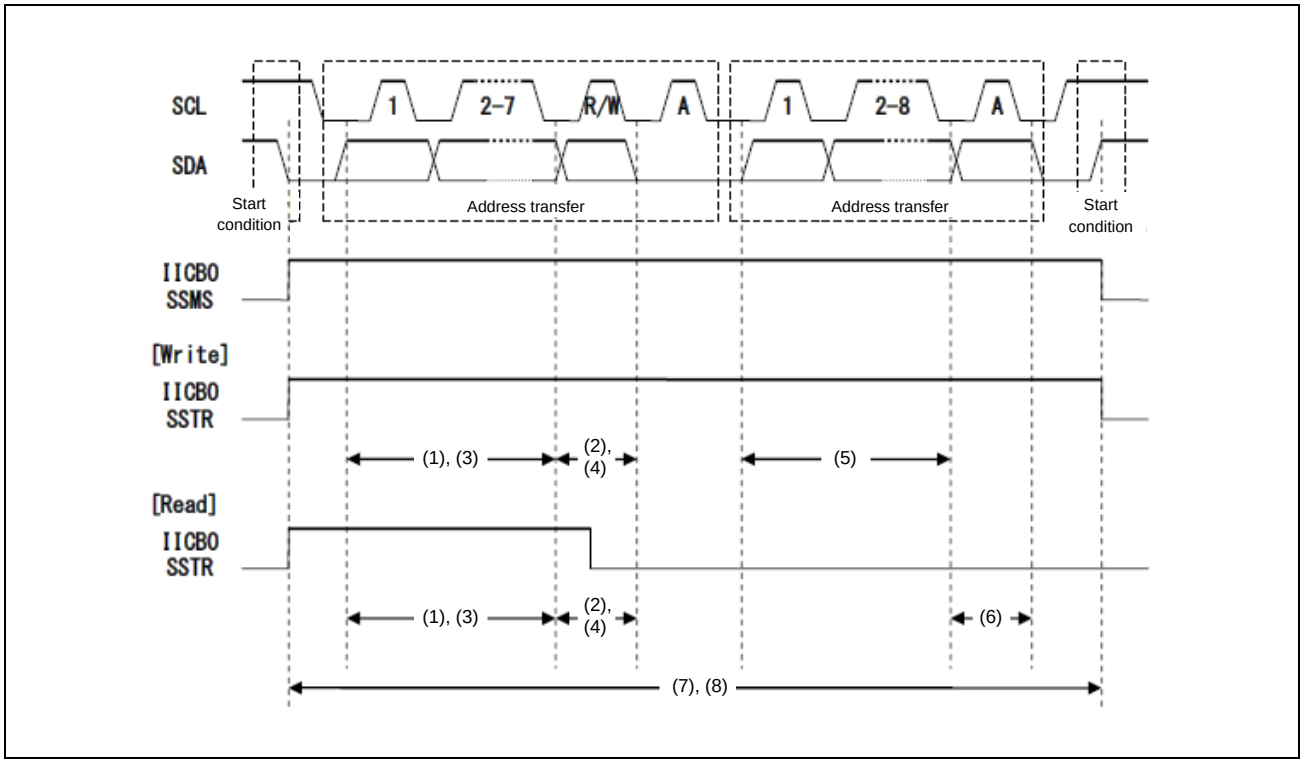


Figure 38.6-12 Arbitration Checking Range (from (1) to (8))

In (9), after writing 1 to IICB0STT, arbitration is checked when the first rising edge of SCLI is detected while the output of a restart condition is being prepared. If SDAI = “L” at this time, this is judged to be an arbitration loss. **Figure 38.6-13** shows the arbitration-lost state in (9).

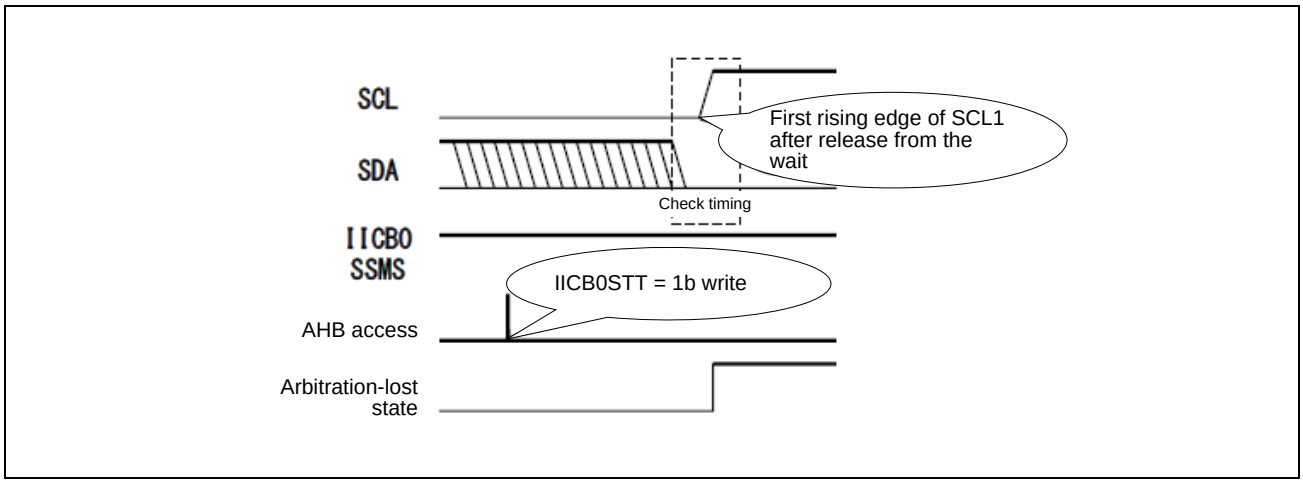


Figure 38.6-13 Arbitration-Lost State in (9)

In (10), after writing 1 to IICB0SPT, arbitration is checked when the first falling edge of SCLI after the output of a stop condition is detected. When the stop condition is not detected by the time the falling edge of SCLI is detected, this is judged to be an arbitration loss. **Figure 38.6-14** shows the arbitration-lost state.

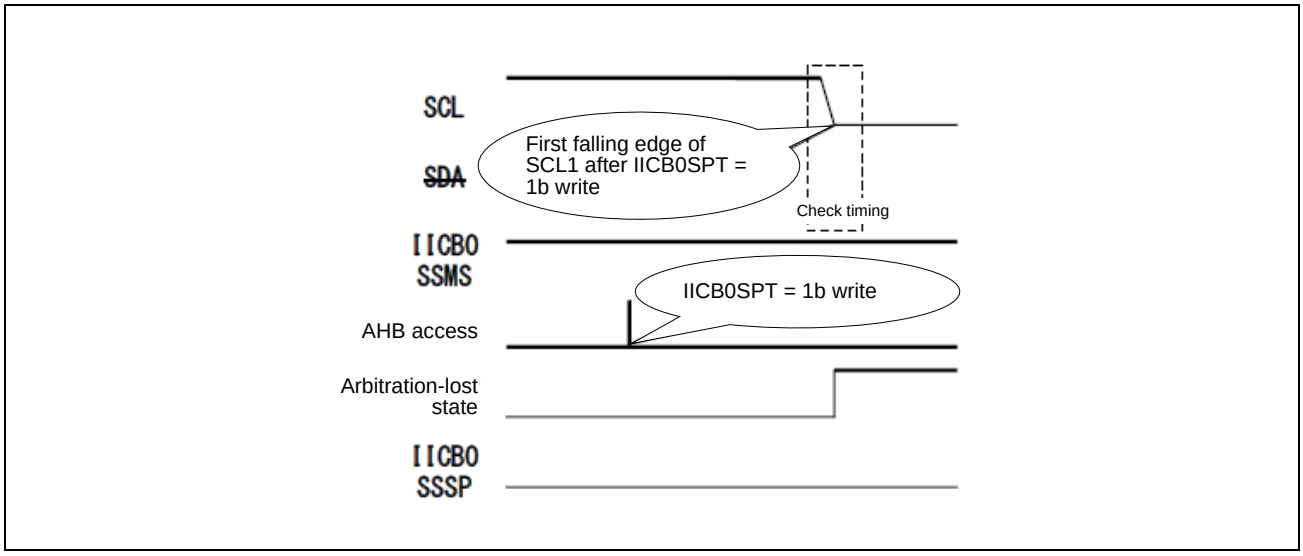


Figure 38.6-14 Arbitration-Lost State in (10)

In (11), after writing 1 to IICB0STT, arbitration is checked when the first falling edge of SCLI is detected while the output of a restart condition is being prepared. When the restart condition is not detected by the time the falling edge of SCLI is detected, this is judged to be an arbitration loss. **Figure 38.6-15** shows the arbitration-lost state.

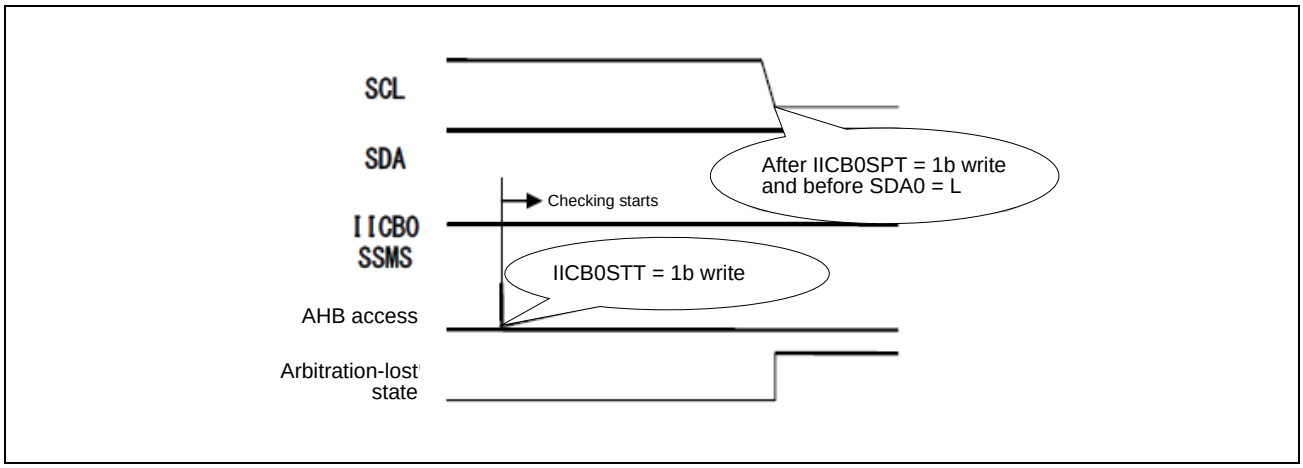
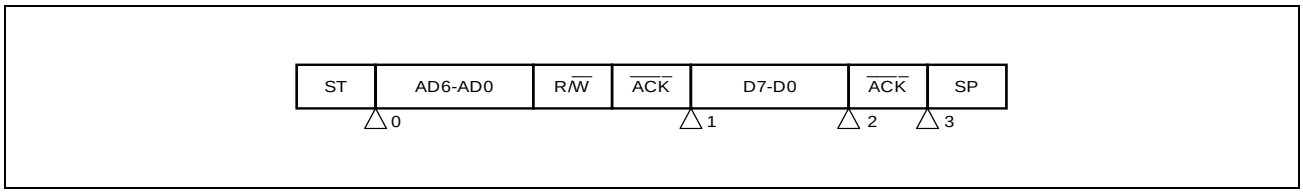


Figure 38.6-15 Arbitration-Lost State in (11)

38.6.3.5 Procedure for Transition to and Release from the Wait State

This unit can be placed in the wait state with the timing shown below.

Table 38.6-2 Timing of Transition to the Wait State



Generation Timing	Description	Reference
△0	Detection of the first falling edge of SCLm after detection of the start condition as the master	**Section 38.6.3.5(1), Wait State on the First Falling Edge of SCLm as the Master**
△1	Detection of the falling edge of the 9th clock cycle of SCLm while address transfer following the start condition is in progress	**Section 38.6.3.5(2), Wait State on Completion of Address Transfer**
△2	Detection of the falling edge of 8th clock cycle of SCLm while data transfer is in progress	**Section 38.6.3.5(3), Wait State on Detection of the 8th Falling Edge of SCLm during Data Transfer**
△3	Detection of the falling edge of 9th clock cycle of SCLm while data transfer is in progress	**Section 38.6.3.5(4), Wait State on Detection of the 9th Falling Edge of SCLm during Data Transfer**

Note: ST: Start condition
AD6-AD0: Address
R/$\overline{W}$: Transfer direction specification
$\overline{ACK}$: Acknowledge
D7-D0: Data
SP: Stop condition

The procedure for release from the wait state depends on the state of waiting.

Release the wait state according to the release conditions for the respective wait states described in **Section 38.6.3.5(1)** to **Section 38.6.3.5(4)**.

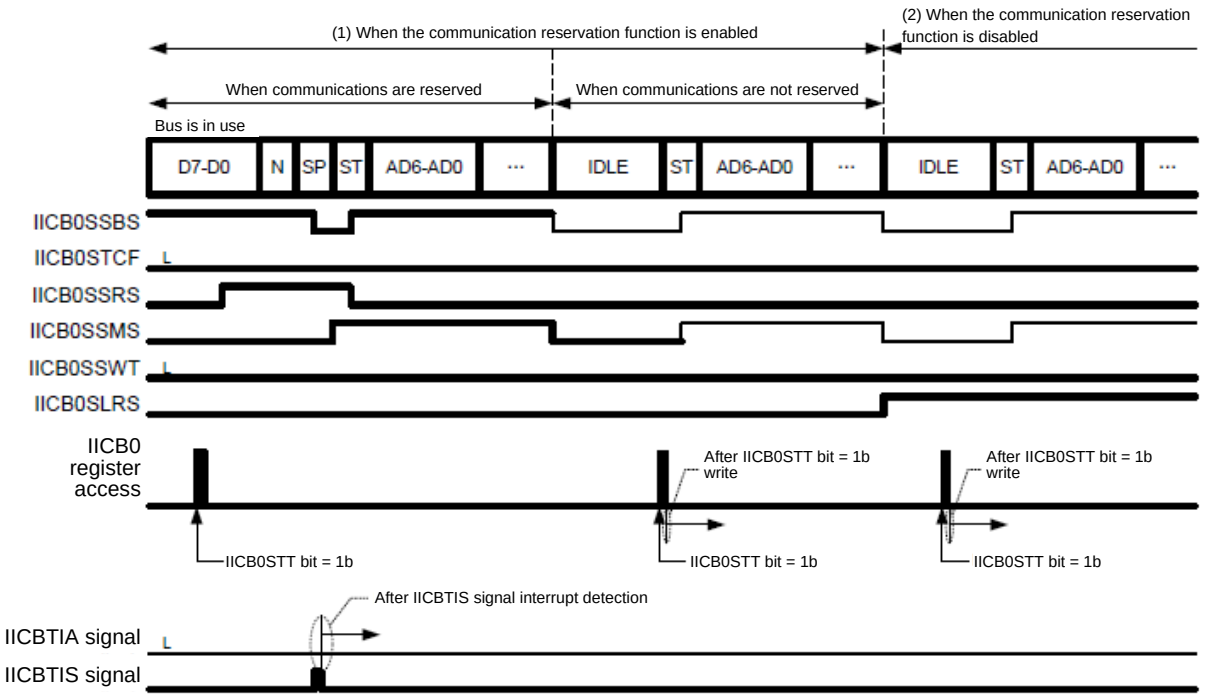
(1) Wait State on the First Falling Edge of SCLm as the Master

△0 is a wait state in the case where the data to be transferred have not been written to the IICB0DAT register when the first falling edge of SCLm as the master is detected after writing 1 to the IICB0TRG.IICB0STT bit.

(a) Condition for Transition to the Wait State

After writing 1b to the IICB0TRG.IICB0STT bit, the IIC is placed in the wait state on detection of the first falling edge of SCLm as the master if writing to the IICB0DAT register has not proceeded by the time of △0 after writing 1b to the IICB0TRG.IICB0STT bit.

However, the timing at which effective writing to the IICB0DAT register can proceed (without a wait) after writing 1b to the IICB0TRG.IICB0STT bit differs between when the communication reservation function is permitted and when this function is prohibited. **Figure 38.6-16** shows the timing of effective writing to the IICB0DAT register with the respective settings.



Caution:

When “(2) The communication reservation function is prohibited” in the figure, the IICB0STR0.IICB0STCF bit = 0b. If the IICB0STR0.IICB0STCF bit = 1b, re-setting from writing 1 to the IICB0STR0.IICB0STCF bit is required.

Figure 38.6-16 Timing of Effective Writing to the IICB0DAT Register

(b) Condition for Release from the Wait State

Release the wait state by writing to the IICB0DAT register.

(2) Wait State on Completion of Address Transfer

△1 is a wait state on completion of address transfer.

(a) Condition for Transition to the Wait State

< Single transfer mode >

In single transfer mode, the IIC is always placed in the wait state in master operation. In slave operation, it is placed in the wait state in response to an address match or the extension code being detected and when the IICB0CTL0.IICB0SLWT bit = 1b.

< Continuous transfer mode >

In continuous transfer mode, the IIC is placed in the wait state in any of the following cases.

- NACK being detected.
- In master transmission, the next data for transfer not having been written.
- In slave operation, the previous received data not having been read or operation is for transmission.

(b) Condition for Release from the Wait State

< Single transfer mode >

Release the wait state by writing to the IICB0DAT register in transmission and by writing 1b to the IICB0TRG.IICB0WRET bit in reception. In master operation, if the IICB0STR0.IICB0SSAC bit = 0b and operation is for transmission, releasing the wait state is possible by writing 1 to the IICB0TRG.IICB0STT or IICB0TRG.IICB0SPT bit.

< Continuous transfer mode >

Release the wait state by writing to the IICB0DAT register in transmission and by reading the IICB0DAT register in reception. In master operation, if the IICB0STR0.IICB0SSAC bit = 0b, releasing the wait state is possible by writing 1b to the IICB0TRG.IICB0STT or IICB0TRG.IICB0SPT bit.

(3) Wait State on Detection of the 8th Falling Edge of SCLm during Data Transfer

△2 is a wait state on detection of the 8th falling edge of SCLm during data transfer.

(a) Condition for Transition to the Wait State

< Single transfer mode >

When the IICB0CTL0.IICB0SLWT bit = 0 while the IIC participates in communications, the IIC is placed in the wait state on detection of the 8th falling edge of SCLm.

< Continuous transfer mode >

When the IICB0STR0.IICB0SSTR bit = 0b while the IIC participates in communications, the IIC is placed in the wait state if processing of the previous data (reading from the IICB0DAT register) has not proceeded and 1b has not been written to the IICB0TRG.IICB0STT or IICB0TRG.IICB0SPT bit before the 8th falling edge of SCLm.

(b) Condition for Release from the Wait State

< Single transfer mode >

Release the wait state by writing 1b to IICB0TRG.IICB0WRET in reception and by writing to the IICB0DAT register in transmission.

< Continuous transfer mode >

Release the wait state by reading the IICB0DAT register.

(4) Wait State on Detection of the 9th Falling Edge of SCLm during Data Transfer

△3 is a wait state on detection of the 9th falling edge of SCLm during data transfer. In continuous transfer mode, the IIC is placed in the wait state on reception of NACK.

(a) Condition for Transition to the Wait State

< Single transfer mode >

When the IICB0CTL0.IICB0SLWT bit = 1 while the IIC participates in communications, the IIC is placed in the wait state on detection of the 9th falling edge of SCLm.

< Continuous transfer mode >

The IIC is placed in the wait state in any of the following states (when it participates in communications in all cases) during data transmission.

- NACK being received in the $\overline{\text{ACK}}$ bit while the IICB0CTL0.IICB0SLWT bit = 1b.
- In transmission, the data for transmission not having been written to the data register.
- In reception, the previous received data not having been read.

(b) Condition for Release from the Wait State

Table 38.6-3 lists the conditions for release from the wait state in each mode.

Table 38.6-3 Conditions for Release from the Wait State

Master/Slave	Transfer Mode	Transmission/ Reception	IICB0STR0. IICB0SSAC Bit	Release Operation
Master	Single transfer mode	Reception	0b	IICB0TRG.IICB0STT bit = 1b or IICB0TRG.IICB0SPT bit = 1b
			1b	IICB0TRG.IICB0WRET = 1b
		Transmission	0b	IICB0TRG.IICB0STT bit = 1b or IICB0TRG.IICB0SPT bit = 1b
			1b	Writing to the IICB0DAT register or IICB0TRG.IICB0STT bit = 1b or IICB0TRG.IICB0SPT bit = 1b
	Continuous transfer mode	Reception	0b	IICB0TRG.IICB0STT bit = 1b or IICB0TRG.IICB0SPT bit = 1b
			1b	Reading from the ICBnDAT register*1
		Transmission	0b	IICB0TRG.IICB0STT bit = 1b or IICB0TRG.IICB0SPT bit = 1b
			1b	Writing to the IICB0DAT register*2
Slave	Single transfer mode	Reception	—	IICB0TRG.IICB0WRET bit = 1b
		Transmission	0b	IICB0TRG.IICB0WRET bit = 1b
			1b	Writing to the IICB0DAT register*1
	Continuous transfer mode	Reception	0b	IICB0TRG.IICB0WRET bit = 1b
		Transmission	0b	IICB0TRG.IICB0WRET bit = 1b
			1b	Writing to the IICB0DAT register

Note 1. The condition for release from the wait state due to the data for transmission not having been written to the data register.

Note 2. The condition for release from the wait state due to the previous received data not having been read.

38.6.3.6 Extension Code

The processing when the extension code is received differs with the data following the extension code, so this processing must be handled by the user's software processing.

Therefore, the operation differs from that at the time of normal slave address reception. The differences are as follows.

(1) When the higher-order 4 bits of the received address are 0000 or 1111, the extension code reception flag (IICB0STR0.IICB0SSEX bit) is set to indicate the reception of the extension code, and a status interrupt request signal (IICBTIS) is generated on the falling edge of the 8th clock cycle, and then the IIC is placed in the wait state (ICB0TRG.IICB0SSWT = 1b).
Also, the IICB0STR0.IICB0SSDR and IICB0STR0.IICB0SSTR bits are set to 1b.

(2) In the output of the acknowledge during address transfer, the acknowledge can be controlled by the setting of the IICB0CTL0.IICB0SLAC bit. During address transfer at the time of normal slave address reception, the acknowledge is output when the addresses match, regardless of the setting of IICB0CTL0.IICB0SLAC.

(3) The procedure for release from the wait state on detection of the extension code is as follows.

- When the IICB0CTL0.IICB0MDTX1 bit = 0b
  In the case of transmission while the IICB0CTL0.IICB0SLWT bit = 0b, release the wait state by writing to the IICB0DAT register. In the case of transmission while the IICB0CTL0.IICB0SLWT bit = 1b or in the case of reception, release the wait state by writing 1b to the IICB0TRG.IICB0WRET bit.
- When the IICB0CTL0.IICB0MDTX1 bit = 1b
  Release the wait state by writing to the IICB0DAT register in transmission and by reading the IICB0DAT register in reception.

(4) On the falling edge of the 9th clock cycle after that, an interrupt request signal (IICBTIA) is generated and the IIC is placed in the wait state (the IICB0TRG.IICB0SSWT bit =1b) if the IICB0CTL0.IICB0SLWT bit = 1b. If the IICB0CTL0.IICB0SLWT bit = 0b, an interrupt request signal (IICBTIA) is not generated and the IIC is not placed in the wait state.

(5) When the IIC receives the extension code, it participates in communications even if the addresses do not match. For example, when the IIC is not to operate as a slave after the reception of the extension code, set the IICB0TRG.IICB0LRET bit to 1b. The IIC is placed in the standby state for the next communications.

38.7 Interrupts

38.7.1 Interrupt Request Signal

CAUTION

The operation when receiving an extension code is omitted from the description. For details, see section, 38.6.2.3, Extention Code.

This unit has two interrupt request signals: a data transmission/reception interrupt request signal (IICBTIA) and a status interrupt request signal (IICBTIS). The timing of the interrupt request signal generation differs depending on the transfer mode set in the IICB0CTL0.IICB0MDTX1 and IICB0CTL0.IICB0MDTX0 bits. In this section, the respective interrupt request signals are explained for different transfer modes.

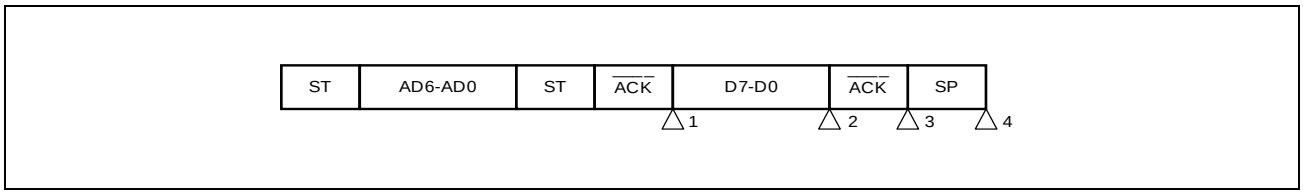
For the selection of single transfer mode or continuous transfer mode, the IICB0CTL0.IICB0MDTX0 bit is used for transfer on an address match between the master and slave, and the IICB0CTL0.IICB0MDTX1 bit is used for transfer on detection of the extension code by the slave.

38.7.1.1 Single Transfer Mode

The table below shows the interrupt request signal generation timing in the single transfer mode.

In single transfer mode, with the IICBTIA interrupt request signal and the IICBTIS interrupt request signal, whether to generate an interrupt is judged based on the status of this unit when the SCLm falling edge of the bus cycle is detected. However, only in the case of the △4 timing, whether to generate an interrupt is judged based on the status of the unit when the stop condition is detected.

Table 38.7-1 Interrupt Request Signal Generation Timing (Single Transfer Mode)



Generation Timing	Description	Reference
△1	When the falling edge of the 9th clock of SCLm is detected during address transfer	**Section 38.7.1.1(1), Conditions for Generating Interrupt Request Signals during Address Transfer and Interrupt Request Signals Generated**
△2	When the falling edge of the 8th clock of SCLm is detected during data transfer	**Section 38.7.1.1(2), Conditions for Generating Interrupt Request Signals during Data Transfer and Interrupt Request Signals Generated**
△3	When the falling edge of the 9th clock of SCLm is detected during data transfer	**Section 38.7.1.1(2), Conditions for Generating Interrupt Request Signals during Data Transfer and Interrupt Request Signals Generated**
△4	When stop condition is detected	**Section 38.7.1.1(3), Interrupt Request Signal Generation when Stop Condition is Detected**

Note: ST: Start condition
AD6-AD0: Address
R/$\overline{W}$: Transfer direction specification
$\overline{ACK}$: Acknowledge
D7-D0: Data
SP: Stop condition

(1) Conditions for Generating Interrupt Request Signals during Address Transfer and Interrupt Request Signals to be Generated

△1 in **Table 38.7-1** is the timing of interrupt request signal generation during address transfer. **Table 38.7-2** shows the interrupt request signal generation conditions at △1 and the interrupt request signals (IICBTIA or IICBTIS) that are generated.

Table 38.7-2 Conditions for Generating Interrupt Request Signals during Address Transfer and Interrupt Request Signals to be Generated (Single Transfer Mode)

IICB0 SSMS	IICB0 ALDF	IICB0 SLWT	IICB0 SSCO	△1		Remarks
				Interrupt	Wait	
1b	0b	×	×	IICBTIA	Wait	—
1b	1b	×	×	There is no such condition.		—
0b	0b	×	0b	IICBTIS*1	—	Non-participation in communications after restart
0b	0b	×	1b	IICBITAn	Wait	—
0b	1b	×	0b	IICBTIS	—	Non-participation in communications after the arbitration loss
0b	1b	×	1b	IICBTIA	Wait	—

Note: ×: Don't care

Note 1. An address match or extension code is detected before the restart condition.

(2) Conditions for Generating Interrupt Request Signals during Data Transfer and Interrupt Request Signals Generated

△2 and △3 in **Table 38.7-1** are the timing of interrupt request signal generation during data transfer. The timing of the interrupt request signal generation at △2 or △3 is determined by the setting of the IICB0CTL0.IICB0SLWT bit. **Table 38.7-3** lists the conditions for generating interrupt request signals at the △2 and △3 timing and the interrupt request signals (IICBTIA or IICBTIS) that are generated.

Table 38.7-3 Conditions for Generating Interrupt Request Signals during Data Transfer and Interrupt Request Signals to be Generated (Single Transfer Mode)

IICB0 SSMS	IICB0 ALDF	IICB0 SLWT	IICB0 SSCO	△2		△3		Remarks
				Interrupt	Wait	Interrupt	Wait	
1b	0b	0b	×	IICBTIA	Wait	—	—	—
1b	0b	1b	×	—	—	IICBTIA	Wait	—
1b	1b	×	×	There is no such condition.				—
0b	0b	×	0b	—	—	—	—	Non-participation in communications
0b	0b	0b	1b	IICBTIA	Wait	—	—	—
0b	0b	1b	1b	—	—	IICBTIA	Wait	—
0b	1b	0b	0b	IICBITSn	—	—	—	Non-participation in communications after the arbitration loss
0b	1b	1b	0b	—	—	IICBTIS	—	Non-participation in communications after the arbitration loss
0b	1b	0b	1b	IICBTIA	Wait	—	—	—
0b	1b	1b	1b	—	—	IICBTIA	Wait	—

Note: ×: Don't care

(3) Interrupt Request Signal Generation when Stop Condition is Detected

△4 in **Table 38.7-1** is the timing of interrupt request signal generation when a stop condition is detected.

When the stop condition is detected, the interrupt request signal generation is controlled by setting the IICB0CTL0.IICB0SLSI bit. When the IICB0CTL0.IICB0SLSI bit is set to 1b and a stop condition is detected, a status interrupt request signal (IICBTIS) is generated.

38.7.1.2 Continuous Transfer Mode

(1) Data Transmission/Reception Interrupt Request Signal (IICBTIA)

The following shows the conditions under which the IICBTIA signal is generated in continuous transfer mode.

- Conditions for generating an interrupt request signal upon reception

  When the receive data is stored from the shift register to the IICB0DAT register (**Figure 38.7-1**, timing (1))

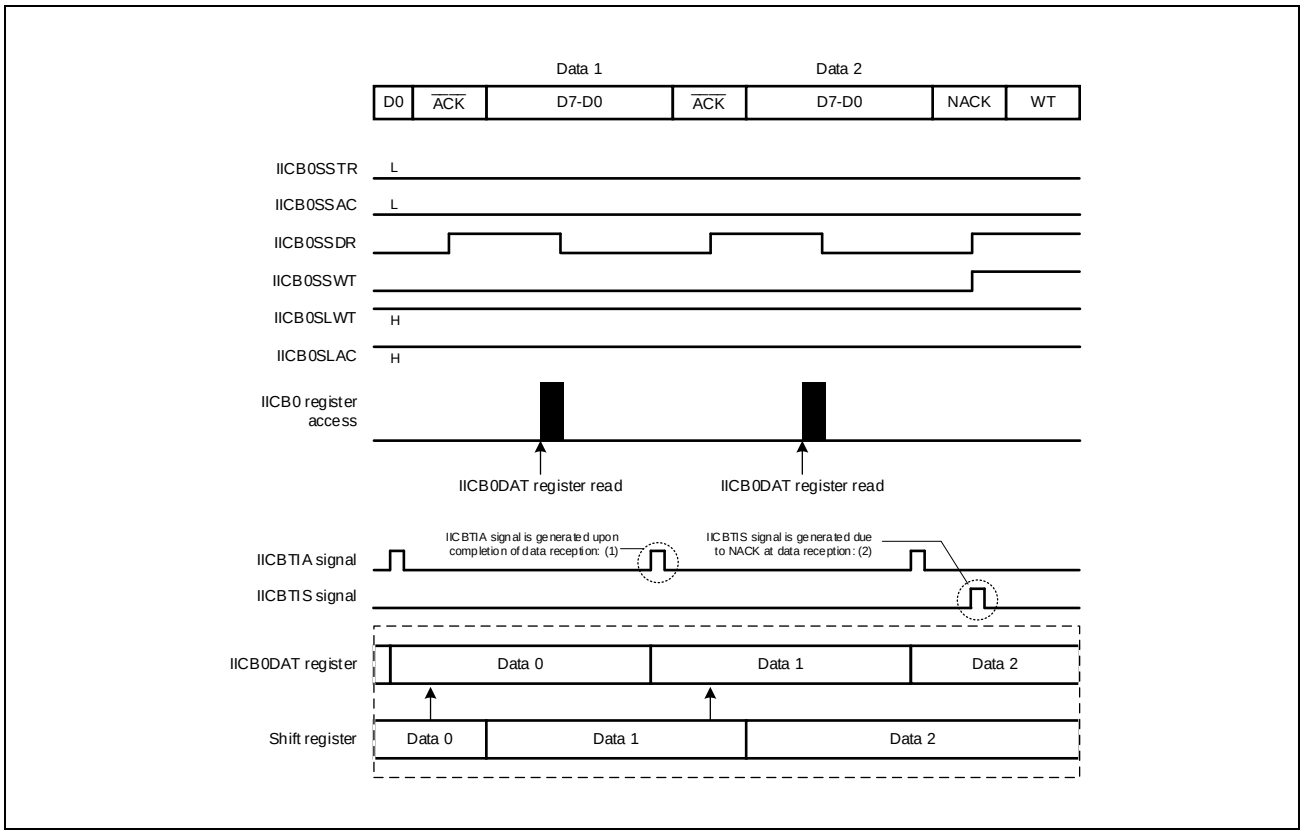


Figure 38.7-1 IICBTIA Signal Generation Timing (Reception, Continuous Transfer Mode)

- Conditions for generating an interrupt request signal during transmission

  When no transmit data is in the shift register and IICB0DAT register, data is written to the IICB0DAT register (**Figure 38.7-2**, timing (2))

  When data is stored from the IICB0DAT register to the shift register (**Figure 38.7-2**, timing (1))

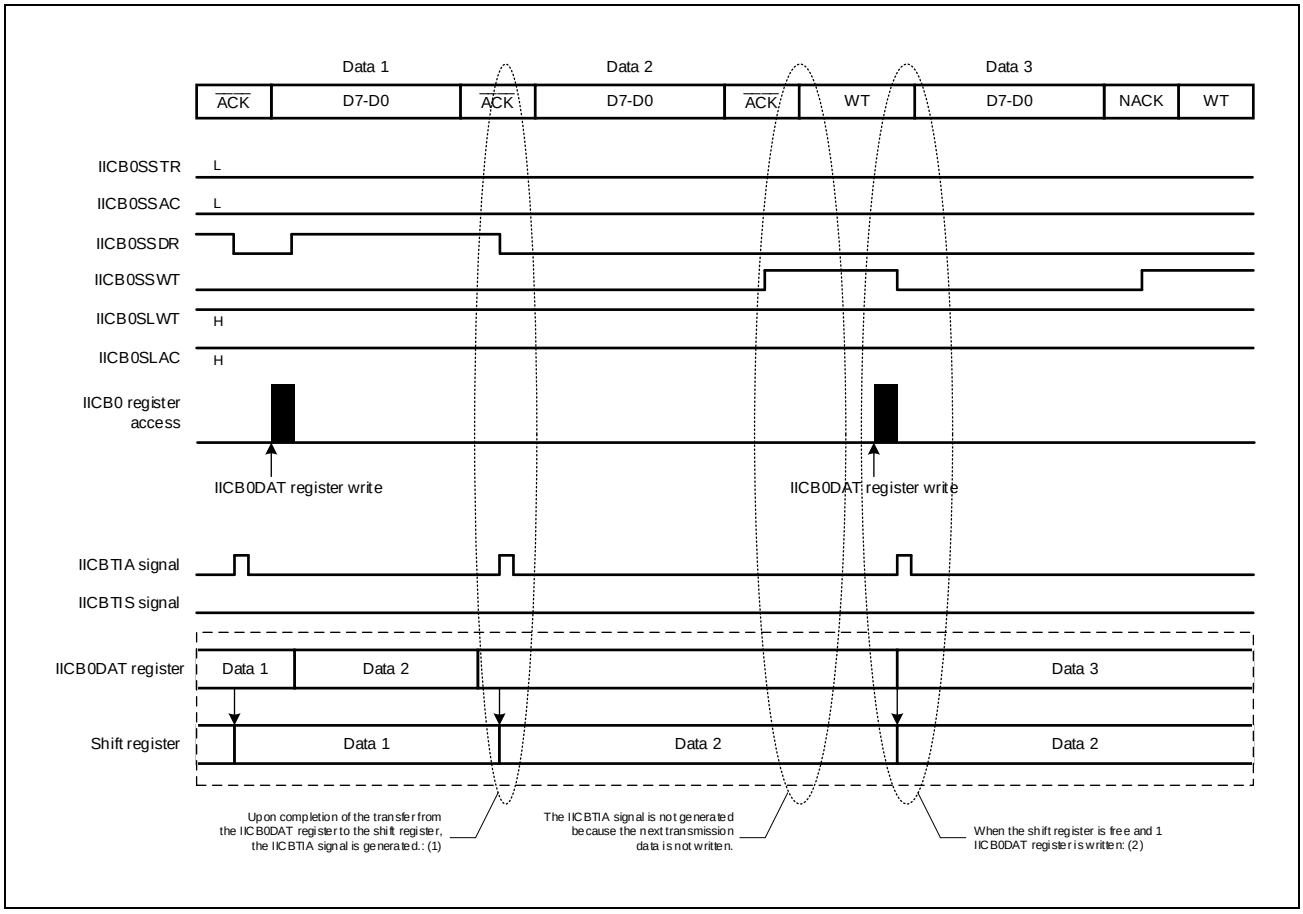
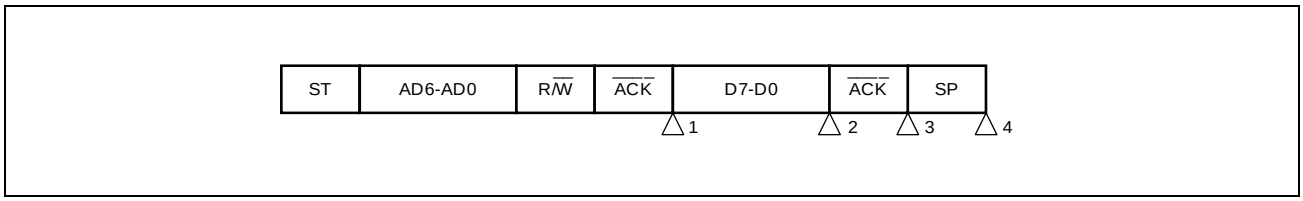


Figure 38.7-2 IICBTIA Signal Generation Timing (Transmission, Continuous Transfer Mode)

(2) Status Interrupt Request Signal (IICBTIS)

The IICBTIS signal generation timing in the continuous transfer mode is the same as that in the single transfer mode.

Table 38.7-4 IICBTIS Signal Generation Timing



Generation Timing	Description	Reference
△1	When the falling edge of the 9th clock of SCLm is detected during address transfer after the start condition	**Section 38.7.1.2(2)(a), IICBTIS Signal Generation Conditions during Address Transfer**
△2	When the falling edge of the 8th clock of SCLm is detected during data transfer	**Section 38.7.1.2(2)(b), IICBTIS Signal Generation Conditions during Data Transfer**
△3	When the falling edge of the 9th clock of SCLm is detected during data transfer	**Section 38.7.1.2(2)(b), IICBTIS Signal Generation Conditions during Data Transfer**
△4	When stop condition is detected	**Section 38.7.1.2(2)(c), IICBTIS Signal Generation when Stop Condition is Detected**

Note: ST: Start condition
AD6-AD0: Address
R/$\overline{W}$: Transfer direction specification
$\overline{ACK}$: Acknowledge
D7-D0: Data
SP: Stop condition

(a) IICBTIS Signal Generation Conditions during Address Transfer

△1 in **Table 38.7-4** is the timing of IICBTIS signal generation during address transfer. **Table 38.7-5** lists the conditions for IICBTIS signal generation at △1.

Table 38.7-5 IICBTIS Signal Generation Condition during Address Transfer (Continuous Transfer Mode)

IICB0 SSMS	IICB0 SSCO	IICB0 ALDF	Transfer Direction	IICB0 SSDR	IICB0 SSAC	△1	
						Interrupt	Wait
1b	×	0b	Transmission	0b	1b	—	Wait
1b	×	0b	Transmission	0b	0b	IICBTIS	Wait
1b	×	0b	Transmission	1b	1b	—	—
1b	×	0b	Transmission	1b	0b	IICBTIS	Wait
1b	×	0b	Reception	0b	1b	—	—
1b	×	0b	Reception	0b	0b	IICBTIS	Wait
1b	×	0b	Reception	1b	1b	IICBTIS when IICB0DAT is read*1	Wait
1b	×	0b	Reception	1b	0b	IICBTIS when IICB0DAT is read	Wait
1b	×	1b	×	×	×	There is no such condition.	
0b	0b	0b	×	×	×	IICBTIS*2	—
0b	0b	1b	×	×	×	IICBTIS	—
0b	1b	×	Transmission	×	1b	IICBTIS	Wait
0b	1b	×	Reception	0b	1b	IICBTIS	—
0b	1b	×	Reception	1b	1b	IICBTIS when IICB0DAT is read	Wait

Note: ×: Don't care

Note: In the case of △1, the value of IICB0STR0.IICB0SSAC bit is always 0b.

Note 1. The operation when restarting without reading after reception is completed

Note 2. The addresses matched before the restart condition

(b) IICBTIS Signal Generation Conditions during Data Transfer

△2 and △3 in **Table 38.7-4** are the IICBTIS signal generation timing during data transfer. **Table 38.7-6** lists the conditions for IICBTIS signal generation at the △2 and △3 timing.

Table 38.7-6 IICBTIS Signal Generation Condition during Data Transfer (Continuous Transfer Mode)

IICB0 SSMS	IICB0 SSCO	IICB0 SLWT	IICB0 ALDF	Transfer Direction	IICB0 SSDR	IICB0 SSAC	IICB0STT or IICB0SPT	△2		△3	
								Interrupt	Wait	Interrupt	Wait
1b	×	0b	×	Transmission	0b	1b	*1	—	—	—	Wait
1b	×	0b	×	Transmission	0b	0b	*1	—	—	IICBTIS	Wait
1b	×	0b	×	Transmission	1b	1b	*1	—	—	—	—
1b	×	0b	×	Transmission	1b	0b	*1	—	—	IICBTIS	Wait
1b	×	0b	×	Reception	0b	1b	*1	—	—	—	—
1b	×	0b	×	Reception	0b	0b	*1	—	—	IICBTIS	Wait
1b	×	0b	×	Reception	1b	1b	*1	—	—	—	—
1b	×	0b	×	Reception	1b	0b	*1	—	—	IICBTIS after IICB0DAT is read	Wait
1b	×	×	×	×	×	0b	*2	—	—	IICBTIS	—
1b	×	×	×	×	×	1b	*2	—	—	—	—
0b	0b	×	0	×	×	×	×	—	—	—	—
0b	0b	0b	1	Reception	×	×	×	IICBTIS	—	—	—
0b	0b	1b	1	Transmission	×	×	×	—	—	IICBTIS	—
0b	1b	0b	×	Transmission	0b	1b	*1	—	—	—	Wait
0b	1b	0b	×	Transmission	0b	0b	*1	—	—	IICBTIS	Wait
0b	1b	0b	×	Transmission	1b	1b	*1	—	—	—	—
0b	1b	0b	×	Transmission	1b	0b	*1	—	—	IICBTIS	Wait
0b	1b	0b	×	Reception	0b	1b	*1	—	—	—	—
0b	1b	0b	×	Reception	0b	0b	*1	—	—	IICBTIS	Wait
0b	1b	0b	×	Reception	1b	1b	*1	—	—	—	—
0b	1b	0b	×	Reception	1b	0b	*1	—	—	IICBTIS after IICB0DAT is read	Wait

Note: ×: Don't care

Note 1. IICB0TRG.IICB0STT bit = 1b or 1b is not written to IICB0TRG.IICB0SPT bit

Note 2. IICB0TRG.IICB0STT bit = 1b or 1b is written to IICB0TRG.IICB0SPT bit

(c) IICBTIS Signal Generation when Stop Condition is Detected

△4 in **Table 38.7-4** is the IICBTIS signal generation timing when a stop condition is detected.

The IICB0CTL0.IICB0SLSI bit setting controls the generation of the IICBTIS signal; when the IICB0CTL0.IICB0SLSI bit is set to 1, the IICBTIS signal is generated when a stop condition is detected.

38.7.2 Interrupt Output and Status

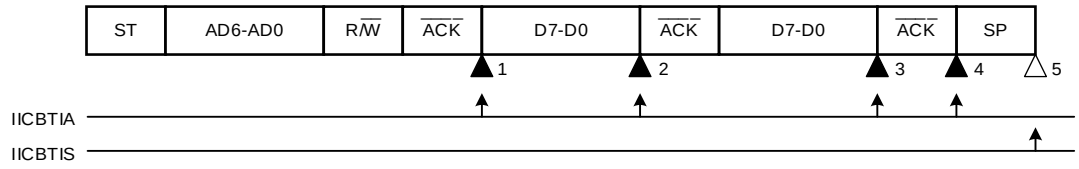
This section describes the states of the IICBnSTR0 register at the time of interrupt output generation by communications flow. The meanings of the symbols which are used in the figures are as follows.

ST:	Start condition
AD6-AD0:	Address
R, $\overline{W}$, R/$\overline{W}$:	Transfer direction specification
$\overline{ACK}$:	Acknowledge
NACK:	Non-acknowledge
D7-D0:	Data
SP:	Stop condition

38.7.2.1 Single Transfer Mode (Master Operation)

(1) Start - Address - Data - Data - Stop (Normal Transmission/Reception)

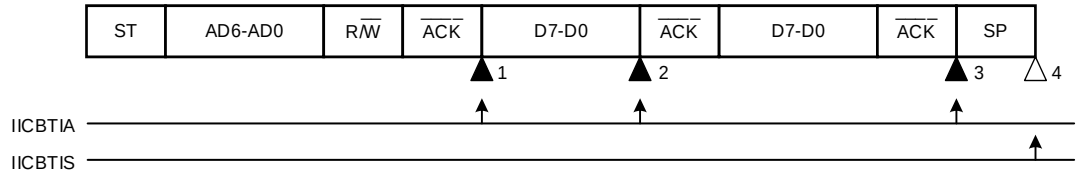
(a) When the IICB0CTL0.IICB0SLWT bit = 0b



▲1: IICB0STR0 register = 1-0100X1 0110--00b
▲2: IICB0STR0 register = 1-0100X0 0100--00b
▲3: IICB0STR0 register = 1-0100X0 0100--00b (IICB0CTL0.IICB0SLWT bit = 1b)
▲4: IICB0STR0 register = 1-0100XX 0100--00b (IICB0TRG.IICB0SPT bit = 1b)
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 0b

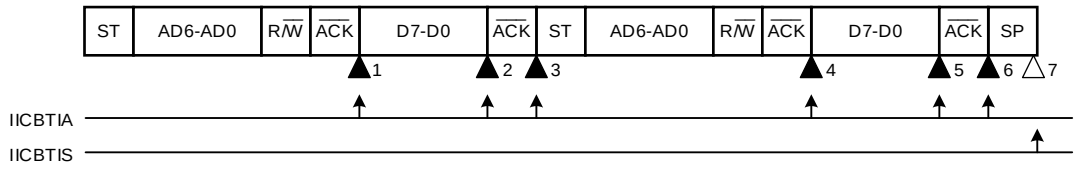


▲1: IICB0STR0 register = 1-0100X1 0110--00b
▲2: IICB0STR0 register = 1-0100X1 0100--00b
▲3: IICB0STR0 register = 1-0100XX 0100--00b (IICB0TRG.IICB0SPT bit = 1b)
△4: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(2) Start - Address - Data - Start - Address - Data - Stop (Restart)

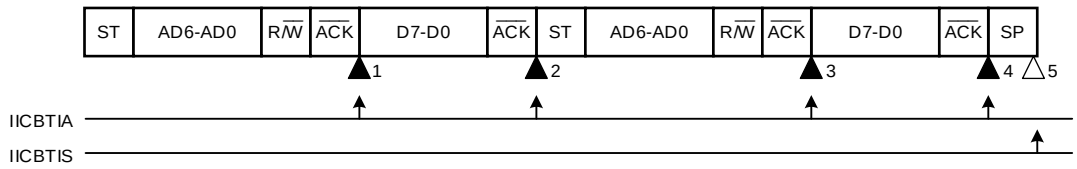
(a) When the IICB0CTL0.IICB0SLWT bit = 0b



▲1: IICB0STR0 register = 1-0100X1 0110--00b
▲2: IICB0STR0 register = 1-0100X0 0100--00b (IICB0CTL0.IICB0SLWT bit =1b)
▲3: IICB0STR0 register = 1-0100XX 0100--00b (IICB0TRG.IICB0STT bit = 1b, IICB0CTL0.IICB0SLWT bit = 0b)
▲4: IICB0STR0 register = 1-0100X1 0110--00b
▲5: IICB0STR0 register = 1-0100X0 0100--00b (IICB0CTL0.IICB0SLWT bit = 1b)
▲6: IICB0STR0 register = 1-0100XX 0100--00b (IICB0TRG.IICB0SPT bit = 1b)
△7: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b

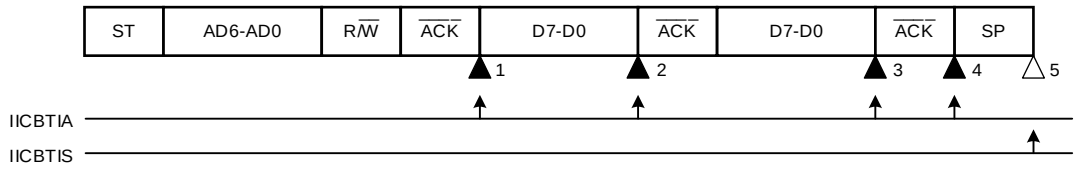


▲1: IICB0STR0 register = 1-0100X1 0110--00b
▲2: IICB0STR0 register = 1-0100XX 0100--00b (IICB0TRG.IICB0STT bit = 1b)
▲3: IICB0STR0 register = 1-0100X1 0110--00b
▲4: IICB0STR0 register = 1-0100XX 0100--00b (IICB0TRG.IICB0SPT bit = 1b)
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(3) Start - Code - Data - Data - Stop (Extension Code Transmission)

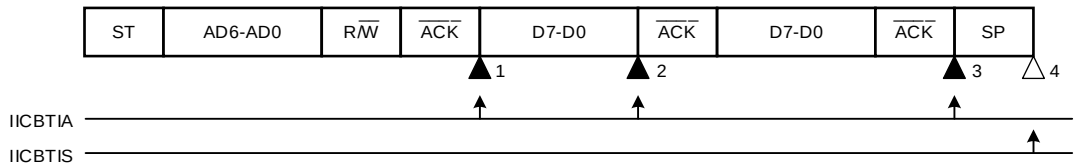
(a) When the IICB0CTL0.IICB0SLWT bit = 0b



▲1: IICB0STR0 register = 1-0110X1 0110--00b
▲2: IICB0STR0 register = 1-0110X0 0100--00b
▲3: IICB0STR0 register = 1-0110X0 0100--00b (IICB0CTL0.IICB0SLWT bit = 1b)
▲4: IICB0STR0 register = 1-0110XX 0100--00b (IICB0TRG.IICB0SPT bit = 1b)
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b



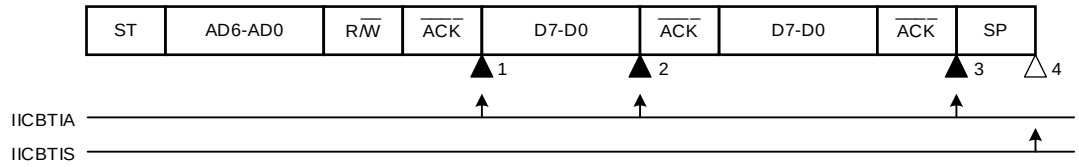
▲1: IICB0STR0 register = 1-0110X1 0110--00b
▲2: IICB0STR0 register = 1-0110X1 0100--00b
▲3: IICB0STR0 register = 1-0110XX 0100--00b (IICB0TRG.IICB0SPT bit = 1b)
△4: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

38.7.2.2 Single Transfer Mode (in Slave Operation: Slave Address Reception)

(1) Start - Address - Data - Data - Stop

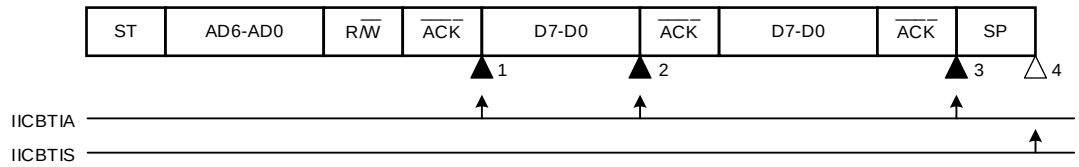
(a) When the IICB0CTL0.IICB0SLWT bit = 0b



▲1: IICB0STR0 register = 0-0101X1 0110--00b
▲2: IICB0STR0 register = 0-0101X0 0100--00b
▲3: IICB0STR0 register = 0-0101X0 0100--00b
△4: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X : Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b

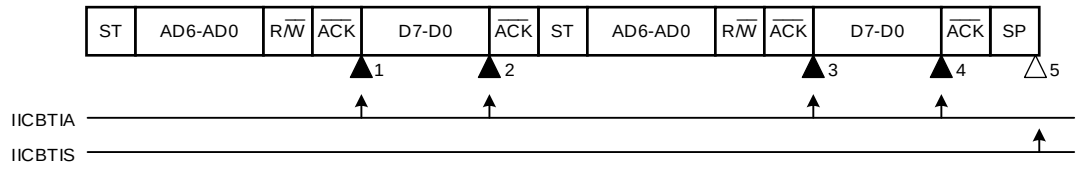


▲1: IICB0STR0 register = 0-0101X1 0110--00b
▲2: IICB0STR0 register = 0-0101X1 0100--00b
▲3: IICB0STR0 register = 0-0101XX 0100--00b
△4: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X : Don't care

(2) Start - Address - Data - Start - Address - Data - Stop

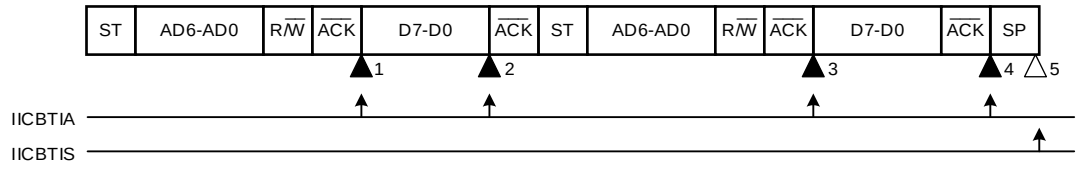
(a) When the IICB0CTL0.IICB0SLWT bit = 0b (Address Match After Restart)



▲1: IICB0STR0 register = 0-0101X1 0110--00b
▲2: IICB0STR0 register = 0-0101X0 0100--00b
▲3: IICB0STR0 register = 0-0101X1 0110--00b
▲4: IICB0STR0 register = 0-0101X0 0100--00b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b (Address Match After Restart)

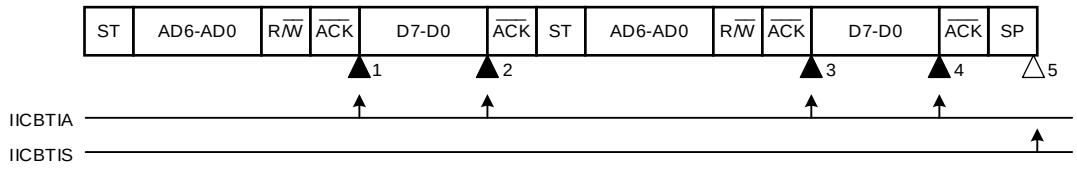


▲1: IICB0STR0 register = 0-0101X1 0110--00b
▲2: IICB0STR0 register = 0-0101XX 0100--00b
▲3: IICB0STR0 register = 0-0101X1 0110--00b
▲4: IICB0STR0 register = 0-0101XX 0100--00b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(3) Start - Address - Data - Start - Code - Data - Stop

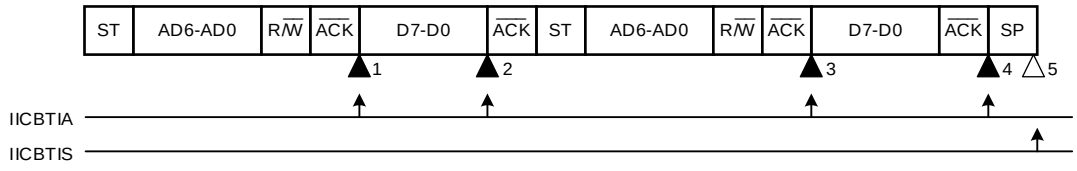
(a) When the IICB0CTL0.IICB0SLWT bit = 0b (Extension Code Reception after Restart)



▲1: IICB0STR0 register = 0-0101X1 0110--00b
▲2: IICB0STR0 register = 0-0101X0 0100--00b
▲3: IICB0STR0 register = 0-0110X1 0110--00b
▲4: IICB0STR0 register = 0-0110X0 0100--00b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b (Extension Code Reception after Restart)

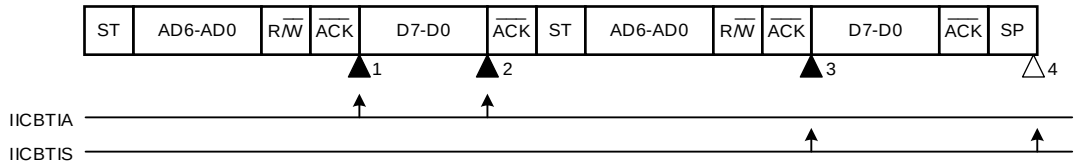


▲1: IICB0STR0 register = 0-0101X1 0110--00b
▲2: IICB0STR0 register = 0-0101XX 0100--00b
▲3: IICB0STR0 register = 0-0110X1 0110--00b
▲4: IICB0STR0 register = 0-0110XX 0100--00b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(4) Start - Address - Data - Start - Address - Data - Stop

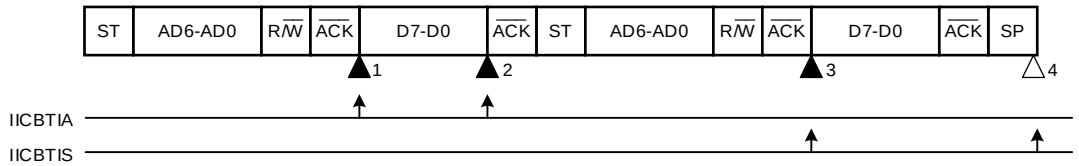
(a) When the IICB0CTL0.IICB0SLWT bit = 0b (Address Mismatch (Extension Code Mismatch) after Restart)



▲1: IICB0STR0 register = 0-0101X1 0110--00b
▲2: IICB0STR0 register = 0-0101X0 0100--00b
▲3: IICB0STR0 register = 0-0000X0 0110--00b
△4: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b (Address Mismatch (Extension Code Mismatch) after Restart)



▲1: IICB0STR0 register = 0-0101X1 0110--00b
▲2: IICB0STR0 register = 0-0101X0 0100--00b
▲3: IICB0STR0 register = 0-0000X0 0110--00b
△4: IICB0STR0 register = 0-000000 0001--00b

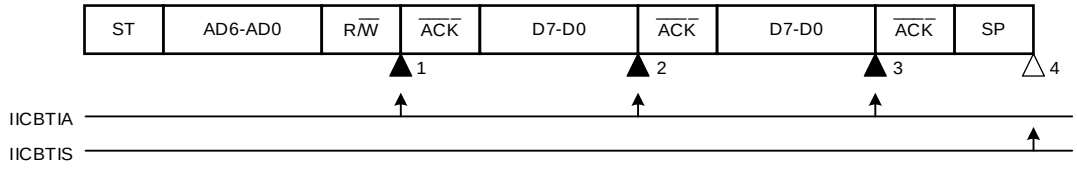
Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

38.7.2.3 Single Transfer Mode (in Slave Operation: Extension Code Reception)

The IIC always participates in communications in reception of the extension code.

(1) Start - Code - Data - Data - Stop

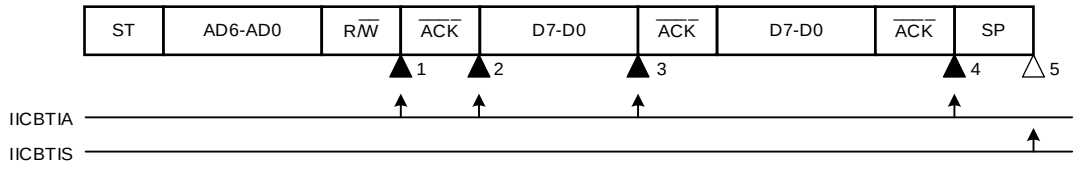
(a) When the IICB0CTL0.IICB0SLWT bit = 0b



▲1: IICB0STR0 register = 0-0110X0 0110--00b
▲2: IICB0STR0 register = 0-0110X0 0100--00b
▲3: IICB0STR0 register = 0-0110X0 0100--00b
△4: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b

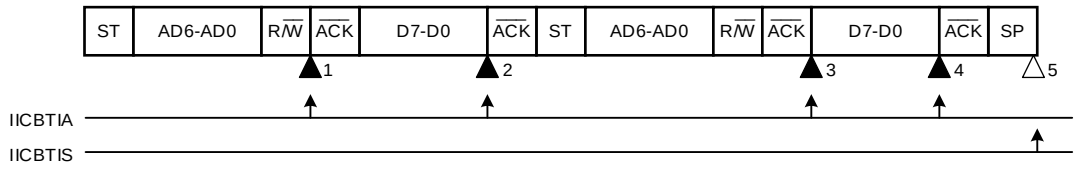


▲1: IICB0STR0 register = 0-0110X0 0110--00b
▲2: IICB0STR0 register = 0-0110X1 0110--00b
▲3: IICB0STR0 register = 0-0110X0 0100--00b
▲4: IICB0STR0 register = 0-0110XX 0100--00b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

(2) Start - Code - Data - Start - Address - Data - Stop

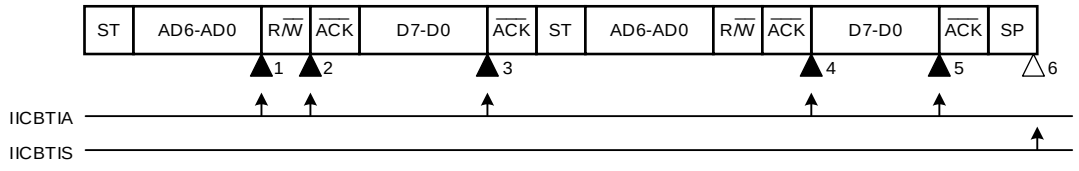
(a) When the IICB0CTL0.IICB0SLWT bit = 0b (Address Match after Restart)



▲1: IICB0STR0 register = 0-0110X0 0110--00b
▲2: IICB0STR0 register = 0-0110X0 0100--00b
▲3: IICB0STR0 register = 0-0101X1 0110--00b
▲4: IICB0STR0 register = 0-0101X0 0100--00b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b (Address Match after Restart)

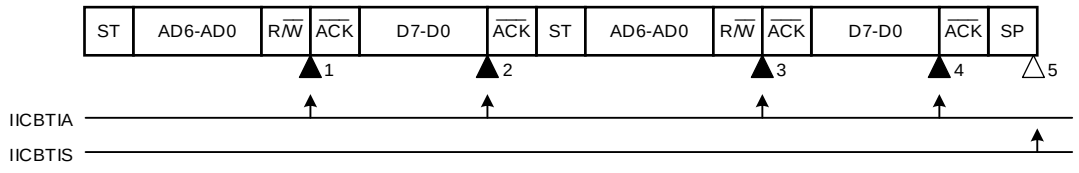


▲1: IICB0STR0 register = 0-0110X0 0110--00b
▲2: IICB0STR0 register = 0-0110X1 0110--00b
▲3: IICB0STR0 register = 0-0110X0 0100--00b
▲4: IICB0STR0 register = 0-0101X1 0110--00b
▲5: IICB0STR0 register = 0-0101XX 0100--00b
△6: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(3) Start - Code - Data - Start - Code - Data - Stop

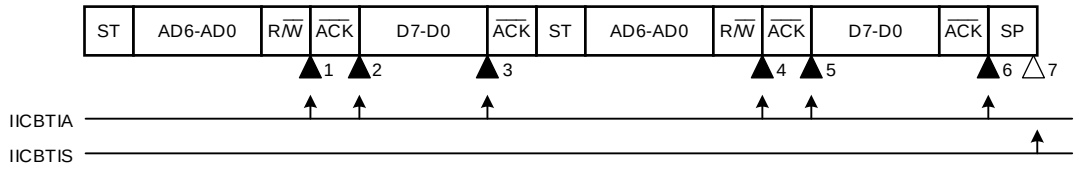
(a) When the IICB0CTL0.IICB0SLWT bit = 0b (Extension Code Reception after Restart)



▲1: IICB0STR0 register = 0-0110X0 0110--00b
▲2: IICB0STR0 register = 0-0110X0 0100--00b
▲3: IICB0STR0 register = 0-0110X0 0110--00b
▲4: IICB0STR0 register = 0-0110X0 0100--00b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b (Extension Code Reception after Restart)

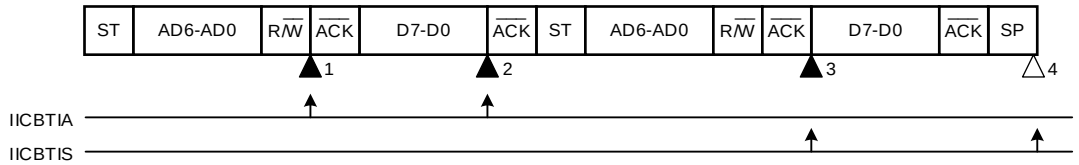


▲1: IICB0STR0 register = 0-0110X0 0110--00b
▲2: IICB0STR0 register = 0-0110X1 0110--00b
▲3: IICB0STR0 register = 0-0110XX 0100--00b
▲4: IICB0STR0 register = 0-0110X0 0110--00b
▲5: IICB0STR0 register = 0-0110X1 0110--00b
▲6: IICB0STR0 register = 0-0110XX 0100--00b
△7: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(4) Start - Code - Data - Start - Address - Data - Stop

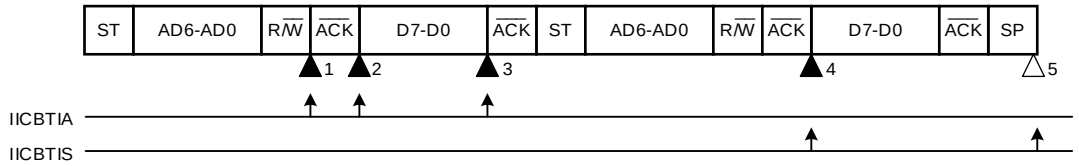
(a) When the IICB0CTL0.IICB0SLWT bit = 0b (Address Mismatch (Extension Code Mismatch) after Restart)



▲1: IICB0STR0 register = 0-0110X0 0110--00b
▲2: IICB0STR0 register = 0-0110X0 0100--00b
▲3: IICB0STR0 register = 0-0000X0 0110--00b
△4: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b (Address Mismatch (Extension Code Mismatch) after Restart)

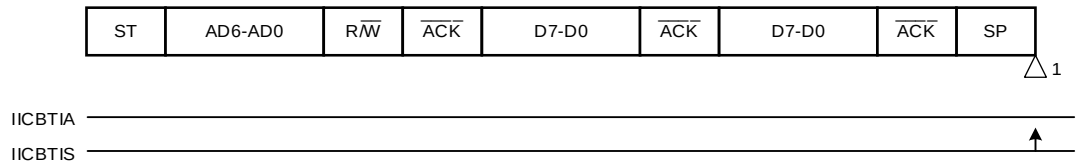


▲1: IICB0STR0 register = 0-0110X0 0110--00b
▲2: IICB0STR0 register = 0-0110X1 0110--00b
▲3: IICB0STR0 register = 0-0000X0 0100--00b
▲4: IICB0STR0 register = 0-0000X0 0110--00b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

38.7.2.4 Single Transfer Mode (Operation in the Case of Non-Participation in Communications)

(1) Start - Code - Data - Data - Stop



△1: IICB0STR0 register = 0-000000 0001--00b

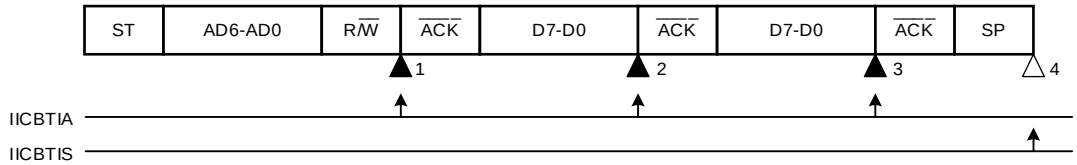
Notes: △: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined

38.7.2.5 Single Transfer Mode (Operation in the Case of Arbitration Loss: Operation as a Slave after Arbitration Loss)

When using the IIC as a master in the multi-master system, read the IICB0STR0.IICB0ALDF bit each time an IICBTIS interrupt is generated to check the result of arbitration.

(1) In the Case of Address Match after a Loss in Arbitration

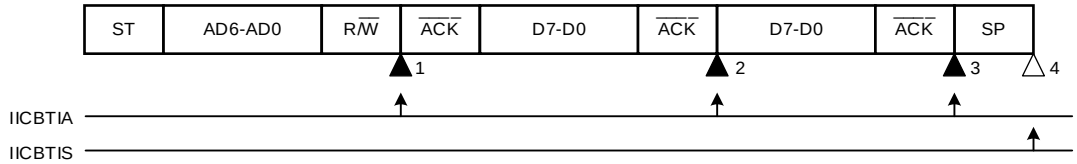
(a) When the IICB0CTL0.IICB0SLWT bit = 0b



▲1: IICB0STR0 register = 0-0101X1 0110--01b (IICB0STRC.IICB0CLAF bit = 1b)
▲2: IICB0STR0 register = 0-0101X0 0100--00b
▲3: IICB0STR0 register = 0-0101X0 0100--00b
△4: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b

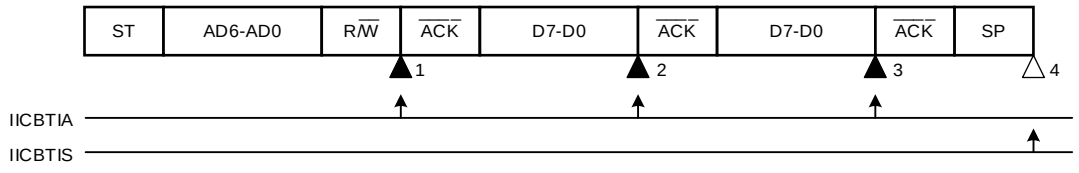


▲1: IICB0STR0 register = 0-0101X1 0110--01b (IICB0STRC.IICB0CLAF bit = 1b)
▲2: IICB0STR0 register = 0-0101X1 0100--00b
▲3: IICB0STR0 register = 0-0101XX 0100--00b
△4: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(2) When the Extension Code is Detected after a Loss in Arbitration

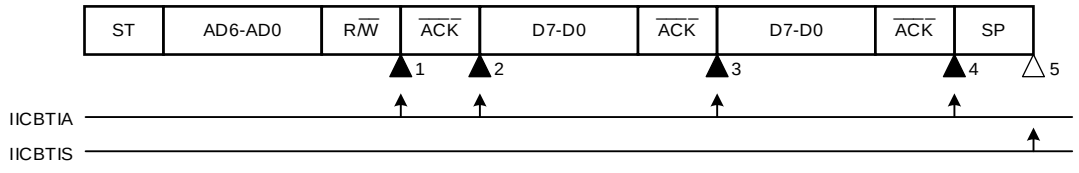
(a) When the IICB0CTL0.IICB0SLWT bit = 0b



▲1: IICB0STR0 register = 0-0110X0 0110--01b (IICB0STRC.IICB0CLAF bit = 1b)
▲2: IICB0STR0 register = 0-0110X0 0100--00b
▲3: IICB0STR0 register = 0-0110X0 0100--00b
△4: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b



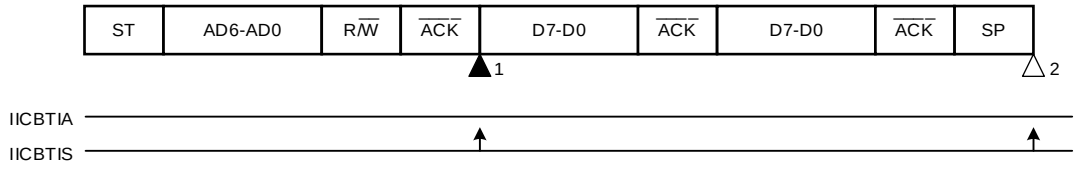
▲1: IICB0STR0 register = 0-0110X0 0110--01b (IICB0STRC.IICB0CLAF bit = 1b)
▲2: IICB0STR0 register = 0-0110X1 0110--00b
▲3: IICB0STR0 register = 0-0110X0 0100--00b
▲4: IICB0STR0 register = 0-0110XX 0100--00b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

38.7.2.6 Single Transfer Mode (Operation in the Case of Arbitration Loss: Non-Participation in Communications after Arbitration Loss)

When using the IIC as a master in the multi-master system, read the IICB0STR0.IICB0ALDF bit each time an IICBTIS interrupt is generated to check the result of arbitration.

(1) In the Case of a Loss in Arbitration during Transmission of Slave Address Data

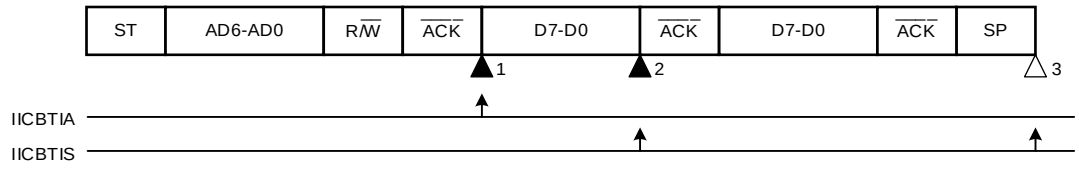


▲1: IICB0STR0 register = 0-0000X1 0110--01b (IICB0STRC.IICB0CLAF bit = 1b)
△2: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(2) In the Case of a Loss in Arbitration during Data Transfer

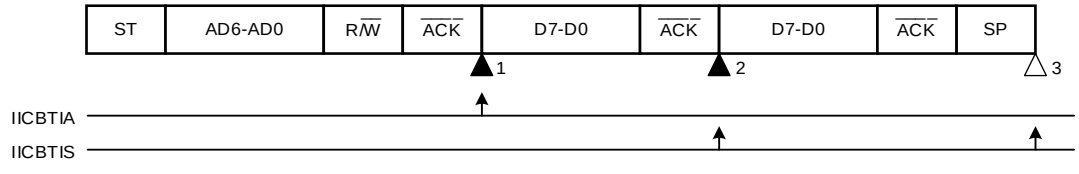
(a) When the IICB0CTL0.IICB0SLWT bit = 0b



▲1: IICB0STR0 register = 1-1000X1 0110--00b
▲2: IICB0STR0 register = 0-0000X0 0100--01b (IICB0STRC.IICB0CLAF bit = 1b)
△3: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b

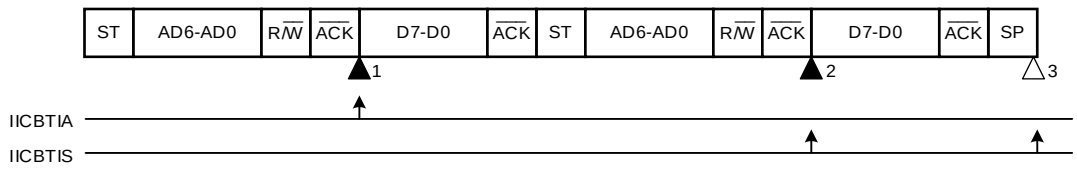


▲1: IICB0STR0 register = 1-1000X1 0110--00b
▲2: IICB0STR0 register = 0-0000X0 0100--01b (IICB0STRC.IICB0CLAF bit = 1b)
△3: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(3) In the Case of a Loss in Arbitration for the Restart Condition during Data Transfer

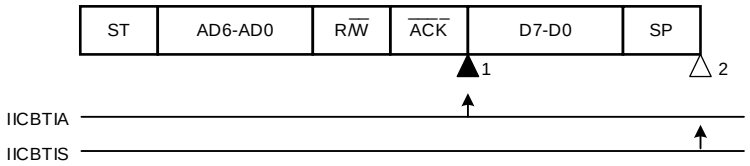
(a) When the IICB0CTL0.IICB0SLWT bit = 1 (Extension Code Mismatch, Address Mismatch)



▲1: IICB0STR0 register = 1-1000X1 0110--00b
▲2: IICB0STR0 register = 0-0000X0 0100--01b（IICB0STRC.IICB0CLAF bit = 1b）
△3: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(4) In the Case of a Loss in Arbitration for the Stop Condition during Data Transfer

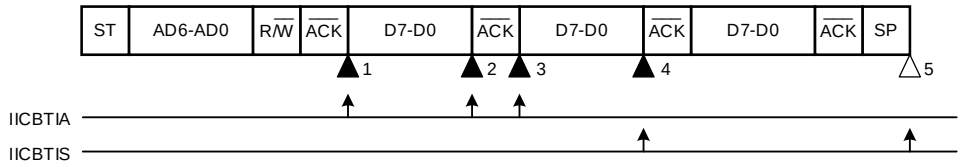


▲1: IICB0STR0 register = 1-1000X1 0110--00b
△2: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Generated regardless of the setting of the IICB0CTL0.IICB0SLSI bit
- : Undefined
X: Don't care

(5) In the Case of a Loss in Arbitration when the SDAm Pin is at the Low Level at the Time of the Attempt to Generate the Restart Condition

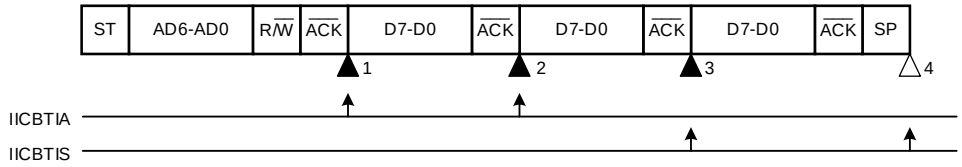
(a) When the IICB0CTL0.IICB0SLWT bit = 0b



▲1: IICB0STR0 register = 1-1000X1 0110--00b
▲2: IICB0STR0 register = 1-1000X0 0100--00b (IICB0CTL0.IICB0SLWT bit = 1b)
▲3: IICB0STR0 register = 1-1000XX 0100--00b (IICB0CTL0.IICB0SLWT bit = 0b, IICB0TRG.IICB0STT bit = 1b)
▲4: IICB0STR0 register = 0-0000X0 0100--01b (IICB0STRC.IICB0CLAF bit = 1b)
△5: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b

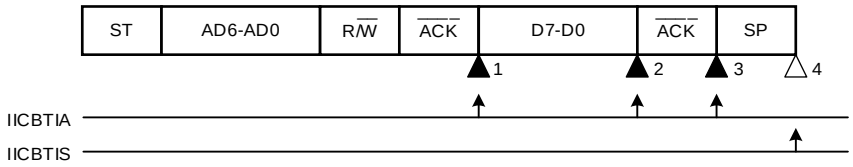


▲1: IICB0STR0 register = 1-1000X1 0110--00b
▲2: IICB0STR0 register = 1-1000XX 0100--00b (IICB0CTL0.IICB0SLWT bit = 0b, IICB0TRG.IICB0STT bit = 1b)
▲3: IICB0STR0 register = 0-0000X0 0100--01b (IICB0STRC.IICB0CLAF bit = 1b)
△4: IICB0STR0 register = 0-000000 0001--00b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

(6) In the Case of a Loss in Arbitration for the Stop Condition at the Time of the Attempt to Generate the Restart Condition

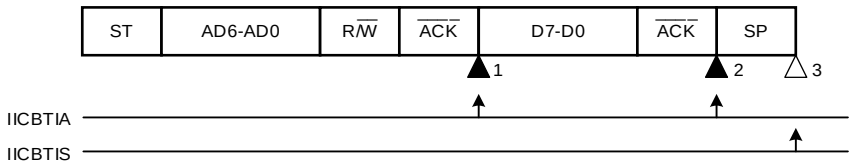
(a) When the IICB0CTL0.IICB0SLWT bit = 0b



▲1: IICB0STR0 register = 1-1000X1 0110--00b
▲2: IICB0STR0 register = 1-1000X0 0100--00b (IICB0CTL0.IICB0SLWT bit = 0b)
▲3: IICB0STR0 register = 1-0000XX 0100--00b (IICB0TRG.IICB0STT bit = 1b)
△4: IICB0STR0 register = 0-000000 0001--01b

Notes: ▲: Always generated
△: Generated regardless of the setting of the IICB0CTL0.IICB0SLSI bit
- : Undefined
X : Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b

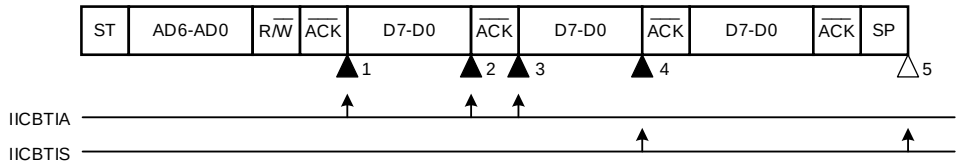


▲1: IICB0STR0 register = 1-1000X1 0110--00b
▲2: IICB0STR0 register = 1-0000XX 0100--00b (IICB0TRG.IICB0STT bit = 1b)
△3: IICB0STR0 register = 0-000000 0001--01b

Notes: ▲: Always generated
△: Generated regardless of the setting of the IICB0CTL0.IICB0SLSI bit
- : Undefined
X : Don't care

(7) In the Case of a Loss in Arbitration when the SDAm Pin is at the Low Level at the Time of the Attempt to Generate the Stop Condition

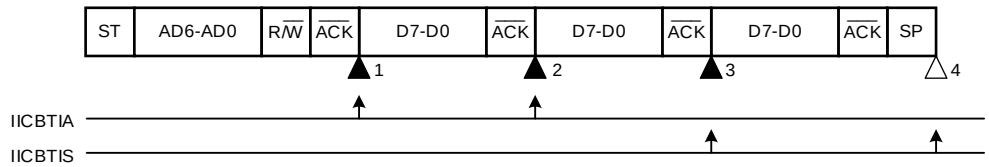
(a) When the IICB0CTL0.IICB0SLWT bit = 0b



▲1: IICB0STR0 register = 1-1000X1 0110--00b
▲2: IICB0STR0 register = 1-1000X0 0100--00b (IICB0CTL0.IICB0SLWT bit = 1b)
▲3: IICB0STR0 register = 1-1000XX 0100--00b (IICB0CTL0.IICB0SLWT bit = 0b, IICB0TRG.IICB0SPT bit = 1b)
▲4: IICB0STR0 register = 0-0000XX 0100--01b (IICB0STRC.IICB0CLAF bit = 1b)
△5: IICB0STR0 register = 0-000000 0001--01b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

(b) When the IICB0CTL0.IICB0SLWT bit = 1b



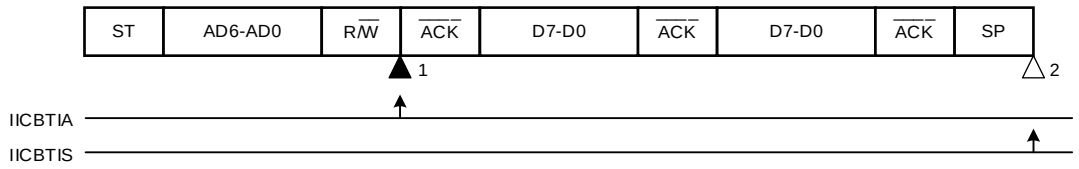
▲1: IICB0STR0 register = 1-1000X1 0110--00b
▲2: IICB0STR0 register = 1-1000XX 0100--00b (IICB0TRG.IICB0SPT bit = 1b)
▲3: IICB0STR0 register = 0-0000XX 0100--01b (IICB0STRC.IICB0CLAF bit = 1b)
△4: IICB0STR0 register = 0-000000 0001--01b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

38.7.2.7 Single Transfer Mode (Operation in the Case of Arbitration Loss: Non-Participation in Communications after Arbitration Loss (during Transfer of the Extension Code))

When using the IIC as a master in the multi-master system, read the IICB0STR0.IICB0ALDF bit each time an IICBTIS interrupt is generated to check the result of arbitration.

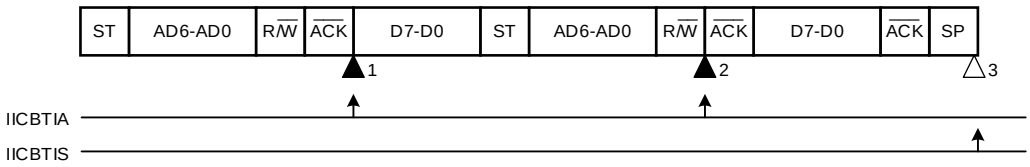
(1) In the Case of a Loss in Arbitration during Transfer of the Extension Code



▲1: IICB0STR0 register = 0-1100X0 0110--01b (IICB0STRC.IICB0CLAF bit = 1b, IICB0TRG.IICB0LRET bit = 1b)
△2: IICB0STR0 register = 0-000000 0001--01b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

(2) In the Case of a Loss in Arbitration for the Restart Condition during Data Transfer (Extension Code Match)



▲1: IICB0STR0 register = 1-1000X1 0110--00b
▲2: IICB0STR0 register = 0-1100X0 0100--01b (IICB0STRC.IICB0CLAF bit = 1b, IICB0TRG.IICB0LRET bit = 1b)
▲3: IICB0STR0 register = 0-000000 0001--01b

Notes: ▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
- : Undefined
X: Don't care

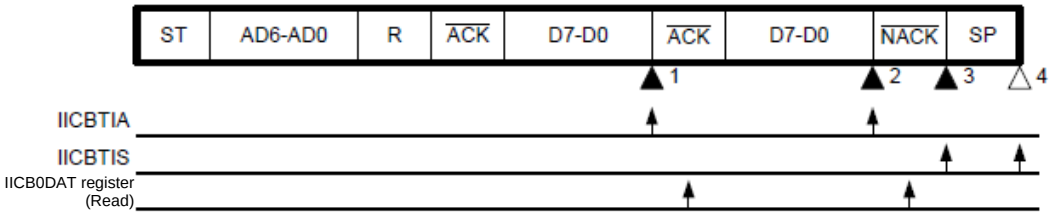
38.7.2.8 Continuous Transfer Mode (Master Operation (Reception))

CAUTION

The interrupts enclosed in brackets [ ] indicate the states at the time of interrupts which do not place the IIC in the wait state. These interrupts are not generated at the time of interrupts in response to the detection of the stop condition.

(1) Start - Address - Data - Data - Stop

(a) When the CB0CTL0.IICB0SLWT bit = 0b

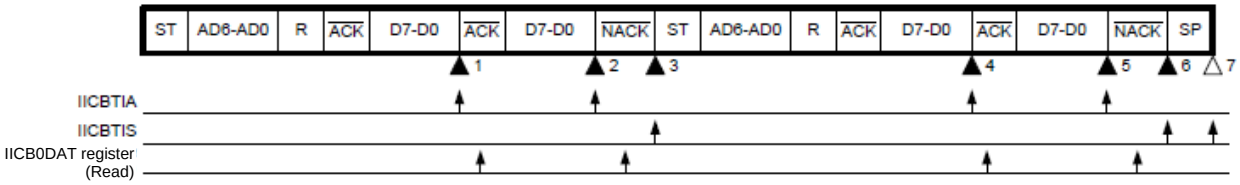


[▲1: IICB0STR0 register = 1-100000 0100--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
[▲2: IICB0STR0 register = 1-100000 0100--00b]
IICB0DAT register read
→ IICB0STR0 register = 1-000000 0100--00b
▲3: IICB0STR0 register = 1-010000 0100--00b
→ IICB0TRG.IICB0SPT bit = 1b
△4: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲:Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(2) Start - Address - Data × 2 - Start - Address - Data × 2 - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 0b

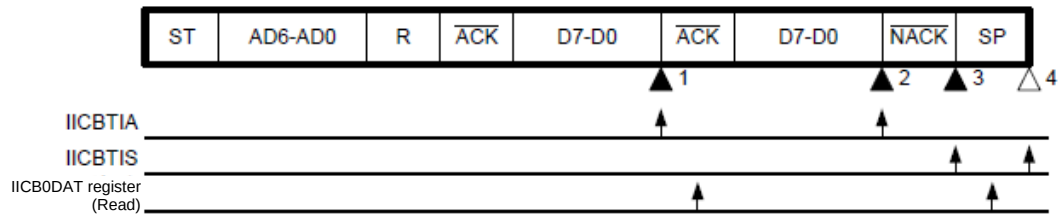


[▲1: IICB0STR0 register = 1-100001 0100--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
[▲2: IICB0STR0 register = 1-100000 0100--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
→ IICB0STR0 register = 1-010000 0100--00b
▲3: IICB0STR0 register = 1-010000 0100--00b
→ IICB0TRG.IICB0STT bit = 1b
[▲4: IICB0STR0 register = 1-100000 0100--00b]
IICB0DAT register read
[▲5: IICB0STR0 register = 1-100000 0100--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
→ IICB0STR0 register = 1-000000 0100--00b
▲6: IICB0STR0 register = 1-010000 0100--00b
→ IICB0TRG.IICB0STT bit = 1b
△7: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(3) Start - Code - Data - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 0b



[▲1: IICB0STR0 register = 1-101001 0100--00b]
IICB0DAT register read
→ IICB0STR0 register = 1-0010001 0100--00b
[▲2: IICB0STR0 register = 1-101000 0100--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
→ IICB0STR0 register = 1-011000 0100--00b
▲3: IICB0STR0 register = 1-01000 0100--00b
→ IICB0TRG.IICB0SPT bit = 1b
△4: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

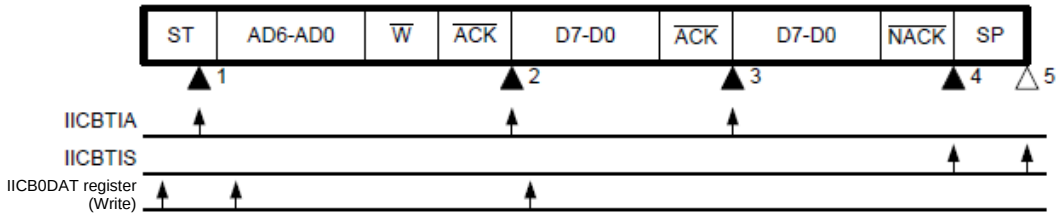
38.7.2.9 Continuous Transfer Mode (Master Operation (Transmission))

CAUTION

The interrupts enclosed in brackets [ ] indicate the states at the time of interrupts which do not place the IIC in the wait state. These interrupts are not generated at the time of interrupts in response to the detection of the stop condition.

(1) Start - Address - Data - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 1b

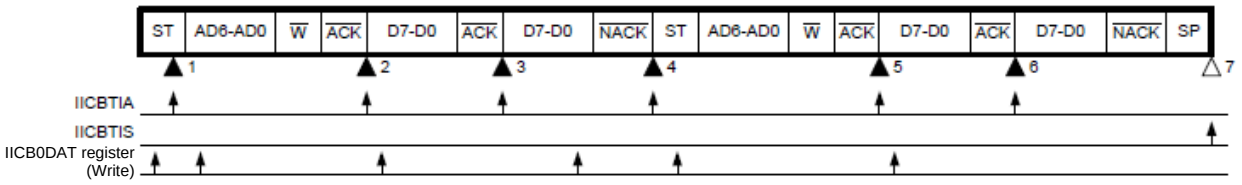


IICB0DAT register write (address)
[▲1: IICB0STR0 register = X-0000X0 0X0X--00b]
IICB0DAT register write
[▲2: IICB0STR0 register = 1-000011 0110--00b]
IICB0DAT register write
[▲3: IICB0STR0 register = 1-000011 0100--00b]
▲4: IICB0STR0 register = 1-010010 0100--00b
IICB0TRG.IICB0SPT bit = 1b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

(2) Start - Address - Data × 2 - Start - Address - Data × 2 - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 1b

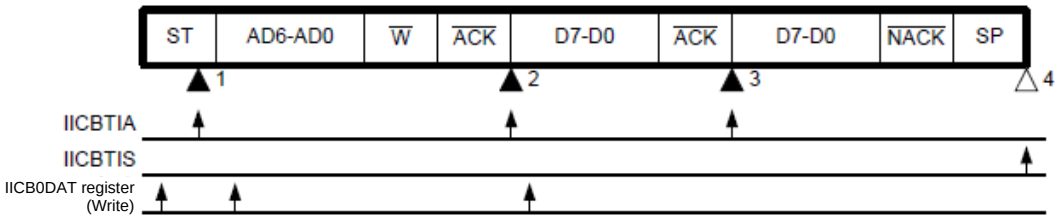


IICB0DAT register write (address)
[▲1: IICB0STR0 register = X-0000X0 0X0X--00b]
IICB0DAT register write
[▲2: IICB0STR0 register = 1-000011 0110--00b]
IICB0DAT register write
[▲3: IICB0STR0 register = 1-000011 0100--00b]
IICB0TRG.IICB0STT bit = 1b
IICB0DAT register write (address)
[▲4: IICB0STR0 register = 1-000010 010X--00b]
IICB0DAT register write
[▲5: IICB0STR0 register = 1-000011 0110--00b]
IICB0DAT register write
[▲6: IICB0STR0 register = 1-000011 0110--00b]
IICB0TRG.IICB0SPT bit = 1b
IICB0DAT register write
△7: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

(3) Start - Code - Data - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 1b



IICB0DAT register write (address)
[▲1: IICB0STR0 register = X-0000X0 0X0X--00b]
IICB0DAT register write
[▲2: IICB0STR0 register = 1-000011 0110--00b]
IICB0DAT register write
[▲3: IICB0STR0 register = 1-000011 0100--00b]
IICB0TRG.IICB0SPT bit = 1b
△4: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

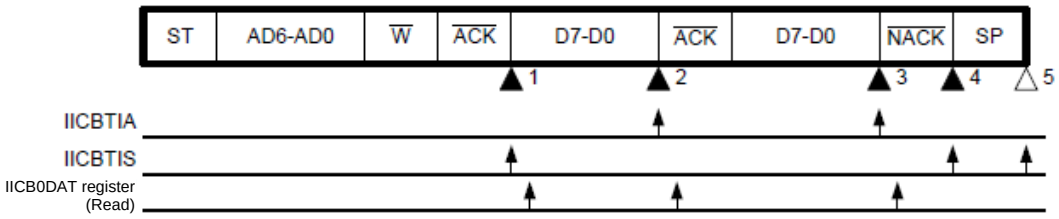
38.7.2.10 Continuous Transfer Mode (in Slave Operation (Reception): Slave Address Reception)

CAUTION

The interrupts enclosed in brackets [ ] indicate the states at the time of interrupts which do not place the IIC in the wait state. These interrupts are not generated at the time of interrupts in response to the detection of the stop condition.

(1) Start - Address - Data - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 0b

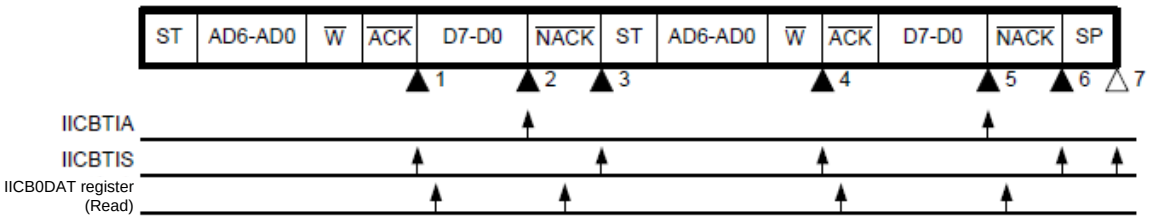


[▲1: IICB0STR0 register = 0-100101 0110--00b]
IICB0DAT register read
[▲2: IICB0STR0 register = 0-100100 0100--00b]
IICB0DAT register read
→ IICB0STR0 register = 0-000100 0100--00b
[▲3: IICB0STR0 register = 0-100100 0100--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
→ IICB0STR0 register = 0-000100 0100-00b
▲4: IICB0STR0 register = 0-010100 0100-00b
IICB0TRG.IICB0WRET bit = 1b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(2) Start - Address - Data - Start - Address - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 0b (Address Match After Restart)

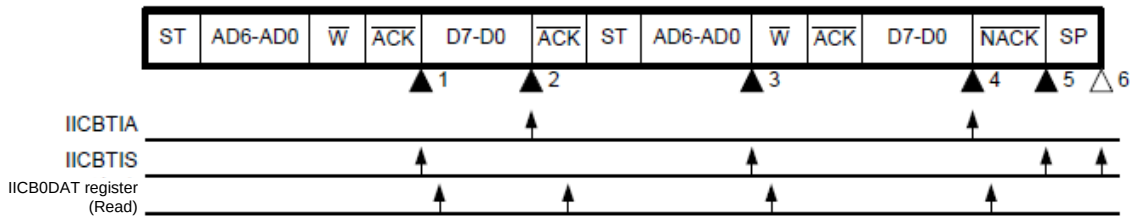


[▲1: IICB0STR0 register = 0-110101 0110--00b]
IICB0DAT register read
[▲2: IICB0STR0 register = 0-100101 0100--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
▲3: IICB0STR0 register = 0-110101 0110--00b
IICB0TRG.IICB0WRET bit = 1b
[▲4: IICB0STR0 register = 0-100100 0110--00B]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
→ IICB0STR0 register = 0-000100 0110--00b
[▲5: IICB0STR0 register = 0-100100 0100--00b]
▲6: IICB0STR0 register = 0-010100 0100--00b
IICB0TRG.IICB0WRET bit = 1b
△7: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(3) Start - Address - Data - Start - Code - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 0b (Extension Code Reception after Restart)

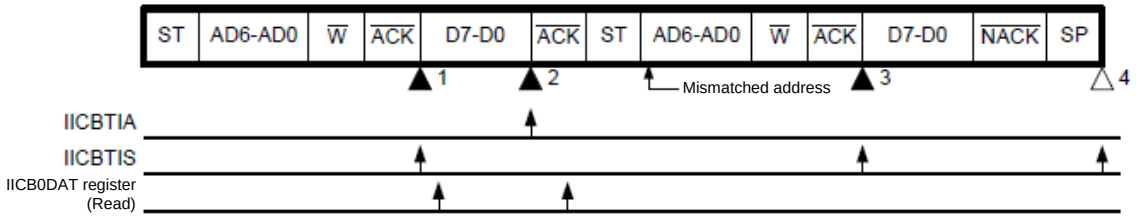


[▲1: IICB0STR0 register = 0-100101 0110--00b]
IICB0DAT register read
[▲2: IICB0STR0 register = 0-100100 0100--00b]
IICB0DAT register read
[▲3: IICB0STR0 register = 0-100100 0110--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
[▲4: IICB0STR0 register = 0-100100 0110--00b]
IICB0DAT register read
▲5: IICB0STR0 register = 0-111000 0100--00b
IICB0TRG.IICB0WRET bit = 1b
△6: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(4) Start - Address - Data - Start - Address - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 0b (Address Mismatch (Extension Code Mismatch) after Restart)



[▲1: IICB0STR0 register = 0-000101 0110--00b]
IICB0DAT register read
[▲2: IICB0STR0 register = 0-100100 0100--00b]
IICB0DAT register read
[▲3: IICB0STR0 register = 0-000000 0110--00b]
△4: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

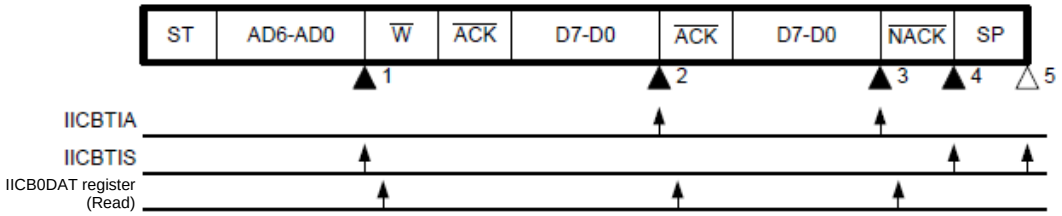
38.7.2.11 Continuous Transfer Mode (in Slave Operation (Reception): Extension Code Reception)

CAUTION

The interrupts enclosed in brackets [ ] indicate the states at the time of interrupts which do not place the IIC in the wait state. These interrupts are not generated at the time of interrupts in response to the detection of the stop condition.

(1) Start - Code - Data - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 0b

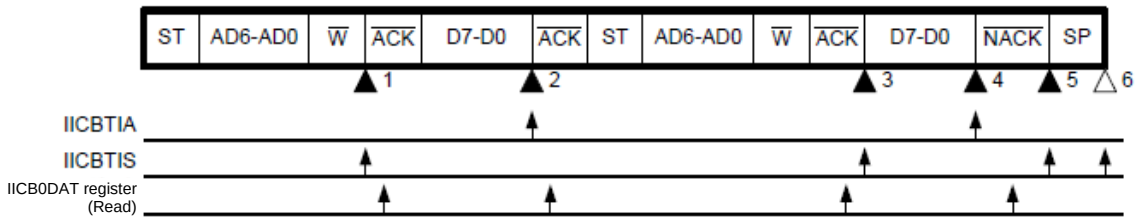


[▲1: IICB0STR0 register = 0-101000 0110--00b]
IICB0DAT register read
[▲2: IICB0STR0 register = 0-101001 0110--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
[▲3: IICB0STR0 register = 0-10001 0100--00b]
IICB0DAT register read
▲4: IICB0STR0 register = 0-111000 0100--00b
IICB0TRG.IICB0WRET bit = 1b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(2) Start - Code - Data - Start - Address - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 0b (Address Match after Restart)

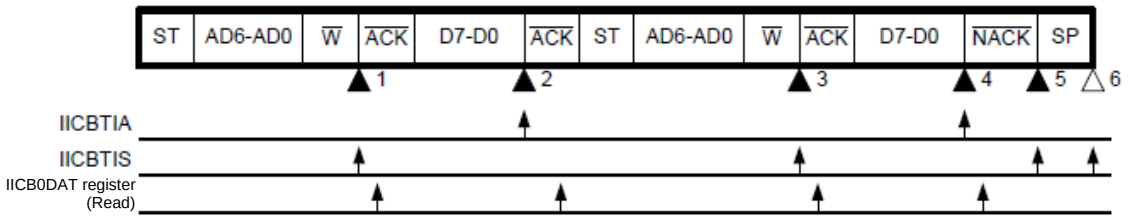


[▲1: IICB0STR0 register = 0-101000 0110--00b]
IICB0DAT register read
[▲2: IICB0STR0 register = 0-011000 0110--00b]
IICB0DAT register read
[▲3: IICB0STR0 register = 0-111001 0100--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
[▲4: IICB0STR0 register = 0-010100 0110--00b]
IICB0DAT register read
▲5: IICB0STR0 register = 0-110100 0100--00b
IICB0TRG.IICB0WRET bit = 1b
△6: IICB0STR0 register = 0-000000 0001--00b

Note:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(3) Start - Code - Data - Start - Code - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 0b (Extension Code Reception after Restart)

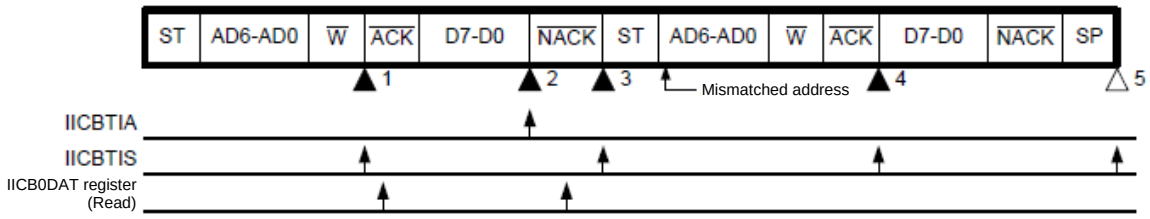


[▲1: IICB0STR0 register = 0-101000 0110--00b]
IICB0DAT register read
[▲2: IICB0STR0 register = 0-011001 0110--00b]
IICB0DAT register read
[▲3: IICB0STR0 register = 0-101000 0110--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
[▲4: IICB0STR0 register = 0-101001 0110--00b]
IICB0DAT register read
▲5: IICB0STR0 register = 0-011000 0100--00b
IICB0TRG.IICB0WRET bit = 1b
△6: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(4) Start - Code - Data - Start - Address - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 0 (Address Mismatch (Extension Code Mismatch) after Restart)



[▲1: IICB0STR0 register = 0-101000 0110--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
[▲2: IICB0STR0 register = 0-101001 0110--00b]
IICB0CTL0.IICB0SLAC bit = 0b
▲3: IICB0STR0 register = 0-010000 0100--00b
IICB0TRG.IICB0WRET bit = 1b
[▲4: IICB0STR0 register = 0-000000 0110--00b]
△5: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

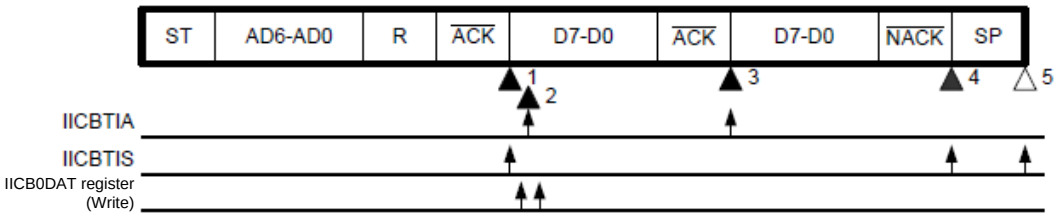
38.7.2.12 Continuous Transfer Mode (in Slave Operation (Transmission): Slave Address Reception)

CAUTION

The interrupts enclosed in brackets [ ] indicate the states at the time of interrupts which do not place the IIC in the wait state. These interrupts are not generated at the time of interrupts in response to the detection of the stop condition.

(1) Start - Address - Data - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 1b

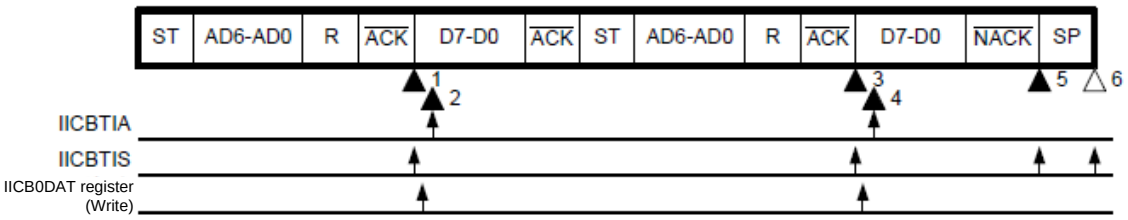


▲1: IICB0STR0 register = 0-110111 0110--00b
IICB0DAT register write
[▲2: IICB0STR0 register = 0-00011X 0100--00b]
IICB0DAT register write
→ IICB0STR0 register = 0-100011X 0100--00b
▲3: IICB0STR0 register = 0-000111 0100--00b
▲4: IICB0STR0 register = 0-010110 0100--00b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

(2) Start - Address - Data - Start - Address - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 1b (Address Match after Restart)

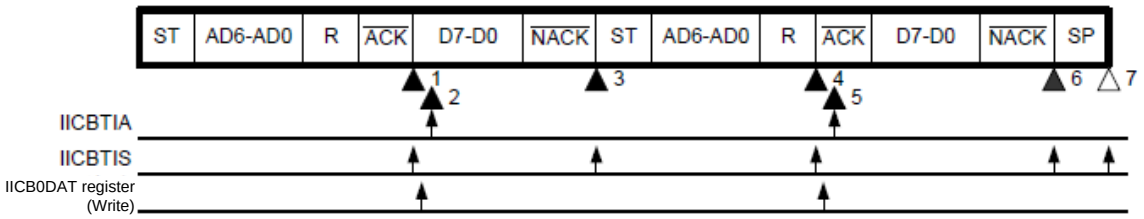


▲1: IICB0STR0 register = 0-010111 0110--00b
IICB0DAT register write
[▲2: IICB0STR0 register = 0-00111X 01X0--00b]
▲3: IICB0STR0 register = 0-010111 0110--00b
IICB0DAT register write
[▲4: IICB0STR0 register = 0-100101 01X0--00b]
▲5: IICB0STR0 register = 0-110100 0100--00b
△6: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

(3) Start - Address - Data - Start - Code - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 1b (Extension Code Reception after Restart)



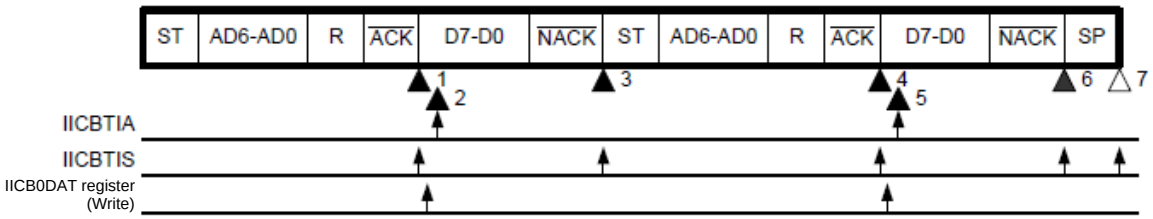
▲1: IICB0STR0 register = 0-110111 0110--00b
IICB0DAT register write
[▲2: IICB0STR0 register = 0-100111 0100--00b]
▲3: IICB0STR0 register = 0-111010 0110--00b
▲4: IICB0STR0 register = 0-111010 0110--00b
IICB0DAT register write
[▲5: IICB0STR0 register = 0-111011 0110--00b]
▲6: IICB0STR0 register = 0-111010 0100--00b
△7: IICB0STR0 register = 0-000000 0001--00b

Notes:

▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(4) Start - Address - Data - Start - Address - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 1 (Address Mismatch (Extension Code Mismatch) after Restart)



▲1: IICB0STR0 register = 0-110111 0110--00b
IICB0DAT register write
[▲2: IICB0STR0 register = 0-100111 0100--00b]
▲3: IICB0STR0 register = 0-000010 0100--00b
▲4: IICB0STR0 register = 0-000011 0110--00b
IICB0DAT register write
[▲5: IICB0STR0 register = 0-00001X 0100--00b]
▲6: IICB0STR0 register = 0-000010 0100--00b
△7: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

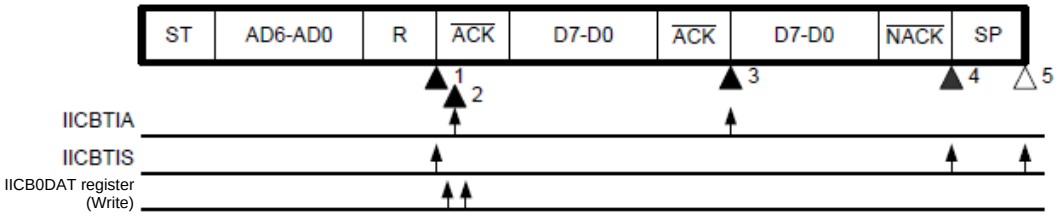
38.7.2.13 Continuous Transfer Mode (in Slave Operation (Transmission): Extension Code Reception)

CAUTION

The interrupts enclosed in brackets [ ] indicate the states at the time of interrupts which do not place the IIC in the wait state. These interrupts are not generated at the time of interrupts in response to the detection of the stop condition.

(1) Start - Code - Data - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 1b

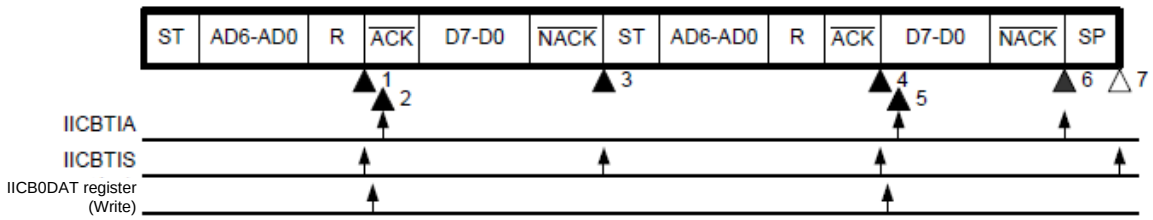


▲1: IICB0STR0 register = 0-011010 0110--00b
IICB0DAT register write
[▲2: IICB0STR0 register = 0-011011 0110--00b]
IICB0DAT register write
[▲3: IICB0STR0 register = 0-011011 0100--00b]
▲4: IICB0STR0 register = 0-111010 0100--00b
△5: IICB0STR0 register = 0-000010 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(2) Start - Code - Data - Start - Address - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 1b (Address Match after Restart)



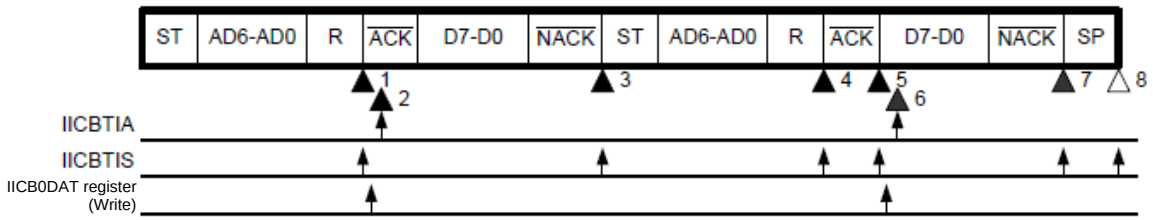
▲1: IICB0STR0 register = 0-011000 0110--00b
IICB0DAT register write
[▲2: IICB0STR0 register = 0-011001 0110--00b]
▲3: IICB0STR0 register = 0-011000 0100--00b
▲4: IICB0STR0 register = 0-010101 0110--00b
IICB0DAT register write
[▲5: IICB0STR0 register = 0-010101 0110--00b]
▲6: IICB0STR0 register = 0-010100 0100--00b
△7: IICB0STR0 register = 0-000000 0001--00b

Notes:

▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(3) Start - Code - Data - Start - Code - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 1b (Extension Code Reception after Restart)

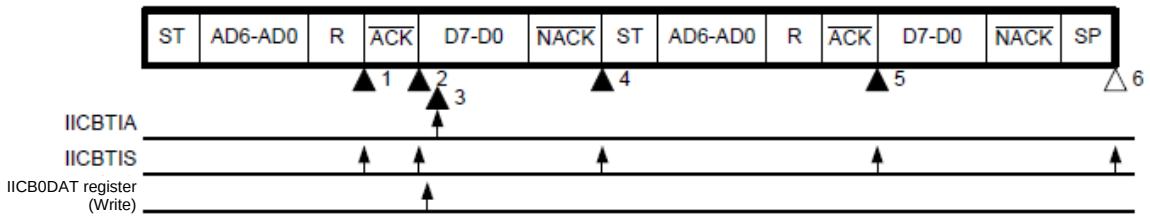


▲1: IICB0STR0 register = 0-011000 0110--00b
IICB0DAT register write
[▲2: IICB0STR0 register = 0-011001 0110--00b]
▲3: IICB0STR0 register = 0-011000 0100--00b
▲4: IICB0STR0 register = 0-011000 0110--00b
▲5: IICB0STR0 register = 0-011001 0110--00b
IICB0DAT register write
[▲6: IICB0STR0 register = 0-011001 0110--00b]
▲7: IICB0STR0 register = 0-011000 0100--00b
△8: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(4) Start - Code - Data - Start - Address - Data - Stop

(a) When the IICB0CTL0.IICB0SLWT bit = 1b (Address Match (Extension Code Mismatch) after Restart)

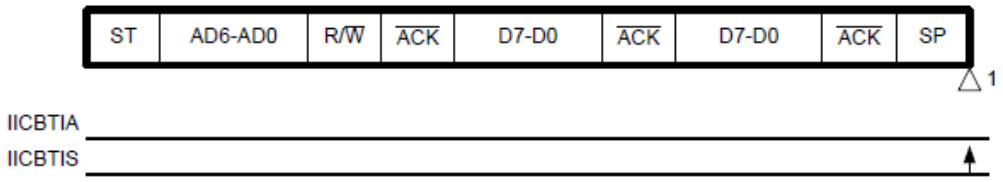


▲1: IICB0STR0 register = 0-011000 0110--00b
▲2: IICB0STR0 register = 0-011001 0110--00b
IICB0DAT register write
[▲3: IICB0STR0 register = 0-011010 0100--00b]
▲4: IICB0STR0 register = 0-000000 0100--00b
▲5: IICB0STR0 register = 0-000000 0110--00b
△6: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

38.7.2.14 Continuous Transfer Mode (Operation in the Case of Non-Participation in Communications)

(1) Start - Code - Data - Data - Stop



△1: IICB0STR0 register = 0-0000X0 0001--00b

Notes:

△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b

-: Undefined

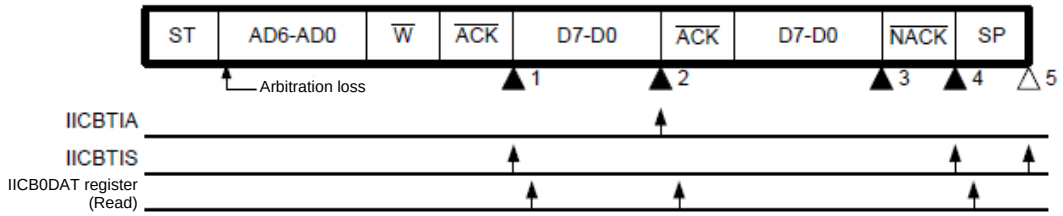
X:Don't care

38.7.2.15 Continuous Transfer Mode (Operation in the Case of Arbitration Loss (when the Address is Transferred in Reception): Operation as a Slave after Arbitration Loss)

When using the IIC as a master in the multi-master system, read the IICB0STR0.IICB0ALDF bit each time an IICBTIS interrupt is generated to check the result of arbitration.

(1) In the Case of Address Match after a Loss in Arbitration

(a) When the IICB0CTL0.IICB0SLWT bit = 0b in Reception

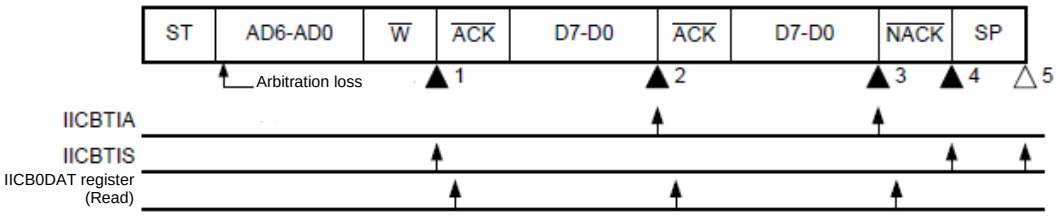


[▲1: IICB0STR0 register = 0-100101 0110--01b]
IICB0STRC.IICB0CLAF bit = 1b
IICB0DAT register read
[▲2: IICB0STR0 register = 0-100101 0100--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
[▲3: IICB0STR0 register = 0-100100 0100--00b]
IICB0DAT register read
▲4: IICB0STR0 register = 0-010100 0100--00b
IICB0TRG.IICB0WRET bit = 1b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(2) When the Extension Code is Detected after a Loss in Arbitration

(a) When the IICB0CTL0.IICB0SLWT bit = 0b in Reception



[▲1: IICB0STR0 register = 0-101000 0110--01b]
IICB0STRC.IICB0CLAF bit = 1
IICB0DAT register read
[▲2: IICB0STR0 register = 0-101000 0110--00b]
IICB0CTL0.IICB0SLAC bit = 0b
IICB0DAT register read
[▲3: IICB0STR0 register = 0-101000 0100--00b]
IICB0DAT register read
▲4: IICB0STR0 register = 0-011000 0100--00b]
IICB0TRG.IICB0WRET bit = 1b
△5: IICB0STR0 register = 0-000000 0001--00b

Notes:

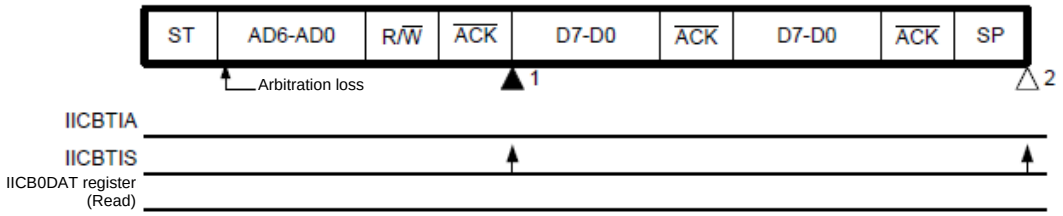
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

38.7.2.16 Continuous Transfer Mode (Operation in the Case of Arbitration Loss (when the Address is Transferred in Reception): Non-Participation in Communications after Arbitration Loss)

When using the IIC as a master in the multi-master system, read the IICB0STR0.IICB0ALDF bit each time an IICBTIS interrupt is generated to check the result of arbitration.

(1) In the Case of a Loss in Arbitration during Transmission of Slave Address Data

(a) When the IICB0CTL0.IICB0SLWT bit = 0b in Reception

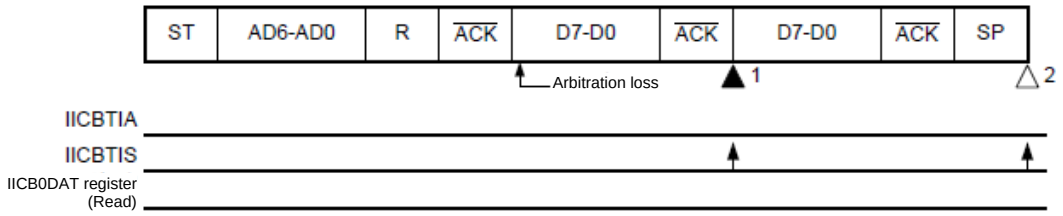


▲1: IICB0STR0 register = 0-000001 0110--01b (IICB0STRC.IICB0CLAF bit = 1b)
△2: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(2) In the Case of a Loss in Arbitration during Data Transfer

(a) When the IICB0CTL0.IICB0SLWT bit = 1b in Reception

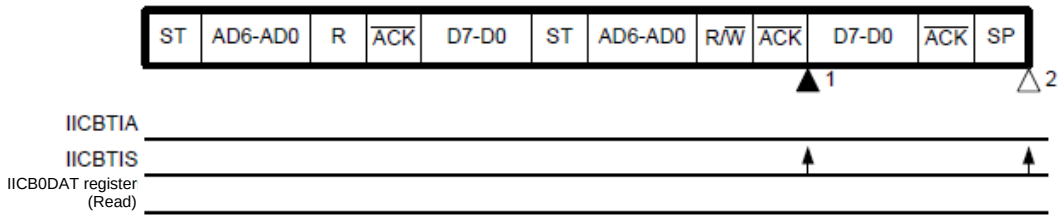


[▲1: IICB0STR0 register = 0-000000 0100--01b]
IICB0STRC.IICB0CLAF bit = 1b
△2: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(3) In the Case of a Loss in Arbitration for the Restart Condition during Data Transfer

(a) When the IICB0CTL0.IICB0SLWT bit = 1b in Reception (Extension Code Mismatch, Address Mismatch)

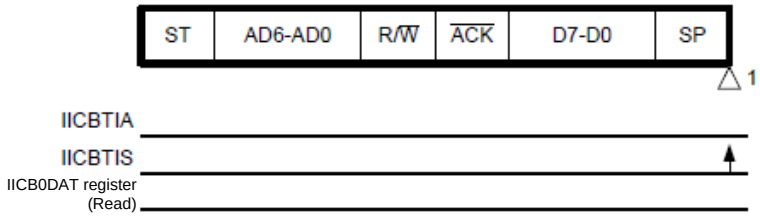


[▲1: IICB0STR0 register = 0-000001 0100--01b]
IICB0STRC.IICB0CLAF bit = 1b
△2: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(4) In the Case of a Loss in Arbitration for the Stop Condition during Data Transfer

(a) When the IICB0CTL0.IICB0SLWT bit = 1b in Reception

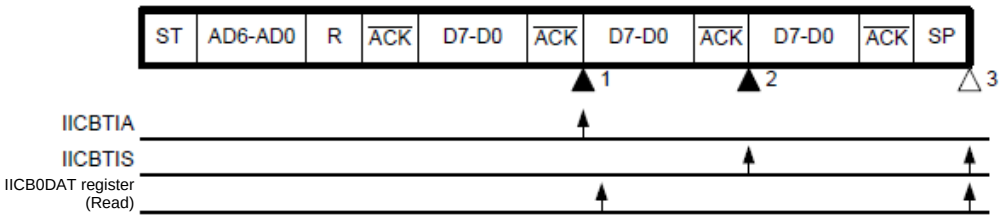


△1: IICB0STR0 register = 0-000000 0001--01b
IICB0STRC.IICB0CLAF bit = 1b

Notes:
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(5) In the Case of a Loss in Arbitration when the SDAm Pin is at the Low Level at the Time of the Attempt to Generate the Restart Condition

(a) When the IICB0CTL0.IICB0SLWT bit = 1b

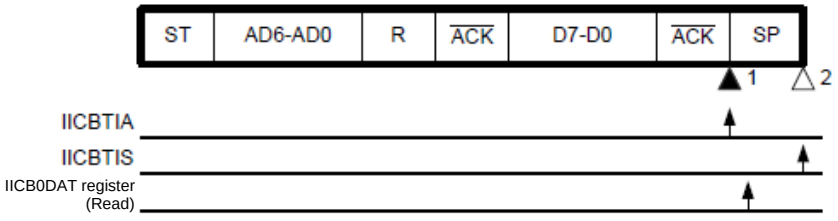


[▲1: IICB0STR0 register = 1-1000XX 0100--00b]
IICB0DAT register read
IICB0TRG.IICB0STT bit = 1b
▲2: IICB0STR0 register = 0-000000 0100--01b
IICB0STRC.IICB0CLAF bit = 1b
△3: IICB0STR0 register = 0-000000 0001--00b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

(6) In the Case of a Loss in Arbitration for the Stop Condition at the Time of the Attempt to Generate the Restart Condition

(a) When the IICB0CTL0.IICB0SLWT bit = 1b

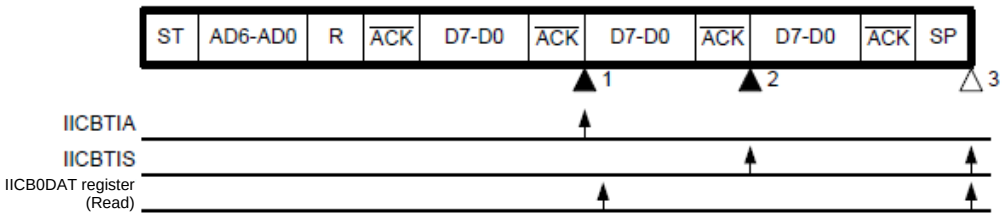


[▲1: IICB0STR0 register = 1-000001 0100--00b]
IICB0DAT register read
IICB0TRG.IICB0STT bit = 1b
△2: IICB0STR0 register = 0-000000 0001--01b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined

(7) In the Case of a Loss in Arbitration when the SDAm Pin is at the Low Level at the Time of the Attempt to Generate the Stop Condition

(a) When the IICB0CTL0.IICB0SLWT bit = 1b



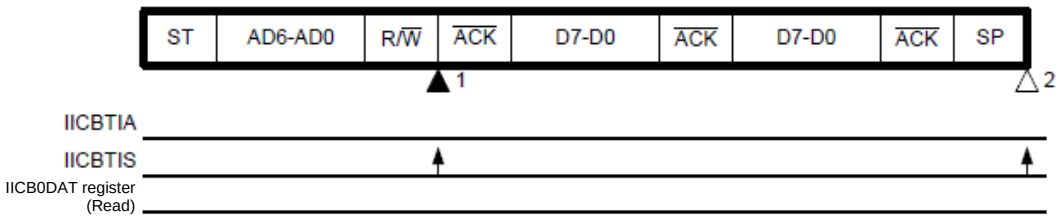
[▲1: IICB0STR0 register = 1-1000XX 0100--00b]
IICB0DAT register read
IICB0TRG.IICB0SPT bit = 1b
[▲2: IICB0STR0 register = 0-0000XX 0100--01b (IICB0STRC.IICB0CLAF bit = 1b)
△3: IICB0STR0 register = 0-000000 0001--01b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

38.7.2.17 Continuous Transfer Mode (Operation in the Case of Arbitration Loss (when the Address is Transferred in Reception): Non-Participation in Communications after Arbitration Loss (during Transfer of the Extension Code))

When using the IIC as a master in the multi-master system, read the IICB0STR0.IICB0ALDF bit each time an IICBTIS interrupt is generated to check the result of arbitration.

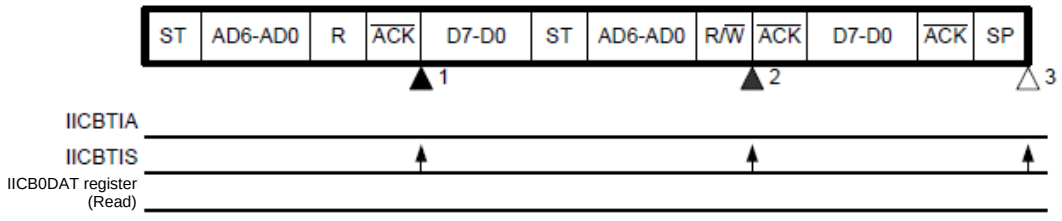
(1) In the Case of a Loss in Arbitration during Transfer of the Extension Code



[▲1: IICB0STR0 register = 0-1000X0 0110--01b]
IICB0STRC.IICB0CLAF bit = 1b
IICB0TRG.IICB0LRET bit = 1b
△2: IICB0STR0 register = 0-000000 0001--01b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

(2) In the Case of a Loss in Arbitration during Data Transfer (Extension Code Match)



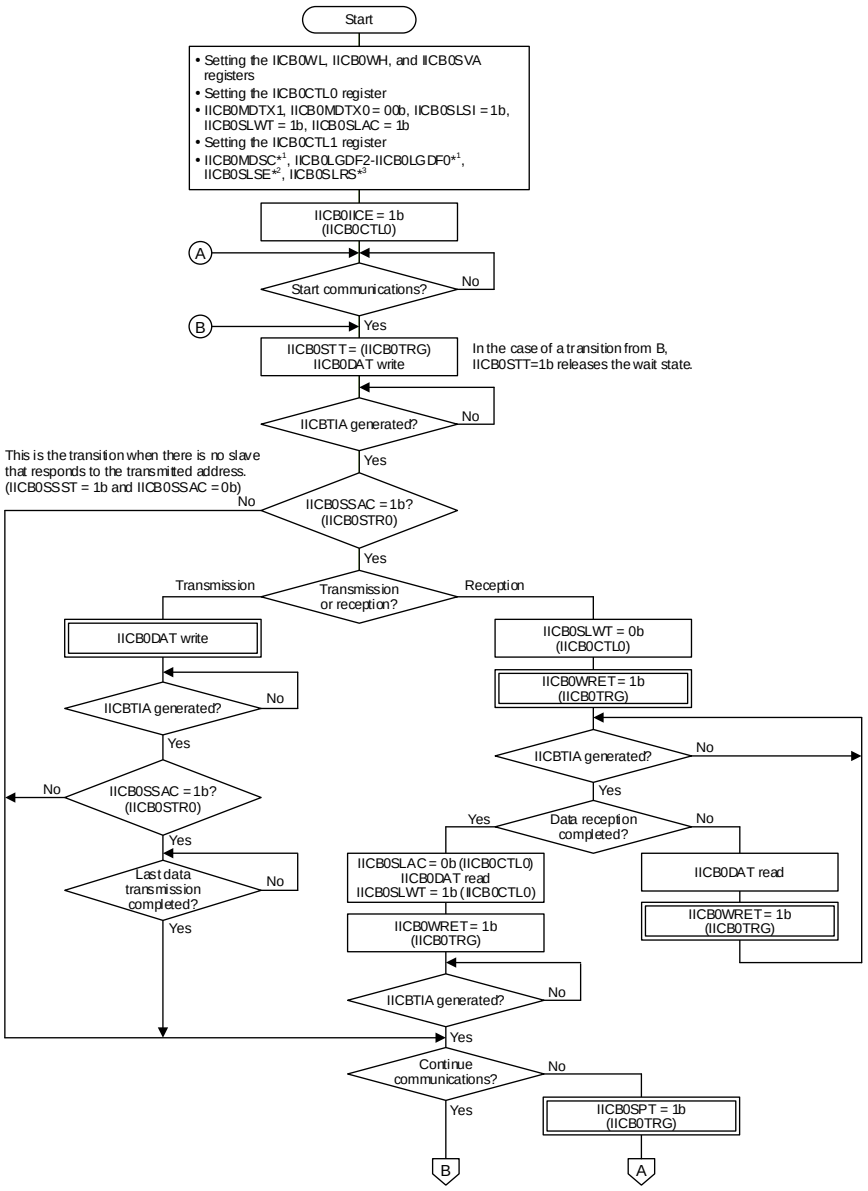
▲1: IICB0STR0 register = 1-0000X1 0110--00b
▲2: IICB0STR0 register = 0-0100X0 0100--01b (IICB0STRC.IICB0CLAF bit = 1b, IICB0TRG.IICB0LRET bit = 1b)
△3: IICB0STR0 register = 0-000000 0001--01b

Notes:
▲: Always generated
△: Only generated when the IICB0CTL0.IICB0SLSI bit = 1b
-: Undefined
X: Don't care

38.8 Setting Procedure

38.8.1 Single Master Environment

38.8.1.1 Procedure for Setting Master Operation in Single Transfer Mode



Note: The double-lined portion represents the process of releasing the wait.

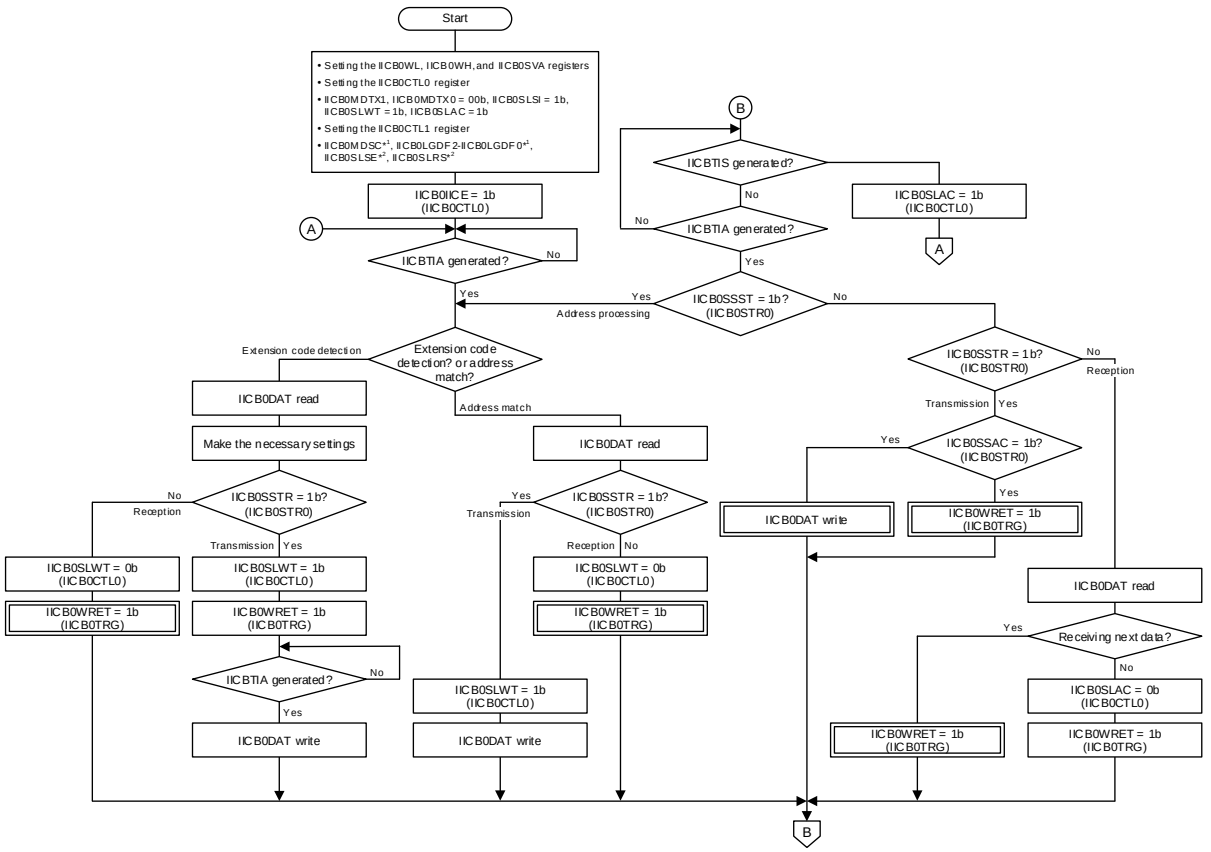
Note 1. Make settings appropriate for the environment.

Note 2. Set 1 for issuing the start condition in the initial state of communications, or set 0 for not issuing the start condition.

Note 3. In this environment, the setting values are not referenced.

Figure 38.8-1 Master Operation Setting Procedure in Single Transfer Mode (Single Master Environment)

38.8.1.2 Slave Operation Setting Procedure in Single Transfer Mode



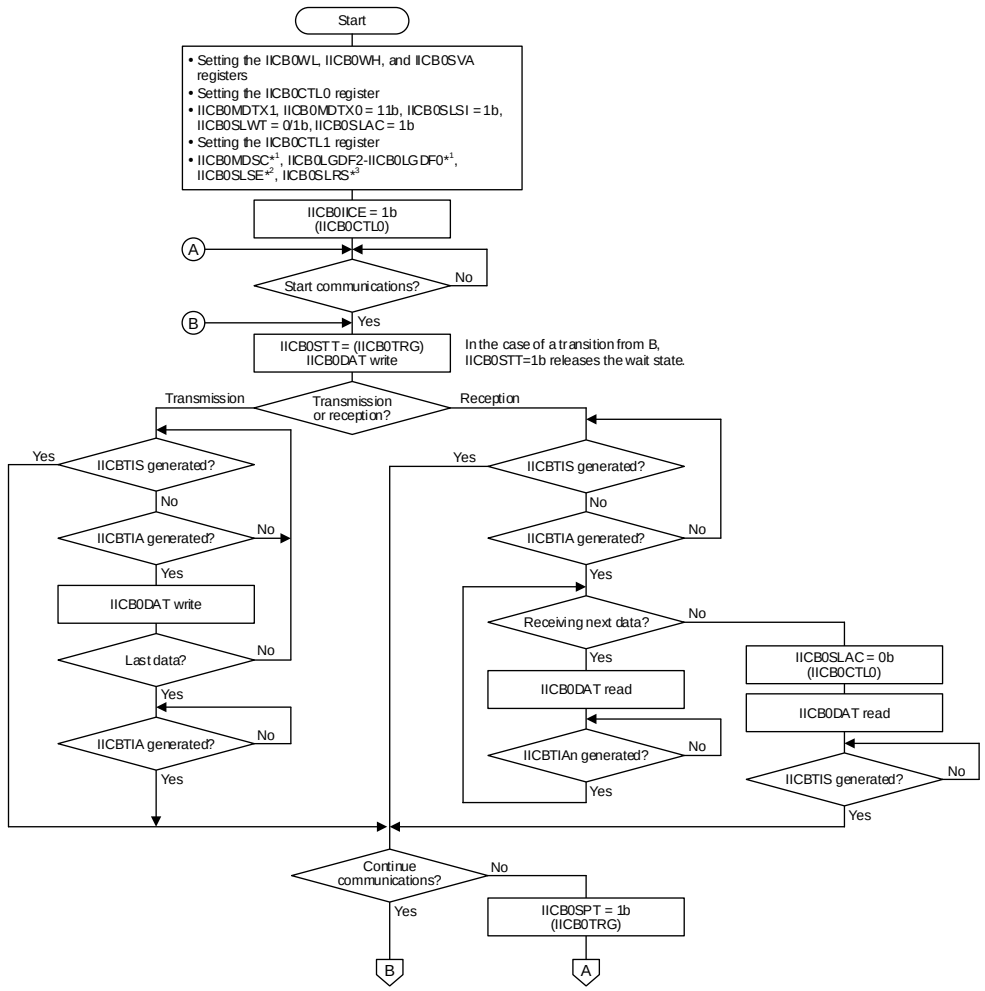
Note: The double-lined portion represents the process of releasing the wait.

Note 1. Make settings appropriate for the environment.

Note 2. In this environment, the setting values are not referenced.

Figure 38.8-2 Slave Operation Setting Procedure in Single Transfer Mode (Single Master Environment)

38.8.1.3 Procedure for Setting Master Operation in Continuous Transfer Mode



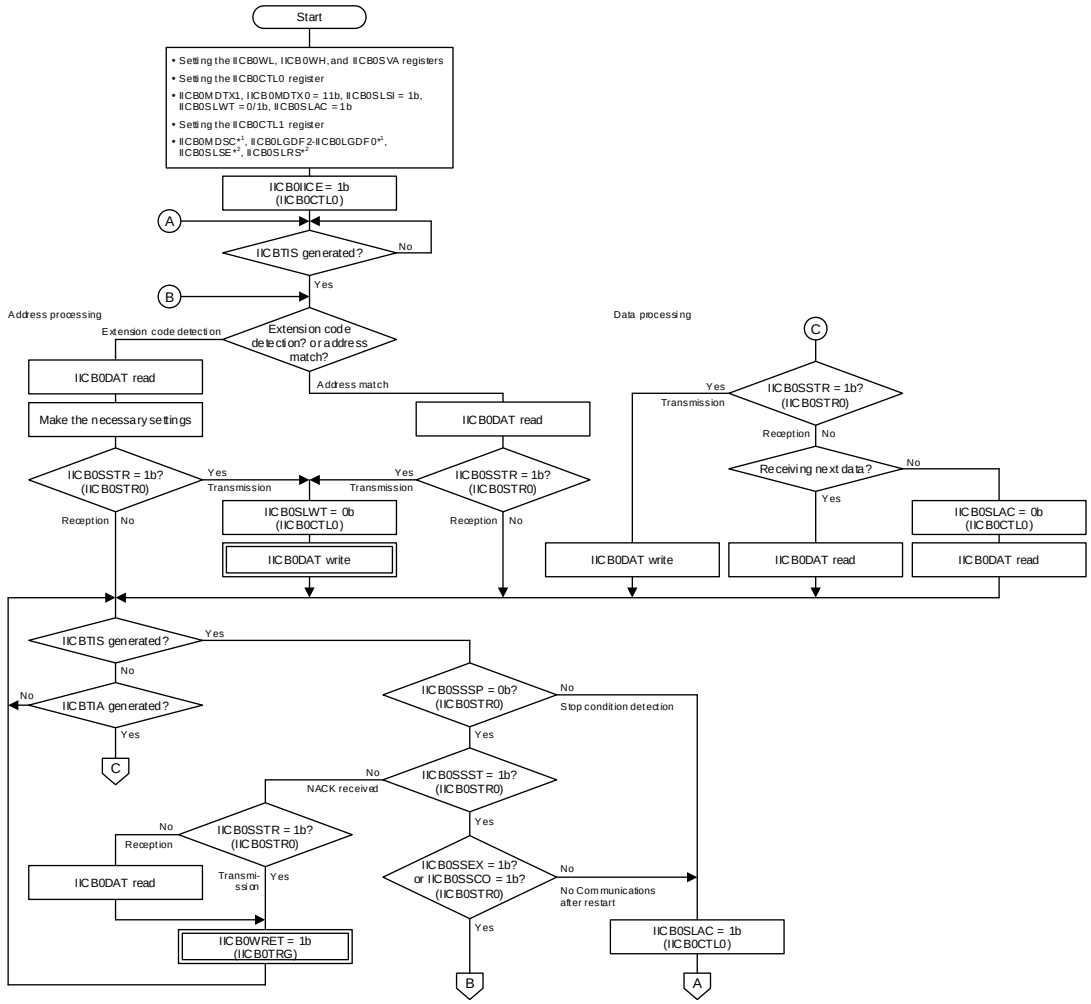
Note 1. Make settings appropriate for the environment.

Note 2. Set 1 for issuing the start condition in the initial state of communications, or set 0 for not issuing the start condition.

Note 3. In this environment, the setting values are not referenced.

Figure 38.8-3 Master Operation Setting Procedure in Continuous Transfer Mode (Single Master Environment)

38.8.1.4 Slave Operation Setting Procedure in Continuous Transfer Mode



Note: The double-lined portion represents the process of releasing the wait.

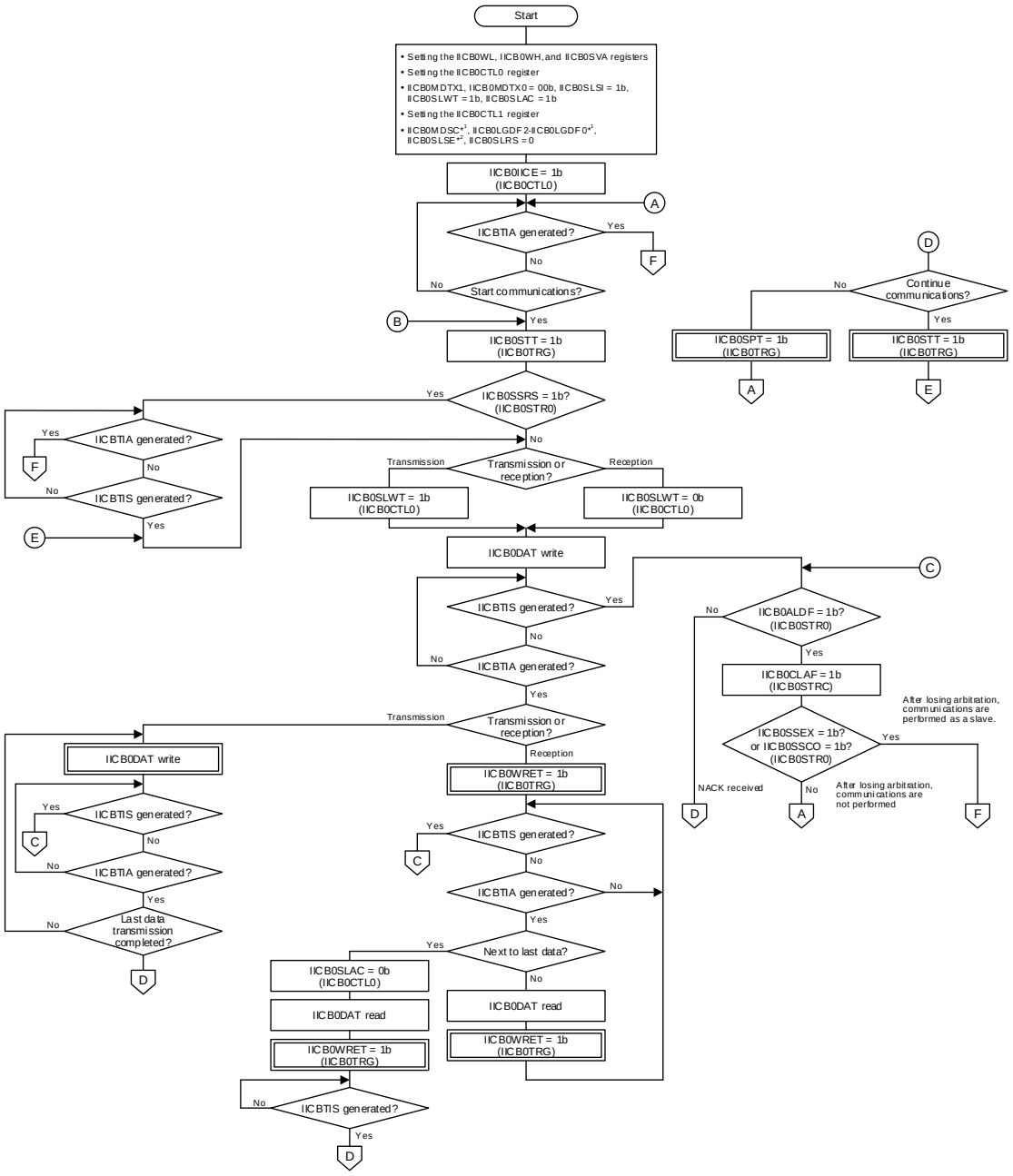
Note 1. Make settings appropriate for the environment.

Note 2. In this environment, the setting values are not referenced.

Figure 38.8-4 Slave Operation Setting Procedure in Continuous Transfer Mode (Single Master Environment)

38.8.2 Multi-Master Environment

38.8.2.1 Procedure for Setting Single Transfer Mode when Communication Reservation Function is Permitted (IICB0CTL1.IICB0SLRS bit = 0b)

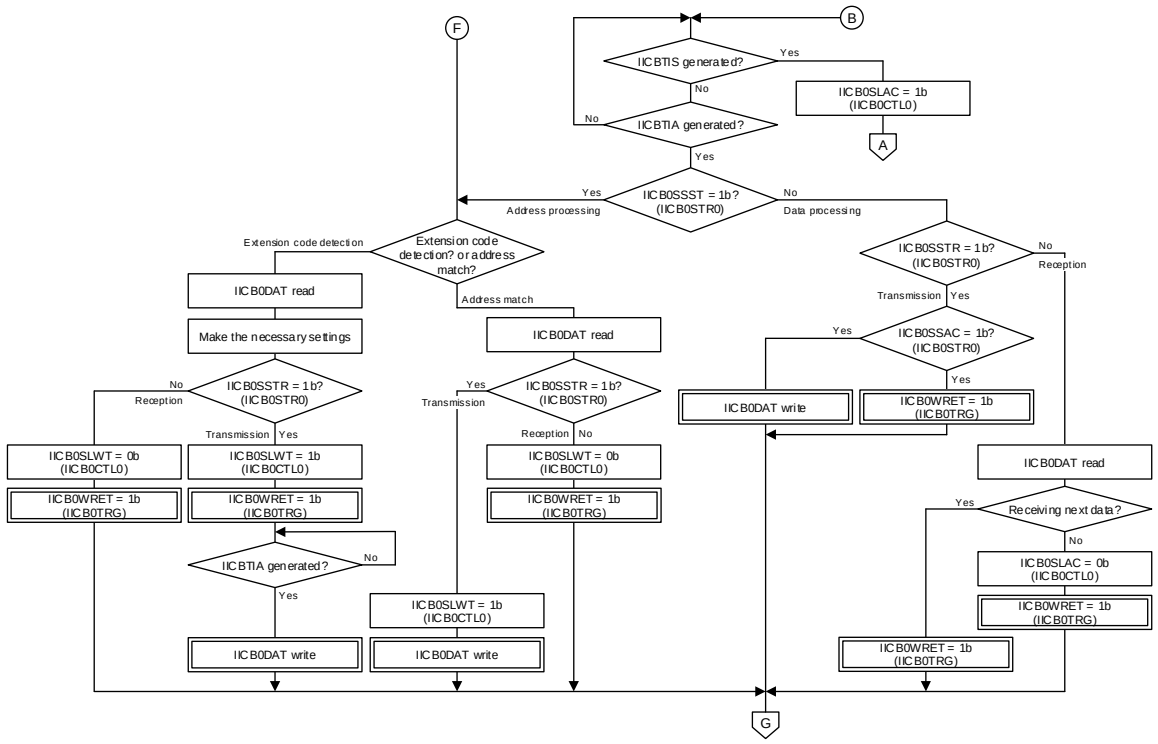


Note: The double-lined portion represents the procss of releasing the wait.

Note 1. Make settings appropriate for the environment.

Note 2. Set 1 for issuing the start condition in the initial state of communications, or set 0 for not issuing the start condition.

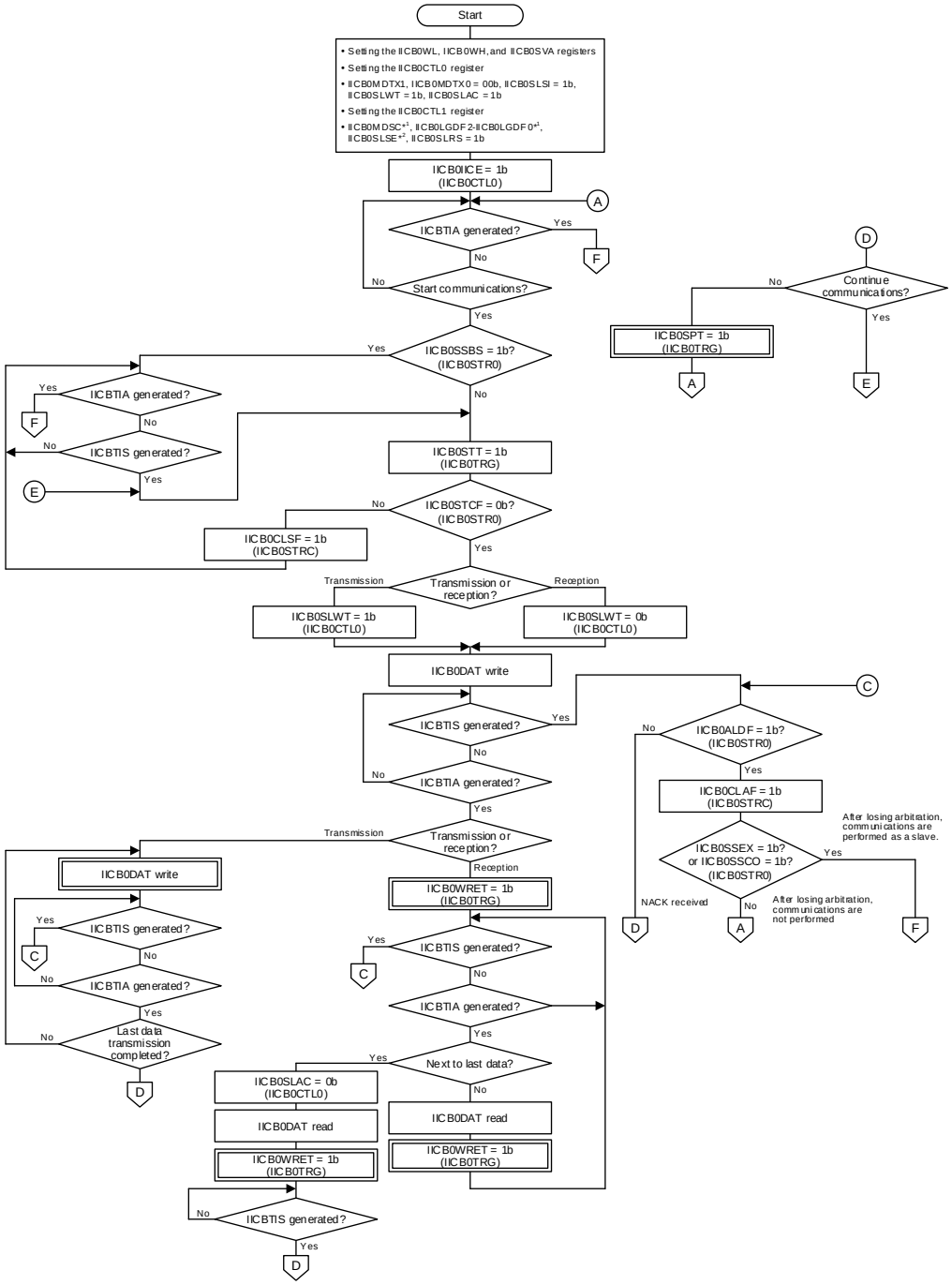
Figure 38.8-5 Procedure for Setting the Single Transfer Mode when the Communication Reservation Function is Permitted (Multi-Master Environment) (1/2)



Note: The double-lined portion represents the process of releasing the wait.

Figure 38.8-5 Procedure for Setting the Single Transfer Mode when the Communication Reservation Function is Permitted (Multi-Master Environment) (2/2)

38.8.2.2 Procedure for Setting the Single Transfer Mode when the Communication Reservation Function is Disabled (IICB0CTL1.IICB0SLRS bit = 1b)

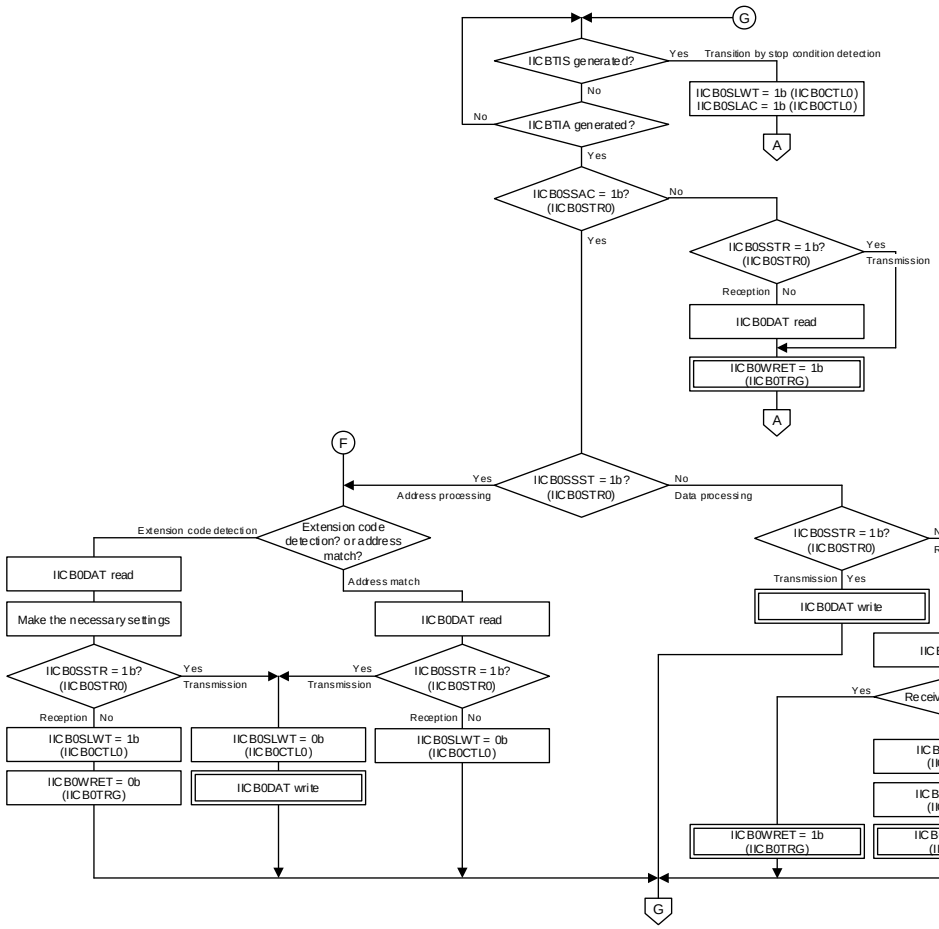


Note: The double-lined portion represents the pro

Note 1. Make settings appropriate for the environment.

Note 2. Set 1 for issuing the start condition in the initial state of communications, or set 0 for not issuing the start condition.

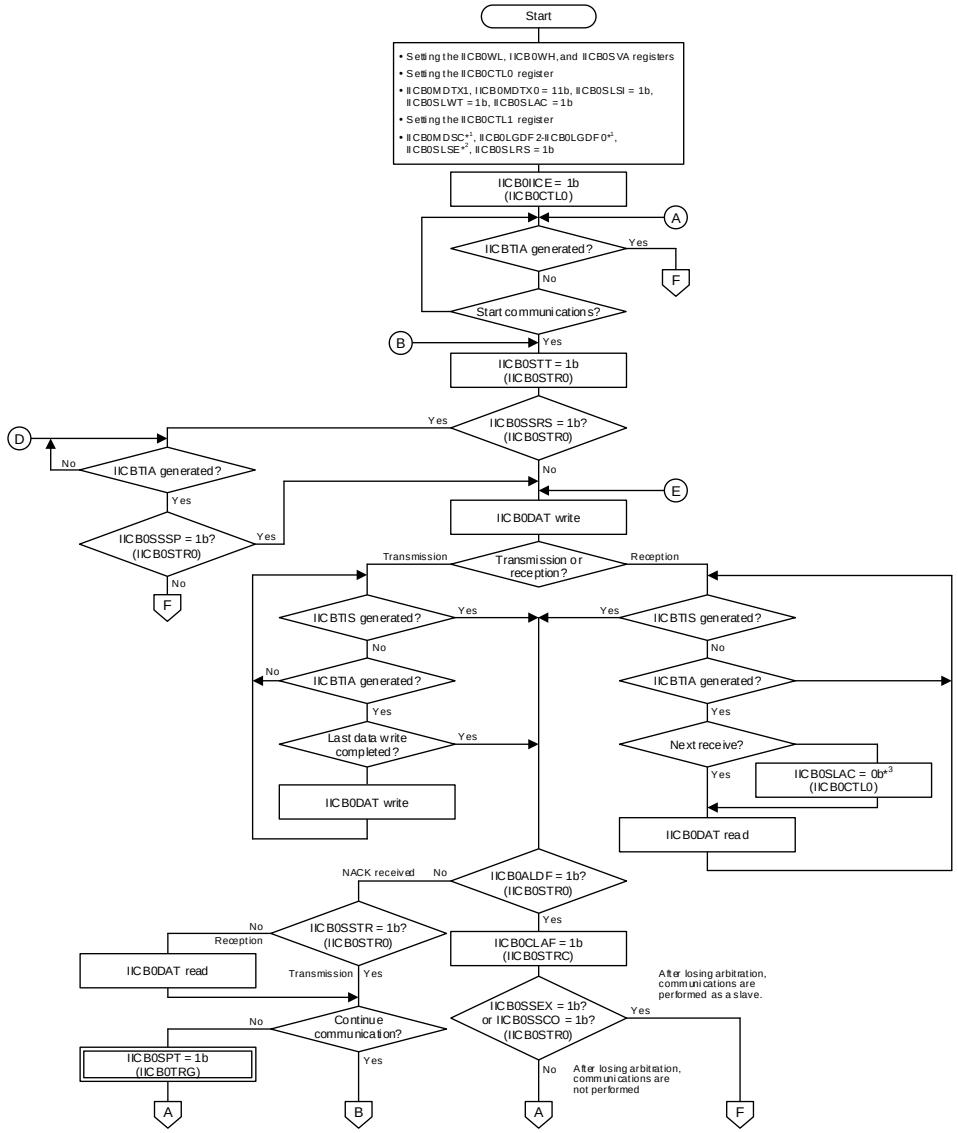
Figure 38.8-6 Procedure for Setting the Single Transfer Mode when the Communication Reservation Function is Disabled (Multi-Master Environment) (1/2)



Note: The double-lined portion represents the process of releasing the wait.

Figure 38.8-6 Procedure for Setting the Single Transfer Mode when the Communication Reservation Function is Disabled (Multi-Master Environment (2/2)

38.8.2.3 Procedure for Setting Continuous Transfer Mode when Communication Reservation Function is Permitted (IICB0CTL1.IICB0SLRS bit = 0b)



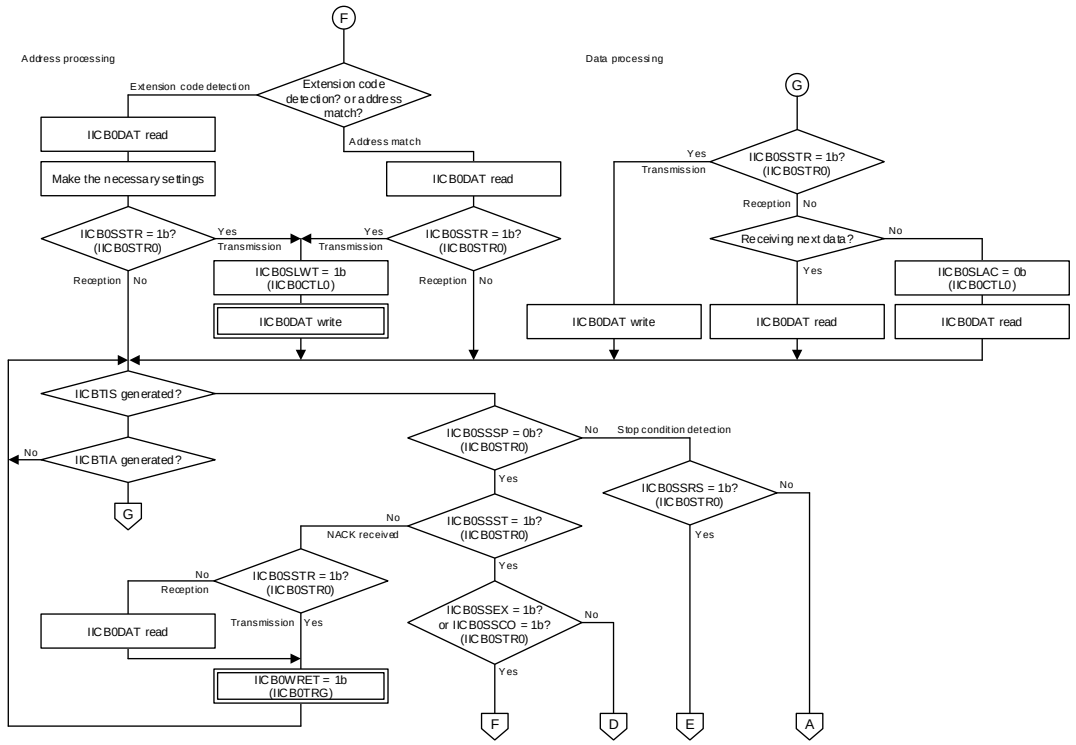
Note: The double-lined portion represents the process of releasing the wait.

Note 1. Make settings appropriate for the environment.

Note 2. Set 1 for issuing the start condition in the initial state of communications, or set 0 for not issuing the start condition.

Note 3. IICB0CTL0.IICB0SLAC bit = 0 must be set by the 8th clock of SCLm.

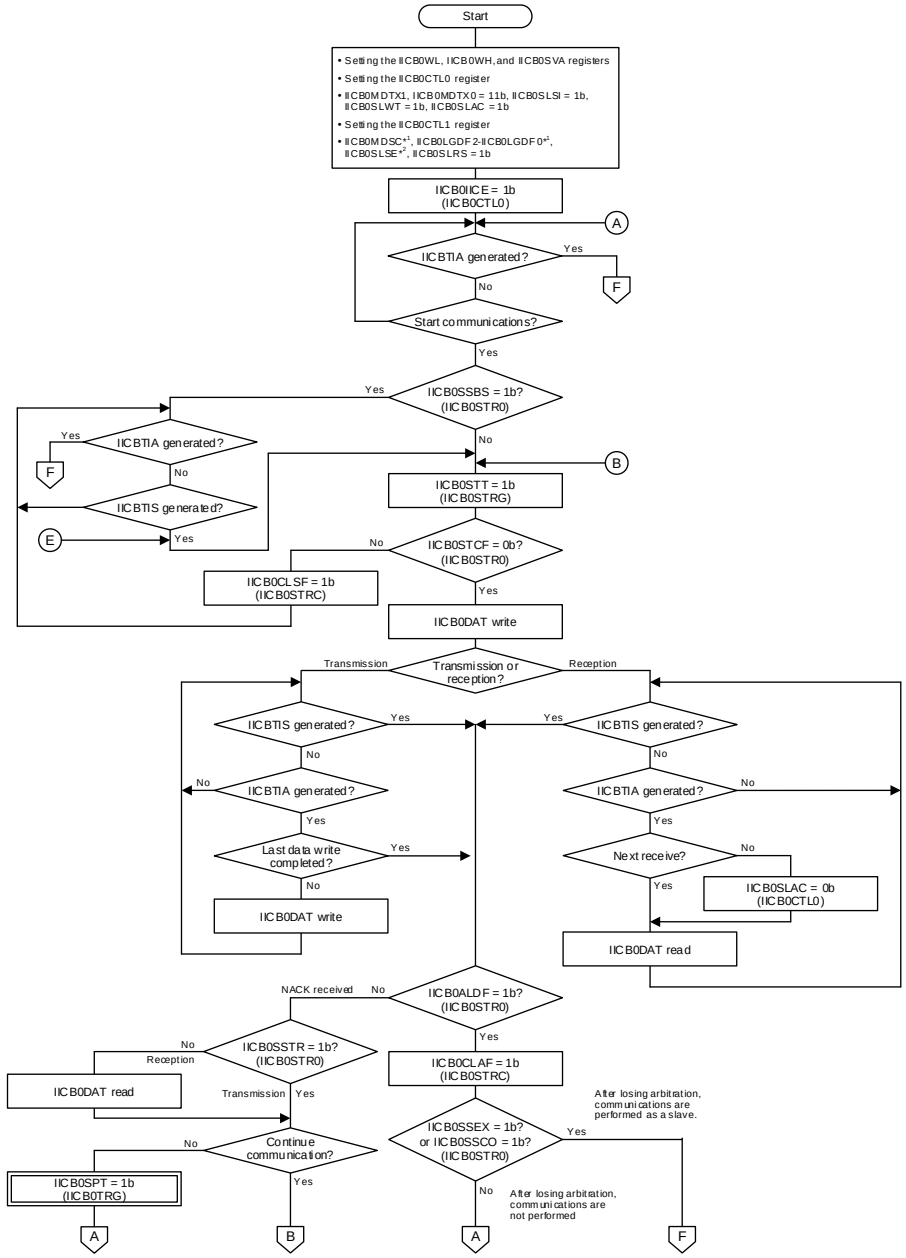
Figure 38.8-7 Procedure for Setting the Continuous Transfer Mode when the Communication Reservation Function is Permitted (Multi-Master Environment) (1/2)



Note: The double-lined portion represents the process of releasing the wait.

Figure 38.8-7 Procedure for Setting the Continuous Transfer Mode when the Communication Reservation Function is Permitted (Multi-Master Environment) (2/2)

38.8.2.4 Procedure for Setting the Continuous Transfer Mode when the Communication Reservation Function is Disabled (IICB0CTL1.IICB0SLRS bit = 1b)

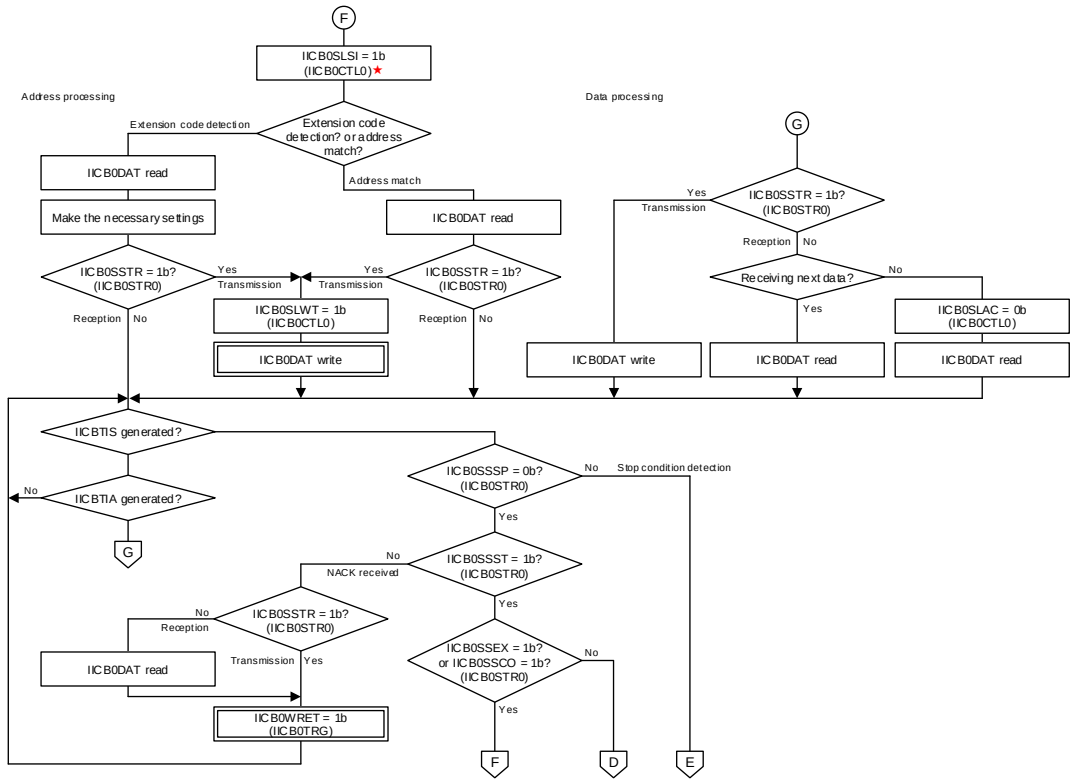


Note: The double-lined portion represents the process of releasing the wait.

Note 1. Make settings appropriate for the environment.

Note 2. Set 1 for issuing the start condition in the initial state of communications, or set 0 for not issuing the start condition.

Figure 38.8-8 Procedure for Setting the Continuous Transfer Mode when the Communication Reservation Function is Disabled (Multi-Master Environment) (1/2)



Note: The double-lined portion represents the process of releasing the wait.

Figure 38.8-8 Procedure for Setting the Continuous Transfer Mode when the Communication Reservation Function is Disabled (Multi-Master Environment) (2/2)

38.9 Emulation Function

38.9.1 Supervisor Mode Emulation Function

Transmission or reception is stopped when the SVSTOP pin becomes high level while IICB0SVSDIS = 0b. This is to support supervisor mode for the development tools.

*** The following is stated as IICB0SVSDIS = 0b.**

When SVSTOP is set (SVSTOP = Low -> High), operations of the transmission/reception circuit and timing generation circuit are stopped and the IIC is placed in the SVSTOP state.

Register access is possible even while in the SVSTOP state.

The registers are readable and writable even while in the SVSTOP state. In the case of writing, the written values are reflected in the internal registers. Synchronous reset (by writing 0b to IICB0IICE) and clearing the status bits (by writing 1b to IICB0CLSF and IICB0CLAF) are also possible.

Writing 1b to IICB0STT and IICB0SPT can also proceed and the start condition and stop condition are output after release from the SVSTOP state.

*** When writing 1 to IICB0STT and IICB0SPT, the time the IIC is placed in the SVSTOP state must be while writing is enabled.**

- SVSTOP during master operation

  When SVSTOP = H while IICB0SVSDIS = 0b during master operation, SCLO and SDAI retain their states at this time, and when SVSTOP = L, communications are resumed.

- SVSTOP during slave operation and while the IIC does not participate in communications

  During slave operation and while the IIC does not participate in communications, SCLO and SDAI are driven to H when SVSTOP = H while IICB0SVSDIS = 0b and the internal state of the unit is initialized when SVSTOP = L.

  However, when IICB0STT = 1b and 1b is written to IICB0SPT during the SVSTOP period, the start condition or stop condition is output after SVSTOP = L.

38.9.2 Received Data Emulation Read Function

When IICB0EDAT is read, the value of ICB0DAT is output as is.

Unlike reading of IICB0DAT, this does not affect the read history management circuit for IICB0DAT.

38.9.3 Shift Register Read Function

When IICB0DATS is read, the value of the shift register is output as is.

38.10 Usage Notes

38.10.1 Restrictions on the Change Timing of the SCL/SDA Line

This unit determines the status by sampling the respective lines of SCL and SDA with the APB clock (PCLK). Therefore, when SCL and SDA change at the timing shown in **Figure 38.10-1**, this is not judged as a start condition (restart condition).

The IIC bus specification does not define the operation when such a timing change occurs.

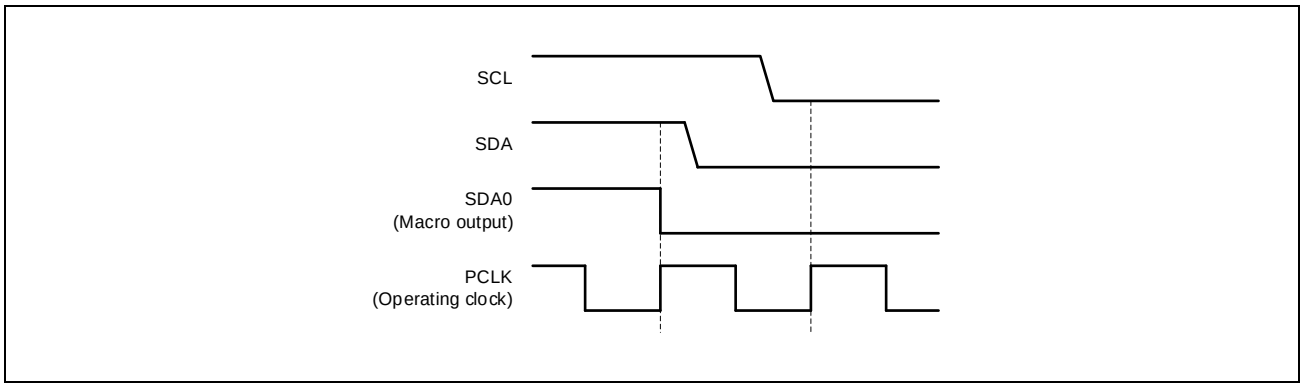
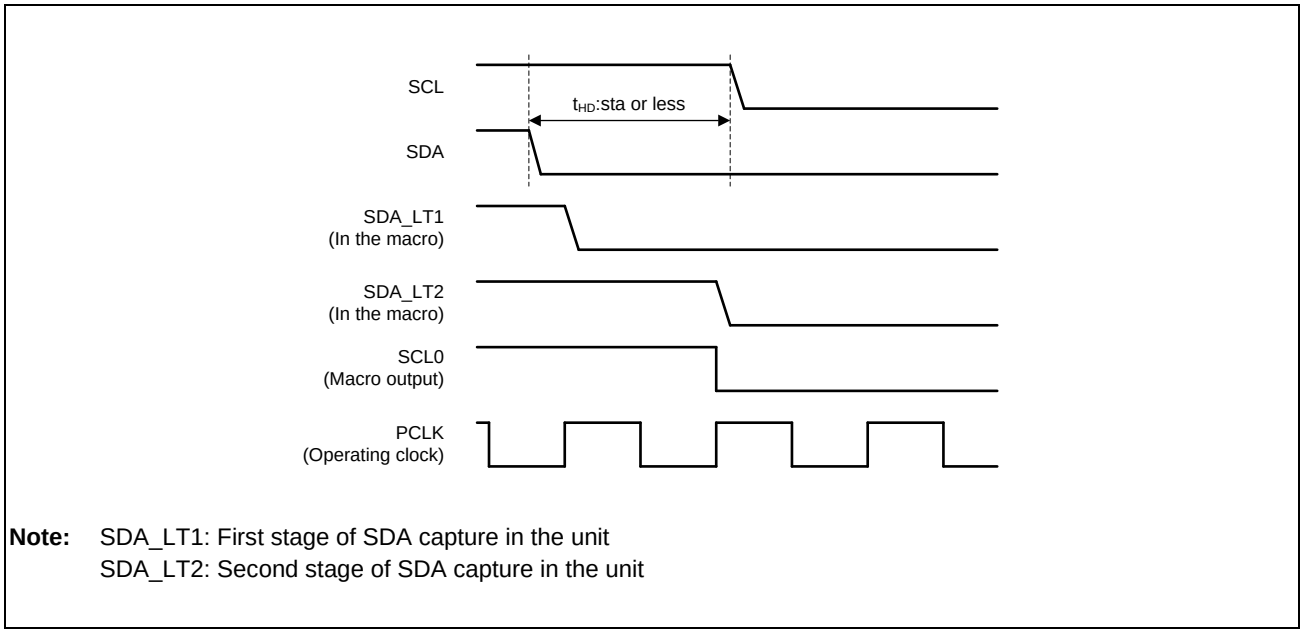


Figure 38.10-1 Timing Example for Determining Simultaneous Change

38.10.2 Restrictions on the Start Condition Hold Time

This unit may set the SCL line to a low level at the timing that does not satisfy the start condition hold time (t_{HD}:STA).

When this unit is operating as the master, after the Tsu:sta time has elapsed, if the SDA line changes by the external source and the set low-width time elapses before this unit detects the change, the SCL line is set to a low level at the time less than t_{HD}:STA. In this case, the unit will not lose in arbitration and continue to operate as the master.



Note: SDA_LT1: First stage of SDA capture in the unit
SDA_LT2: Second stage of SDA capture in the unit

Figure 38.10-2 Timing Example where Start Condition Hold Time is Not Satisfied

Section 39 Clocked Serial Interface (CSI)

This section describes the functions of the clocked serial interface (CSI).

39.1 Functional Overview

The CSI is an interface for clock synchronized serial communication that uses three signals: the serial clock (SCK), serial data input (SI), and serial data output (SO); and it is compatible with the SPI (Serial Peripheral Interface).

The CSI can handle the slave selection (SS) signal as an input and in this case can operate as an SPI slave. It can also handle the slave selection (SS) signal as an output and in this case can operate as an SPI master.

This LSI has a total of six CSIs from ch. 0 to ch. 5. Of those, ch. 1, ch. 2, ch. 3, and ch. 5 are for use with the ISP support package, so do not use registers related to those channels.

In addition, since the DMAC is for use with the ISP support package, do not use the DMA transfer method for the CSI.

39.1.1 Features

- Master reception-only mode, master transmission/reception mode, slave reception-only mode, or slave transmission/reception mode is selectable.
- The serial data length is selectable from 8 or 16 bits.
- The first bit of serial data is selectable from MSB or LSB.
- The serial clock is selectable as the master clock divided by values from 2 to 32766 (the master clock frequency is up to 48 MHz).
- The serial clock input frequency is up to 24 MHz in slave mode.
- Data transfer in response to interrupts or DMA transfer by the external DMA controller is selectable.
- Two 16-bit (8-bit + 8-bit) 16-stage FIFO buffers are included, one for transmission and one for reception.
- The waiting time between serial data is specifiable in master mode.

39.1.2 Block Diagram

The figure below is a block diagram of the CSI.

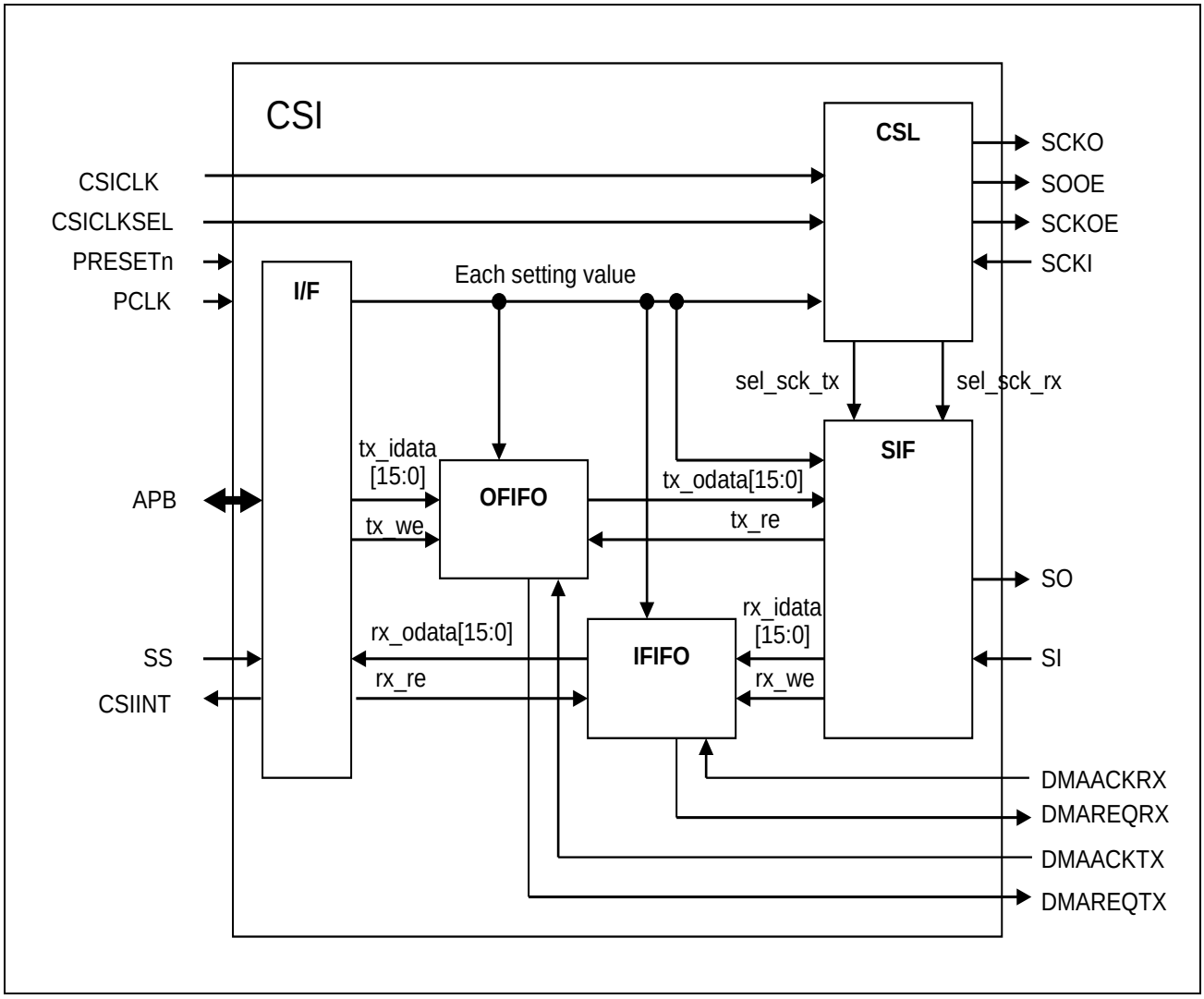


Figure 39.1-1 Block Diagram

39.1.3 Connection Configuration

Figure 39.1-2 shows the CSI connection configuration.

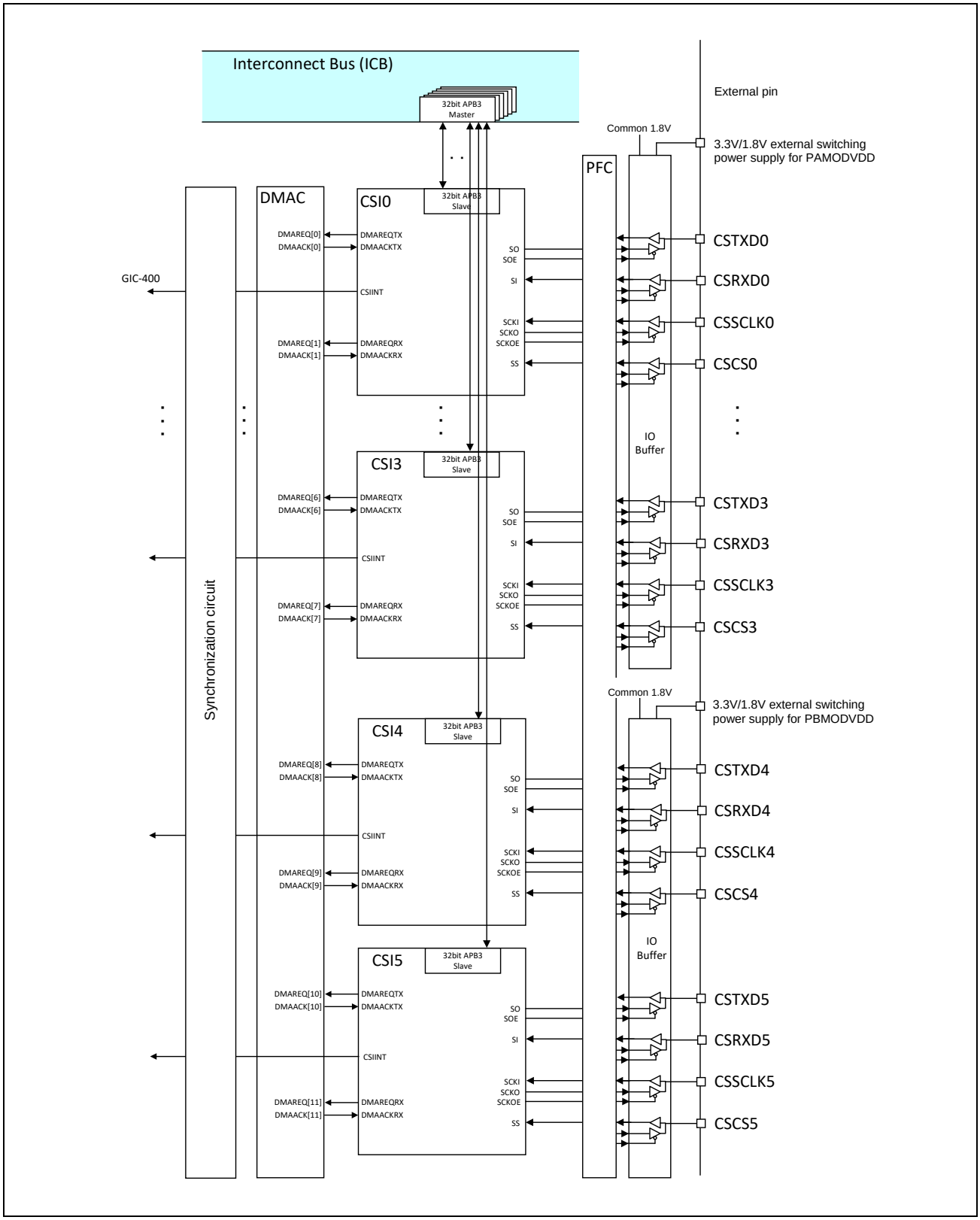


Figure 39.1-2 Connection Configuration

39.2 Pin Functions

39.2.1 List of Internal Pins

Table 39.2-1 lists the internal pins of the CSI.

Table 39.2-1 List of Internal Pins

Pin Name		I/O	Function
Serial control pins	SCKOE	Output	Serial clock output enable signal 0b: Disable (slave mode) 1b: Enable (master mode)
	SCKI	Input	Serial clock input (Maximum frequency: 1/2 PCLK)
	SCKO	Output	Serial clock output
	SI	Input	Serial data input
	SO	Output	Serial data output
	SOOE	Output	Serial data output enable signal 0b: Disable 1b: Enable
	SS	Input	Slave selection The active level can be set by a register.
	CSICLK	Input	External clock input pin (Maximum frequency: 1/2 PCLK)
	CSICLKSEL	Input	Master clock source selection 0b: PCLK is used 1b: CSICLK is used The value is fixed to 1b in this LSI.
Interrupt pin	CSIINT	Output	CSI interrupt signal The interrupt controller uses this signal as a level signal.
DMA control pins	DMAREQTX	Output	DMA transfer request signal for transmission Signal requesting writing of data for transmission to the DMAC
	DMAACKTX	Input	DMA acknowledge signal for transmission Signal notifying the completion of writing data for transmission from the DMAC
	DMAREQRX	Output	DMA transfer request signal for reception Signal requesting reading of received data to the DMAC
	DMAACKRX	Input	DMA acknowledge signal for reception Signal notifying the completion of reading received data from the DMAC

39.3 Register Descriptions

For the register base addresses (<CSI0_S0_base>, <CSI1_S0_base>, <CSI2_S0_base>, <CSI3_S0_base>, <CSI4_S0_base>, and <CSI5_S0_base>), see the section of Address Map.

39.3.1 List of Registers

The table below lists the registers of the CSI.

Table 39.3-1 List of Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
00h	CSI Mode Control Register	CSIm_CSI_MODE	0000_0000h	32
04h	CSI Clock Select Register	CSIm_CSI_CLKSEL	0000_FFFEh	32
08h	CSI Control Register	CSIm_CSI_CNT	10x0_0000h	32
0Ch	CSI Interrupt Status Register	CSIm_CSI_INT	0000_0000h	32
10h	CSI Receive FIFO Level Indicate Register	CSIm_CSI_IFIFOL	0000_0000h	32
14h	CSI Transmit FIFO Level Indicate Register	CSIm_CSI_OFIFOL	0000_0000h	32
18h	CSI Receive Window Register	CSIm_CSI_IFIFO	0000_0000h	32
1Ch	CSI Transmit Window Register	CSIm_CSI_OFIFO	0000_0000h	32
20h	CSI FIFO Trigger Level Register	CSIm_CSI_FIFOTRG	0000_0000h	32
24h to 3Fh	Reserved	—	0000_0000h	32

Note: m = 0 to 5, x: Don't care

39.3.2 Register Descriptions

The function description of each register is given below.

The prefix (CSIm_) of the register names is omitted in the register descriptions and the field descriptions in this section.

39.3.2.1 CSI Mode Control Register (CSIm_CSI_MODE) (m = 0 to 5)

This register controls the serial communication processing of CSI. It is initialized to 0b by a reset. This register is set before communication starts for basic communication settings such as CSI communication mode, data length, and head data selection. It also monitors the communication status and starts and stops communication.

DATWT, TRMD, CCL, and DIR may not be changed during the communication (CSIE=1b or CSOT=1b). Therefore, when setting these bits, set the CSIE bit to 0b and read the CSOT bit to confirm that communication has stopped.

The CSIE bit should not be changed with other bits simultaneously.

Access Size: 32 bits

Address: <CSI0_S0_base> + 0000h
<CSI1_S0_base> + 0000h
<CSI2_S0_base> + 0000h
<CSI3_S0_base> + 0000h
<CSI4_S0_base> + 0000h
<CSI5_S0_base> + 0000h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	DATWT[3:0]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CSIE	TRMD	CCL	DIR	—	—	—	CSOT
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R

Table 39.3-2 CSIm_CSI_MODE Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	DATWT[3:0]	Setting of the interval time between the serial data transfer. This setting is valid in the master mode. Invalid is the slave mode. Set in the range of 0 to 15 clocks (1 clock is SCKO clock).
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7	CSIE	Starting and stopping communication. 0b: Stop (initial value) 1b: Start
6	TRMD	Select the communication mode. 0b: Receive-only mode (initial value) 1b: Transmit/reception mode
5	CCL	Select the serial data length. 0b: 8 bits (initial value) 1b: 16 bits

Table 39.3-2 CSIm_CSI_MODE Register Contents (2/2)

Bit Position	Bit Name	Description
4	DIR	Select the first data of serial data. 0b: MSB (initial value) 1b: LSB
3 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	CSOT	The communication state flag. Writing is invalid. 0b: Communication is stopped. 1b: Communication is in progress.

39.3.2.2 CSI Clock Select Register (CSIm_CSI_CLKSEL) (m = 0 to 5)

This register selects master/slave mode, sets the slave selection pin (SS pin), selects the clock polarity and data phase for serial communication, and selects the baud rate. Initialize the SLAVE bit to 1b and other bits to 0b by a reset.

This register may not be rewritten. Therefore, when setting, set the CSIE bit to 0 and read the CSOT bit to confirm that communication has stopped.

Also, issue a CSI reset after changing the setting.

Access Size: 32 bits

Address: <CSI0_S0_base> + 0004h
<CSI1_S0_base> + 0004h
<CSI2_S0_base> + 0004h
<CSI3_S0_base> + 0004h
<CSI4_S0_base> + 0004h
<CSI5_S0_base> + 0004h

Initial Value: 0000_FFFEh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	SS_ENA	SS_POL	CKP	DAP
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SLAVE	CKS[14:1]														—
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 39.3-3 CSIm_CSI_CLKSEL Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19	SS_ENA	Control by the SS pin. This setting is valid in slave mode. Invalid in master mode. 0b: Disable control by the SS pin (initial value). 1b: Enable control by the SS pin.
18	SS_POL	Select the polarity of the SS pin. This setting is valid in slave mode. Invalid in master mode. 0b: Active low (initial value). 1b: Active high.
17	CKP	Select the polarity of the serial clock in idle time. 0b: The polarity of the serial clock is high (initial value). 1b: The polarity of the serial clock is low.
16	DAP	Select the phase of the serial data. 0b: SO is output with the same phase as SCK. SI is sampled after half a cycle (initial value). 1b: SO is output half a cycle before SCK. SI is sampled in the same phase.
15	SLAVE	Select the operation mode (master/slave mode). 0b: Master mode 1b: Slave mode (initial value)

Table 39.3-3 CSIm_CSI_CLKSEL Register Contents (2/2)

Bit Position	Bit Name	Description
14 to 1	CKS[14:1]	Select the divided ratio of the serial clock. Select the division ratio from the master clock to determine the frequency of the serial clock output SCKO. The master clock is the clock (CSICLK is used in this LSI) selected by the master clock source selection (CSICLKSEL). This setting is enabled in master mode. It is disabled in sleep mode. The division ratio is selected in the range of 1/2 to 1/32766 with the setting value from 0001h to 3FFFh. The division ratio of the serial clock should be set in consideration of the available frequency of PCLK, CSICLK, and the serial clock. Table 39.3-3a

CKS[14:1]	Ratio
0000h	1/2 (prohibited)
0001h	1/2
0002h	1/4
0003h	1/6
0004h	1/8
0008h	1/16
0010h	1/32
0100h	1/512
1000h	1/8192
3FFFh	1/32766 (initial value)

Note: Division ratio = 1/(2*CKS) (except when CKS = 0000h)

0	—	Reserved. This bit is read as 0b. The write value should always be 0b.

39.3.2.3 CSI Control Register (CSIm_CSI_CNT) (m = 0 to 5)

This register controls and sets CSI. This register consists of software reset, trigger function enable/disable, transmit and receive status display, DMA mode enable/disable, interrupt mask, and SS pin level monitor bits for CSI. Resetting initializes the CSIRST bit to 1b and all other bits to 0b. However, the initial value of the SS_MON bit depends on the SS pin. During communication (CSIE = 1b or CSOT = 1b), a value different from the previous value may not be written except for the interrupt control bits (bits[13: 0]). If these bits are rewritten during communication, operation is not guaranteed.

Access Size: 32 bits

Address: <CSI0_S0_base> + 0008h
<CSI1_S0_base> + 0008h
<CSI2_S0_base> + 0008h
<CSI3_S0_base> + 0008h
<CSI4_S0_base> + 0008h
<CSI5_S0_base> + 0008h

Initial Value: 10x0_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CSIRST	T_TRGEN	T_FIFOF	—	T_DMAEN	—	—	SS_MON	—	R_TRGEN	R_FIFOF	—	R_DMAEN
Initial Value	0	0	0	1	0	0	0	0	0	0	x	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	R	RW	RW	RW	RW	R	RW	RW	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	UNDER_E	OVERF_E	—	—	TREND_E	CSIEND_E	—	—	—	T_TRGR_E	—	—	—	R_TRGR_E
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 39.3-4 CSIm_CSI_CNT Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 29	—	Reserved. These bits are read as 0b. The write value should always be 0b.
28	CSIRST	CSI software reset. 0b: Release the reset. 1b: Reset (initial value)
27	T_TRGEN	Select enabling or disabling of the transmission FIFO trigger level setting (CSI_FIFOTRG register T_TRG[2:0]). 0b: Disable (initial value) 1b: Enable
26	T_FIFOF	The state of the transmission FIFO. Regardless of the transmission data length (8 or 16 bits), the transmission FIFO having 32 bytes of data is judged to be full. Writing is invalid. 0b: Tx FIFO buffer is not full (initial value). 1b: Tx FIFO buffer is full.
25	—	Reserved. This bit is read as 0b. The write value should always be 0b.
24	T_DMAEN	The transmission DMA mode. 0b: Disable (initial value) 1b: Enable
23, 22	—	Reserved. These bits are read as 0b. The write value should always be 0b.

Table 39.3-4 CSIm_CSI_CNT Register Contents (2/2)

Bit Position	Bit Name	Description
21	SS_MON	Monitoring the SS pin. Indicate the input level of the SS pin. Writing is invalid. *Note*: The initial value of bit 21 depends on the state of the SS pin. 0b: The SS pin is at the low level. 1b: The SS pin is at the high level.
20	—	Reserved. This bit is read as 0b. The write value should always be 0b.
19	R_TRGEN	Select enabling or disabling of the reception FIFO trigger level setting (CSI_FIFOTRG register R_TRG[2:0]). 0b: Disable (initial value) 1b: Enable
18	R_FIFOF	The state of the reception FIFO. Regardless of the transmission data length (8 or 16 bits), the reception FIFO having 32 bytes of data is judged to be full. Writing is invalid. 0b: Rx FIFO buffer is not full (initial value). 1b: Rx FIFO buffer is full.
17	—	Reserved. This bit is read as 0b. The write value should always be 0b.
16	R_DMAEN	The reception DMA mode. 0b: Disable (initial value) 1b: Enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13	UNDER_E	Tx FIFO buffer underrun error interrupt (enabling CSI_INT register bit 13 (UNDER)). 0b: Disable interrupt (initial value). 1b: Enable interrupt.
12	OVERF_E	Rx FIFO buffer overflow error interrupt (enabling CSI_INT register bit 12 (OVERF)). 0b: Disable interrupt (initial value). 1b: Enable interrupt.
11, 10	—	Reserved. These bits are read as 0b. The write value should always be 0b.
9	TREND_E	All transmission complete interrupt (enabling CSI_INT register bit 9 (TREND)). 0b: Disable interrupt (initial value). 1b: Enable interrupt.
8	CSIEND_E	Transfer completion interrupt (enabling CSI_INT register bit 8 (CSIEND)). 0b: Disable interrupt (initial value). 1b: Enable interrupt.
7 to 5	—	Reserved. These bits are read as 0b. The write value should always be 0b.
4	T_TRGR_E	Transmission trigger level interrupt (enabling CSI_INT register bit 4 (T_TRGR)). 0b: Disable interrupt (initial value). 1b: Enable interrupt.
3 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	R_TRGR_E	Reception trigger level interrupt (enabling CSI_INT register bit 0 (R_TRGR)). 0b: Disable interrupt (initial value). 1b: Enable interrupt.

39.3.2.4 CSI Interrupt Status Register (CSIm_CSI_INT) (m = 0 to 5)

This register is used to read and clear the interrupt factors. It is initialized to 0b by a reset.

In addition, when clearing the interrupt factor, release the interrupt cause before clearing it. Even if interrupts are disabled in the CSI_CNT register, each bit is asserted if the condition is met.

Access Size: 32 bits

Address: <CSI0_S0_base> + 000Ch
<CSI1_S0_base> + 000Ch
<CSI2_S0_base> + 000Ch
<CSI3_S0_base> + 000Ch
<CSI4_S0_base> + 000Ch
<CSI5_S0_base> + 000Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	UNDER	OVERF	—	—	TREND	CSIEND	—	—	—	T_TRGR	—	—	—	R_TRGR
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 39.3-5 CSIm_CSI_INT Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15, 14	—	Reserved. The write value should always be 0b.
13	UNDER	Tx FIFO buffer underrun error interrupt. Read: 0b: No interrupt. 1b: An underrun error occurs. Write: 0b: Hold the interrupt factor. 1b: Clear the interrupt factor.
12	OVERF	Rx FIFO buffer overflow error interrupt. Read: 0b: No interrupt. 1b: A buffer overflow error occurs. Write: 0b: Hold the interrupt factor. 1b: Clear the interrupt factor.
11, 10	—	Reserved. These bits are read as 0b. The write value should always be 0b.

Table 39.3-5 CSIm_CSI_INT Register Contents (2/2)

Bit Position	Bit Name	Description
9	TREND	The all transmission complete interrupt. Indicates that transmission of all data in the Tx FIFO is complete. If the Tx FIFO is empty when transmission is complete, an all transmission complete interrupt occurs. Read: 0b: No interrupt. 1b: All transmission completed. Write: 0b: Hold the interrupt factor. 1b: Clear the interrupt factor.
8	CSIEND	The transfer complete interrupt. When transmission or reception of a single unit of data is completed, this interrupt occurs. Read: 0b: No interrupt. 1b: Completion of transmission or reception Write: 0b: Hold the interrupt factor. 1b: Clear the interrupt factor.
7 to 5	—	Reserved. These bits are read as 0b. The write value should always be 0b.
4	T_TRGR	The transmission trigger level interrupt. When the transmission trigger level setting is invalid (T_TRGEN=0), this interrupt does not occur. Read: 0b: Tx trigger level not reached. 1b: Tx trigger level reached. Write: 0b: Hold the interrupt factor. 1b: Clear the interrupt factor.
3 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	R_TRGR	The Rx trigger level interrupt. When the reception trigger level setting is invalid (R_TRGEN=0), this interrupt does not occur. Read: 0b: Rx trigger level not reached. 1b: Rx trigger level reached. Write: 0b: Hold the interrupt factor. 1b: Clear the interrupt factor.

39.3.2.5 CSI Receive FIFO Level Indicate Register (CSIm_CSI_IFIFOL) (m = 0 to 5)

CSI is equipped with a 16-stage receive FIFO buffer (1 stage is 8 bits + 8 bits) to store the received data.

This register indicates the receive FIFO buffer usage in bytes (8 bits). It is initialized by a reset or CSI reset (CIRST=1b in CSI_MODE register).

When the serial data length is 8 bits (CCL = 0b in the CSI_MODE register), it is incremented by 1 each time data is received in the receive FIFO buffer and is decremented by 1 each time data (8 bits) is read from the receive FIFO buffer.

When the serial data length is 16 bits (CCL = 1b in CSI_MODE register), it is incremented by 2 each time data is received in the receive FIFO buffer and is decremented by 2 each time data (16 bits) is read from the receive FIFO buffer.

Writing to this register deletes the whole receive FIFO buffer (flush) regardless of the written value and sets RFL[5:0]=000000b.

Writing is prohibited during communication (when CSIE in the CSI_MODE register is 1 or CSOT = 1b).

Access Size: 32 bits

Address: <CSI0_S0_base> + 0010h
<CSI1_S0_base> + 0010h
<CSI2_S0_base> + 0010h
<CSI3_S0_base> + 0010h
<CSI4_S0_base> + 0010h
<CSI5_S0_base> + 0010h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	RFL[5:0]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 39.3-6 CSIm_CSI_IFIFOL Register Contents

Bit Position	Bit Name	Description
31 to 6	—	Reserved. These bits are read as 0b.
5 to 0	RFL[5:0]	The number of bytes occupied in the receive FIFO buffer. Read: 000000b: The receive FIFO buffer is empty. 000001b: 1 byte 000010b: 2 bytes | 011111b: 31 bytes 100000b: 32 bytes 100001b to 111111b: Reserved. Write: Regardless of the written value, delete the receive FIFO buffer data and set the register value to 0b simultaneously.

39.3.2.6 CSI Transmit FIFO Level Indicate Register (CSIm_CSI_OFIFOL) (m = 0 to 5)

CSI is equipped with a 16-stage transmit FIFO buffer (1 stage is 8 bits + 8 bits) to store the transmit data.

This register indicates the transmit FIFO buffer usage in bytes (8 bits). It is initialized by a reset or CSI reset (CIRST=1b in CSI_MODE register).

When the serial data length is 8 bits (CCL = 0b in CSI_MODE register), it is incremented by 1 each time data is written in the transmit FIFO buffer and is decremented by 1 each time data (8 bits) is transmitted from the transmit FIFO buffer.

When the serial data length is 16 bits (CCL = 1b in CSI_MODE register), it is incremented by 2 each time data is written in the transmit FIFO buffer and is decremented by 2 each time data (16 bits) is transmitted from the transmit FIFO buffer.

Writing to this register deletes the whole transmit FIFO buffer (flush) regardless of the written value and sets TFL[5:0]=000000b.

Writing is prohibited during communication (when CSIE in the CSI_MODE register is 1 or CSOT = 1b).

Access Size: 32 bits

Address: <CSI0_S0_base> + 0014h
<CSI1_S0_base> + 0014h
<CSI2_S0_base> + 0014h
<CSI3_S0_base> + 0014h
<CSI4_S0_base> + 0014h
<CSI5_S0_base> + 0014h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	TFL					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 39.3-7 CSIm_CSI_OFIFOL Register Contents

Bit Position	Bit Name	Description
31 to 6	—	Reserved. These bits are read as 0b.
5 to 0	TFL	The number of bytes occupied in the transmit FIFO buffer. Read: 000000b: The transmit FIFO buffer is empty. 000001b: 1 byte 000010b: 2 bytes | 011111b: 31 bytes 100000b: 32 bytes 100001b to 111111b: Reserved. Write: Regardless of the written value, delete the transmit FIFO buffer data and set the register value to 0b simultaneously.

39.3.2.7 CSI Receive Window Register (CSIm_CSI_IFIFO) (m = 0 to 5)

This register is a window register used to read data in the receive FIFO buffer. Every time this register is read, the read pointer is moved to read the latest data input to the receive FIFO buffer. The contents of this register are valid when the receive FIFO Level Indicate Register (CSI_IFIFO) is not 0. When the serial data length is 8 bits (CCL=0b in the CSI_MOE register) use the lower 8 bits. When the serial data length is 16 bits (CCL=1b in the CSI_MOE register) use the lower 16 bits.

Access Size: 32 bits

Address: <CSI0_S0_base> + 0018h
<CSI1_S0_base> + 0018h
<CSI2_S0_base> + 0018h
<CSI3_S0_base> + 0018h
<CSI4_S0_base> + 0018h
<CSI5_S0_base> + 0018h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IFIFO[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 39.3-8 CSIm_CSI_IFIFO Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15 to 0	IFIFO[15:0]	Rx FIFO register data. Writing is invalid.

39.3.2.8 CSI Transmit Window Register (CSIm_CSI_OFIFO) (m = 0 to 5)

This register is a window register used to write data to the transmit FIFO buffer. Every time data is written to this register, the write pointer is moved and the transmit data is stored. If DMA transfer is not used, read the CSI transmit window register (CSI_OFIFOL register) to confirm that the transmit FIFO buffer is not full before writing. When the serial data length is 8 bits (CCL=0b in the CSI_MOE register) use the lower 8 bits. When the serial data length is 16 bits (CCL=1b in the CSI_MOE register) use the lower 16 bits.

Access Size: 32 bits

Address: <CSI0_S0_base> + 001Ch
<CSI1_S0_base> + 001Ch
<CSI2_S0_base> + 001Ch
<CSI3_S0_base> + 001Ch
<CSI4_S0_base> + 001Ch
<CSI5_S0_base> + 001Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OFIFO[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W	R0W	R0W	R0W	R0W	R0W	R0W	R0W	R0W	R0W	R0W	R0W	R0W	R0W	R0W	R0W

Table 39.3-9 CSIm_CSI_OFIFO Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15 to 0	OFIFO[15:0]	Tx FIFO register data. These bits are read as 0b.

39.3.2.9 CSI FIFO Trigger Level Register (CSIm_CSI_FIFOTRG) (m = 0 to 5)

This register sets the trigger level of the transmit FIFO buffer and the receive FIFO buffer. If the receive FIFO trigger level setting is valid (R_TRGEN=1b in the CSI_CNT register), the R_TRG[2:0] bit setting is valid. And if the transmit FIFO trigger level setting is valid (T_TRGEN=1 in the CSI_CNT register), the T_TRG[2:0] bit setting is valid.

Access Size: 32 bits

Address: <CSI0_S0_base> + 0020h
<CSI1_S0_base> + 0020h
<CSI2_S0_base> + 0020h
<CSI3_S0_base> + 0020h
<CSI4_S0_base> + 0020h
<CSI5_S0_base> + 0020h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	T_TRG[2:0]			—	—	—	—	—	R_TRG[2:0]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 39.3-10 CSIm_CSI_FIFOTRG Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 11	—	Reserved. These bits are read as 0b. The write value should always be 0b.
10 to 8	T_TRG[2:0]	Set the free space of the transmit FIFO buffer as a trigger level. Used for timing control of the transmit trigger level interrupt and the transmit DMA transfer request signal (DMAREATX) output.
7 to 3	—	Reserved. These bits are read as 0b. The write value should always be 0b.

Table 39.3-10a

	Serial data length	
T_TRG	8 bits	16 bits
000b	8 bits × 1	16 bits × 1
001b	8 bits × 2	16 bits × 2
010b	8 bits × 4	16 bits × 4
011b	8 bits × 8	16 bits × 8
100b	8 bits × 16	16 bits × 16
101b	8 bits × 32	Prohibited*1
110b	Prohibited*1	Prohibited*1
111b	Prohibited*1	Prohibited*1

Table 39.3-10 CSIm_CSI_FIFOTRG Register Contents (2/2)

Bit Position	Bit Name	Description
2 to 0	R_TRG[2:0]	Set the free space of the receive FIFO buffer as a trigger level. Used for timing control of the receive trigger level interrupt and the receive DMA transfer request signal (DMAREQRX) output.

Table 39.3-10b

	Serial data length	
R_TRG	8 bits	16 bits
000b	8 bits × 1	16 bits × 1
001b	8 bits × 2	16 bits × 2
010b	8 bits × 4	16 bits × 4
011b	8 bits × 8	16 bits × 8
100b	8 bits × 16	16 bits × 16
101b	8 bits × 32	Prohibited*1
110b	Prohibited*1	Prohibited*1
111b	Prohibited*1	Prohibited*1

Note 1. Do not set the corresponding value. Operation is not guaranteed if the setting is made.

39.4 Operation

The prefix (CSIm_) of the register names is omitted in this and subsequent sections.

39.4.1 Software Reset

This unit has a software reset (CSI reset) function by a register setting, in addition to a reset by the PRESETn signal.

While a reset by the PRESETn signal initializes all registers, a CSI reset clears the interrupt flag and the transmission and reception FIFO buffers. It also initializes the specified registers.

39.4.1.1 CSI Reset Function

A CSI reset occurs when the CSI software reset (CSIRST) bit of the CSI control register (CSI_CNT) is set. Clearing the CSIRST bit de-asserts the CSI reset.

The table below lists the pins and registers to be initialized by a CSI reset.

Table 39.4-1 Pins and Registers to be Initialized by a CSI Reset

Category	Pin Name or Register Name	Bit Name
Pins*1	SCKOE SCKO SOOE (*Fixed to 0 in reception mode)	
Registers*2	CSI_MODE	CSIE, CSOT
	CSI_CNT	T_FIFOF, R_FIFOF
	CSI_INT	UNDER, OVERF, TREND, CSIEND, T_TRGR, R_TRGR
	CSI_IFIFOL	RFL[5:0]
	CSI_OFIFOL	TFL[5:0]

Note 1. The SCKOE pin is at the low level during a CSI reset regardless of the operating mode setting. When the CSI reset is de-asserted, the output on this pin goes to the level that is dependent on the operating mode.

Note 2. Writing to the above registers has no effect during a CSI reset (i.e., while CSIRST is 1b).
When writing to these registers, only do so after the CSI reset has been de-asserted (i.e., CSIRST is set to 0b).

The registers other than those listed in **Table 39.4-1** are not initialized by a CSI reset but retain their values.

Since there registers retain the initial settings required for communications, operation can be restarted without re-setting them after the CSI reset has been de-asserted.

39.4.1.2 Notes on Using a CSI Reset

Applying a CSI reset while operations for communications are in progress may disrupt communications in a way that affects operations by the other party.

To apply a CSI reset, clear the CSIE flag in the CSI mode control register (CSI_MODE) and check that communications have been stopped (the CSOT flag is 0b) by reading the CSI mode control register (CSI_MODE).

Similarly, applying a CSI reset during transmission or reception with the aid of DMA transfer may place the CSI in an unexpected state. When applying a CSI reset while DMA transfer is in use, only do so after having confirmed that DMA transfer has stopped.

39.4.2 Starting and Stopping Communications

Communications are started and stopped by using the CSIE flag of the CSI mode control register (CSI_MODE).

Operations for communications are started when the flag is set and stopped when the flag is cleared.

The state of communications can be checked by reading the CSOT flag of the CSI mode control register (CSI_MODE).

If the CSIE is cleared during the cycle of communications, operations for communications are not stopped immediately but are stopped after a wait for the completion of this cycle. Accordingly, poll the CSOT flag to check that communications have been stopped before proceeding with processing after stopping communications.

Only the registers and register bits listed below are writable while operations for communications are in progress.

Table 39.4-2 List of the Registers and Flags which are Writable during Operations for Communications

Register Name	Flag
CSI_MODE	CSIE
CSI_CNT	Interrupt enable flag (bits 0:13)
CSI_INT	All
CSI_OFIFO	All

39.4.2.1 Notes on Using the CSIE Flag

Changing the settings of the registers other than those listed in **Table 39.4-2**, and which set the operating mode, communications data format, communications speed, or trigger level, is prohibited during operations for communications.

When changing the settings after starting communications, only do so after stopping communications.

The initial settings must be made before starting communications after the CSI reset has been de-asserted. Specifically, the initial settings for both master and slave must be completed before starting communications.

39.4.3 Setting the Communications Function

39.4.3.1 Format of Serial Data

This unit can comply with four serial data formats by settings.

The CCL and DIR flags of the CSI mode control register (CSI_MODE) are used to make the settings.

Set the following items such that the conditions for the master are the same as those for the slave.

- Serial data length (CCL):
  Select 8 or 16 bits as the serial data length.
- First bit of serial data (DIR):
  Select MSB or LSB for the first bit of serial data.

39.4.3.2 Serial Clock Timing

This unit can comply with four serial clock timings by settings.

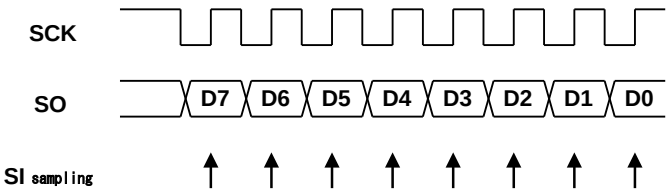
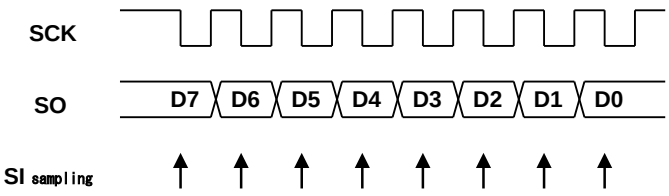
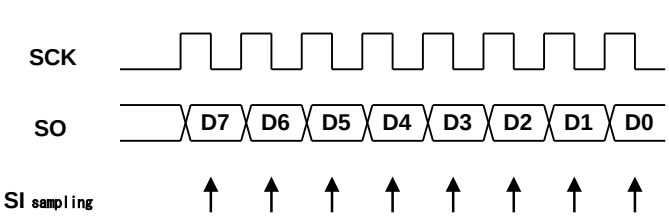
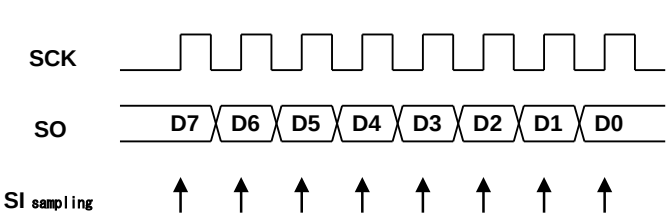
The CKP and DAP flags of the CSI clock select register (CSI_CLKSEL) are used to make the settings.

Set the following items such that the conditions for the master are the same as those for the slave.

- Polarity of the serial clock in the idle state (CKP):
  Select the polarity of the serial clock in the idle state as the high or low level.
- Phase of serial data (DAP):
  For SO, select the same phase as that of SCK or the phase half a cycle before that of SCK.

Table 39.4-3 shows the timing of operations by the combination of the values of the polarity selection bit (CKP) while the serial clock is idle and the phase selection bit for serial data (DAP).

Table 39.4-3 Polarity of the Clock and the Phase of Data

CKP Bit	DAP Bit	Operation Timing
0	0	
0	1	
1	0	
1	1	

Note: The setting of the polarity selection bit (CKP) for the serial clock must match the clamp level of the SCK signal line.
- SCK is clamped at the high level: CKP ← 0b
- SCK is clamped at the low level: CKP ← 1b

39.4.3.3 Interval Time between Serial Data Communications

The serial clock and serial data are seamlessly transferred during continuous data transfer.

If the communications speed is too high, processing may not proceed in time. This depends on the connected slave. For communications with such slaves, an interval can be provided between the units of serial data.

An interval time is set by using the DATWT[3:0] bits of the CSI mode control register (CSI_MODE).

Specifically, an interval equivalent to 0 to 15 clock cycles of the serial clock (SCKO) can be inserted through the setting of DATWT[3:0].

The figure below shows the timing when DATWT[3:0] = 0 and DATWT[3:0] = 4.

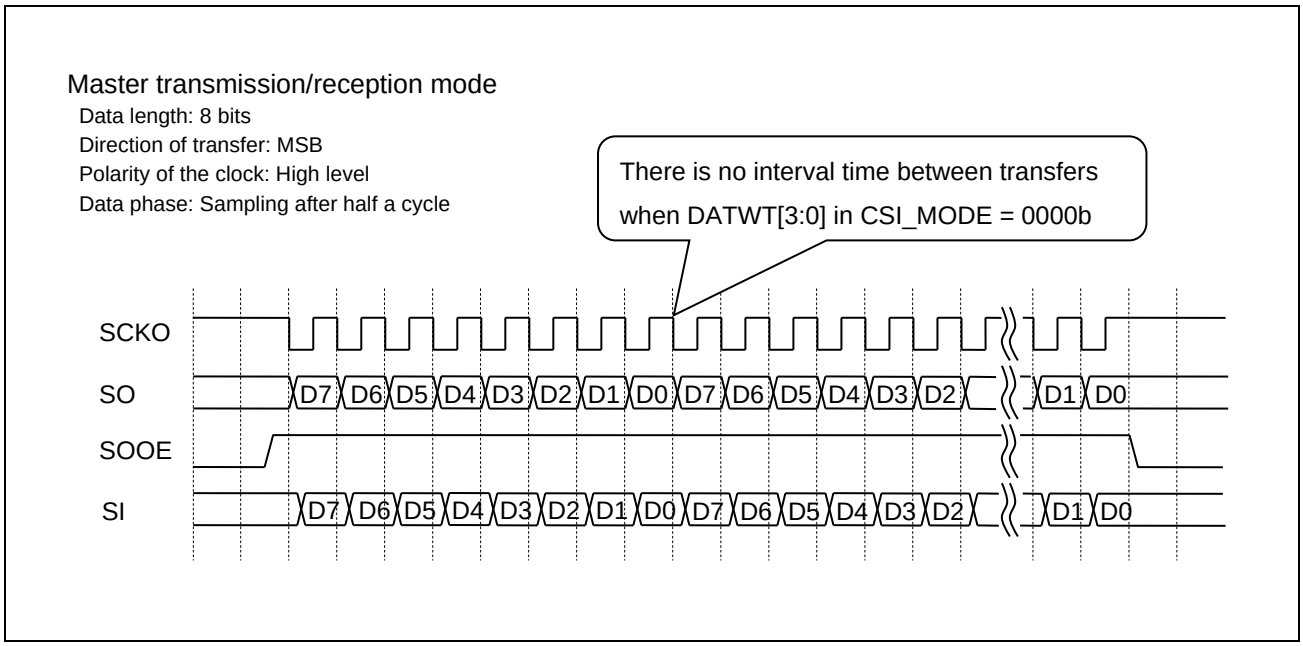


Figure 39.4-1 Interval Time Timing (when DATWT[3:0] = 0000b)

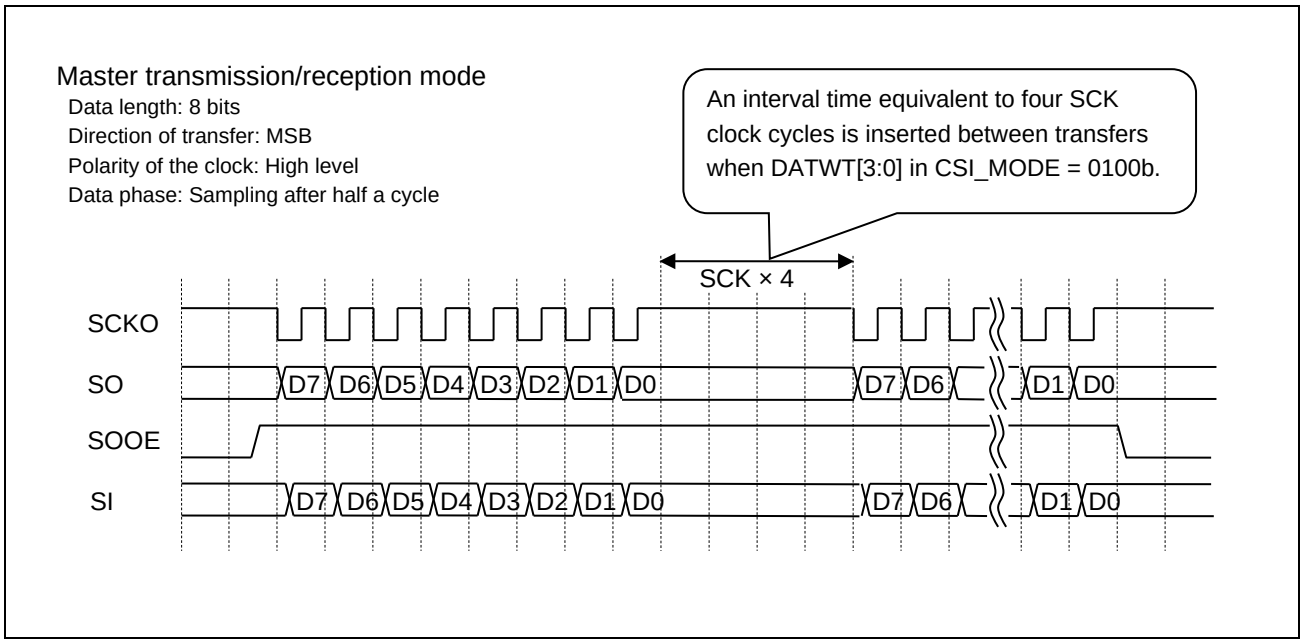


Figure 39.4-2 Interval Time Timing (when DATWT[3:0] = 0100b)

39.4.3.4 Slave Selection Signal Function and Setting

The slave selection signal can be used for operation in slave reception-only mode and slave transmission/reception mode.

This signal is used to select a slave for communications with the master in the system in which multiple slaves are connected to one master.

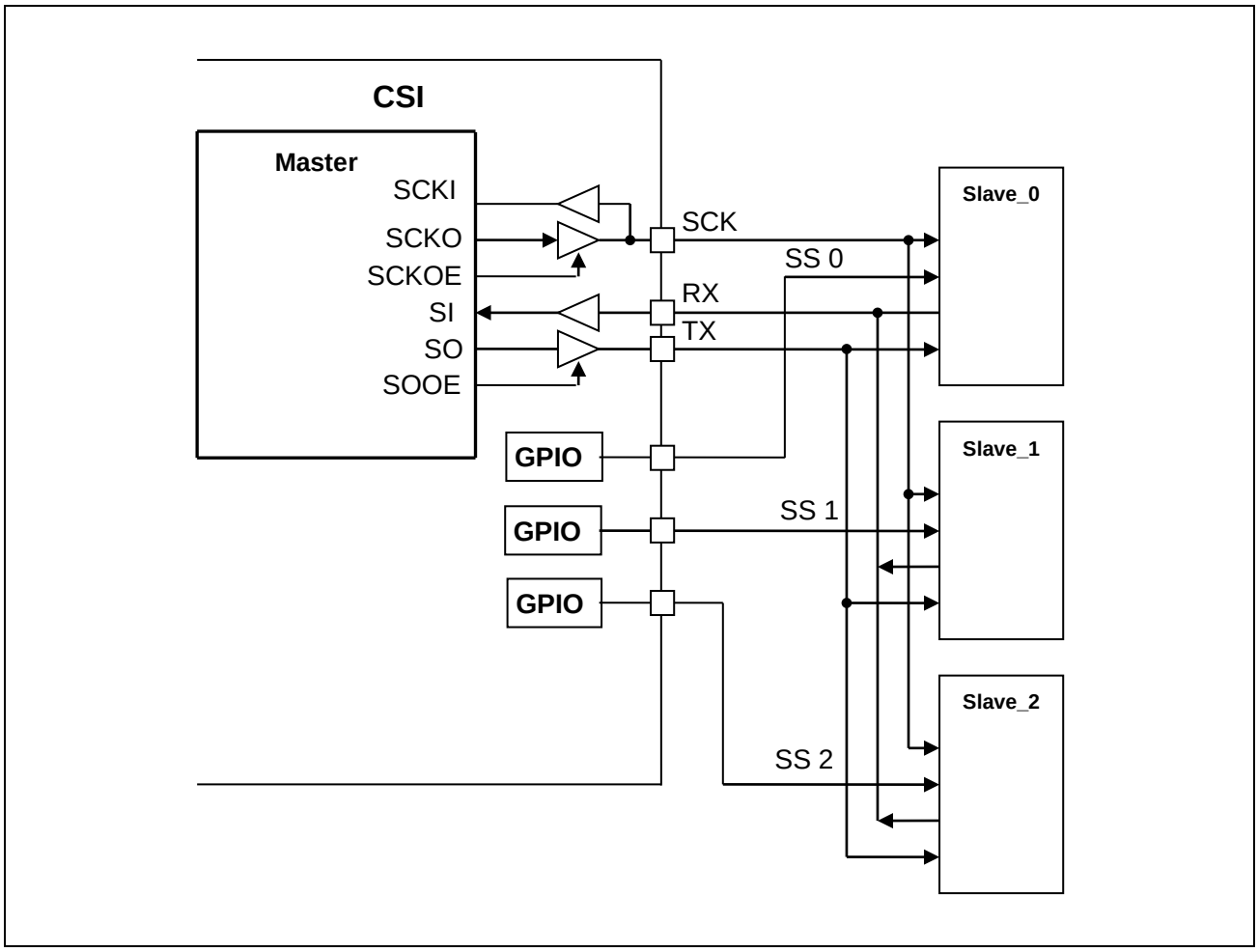


Figure 39.4-3 Example of Connections between the Master and Three Slaves

As shown in **Figure 39.4-3**, the master generates the slave selection signal by using a general-purpose port (GPIO), etc.

The master activates the slave selection signal of the other party before starting operations for communications and deactivates the slave selection signal before switching to communications with another slave.

The slave handles operations for communications based on the received serial clock signal while the slave selection signal is active.

The slave selection signal is set by using the SS_ENA and SS_POL flags of the CSI clock select register (CSI_CLKSEL).

The table below gives the functional operations corresponding to the settings of these flags.

Table 39.4-4 Functional Operations of the Slave Selection Pin

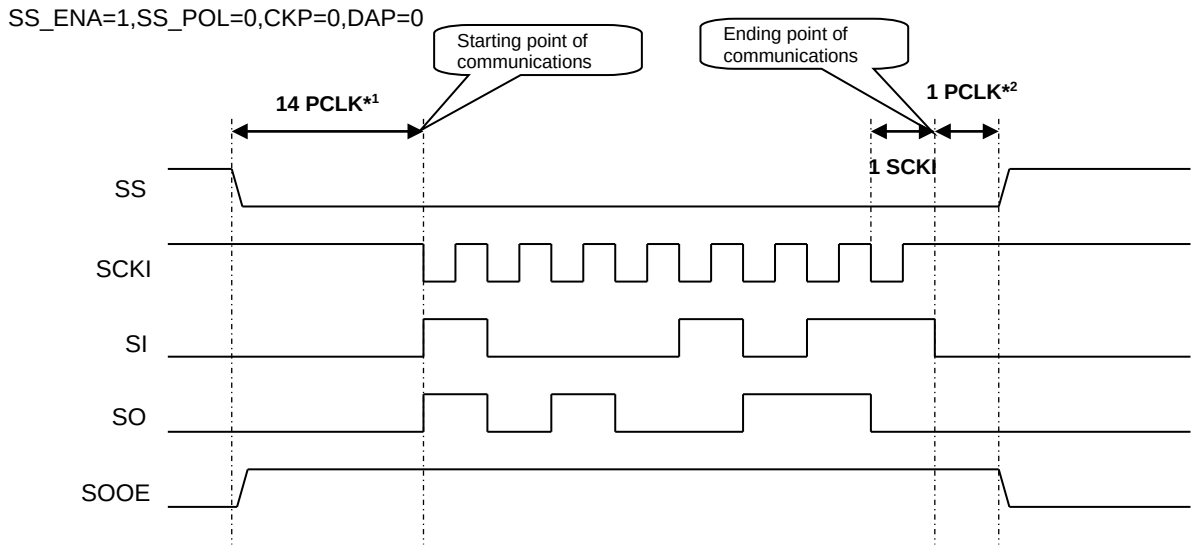
SS_ENA	SS_POL	Operation
0b	X	• This setting is for one-to-one use of the master and slave. • The slave's communications function is always active regardless of the signal level of the SS pin. • Transmission/reception or reception starts in response to input of the serial clock (SCKI). • In transmission/reception mode, the SOOE pin is always active.*1
1b	0b	• When the SS pin is at the low level, the slave's communications function is active. • Operation corresponds to the serial clock (SCKI while the SS pin is at the low level. In transmission/reception mode, the SOOE pin is active*1 while the SS pin is at the low level.
1b	1b	• The slave's communications function is active when the SS pin is at the high level. • Operation corresponds to the serial clock (SCKI while the SS pin is at the high level. In transmission/reception mode, the SOOE pin is active*1 while the SS pin is at the high level.

Note 1. This pin is not active if the operations for communications are stopped (CSIE = 0b).

The slave handles operations for communications with the serial clock from the master. Accordingly, the slave selection signal must retain the active level while operations for communications are in progress.

Care should be taken with the following timing when the slave selection signal is generated.

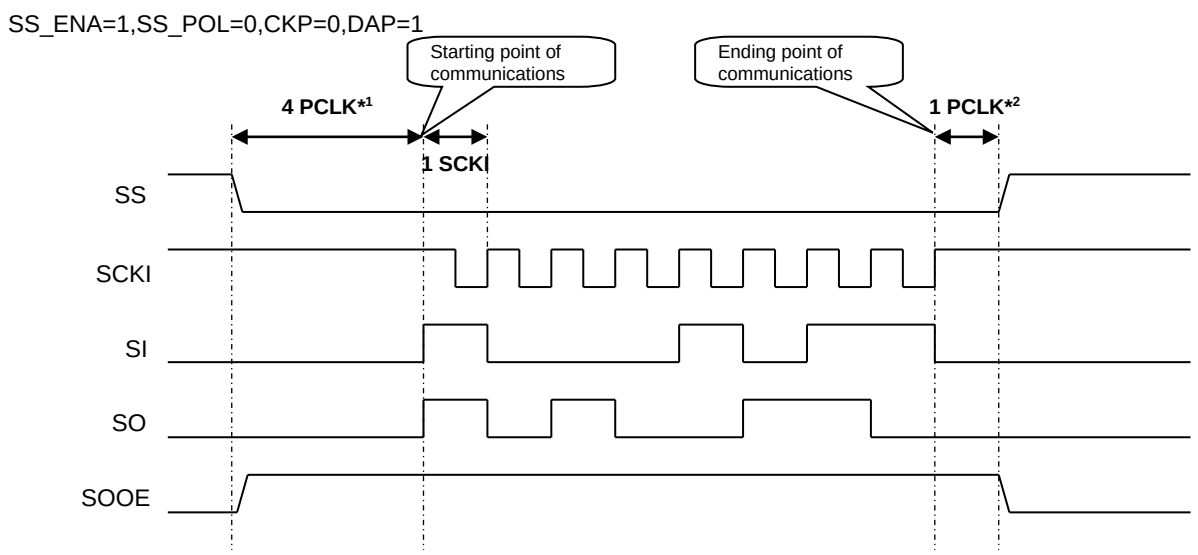
The timing differs with the setting for the phase of serial data (DAP).



Note 1. The master must activate the slave selection signal four or more PCLK cycles before starting communications. The starting point of communications depends on the setting of DAP (at the rising edge in Figure 39.4-4).

Note 2. At least one PCLK cycle of the hold time must be secured until the slave selection signal is deactivated following the completion of communications.

Figure 39.4-4 Slave Selection Signal Control Timing (when DAP = 0 for Slave)



Note 1. The master must activate the slave selection signal four or more PCLK cycles before starting communications. The starting point of communications depends on the setting of DAP (half a clock cycle before the falling edge of SCKI in **Figure 39.4-5**).

Note 2. At least one PCLK cycle of the hold time must be secured until the slave selection signal is deactivated following the completion of communications.

Figure 39.4-5 Slave Selection Signal Control Timing (when DAP = 1b for Slave)

39.4.4 Interrupt

The CSI interrupt signal (CSIINT) is provided as an interrupt output signal.

CSIINT is a level interrupt.

Clearing the interrupt source flag in the CSI interrupt status register (CSI_INT) deactivates the interrupt signal.

There are six interrupt sources listed below. The interrupt sources can be masked individually.

Table 39.4-5 List of Interrupt Sources

Interrupt Source	Flag Name	Function
Underrun error interrupt	UNDER	This interrupt occurs when the request for transmission is received while data for transmission have not been prepared in the transmission FIFO, i.e. it is empty. For details, see **Section 39.4.5.2, Underrun Error**.
Overflow error interrupt	OVERF	This interrupt occurs when reception proceeds while the reception FIFO has no space. For details, see **Section 39.4.5.1, Overflow Error**.
All transmission completed interrupt	TREND	An all transmission completed interrupt occurs when all data for transmission in the transmission FIFO have been transmitted. This interrupt does not occur in master reception-only mode and slave reception-only mode.
Transfer completed interrupt	CSIEND	A transfer completed interrupt occurs when reception or transmission/reception of a single unit of data is completed. Operations for communications continue even if the transfer completed interrupt occurs.
Tx trigger level interrupt	T_TRGR	This interrupt occurs when the free space of the transmission FIFO reaches the specified trigger level due to the operation for transmission. For details, see **Section 39.4.11.1, Transmission Trigger Level**.
Rx trigger level interrupt	R_TRGR	This interrupt occurs if the buffering level of the reception FIFO reaches the specified trigger level due to the operation for reception. For details, see **Section 39.4.11.2, Reception Trigger Level**.

39.4.4.1 All Transmission Completed Interrupt

An all transmission completed interrupt (TREND) occurs when all data for transmission in the transmission FIFO have been transmitted.

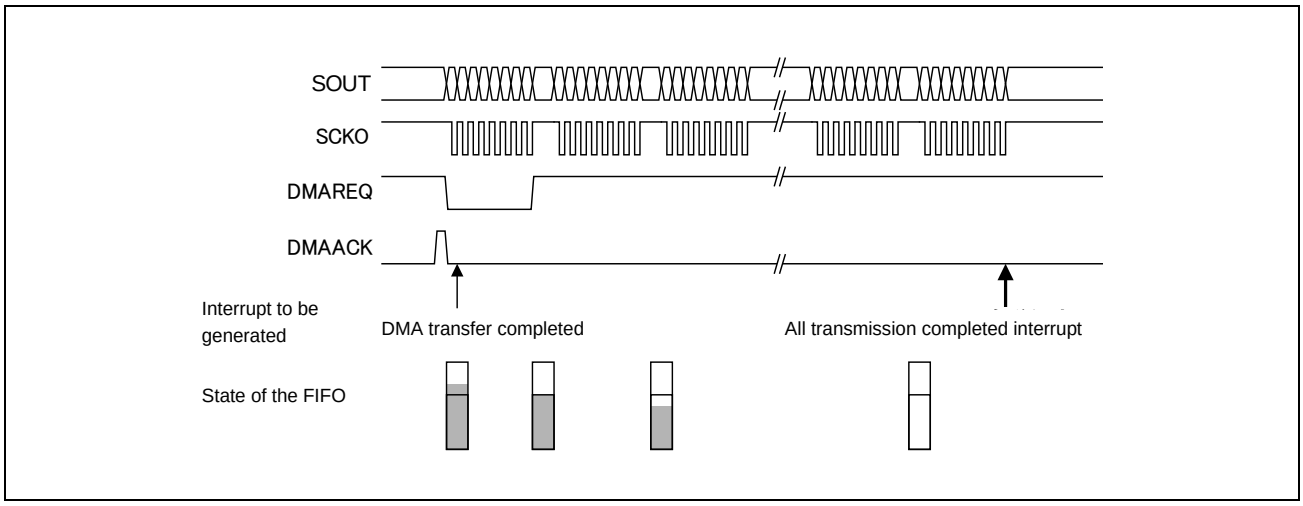


Figure 39.4-6 CSI All Transmission Completed Interrupt

However, as shown in **Figure 39.4-7**, even if an all transmission completed interrupt occurs, writing to the transmission FIFO by the DMAC may proceed after that and data for transmission may remain in the transmission FIFO.

When transmission is to be completed by the handler for the all transmission completed interrupt, check whether data for transmission remain in the transmission FIFO.

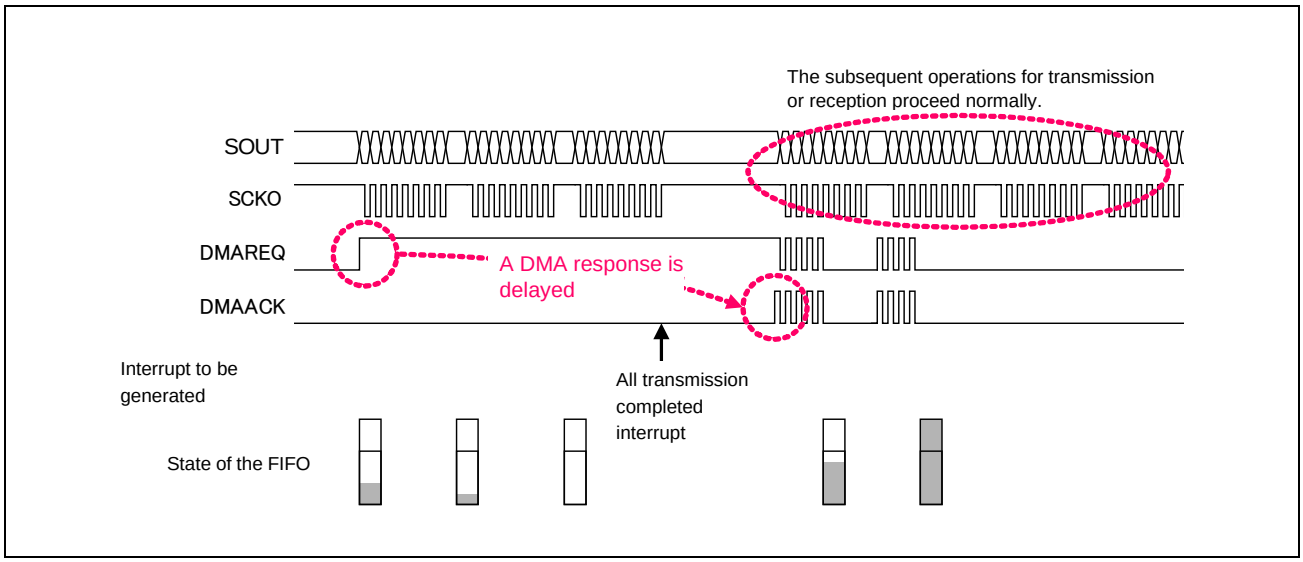


Figure 39.4-7 CSI All Transmission Completed Interrupt

39.4.5 Operation and Procedure for Processing when an Error Occurs

The CSI detects two errors: an overflow error in reception and an underrun error in transmission.

39.4.5.1 Overflow Error

An overflow error occurs when reception proceeds while the reception FIFO buffer has no space.

An overflow error may occur in master transmission/reception mode, in slave reception-only mode, or in slave transmission/reception mode.

In master reception-only mode, an overflow error does not occur because communications are stopped before the buffer overflows.

If an overflow error occurs, subsequent data for reception are not captured. Note, however, that transmission which is proceeding at the same time is not stopped in master transmission/reception mode or in slave transmission/reception mode.

Reception is restarted when data have been read from the reception FIFO buffer or the overflow interrupt source flag is cleared after flushing of the buffer to make space in it.

An overflow can be detected by the interrupt signal.

For recovery from communications errors due to overflows, create a protocol in software to be triggered by the interrupt.

39.4.5.2 Underrun Error

An underrun error occurs when the request for transmission is received while data for transmission have not been prepared in the transmission FIFO, i.e. it is empty.

An underrun error may only occur in slave transmission/reception mode.

If an underrun error occurs, transmission as well as reception is stopped.

The master receives 0-valued data because the serial data output (SO) pin is at the low level while transmission is stopped.

Data for reception which are transmitted from the master following an error are not captured because reception is stopped.

To restart operation, a CSI reset (CSIRST in the CSI_CNT register = 1b) is used. Follow the procedure below to restart operation.

1. Assert the CSI reset signal.
2. De-assert the CSI reset signal.
3. Write data for transmission to the transmission FIFO.
4. Start communications (CSIE in CSI_MODE = 1b).

An underrun error can be detected by the interrupt signal.

For recovery from communications errors due to underrun errors, create a protocol in software to be triggered by the interrupt.

39.4.6 Operating Mode

This unit has four operating modes listed below.

The operating mode must be determined by a register setting at start-up.

- Master reception-only mode
- Master transmission/reception mode
- Slave reception-only mode (default at the time of a reset)
- Slave transmission/reception mode

The operating mode is set with a combination of two flags, the SLAVE flag of the CSI clock select register (CSI_CLKSEL) and the TRMD flag of the CSI mode control register (CSI_MODE).

The operating mode should be set before starting communications after release from the reset state. The setting cannot be changed during communications (while CSIE = 1 or CSOT = 1 in the CSI_MODE register).

Table 39.4-6 List of Operation Modes

CSI_CLKSEL SLAVE (Bit 15)	CSI_MODE TRMD (Bit 6)	Operating Mode	Functional Overview
0b	0b	Master reception-only mode	This mode is dedicated for reception to receive data from a slave.
0b	1b	Master transmission/reception mode	In this mode, transmission and reception to and from a slave proceed simultaneously.
1b	0b	Slave reception-only mode	This mode is dedicated for reception to receive data transmitted from the master (default at the time of a reset).
1b	1b	Slave transmission/reception mode	In this mode, transmission and reception of data to and from the master proceed simultaneously.

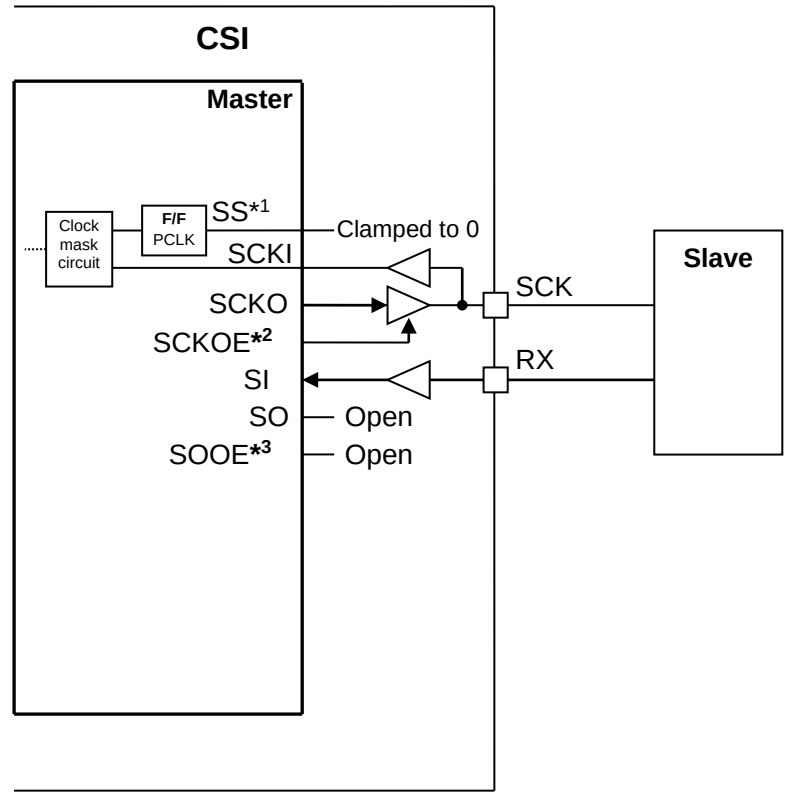
39.4.7 Master Reception-only Mode

This mode is dedicated for reception to receive data from a slave.

The transmission function is not used.

The master outputs the serial clock (SCK) along with operation for reception and receives serial data which are transmitted from a slave.

Figure 39.4-8 shows an example of one-to-one connection with a slave.



Note 1. The state of the SS pin is ignored.

Note 2. SCKOE always outputs the high level.

Note 3. SOOE always outputs the low level.

Figure 39.4-8 Example of Connection in Master Reception-only Mode

39.4.7.1 Setting Items in Master Reception-only Mode

The table below lists the registers to be set in master reception-only mode.

Table 39.4-7 List of the Registers to be Set in Master Reception-only Mode

*1	Register Name	Bit Name	Bit	Setting
[R]	CSI_MODE	Communications mode: TRMD	6	0b (reception only)
[R]		Serial data length: CCL	5	Select 16 bits or 8 bits. The data length for the slave and that for the master must match.
[R]		First bit: DIR	4	Select MSB or LSB. The first bit settings for the slave and master must match.
[R]		Interval time: DATWT	19:16	Set an appropriate value as required. See **Section 39.4.3.3, Interval Time between Serial Data Communications**.
[R]	CSI_CLKSEL	Operating mode: SLAVE	15	0b (master)
[R]		Polarity of the clock: CKP	17	The setting must match the clamp level of the SCK signal line.
[R]		Data phase: DAP	16	Select the phase of serial data. It must match the data phase selection by the master.
[R]		Communications clock selection: CKS	14:1	Determines the communications frequency of SCK.
[O]	CSI_CNT	DMA transfer for reception: R_DMAEN	16	Determines the method for transfer of received data.
[O]		Reception FIFO trigger level: R_TRGEN	19	Determines use of the reception FIFO trigger level.
[O]		Transfer completed interrupt: CSIEND_E	8	Determines use of the transfer completed interrupt.
[O]		Reception trigger level interrupt: R_TRGR_E	0	Determines use of the reception trigger level interrupt.
[O]	CSI_FIFOTRG	Reception FIFO trigger level: R_TRG	2:0	Determines the level value when the reception FIFO trigger level is used.

Note 1. [R]: Required setting items.
[O]: Optional. Set these items as required.

39.4.7.2 Operation in Master Reception-only Mode

(1) How to Start Operation

After the initial settings, setting the startup flag for communications (the CSIE bit in CSI_MODE) starts reception

(2) How to End Operation

Clearing the startup flag for communications (the CSIE bit in CSI_MODE) stops reception.

If the startup flag is cleared during the reception cycle, transmission or reception is stopped after the completion of the cycle.

(3) Operation during Communications

When the reception FIFO buffer has no space, output of the serial clock SCK is stopped and overall operation for reception is stopped.

Reception is restarted when data have been read from the reception FIFO and the FIFO has space.

(4) Reception Trigger Level Interrupt

A reception trigger level interrupt can be used. For details of the reception trigger level, see **Section 39.4.11.2, Reception Trigger Level**.

If received data are accumulated to the value set in R_TRG[2:0] of the CSI FIFO trigger level register (CSI_FIFOTRG), a reception trigger level interrupt occurs and reception is stopped.

Reception is restarted when the reception trigger level interrupt source flag (R_TRGR) in the CSI_INT register is cleared by reading the data from the reception FIFO.

(5) Communications Error

No error occurs in master reception-only mode.

39.4.7.3 Settings in Master Reception-only Mode and Flow of Operations

The figure below shows a flow of operations for reception with the use of the reception trigger level interrupt in master reception-only mode.

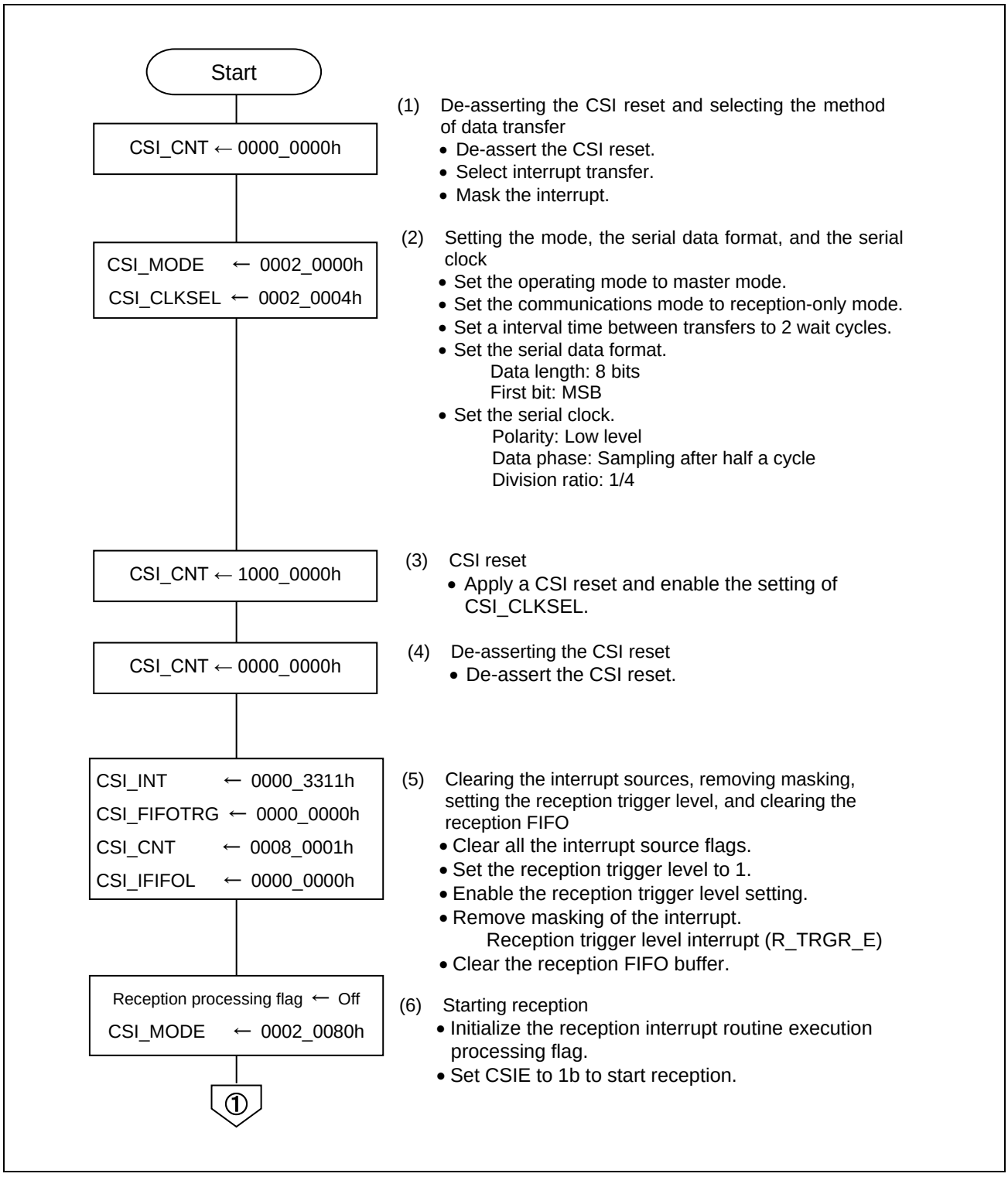


Figure 39.4-9 Flow of Operations with Interrupt Transfer in Master Reception-only Mode (1/3)

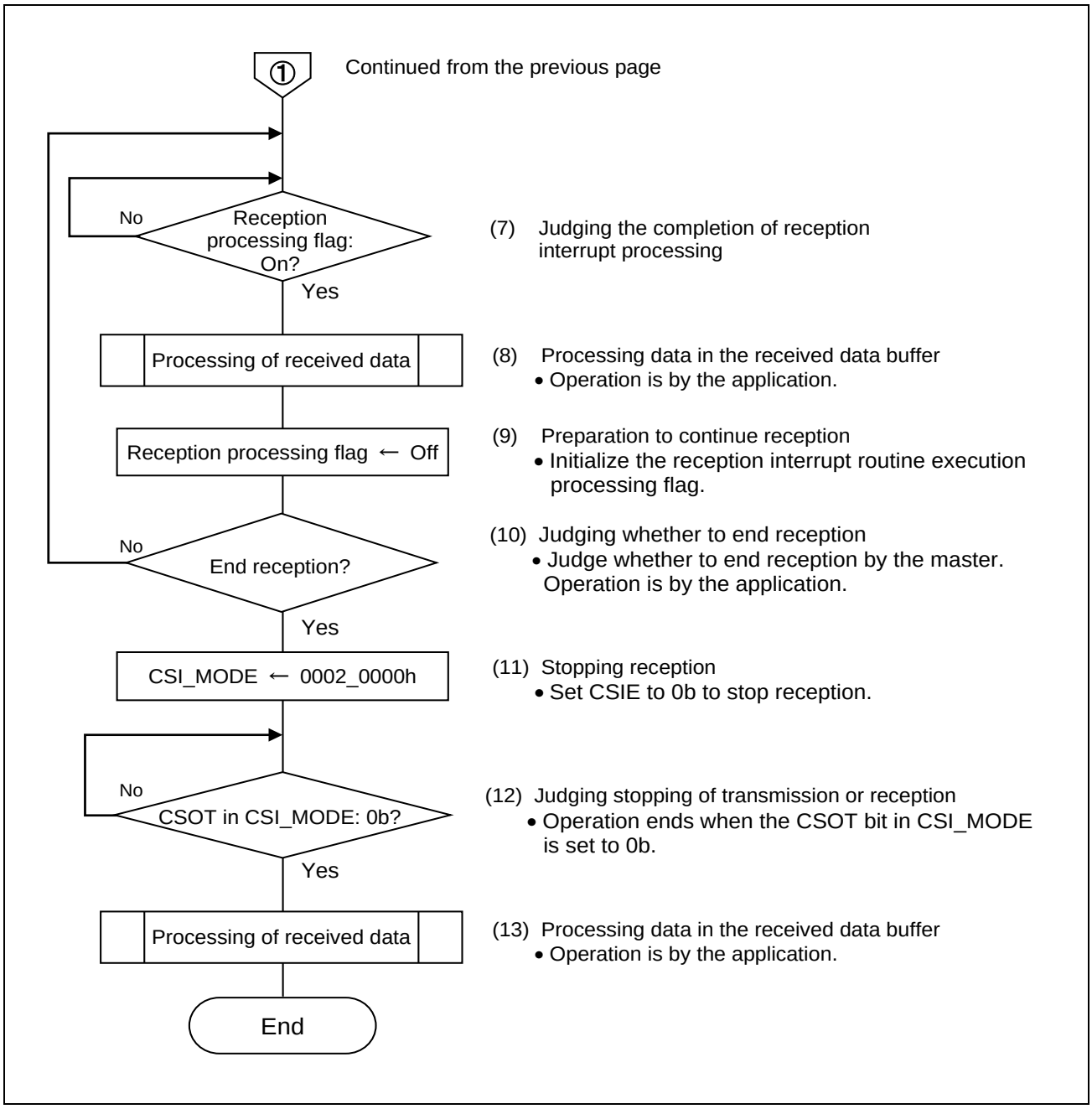


Figure 39.4-9 Flow of Operations with Interrupt Transfer in Master Reception-only Mode (2/3)

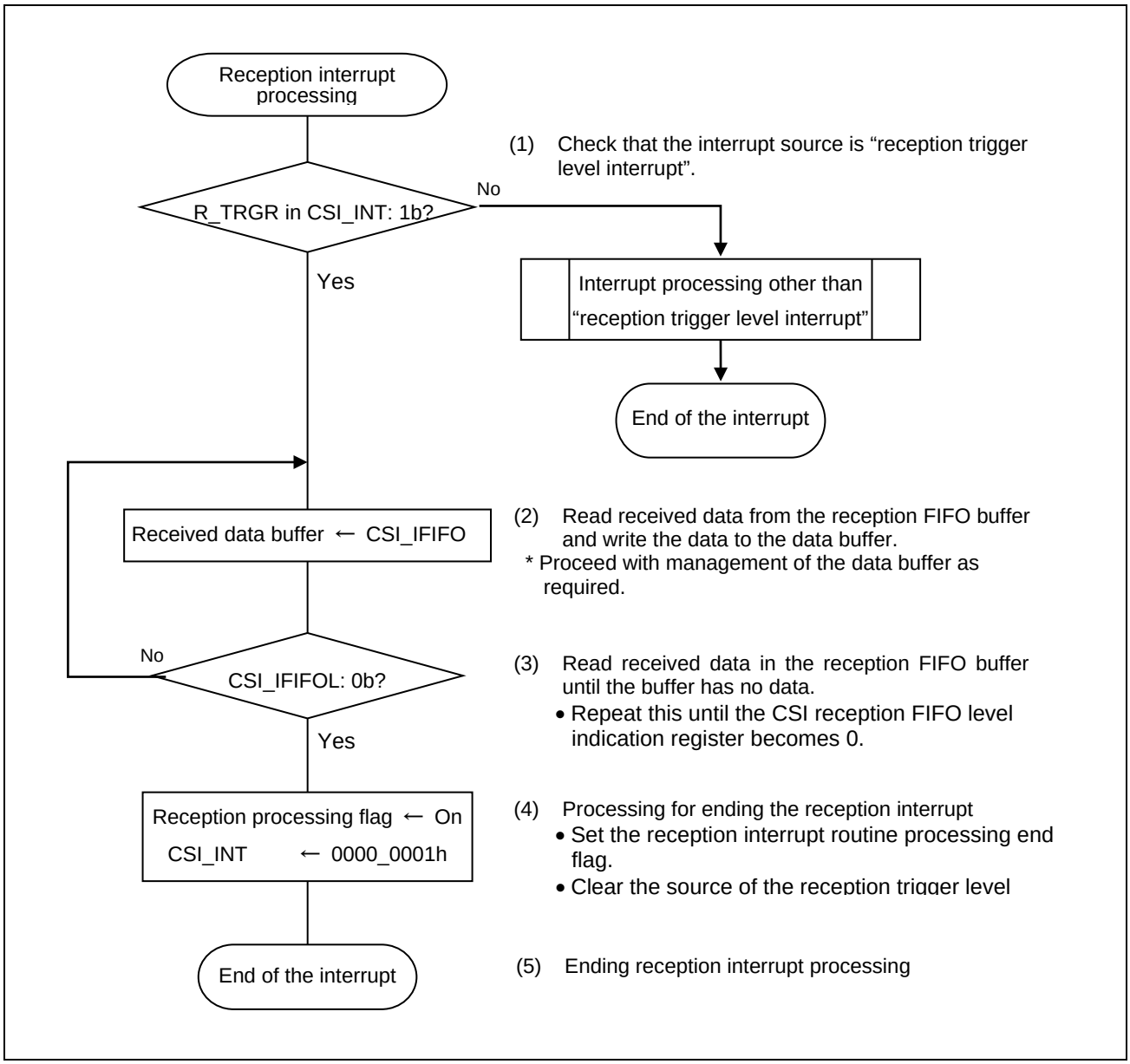


Figure 39.4-9 Flow of Operations with Interrupt Transfer in Master Reception-only Mode (3/3)

39.4.8 Master Transmission/Reception Mode

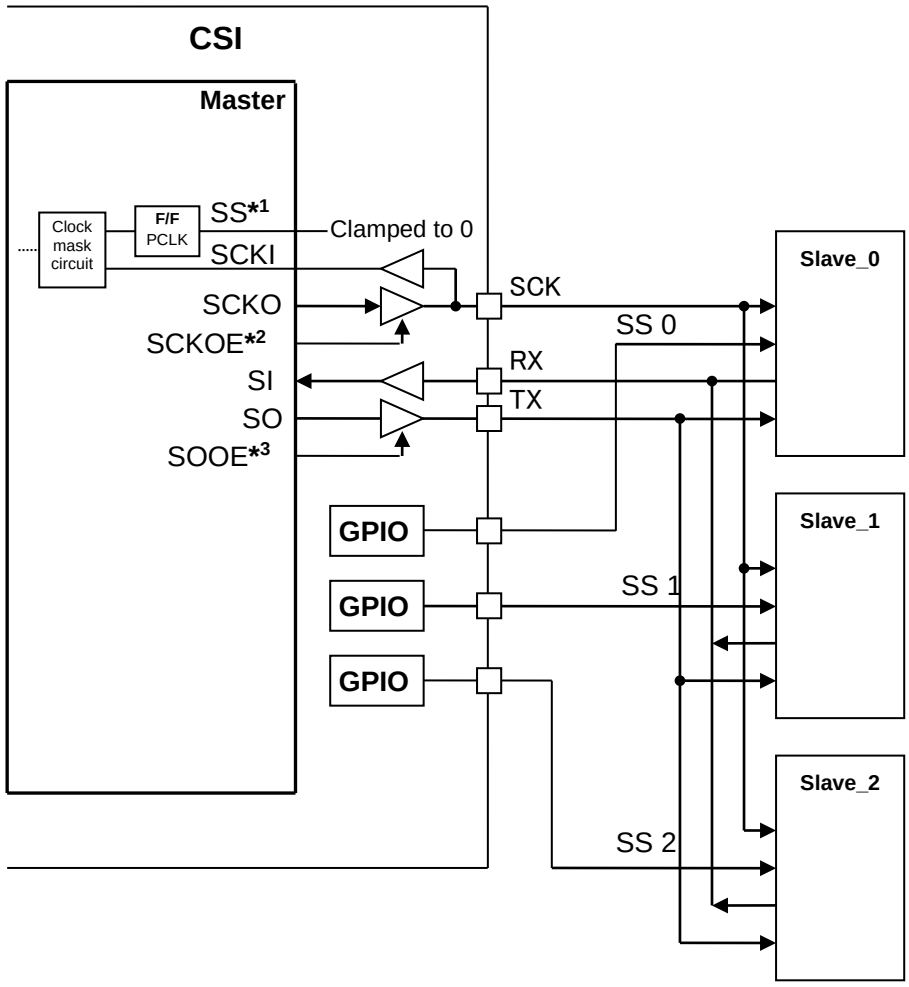
In this mode, transfer to and from a slave proceeds.

It allows high-speed communications since transmission and reception proceed simultaneously.

The master outputs the serial clock (SCK) during transfer.

Operation must be in this mode even when the transmission function is only used and the reception function is not used.

Figure 39.4-10 shows an example of connection with multiple slaves.



Note 1. The state of the SS pin is ignored.

Note 2. SCKOE always outputs the high level.

Note 3. SOOE outputs the high level while the serial clock is output.

Figure 39.4-10 Example of Connection in Master Transmission/Reception Mode (Connection with Multiple Slaves)

39.4.8.1 Setting Items in Master Transmission/Reception Mode

The table below lists the registers to be set in master transmission/reception mode.

Table 39.4-8 List of the Registers to be Set in Master Transmission/Reception Mode

*1	Register Name	Bit Name	Bit	Setting
[R]	CSI_MODE	Communications mode: TRMD	6	1b (transmission/reception mode)
[R]		Serial data length: CCL	5	Select 16 bits or 8 bits. The data length for the slave and that for the master must match.
[R]		First bit: DIR	4	Select MSB or LSB. The first bit settings for the slave and master must match.
[R]		Interval time: DATWT	19:16	Set an appropriate value as required. See **Section 39.4.3.3, Interval Time between Serial Data Communications**..
[R]	CSI_CLKSEL	Operating mode: SLAVE	15	0b (master)
[R]		Polarity of the clock: CKP	17	The setting must match the clamp level of the SCK signal line.
[R]		Data phase: DAP	16	Select the phase of serial data. It must match the data phase selection by the master.
[R]		Communications clock selection: CKS	14:1	Determines the communications frequency of SCK.
[O]	CSI_CNT	DMA transfer for transmission: T_DMAEN	24	Determines the method for transfer of data for transmission.
[O]		Transmission FIFO trigger level: T_TRGEN	27	Determines use of the transmission FIFO trigger level.
[O]		DMA transfer for reception: R_DMAEN	16	Determines the method for transfer or received data.
[O]		Reception FIFO trigger level: R_TRGEN	19	Determines use of the reception FIFO trigger level.
[O]		All transmission completed interrupt: TREND_E	9	Determines use of the all transmission completed interrupt.
[O]		Overflow interrupt: OVERF_E	12	Determines use of the overflow interrupt.
[O]		Transfer completed interrupt: CSIEND_E	8	Determines use of the transmission completed interrupt.
[O]		Transmission trigger level interrupt: T_TRGR_E	4	Determines use of the transmission trigger level interrupt.
[O]		Reception trigger level interrupt: R_TRGR_E	0	Determines use of the reception trigger level interrupt.
[O]	CSI_FIFOTRG	Transmission FIFO trigger level: T_TRG	10:8	Sets the level value when the transmission FIFO trigger level is used.
[O]		Reception FIFO trigger level: R_TRG	2:0	Sets the level value when the reception FIFO trigger level is used.

Note 1. [R]: Required setting items
[O]: Optional. Set these items as required.

39.4.8.2 Operation in Master Transmission/Reception Mode

(1) How to Start Operation

After the initial settings, setting the startup flag for communications (the CSIE bit in CSI_MODE) and writing data for transmission to the transmission FIFO starts operations for transmission and reception.

If data for transmission have been written to the transmission FIFO before setting the startup flag, only setting the startup flag starts operations for transmission and reception.

(2) How to End Operation

Clearing the startup flag for communications (the CSIE bit in CSI_MODE) stops operations for transmission and reception.

Even if data for transmission remain in the transmission FIFO at the time the startup flag is cleared, operations for transmission and reception are stopped.

Clearing the startup flag after a wait until the communications state flag indicates stopping of communications can prevent data from remaining in the transmission FIFO.

(3) Operation during Communications

Operations for transmission and reception proceed until the transmission FIFO buffer has no data.

When the transmission FIFO buffer has no data for transmission and the buffer is empty, output of the serial clock SCK is stopped and operations for transmission and reception are stopped.

When transmission and reception are stopped, writing data to the transmission FIFO restarts operations for transmission and reception.

Since transmission is main operation in operations for transmission and reception, transmission and reception are not stopped even if the reception FIFO becomes full during operation. In such cases, an overflow error occurs and subsequent data for reception are not captured.

For details of an overflow error, see **Section 39.4.5.1, Overflow Error**.

(4) Reception Trigger Level Interrupt

A reception trigger level interrupt can be used. For details, see **Section 39.4.11.2, Reception Trigger Level**.

This interrupt occurs when received data are accumulated to the value set in R_TRG of the CSI_FIFOTRG register.

Operations for transmission and reception continue even if the reception trigger level interrupt has occurred.

(5) Transmission Trigger Level Interrupt

A transmission trigger level interrupt can be used. For details, see **Section 39.4.11.1 Transmission Trigger Level**.

The transmission trigger level interrupt occurs when data in the transmission FIFO are reduced due to the operation for transmission and the free space increases to the value set in T_TRG.

Even if this interrupt occurs, operations for transmission and reception continue.

If the transmission trigger level interrupt is to be used, fill the transmission FIFO with data for transmission before starting communications in order to generate the first interrupt.

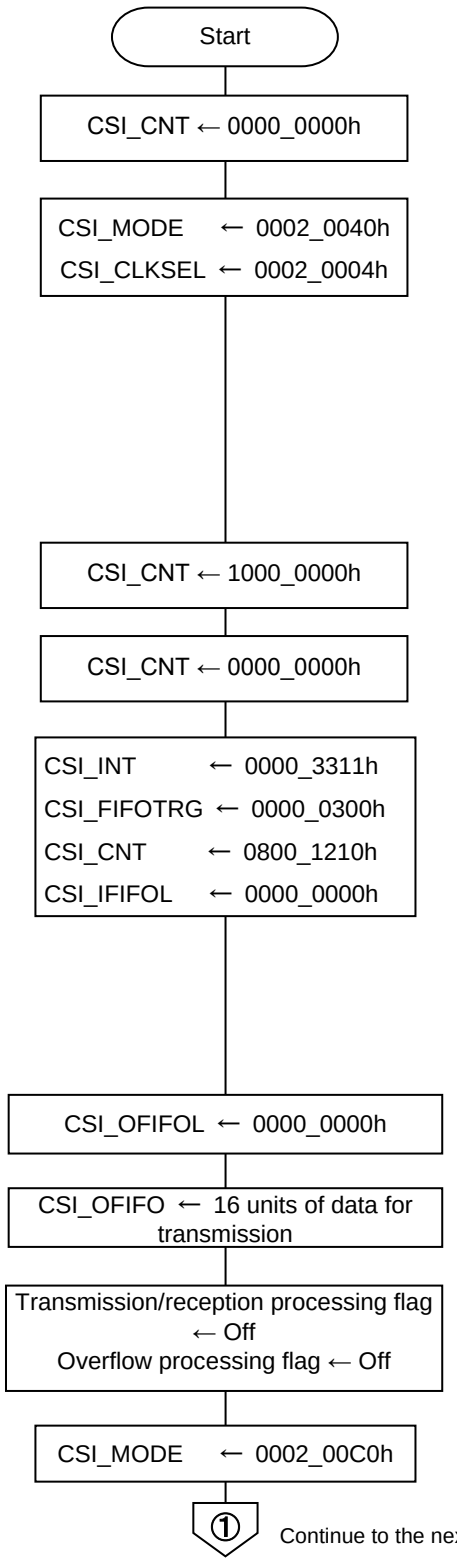
(6) Communications Error

An overflow error may occur.

39.4.8.3 Settings in Master Transmission/Reception Mode and Flow of Operations (for Transmission and Reception)

The figure below shows a flow of operations for transmission and reception with the use of the transmission trigger level interrupt in master transmission/reception mode.

Data for transmission prepared in the transmission buffer are continuously transferred with the use of the transmission trigger level interrupt and the all transmission completed interrupt.



(1) De-asserting the CSI reset and selecting the method of data transfer
- De-assert the CSI reset.
- Select interrupt transfer.
- Mask the interrupt.

(2) Setting the mode, the serial data format, and the serial clock
- Set the operating mode to master transmission/reception mode.
- Set a interval time between transfers to 2 wait cycles.
- Set the serial data format.
  Data length: 8 bits
  First bit: MSB
- Set the serial clock.
  Polarity: Low level
  Data phase: Sampling after half a cycle
  Division ratio: 1/4

(3) CSI reset
- Apply a CSI reset and enable the setting of CSI_CLKSEL.

(4) De-asserting the CSI reset

(5) Clearing the interrupt sources, removing masking, and setting the transmission trigger level
- Clear all the interrupt source flags.
- Set the transmission trigger level to 8.
- Enable the transmission trigger level setting.
- Remove masking of the interrupts.
  All transmission completed interrupt (TREND_E)
  Transmission trigger level interrupt (T_TRGR_E)
  Overflow error interrupt (OVERF_E)
- Clear the reception FIFO buffer.

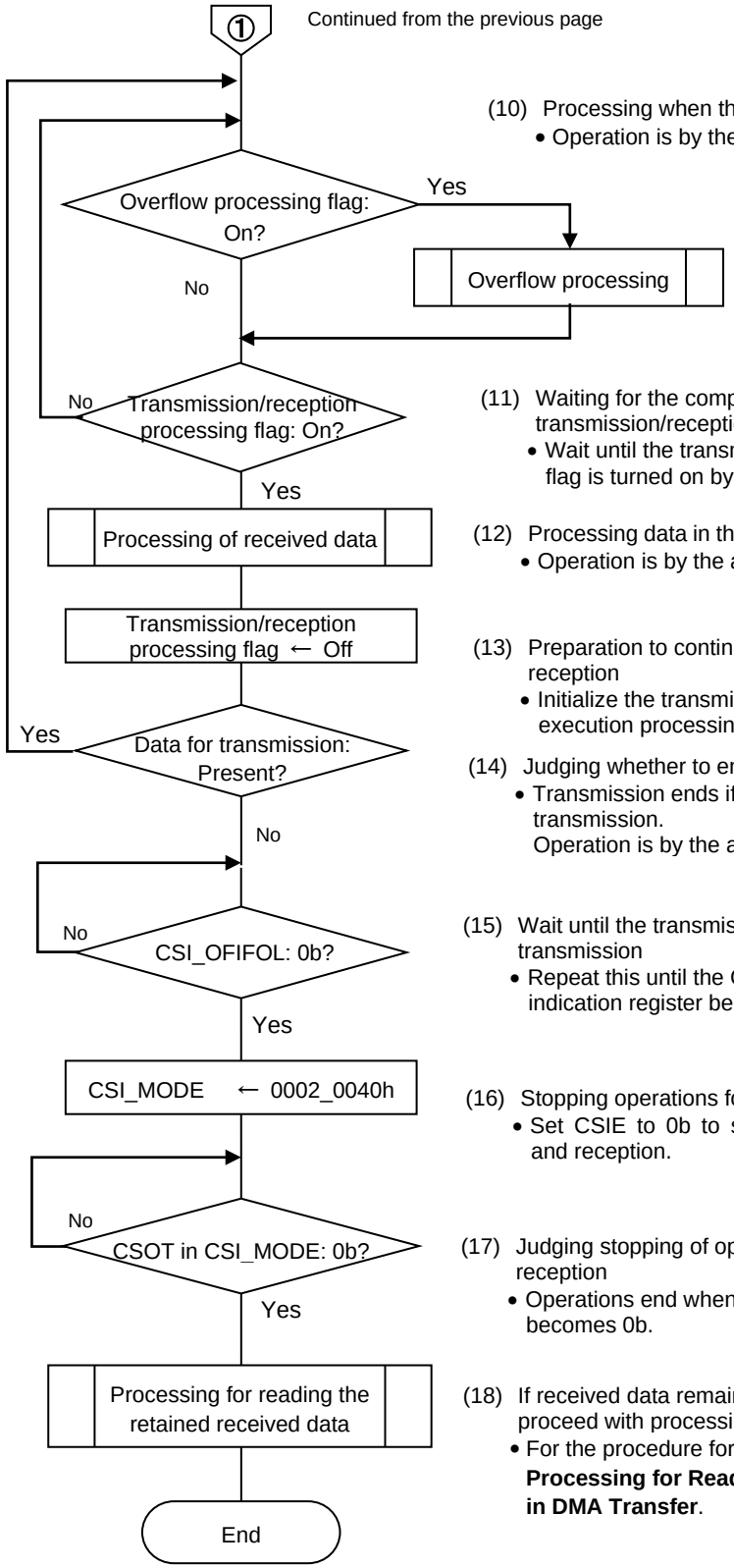
(6) Clearing the transmission FIFO buffer
- Write 0 to the transmission FIFO level indication register to clear the transmission FIFO. Writing a desired value other than 0 is possible.

(7) Writing the first data for transmission to the transmission FIFO
- Write 16 units of data for transmission to the transmission FIFO buffer.

(8) Preparation to start transmission and reception
- Initialize the transmission/reception interrupt routine execution processing flag.
- Initialize the overflow error processing flag.

(9) Starting operations for transmission and reception
- Set CSIE to 1b to start operations for transmission and reception.

Figure 39.4-11 Flow of Operations with Interrupt Transfer in Master Transmission/Reception Mode (for Transmission and Reception) (1/4)



(10) Processing when the overflow interrupt has occurred
- Operation is by the application

(11) Waiting for the completion of transmission/reception interrupt processing
- Wait until the transmission/reception processing flag is turned on by interrupt processing.

(12) Processing data in the received data buffer
- Operation is by the application

(13) Preparation to continue operations for transmission and reception
- Initialize the transmission/reception interrupt routine execution processing flag.

(14) Judging whether to end transmission
- Transmission ends if the buffer has no data for transmission.
  Operation is by the application.

(15) Wait until the transmission FIFO buffer has no data for transmission
- Repeat this until the CSI transmission FIFO level indication register becomes 0.

(16) Stopping operations for transmission and reception
- Set CSIE to 0b to stop operations for transmission and reception.

(17) Judging stopping of operations for transmission and reception
- Operations end when the CSOT bit in CSI_MODE becomes 0b.

(18) If received data remain in the reception FIFO buffer, proceed with processing for reading the remained data
- For the procedure for processing, see **Section 39.4.14.3, Processing for Reading the Remained Received Data in DMA Transfer**.

Figure 39.4-11 Flow of Operations with Interrupt Transfer in Master Transmission/Reception Mode (for Transmission and Reception) (2/4)

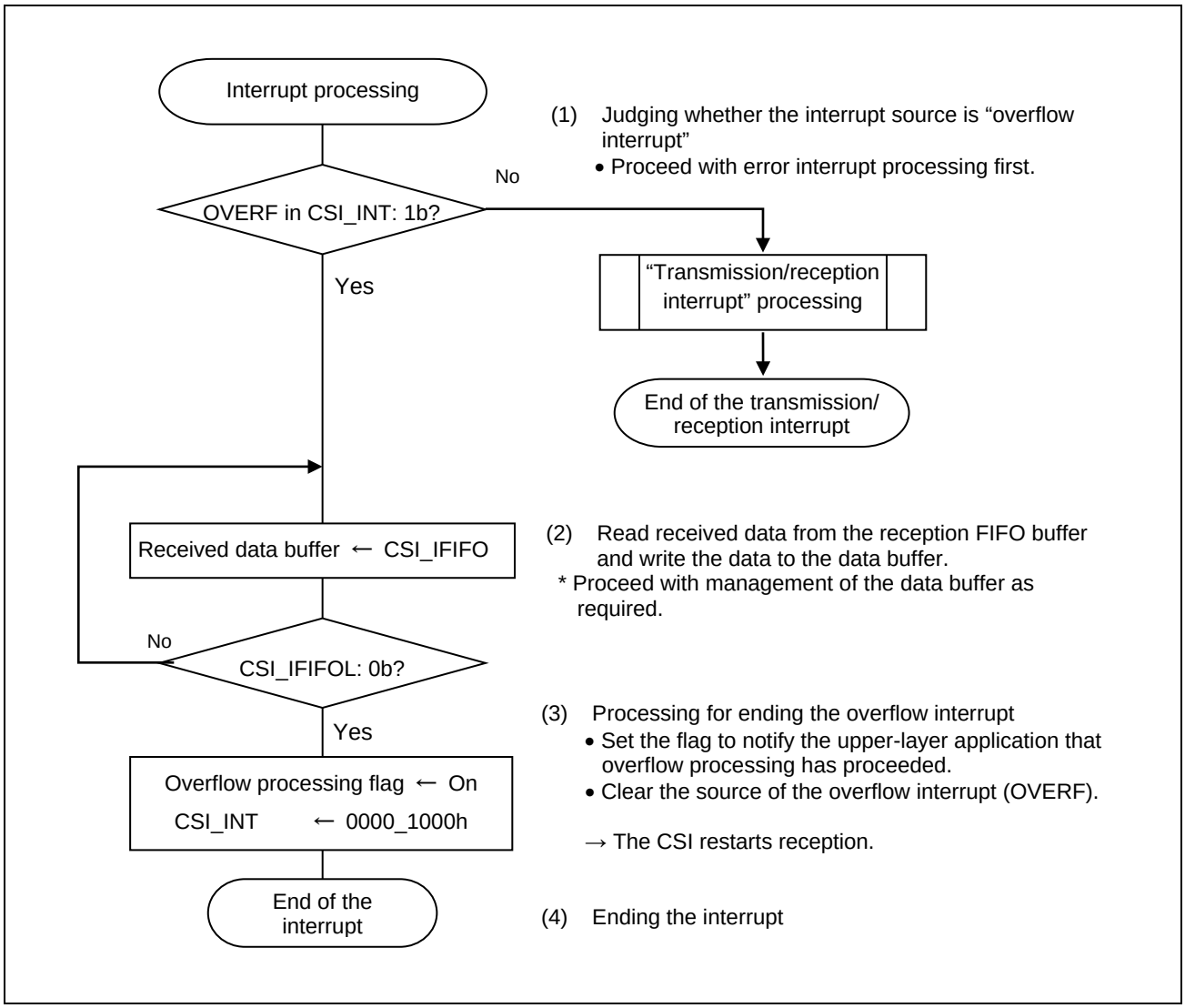


Figure 39.4-11 Flow of Operations with Interrupt Transfer in Master Transmission/Reception Mode (for Transmission and Reception) (3/4)

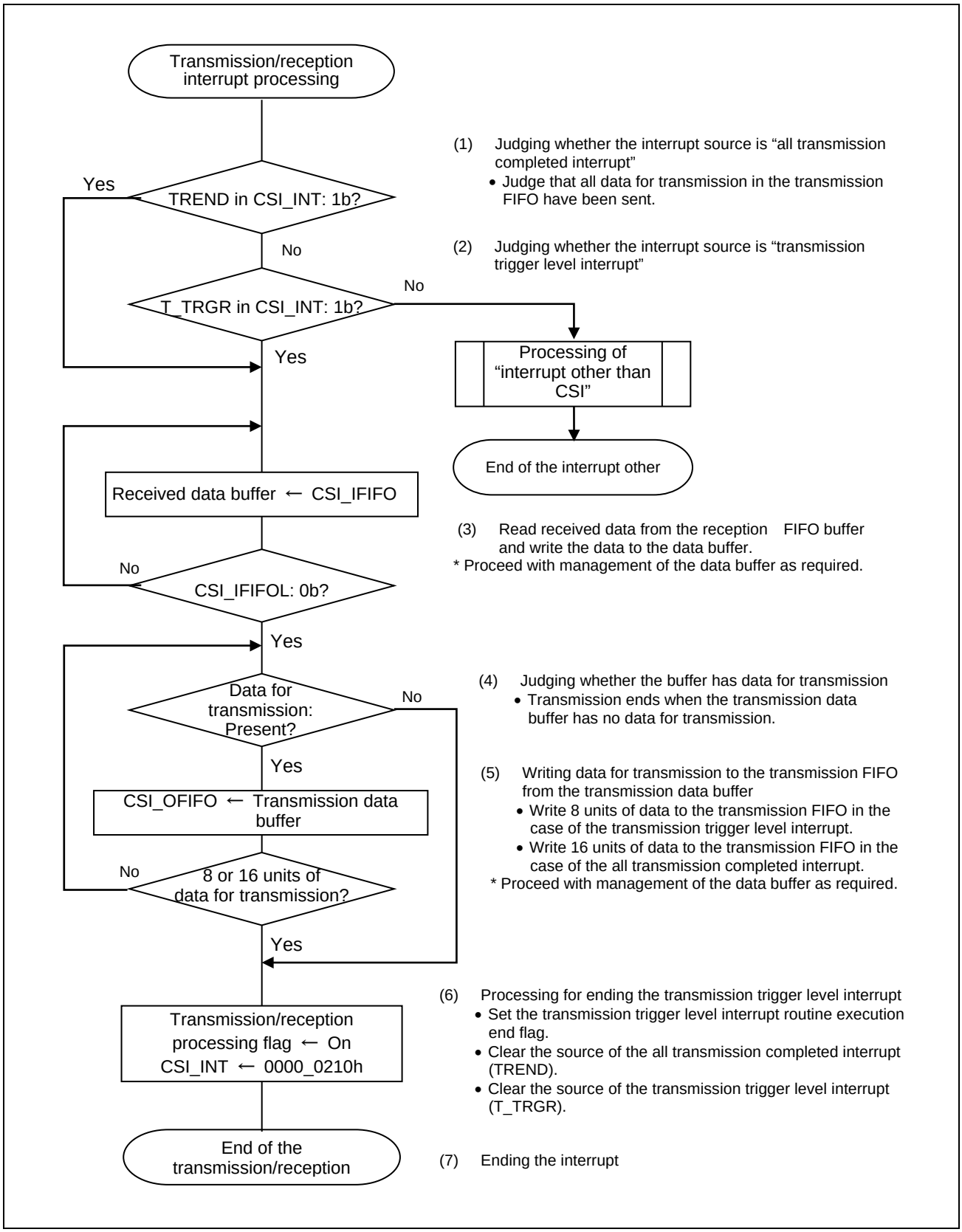


Figure 39.4-11 Flow of Operations with Interrupt Transfer in Master Transmission/Reception Mode (for Transmission and Reception) (4/4)

39.4.8.4 Settings in Master Transmission/Reception Mode and Flow of Operations (for Transmission-only Operation)

The figure below shows a flow of operations for transmission with the use of the transmission trigger level interrupt in master transmission/reception mode.

Data for transmission prepared in the transmission buffer are continuously transferred with the use of the transmission trigger level interrupt and the all transmission completed interrupt. Since the transmission function is only used, processing of received data is not handled.

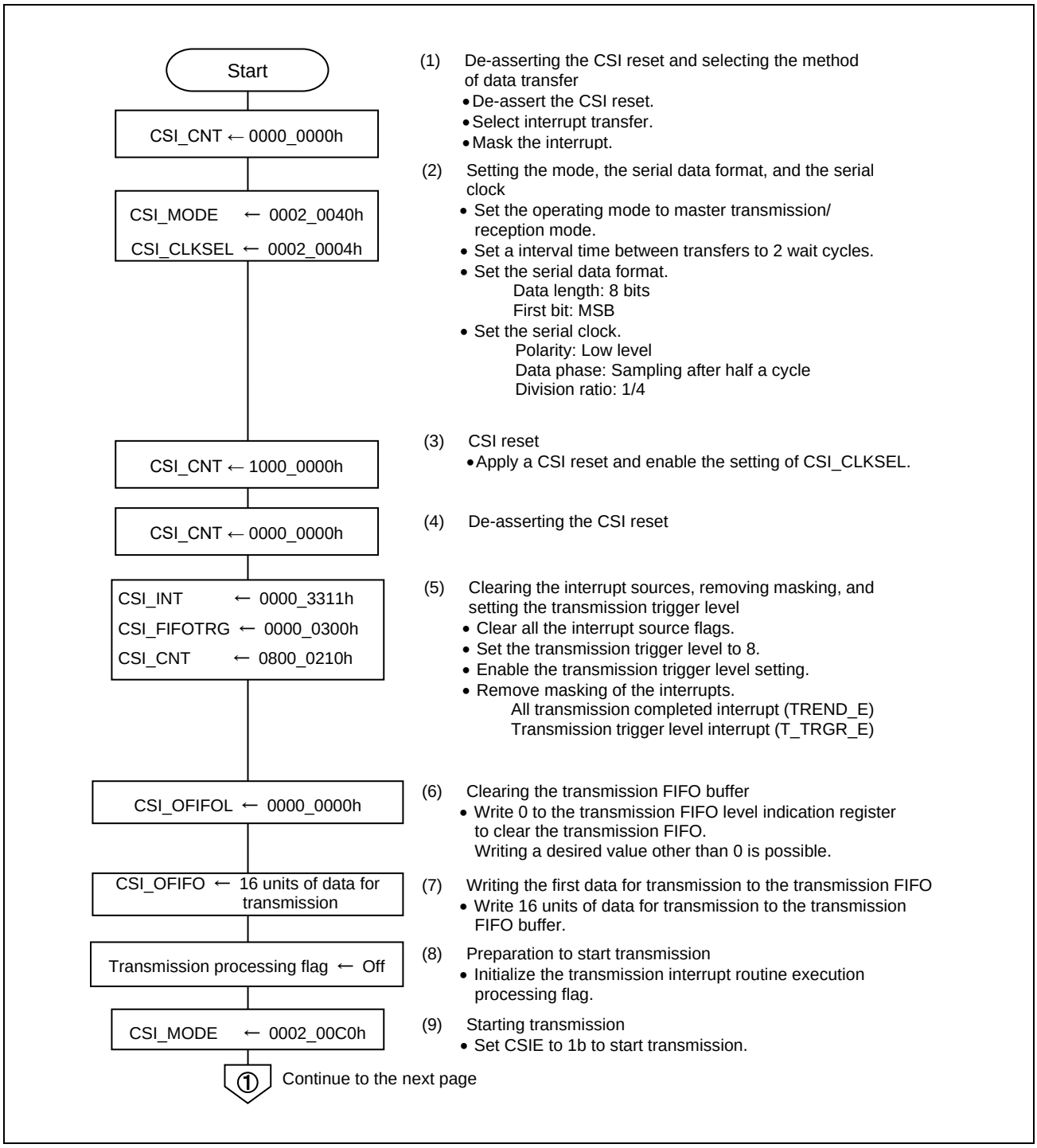


Figure 39.4-12 Flow of Operations with Interrupt Transfer in Master Transmission/Reception Mode (for Transmission-only Operation) (1/3)

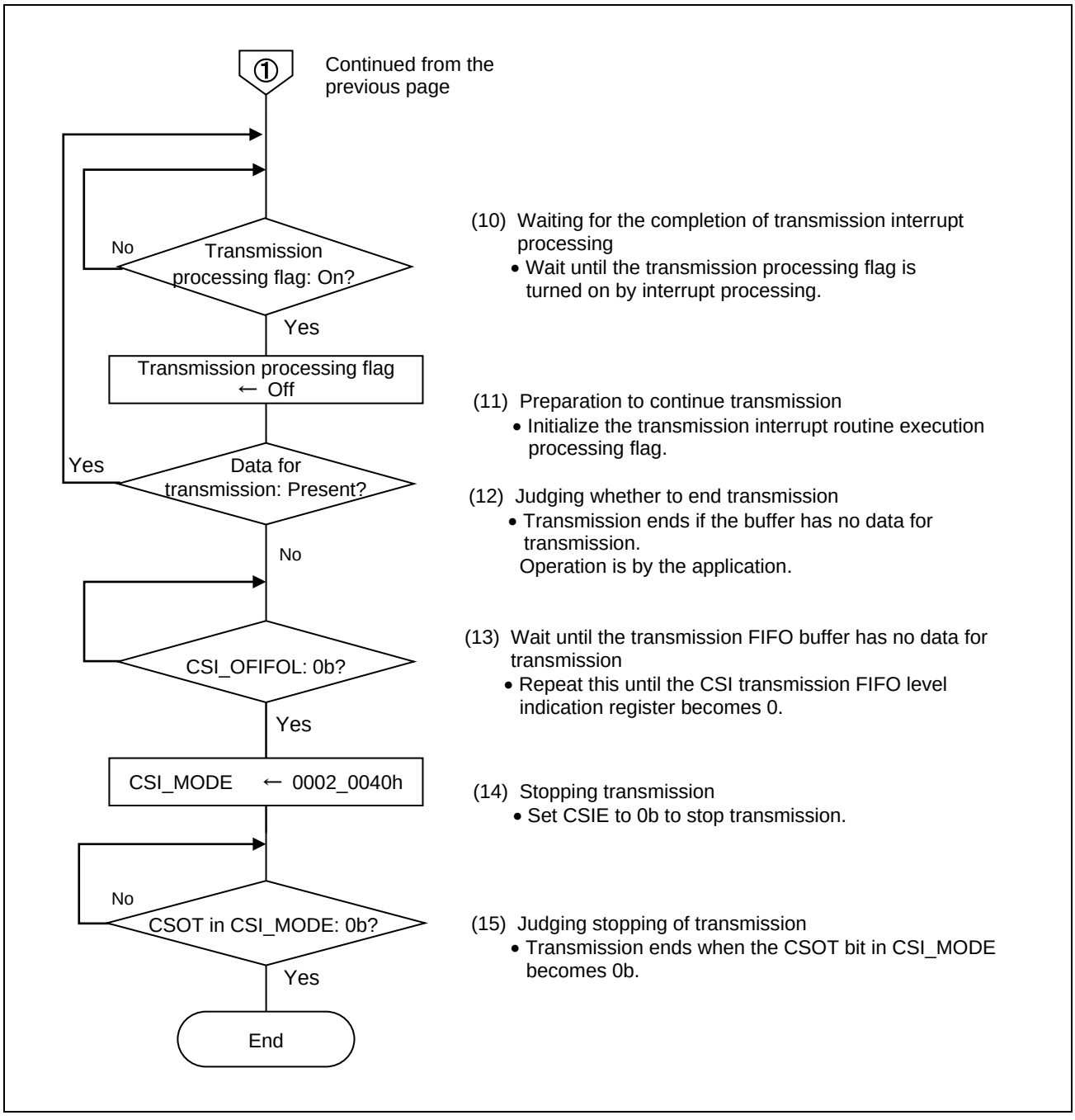
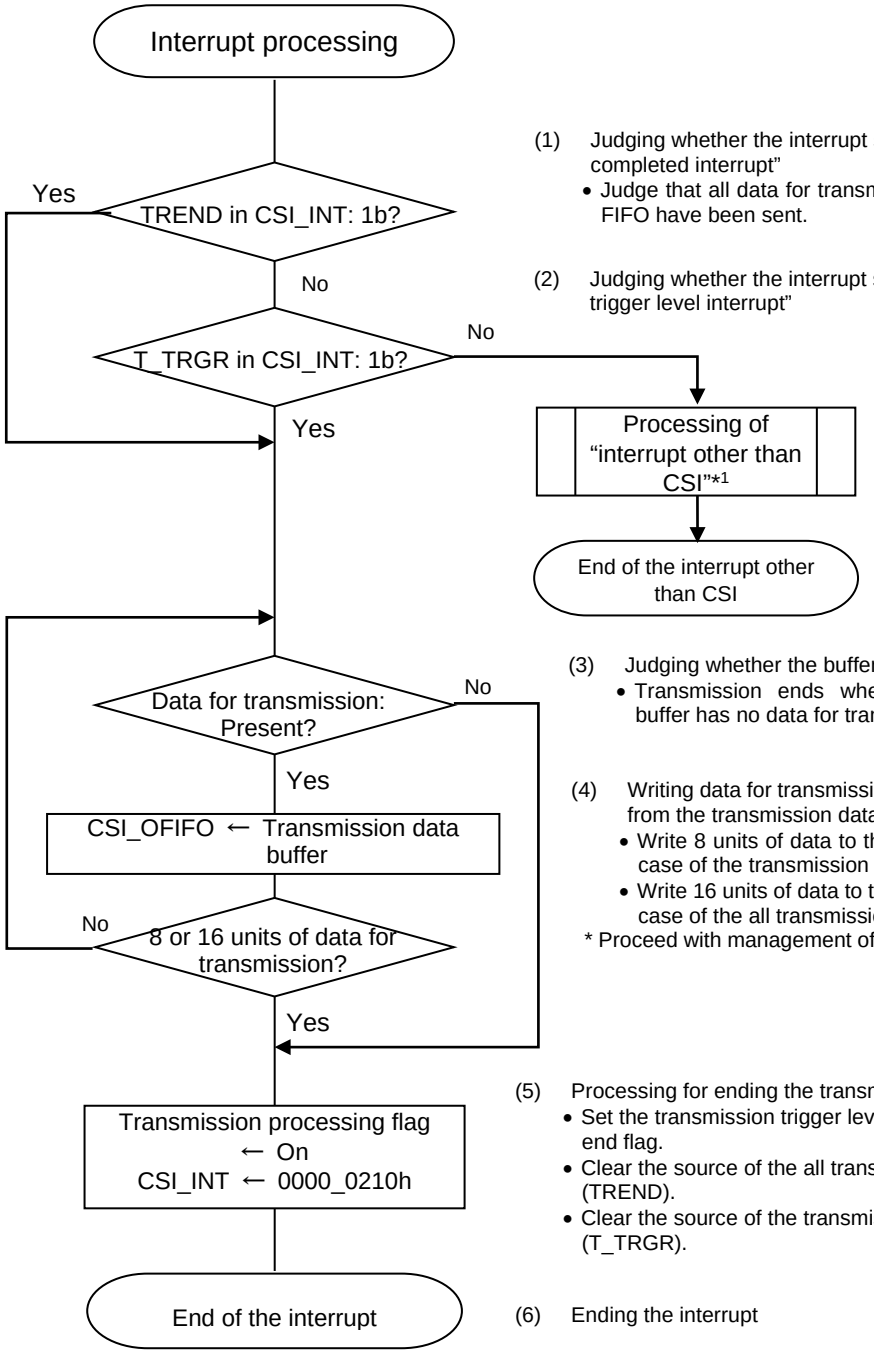


Figure 39.4-12 Flow of Operations with Interrupt Transfer in Master Transmission/Reception Mode (for Transmission-only Operation) (2/3)



Note 1. No interrupt request is generated because the overflow interrupt enable signal has not been set due to the transmission-only operation, but the overflow interrupt source flag may be set.

Figure 39.4-12 Flow of Operations with Interrupt Transfer in Master Transmission/Reception Mode (for Transmission-only Operation) (3/3)

39.4.9 Slave Reception-Only Mode

This mode is dedicated for reception to receive data transmitted from the master.

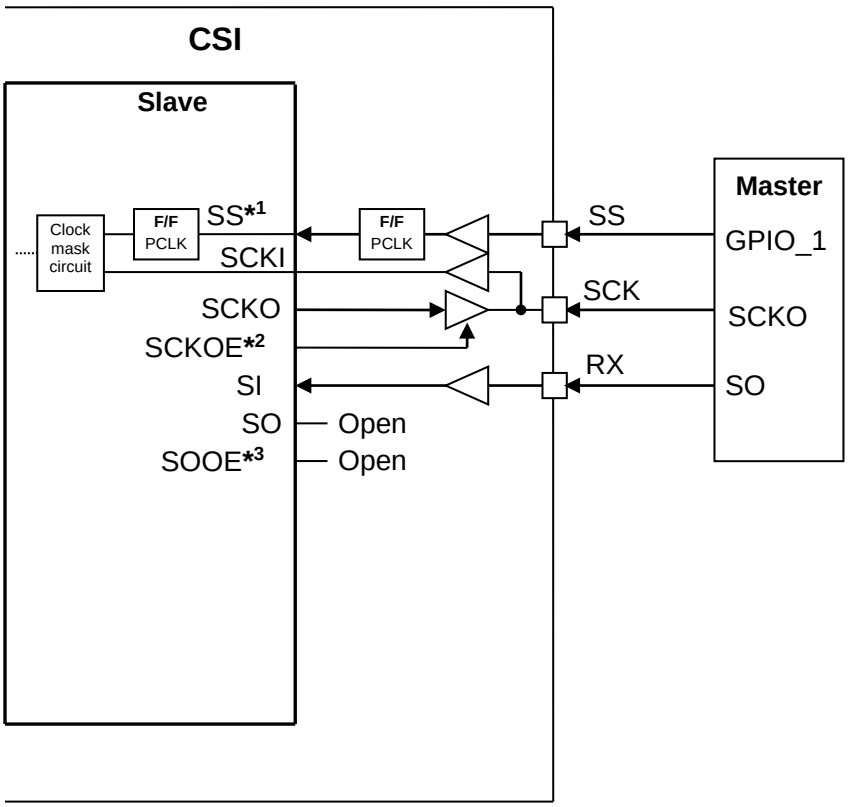
The transmission function is not used.

The slave operates in response to the serial clock (SCK) from the master.

Due to the slave section (SS pin) mechanism, one slave can communicate with the master in the system connected to multiple slaves.

Slave reception-only mode is a default mode at the time of a reset.

Figure 39.4-13 shows an example of connection with the master.



Note 1. When SS_ENA in the CSI_CLKSEL register = 1, the SS pin is used for mask control of the SCKI clock.

Note 2. SCKOE always outputs the low level.

Note 3. SOOE always outputs the low level.

Figure 39.4-13 Example of Connections in Slave Reception-only Mode

39.4.9.1 Setting Items in Slave Reception-only Mode

The table below lists the registers to be set in slave reception-only mode.

Table 39.4-9 List of the Registers to be Set in Slave Reception-only Mode

*1	Register Name	Bit Name	Bit	Setting
[R]	CSI_MODE	Communications mode: TRMD	6	0b (reception-only)
[R]		Serial data length: CCL	5	Select 16 bits or 8 bits. The data length for the slave and that for the master must match.
[R]		First bit: DIR	4	Select MSB or LSB. The first bit settings for the slave and master must match.
[R]	CSI_CLKSEL	Operating mode: SLAVE	15	1b (slave)
[O]		Control by the SS pin: SS_ENA	19	Determines use of the SS pin. Whether the SS pin is to be used depends on the system configuration.
[O]		Selection of the polarity of the SS pin: SS_POL	18	Selects the active level when the SS pin is used. It must match the active level of the control signal output by the master.
[R]		Polarity of the clock: CKP	17	The settings for the slave and master must match.
[R]		Data phase: DAP	16	Select the phase of serial data. It must match the data phase selection by the master.
[O]	CSI_CNT	DMA transfer for reception: R_DMAEN	16	Determines the method for transfer or received data.
[O]		Reception FIFO trigger level: R_TRGEN	19	Determines use of the reception FIFO trigger level.
[O]		Overflow interrupt: OVERF_E	12	Determines use of the overflow interrupt.
[O]		Transfer completed interrupt: CSIEND_E	8	Determines use of the transmission completed interrupt.
[O]		Reception trigger level interrupt: R_TRGR_E	0	Determines use of the reception trigger level interrupt.
[O]	CSI_FIFOTRG	Reception FIFO trigger level: R_TRG	2:0	Sets the level value when the reception FIFO trigger level is used.

Note 1. [R]: Required setting items.
[O]: Optional. Set these items as required.

39.4.9.2 Operation in Slave Reception-only Mode

(1) How to Start Operation

Reception starts following setting of the startup flag for communications (the CSIE bit in CSI_MODE) and the input of the serial clock (SCKI) after the initial settings.

When the control function of the SS pin is set, reception starts when the SS pin is asserted and the serial clock (SCKI) is input after the startup flag for communications has been set. For the specifications of the SS pin, see **Section 39.5.2, Timing of Serial Communications (Continuous Data Transfer)**.

The slave starts to read serial data (SI) on reception of the serial clock (SCK).

Since operations for communications start in response to reception of the serial clock and serial data output by the master, the initial setting must be completed before the master starts communications.

(2) How to End Operation

Clearing the startup flag for communications (the CSIE bit in CSI_MODE) stops reception.

If the startup flag is cleared during communications, reception is stopped after the completion of communications.

After reception is stopped, the slave does not respond to the request for reception from the master.

(3) Operation during Communications

When the slave receives the serial clock and serial data from the master, it writes the received data to the reception FIFO.

If the slave receives data while the reception FIFO has no space, an overflow error occurs and the subsequent data for reception are discarded.

To prevent data from being discarded, received data must be read to make space in the reception FIFO.

For details of an overflow error, see **Section 39.4.5.1, Overflow Error**.

(4) Reception Trigger Level Interrupt

A reception trigger level interrupt can be used. For details, see **Section 39.4.11.2, Reception Trigger Level**.

This interrupt occurs when received data are accumulated to the value set in R_TRG of the CSI_FIFOTRG register.

Reception will continue even if the reception trigger level interrupt occurs.

(5) Communications Error

An overflow error may occur.

39.4.9.3 Settings in Slave Reception-only Mode and Flow of Operations

The figure below shows a flow of operations for reception with the use of the reception trigger level interrupt in slave reception-only mode.

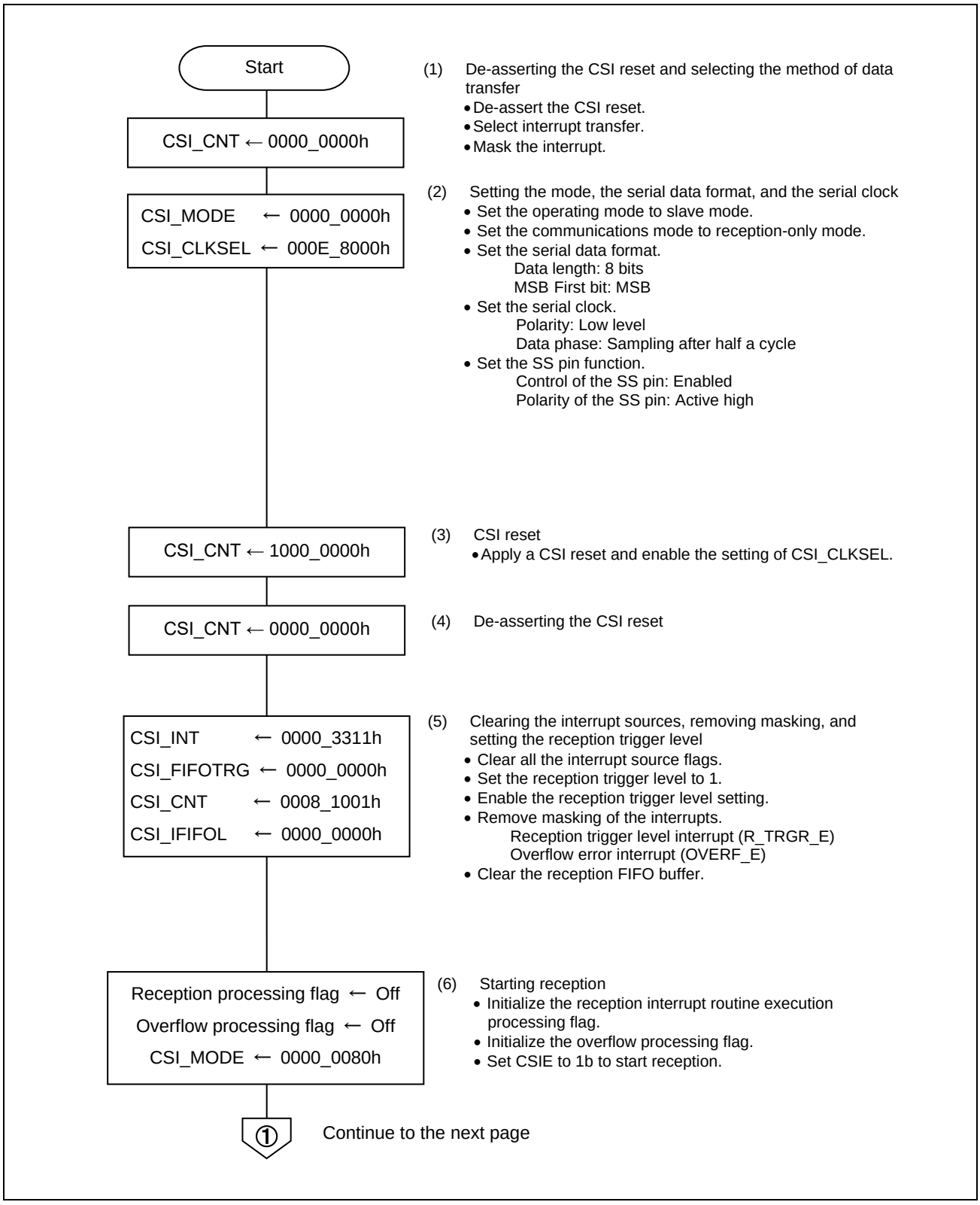


Figure 39.4-14 Flow of Operations with Interrupt Transfer in Slave Reception-only Mode (1/3)

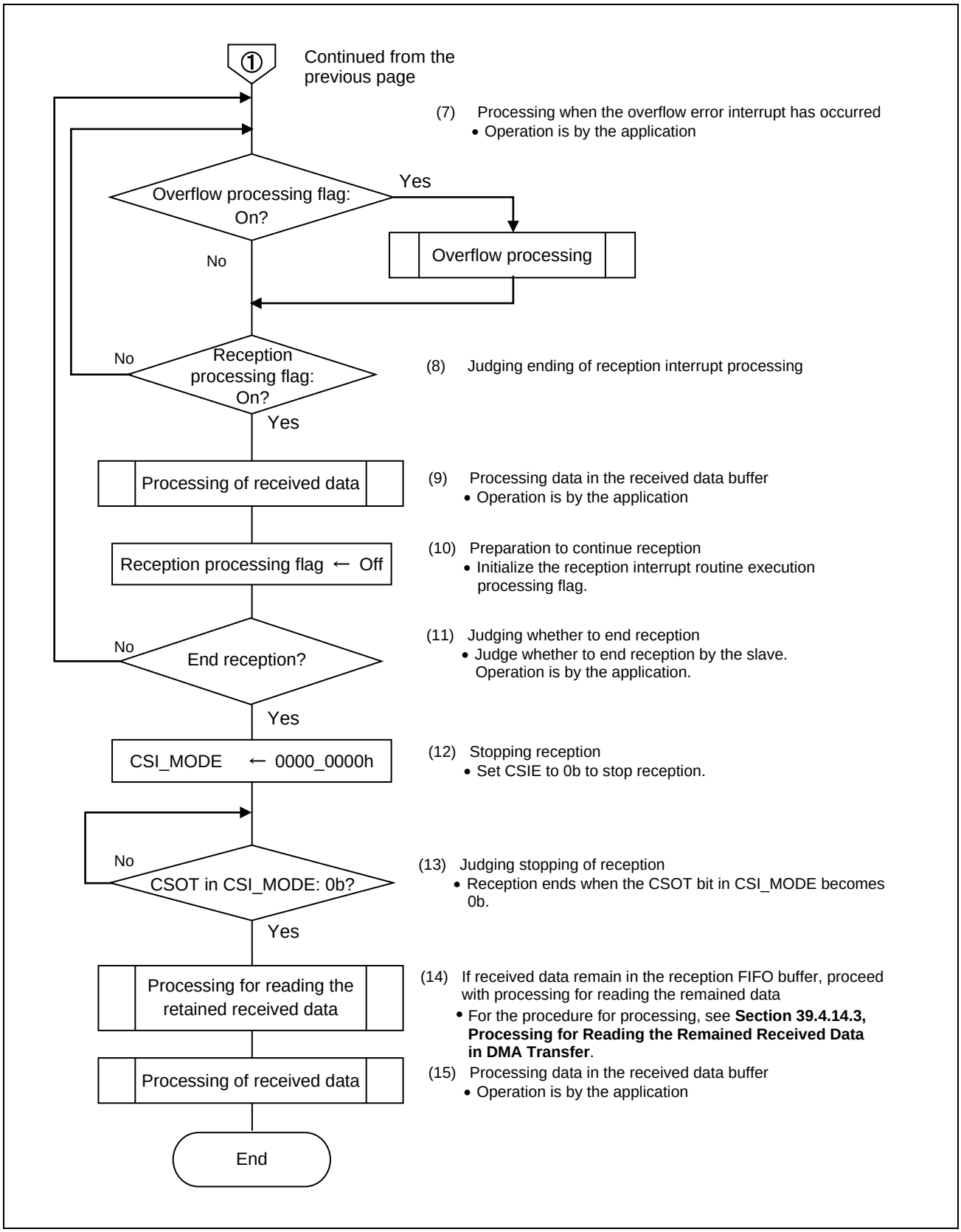


Figure 39.4-14 Flow of Operations with Interrupt Transfer in Slave Reception-only Mode (2/3)

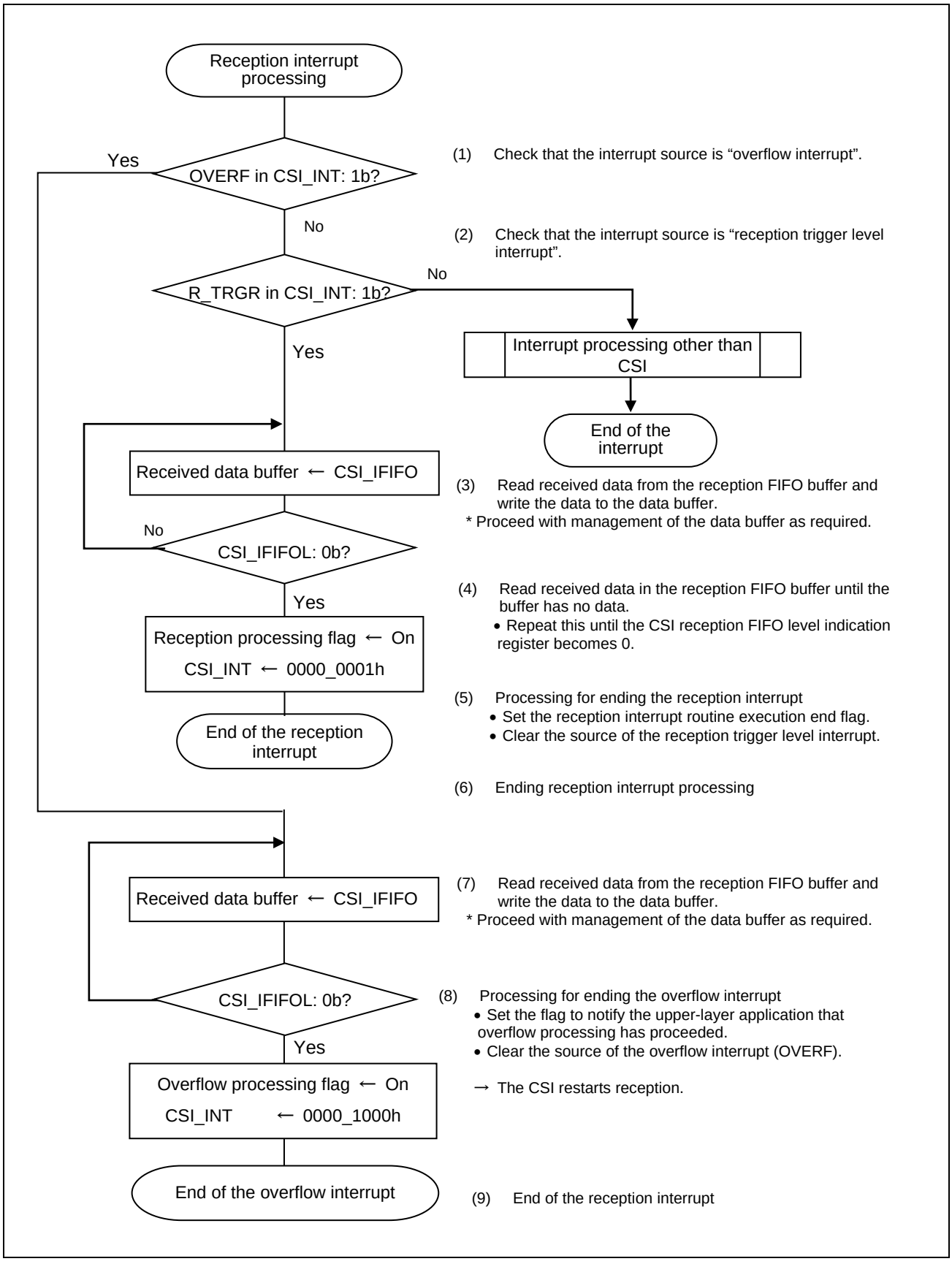


Figure 39.4-14 Flow of Operations with Interrupt Transfer in Slave Reception-only Mode (3/3)

39.4.10 Slave Transmission/Reception Mode

In this mode, transmission and reception of data to and from the master proceed simultaneously.

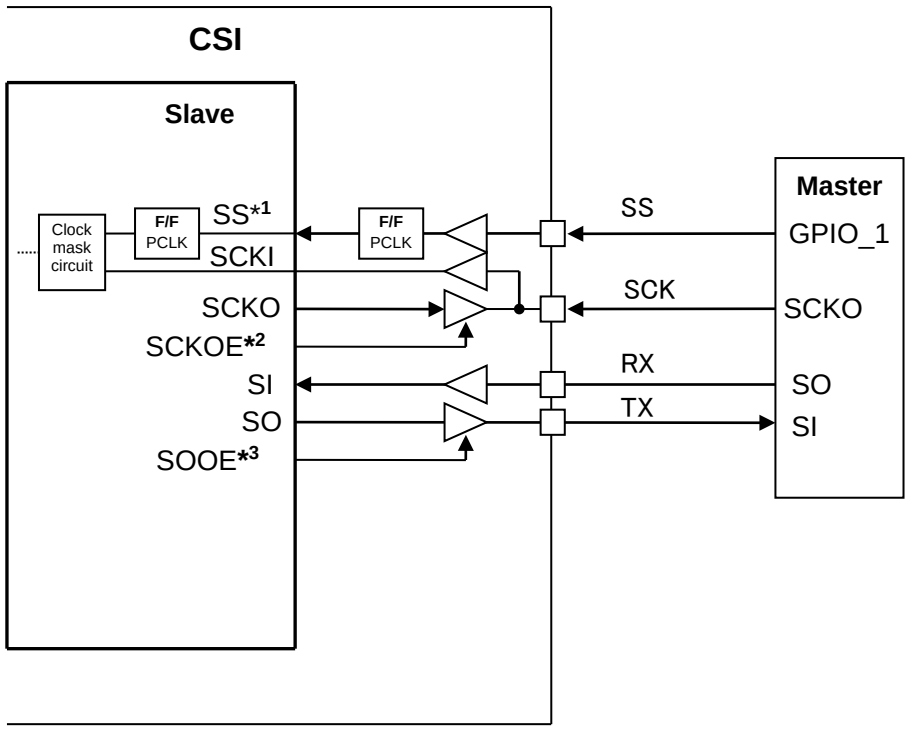
The slave operates in response to the serial clock (SCK) from the master.

It allows high-speed communications since transmission and reception proceed simultaneously.

Operation must be in this mode even when the transmission function is only used and the reception function is not used.

Due to the slave section (SS pin) mechanism, one slave can communicate with the master in the system connected to multiple slaves.

Figure 39.4-15 shows an example of connection with the master.



Note 1. When SS_ENA in the CSI_CLKSEL register = 1b, the SS pin is used for mask control of the SCKI clock. SCKOE always outputs the low level.

Note 2. When the SS pin function is in use, the startup flag for communications is set, and the SOOE pin outputs the high level while the SS pin is at the active level.

Note 3. When the SS pin function is not in use, this pin outputs the high level when the startup flag for communications is set. It goes to the low level when the startup flag is cleared to stop operations for transmission and reception.

Figure 39.4-15 Example of Connection in Slave Transmission/Reception Mode

39.4.10.1 Setting Items in Slave Transmission/Reception Mode

The table below lists the registers to be set in slave transmission/reception mode.

Table 39.4-10 List of the Registers to be Set in Slave Transmission/Reception Mode

*1	Register Name	Bit Name	Bit	Setting
[R]	CSI_MODE	Communications mode: TRMD	6	1b (transmission/reception mode)
[R]		Serial data length: CCL	5	Select 16 bits or 8 bits. The data length for the slave and that for the master must match.
[R]		First bit: DIR	4	Select MSB or LSB. The first bit settings for the slave and master must match.
[R]	CSI_CLKSEL	Operating mode: SLAVE	15	1b (slave)
[O]		Control by the SS pin: SS_ENA	19	Determines use of the SS pin. Whether the SS pin is to be used depends on the system configuration.
[O]		Selection of the polarity of the SS pin: SS_POL	18	Selects the active level when the SS pin is used. It must match the active level of the control signal output by the master.
[R]		Polarity of the clock: CKP	17	The settings for the slave and master must match.
[R]		Clock phase: DAP	16	Select the phase of serial data. It must match the data phase selection by the master.
[O]	CSI_CNT	DMA transfer for transmission: T_DMAEN	24	Determines the method for transfer or data for transmission.
[O]		Transmission FIFO trigger level: T_TRGEN	27	Determines use of the transmission FIFO trigger level.
[O]		DMA transfer for reception: R_DMAEN	16	Determines the method for transfer of received data.
[O]		Reception FIFO trigger level: R_TRGEN	19	Determines use of the reception FIFO trigger level.
[O]		All transmission completed interrupt: TREND_E	9	Determines use of the all transmission completed interrupt.
[O]		Underrun error interrupt: UNDER_E	13	Determines use of the underrun error interrupt.
[O]		Overflow interrupt: OVERF_E	12	Determines use of the overflow interrupt.
[O]		Transfer completed interrupt: CSIEND_E	8	Determines use of the transmission completed interrupt.
[O]		Transmission trigger level interrupt: T_TRGR_E	4	Determines use of the transmission trigger level interrupt.
[O]		Reception trigger level interrupt: R_TRGR_E	0	Determines use of the reception trigger level interrupt.
[O]	CSI_FIFOTRG	Transmission FIFO trigger level: T_TRG	10:8	Sets the level value when the transmission FIFO trigger level is used.
[O]		Reception FIFO trigger level: R_TRG	2:0	Sets the level value when the reception FIFO trigger level is used.

Note 1. [R]: Required setting items.
[O]: Optional. Set these items as required.

39.4.10.2 Operation in Slave Transmission/Reception Mode

(1) How to Start Operation

After the initial settings, set the startup flag for communications (the CSIE bit in CSI_MODE) and write data for transmission to the transmission FIFO to prepare for operations for transmission and reception.

The slave starts operations for transmission and reception on reception of the serial clock (SCK) from the master. To use the function for slave selection (SS pin), however, the SS pin must be at the active level before starting transmission and reception.

To start operations for communications with the serial clock output by the master, the initial settings must be completed to start operations for transmission and reception.

(2) How to End Operation

Clearing the startup flag for communications (the CSIE bit in CSI_MODE) stops operations for transmission and reception.

Even if data for transmission remain in the transmission FIFO at the time the startup flag is cleared, operations for transmission and reception are stopped.

If the startup flag is cleared during the cycle of operations for transmission and reception, operations for transmission and reception are stopped after the completion of the cycle.

After operations for transmission and reception are stopped, the slave does not respond to the request for transmission and reception from the master.

The SOOE pin goes to the low level when the CSIE bit is cleared and communications for transmission and reception are stopped.

(3) Operation during Communications

The slave handles operations for transmission and reception according to the serial clock transmitted from the master.

If transmission proceeds while the transmission FIFO has no data, an underrun error occurs.

Operations for transmission and reception are stopped if an underrun error occurs.

An overflow error occurs if reception proceeds while the reception FIFO is full.

If an overflow error occurs, reception is stopped, but transmission continues.

For details of underrun and overflow errors, see **Section 39.4.5, Operation and Procedure for Processing when an Error Occurs**.

To avoid an error, control is required to ensure that the transmission FIFO is never empty and the reception FIFO is never full.

(4) Reception Trigger Level Interrupt

A reception trigger level interrupt can be used. For details, see **Section 39.4.11.2, Reception Trigger Level**.

This interrupt occurs when received data are accumulated to the value set in R_TRG of the CSI_FIFOTRG register.

Reception will continue even if the reception trigger level interrupt occurs.

(5) Transmission Trigger Level Interrupt

A transmission trigger level interrupt can be used. For details, see **Section 39.4.11.1, Transmission Trigger Level**.

The transmission trigger level interrupt occurs when data in the transmission FIFO are reduced due to the operation for transmission and the free space increases to the value set in T_TRG of the CSI_FIFOTRG register.
Even if this interrupt occurs, transmission and reception continue.

(6) Communications Error

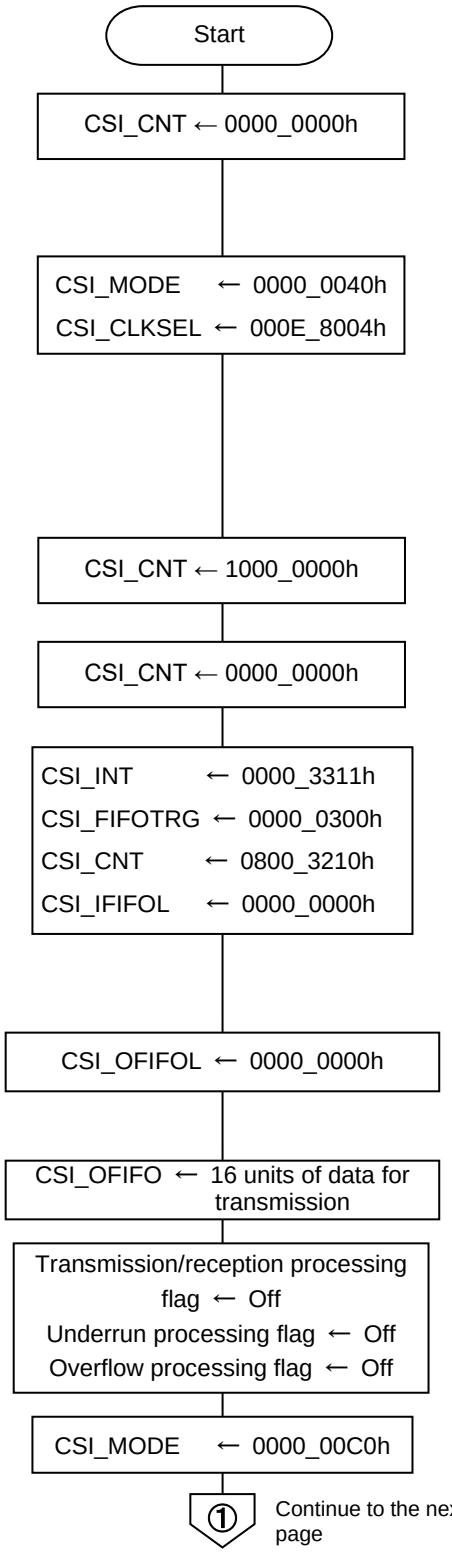
An underrun error may occur.

An overflow error may occur.

39.4.10.3 Settings in Slave Transmission/Reception Mode and Flow of Operations (for Transmission and Reception)

The figure below shows a flow of operations for transmission and reception with the use of the transmission trigger level interrupt in slave transmission/reception mode.

Data for transmission prepared in the transmission buffer are continuously transferred with the use of the transmission trigger level interrupt and all transmission completed interrupt.



(1) De-asserting the CSI reset and selecting the method of data transfer
- De-assert the CSI reset.
- Select interrupt transfer.
- Mask the interrupt.

(2) Setting the operating mode, the serial data format, the SS pin, and the serial clock
- Set the operating mode to slave transmission/reception mode.
- Set the serial data format.
  Data length: 8 bits
  First bit: MSB
- Set the serial clock.
  Polarity: Low level
  Data phase: Sampling after half a cycle
- Set the SS pin function.
  Control of the SS pin: Enabled
  Polarity of the SS pin: Active high

(3) CSI reset
- Apply a CSI reset and enable the setting of CSI_CLKSEL.

(4) De-asserting the CSI reset

(5) Clearing the interrupt sources, removing masking, and setting the transmission trigger level
- Clear all the interrupt source flags.
- Set the transmission trigger level to 8.
- Enable the transmission trigger level setting.
- Remove masking of the interrupts.
  All transmission completed interrupt (TREND_E)
  Transmission trigger level interrupt (T_TRGR_E)
  Overflow error interrupt (OVERF_E)
  Underrun error interrupt (UNDER_E)
- Clear the reception FIFO buffer.

(6) Clearing the transmission FIFO buffer
- Write 0 to the transmission FIFO level indication register to clear the transmission FIFO.
- Writing a desired value other than 0 is possible.

(7) Writing the first data for transmission to the transmission FIFO
- Write 16 units of data for transmission to the transmission FIFO buffer.

(8) Preparation to start transmission and reception
- Initialize the transmission/reception interrupt routine execution processing flag.
- Initialize the underrun error processing flag.
- Initialize the overflow error processing flag.

(9) Starting operations for transmission and reception
- Set CSIE to 1b to start operations for transmission and reception.

Figure 39.4-16 Flow of Operations with Interrupt Transfer in Slave Transmission/Reception Mode (for Transmission and Reception) (1/4)

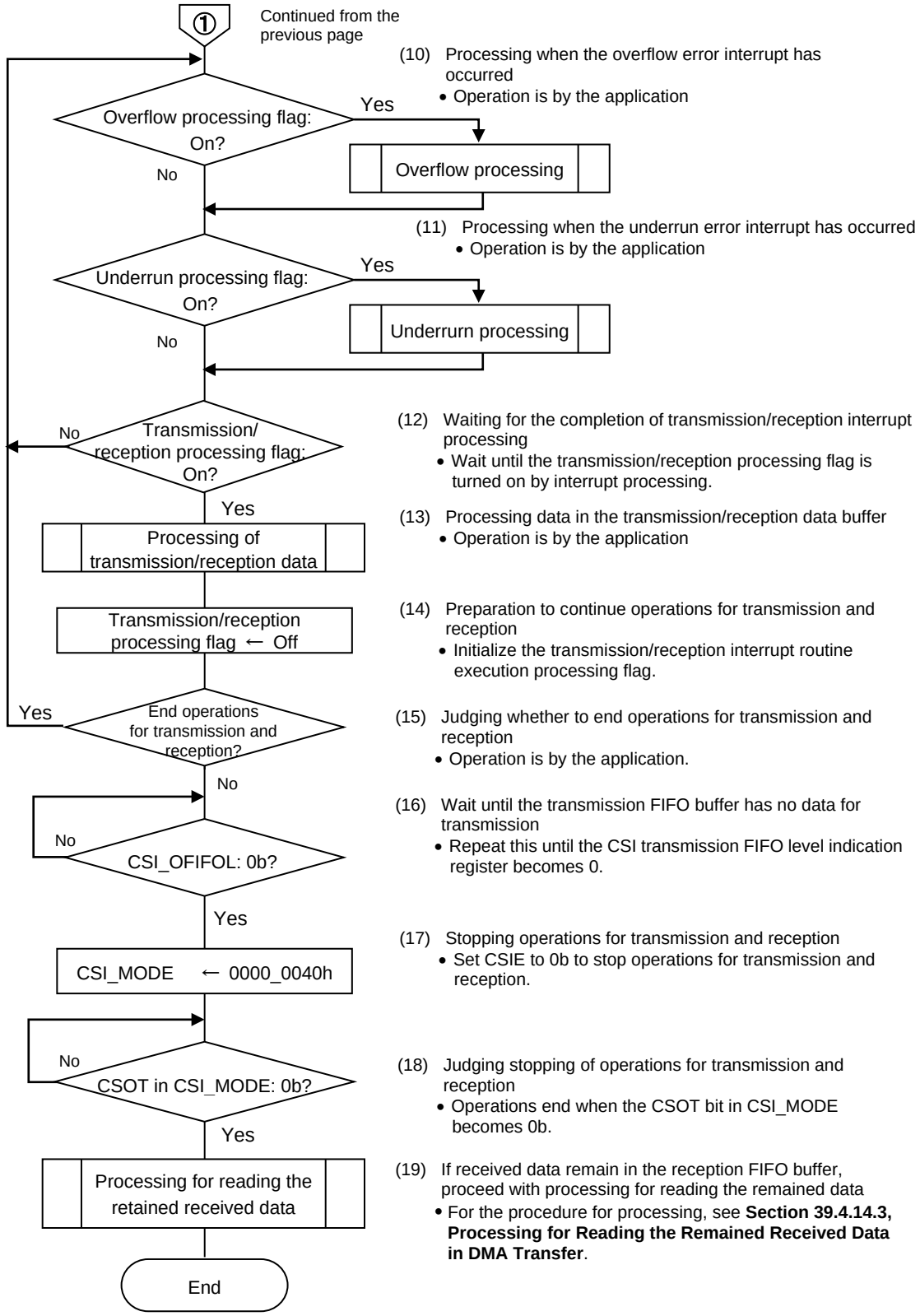


Figure 39.4-16 Flow of Operations with Interrupt Transfer in Slave Transmission/Reception Mode (for Transmission and Reception) (2/4)

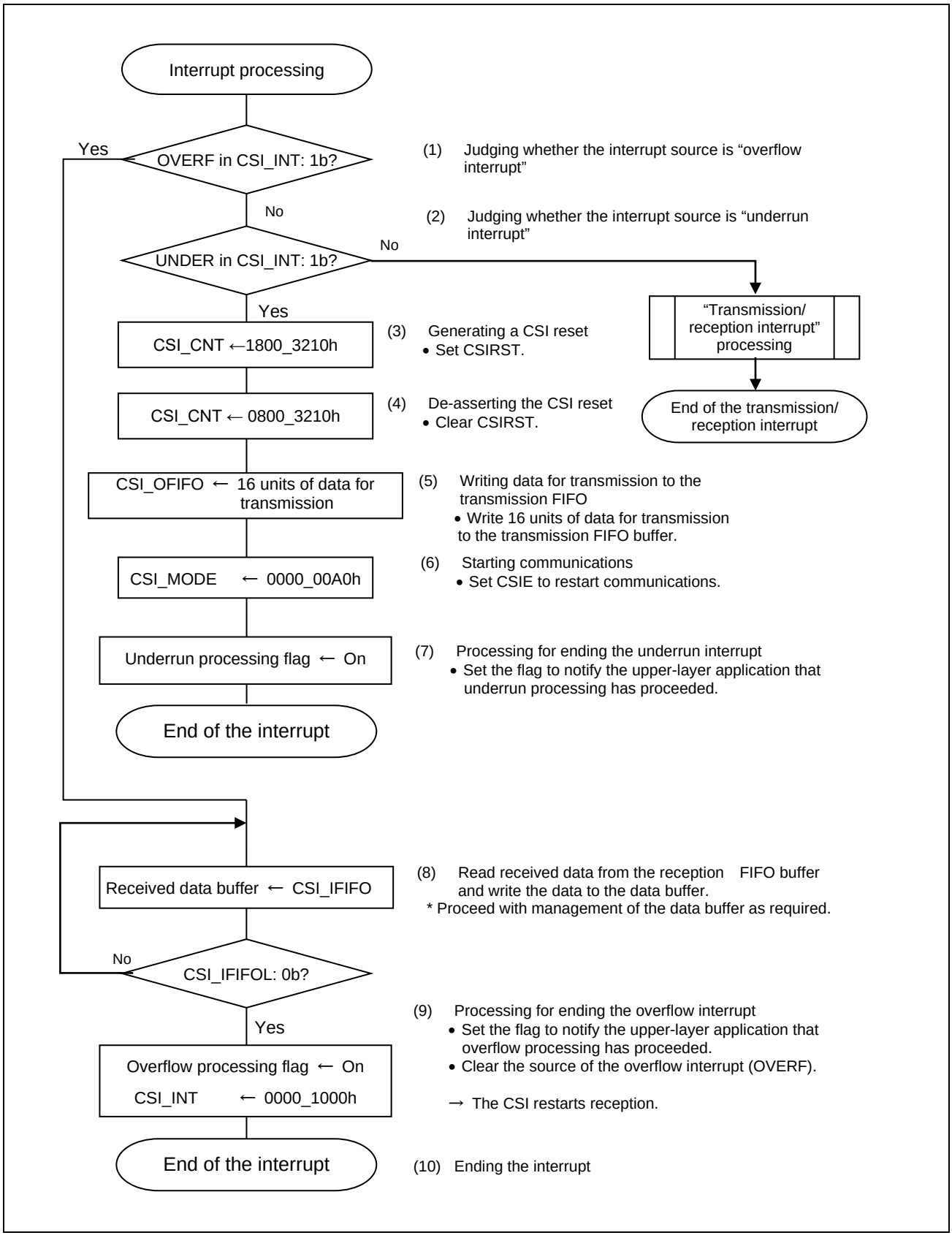


Figure 39.4-16 Flow of Operations with Interrupt Transfer in Slave Transmission/Reception Mode (for Transmission and Reception) (3/4)

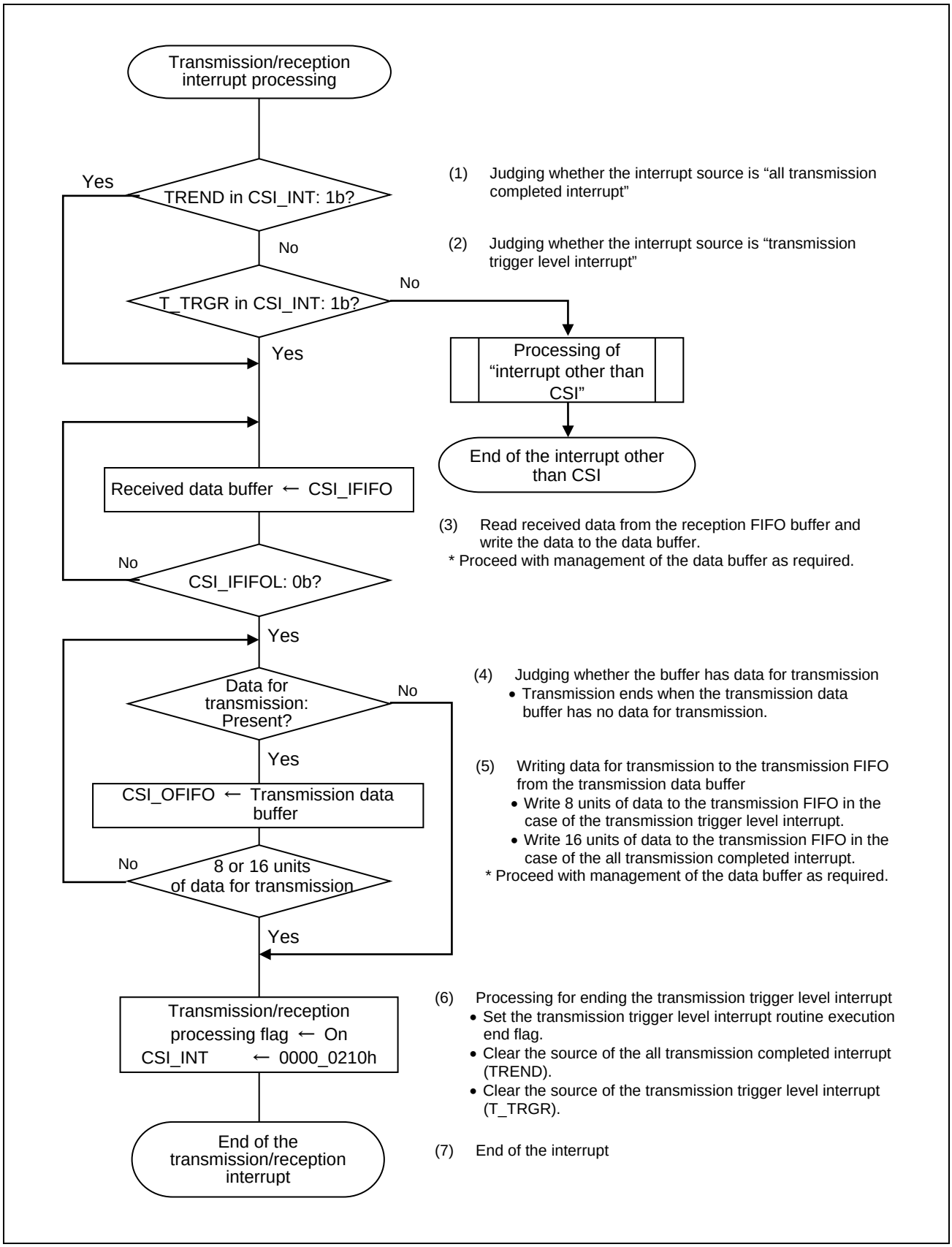
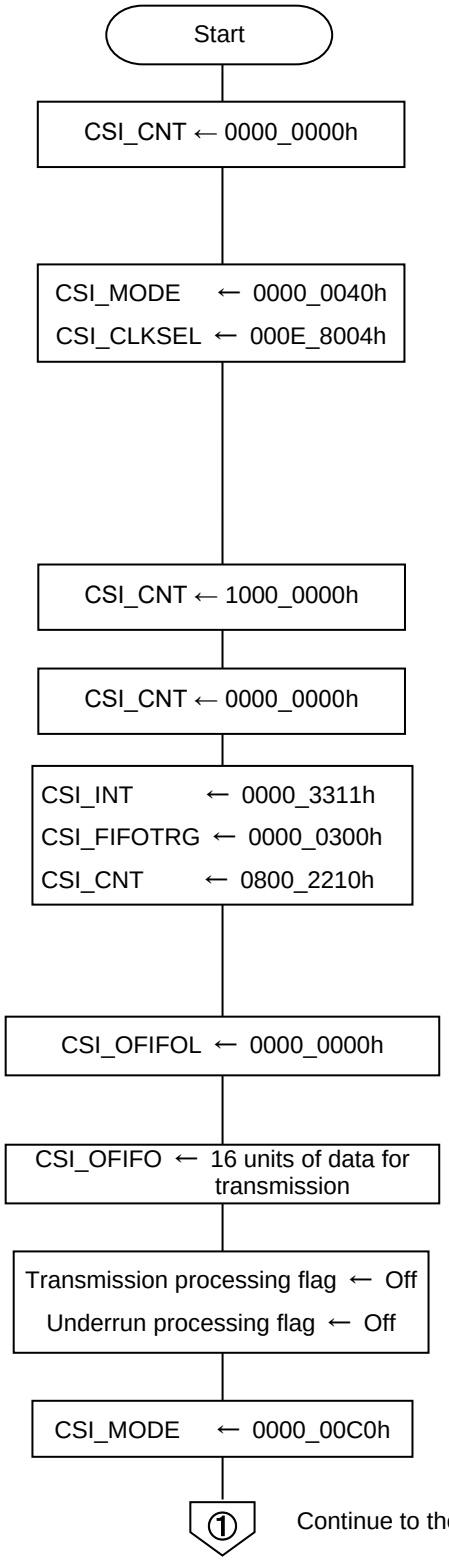


Figure 39.4-16 Flow of Operations with Interrupt Transfer in Slave Transmission/Reception Mode (for Transmission and Reception) (4/4)

39.4.10.4 Settings in Slave Transmission/Reception Mode and Flow of Operations (for Transmission-only Operation)

The figure below shows a flow of operations for transmission with the use of the transmission trigger level interrupt in slave transmission/reception mode.

Data for transmission prepared in the transmission buffer are continuously transferred with the use of the transmission trigger level interrupt and all transmission completed interrupt. Since the transmission function is only used, processing of received data is not handled.



(1) De-asserting the CSI reset and selecting the method of data transfer
- De-assert the CSI reset.
- Select interrupt transfer.
- Mask the interrupt.

(2) Setting the operating mode, the serial data format, the SS pin, and the serial clock
- Set the operating mode to slave transmission/reception mode.
- Set the serial data format.
  Data length: 8 bits
  MSBFirst bit: MSB
- Set the serial clock.
  Polarity: Low level
  Data phase: Sampling after half a cycle
- Set the SS pin function.
  Control of the SS pin: Enabled
  Polarity of the SS pin: Active high

(3) CSI reset
- Apply a CSI reset and enable the setting of CSI_CLKSEL.

(4) De-asserting the CSI reset

(5) Clearing the interrupt sources, removing masking, and setting the transmission trigger level
- Clear all the interrupt source flags.
- Set the transmission trigger level to 8.
- Enable the transmission trigger level setting.
- Remove masking of the interrupts.
  All transmission completed interrupt (TREND_E)
  Transmission trigger level interrupt (T_TRGR_E)
  Underrun error interrupt (UNDER_E)

(6) Clearing the transmission FIFO buffer
- Write 0 to the transmission FIFO level indication register to clear the transmission FIFO.
- Writing a desired value other than 0 is possible.

(7) Writing the first data for transmission to the transmission FIFO
- Write 16 units of data for transmission to the transmission FIFO buffer.

(8) Preparation to start transmission
- Initialize the transmission interrupt routine execution processing flag.
- Initialize the underrun error processing flag.

(9) Starting transmission
- Set CSIE to 1b to start transmission.

Figure 39.4-17 Flow of Operations with Interrupt Transfer in Slave Transmission/Reception Mode (for Transmission-only Operation) (1/4)

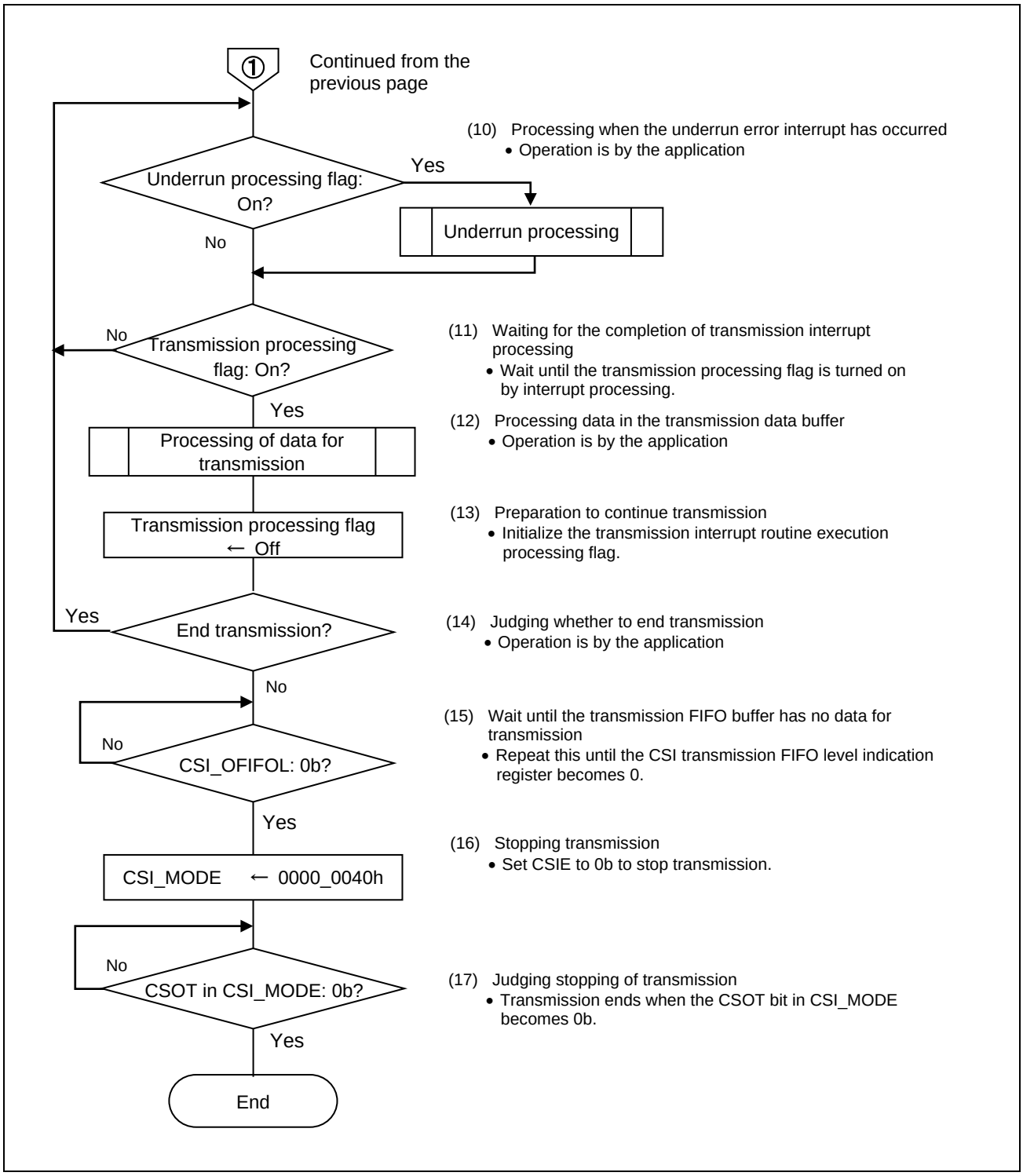


Figure 39.4-17 Flow of Operations with Interrupt Transfer in Slave Transmission/Reception Mode (for Transmission-only Operation) (2/4)

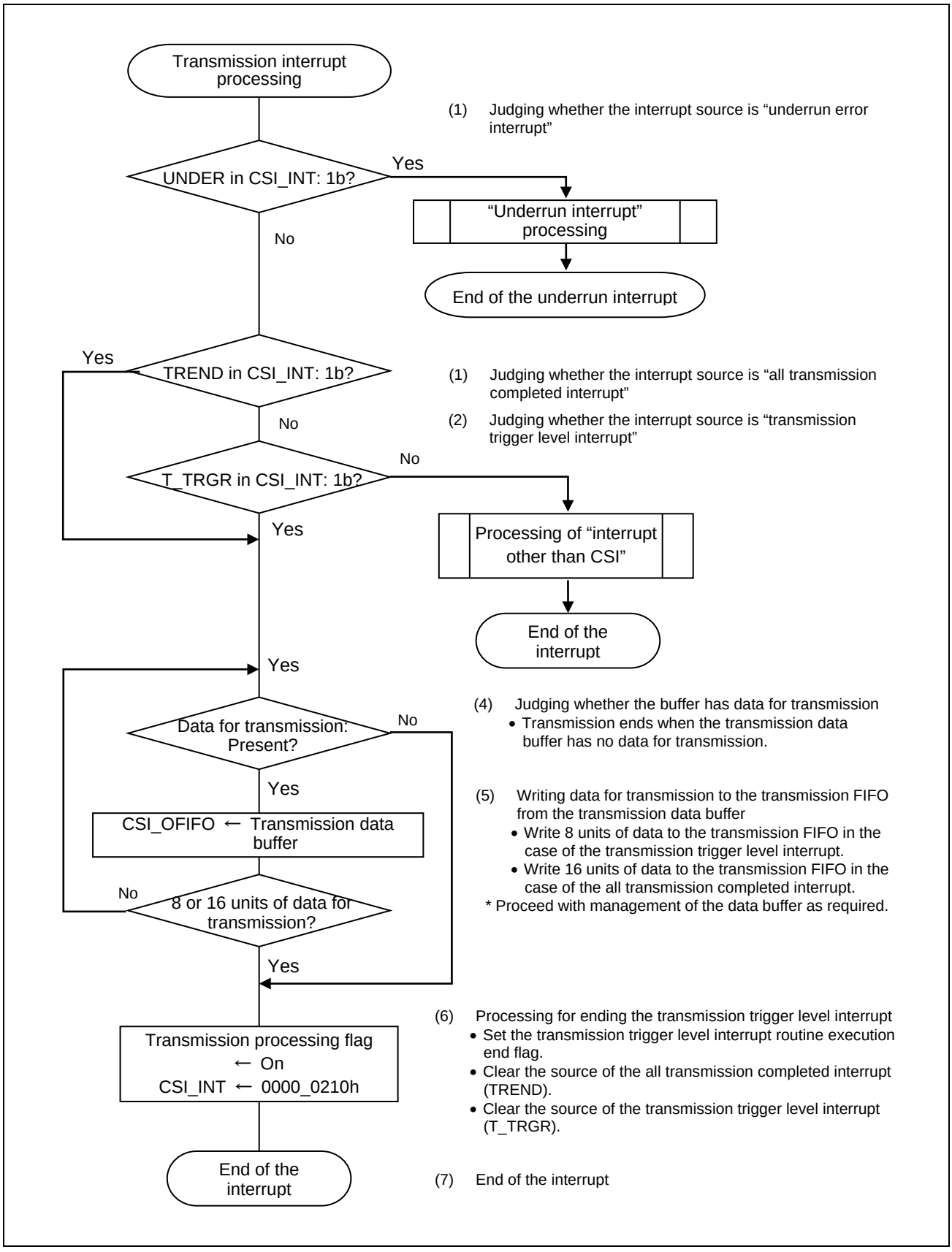


Figure 39.4-17 Flow of Operations with Interrupt Transfer in Slave Transmission/Reception Mode (for Transmission-only Operation) (3/4)

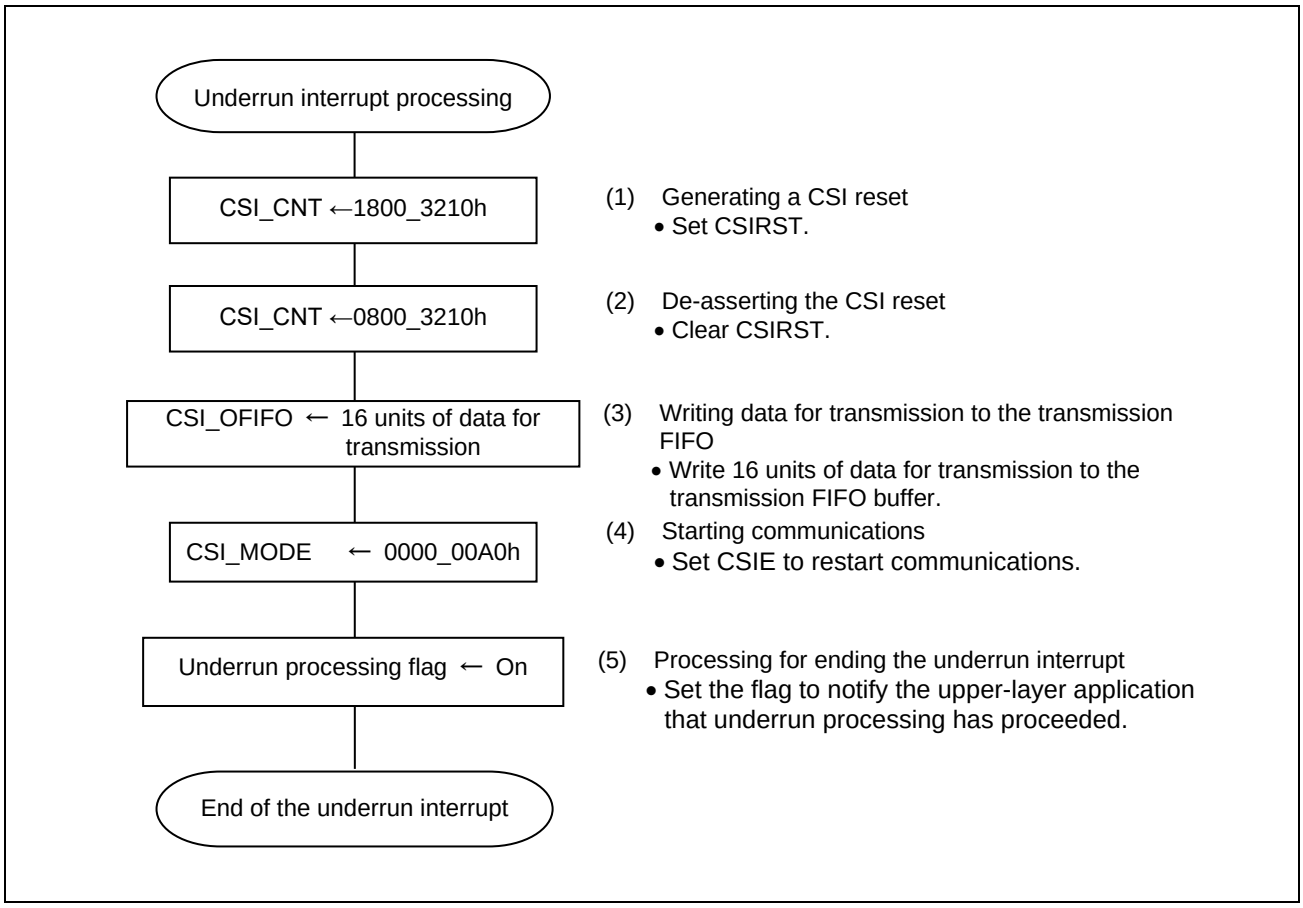


Figure 39.4-17 Flow of Operations with Interrupt Transfer in Slave Transmission/Reception Mode (for Transmission-only Operation) (4/4)

39.4.11 Trigger Level Function

The CSI has the trigger level function which monitors the buffering level of data for the transmission FIFO and the reception FIFO respectively and generates a trigger in response to the setting.

The trigger level function can be set for transmission and for reception individually.

A trigger can be used as a source of the interrupt request and the DMA transfer request.

39.4.11.1 Transmission Trigger Level

A trigger occurs when the free space in the transmission FIFO reaches the specified level due to the operation for transmission.

(1) Setting Procedure

Set the level at which a trigger occurs in T_TRG[2:0] of the CSI FIFO trigger level register (CSI_FIFOTRG). Also, setting the transmission trigger level setting enable flag (T_TRGEN) in the CSI control register (CSI_CNT) makes the trigger level available. To use the transmission trigger level as an interrupt, set the transmission trigger level interrupt enable flag (T_TRGR_E) in the CSI control register (CSI_CNT).

If the T_DMAEN bit in the CSI control register (CSI_CNT) is set to enable DMA transfer for transmission, the transmission trigger level can be used for the DMA transfer request for transmission.

CAUTION

The settings for the transmission trigger level other than the interrupt enable flag should be made while communications are stopped (CSOT bit of CSI_MODE = 0b). Operation when the settings are made during communications (when CSIE of the CSI_MODE register = 1b or CSOT = 1b) is not guaranteed.

(2) Description of Operation

A trigger occurs when the free space in the transmission FIFO reaches the setting of the transmission trigger level (T_TRG[2:0] in CSI_CNT).

A trigger does not occur if the setting is exceeded when data for transmission are written to the transmission FIFO and the free space is reduced. A trigger does not also occur when the free space in the transmission FIFO does not fall below the specified level after the occurrence of a trigger. Therefore, to continue transmission by using the transmission trigger level, care should be taken with management of the free space in the transmission FIFO in order to maintain the occurrence of triggers.

To use the transmission trigger level as an interrupt, clear the transmission trigger level interrupt flag (T_TRGR) in the CSI interrupt status register (CSI_INT) after writing data for transmission to the transmission FIFO following the occurrence of the transmission trigger level interrupt.

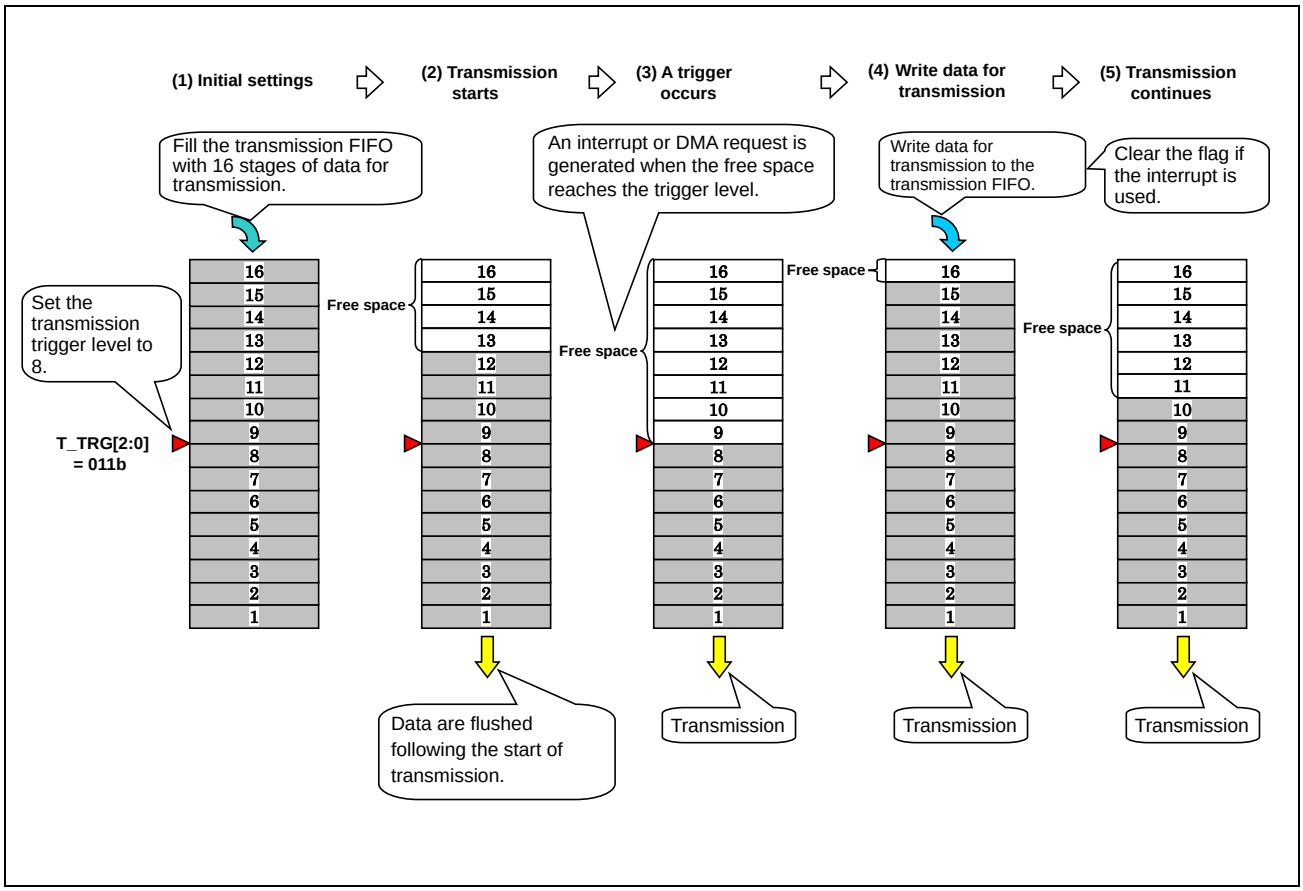


Figure 39.4-18 Operation of the Transmission FIFO when the Transmission Trigger Level is Set

39.4.11.2 Reception Trigger Level

A trigger occurs when the buffering level of the reception FIFO exceeds the specified level due to the operation for reception.

(1) Setting Procedure

Set the level at which a trigger occurs in R_TRG[2:0] of the CSI FIFO trigger level register (CSI_FIFOTRG). Also, setting the reception trigger level setting enable flag (R_TRGEN) in the CSI control register (CSI_CNT) makes the trigger level available.

To use the reception trigger level as an interrupt, set the reception trigger level interrupt enable flag (R_TRGR_E) in the CSI control register (CSI_CNT).

If the R_DMAEN bit in the CSI control register (CSI_CNT) is set to enable DMA transfer for reception, the reception trigger level can be used for the DMA transfer request for reception.

CAUTION

The settings for the reception trigger level other than the interrupt enable flag should be made while communications are stopped (CSOT bit of CSI_MODE = 0b). Operation when the settings are made during communications (when CSIE of the CSI_MODE register = 1b or CSOT = 1b) is not guaranteed.

(2) Description of Operation

A trigger occurs when the capacity in the reception FIFO reaches the setting of the reception trigger level (R_TRG[2:0] in CSI_CNT).

A trigger does not occur if the setting is exceeded when received data are read from to the reception FIFO and the amount of received data is reduced. A trigger does not also occur when the amount of data in the reception FIFO does not exceed the specified level after the occurrence of a trigger. Therefore, to continue reception by using the reception trigger level, care should be taken with management of the amount of received data in the reception FIFO in order to maintain the occurrence of triggers.

To use the reception trigger level as an interrupt, clear the reception trigger level interrupt flag (R_TRGR) in the CSI interrupt status register (CSI_INT) after reading received data from the reception FIFO following the occurrence of the reception trigger level interrupt.

When the reception trigger level is used for DMA transfer, data may remain in the reception FIFO if the amount of received data in the FIFO falls below the setting at the end of operation.

For the procedure for processing remained data in DMA transfer, see **Section 39.4.14.3, Processing for Reading the Remained Received Data in DMA Transfer**.

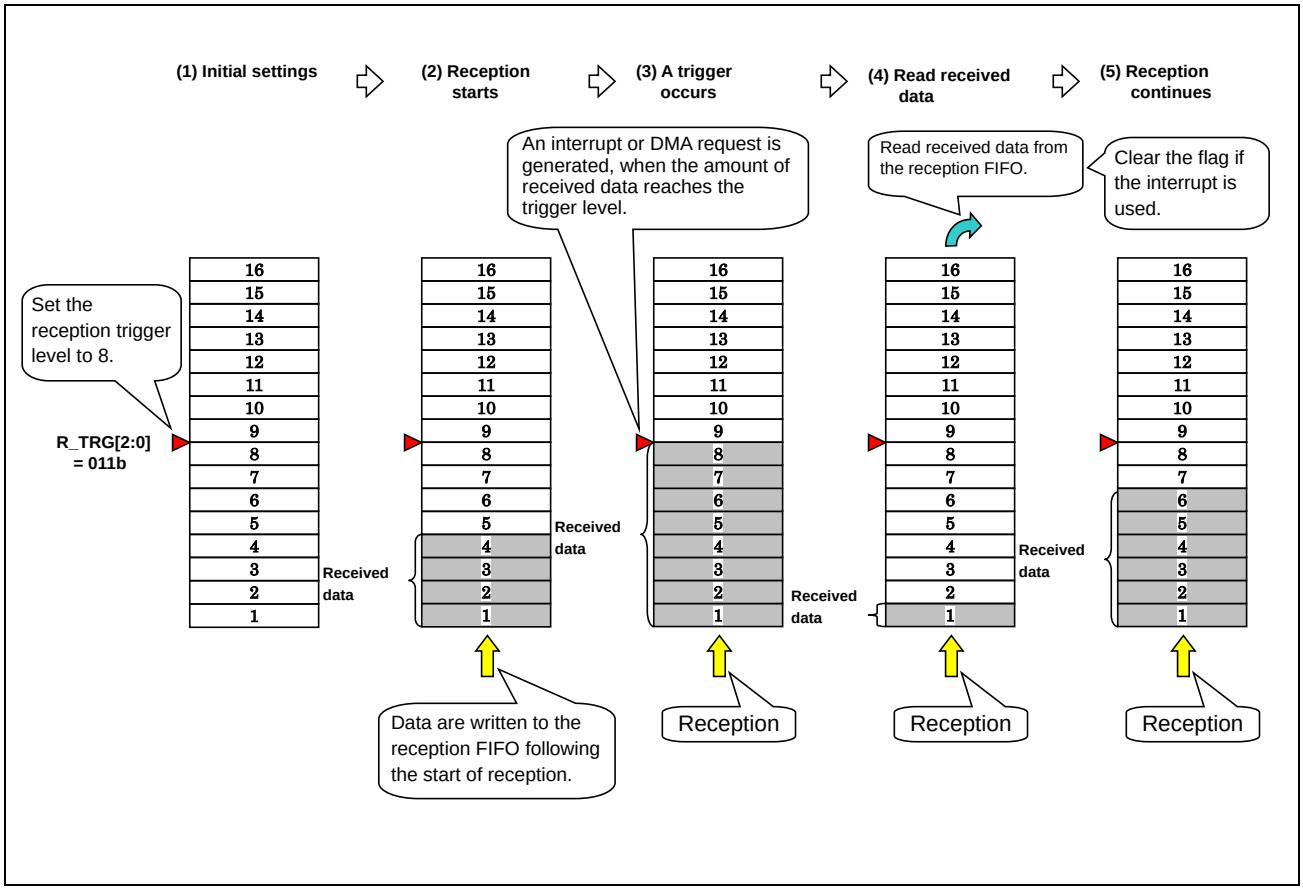


Figure 39.4-19 Operation of the Reception FIFO when the Reception Trigger Level is Set

39.4.12 Method of Data Transfer

Reading of received data from the CSI and writing of data for transmission proceeds with “interrupt transfer” or “DMA transfer”.

Whichever method of data transfer is used, the trigger level function can be used.

The method of data transfer is selected by using T_DMAEN and R_DMAEN of the CSI_CNT register. The initial setting at the time of a reset is “interrupt transfer”.

39.4.13 Interrupt Transfer

In interrupt transfer, the program handles writing of data for transmission to the transmission FIFO and reading of received data from the reception FIFO.

This method of data transfer allows flexible data processing, buffer control, and communications protocol control because data are transferred by the program, though the load on the CPU is greater than that when DMA transfer is used.

For writing of data for transmission, the all transmission completed interrupt (TREND) or transfer completed interrupt (CSIEND) are used.

For reading of received data, the transfer completed interrupt (CSIEND) is used.

In addition, the transmission and reception trigger level interrupts can be used with the use of the trigger level function.

For details of the trigger level function, see **Section 39.4.11, Trigger Level Function**.

39.4.14 DMA Transfer

In DMA transfer, the DMA controller handles writing of data for transmission and reading of received data.

This method of data transfer allows reduced CPU load and is suited to transfer large data all at once, though it does not allow flexible control compared with interrupt transfer by the program.

For writing of data for transmission, the transmission DMA request signal (DMAREQTX) is used. For reading of received data, the reception DMA request signal (DMAREQRX) is used. In addition, the transmission and reception trigger level functions can be used respectively for the transmission DMA and reception DMA requests.

DMA transfer can only be used in single transfer mode and cannot be used in block transfer mode.

Figure 39.4-20 shows an example of connection of the CSI with the DMA controller.

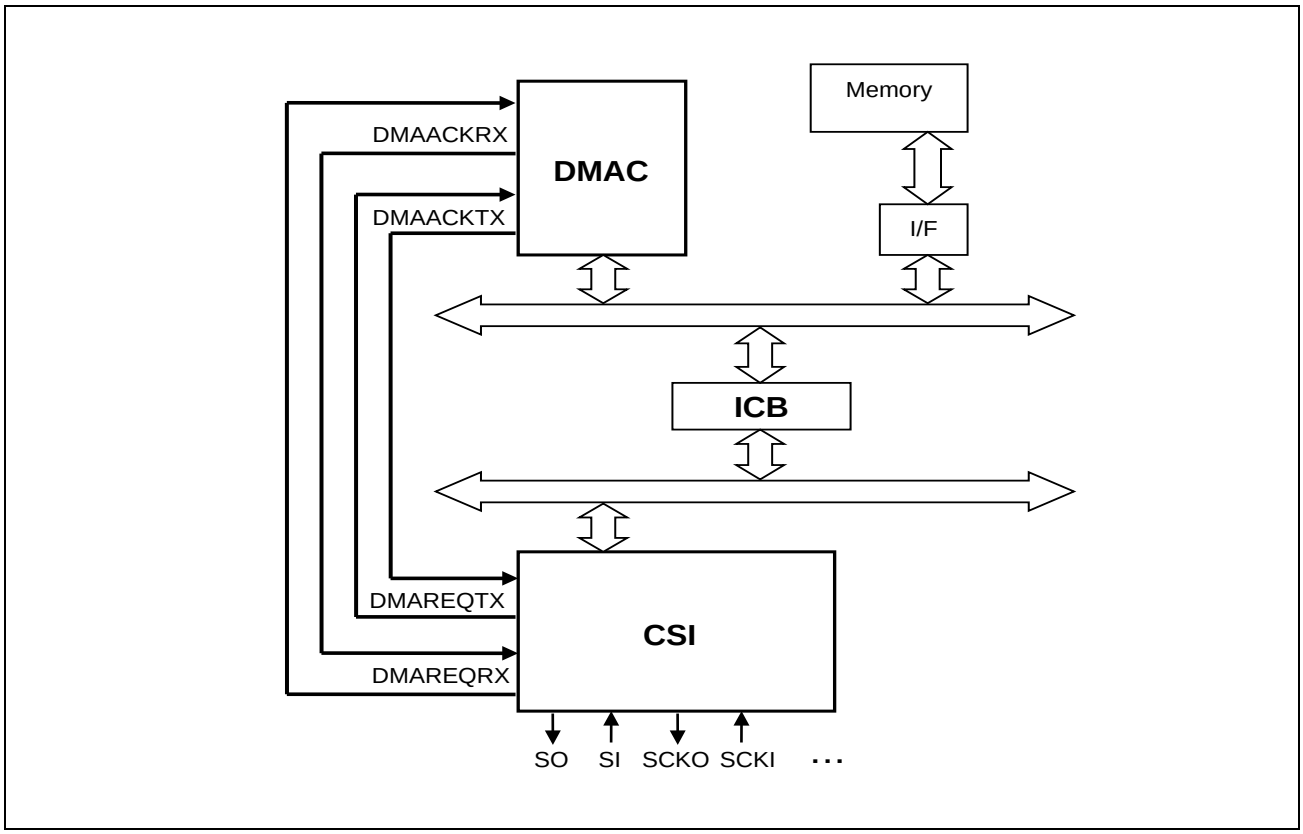
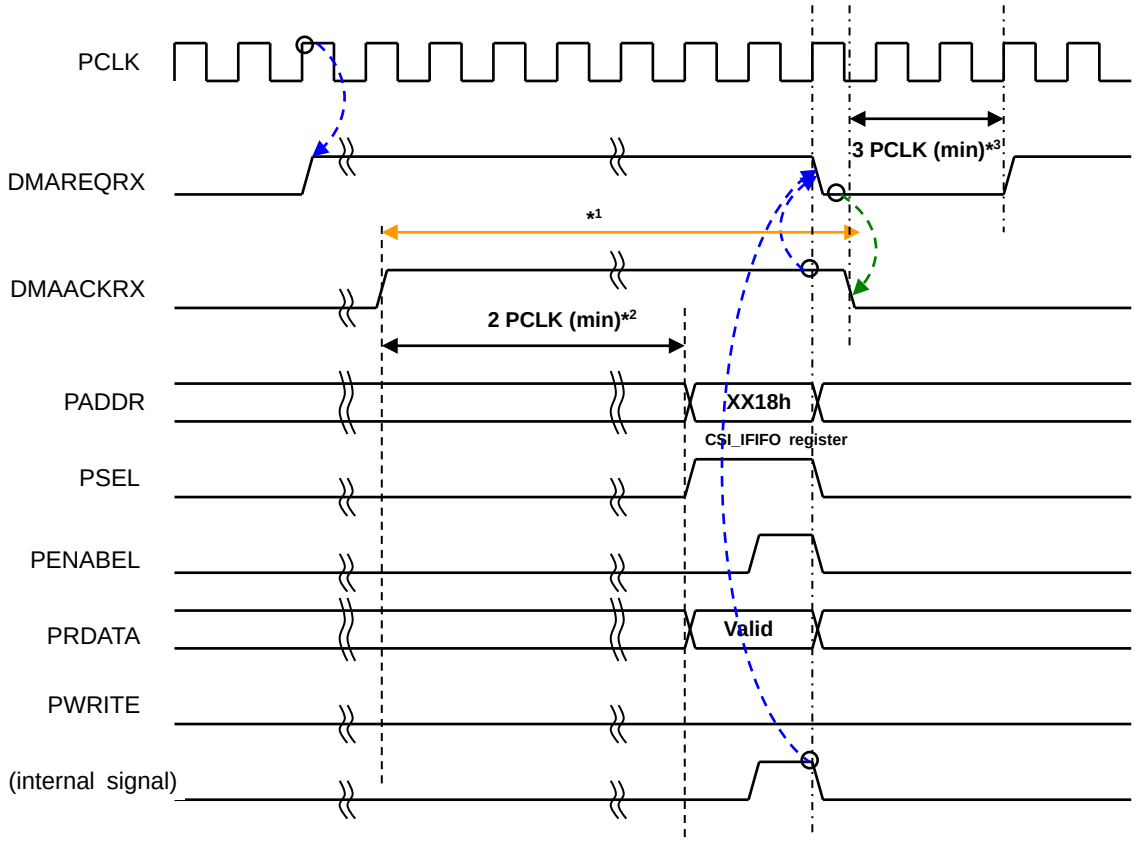


Figure 39.4-20 Basic Connection of the DMAC and the CSI

Figure 39.4-21 and **Figure 39.4-22** show the timing of interfacing with the DMA controller.

Transfer of data to and from the DMA controller proceeds in single transfer mode. Make settings for the DMA controller such that the DMA request signal and DMA acknowledge signal operate under the following conditions for both reception and transmission.

- The DMA request signals (DMAREQRX, DMAREQTX) are set to level operation mode.
- The DMA transfer mode is set to single transfer mode.
- The DMA response signals (DMAACKRX, DMAACKTX) correspond to cycles for access to the CSI register.

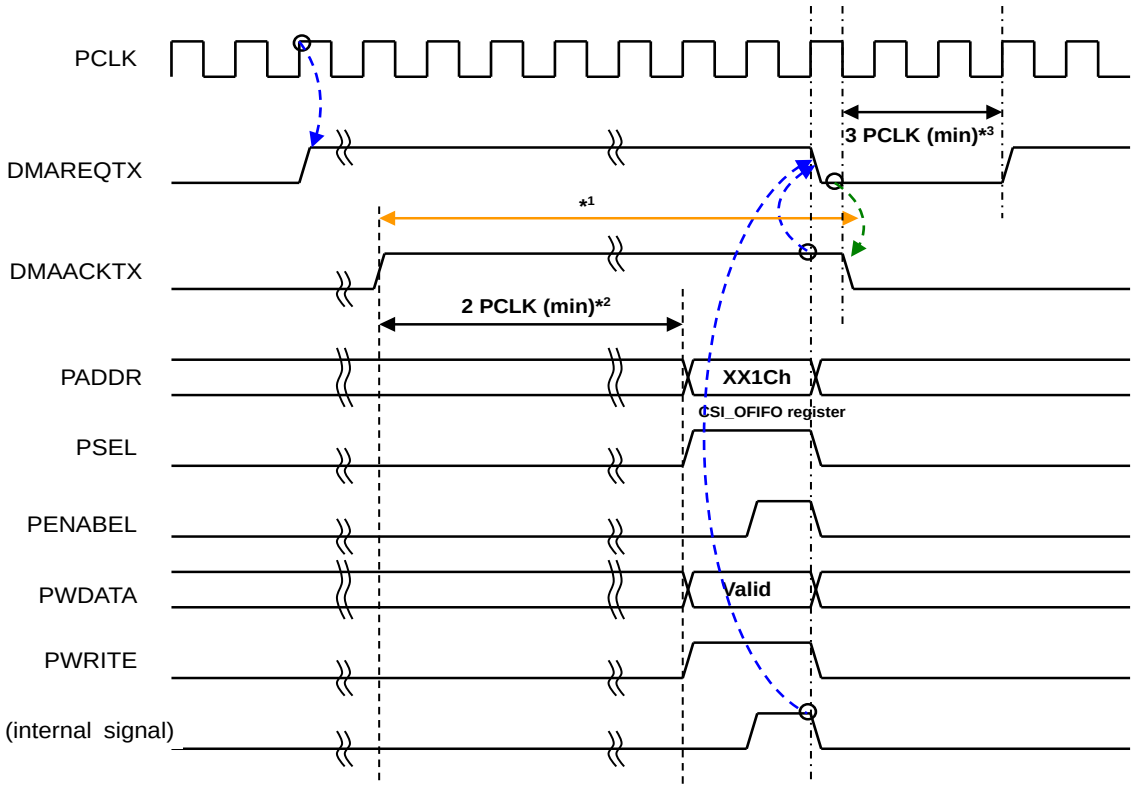


Note 1. The DMAACKRX signal should not be at the low level while the DMAREQRX signal is active.

Note 2. A cycle of reading received data from the DMAC requires a wait for at least two cycles of PCLK after the DMAACKRX signal becomes active.

Note 3. In the case of continuous DMA transfer for reception, an interval time of three or more cycles of PCLK is inserted after the DMAACKRX signal becomes inactive until the next DMAREQRX signal becomes active.

Figure 39.4-21 Timing of DMA Transfer for Reception



Note 1. The DMAACKTX signal should not be at the low level while the DMAREQTX signal is active.

Note 2. A cycle of writing data for transmission from the DMAC requires a wait for at least two cycles of PCLK after the DMAACKTX signal becomes active.

Note 3. In the case of continuous DMA transfer for transmission, an interval time of three or more cycles of PCLK is inserted after the DMAACKTX signal becomes inactive until the next DMAREQTX signal becomes active.

Figure 39.4-22 Timing of DMA Transfer for Transmission

39.4.14.1 DMA Transfer for Reception

Following the start of reception, the reception DMA request signal is output when received data are stored in the reception FIFO.

The DMA controller transfers received data to memory from the reception FIFO in response to the DMA request signal.

DMA transfer corresponds to single transfer mode and the reception DMA request signal is output every time one unit of received data is transferred.

DMA transfer for reception operates until the reception FIFO has no data.

(1) Startup Procedure

1. When DMA transfer for reception is to be used, set the reception DMA transfer enable flag (R_DMAEN) of the CSI control register (CSI_CNT).
2. Set up the DMA controller.
3. Set the startup flag for communications to start reception.

(2) End of Operation

The output of the reception DMA request is stopped when communications by the CSI are stopped and all received data in the reception FIFO are read out.

After reception by the CSI is stopped, DMA operation of the DMA controller is stopped.

To end DMA operation after all received data in the reception FIFO are read out, mask the DMA request signal by the DMA controller so as not to accept the subsequent DMA request from the CSI before stopping the CSI by a CSI reset.

Operation when a CSI reset is applied during DMA operation is not guaranteed.

(3) Restarting DMA Transfer

Transfer by the DMA controller is completed when the numbers of data transfers specified in the DMA controller are completed. However, the CSI continues to output the DMA request for reception as long as there are received data, so proceed with restarting the DMAC to continue data transfer.

(4) Reception Trigger Level

The reception trigger level function can also be used for control of DMA transfer. For the setting of the trigger level function, see **Section 39.4.11.2, Reception Trigger Level**.

In DMA transfer for reception, when the reception trigger level is set, the reception DMA request signal is output when the amount of data in the reception FIFO reaches the trigger level.

The reception DMA request signal transfers data the number of times set as the trigger level.

When the reception trigger level is used, if the amount of data in the reception FIFO is less than the setting of the trigger level on completion of communications by the CSI, the data remain in the FIFO.

Regarding processing for reading of remained data, see **Section 39.4.14.3, Processing for Reading the Remained Received Data in DMA Transfer**.

39.4.14.2 DMA Transfer for Transmission

Following the start of transmission, the transmission DMA request signal is output if the transmission FIFO has space.

The DMA controller transfers data for transmission to the transmission FIFO from memory in response to the DMA request signal.

DMA transfer corresponds to single transfer mode and the transmission DMA request signal is output every time one unit of data for transmission is written.

In DMA transfer, data transfer continues as long as the transmission FIFO has space.

(1) Starup Procedure

1. When DMA transfer for transmission is to be used, set the transmission DMA transfer enable flag (T_DMAEN) of the CSI control register (CSI_CNT).
2. Set up the DMA controller.
3. Set the startup flag for communications to start transmission.

(2) End of Operation

The output of the transmission DMA request is stopped when communications by the CSI are stopped and data are written to the transmission FIFO and it has no space.

After transmission by the CSI is stopped, DMA operation of the DMA controller is stopped.

To transmit data remained in the transmission FIFO, restart communications by the CSI and wait until the FIFO is empty.

In addition, if the transmission DMA transfer request can be masked by the DMA controller, stop the DMA controller before stopping communications, then send all data in the transmission FIFO and stop communications.

(3) Restarting DMA Transfer

Transfer by the DMA controller is completed when the numbers of data transfers specified in the DMA controller are completed. However, the CSI continues to output the DMA request for transmission as long as the transmission FIFO has space, so proceed with restarting the DMAC to continue data transfer.

(4) Transmission Trigger Level

The transmission trigger level function can also be used for control of DMA transfer. For the setting of the trigger level function, see **Section 39.4.11.1, Transmission Trigger Level**.

When the transmission trigger level is set, the transmission DMA request signal is output when the free space in the transmission FIFO is equal to or greater than the trigger level.

The transmission DMA request signal by the transmission trigger level transfers data the number of times set as the trigger level.

If the free space in the FIFO does not reach the trigger level due to the transmission proceeding while data are transferred to the transmission FIFO by the DMA controller, data are further transferred the number of times set as the trigger level.

39.4.14.3 Processing for Reading the Remained Received Data in DMA Transfer

In DMA transfer of received data, the DMA controller reads the amount of received data set as the trigger level from the reception FIFO by the DMA controller. Therefore, data newly received during DMA transfer remain in the FIFO until DMA transfer is completed once and the amount of data reaches the trigger level the next time.

If the amount of data in the FIFO does not reach the trigger level on completion of communications, the received data remain in the FIFO. In such cases, the remained received data can be read through the following processing procedure.

(1) Processing for Reading in DMA Transfer (Changing the Trigger Level Setting to the Disabled Setting)

If data remain in the reception FIFO, disabling the trigger level setting asserts DMAREQRX and the remained data are transferred by the DMAC.

The following shows the procedure.

1. Check that the communications state flag of the CSI indicates that communications are stopped (CSOT in CSI_MODE is 0b).
2. Disable the reception FIFO trigger level setting (R_TRGEN in CSI_CNT = 0b).
3. Wait until DMA transfer by the DMA controller is completed.
4. Check that the value of the CSI reception FIFO level indication register (CSI_IFIFOL) is 0b.

(2) Processing for Reading by the Program

The received data are read from the CSI reception window register (CSI_IFIFO) until the value of the CSI reception FIFO level indication register becomes 0 and the data are written to the reception buffer. Since the DMAC is not used, management of the buffer is required.

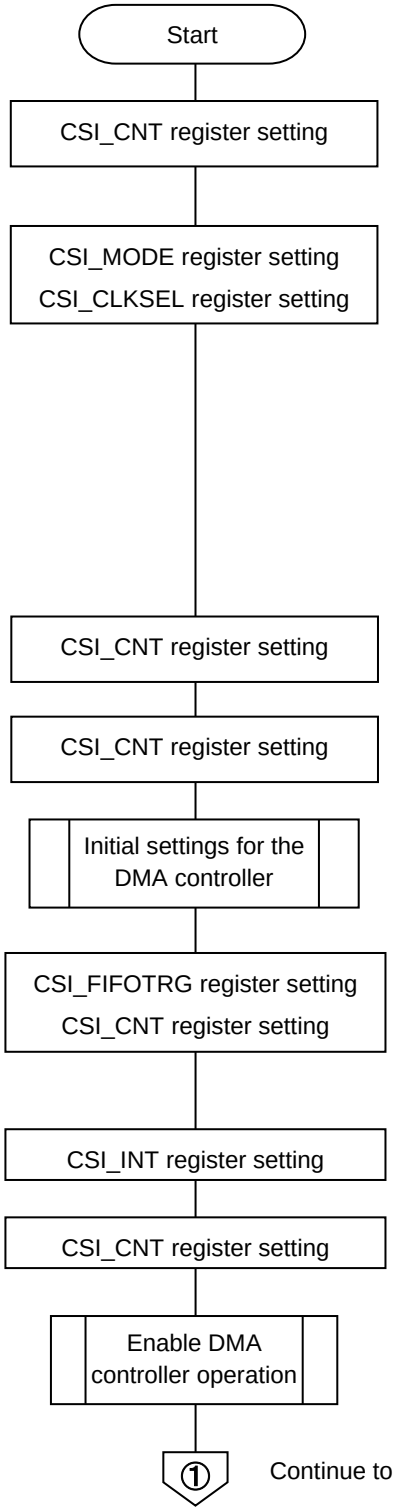
The following shows the procedure.

1. Check that the communications state flag of the CSI indicates that communications are stopped (CSOT in CSI_MODE is 0b).
2. Repeat the following operations until the value of the CSI reception FIFO level indication register (CSI_IFIFOL) becomes 0b.
3. Read the received data from the CSI reception window register (CSI_IFIFO).
4. Write the read data to the reception buffer.

39.4.14.4 Settings in Master Transmission/Reception Mode with the Use of DMA Transfer and Flow of Operations

The figure below shows example settings and a flow of operations when DMA transfer is used in master transmission/reception mode

For the specifications of the registers of the DMAC, refer to the section of DMAC.



(1) De-asserting the CSI reset and selecting the method of data transfer
- De-assert the CSI reset (CSIRST = “0b”).
- Select DMA transfer for transmission (T_DMAEN = “1b”).
- Select DMA transfer for reception (R_DMAEN = “1b”).
- Mask the interrupt.

(2) Setting the mode, the serial data format, and the serial clock
- Set the operating mode to master transmission/reception mode.
- Set a interval time between transfers to 2 wait cycles.
- Set the serial data format.
  Data length: 8 bits
  First bit: MSB
- Set the serial clock.
  Polarity: Low level
  Data phase: Sampling after half a cycle
  Division ratio: 1/4

(3) CSI reset
- Apply a CSI reset and enable the setting of CSI_CLKSEL.

(4) De-asserting the CSI reset

(5) Initial settings for the external DMA controller
- See **Figure 39.4-23 (3/3)**.

(6) Setting the transmission and reception trigger levels
- Set the transmission trigger level to 8.
- Set the reception trigger level to 8.
- Enable the transmission trigger level setting.
- Enable the reception trigger level setting.

(7) Clearing the interrupt sources and removing masking
- Clear all the interrupt source flags.

(8) Enabling the interrupt
- Enable the interrupt to be used.

(9) Enabling DMA controller operation
- Use the enable register for the DMA controller to enable DMA operation.

① Continue to the next page

Figure 39.4-23 Flow of Operations of DMA Transfer in Master Transmission/Reception Mode (Continuous Data Transmission) (1/3)

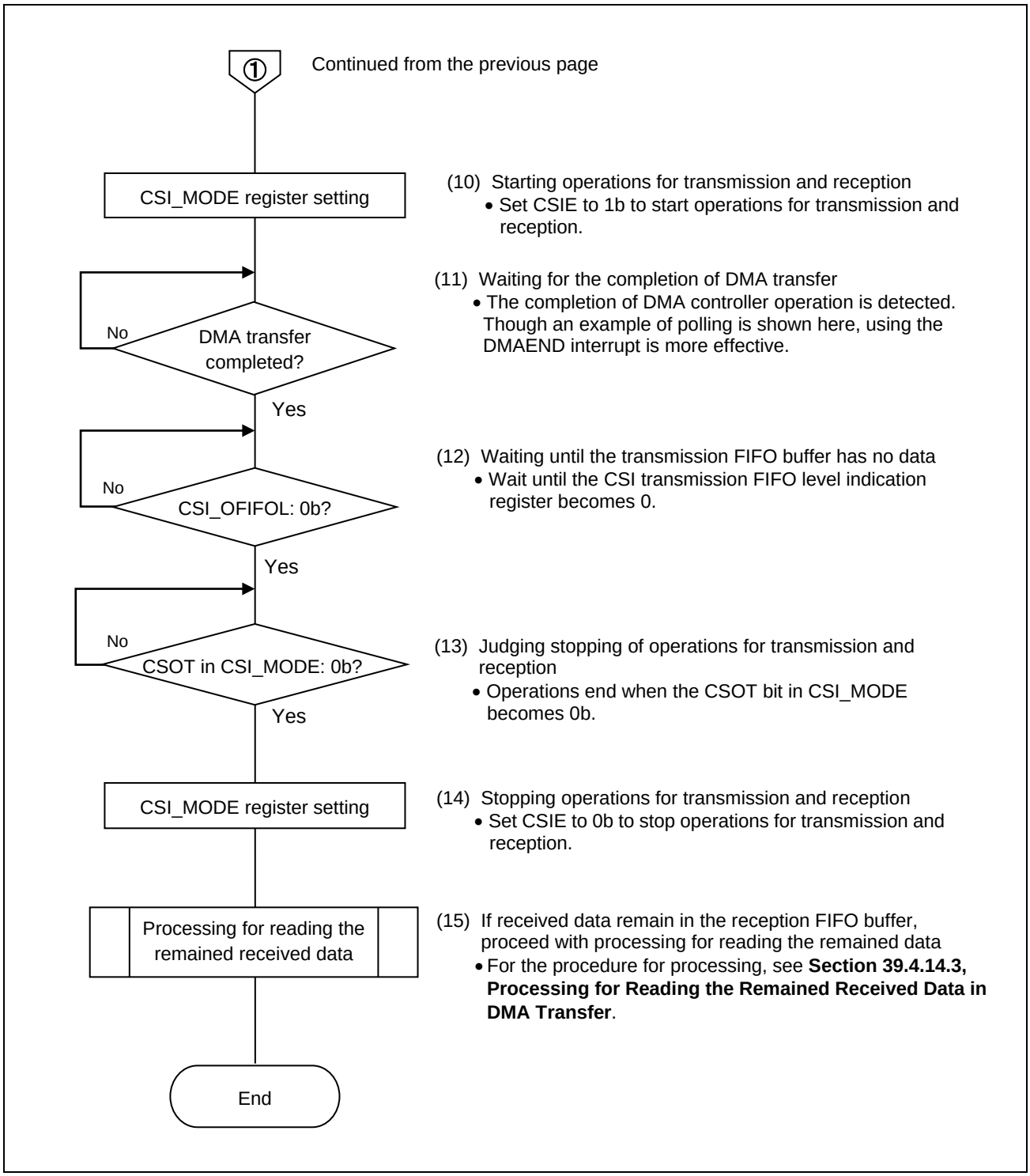


Figure 39.4-23 Flow of Operations of DMA Transfer in Master Transmission/Reception Mode (Continuous Data Transmission) (2/3)

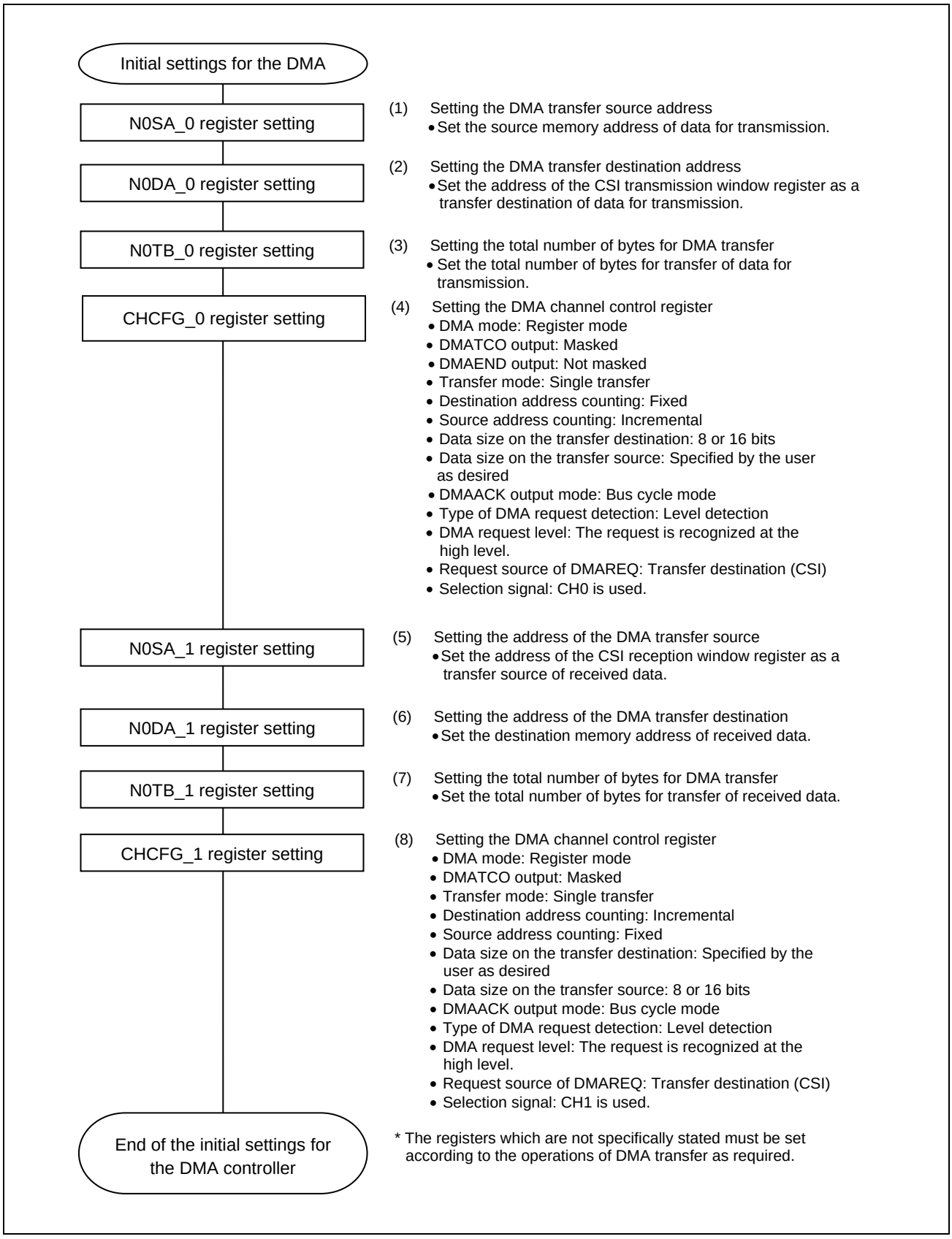


Figure 39.4-23 Flow of Operations of DMA Transfer in Master Transmission/Reception Mode (Continuous Data Transmission) (3/3)

39.5 Timing Chart

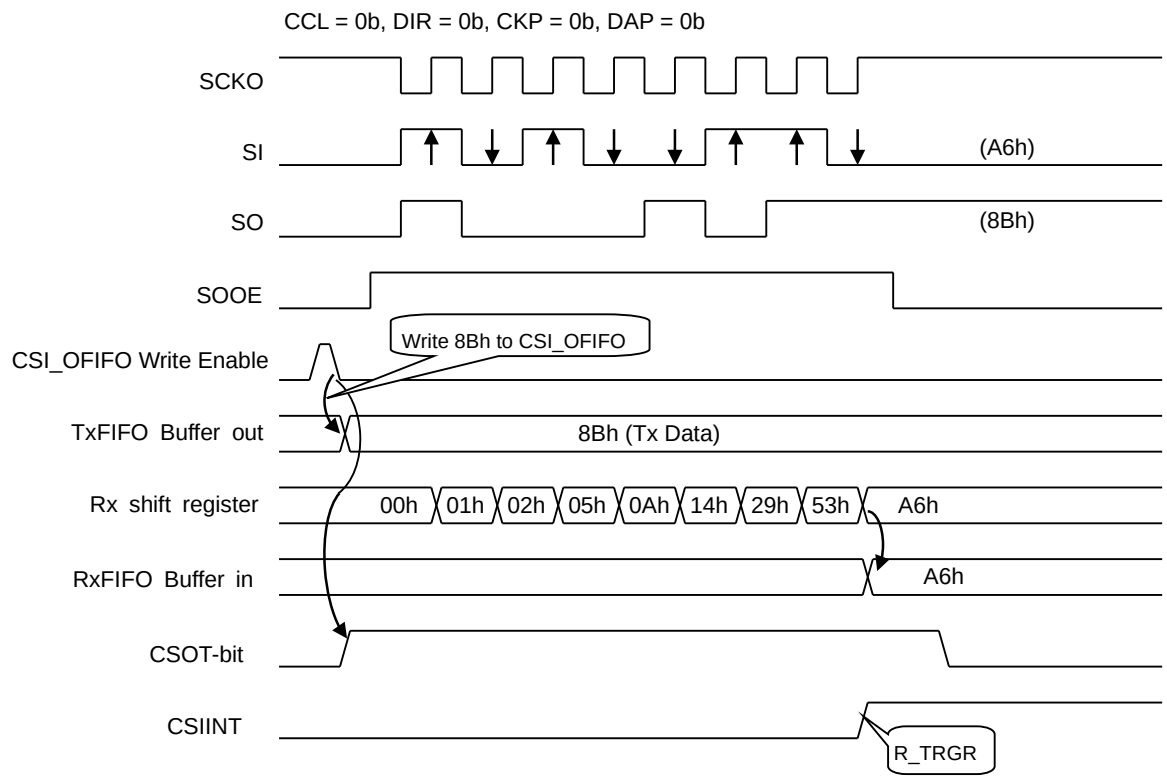
39.5.1 Timing of Serial Communications (Single-Word Transfer)

The following shows the timing of operation for single-word transfer.

Figure 39.5-1 is a timing chart for transmission and reception of a single unit of data.

＜Operating Conditions＞

- Data length: 8 bits
- MSB Start of data: MSB
- Polarity of the clock: High level
- Phase of data: The same phase as that of SCK
- Data for transmission: 8Bh
- Data for reception: A6h



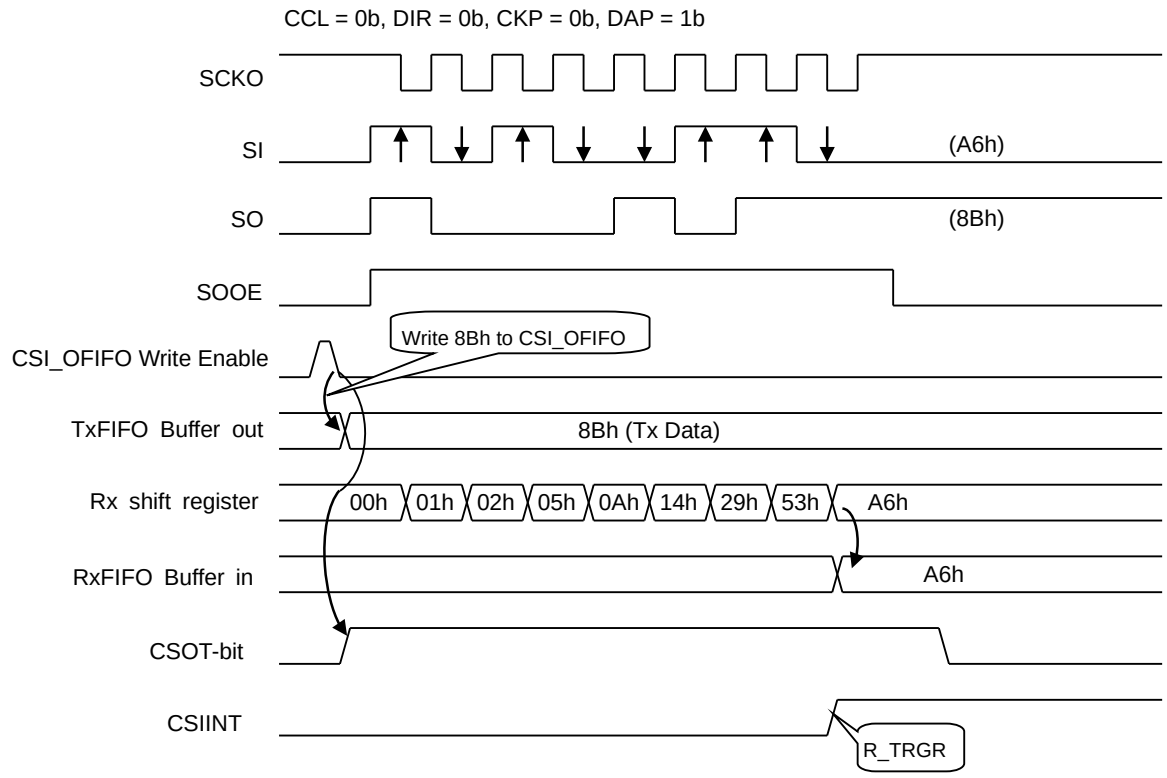
Note: An arrow (↑ or ↓) shows the timing of sampling of the SI signal.

Figure 39.5-1 Timing of Single-Word Transfer (in Master Transmission/Reception Mode)

Figure 39.5-2 is a timing chart for transmission and reception of a single unit of data in master transmission/reception mode.

＜Operating Conditions＞

- Data length: 8 bits
- Start of data: MSB
- Polarity of the clock: High level
- Phase of data: Half a cycle after SCK
- Data for transmission: 8Bh
- Data for reception: A6h



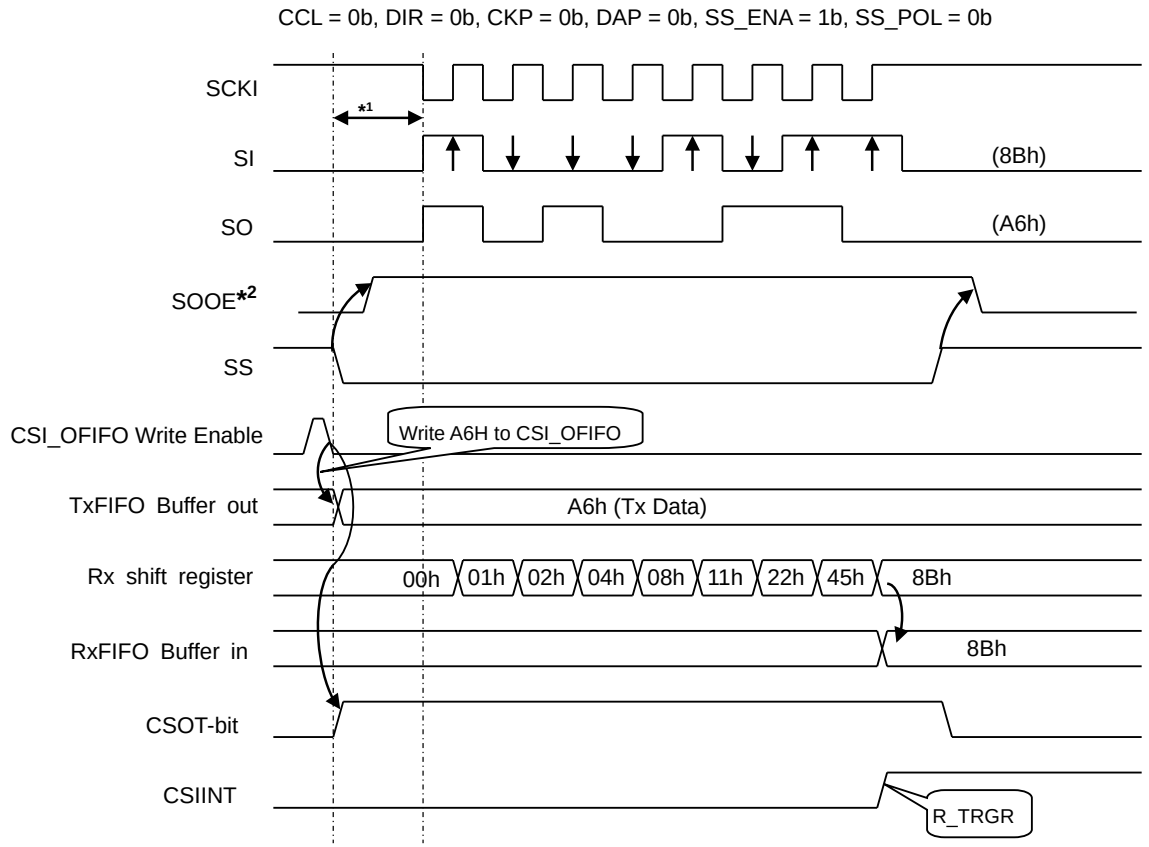
Note: An arrow (↑ or ↓) shows the timing of sampling of the SI signal.

Figure 39.5-2 Timing of Single-Word Transfer (in Master Transmission/Reception Mode)

Figure39.5-3 is a timing chart for transmission and reception of a single unit of data in slave transmission/reception mode.

＜Operating Conditions＞

- Data length: 8 bits
- Start of data: MSB
- Polarity of the clock: High level
- Phase of data: The same phase as that of SCK
- Data for transmission: A6H
- Data for reception: 8BH



Note: An arrow (↑ or ↓) shows the timing of sampling of the SI signal.

Note 1. The master must assert the SS pin before starting communications (at least four PCLK cycles before). If there is no sufficient interval between the start of communications and the assertion of the SS pin, transmission or received data may be destroyed due to bit shifting.

Note 2. When the SS pin is in use, the SOOE signal becomes active at least two clock cycles of the APB bus clock (PCLK) after the assertion of the SS pin.
When the SS pin is not in use, if operation is in transmission/reception mode, the SOOE signal is always active regardless of the state of the SS pin after starting communications.

Figure39.5-3 Timing of Single-Word Transfer (in Slave Transmission/Reception Mode)

39.5.2 Timing of Serial Communications (Continuous Data Transfer)

The figure below shows the timing of operation for continuous data transfer.

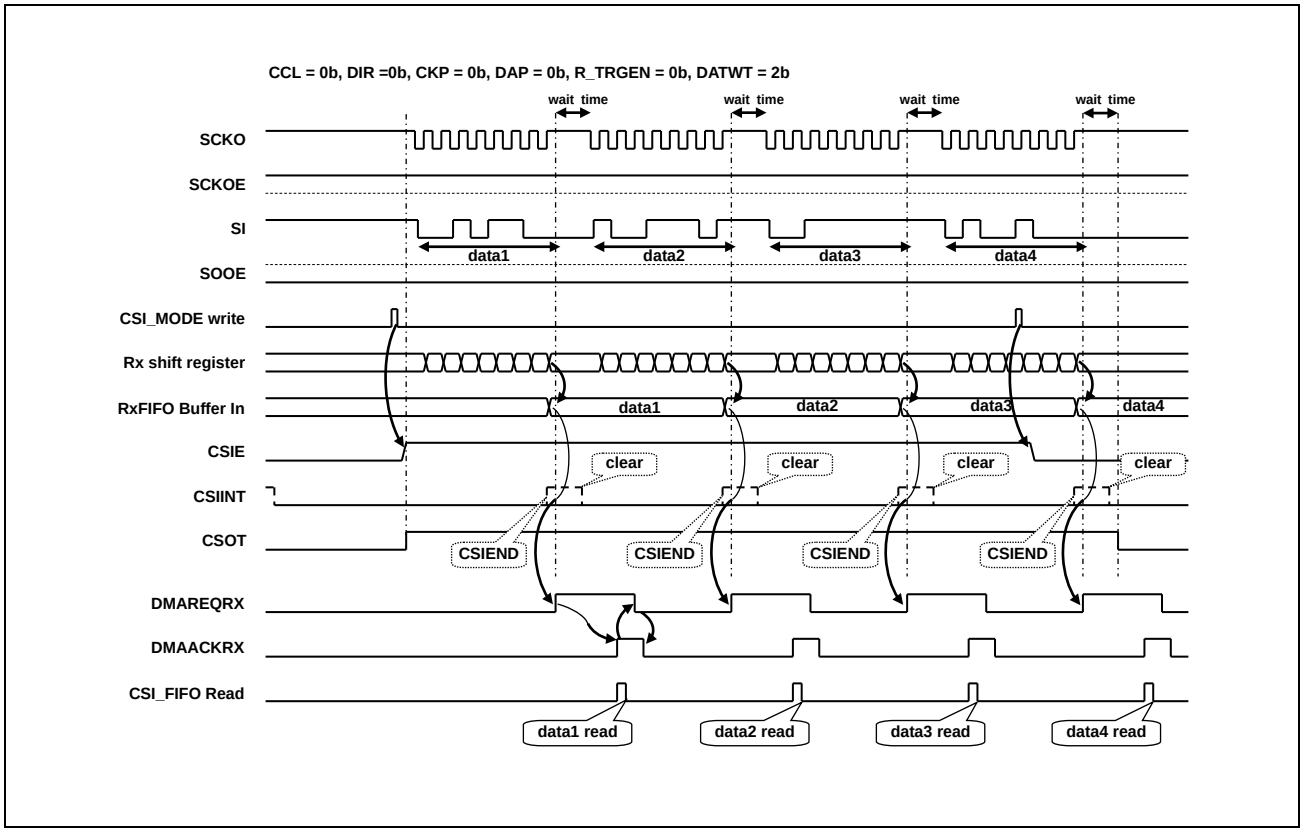


Figure 39.5-4 Timing of Continuous Transfer (in Master Reception-only Mode)

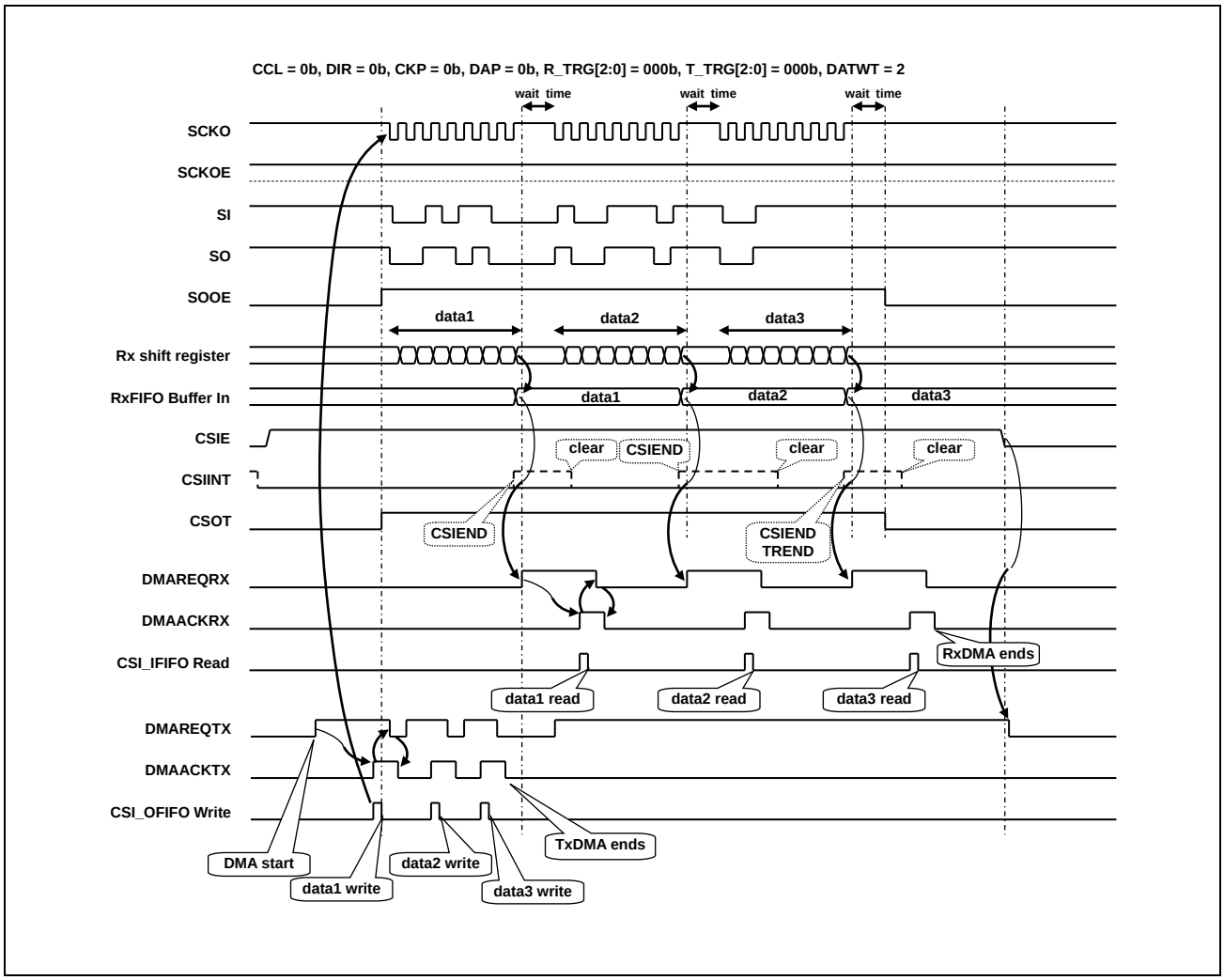


Figure 39.5-5 Timing of Continuous Transfer (in Master Transmission/Reception Mode)

When the startup flag for communications is set, the transmission DMA request signal (DMAREQTX) is asserted to start DMA transfer.

Writing the first data to the transmission FIFO buffer with DMA transfer starts operations for transmission and reception.

When DMA transfer of data for transmission is completed, wait for the completion of transmission and poll the communications state flag (CSOT).

Check that communications are stopped by reading the communications state flag and clear the startup flag for communications (CSIE).

Clearing the startup flag for communications (CSIE) de-asserts the transmission DMA request signal (DMAREQTX).

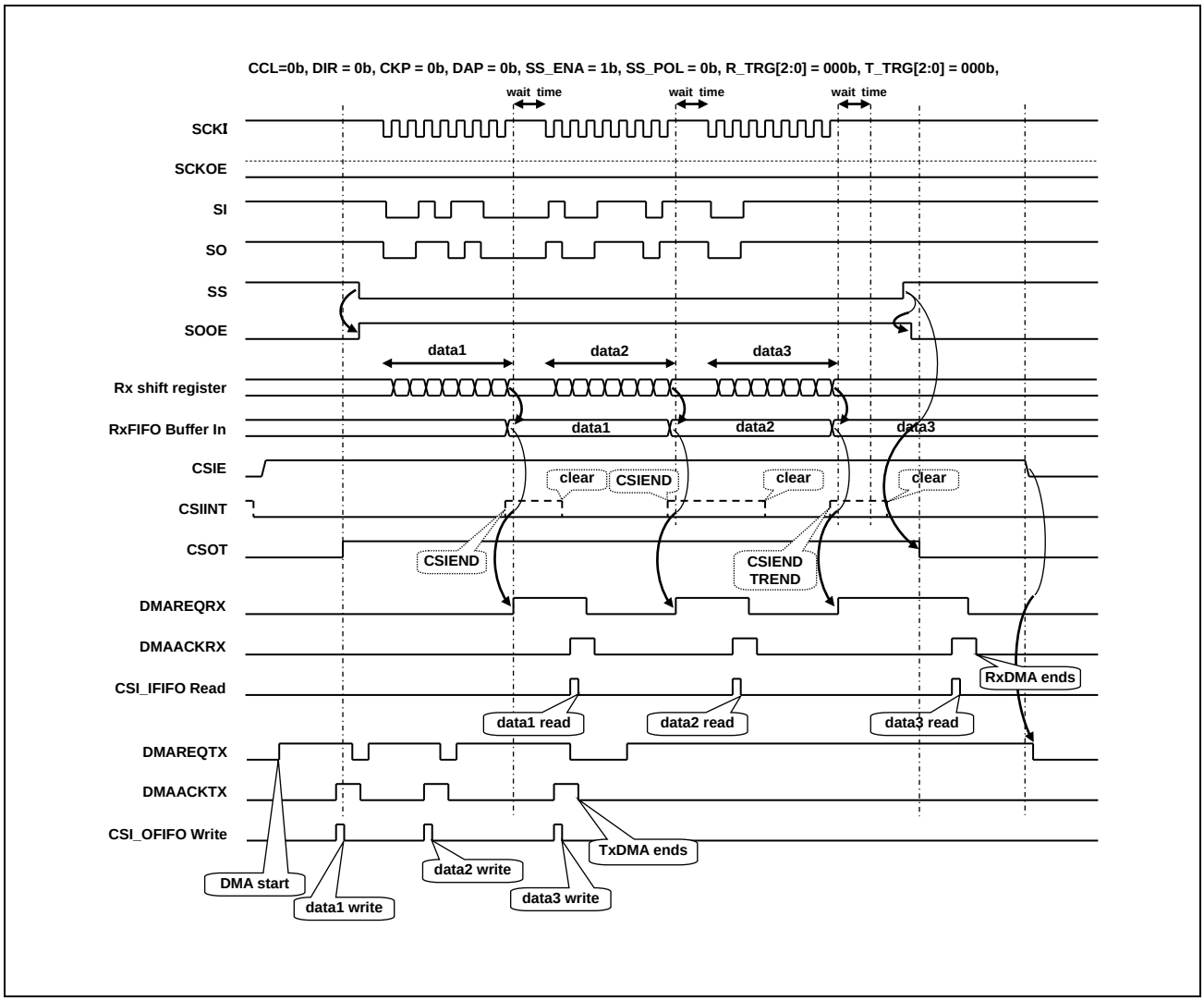


Figure 39.5-6 Timing of Continuous Transfer (in Slave Transmission/Reception Mode)

When the startup flag for communications is set, if the transmission FIFO has space, the transmission DMA request signal (DMAREQTX) is asserted to start DMA transfer.

Writing the first data to the transmission FIFO buffer with DMA transfer completes preparation for starting operations for transmission and reception.

Operations for transmission and reception start when the slave selection pin (SS) is asserted by the master and the serial clock (SCKI) is input.

Note that the slave selection signal requires at least four PCLK cycles of the setup time relative to the timing for starting communications. If a sufficient setup time is not secured, bit shifting of transfer data occurs and data may be destroyed.

Operations for transmission and reception are stopped when the slave selection signal is de-asserted.

To complete operations for communications by the slave, check that operations for transmission and reception have been stopped by reading the communications state flag (CSOT) and then clear the startup flag (CSIE).

Clearing the startup flag for communications (CSIE) de-asserts the transmission DMA request signal (DMAREQTX).

39.6 Usage Notes

39.6.1 Notes on the Communications Speed

The following illustrates an example with the polarity of the clock and the phase when the CKP bit = 0 and the DAP bit = 0 in the CSI_CLKSEL register. In the case of other settings, consider the case with the polarity of the clock and the phase corresponding to these settings.

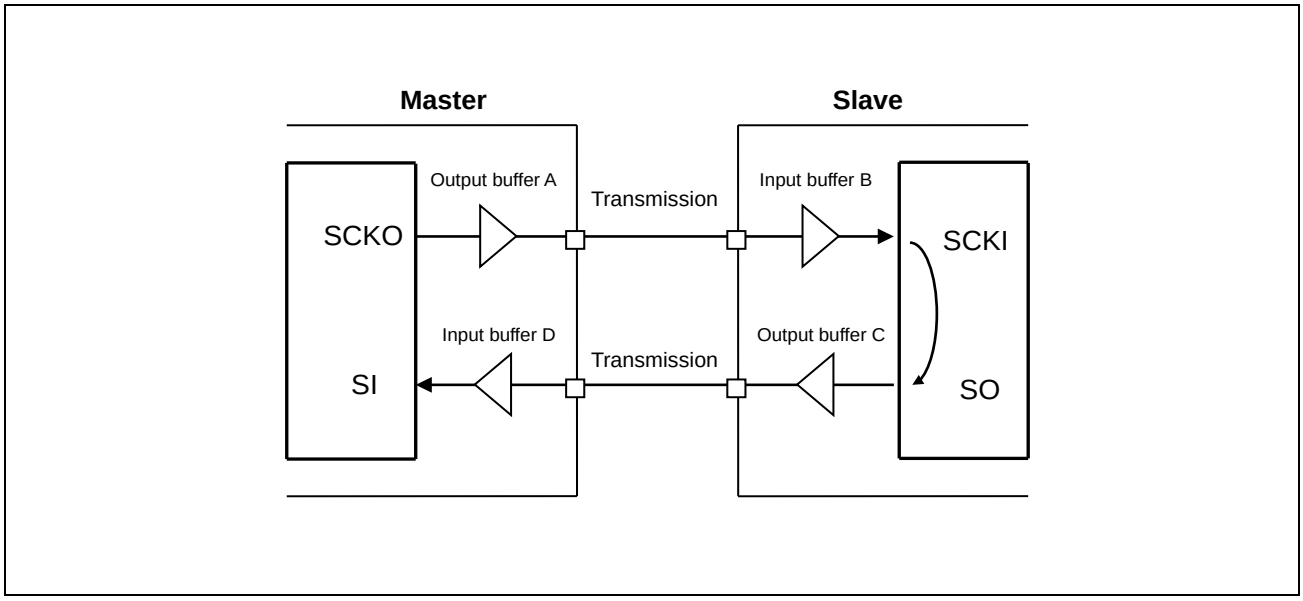


Figure 39.6-1 Master and Slave Connection

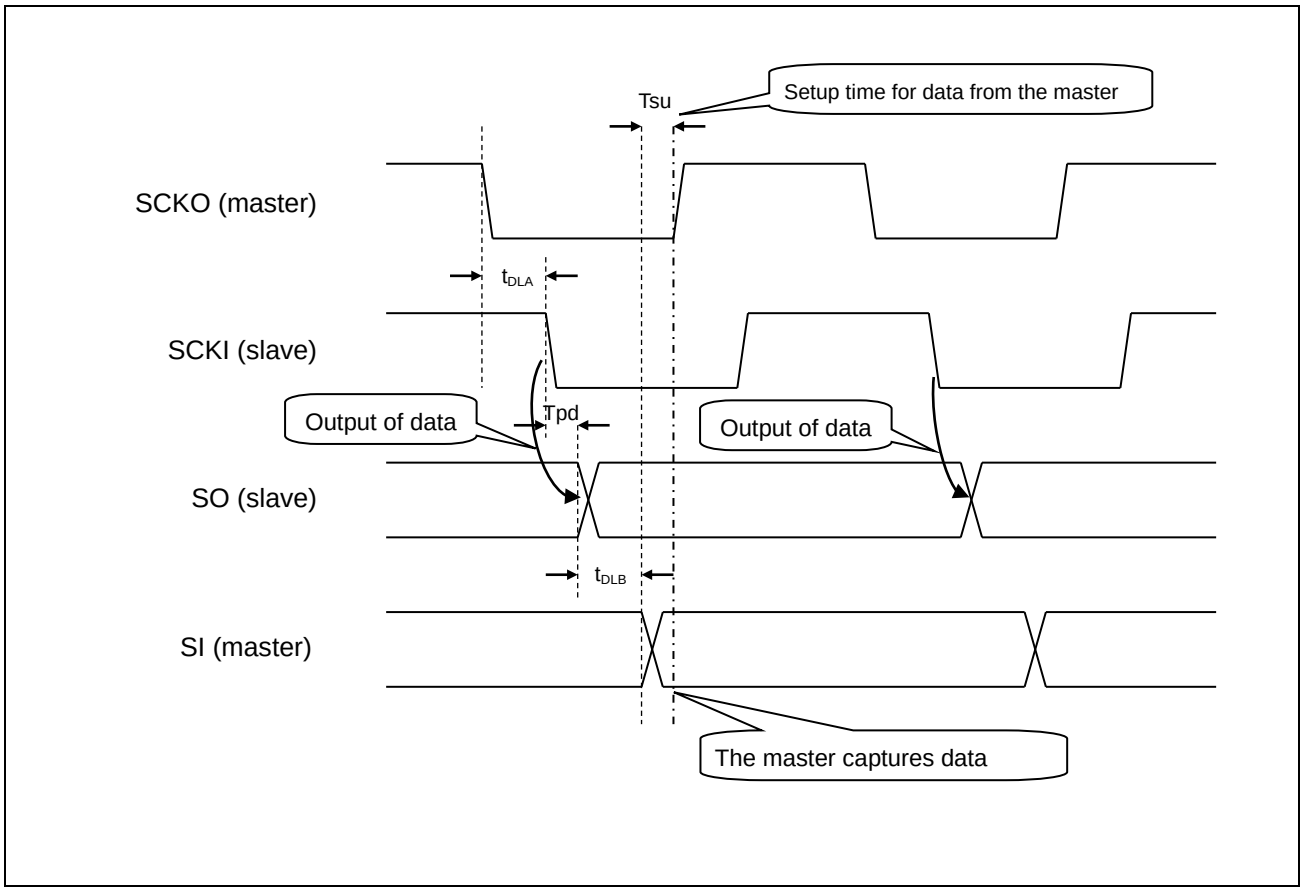


Figure 39.6-2 Timing of Data Reception by the Master

Serial data (SI) are sampled by the master on the edge of half a cycle of the serial clock (SCKO).

Figure 39.6-2 shows the timing of data reception by the master.

The slave outputs data for transmission to the SO pin on rising edges of the serial clock SCK signal from the master.

The master captures data for transmission from the slave on rising edges of SCK.

Calculate the highest frequency of the serial clock from the time which is required for the master to receive serial data from the slave.

$$\frac{\text{Serial clock frequency}}{2} > t_{DLA} + Tpd + t_{DLB} + Tsu$$

t_{DLA}: Delay of output buffer A and input buffer B and signal delay in the transmission path of SCK

Tpd: Delay of SO from SCKI of the slave

t_{DLB}: Delay of output buffer C and input buffer D and signal delay in the transmission path of SO

Tsu: Setup time for data from the master

When the serial clock is used at 25 MHz, design such that the above value is within 20 ns.

Section 40 Universal Asynchronous Receiver/Transmitter (UART)

This section describes the functions of a universal asynchronous receiver/transmitter (UART).

40.1 Overview

The UART includes two 64-byte FIFO buffers, one for transmission and has functional compatibility with the general-purpose 16750 UART chip.

This LSI has two channels of UART, ch. 0 and ch. 1. Of those, ch. 1 is for use with the ISP support package, so do not use registers related to this channel.

In addition, DMAC is for use with the ISP support package, so do not use the DMA transfer using the DMA interface of the UART.

40.1.1 Features

- Register-compatible with the general-purpose 16750 UART chip
- Two 64-byte FIFO buffers are included, one for transmission and one for reception. One of the following operating modes is selectable by settings.
  - Non-FIFO mode (16450 mode)
  - 16-byte FIFO mode (16550 mode)
  - 64-byte FIFO mode
- The reception FIFO buffer includes a 3-bit (PE: Parity error, FE: Framing error, BI: Break interrupt) error data register.
- Programmable auto-RTS and auto-CTS are supported.
  (DSR, DTR, RI, and DCD are not supported.)
- Start, stop, and parity bits as the standard asynchronous transfer control bits can be appended to serial data for transmission and handled in received data. The following forms of programmable control are available.
  - Character length control: 5, 6, 7, or 8 bits
  - Parity bit control: Even, odd, or no parity
  - Stop-bit length control: 1 or 2 bits
  - Baud rate control: The on-chip baud rate generator allows selection of the desired bit rate.
    Supports major baud rates (such as 9600 bps, 19200 bps, 38400 bps, 57600 bps, and 115200 bps)
- CTS and RTS are supported for the modem control interface.
- Various status registers and an interrupt generation circuit with priority control are included.
- DMA interface supported
- Loopback function supported
- Asynchronous clock signals can be input as the bus clock and serial clock signals.

- The frequency of the bus clock (PCLK) must be greater than the frequency of the bit-rate generator output clock (the clock signal produced by frequency dividing the serial clock (SCLK)).
- 1-bit sampling in 16 clock cycles of the bit-rate generator output clock

40.1.2 Connection Configuration

Figure 40.1-1 shows the connection configuration of the UART.

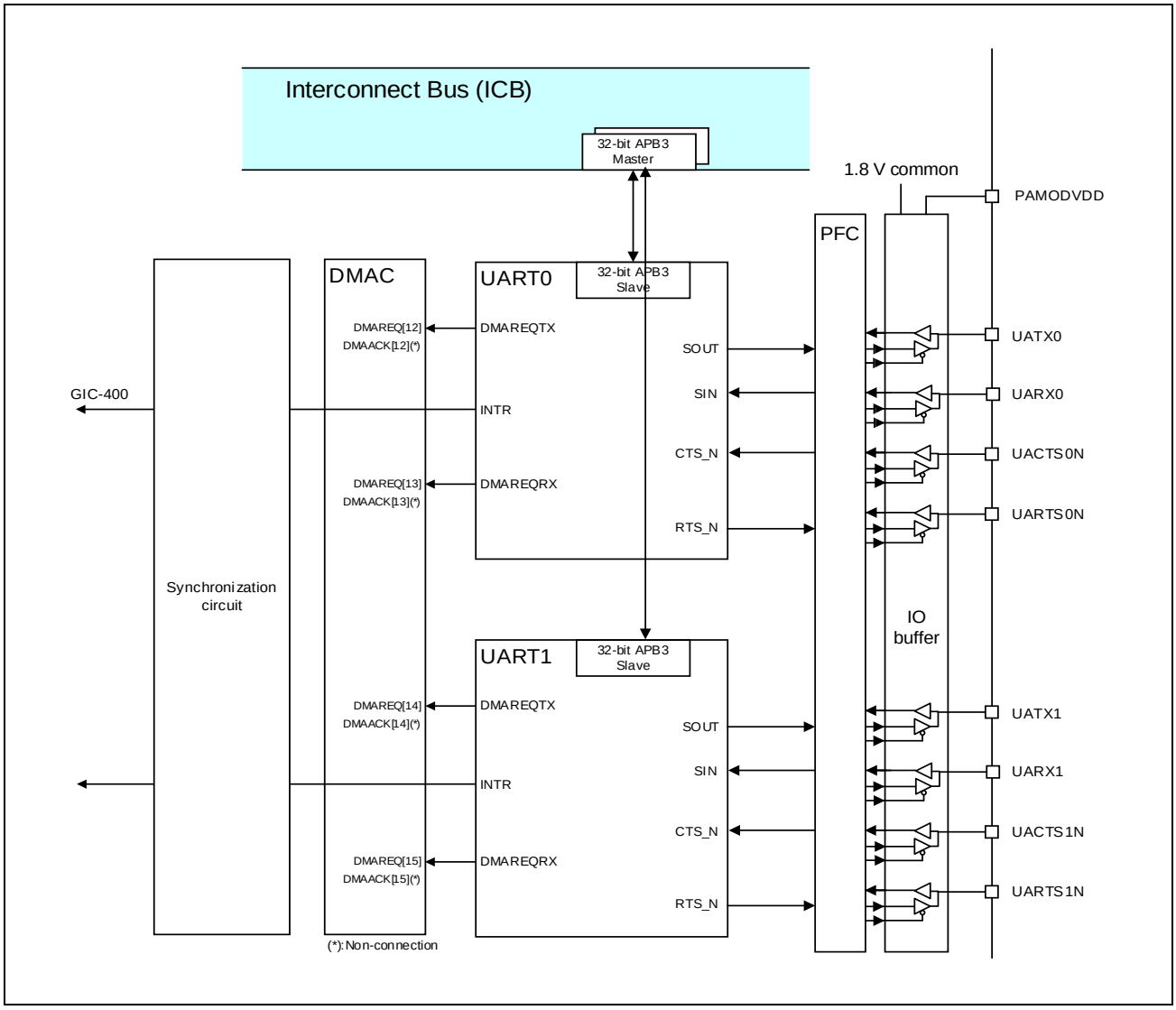


Figure 40.1-1 Connection Configuration

40.2 Pin Functions

40.2.1 List of Internal Pins

Table 40.2-1 lists the internal pins of the UART.

Table 40.2-1 List of Interface Pins

Classification	Pin name	I/O	Function
Serial Interface Pins	CTS_N	Input	Modem status signal (Clear to Send)
	SIN	Input	Serial data input
	RTS_N	Output	Transmission request signal for modem control (Request to Send)
	SOUT	Output	Serial data output After a reset, the high level is output when operation is in loopback mode.
	SCLK	Input	Serial clock input for baud-rate generation
DMA Interface Pins	DMA_TX_REQ	Output	DMA request signal for transmission. The high level is output when a DMA request is issued. There are two DMA modes for the FIFO buffer when it is in use. One is for single DMA transfers and the other is for multiple DMA transfers. Either is selectable. For details, see **Section 40.3.3.4, FIFO Control Register (URTm_FCR) (m = 0 to 1)**).
	DMA_RX_REQ	Output	DMA request signal for reception. The high level is output in response to a DMA request. When the FIFO buffer is in use, either of the two DMA modes is selectable as with transmission. For details, see **Section 40.3.3.4, FIFO Control Register (URTm_FCR) (m = 0 to 1)**).
Interrupt Pin	INTR	Output	Interrupt (level output). The high level is output when any of the following interrupt source conditions is satisfied. [Interrupt sources] 1) Reception error 2) Completion of the reception or a timeout (only when the FIFO buffer is in use) 3) The transmission buffer being empty 4) Modem status Which interrupt sources to include is controllable by the interrupt enable register, IER. The INTR signal is reset to the low level from within the given interrupt processing or by a master reset.

40.3 Register Descriptions

For the register base addresses (<URT0_S0_base> and <URT1_S0_base>), see the section Address Map.

40.3.1 List of Registers

The registers are readable and writable in 32-bit units, but only the 8 lower-order bits are actually functional (so 1-byte access is equally effective) as shown in **Table 40.3-2.**

Table 40.3-1 List of Registers

DLAB (LCR[7])*1	Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
x	00h	Receiver Buffer Register (when reading received data)	URTm_RBR	0000_0000h	32
		Transmitter Holding Register (when writing transmission data)	URTm_THR	0000_0000h	32
x	04h	Interrupt Enable Register	URTm_IER	0000_0000h	32
x	08h	Interrupt Ident. Register	URTm_IIR	0000_0001h	32
x	0Ch	FIFO Control Register	URTm_FCR	0000_0000h	32
x	10h	Line Control Register	URTm_LCR	0000_0000h	32
x	14h	Modem Control Register	URTm_MCR	0000_0000h	32
x	18h	Line Status Register	URTm_LSR	0000_0060h	32
x	1Ch	Modem Status Register	URTm_MSR	0000_0000h	32
x	20h	Scratch Register	URTm_SCR	0000_0000h	32
1b	24h	Divisor Latch LS Byte	URTm_DLL	0000_0000h	32
1b	28h	Divisor Latch MS Byte	URTm_DLM	0000_0000h	32
x	2Ch	HW Control Register0	URTm_HCR0	0000_0000h	32
x	30h	HW Status Register 2	URTm_HCR2	0000_0000h	32
x	34h	HW Status Register 3	URTm_HCR3	0000_0000h	32
x	38h	Reserved*2	—	—	32
x	3Ch	Reserved*2	—	—	32
x	40h	RFU*3	—	—	32
x	44h	RFU*3	—	—	32
x	48h	RFU*3	—	—	32
x	4Ch	RFU*3	—	—	32
x	50h	RFU*3	—	—	32
x	54h to 7Ch	Reserved*2	—	—	32

Note: x: Don't care; m = 0, 1

Note 1. LCR7: Bit 1 in the line control register
For the setting, see **Section 40.5, Operation**. When LCR[7] is set to 0b, access to DLL and DLM is disabled and generation of a 16x baud rate clock is started.

Note 2. The reserved area is not used. It is always read as 0b.

Note 3. Access to the RFU area is prohibited.

Table 40.3-2 List of Registers (Detail) (1/2)

Offset Address	Register Name	Description								
00h	URTm_RBR (Read Only) Receiver Buffer Register	b31 to b8	b7	b6	b5	b4	b3	b2	b1	b0
		0000_0000_0000_0000_0000_0000b	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
	URTm_THR (Write Only) Transmitter Holding Register	— *1	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
		b31 to b8	b7	b6	b5	b4	b3	b2	b1	b0
04h	URTm_IER (R/W) Interrupt Enable Register	0000_0000_0000_0000_0000_0000b	— *2	— *2	— *2	— *2	Enable Modem Status Interrupt (EDSSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Enable Received Data Available/ time-out Interrupt (ERBI)
08h	URTm_IIR (Read Only) Interrupt Ident. Register	0000_0000_0000_0000_0000_0000b	FIFOs Enabled	FIFOs Enabled	64 Byte FIFO Enabled	0	Interrupt ID Bit 3	Interrupt ID Bit 2	Interrupt ID Bit 1	0 when interrupt pending
0Ch	URTm_FCR (R/W) FIFO Control Register	0000_0000_0000_0000_0000_0000b	Receiver Trigger (MSB)	Receiver Trigger (LSB)	64 Byte FIFO Enable	— *2	DMA Mode Select	Transmitter FIFO Reset	Receiver FIFO Reset	FIFO Enable
10h	URTm_LCR (R/W) Line Control Register	0000_0000_0000_0000_0000_0000b	Divisor Latch Access Bit (DLAB)	Break Control	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
14h	URTm_MCR (R/W) Modem Control Register	0000_0000_0000_0000_0000_0000b	— *2	— *2	Flow Control Enable (AFE)	Loop	OUT2	OUT1	Request to Send (RTS)	Data Terminal Ready (DTR)
18h	URTm_LSR (Read Only) Line Status Register	0000_0000_0000_0000_0000_0000b	Error in Receiver FIFO	Transmitter Empty (TEMT)	Transmitter Holding Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Data Ready (DR)
1Ch	URTm_MSR (Read Only) Modem Status Register	0000_0000_0000_0000_0000_0000b	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (ΔDCD)	Trailing Edge Ring Indicator (TERI)	Delta Data Set Ready (ΔDSR)	Delta Clear to Send (ΔCTS)
20h	URTm_SCR (R/W) Scratch Register	0000_0000_0000_0000_0000_0000b	Scratch Register							
		b31 to b8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
24h LCR[7] = 1b	URTm_DLL (R/W) Divisor Latch (LSB)	0000_0000_0000_0000_0000_0000b	Divisor							
		b31 to b8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
28h LCR[7]= 1b	URTm_DLM (R/W) Divisor Latch (MSB)	0000_0000_0000_0000_0000_0000b	Divisor							
		b31 to b8	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
2Ch	URTm_HCR0 (R/W) HW Control Register 0	b31 to b8	b7	b6	b5	b4	b3	b2	b1	b0
		0000_0000_0000_0000_0000_0000b	SW Reset	RTS Mode	DMA 2Byte Access Enable	Receiver time-out DMA Disable	Receiver DMA Mode	Transmitter DMA Mode	Receiver DMA Enable	Transmitter DMA Enable
30h	URTm_HCR2 (Read Only) HW Status Register 2	0000_0000_0000_0000_0000_0000b	Receiver FIFO Underrun	Receiver FIFO Data Count						
		b31 to b8	b7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
34h	URTm_HCR3 (Read Only) HW Status Register 3	0000_0000_0000_0000_0000_0000b	Transmitter FIFO Overrun	Transmitter FIFO Data Count						
		b31 to b8	b7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
38h	Reserved	0000_0000_0000_0000_0000_0000b	0b	0b	0b	0b	0b	0b	0b	0b
3Ch	Reserved	0000_0000_0000_0000_0000_0000b	0b	0b	0b	0b	0b	0b	0b	0b

Table 40.3-2 List of Registers (Detail) (2/2)

Offset Address	Register Name	Description								
40h	RFU	b31 to b8	b7	b6	b5	b4	b3	b2	b1	b0
		— *3	— *3	— *3	— *3	— *3	— *3	— *3	— *3	— *3
44h	RFU	— *3	— *3	— *3	— *3	— *3	— *3	— *3	— *3	— *3
48h	RFU	— *3	— *3	— *3	— *3	— *3	— *3	— *3	— *3	— *3
4Ch	RFU	— *3	— *3	— *3	— *3	— *3	— *3	— *3	— *3	— *3
50h	RFU	— *3	— *3	— *3	— *3	— *3	— *3	— *3	— *3	— *3
54h to 7Ch	Reserved	0000_0000_0000_0000_0000_0000b	0b	0b	0b	0b	0b	0b	0b	0b

Note: m = 0, 1

Note 1. Unused bits. Writing to these bits has no effect.

Note 2. Unused bits. However, these bits are readable and writable.

Note 3. Access to these bits is prohibited.

Note 4. Unused bits. These bits are always read as 0b.

Note 5. Unused reserved area. Writing to this area has no effect. It is always read as 0b.

40.3.2 Register Descriptions

The function description of each register is given below.

The prefix (URTm_) of the register names is omitted in the register descriptions and the field descriptions in this section.

40.3.2.1 Receiver Buffer Register (when reading received data) (URTm_RBR) / Transmitter Holding Register (when writing transmission data) (URTm_THR) (m = 0, 1)

This register is a received data reading/transmitting data writing register. In FIFO mode (FCR[0] = 1b), an access target is FIFO.

Access Size: 32 bits

Address(es): <URT0_S0_base> + 0000h
<URT1_S0_base> + 0000h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DATA[7:0]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 40.3-3 URTm_RBR / URTm_THR Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	DATA[7:0]	• Non-FIFO mode (FCR[0]=0b) Reading address 00h will read the data from the RBR, and writing will store the data to THR. The first bit received or transmitted is the data bit[0] of LSB. Both RBR and THR are the 1-byte registers on implementation. • FIFO mode (FCR[0]=1b) Reading address 0 will read the data from the receive FIFO, and writing will store the data to the transmit FIFO. Selecting the size of FIFO with FCR[5]. If FCR[5]=0b, the FIFO size is 16 bytes (16550 mode), and if FCR[5]=1b, the FIFO size is 64 bytes. *Note*: When writing to the transmit FIFO full of data, an overrun is detected and the transmit FIFO will not be written. When an overrun is detected, status register HCR3[7] is set to high. When reading from receive FIFO empty of data, and underrun is detected and the FIFO will not be read (all read as 0b). When an underrun is detected, status register HCR2[7] is set to high. When the received or transmitting data is less than 8 bits (5, 6, or 7 bits), lower bits are received or transmitted and upper bits exceeding the set transfer bit count are discarded. (Ex) When the amount of transfer data is set as 5 bits (LCR[1:0]=00b), on the transmit side, the data bits 0 to 4 are transmitted and data bits 7 to 5 are discarded. On the receive side, the valid data to bits 4 to 0 and 0 to the data bits 7 to 5 are written.

40.3.2.2 Interrupt Enable Register (URTm_IER) (m = 0, 1)

This register enables an interrupt. Set each interrupt factor individually. Setting 1b enables the corresponding interrupt. (See URTm_IIR about the detail of the interrupt factors, the releasing interrupt conditions, the priority of the interrupt factors.)

Access Size: 32 bits

Address(es): <URT0_S0_base> + 0004h
<URT1_ S0_base> + 0004h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	EDSSI	ELSI	ETBEI	ERBI
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 40.3-4 URTm_IER Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 4	—	Reserved. These bits are read as 0b. The write value should be always 0b.
3	EDSSI	Enable Modem Status Interrupt.
2	ELSI	Enable Receiver Line Status Interrupt.
1	ETBEI	Enable Transmitter Holding Register (THR) Empty Interrupt.
0	ERBI	Enable Received Data Available/ time-out Interrupt.

Note: Receive complete and timeout may be excluded from the interrupt factor with IER[0]=0b. When HCR0[4]=1b (time-out DMA REQ disable), regardless of the setting of IER[0], a timeout is added to the interrupt factor.

Note: Timeout detecting condition: When there is at least one character in the FIFO, with the following condition 1 or 2 met, a timeout is detected.

- The received latest 4 serial characters are before character-time consecutively.
- The 4 latest FIFO readings are before character-time consecutively.

4 consecutive character-time = 768 cycles of BAUDOUT_N
4 characters of 12-bit received character (1-bit start, 8-bit data, 1-bit parity, 2-bit stop) (12 × 4 × 16 = 768 cycles of BAYDIYT_N)

40.3.2.3 Interrupt Identification Register (URTm_IIR) (m = 0, 1)

This register is a read-only interrupt identification register. This register identifies the operation mode (bits 7 to 5) and the interrupt factor (bits 3 to 0).

When multiple interrupt factors occur, this register outputs the priority processed result.

Access Size: 32 bits

Address(es): <URT0_ S0_base> + 0008h
<URT1_ S0_base> + 0008h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	FIFOs Enabled		64 Byte FIFO Enabled	—	Interrupt ID			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 40.3-5 URTm_IIR Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 6	FIFOs Enabled	FIFOs Enabled
5	64 Byte FIFO Enabled	64 Byte FIFO Enabled Table 40.3-5a FIFO Operation Mode (IIR[7:5]) IIR[7:5] / FIFO Operation Mode 000b / Non-FIFO mode (16450 mode) 110b / 16-Byte FIFO mode (16550 mode) 111b / 64-Byte FIFO mode Note: It will not be in a state other than the above.
4	—	Reserved. This bit is read as 0b. Writing is invalid.
3 to 0	Interrupt ID	Interrupt ID

Table 40.3-6 Interrupt Factor/Interrupt Priority Process (IIR[3:0])

IIR[3:0]	Priority	Interrupt Type	Interrupt Factor	Interrupt Clearing Condition
0001b	None	None	None*1	None
0110b	1	Receiver Line Status (Receive Error)	One or more of the following will occur.*2 • Overrun • Parity error • Framing error • Break Interrupt	Reading Line Status Register (LSR)
0100b	2	Received Data Available (Receive completed)	• Non-FIFO mode Date receive completed in Receive buffer register. • FIFO mode The amount of data in receive FIFO is more than trigger level.	• Non-FIFO mode Reading receive buffer register (RBR) • FIFO mode Reading receive FIFO, the amount of data in receive FIFO is less than trigger level.
1100b		Character Timeout Indication (Timeout)	FIFO mode Timeout of received data occur.	Reading receive FIFO.
0010b*4	3	Transmitter Holding Register Empty (transmit buffer empty)	Transmitter Holding Register (THR) or transmit FIFO is empty.	Reading IIR or writing data to THR / transmit FIFO.
0000b	4	Modem Status	One or more of the following will occur.* 3 • ΔCTS • ΔDSR • ΔDCD • Trailing Edge RI	Reading MSR

Note 1. If the DMA reads the FIFO when a reception complete or timeout interrupt occurs, that interrupt factor (reception complete or timeout) information is overwritten and the interrupt factor becomes “None”. (When the status is confirmed by the system F/W, it may look like “None”. Ignore a “None” interrupt in that situation, and control that situation.)

Note 2. See Line Status Register (LSR) about the detection conditions of Overrun/Framing Error/Break Interrupt.

Note 3. See Modem Status Register (MSR) about the detection conditions of ΔCTS/ΔDSR/ΔDCD/Trailing Edge RI. It will not be in a state other than the above.

Note 4. The interrupt of transmit buffer empty (IIR[3:0] = 0010b) is cleared by either
• Reading IIR
• Writing data to THR
Specifically, the operation of 1 as follows.
If the transmit buffer is empty when IIR is read to check the interrupt cause, it is masked by the read operation and this interrupt will not occur. This mask is cleared when data is written to the transmit buffer, and subsequent transmit buffer empty interrupts are output.

40.3.2.4 FIFO Control Register (URTm_FCR) (m = 0, 1)

This register controls FIFO.

Access Size: 32 bits

Address(es): <URT0_ S0_base> + 000Ch
<URT1_ S0_base> + 000Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Receiver Trigger[1:0]		64 Byte FIFO Enabled	—	DMA Mode Select	Transmitter FIFO Reset	Receiver FIFO Reset	FIFO Enable
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 40.3-7 URTm_FCR Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7, 6	Receiver Trigger[1:0]	Receiver Trigger Valid only in FIFIO mode. (FCR[0]=1b) Set the trigger level of the interrupt and the receive DMA request. The setting value and the corresponding trigger level are as listed in **Table 40.3-7a**.
5	64 Byte FIFO Enable	64 Byte FIFO Enable Valid only in FIFIO mode. (FCR[0]=1b) Set the FIFO capacity. The setting 1b is 64 bytes. The setting 0b is 16 bytes (16550 mode).
4	—	Reserved. This bit is read as 0b. The write value should be always 0b.
3	DMA Mode Select	DMA Mode Select This bit set DMA mode in FIFO mode. See **Table 40.3-7b**. The DMA mode and DMA request generation conditions are shown in **Table 40.3-8**.

Table 40.3-7a Receive Trigger Level Setting

FCR[7:6]	16-Byte Mode (FCR[5]=0) Trigger Level	64-Byte Mode (FCR[5]=1) Trigger Level
00b	1 byte	1 byte
01b	4 bytes	16 bytes
10b	8 bytes	32 bytes
11b	14 bytes	56 bytes

Table 40.3-7b DMA Mode Setting (FCR[3], HCR0[3:2])

FCR[3]	HCR0[3:2]	Receive DMA Request	Transmit DMA Request
0b	00b	Mode 0	
1b	00b	Mode 1	
0b	01b	Mode 0	Mode 1
	10b	Mode 1	Mode 0
Others: Prohibited		—	—

Table 40.3-7 URTm_FCR Register Contents (2/2)

Bit Position	Bit Name	Description
2	Transmitter FIFO Reset	Transmitter FIFO Reset When set to “1b”, the synchronized reset pulse (1 cycle of PCK) is generated, and then reset the whole byte of the transmit FIFO, and the FIFO address counter. This bit is automatically reset to “0”. *Note*: The transmit shift-register TSR is not reset. Therefore, if it is reset during transmission, transmission of data in the shift register is completed and one more “0” frame may be transmitted.
1	Receiver FIFO Reset	Receiver FIFO Reset When set to “1b”, the synchronized reset pulse (1 cycle of PCK) is generated, and then reset the whole byte of the receive FIFO, and the FIFO address counter. This bit is automatically reset to “0”. *Note*: The receive shift-register RSR is not reset. Therefore, if it is reset during reception, the data being received is stored in the receive FIFO normally.
0	FIFO Enable	FIFO Enable Set to “1b”, both transmission and reception are in FIFO mode. Set to “0b”, both transmission and reception are in non-FIFO mode.

Table 40.3-8 DMA Mode and DMA Request Generation Condition

Mode		DMA Request Generation Condition	DMA Request Releasing Condition
DMA access data width 1 byte (HCR[5]=0)			
Receive DMA request	Mode 0	There is more than 1 byte of data in the receive FIFO	The receive FIFO is empty.
	Mode 1	The receive FIFO trigger level reached or time-out occurs.*1	The receive FIFO is empty.
Transmit DMA request	Mode 0	The transmit FIFO is empty.	There is more than 1 byte of data in the transmit FIFO.
	Mode 1	The transmit FIFO is empty.	The transmit FIFO is full.

Note 1. Timeout may be excluded from the receive DMA condition with setting HCR0[4].

Note 2. Performs operation equivalent to mode 0 in non-FIFO mode regardless setting FCR[3], HCR0[3:2].
- Receive DMA request: When 1-byte data receiving in the receive buffer register is completed, the DMA request occurs.
- Clear the request, when the register is empty.
  Transmit DMA request: When the transmit buffer is empty, the DMA request occurs. Clear the request, when there is 1-byte data.

40.3.2.5 Line Control Register (URTm_LCR) (m = 0, 1)

This register controls the FIFO.

Access Size: 32 bits

Address(es): <URT0_ S0_base> + 0010h
<URT1_ S0_base> + 0010h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DLAB	Break Control	Stick Parity	EPS	PEN	STB	WLS	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 40.3-9 URTm_LCR Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7	DLAB	Divisor Latch Access Bit When 1b is set, the divider latch (DLM / DLL) may be set. Setting the divisor latch, and then this bit is set to 0b, accessing divisor latch is forbitten and generation of 16x clock corresponding to the setting value of the baud-rate-generator is started. *Note*: After the master reset, the 16x clock is stopped. The baud-rate-generator starts generating the 16x clock by detecting this bit changing from high to low. (Once generated, the 16x clock will not stop unless a master reset is entered again.)
6	Break Control	Break Control Control occurrence and transmit of break condition. While this bit is set to 1b, serial out (SOUT) is forced to 0b. If this bit is set to 0b again, release forcing. This bit only controls the output level of SOUT, so the internal circuit is not affected. *Note*: If set to “1b” during transmission, only framing error may be detected in receive side. To make sure that a break is detected, it is necessary to set it in the transmission complete (transmission buffer empty) state.
5	Stick Parity	Stick Parity When LCR[3]=1b, setting this bit to 1b performs stick parity transmission/reception checks. The stick value (high/low) is set with LCR[4].
4	EPS	Even Parity Select When LCR[3]=1b, LCR[5]=0b, it is able to set even/odd parity.
3	PEN	Parity Enable If this bit is 1b, a parity bit is added in transmit side, and parity is checked in receive side. See **Table 40.3-10**.
2	STB	Number of Stop Bit Set the number of stop bits in the serial transmit data. 0b: The number of stop bits is 1. 1b: The number of stop bits is 2. Regardless this bit, the first stop bit is checked in receive side.

Table 40.3-9 URTm_LCR Register Contents (2/2)

Bit Position	Bit Name	Description
1 to 0	WLS	Word Length Select Set the word length of the serial transmit/receive data. 00b: 5-bit word length 01b: 6-bit word length 10b: 7-bit word length 11b: 8-bit word length

Table 40.3-10 Parity Type Setting

LCR[5:3]	Parity Type
xx0b	No parity bit
001b	Odd parity
011b	Even parity
101b	Sticky high (fixed to “1b”)
111b	Sticky low (fixed to “0b”)

Remarks: x: Don’t care

40.3.2.6 Modem Control Register (URTm_MCR) (m = 0, 1)

This register controls the interface of modem (peripheral devices).

Access Size: 32 bits

Address(es): <URT0_ S0_base> + 0014h
<URT1_ S0_base> + 0014h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	AFE	Loop	OUT2	OUT1	RTS	DTR
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 40.3-11 URTm_MCR Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b. Writing is invalid.
7, 6	—	Reserved. These bits are read as 0b. The write value should be always 0b.
5	AFE	Flow Control Enable Set auto flow control (auto-CTS, auto-RTS). Auto flow can be set in combination with MCR[1] (RTS) and HCR[6]. See **Table 40.3-12**.
4	Loop	When 1b is set, local loopback operation for UART test is performed. When UART is operated in loopback, the following occurs: — SOUT is asserted high. — SIN is disconnected. — The output of the TSR is looped back into the RSR input. — The modem control input (CTS_N) is disconnected. — The four modem control output (RTS_N) is internally connected to CTS_N. — RTS_N is asserted high.
3	OUT2	Reserved. This bit is read as 0b. The write value should be always 0b.
2	OUT1	Reserved. This bit is read as 0b. The write value should be always 0b.
1	RTS	Request To Send When auto-RTS (MCR[5]=0b) is not used, control the output terminal RTS_N (send request). The inversion level of this MCR[1] setting value is output to RTS_N. In loopback, it functions as a control bit for the input terminal CTS_N.
0	DTR	Data Terminal Ready. Control the output terminal DTR_N (ready to establish communication link). The Inversion level of this MCR[0] setting value is output to DTR_N. In loopback, it functions as a control bit for the input terminal DSR_N.

Table 40.3-12 Auto Flow Setting (MCR[5], [1], HCR0[6])

MCR[5] (AFE)	MCR[1] (RTS)	HCR0[6] (RTS Mode)	Auto-CTS	Auto-RTS
1b	1b	0b	●	● (auto-RTS mode 0)
		1b	●	● (auto-RTS mode 1)
	0b	x	●	— (RTS_N is fixed to high)
0	x	x	—	—

Note: x: Don't care ●: Enable —: Disable

Auto-CTS operation:

While input terminal CTS_N is at the low level (transmit request), the data in the transmit buffer (THR/transmit FIFO) is transmitted. When CTS_N becomes high, transmission is stopped. During transmission, if CTS_N changes from high to low, the data in transmission (rest data in shift-register) will be sent, and the next data is stopped from being transmitted.

Auto-RTS operation (Valid only in FIFO mode):

- Auto-RTS mode 0

  When the amount of the data in the receive FIFO reaches the trigger level, the output terminal RTS_N is set to the high level (transmission stop request). After the receive FIFO data is read and becomes empty, it is set to the low level (transmission request).

- Auto-RTS mode 1
  - 16-byte FIFO: When the amount of data in the receive FIFO is more than 14 bytes, RTS_N is set to the high level. and when less than 13 bytes, it is set to the low level.
  - 64-byte FIFO: When the amount of data in the receive FIFO is more than 56 bytes, RTS_N is set to the high level, and when less than 55 bytes, it is set to the low level.

NOTE

- When auto flow operation is not used, hardware flow control is not performed. Therefore, monitoring CTS and RTS by software is required to prevent FIFO overrun.
- When auto flow is not used (MCR[5] = 0b), MCR[1] is an RTS_N output software control bit (the inverted level of the MCR[1] setting value is output to RTS_N).
- If both the modem status interrupt (IER[3] = 1b) and auto-CTS are set, the auto-CTS function is disabled.
- In non-FIFO mode, the auto-RTS function is disabled.

40.3.2.7 Line Status Register (URTm_LSR) (m = 0, 1)

This register checks the transmission/reception status.

Access Size: 32 bits

Address(es): <URT0_ S0_base> + 0018h
<URT1_ S0_base> + 0018h

Initial Value: 0000_0060h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Error in Receiver FIFO	TEMT	THRE	BI	FE	PE	OE	DR
Initial Value	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 40.3-13 URTm_LSR Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7	Error in Receiver FIFO	In non-FIFO mode, this bit is always read as 0b. In FIFO mode, set to 1b if any one of break interrupt, parity error, and framing error exists in the data read from the receive FIFO. Cleared to 0b by LSR read.
6	TEMT	Transmitter Empty Set to 1b if both the transmit buffer (THR or the transmit FIFO) and the transmit shift-register TSR are empty. Cleared to 0b when data exists in either the transmit buffer or transmit shift register TSR.
5	THRE	Transmitter Holding Register Empty Set to 1b if the transmit buffer (THR or the transmit FIFO) is empty. 1 byte of write data will enable the bit to be cleared to 0b.
4	BI	Break Interrupt This bit is set to 1b when a break interrupt is detected. • A break interrupt is detected when a low level is received for one frame (start bit + data bit + stop bit) or more. When the receiver detects the start bit (low level), it interprets that data is being sent and performs the reception operation. Therefore, while receiving a break interrupt (while the low level is being input), it continues to receive all "0" data (reception stops when Overrun occurs). • In FIFO mode, break interrupt information is stored in the FIFO together with all 0b data. A break interrupt is detected when data is read. *Note*: A framing error always occurs when a break interrupt is detected. Depending on the LCR[5:3] setting, a parity error may occur.
3	FE	Framing Error When a framing error is detected in the received data, this bit is set to 1b. Cleared to 0b by LSR read. • A framing error is detected when the first stop bit following the data bit or parity bit of the received data is checked and is abnormal (low level). • In FIFO mode, framing error information is stored in the FIFO simultaneously with the received data. Error detection is performed when data is subsequently read.

Table 40.3-13 URTm_LSR Register Contents (2/2)

Bit Position	Bit Name	Description
2	PE	Parity Error • When a parity error is detected in the received data, this bit is set to 1b. Cleared to 0b by LSR read. In FIFO mode, parity error information is stored in the FIFO simultaneously with the received data. Error detection is performed when data is subsequently read.
1	OE	Overrun Error • This bit is set to 1b when a reception overrun error is detected. Cleared to 0b by LSR read. • Detection of a received overrun is performed when a received start bit data is newly detected, if the received buffer register or the received FIFO is full of received data and data in the received shift register is on hold. • When this error occurs, the new received data is not stored in the receiving buffer register or the receiving FIFO. The data held in receiving shift register is stored, when the received buffer has free space.
0	DR	Data Ready 1b is set if 1 byte is stored in the receiving buffer (RBR or receiving FIFO). When the received data is read and empty, it is cleared to 0b.

40.3.2.8 Modem Status Register (URTm_MSR) (m = 0, 1)

This register is the status register of the control signals connected to Modem (or the peripheral devices).

Access Size: 32 bits

Address(es): <URT0_ S0_base> + 001Ch
<URT1_ S0_base> + 001Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DCD	RI	DSR	CTS	ΔDCD	TERI	ΔDSR	ΔCTS
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 40.3-14 URTm_MSR Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7	DCD	Reserved. This bit is read as 0b.
6	RI	Reserved. This bit is read as 0b.
5	DSR	Reserved. This bit is read as 0b.
4	CTS	Clear To Send Indicate the invert level of input terminal CTS_N. In loopback, read the setting value of MCR[1] (RTS).
3	ΔDCD	Reserved. This bit is read as 0b.
2	TERI	Reserved. This bit is read as 0b.
1	ΔDSR	Reserved. This bit is read as 0b.
0	ΔCTS	Delta Clear To Send Set to 1b when the input terminal CTS_N changes (from high to low or from low to high). Cleared by MSR read

40.3.2.9 Scratch Register (URTm_SCR) (m = 0, 1)

This register may be freely used for programming.

Access Size: 32 bits

Address(es): <URT0_ S0_base> + 0020h
<URT1_ S0_base> + 0020h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SCR							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 40.3-15 URTm_SCR Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	SCR	This 8-bit read/write register has no effect on unit control. This register may be freely used for programming.

40.3.2.10 Divisor Latch LS Byte Register (URTm_DLL) (m = 0, 1)

This register is the lower 8 bits (bits 7 to 0) of the divisor setting for the baud rate generator.

The baud rate generator uses this divisor setting value to divide the reference clock (SCLK) to generate a 16x baud rate clock for the transceiver. For divisor settings, two 8-bit registers (DLM, DLL) are used.

Access Size: 32 bits

Address(es): <URT0_ S0_base> + 0024h
<URT1_ S0_base> + 0024h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DLL							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 40.3-16 URTm_DLL Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	DLL	The lower 8 bits (bits 7 to 0) of the divisor setting for the baud rate generator.

Note: LCR[7] shall be set to 1b before setting DLL and DLM and after writing DLM, DLL LCR[7] shall be set to 0b. See **Section 40.3.3.5, Line Control Register (URTm_LCR) (m = 0 to 1)** for details.

40.3.2.11 Divisor Latch MS Byte Register (URTm_DLM) (m = 0, 1)

This register is the upper 8 bits (bits 15 to 8) of the divisor setting for the baud rate generator.

The baud rate generator uses this divisor setting value to divide the reference clock (SCLK) to generate a 16x baud rate clock for the transceiver. For divisor settings, two 8-bit registers (DLM, DLL) are used.

Access Size: 32 bits

Address(es): <URT0_ S0_base> + 0028h
<URT1_ S0_base> + 0028h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DLM							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 40.3-17 URTm_DLM Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	DLM	The upper 8 bits (bits 15 to 8) of the divisor setting for the baud rate generator.

Note: LCR[7] shall be set to 1b before setting DLL and DLM and after writing DLM, DLL LCR[7] shall be set to 0b. See **Section 40.3.3.5, Line Control Register (URTm_LCR) (m = 0 to 1)** for details.

The setting value is as follows. Note that the range of the divisor setting is from 1 to $2^{16}-1$. The setting example is indicated in table “Divisor Setting Example”.

$$\text{The setting value of divisor} = \frac{\text{the frequency of the reference clock [Hz]}}{\text{request baud rate [bps]} \times 16}$$

Table 40.3-18 Divisor Setting Example (DLM/DLL)

Request Baud Rate [bps]	Reference Clock (SCLK) 48 MHz		
	Divisor Bits 15 to 0	Real Baud Rate [bps]	Error [%]
300	10000	300	0
600	5000	600	0
1200	2500	1200	0
2400	1250	2400	0
4800	625	4800	0
9600	312	9600	0
19200	156	19200	0
38400	78	38400	0
57600	52	57600	0
115200	26	115200	0
230400	13	230400	0

Note: The value of divisor is decimal notation.

40.3.2.12 HW Control Register 0 (URTm_HCR0) (m = 0, 1)

This register controls DMA and others. This is the additional register for unit control.

Access Size: 32 bits

Address(es): <URT0_ S0_base> + 002Ch
<URT1_ S0_base> + 002Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SW Reset	RTS Mode	DMA 2Byte Access Enable	Receiver time-out DMA Disable	Receiver DMA Mode	Transmitter DMA Mode	Receiver DMA Enable	Transmitter DMA Enable
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 40.3-19 URTm_HCR0 Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7	SW Reset	When set to 1b, the unit internal registers except the transmit/receive FIFO, DLL, DLM, and baud rate generator are reset. It is canceled when 0b is set. *Note*: The transmit/receive FIFO should be reset before using the SW reset (FCR[2:1]). And all registers except DLL and DLM should be set after SW reset.
6	RTS Mode	RTS mode setting register when auto-RTS is used. 0b: Auto-RTS mode 0 1b: Auto-RTL mode 1 See **Table 40.3-12** for details.
5	DMA 2Byte Access Enable	Setting register for the DMA access data width of the transmit/receive FIFO. This UART is 1-byte access only, so 0 should be set.
4	Receiver time-out DMA REQ Disable	0b: Timeout is included in the receive DMA request factor. 1b: Timeout is excluded from the receive DMA request factor (added to the interrupt factor automatically). See **Table 40.3-8** for details
3	Receiver DMA Mode	Bits 3 and 2 are the control bits to set DMA request mode for transmission and reception individually, which is used together with FCR [3]. See **Table 40.3-8b** for details.
2	Transmitter DMA Mode	
1	Receiver DMA Enable	0b: Disable receive DMA request output. The low level is output to the terminal DMA_RX_REQ.l 1b: Enable receive DMA request output.
0	Transmitter DMA Enable	0b: Disable transmit DMA request output. The low level is output to the terminal DMA_TX_REQ. 1b: Enable transmit DMA request output.

40.3.2.13 HW Status Register 2 (URTm_HCR2) (m = 0, 1)

This register is the additional register to check the status of the receive FIFO.

Access Size: 32 bits

Address(es): <URT0_ S0_base> + 0030h
<URT1_ S0_base> + 0030h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Receiver FIFO Underrun	Receiver FIFO Data Count						
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 40.3-20 URTm_HCR2 Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7	Receiver FIFO Underrun	If a read is performed when the receive FIFO is empty, an underrun is detected, and the high level is set. Cleared by HCR2 read. *Note*: When an underrun is detected, all 0b are read. There is no interrupt request due to an underrun.
6 to 0	Receiver FIFO Data Count	The amount of data in the receive FIFO is output.

40.3.2.14 HW Status Register 3 (URTm_HCR3) (m = 0, 1)

This register is the additional register to check the status of the transmit FIFO.

Access Size: 32 bits

Address(es): <URT0_ S0_base> + 0034h
<URT1_ S0_base> + 0034h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Transmitter FIFO Overrun	Transmitter FIFO Data Count						
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 40.3-21 URTm_HCR3 Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7	Transmitter FIFO Overrun	If a write is performed when the transmit FIFO is full, an overrun is detected, and the high level is set. Cleared by HCR3 read. *Note*: When an overrun is detected, no data is written to the transmit FIFO. There is no interrupt request due to an overrun.
6 to 0	Transmitter FIFO Data Count	The amount of data in the receive FIFO is output.

40.4 Operation

The prefix (URTm_) of the register names is omitted in this and subsequent sections.

40.4.1 Clock Timing

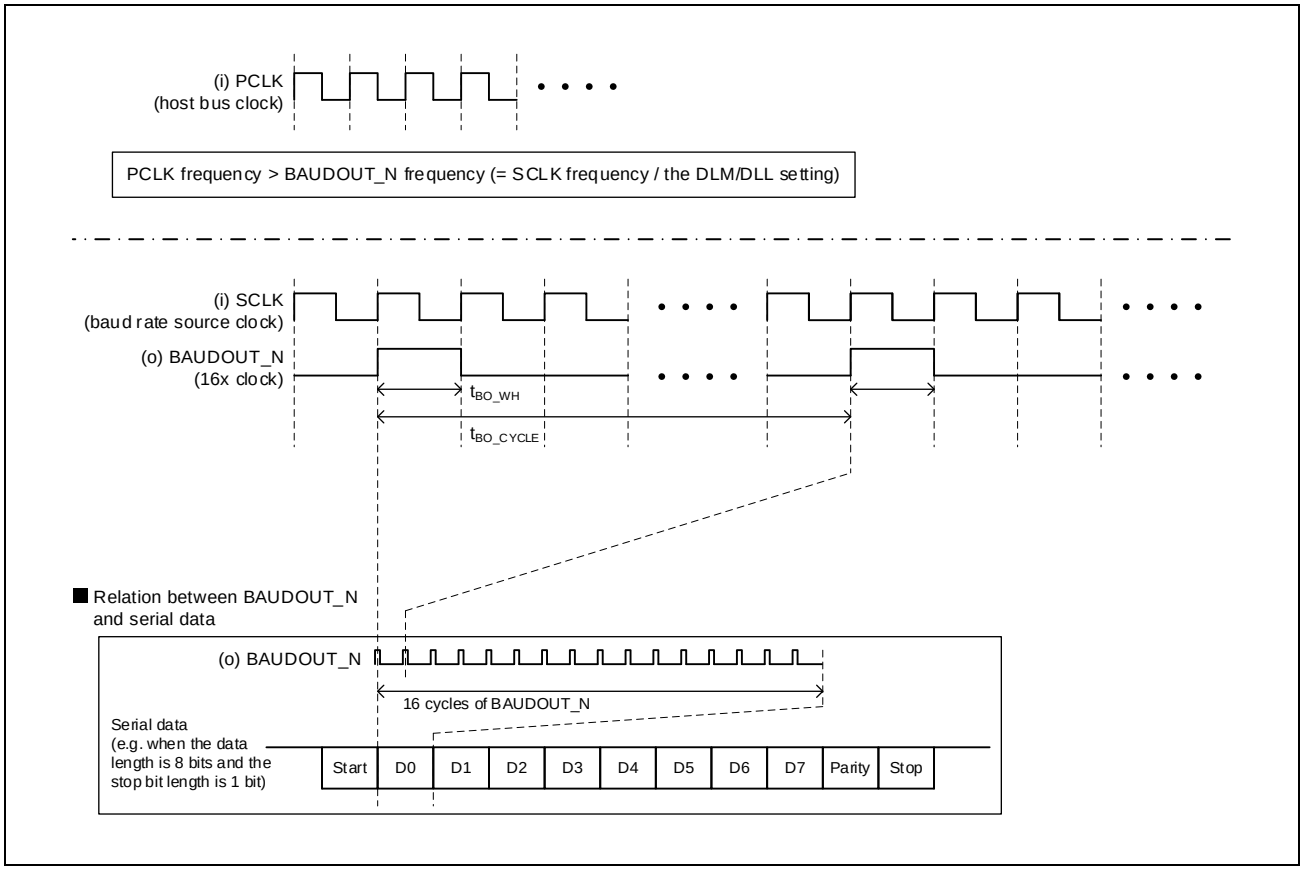


Figure 40.4-1 Clock Timing

Table 40.4-1 Clock Timing

Symbol	Parameter	Figure	Min.	Typ.	Max.	Unit	Remarks
■ PCLK, SCLK, BAUDOUT_N							
—	PCLK frequency	**Figure 40.4-1**	PCLK frequency > BAUDOUT_N (16x clock) frequency			Hz	BAUDOUT_N frequency = SCLK frequency/DLM, DLL setting
t_{BO_WH}	BAUDOUT_N output width at high level		1			SCLK cycle	
t_{BO_CYCLE}	BAUDOUT_N1 cycle time		1	—	$2^{16} - 1$		

Note: The specifications listed in this table are all theoretical values by design.

40.4.2 UART Serial Protocol

The UART serial protocol is briefly described. Serial communications between this UART and an other-party UART device proceed asynchronously. The format of UART serial data is as shown below. Additional bits such as start and stop bits are appended to the first and last of serial data. **Figure 40.4-2** shows the structure of serial data with start and stop bits.

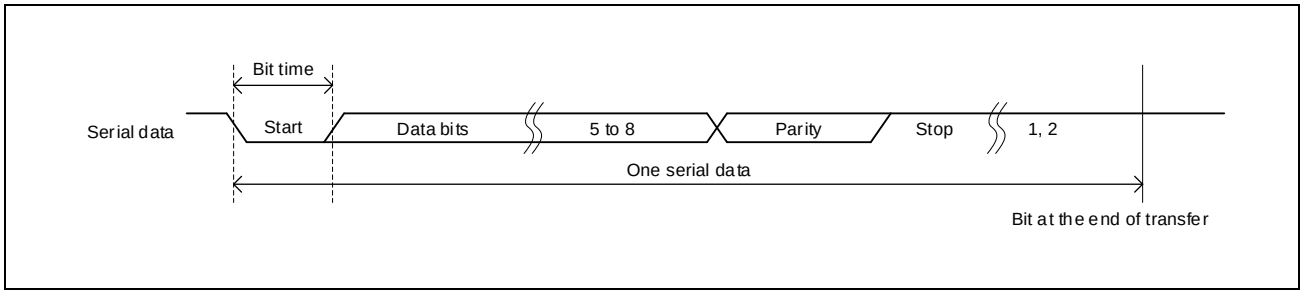


Figure 40.4-2 Structure of Serial Data

A parity bit may be appended to serial data. This bit is effective for simple error checking of received data in communications by the UART. It is appended before the stop bit of transferred data and after the last of the data. UART communications can be controlled by the line control register (LCR register). Data are transmitted from the LSB after the start bit. Optional parity bits and one or two stop bits can be used (this UART does not support half-stop when 1.5 stop bits are used). All bits are transmitted with the same timing.

The communications time for 1-bit data is a clock signal at 16x the baud rate. Once a start bit is detected, received data are sampled almost in the middle of the communications time for each bit of data so that stability is secured for the received data. After the time of sampling in the middle of the start bit, bits are sampled every 16 cycles of the baud rate clock. **Figure 40.4-3** shows the timing of sampling of the first two bits of serial data.

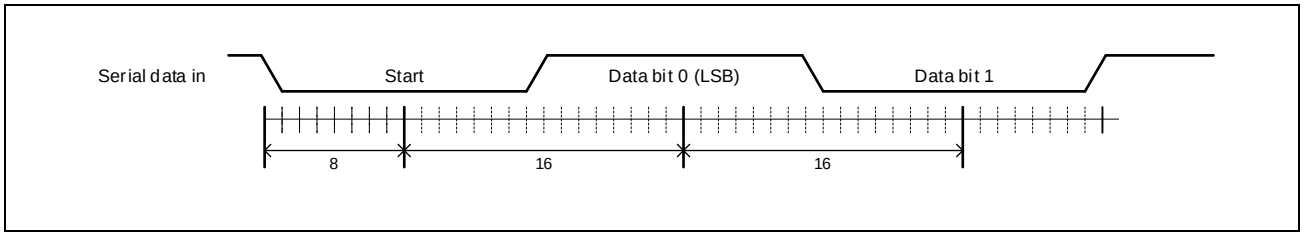


Figure 40.4-3 Serial Data Sampling Timing

The baud rate is controlled by the serial clock and the divisor latch registers (DLH and DLL). The relation between the setting of the devisor latch register and the baud-rate clock is described in **Section 40.3.3.10, Divisor Latch LS Byte Register (URTm_DLL) (m = 0 to 1)** and **Section 40.3.3.11, Divisor Latch MS Byte Register (URTm_DLM) (m = 0 to 1)**.

40.4.3 Interrupt

When an interrupt occurs, NTR is asserted. There are interrupt sources as listed below and each interrupt can be enabled by the IER register (bits 3 to 0).

- Reception error
- When data is received
- Character timeout (for use in FIFO mode)
- The transmission data hold register being empty
- Modem status

The interrupt source can be analyzed by referring to the IIR register. Proceed with the appropriate processing according to the given interrupt source.

Table 40.4-2 Interrupt Setting and Clearing Conditions

IIR Register (Bits 3 to 0)				Interrupt Setting and Clearing Conditions			
3	2	1	0	Priority Order	Interrupt Type	Interrupt Setting Condition	Interrupt Clearing Condition
0b	0b	0b	1b	None	None	None	None
0b	1b	1b	0b	Highest priority	Reception line status	Overrun error, parity error, framing error, or break	Reading of the line status register
0b	1b	0b	0b	2	Received data present	16450 mode: Received data being present.	Reading of the reception buffer register
						FIFO mode: The triggering level being reached.	The FIFO buffer falling below the triggering level by reading the reception buffer register.
1b	1b	0b	0b	2	Character timeout	The interrupt occurs when all the following conditions are satisfied. 1) FIFO being enabled. 2) The reception FIFO triggering level being set to 14, 8, or 4 bytes (other than 1 byte). 3) The reception FIFO triggering level not being reached. 4) No character being taken out from the reception FIFO buffer and no character being input to the reception FIFO buffer within the time for the most recent four characters. 5) At least one character being present in the reception FIFO buffer within the time for the most resent four characters.	Reading of the reception buffer register
0b	0b	1b	0b	3	Transmission hold register empty	The transmission register being empty.	Reading of IIR (when this is a source to generate the interrupt) or writing to the transmission hold register
0b	0b	0b	0b	4	Modem status	Detection of any of the CTS_N, RI_N, DSR_N, and DCD_N signals going to the low level. If automatic flow control is enabled, the interrupt does not occur on detection of the low level of the CTS_N signal.	Reading of the modem status register

40.4.4 DMA Interface

This unit has a reception DMA request signal (DMA_RX_REQ) and a transmission DMA request signal (DMA_TX_REQ) to support the DMA interface.

40.4.4.1 DMA Modes of UART

The conditions for issuing and clearing of the DMA request in this unit are selectable from DMA modes, (1) to (3) for reception and (4) to (6) for transmission, as listed in **Table 40.4-3**. For the flow of DMA transfer in each mode, see **Section 40.5, Operation**.

Operation in non-FIFO mode is equivalent to that in mode 0. The register settings when the FIFO buffer is in use are described in **Section 40.3.3.4, FIFO Control Register (URTm_FCR) (m = 0 to 1)**.

Table 40.4-3 List of DMA Modes of UART

DMA Mode		DMA Request Issuing Condition	DMA Request Clearing Condition	DMA Transfer Flow
Reception	(1) Non-FIFO	Completion of the reception of one byte of data in the reception buffer register	The reception buffer being empty	**Figure 40.5-1**
	(2) Mode 0	The reception FIFO containing one or more bytes of data	The reception FIFO being empty	**Figure 40.5-2**
	(3) Mode 1	The reception FIFO triggering level being reached or occurrence of a timeout		**Figure 40.5-3**
		The FIFO triggering level being reached		**Figure 40.5-4**
Transmission	(4) Non-FIFO	The transmission buffer being empty	The transmission buffer register containing one byte of data	**Figure 40.5-5**
	(5) Mode 0	The transmission FIFO being empty	The transmission FIFO containing one or more bytes of data	**Figure 40.5-6**
	(6) Mode 1		The transmission FIFO being full*1	**Figure 40.5-7**

Note 1. Since the condition for clearing of the DMA request is the transmission FIFO being full, this mode cannot be used except with the per-byte transfer setting.

40.4.4.2 Initialization of the DMAC

This section describes operations for DMA transfer. For the detailed DMAC setup procedures, see the section of DMAC.

- The DMA interface of this unit only has a DMA request signal for transmission and reception, so select level detection mode for the detection of DMA transfer requests and bus cycle output mode for the acknowledge output function.
  - DMA transfer request: Leve detection mode
    → Set the LVL bit in the DMAA_DMACn_CHCFG_m register of the DMAC to 1b.
  - DMA acknowledge output: Bus cycle output mode
    → Set the AM[2:0] bits in the DMAA_DMACn_CHCFG_m register of the DMAC to 010b.

- In bus cycle output mode, the DMA acknowledge signal (DMAACK) is at the active level during the bus cycle periods. If DMAREQ is asserted at the point where a bus cycle is completed, it is handled as a next DMA transfer request.
  In level output mode, the DMA request signal and the DMA acknowledge signal are handled as a handshake interface, they must be de-asserted at the same time once before the next DMA request.

40.4.4.3 Timing Comparison of Mode 0 and Mode 1 in DMA Transfer for Reception by This Unit

Figure 40.4-4 shows an example of timing comparison of (2) Mode 0 and (3) Mode 1 listed in **Table 40.4-3, List of DMA Modes of UART**, in DMA transfer for reception. In this example, a period difference indicated by ★ is generated at the time when transfer of received data is completed.

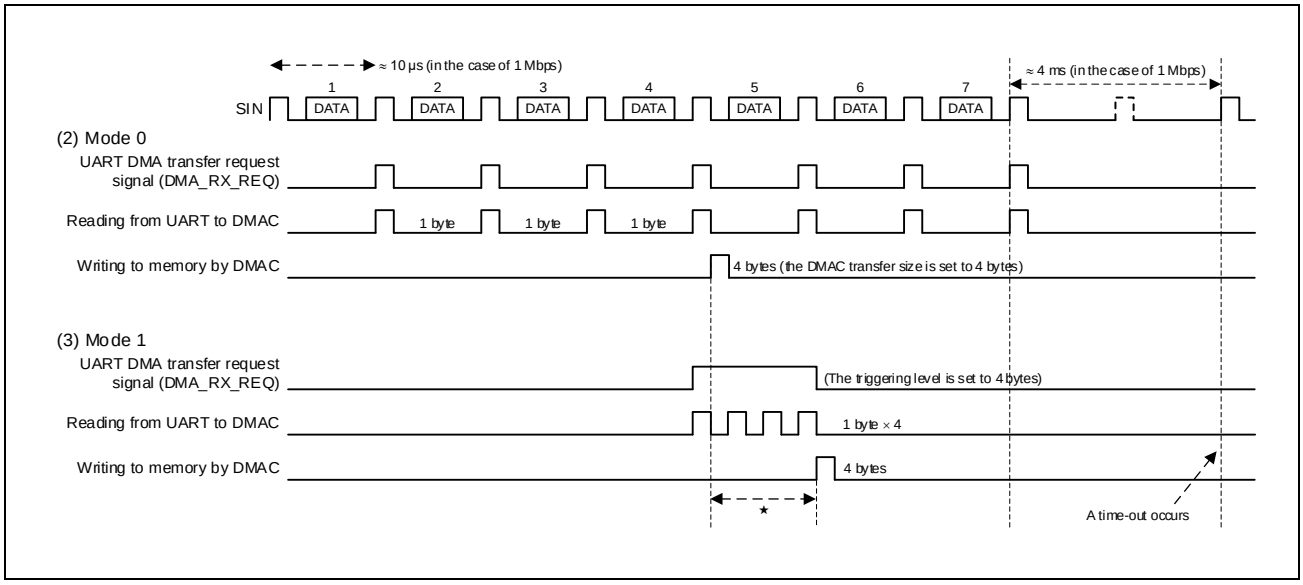


Figure 40.4-4 Example Comparison of Mode 0 and Mode 1 in DMA Transfer for Reception

40.4.4.4 Timing of DMA Transfer for Reception with the Use of the DMAC

Figure 40.4-5 shows an example of the timing of DMA transfer for reception when the DMAC is in use.

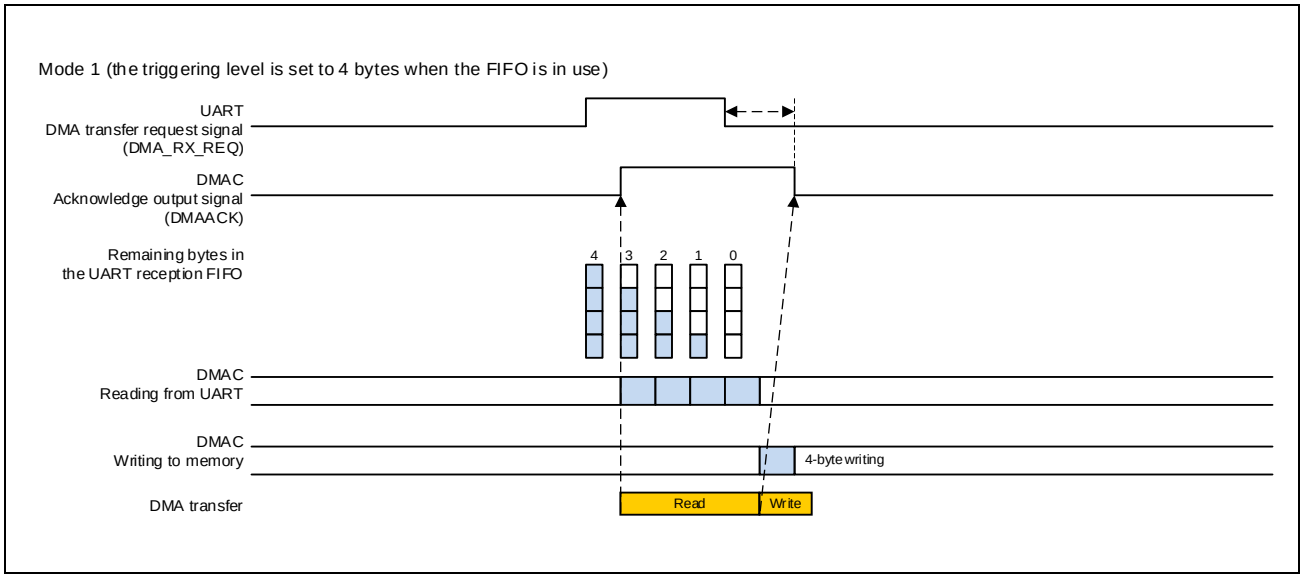


Figure 40.4-5 Example Timing of DMA Transfer for Reception

- The DMAACK signal of the DMAC is at the active level during the period from the time a read request is output to the host bus until one cycle after the last of the read data.
- The DMA transfer request signal (DMA_RX_REQ) of the UART becomes inactive level before de-assertion of the DMAACK signal of the DMAC, so DMA transfer proceeds normally.

40.4.4.5 Timing of DMA Transfer for Transmission with the Use of the DMAC

Figure 40.4-6 shows an example of the timing of DMA transfer for transmission when the DMAC is in use.

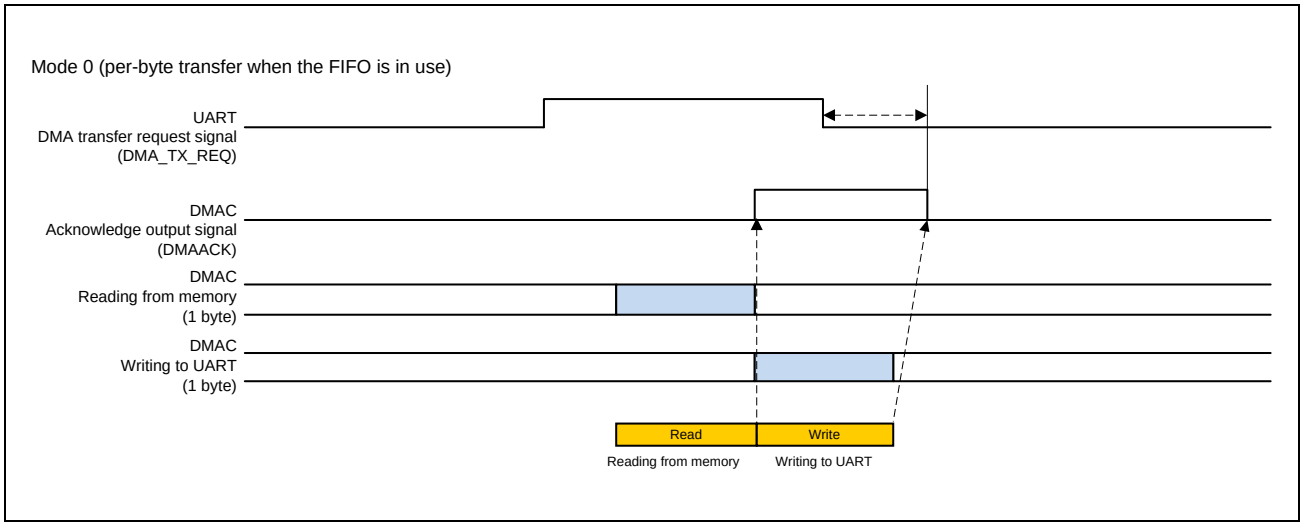


Figure 40.4-6 Example Timing of DMA Transfer for Transmission

- The DMAACK signal of the DMAC is at the active level during the period from the time a write request is output to the host bus until one cycle after a response for the last of the data is returned.
- The DMA transfer request signal (DMA_RX_REQ) of the UART becomes inactive level before de-assertion of the DMAACK signal of the DMAC, so DMA transfer proceeds normally.

CAUTION

- Writing by the DMAC with the bufferable attribute to the FIFO buffer may proceed after DMAACK is at the inactive level. In such cases, de-assertion of DMA_TX_REQ may be delayed and as such the DMAC may mistakenly take DMA_TX_REQ to be a next DMA request and proceed with unnecessary transfer.
- To prevent this, use the non-bufferable attribute for writing by the DMAC.

40.4.4.6 DMA Request Timing for Reception

Figure 40.4-7 shows the DMA request timing for reception by this unit.

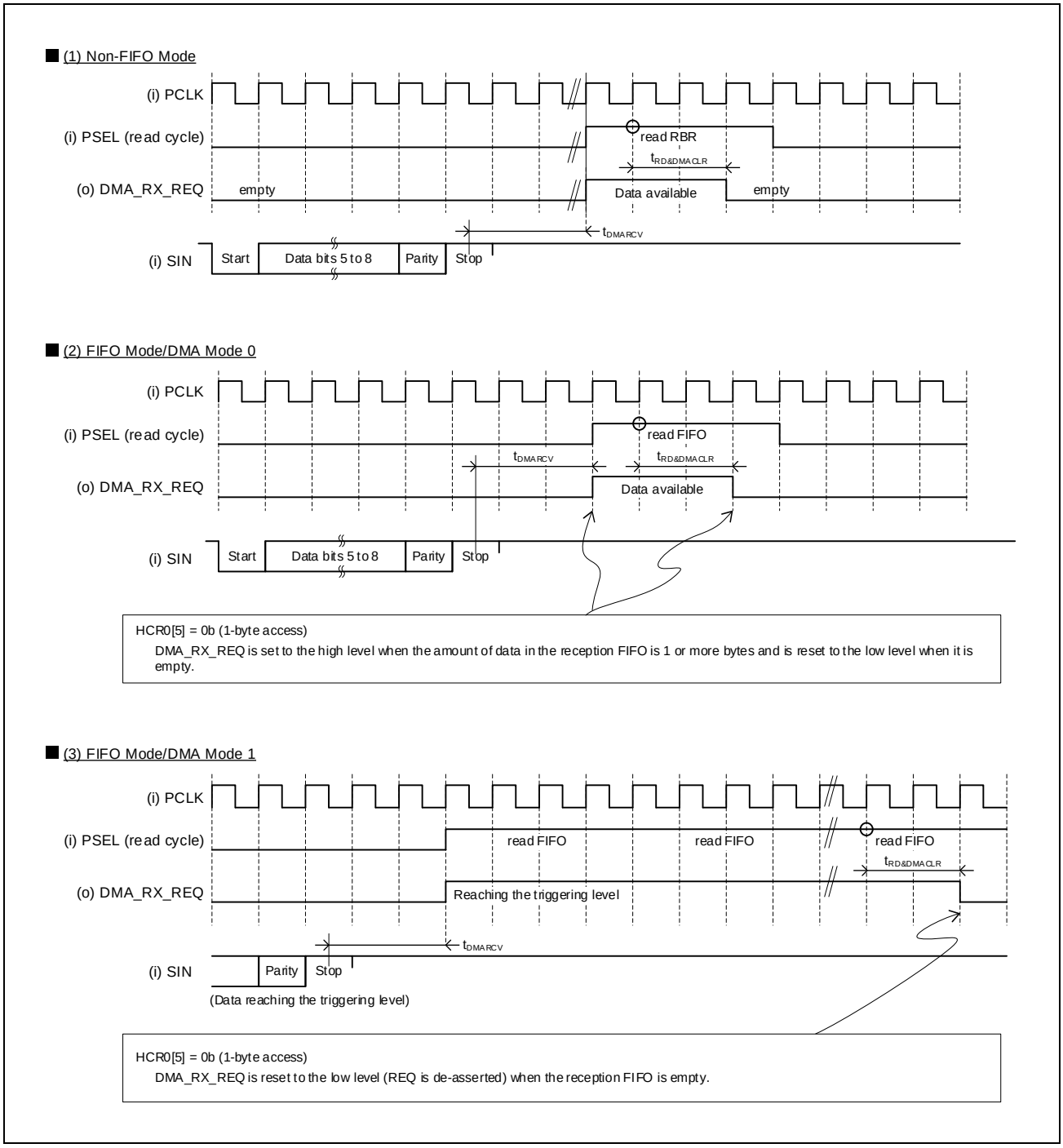


Figure 40.4-7 DMA Request Timing for Reception

Table 40.4-4 DMA Request Timing for Reception

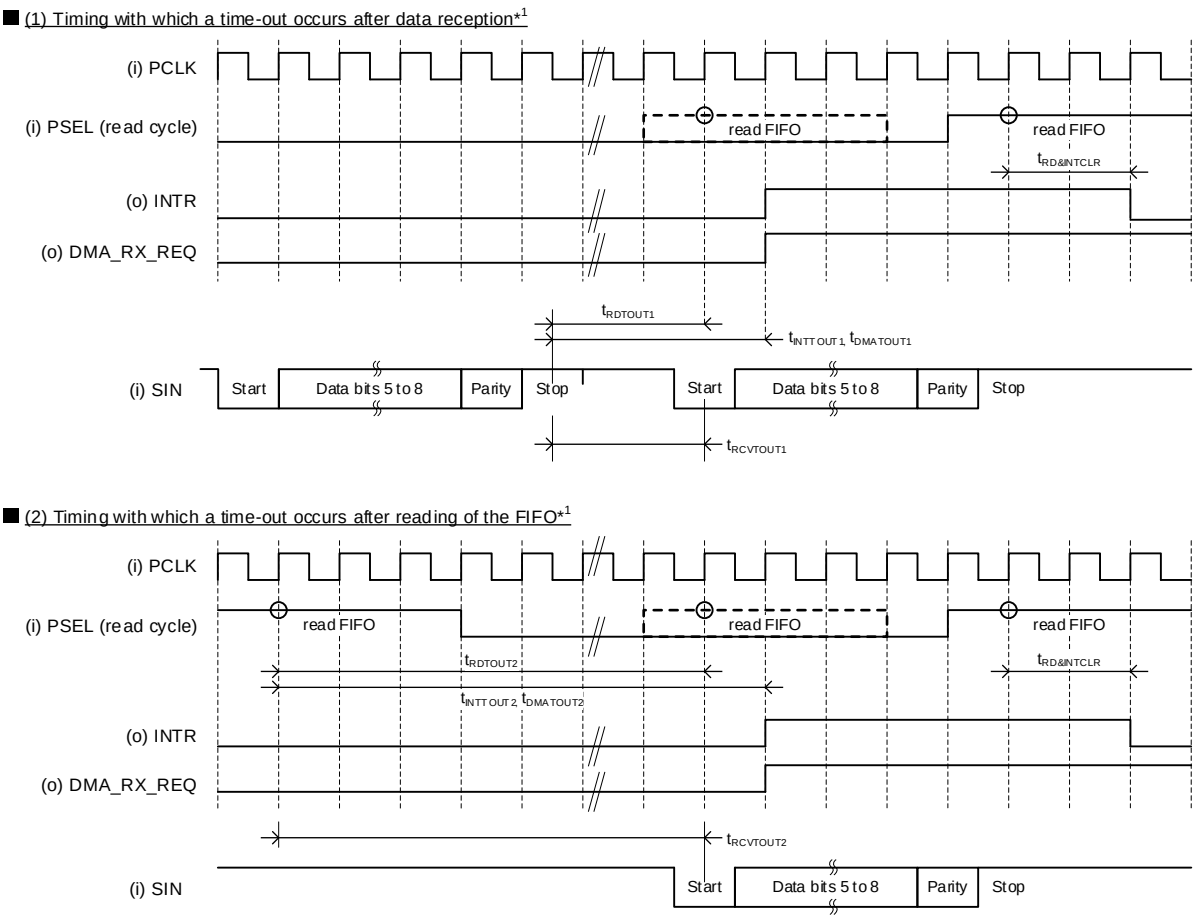
Symbol	Parameter	Figure	Min.	Typ.	Max.	Unit	Remarks
t_{DMARCV}	Data reception completion DMA request delay • Center phase of the stop bit => Rising edge of DMA_RX_REQ	**Figure 40.4-7**	0	—	1	BAUDOUT_N cycle	t_{DMARCV} = BAUDOUT_N cycles + PCLK cycles
			4	—	5	PCLK cycle	
$t_{RD\&DMACLR}$*1	FIFO read DMA request clearing delay • From reading of the reception FIFO to the falling edge of DMA_RX_REQ		2			PCLK cycle	

Note: The specifications listed in this table are all theoretical values by design.

Note 1. These are also defined in the other specification tables.

40.4.4.7 Time-out Timing

Figure 40.4-8 shows the timing of a time-out for this unit.



Note 1. If reading of the FIFO is completed after the received data reach the reception FIFO triggering level setting, a time-out interrupt occurs and remaining data in the reception FIFO are read.

Figure 40.4-8 Time-out Timing

Table 40.4-5 Time-out Timing

Symbol	Parameter	Figure	Min.	Typ.	Max.	Unit	Remarks
$t_{RDTOUT1}$ $t_{RDTOUT2}$ $t_{RCVTOUT1}$ $t_{RCVTOUT2}$	FIFO read time-out detection time • $t_{RDTOUT1}$: From the center phase of the stop bit to reading of the reception FIFO • $t_{RDTOUT2}$: From reading of the reception FIFO to the next reading of the reception FIFO Data reception time-out detection time • $t_{RCVTOUT1}$: From the center phase of the stop bit to the center phase of the start bit • $t_{RCVTOUT2}$: From reading of the reception FIFO to the center phase of the start bit	**Figure 40.4-8**	768 BAUDOUT_N cycles to 771 BAUTDOUT_N cycles + 3 PCLK cycles				
$t_{INTTOUT1}$ $t_{INTTOUT2}$ $t_{DMATOUT1}$ $t_{DMATOUT2}$	Time-out interrupt output delay • $t_{INTTOUT1}$: From the center phase of the stop bit to the rising edge of INTR • $t_{INTTOUT2}$: From reading of the reception FIFO to the rising edge of INTR Time-out DMA request output delay • $t_{DMATOUT1}$: From the center phase of the stop bit to the rising edge of DMA_RX_REQ • $t_{DMATOUT2}$: From reading of the reception FIFO to the rising edge of DMA_RX_REQ		768 BAUDOUT_N cycles + 2 PCLK cycles to 771 BAUTDOUT_N cycles + 4 PCLK cycles				
$t_{RD\&INTCLR}$*1	Register or received data read interrupt de-assertion delay • From reading of the reception FIFO to the falling edge of INTR		2		PCLK cycle		

Note: The specifications listed in this table are all theoretical values based on RTL.

Note 1. These are also defined in the other specification tables.

40.4.4.8 DMA Request Timing for Transmission

Figure 40.4-9 shows the DMA request timing for transmission by this unit.

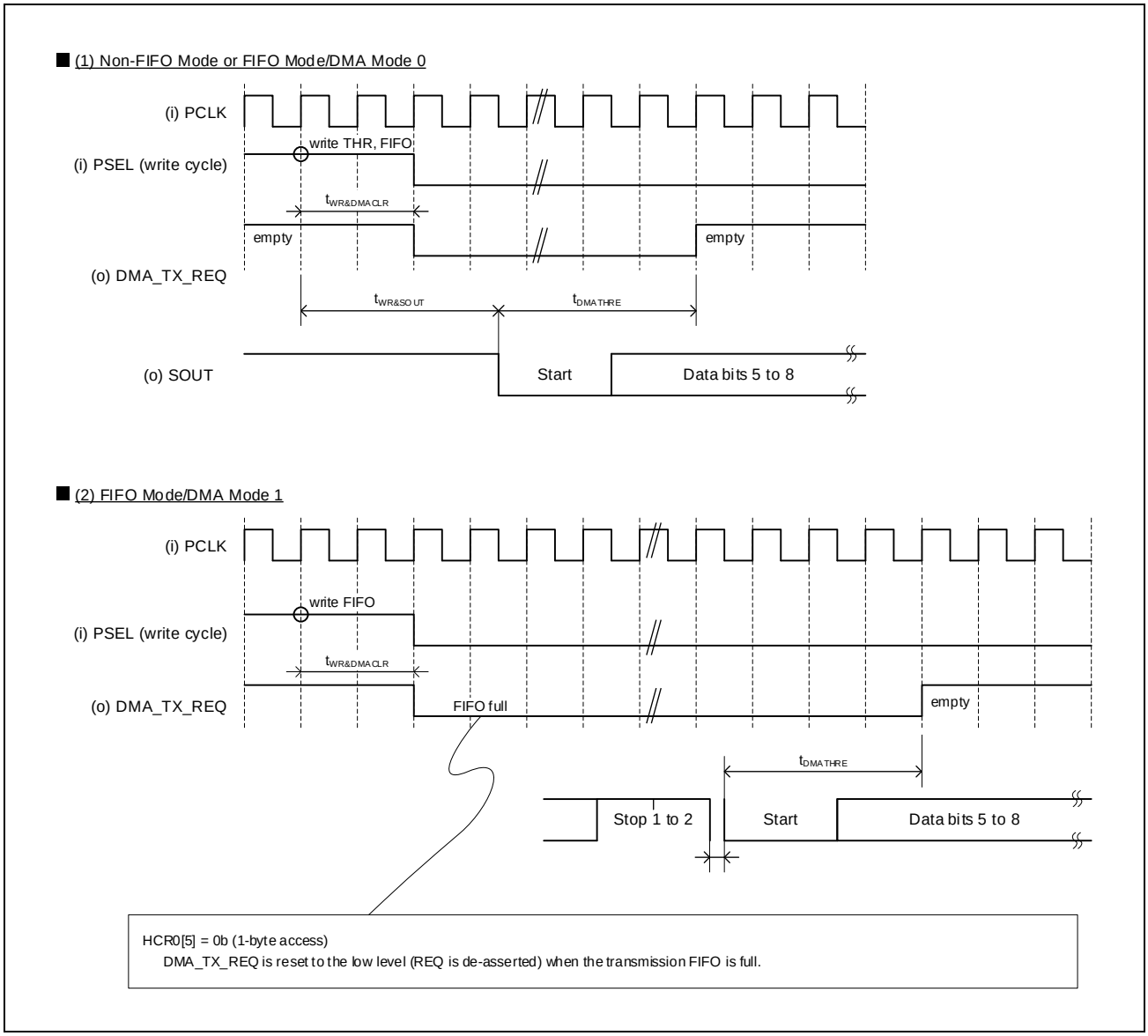


Figure 40.4-9 DMA Request Timing for Transmission

Table 40.4-6 DMA Request Timing for Transmission

Symbol	Parameter	Figure	Min.	Typ.	Max.	Unit	Remarks
$t_{WR\&SOUT}$	Serial data output delay • From writing of data for transmission while THR and FIFO are empty to the falling edge of SOUT (Start)	**Figure 40.4-9**	2	—	3	BAUDOUT_N cycle	$t_{WR\&SOUT}$ = BAUDOUT_N cycles + PCLK cycles
			3	—	3	PCLK cycle	
$t_{WR\&DMACLR}$	Transmission data write DMA request clearing delay • Falling edge of the write enable signal => Falling edge of DMA_TX_REQ		2			PCLK cycle	
$t_{DMATHRE}$	Transmission THE and FIFO empty DMA request delay • Falling edge of Start => Rising edge of DMA_TX_REQ		3	—	4	PCLK cycle	
t_{TRSDW}	Serial data interval for consecutive transmission • Last bit <=> Falling edge of Start for a next frame		1			BAUDOUT_N cycle	

Note: The specifications listed in this table are all theoretical values based on RTL.

40.5 Procedure

40.5.1 Initialization of the UART

The following describes the basic initialization procedures which are required to operate this unit.

1. Input PRESETn (master reset).

↓

2. Set the baud rate.

LCR[7] = 1b	Enable access to DLM and DL.
↓	
Set DLM and DLL	Set the divisor.
↓	
LCR[7] = 0b	Disable access to DLM and DLL. Generation of a 16x baud rate clock is started.

↓

3. Set the FIFO.

FCR[0]	Set FIFO mode or non-FIFO mode.
FCR[3]	Select the DMA mode.
FCR[5]	Select FIFO 16- or 64-byte mode.
FCR[7:6]	Select the triggering level for the reception FIFO.

↓

4. Set the serial interface.

LCR[1:0]	Specify the data bit length.
LCR[2]	Specify the number of stop bits.
LCR[5:3]	Select parity as odd, even, stick, or none.

↓

5. Set the modem interface.

MCR[0] = 1b	Activate the DTR_N output.
MCR[5][1]	Set flow control. If auto flow control is not to be used, set MCR[1] = 1b to activate the RTS_N output.

Setting for the basic operating modes is now completed.

40.5.2 Data Transfer

After the basic initialization, to proceed with data transfer (PIO transfer, DMA transfer) through the host bus, set IER and HCR0 to activate the interrupt/DMA function.

↓

6. Set the reception line status interrupt and the modem status interrupt.

IER [3:2] =11b

Enabling the modem status interrupt may immediately lead to generation of this interrupt. To prevent this, read the value of the MSR register to clear it before making this setting.

40.5.2.1 PIO Transfer

PIO transfer refers to transfer by interrupt or polling. In reception, processing for reception proceeds upon reception of data. In transmission, processing for transmission proceeds unless the FIFO buffer is full.

↓

- Register settings in the case of data transfer by interrupt

  HCR0[6] Set auto-RTS mode.
  IER[1:0] = 11b Enable interrupts for response to the transmission buffer being empty and received data being present.

40.5.2.2 DMA Transfer

The settings for data transfer with the use of the DMA controller and the flow of transfer are described.

↓

- Setting the value of HW Control Register 0 (HCR0)

  HCR0[6] Set auto-RTS mode.
  HCR0[5:2] Set additional DMA modes.
  HCR0[1:0] = 11b Enable DMA requests for transmission and reception.

The following are flowcharts for DMA transfer in DMA modes (1) to (6) listed in **Table 40.4-3**.

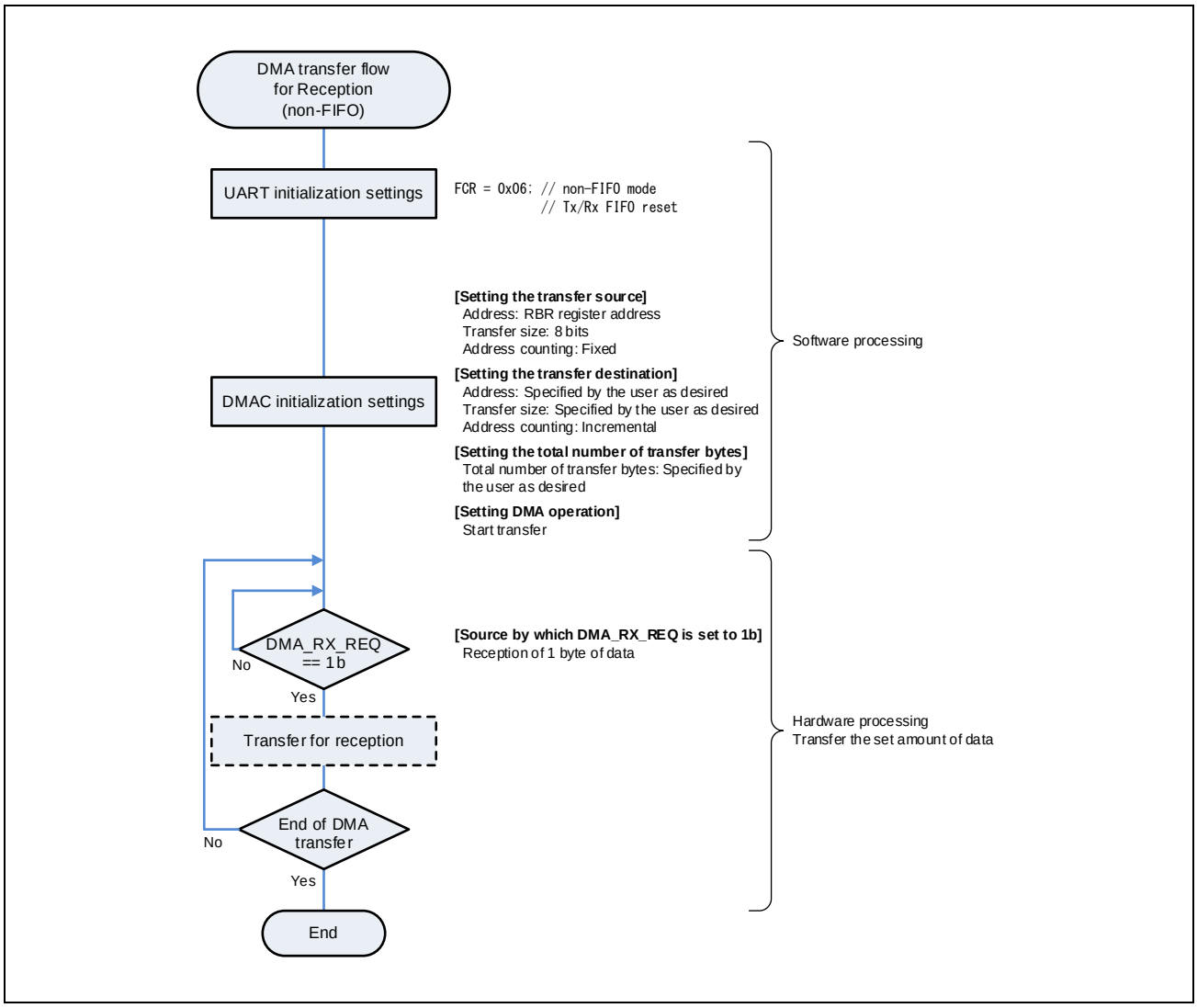
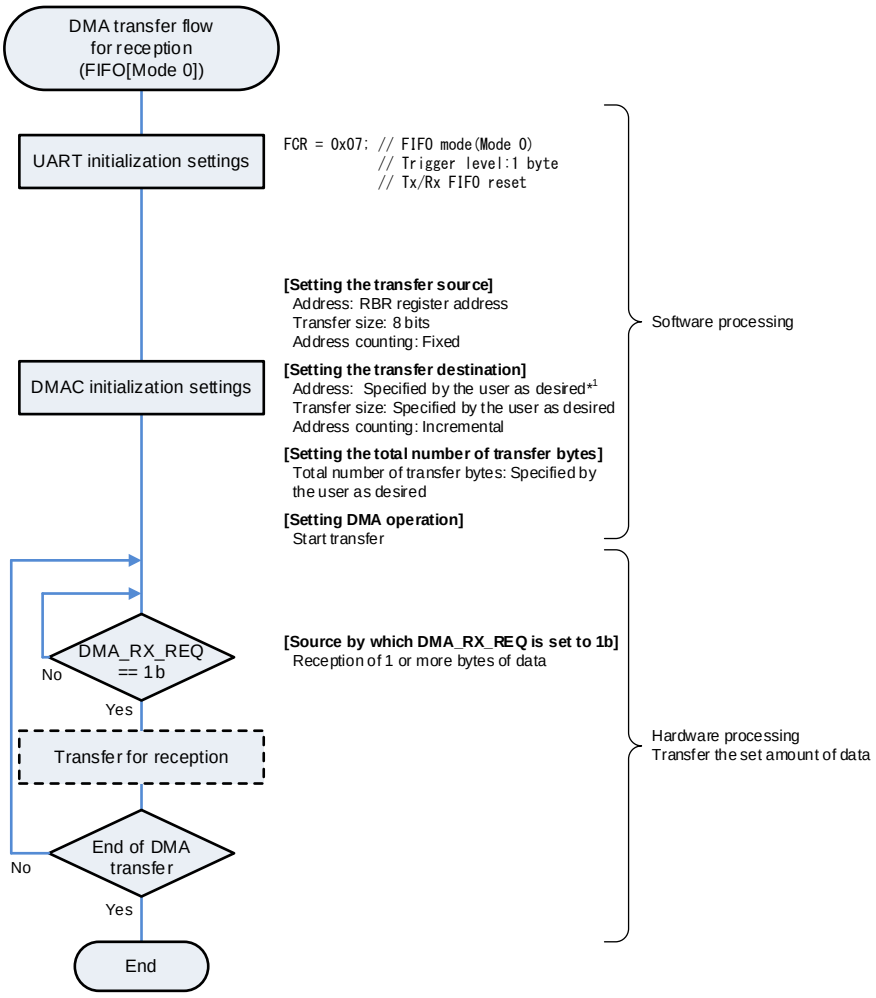
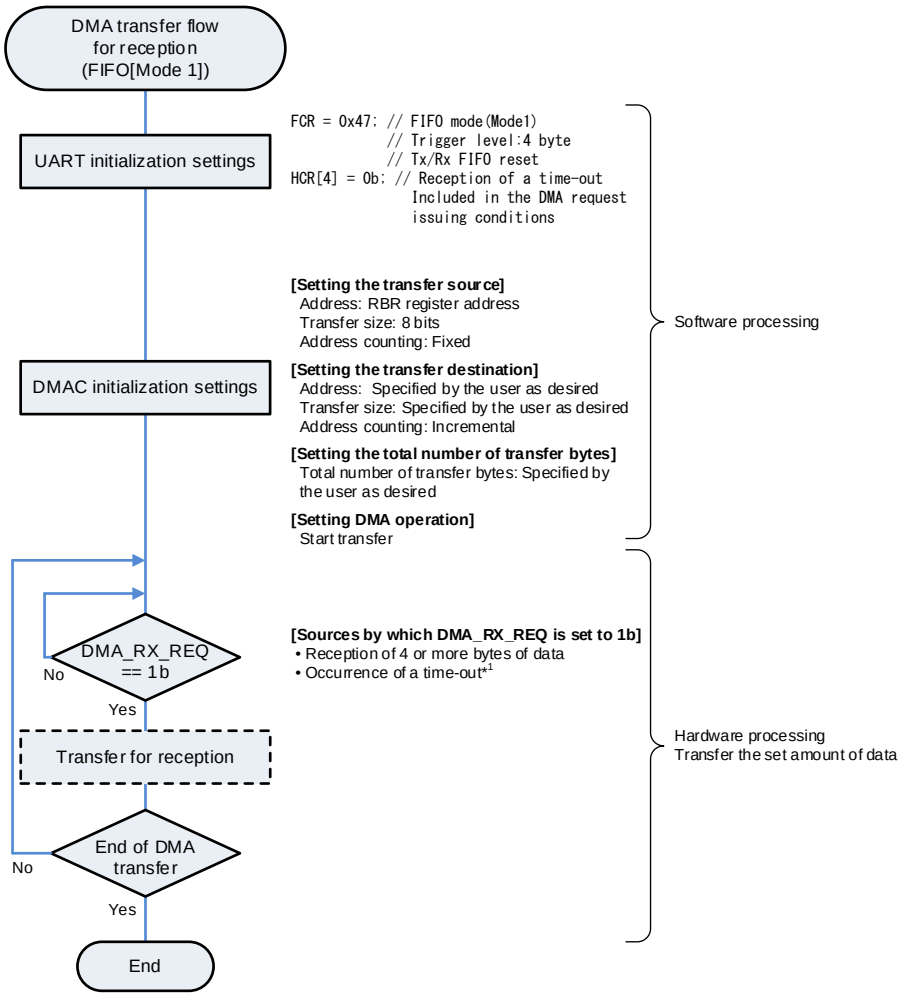


Figure 40.5-1 DMA Transfer Flow for Reception (in (1) Non-FIFO Mode)



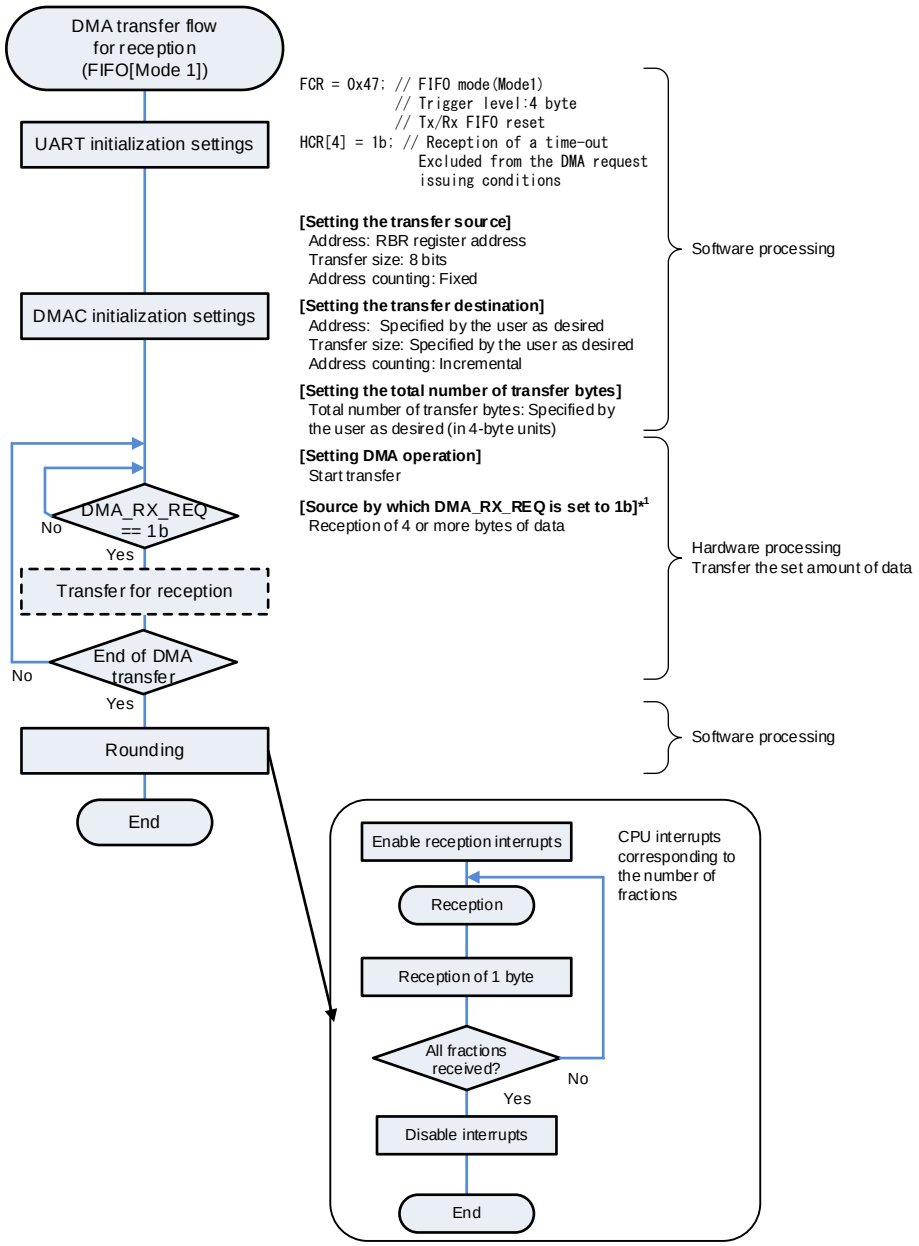
Note 1. When making the settings to make the bus size suit the memory in use, etc., verify that transfer will not create any problem in the given product.

Figure 40.5-2 DMA Transfer Flow for Reception (in (2) Mode 0 when the FIFO Buffer is in Use)



Note 1. Depending on the timing of transfer of received data, DMA transfer of data may not proceed until a time-out occurs even if transfer by this unit has been actually completed.

Figure 40.5-3 DMA Transfer Flow for Reception (a Time-out in Mode 1 when the FIFO Buffer is in Use is Included in the DMA Request Issuing Conditions)



Note 1. As shown in **Section 40.4.4.7, Time-out Timing**, when an error interrupt occurs, the DMA request signal **(**DMA_RX_REQ) also rises and data are transferred. This can be confirmed by checking that the setting of HCR2 [bit 7] (Receiver FIFO Underrun) is 1. The amount of data in the reception FIFO buffer can also be checked by reading HCR2 [bits 6 to 0]. However, care should be taken with time-out errors in such cases because the specification is such that the interrupt is de-asserted when the reception FIFO buffer is read.

Figure 40.5-4 DMA Transfer Flow for Reception (a Time-out in Mode 1 when the FIFO Buffer is in Use is Excluded from the DMA Request Issuing Conditions)

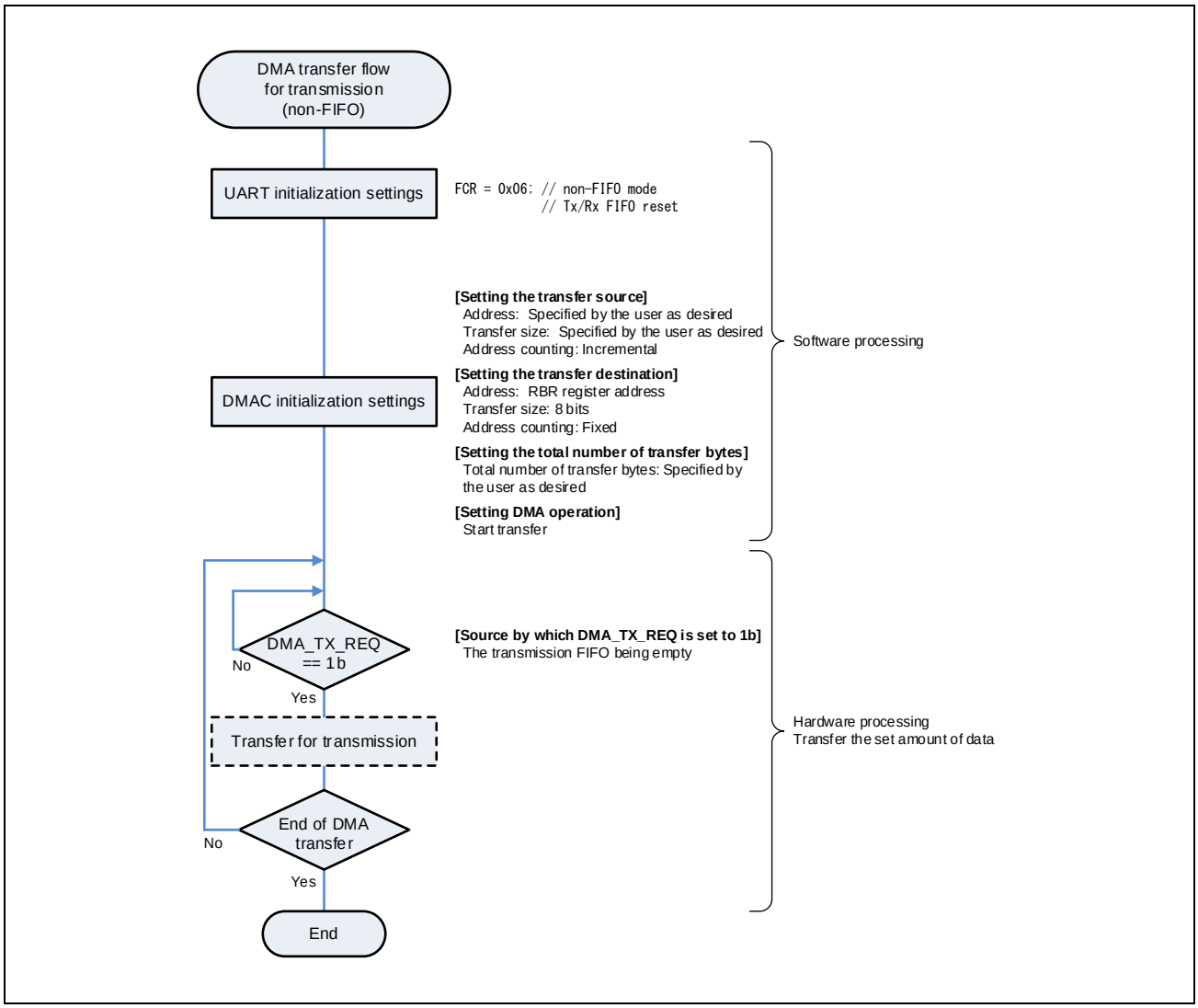
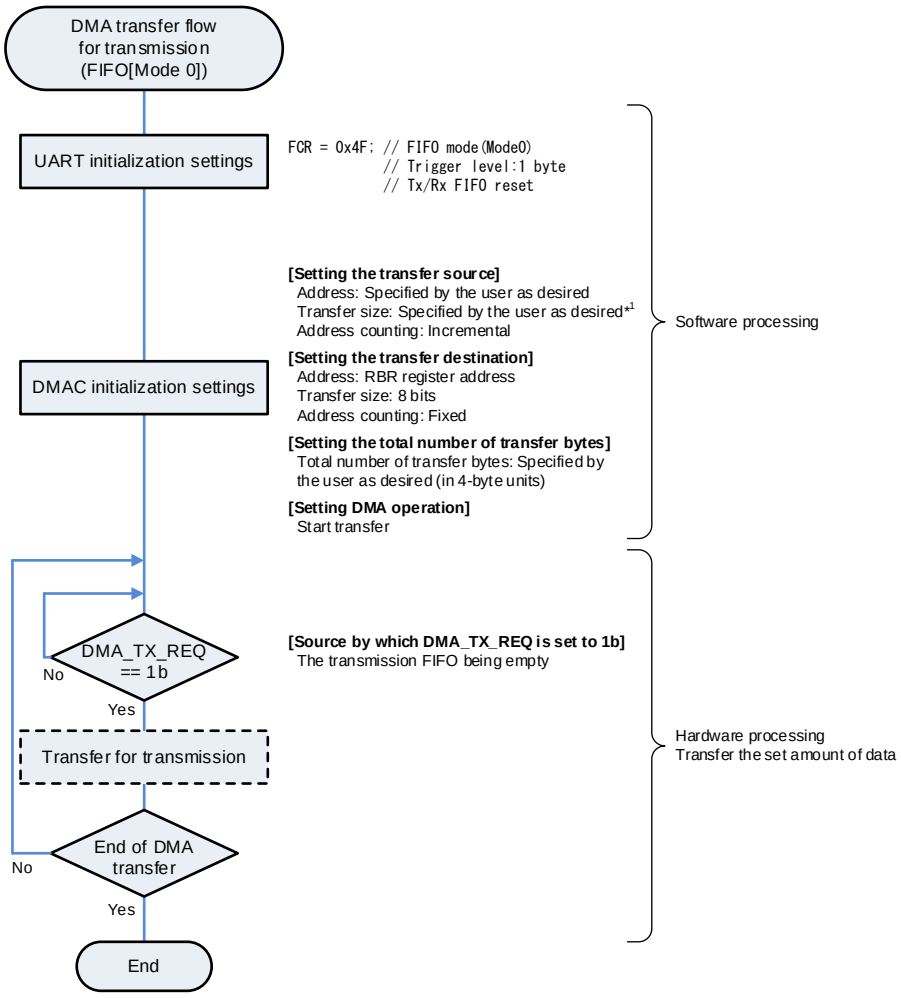
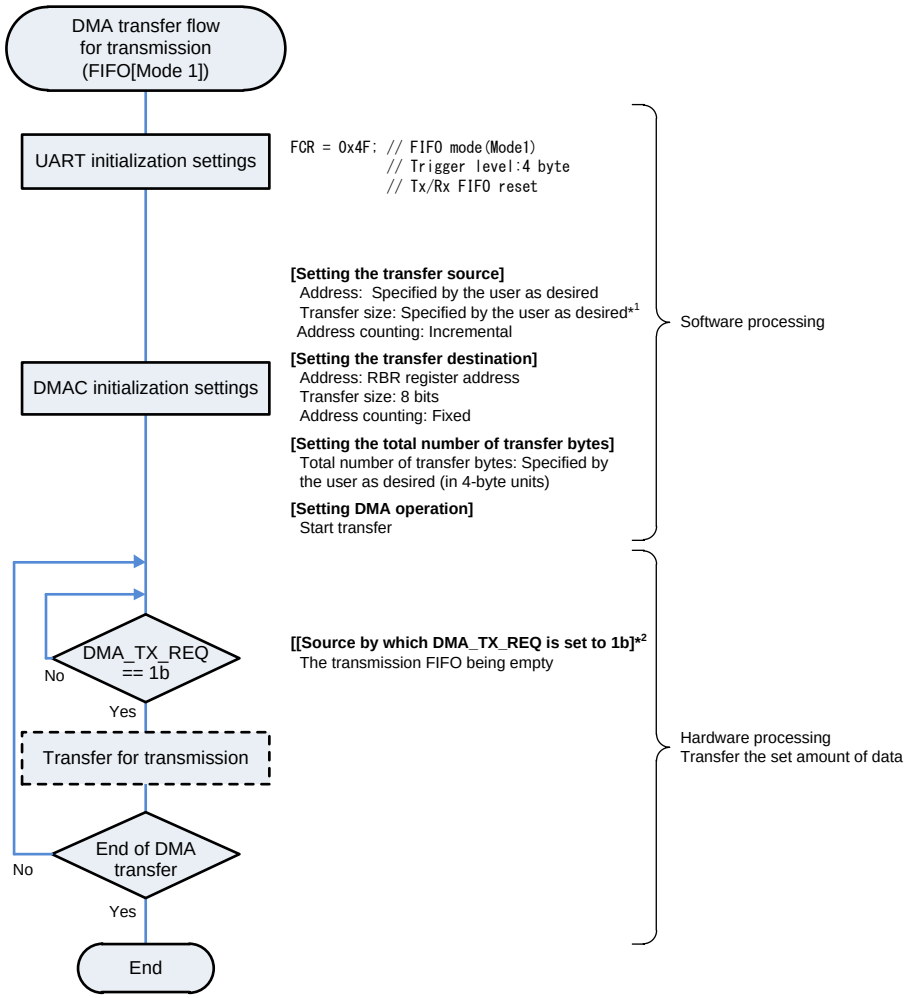


Figure 40.5-5 DMA Transfer Flow for Transmission (in (4) Non-FIFO Mode)



Note 1. When making the settings to make the bus size suit the memory in use, etc., verify that transfer will not create any problem in the given product.

Figure 40.5-6 DMA Transfer Flow for Transmission (in (5) Mode 0)



Note 1. When making the settings to make the bus size suit the memory in use, etc., verify that transfer will not create any problem in the given product.

Note 2. Since the condition for clearing of the DMA request is the transmission FIFO being full, this mode cannot be used except with the per-byte transfer setting.

Figure 40.5-7 DMA Transfer Flow for Transmission (in (6) Mode 1)

40.6 Usage Notes

40.6.1 Point for Caution when Changing the Register Settings

When changing the settings of the following registers, a PRESETn master reset or FIFO reset + SW reset (FCR[2], FCR[1], HCR0[7]) must be input to re-initialize them.

Target Registers: FCR[7:5], FCR[3:0], LCR[7][5:0], MCR[6:4], DLL[7:0], DLM[7:0], HCR0[6:5][3:2]

Section 41 Pin Function Controller (PFC)

This section describes the functions of the pin function controller (PFC).

41.1 Functional Overview

The PFC is a control unit for external pins of the LSI, which includes the general-purpose input/output port (GPIO) function.

The following pins are for use with the ISP support package, so do not use the PFC registers related to these pins.

Pin Names:

PM0, PM1, PM2, PM3, PM4, PM5, PM6, PM7, PM15, INEXINT0, INEXINT1, INEXINT2, INEXINT3,
CSTXD1, CSRXD1, CSSCLK1, CSCS1, CSSCLK2, CSCS2, CSTXD3, CSRXD3, CSSCLK3, CSCS3,
CSTXD5, CSRXD5, CSSCLK5, CSCS5, I2SDA1, I2SCL1,
P0600, P0601, P0602, P0603, P0604, P0605, P0606, P0607,
AULRCK, AUBICK, AUDI, AUDO, AUMCLK, AUPLLCLK,
IM0VS, IM0HS, IM0CS, IM0TXD, IM0RXD, IM0SCLK, IM0SIG0, IM0SIG1, IM0SIG2,
IM1VS, IM1HS, IM1CS, IM1TXD, IM1RXD, IM1SCLK, IM1SIG0, IM1SIG1, IM1SIG2,
IMSHUT0, IMSHUT1, IMSTSIG0, IMSTSIG1,
MTDRV0, MTDRV1, MTDRV2, MTDRV3, MTDRV4, MTDRV5, MTDRV6, MTDRV7,
MTDCPLS0, MTDCPLS1, MTDCPLS2, MTDCPLS3,
MTCS0, MTTXD0, MTRXD0, MTSCLK0, MTCS1, MTTXD1, MTRXD1, MTSCLK1,
HDSCL, HDSDA, HDHPD

As this pin is intended to be used for LED control during the boot sequence, do not use the registers related to it.

Pin Name: MD8

Table 41.1-1 PFC Functions in Outline

Category	Function	Description
Pin Function Controller	Pin Function Controller	• GPIO control • LSI multiplexed pin switching • Pull-up/down control for LSI pins • Drive strength switching for LSI pins • Slew rate switching for LSI pins • CSRXD input pin selection • External interrupt signal masking control • External interrupt signal active sense non-inversion/inversion control

41.1.1 Multiplexed Pins

The multiplexed pins of this LSI pin are divided into 20 categories (PORT00 to PORT17. PORT20, and PORT21).
Note: PORT18 and PORT19 are the missing numbers.

Table 41.1-2 lists the correspondence between the external pins and the IO buffer control functions.

Table 41.1-3 lists the correspondence between the external pins, the multiplexed pin functions, and the GPIO functions.

For the control registers, see **Section 41.4.2.1** to **Section 41.4.2.223**.

Supplementary notes:

PF_SEL switching:	Multiplexed function switching control for the external pins
PU/PD switching:	Pull-up/pull-down switching control for the external pins
DRV:	Drive strength switching control for the external pins
SR:	Slew rate switching control for the external pins
DI masking:	Masking control for data input from the external pins
EN masking:	IO buffer input/output enable control for the external pins

Table 41.1-2 External Pins, Port Assignments, and Functions of the Ports (1/5)

External Pin	Port Assignment	External Pin Control					
		PF_SEL Multiplexed Pin Switching	PU/PD Switching	DRV Switching	SR Switching	DI Masking Control	EN Masking Control
NADAT0	PORT00[0]	Yes	Variable	Variable	Variable	Possible	Possible
NADAT1	PORT00[1]	Yes	Variable	Variable	Variable	Possible	Possible
NADAT2	PORT00[2]	Yes	Variable	Variable	Variable	Possible	Possible
NADAT3	PORT00[3]	Yes	Variable	Variable	Variable	Possible	Possible
NADAT4	PORT00[4]	Yes	Variable	Variable	Variable	Possible	Possible
NADAT5	PORT00[5]	Yes	Variable	Variable	Variable	Possible	Possible
NADAT6	PORT00[6]	Yes	Variable	Variable	Variable	Possible	Possible
NADAT7	PORT00[7]	Yes	Variable	Variable	Variable	Possible	Possible
NACEN	PORT00[8]	Yes	Variable	Variable	Variable	Possible	Possible
NAREN	PORT00[9]	Yes	Variable	Variable	Variable	Possible	Possible
NAWEN	PORT00[10]	Yes	Variable	Variable	Variable	Possible	Possible
NACLE	PORT00[11]	Yes	Variable	Variable	Variable	Possible	Possible
NAALE	PORT00[12]	Yes	Variable	Variable	Variable	Possible	Possible
NARBN	PORT00[13]	Yes	Variable	Variable	Variable	Possible	Possible
PM0	PORT01[0]	Yes	Variable	Variable	Variable	Possible	Possible
PM1	PORT01[1]	Yes	Variable	Variable	Variable	Possible	Possible
PM2	PORT01[2]	Yes	Variable	Variable	Variable	Possible	Possible
PM3	PORT01[3]	Yes	Variable	Variable	Variable	Possible	Possible
PM4	PORT01[4]	Yes	Variable	Variable	Variable	Possible	Possible
PM5	PORT01[5]	Yes	Variable	Variable	Variable	Possible	Possible
PM6	PORT01[6]	Yes	Variable	Variable	Variable	Possible	Possible
PM7	PORT01[7]	Yes	Variable	Variable	Variable	Possible	Possible

Table 41.1-2 External Pins, Port Assignments, and Functions of the Ports (2/5)

External Pin	Port Assignment	External Pin Control					
		PF_SEL Multiplexed Pin Switching	PU/PD Switching	DRV Switching	SR Switching	DI Masking Control	EN Masking Control
PM8	PORT01[8]	Yes	Variable	Variable	Variable	Possible	Possible
PM9	PORT01[9]	Yes	Variable	Variable	Variable	Possible	Possible
PM10	PORT01[10]	Yes	Variable	Variable	Variable	Possible	Possible
PM11	PORT01[11]	Yes	Variable	Variable	Variable	Possible	Possible
PM12	PORT01[12]	Yes	Variable	Variable	Variable	Possible	Possible
PM13	PORT01[13]	Yes	Variable	Variable	Variable	Possible	Possible
PM14	PORT01[14]	Yes	Variable	Variable	Variable	Possible	Possible
PM15	PORT01[15]	Yes	Variable	Variable	Variable	Possible	Possible
INEXINT0	PORT02[0]	Yes	Variable	Variable	Variable	Possible	Possible
INEXINT1	PORT02[1]	Yes	Variable	Variable	Variable	Possible	Possible
INEXINT2	PORT02[2]	Yes	Variable	Variable	Variable	Possible	Possible
INEXINT3	PORT02[3]	Yes	Variable	Variable	Variable	Possible	Possible
INEXINT4	PORT02[4]	Yes	Variable	Variable	Variable	Possible	Possible
INEXINT5	PORT02[5]	Yes	Variable	Variable	Variable	Possible	Possible
INEXINT6	PORT02[6]	Yes	Variable	Variable	Variable	Possible	Possible
INEXINT7	PORT02[7]	Yes	Variable	Variable	Variable	Possible	Possible
CSTXD0	PORT03[0]	Yes	Variable	Variable	Variable	Possible	Possible
CSRXD0	PORT03[1]	Yes	Variable	Variable	Variable	Possible	Possible
CSSCLK0	PORT03[2]	Yes	Variable	Variable	Variable	Possible	Possible
CSCS0	PORT03[3]	Yes	Variable	Variable	Variable	Possible	Possible
CSTXD1	PORT03[4]	Yes	Variable	Variable	Variable	Possible	Possible
CSRXD1	PORT03[5]	Yes	Variable	Variable	Variable	Possible	Possible
CSSCLK1	PORT03[6]	Yes	Variable	Variable	Variable	Possible	Possible
CSCS1	PORT03[7]	Yes	Variable	Variable	Variable	Possible	Possible
CSTXD2	PORT03[8]	Yes	Variable	Variable	Variable	Possible	Possible
CSRXD2	PORT03[9]	Yes	Variable	Variable	Variable	Possible	Possible
CSSCLK2	PORT03[10]	Yes	Variable	Variable	Variable	Possible	Possible
CSCS2	PORT03[11]	Yes	Variable	Variable	Variable	Possible	Possible
CSTXD3	PORT03[12]	Yes	Variable	Variable	Variable	Possible	Possible
CSRXD3	PORT03[13]	Yes	Variable	Variable	Variable	Possible	Possible
CSSCLK3	PORT03[14]	Yes	Variable	Variable	Variable	Possible	Possible
CSCS3	PORT03[15]	Yes	Variable	Variable	Variable	Possible	Possible
CSTXD4	PORT04[0]	Yes	Variable	Variable	Variable	Possible	Possible
CSRXD4	PORT04[1]	Yes	Variable	Variable	Variable	Possible	Possible
CSSCLK4	PORT04[2]	Yes	Variable	Variable	Variable	Possible	Possible
CSCS4	PORT04[3]	Yes	Variable	Variable	Variable	Possible	Possible
CSTXD5	PORT04[4]	Yes	Variable	Variable	Variable	Possible	Possible
CSRXD5	PORT04[5]	Yes	Variable	Variable	Variable	Possible	Possible
CSSCLK5	PORT04[6]	Yes	Variable	Variable	Variable	Possible	Possible
CSCS5	PORT04[7]	Yes	Variable	Variable	Variable	Possible	Possible

Table 41.1-2 External Pins, Port Assignments, and Functions of the Ports (3/5)

External Pin	Port Assignment	External Pin Control					
		PF_SEL Multiplexed Pin Switching	PU/PD Switching	DRV Switching	SR Switching	DI Masking Control	EN Masking Control
I2SDA0	PORT05[0]	Yes	Variable	Variable	Variable	Possible	Possible
I2SCL0	PORT05[1]	Yes	Variable	Variable	Variable	Possible	Possible
I2SDA1	PORT05[2]	Yes	Variable	Variable	Variable	Possible	Possible
I2SCL1	PORT05[3]	Yes	Variable	Variable	Variable	Possible	Possible
P0600	PORT06[0]	Yes	Variable	Variable	Variable	Possible	Possible
P0601	PORT06[1]	Yes	Variable	Variable	Variable	Possible	Possible
P0602	PORT06[2]	Yes	Variable	Variable	Variable	Possible	Possible
P0603	PORT06[3]	Yes	Variable	Variable	Variable	Possible	Possible
P0604	PORT06[4]	Yes	Variable	Variable	Variable	Possible	Possible
P0605	PORT06[5]	Yes	Variable	Variable	Variable	Possible	Possible
P0606	PORT06[6]	Yes	Variable	Variable	Variable	Possible	Possible
P0607	PORT06[7]	Yes	Variable	Variable	Variable	Possible	Possible
P0608	PORT06[8]	Yes	Variable	Variable	Variable	Possible	Possible
P0609	PORT06[9]	Yes	Variable	Variable	Variable	Possible	Possible
P0610	PORT06[10]	Yes	Variable	Variable	Variable	Possible	Possible
P0611	PORT06[11]	Yes	Variable	Variable	Variable	Possible	Possible
AULRCK	PORT07[0]	Yes	Variable	Variable	Variable	Possible	Possible
AUBICK	PORT07[1]	Yes	Variable	Variable	Variable	Possible	Possible
AUDI	PORT07[2]	Yes	Variable	Variable	Variable	Possible	Possible
AUDO	PORT07[3]	Yes	Variable	Variable	Variable	Possible	Possible
AUMCLK	PORT07[4]	Yes	Variable	Variable	Variable	Possible	Possible
AUPLLCLK	PORT07[5]	Yes	Variable	Variable	Variable	Possible	Possible
SD0CMD	PORT08[0]	Yes	Variable	Variable	Variable	Possible	Possible
SD0CLK	PORT08[1]	Yes	Variable	Variable	Variable	Possible	Possible
SD0DAT0	PORT08[2]	Yes	Variable	Variable	Variable	Possible	Possible
SD0DAT1	PORT08[3]	Yes	Variable	Variable	Variable	Possible	Possible
SD0DAT2	PORT08[4]	Yes	Variable	Variable	Variable	Possible	Possible
SD0DAT3	PORT08[5]	Yes	Variable	Variable	Variable	Possible	Possible
SD0WP	PORT08[6]	Yes	Variable	Variable	Variable	Possible	Possible
SD0CD	PORT08[7]	Yes	Variable	Variable	Variable	Possible	Possible
SD1FCMD	PORT09[0]	Yes	Variable	Variable	Variable	Possible	Possible
SD1FCLK	PORT09[1]	Yes	Variable	Variable	Variable	Possible	Possible
SD1FDAT0	PORT09[2]	Yes	Variable	Variable	Variable	Possible	Possible
SD1FDAT1	PORT09[3]	Yes	Variable	Variable	Variable	Possible	Possible
SD1FDAT2	PORT09[4]	Yes	Variable	Variable	Variable	Possible	Possible
SD1FDAT3	PORT09[5]	Yes	Variable	Variable	Variable	Possible	Possible
SD1FWP	PORT09[6]	Yes	Variable	Variable	Variable	Possible	Possible
SD1FCD	PORT09[7]	Yes	Variable	Variable	Variable	Possible	Possible
IM0VS	PORT10[0]	Yes	Variable	Variable	Variable	Possible	Possible
IM0HS	PORT10[1]	Yes	Variable	Variable	Variable	Possible	Possible
IM0CS	PORT10[2]	Yes	Variable	Variable	Variable	Possible	Possible
IM0TXD	PORT10[3]	Yes	Variable	Variable	Variable	Possible	Possible
IM0RXD	PORT10[4]	Yes	Variable	Variable	Variable	Possible	Possible

Table 41.1-2 External Pins, Port Assignments, and Functions of the Ports (4/5)

External Pin	Port Assignment	External Pin Control					
		PF_SEL Multiplexed Pin Switching	PU/PD Switching	DRV Switching	SR Switching	DI Masking Control	EN Masking Control
IM0SCLK	PORT10[5]	Yes	Variable	Variable	Variable	Possible	Possible
IM0SIG0	PORT10[6]	Yes	Variable	Variable	Variable	Possible	Possible
IM0SIG1	PORT10[7]	Yes	Variable	Variable	Variable	Possible	Possible
IM0SIG2	PORT10[8]	Yes	Variable	Variable	Variable	Possible	Possible
IM1VS	PORT11[0]	Yes	Variable	Variable	Variable	Possible	Possible
IM1HS	PORT11[1]	Yes	Variable	Variable	Variable	Possible	Possible
IM1CS	PORT11[2]	Yes	Variable	Variable	Variable	Possible	Possible
IM1TXD	PORT11[3]	Yes	Variable	Variable	Variable	Possible	Possible
IM1RXD	PORT11[4]	Yes	Variable	Variable	Variable	Possible	Possible
IM1SCLK	PORT11[5]	Yes	Variable	Variable	Variable	Possible	Possible
IM1SIG0	PORT11[6]	Yes	Variable	Variable	Variable	Possible	Possible
IM1SIG1	PORT11[7]	Yes	Variable	Variable	Variable	Possible	Possible
IM1SIG2	PORT11[8]	Yes	Variable	Variable	Variable	Possible	Possible
IMSHUT0	PORT12[0]	Yes	Variable	Variable	Variable	Possible	Possible
IMSHUT1	PORT12[1]	Yes	Variable	Variable	Variable	Possible	Possible
IMSTSIG0	PORT12[2]	Yes	Variable	Variable	Variable	Possible	Possible
IMSTSIG1	PORT12[3]	Yes	Variable	Variable	Variable	Possible	Possible
MTDRV0	PORT13[0]	Yes	Variable	Variable	Variable	Possible	Possible
MTDRV1	PORT13[1]	Yes	Variable	Variable	Variable	Possible	Possible
MTDRV2	PORT13[2]	Yes	Variable	Variable	Variable	Possible	Possible
MTDRV3	PORT13[3]	Yes	Variable	Variable	Variable	Possible	Possible
MTDRV4	PORT13[4]	Yes	Variable	Variable	Variable	Possible	Possible
MTDRV5	PORT13[5]	Yes	Variable	Variable	Variable	Possible	Possible
MTDRV6	PORT13[6]	Yes	Variable	Variable	Variable	Possible	Possible
MTDRV7	PORT13[7]	Yes	Variable	Variable	Variable	Possible	Possible
MTDCPLS0	PORT13[8]	Yes	Variable	Variable	Variable	Possible	Possible
MTDCPLS1	PORT13[9]	Yes	Variable	Variable	Variable	Possible	Possible
MTDCPLS2	PORT13[10]	Yes	Variable	Variable	Variable	Possible	Possible
MTDCPLS3	PORT13[11]	Yes	Variable	Variable	Variable	Possible	Possible
MTCS0	PORT14[0]	Yes	Variable	Variable	Variable	Possible	Possible
MTTXD0	PORT14[1]	Yes	Variable	Variable	Variable	Possible	Possible
MTRXD0	PORT14[2]	Yes	Variable	Variable	Variable	Possible	Possible
MTSCLK0	PORT14[3]	Yes	Variable	Variable	Variable	Possible	Possible
MTCS1	PORT14[4]	Yes	Variable	Variable	Variable	Possible	Possible
MTTXD1	PORT14[5]	Yes	Variable	Variable	Variable	Possible	Possible
MTRXD1	PORT14[6]	Yes	Variable	Variable	Variable	Possible	Possible
MTSCLK1	PORT14[7]	Yes	Variable	Variable	Variable	Possible	Possible
GETXC	PORT15[0]	Yes	Variable	Variable	Variable	Possible	Possible
GETXEN	PORT15[1]	Yes	Variable	Variable	Variable	Possible	Possible
GETXER	PORT15[2]	Yes	Variable	Variable	Variable	Possible	Possible
GETXD0	PORT15[3]	Yes	Variable	Variable	Variable	Possible	Possible
GETXD1	PORT15[4]	Yes	Variable	Variable	Variable	Possible	Possible
GETXD2	PORT15[5]	Yes	Variable	Variable	Variable	Possible	Possible

Table 41.1-2 External Pins, Port Assignments, and Functions of the Ports (5/5)

External Pin	Port Assignment	External Pin Control					
		PF_SEL Multiplexed Pin Switching	PU/PD Switching	DRV Switching	SR Switching	DI Masking Control	EN Masking Control
GETXD3	PORT15[6]	Yes	Variable	Variable	Variable	Possible	Possible
GETXD4	PORT15[7]	Yes	Variable	Variable	Variable	Possible	Possible
GETXD5	PORT15[8]	Yes	Variable	Variable	Variable	Possible	Possible
GETXD6	PORT15[9]	Yes	Variable	Variable	Variable	Possible	Possible
GETXD7	PORT15[10]	Yes	Variable	Variable	Variable	Possible	Possible
GERXC	PORT15[11]	Yes	Variable	Variable	Variable	Possible	Possible
GERXDV	PORT15[12]	Yes	Variable	Variable	Variable	Possible	Possible
GERXER	PORT15[13]	Yes	Variable	Variable	Variable	Possible	Possible
GERXD0	PORT15[14]	Yes	Variable	Variable	Variable	Possible	Possible
GERXD1	PORT15[15]	Yes	Variable	Variable	Variable	Possible	Possible
GERXD2	PORT16[0]	Yes	Variable	Variable	Variable	Possible	Possible
GERXD3	PORT16[1]	Yes	Variable	Variable	Variable	Possible	Possible
GERXD4	PORT16[2]	Yes	Variable	Variable	Variable	Possible	Possible
GERXD5	PORT16[3]	Yes	Variable	Variable	Variable	Possible	Possible
GERXD6	PORT16[4]	Yes	Variable	Variable	Variable	Possible	Possible
GERXD7	PORT16[5]	Yes	Variable	Variable	Variable	Possible	Possible
GECRS	PORT16[6]	Yes	Variable	Variable	Variable	Possible	Possible
GECOL	PORT16[7]	Yes	Variable	Variable	Variable	Possible	Possible
GEMDC	PORT16[8]	Yes	Variable	Variable	Variable	Possible	Possible
GEMDIO	PORT16[9]	Yes	Variable	Variable	Variable	Possible	Possible
GEGTXCLK	PORT16[10]	Yes	Variable	Variable	Variable	Possible	Possible
GELINK	PORT16[11]	Yes	Variable	Variable	Variable	Possible	Possible
GEINT	PORT16[12]	Yes	Variable	Variable	Variable	Possible	Possible
GECLK	PORT16[13]	Yes	Variable	Variable	Variable	Possible	Possible
GEPPS	PORT17[0]	Yes	Variable	Variable	Variable	Possible	Possible
HDSCL	PORT20[0]	Yes	Fixed (OFF)	Variable	—	Possible	Possible
HDSDA	PORT20[1]	Yes	Fixed (OFF)	Variable	—	Possible	Possible
HDHPD	PORT20[2]	Yes	Fixed (OFF)	Variable	—	Possible	Possible
MD8	PORT21[0]	—	Fixed (OFF)	Variable	Variable	—	—

Note: "—" indicates that these pins have no function.

Table 41.1-3 Correspondence between External Pins (Ports) and Multiplexed Function Pins (1/5)

External Pin	Port Assignment	Multiplexed Pin Function (PF_SEL Multiplexed Pin Switching)							
		Multiplexed Pin 0	Multiplexed Pin 1	Multiplexed Pin 2	Multiplexed Pin 3	Multiplexed Pin 4	Multiplexed Pin 5	Multiplexed Pin 6	Multiplexed Pin 7
NADAT0	PORT00[0]	P00_00	NADAT0	MMDAT0	—	—	—	—	—
NADAT1	PORT00[1]	P00_01	NADAT1	MMDAT1	—	—	—	—	—
NADAT2	PORT00[2]	P00_02	NADAT2	MMDAT2	—	—	—	—	—
NADAT3	PORT00[3]	P00_03	NADAT3	MMDAT3	—	—	—	—	—
NADAT4	PORT00[4]	P00_04	NADAT4	MMDAT4	—	—	—	—	—
NADAT5	PORT00[5]	P00_05	NADAT5	MMDAT5	—	—	—	—	—
NADAT6	PORT00[6]	P00_06	NADAT6	MMDAT6	—	—	—	—	—
NADAT7	PORT00[7]	P00_07	NADAT7	MMDAT7	—	—	—	—	—
NACEN	PORT00[8]	P00_08	NACEN	—	—	—	—	—	—
NAREN	PORT00[9]	P00_09	NAREN	—	—	—	—	—	—
NAWEN	PORT00[10]	P00_10	NAWEN	MMCMD	—	—	—	—	—
NACLE	PORT00[11]	P00_11	NACLE	MMCLK	—	—	—	—	—
NAALE	PORT00[12]	P00_12	NAALE	—	—	—	—	—	—
NARBN	PORT00[13]	P00_13	NARBN	—	—	—	—	—	—
PM0	PORT01[0]	P01_00	PM0	INEXINT8	—	—	—	—	—
PM1	PORT01[1]	P01_01	PM1	INEXINT9	—	—	—	—	—
PM2	PORT01[2]	P01_02	PM2	INEXINT10	—	—	—	—	—
PM3	PORT01[3]	P01_03	PM3	INEXINT11	—	—	—	—	—
PM4	PORT01[4]	P01_04	PM4	INEXINT12	—	—	—	—	SDTCS1
PM5	PORT01[5]	P01_05	PM5	INEXINT13	GFPLS0	—	—	—	SDTCS2
PM6	PORT01[6]	P01_06	PM6	INEXINT14	GMCLK0	—	—	—	SDTCS3
PM7	PORT01[7]	P01_07	PM7	INEXINT15	GMCLK1	—	—	—	—
PM8	PORT01[8]	P01_08	PM8	INEXINT16	—	—	—	—	—
PM9	PORT01[9]	P01_09	PM9	INEXINT17	—	—	—	—	—
PM10	PORT01[10]	P01_10	PM10	INEXINT18	—	—	—	—	—
PM11	PORT01[11]	P01_11	PM11	INEXINT19	—	—	—	—	—
PM12	PORT01[12]	P01_12	PM12	INEXINT20	—	—	—	—	—
PM13	PORT01[13]	P01_13	PM13	INEXINT21	GFPLS1	—	—	—	—
PM14	PORT01[14]	P01_14	PM14	INEXINT22	GMCLK0	—	—	—	—
PM15	PORT01[15]	P01_15	PM15	INEXINT23	GMCLK1	—	—	—	—
INEXINT0	PORT02[0]	P02_00	—	INEXINT0	—	—	—	—	—
INEXINT1	PORT02[1]	P02_01	—	INEXINT1	—	—	—	—	—
INEXINT2	PORT02[2]	P02_02	—	INEXINT2	—	—	—	—	—
INEXINT3	PORT02[3]	P02_03	—	INEXINT3	—	—	—	—	—
INEXINT4	PORT02[4]	P02_04	—	INEXINT4	—	—	—	—	—
INEXINT5	PORT02[5]	P02_05	—	INEXINT5	—	—	—	—	—
INEXINT6	PORT02[6]	P02_06	—	INEXINT6	—	—	—	—	—
INEXINT7	PORT02[7]	P02_07	—	INEXINT7	—	—	—	—	—
CSTXD0	PORT03[0]	P03_00	CSTXD0	UATX0	CSRXD0	—	—	—	—
CSRXD0	PORT03[1]	P03_01	CSRXD0	UARX0	—	—	—	—	—
CSSCLK0	PORT03[2]	P03_02	CSSCLK0	UACTS0N	—	—	—	—	—
CSCS0	PORT03[3]	P03_03	CSCS0	UARTS0N	—	—	—	—	—
CSTXD1	PORT03[4]	P03_04	CSTXD1	UATX1	CSRXD1	—	—	—	—
CSRXD1	PORT03[5]	P03_05	CSRXD1	UARX1	—	—	—	—	—

Table 41.1-3 Correspondence between External Pins (Ports) and Multiplexed Function Pins (2/5)

External Pin	Port Assignment	Multiplexed Pin Function (PF_SEL Multiplexed Pin Switching)							
		Multiplexed Pin 0	Multiplexed Pin 1	Multiplexed Pin 2	Multiplexed Pin 3	Multiplexed Pin 4	Multiplexed Pin 5	Multiplexed Pin 6	Multiplexed Pin 7
CSSCLK1	PORT03[6]	P03_06	CSSCLK1	UACTS1N	—	TRDAT15	—	—	—
CSCS1	PORT03[7]	P03_07	CSCS1	UARTS1N	—	TRDAT14	—	—	—
CSTXD2	PORT03[8]	P03_08	CSTXD2	I2SDA2	CSRXD2	TRDAT13	—	—	—
CSRXD2	PORT03[9]	P03_09	CSRXD2	I2SCL2	—	TRDAT12	—	—	—
CSSCLK2	PORT03[10]	P03_10	CSSCLK2	I2SDA3	—	TRDAT11	—	—	—
CSCS2	PORT03[11]	P03_11	CSCS2	I2SCL3	—	TRDAT10	—	—	—
CSTXD3	PORT03[12]	P03_12	CSTXD3	CSRXD3	—	TRDAT9	—	—	SDTTXD
CSRXD3	PORT03[13]	P03_13	CSRXD3	—	—	TRDAT8	—	—	SDTRXD
CSSCLK3	PORT03[14]	P03_14	CSSCLK3	—	—	TRDAT7	—	—	SDTSCLK
CSCS3	PORT03[15]	P03_15	CSCS3	—	—	TRDAT6	—	—	SDTCS0
CSTXD4	PORT04[0]	P04_00	CSTXD4	CSRXD4	—	TRDAT5	—	—	—
CSRXD4	PORT04[1]	P04_01	CSRXD4	—	—	TRDAT4	—	—	—
CSSCLK4	PORT04[2]	P04_02	CSSCLK4	—	—	TRDAT3	—	—	—
CSCS4	PORT04[3]	P04_03	CSCS4	—	—	TRDAT2	—	—	—
CSTXD5	PORT04[4]	P04_04	CSTXD5	CSRXD5	—	TRDAT1	—	—	—
CSRXD5	PORT04[5]	P04_05	CSRXD5	—	—	TRDAT0	—	—	—
CSSCLK5	PORT04[6]	P04_06	CSSCLK5	—	—	TRCLK	—	—	—
CSCS5	PORT04[7]	P04_07	CSCS5	—	—	TRCTL	—	—	—
I2SDA0	PORT05[0]	P05_00	—	I2SDA0	—	—	—	—	—
I2SCL0	PORT05[1]	P05_01	—	I2SCL0	—	—	—	—	—
I2SDA1	PORT05[2]	P05_02	—	I2SDA1	—	—	—	—	—
I2SCL1	PORT05[3]	P05_03	—	I2SCL1	—	—	—	—	—
P0600	PORT06[0]	P06_00	—	—	—	—	—	—	—
P0601	PORT06[1]	P06_01	—	—	—	—	—	—	—
P0602	PORT06[2]	P06_02	—	—	—	—	—	—	—
P0603	PORT06[3]	P06_03	—	—	—	—	—	—	—
P0604	PORT06[4]	P06_04	—	—	—	—	—	—	—
P0605	PORT06[5]	P06_05	—	—	—	—	—	—	—
P0606	PORT06[6]	P06_06	—	—	—	—	—	—	—
P0607	PORT06[7]	P06_07	—	—	—	—	—	—	—
P0608	PORT06[8]	P06_08	—	—	—	—	—	—	—
P0609	PORT06[9]	P06_09	—	—	—	—	—	—	—
P0610	PORT06[10]	P06_10	—	—	—	—	—	—	—
P0611	PORT06[11]	P06_11	—	—	—	—	—	—	—
AULRCK	PORT07[0]	P07_00	AULRCK	—	—	—	—	—	—
AUBICK	PORT07[1]	P07_01	AUBICK	—	—	—	—	—	—
AUDI	PORT07[2]	P07_02	AUDI	—	—	—	—	—	—
AUDO	PORT07[3]	P07_03	AUDO	—	—	—	—	—	—
AUMCLK	PORT07[4]	P07_04	AUMCLK	—	—	—	—	—	—
AUPLLCLK	PORT07[5]	P07_05	AUPLLCLK	—	—	—	—	—	—
SD0CMD	PORT08[0]	P08_00	SD0CMD	—	—	—	—	—	—
SD0CLK	PORT08[1]	P08_01	SD0CLK	—	—	—	—	—	—
SD0DAT0	PORT08[2]	P08_02	SD0DAT0	—	—	—	—	—	—
SD0DAT1	PORT08[3]	P08_03	SD0DAT1	—	—	—	—	—	—

Table 41.1-3 Correspondence between External Pins (Ports) and Multiplexed Function Pins (3/5)

External Pin	Port Assignment	Multiplexed Pin Function (PF_SEL Multiplexed Pin Switching)							
		Multiplexed Pin 0	Multiplexed Pin 1	Multiplexed Pin 2	Multiplexed Pin 3	Multiplexed Pin 4	Multiplexed Pin 5	Multiplexed Pin 6	Multiplexed Pin 7
SD0DAT2	PORT08[4]	P08_04	SD0DAT2	—	—	—	—	—	—
SD0DAT3	PORT08[5]	P08_05	SD0DAT3	—	—	—	—	—	—
SD0WP	PORT08[6]	P08_06	SD0WP	—	—	—	—	—	—
SD0CD	PORT08[7]	P08_07	SD0CD	—	—	—	—	—	—
SD1FCMD	PORT09[0]	P09_00	SD1FCMD	—	—	—	—	—	—
SD1FCLK	PORT09[1]	P09_01	SD1FCLK	—	—	—	—	—	—
SD1FDAT0	PORT09[2]	P09_02	SD1FDAT0	—	—	—	—	—	—
SD1FDAT1	PORT09[3]	P09_03	SD1FDAT1	—	—	—	—	—	—
SD1FDAT2	PORT09[4]	P09_04	SD1FDAT2	—	—	—	—	—	—
SD1FDAT3	PORT09[5]	P09_05	SD1FDAT3	—	—	—	—	—	—
SD1FWP	PORT09[6]	P09_06	SD1FWP	INEXINT24	—	—	—	—	—
SD1FCD	PORT09[7]	P09_07	SD1FCD	INEXINT25	—	—	—	—	—
IM0VS	PORT10[0]	P10_00	IM0VS	—	—	—	—	—	—
IM0HS	PORT10[1]	P10_01	IM0HS	—	—	—	—	—	—
IM0CS	PORT10[2]	P10_02	IM0CS	—	—	—	—	—	—
IM0TXD	PORT10[3]	P10_03	IM0TXD	—	—	—	—	—	—
IM0RXD	PORT10[4]	P10_04	IM0RXD	—	—	—	—	—	—
IM0SCLK	PORT10[5]	P10_05	IM0SCLK	—	—	—	—	—	—
IM0SIG0	PORT10[6]	P10_06	IM0SIG0	INEXINT26	—	—	—	—	—
IM0SIG1	PORT10[7]	P10_07	IM0SIG1	INEXINT27	—	—	—	—	—
IM0SIG2	PORT10[8]	P10_08	IM0SIG2	—	—	—	—	—	—
IM1VS	PORT11[0]	P11_00	IM1VS	—	—	—	—	—	—
IM1HS	PORT11[1]	P11_01	IM1HS	—	—	—	—	—	—
IM1CS	PORT11[2]	P11_02	IM1CS	—	—	—	—	—	—
IM1TXD	PORT11[3]	P11_03	IM1TXD	—	—	—	—	—	—
IM1RXD	PORT11[4]	P11_04	IM1RXD	—	—	—	—	—	—
IM1SCLK	PORT11[5]	P11_05	IM1SCLK	—	—	—	—	—	—
IM1SIG0	PORT11[6]	P11_06	IM1SIG0	INEXINT28	—	—	—	—	—
IM1SIG1	PORT11[7]	P11_07	IM1SIG1	INEXINT29	—	—	—	—	—
IM1SIG2	PORT11[8]	P11_08	IM1SIG2	—	—	—	—	—	—
IMSHUT0	PORT12[0]	P12_00	IMSHUT0	INEXINT30	—	—	—	—	—
IMSHUT1	PORT12[1]	P12_01	IMSHUT1	INEXINT31	—	—	—	—	—
IMSTSIG0	PORT12[2]	P12_02	IMSTSIG0	INEXINT32	—	—	—	—	—
IMSTSIG1	PORT12[3]	P12_03	IMSTSIG1	INEXINT33	—	—	—	—	—
MTDRV0	PORT13[0]	P13_00	—	—	MTDRV0	—	—	—	—
MTDRV1	PORT13[1]	P13_01	—	—	MTDRV1	—	—	—	—
MTDRV2	PORT13[2]	P13_02	—	—	MTDRV2	—	—	—	—
MTDRV3	PORT13[3]	P13_03	—	—	MTDRV3	—	—	—	—
MTDRV4	PORT13[4]	P13_04	—	—	MTDRV4	—	—	—	—
MTDRV5	PORT13[5]	P13_05	—	—	MTDRV5	—	—	—	—
MTDRV6	PORT13[6]	P13_06	—	—	MTDRV6	—	—	—	—
MTDRV7	PORT13[7]	P13_07	—	—	MTDRV7	—	—	—	—
MTDCPLS0	PORT13[8]	P13_08	—	—	MTDCPLS0	—	—	—	—
MTDCPLS1	PORT13[9]	P13_09	—	INEXINT34	MTDCPLS1	—	—	—	—

Table 41.1-3 Correspondence between External Pins (Ports) and Multiplexed Function Pins (4/5)

External Pin	Port Assignment	Multiplexed Pin Function (PF_SEL Multiplexed Pin Switching)							
		Multiplexed Pin 0	Multiplexed Pin 1	Multiplexed Pin 2	Multiplexed Pin 3	Multiplexed Pin 4	Multiplexed Pin 5	Multiplexed Pin 6	Multiplexed Pin 7
MTDCPLS2	PORT13[10]	P13_10	—	INEXINT35	MTDCPLS2	—	—	—	—
MTDCPLS3	PORT13[11]	P13_11	—	INEXINT36	MTDCPLS3	—	—	—	—
MTCS0	PORT14[0]	P14_00	—	—	MTCS0	—	—	—	—
MTTXD0	PORT14[1]	P14_01	—	—	MTTXD0	—	—	—	—
MTRXD0	PORT14[2]	P14_02	—	INEXINT37	MTRXD0	—	—	—	—
MTSCLK0	PORT14[3]	P14_03	—	—	MTSCLK0	—	—	—	—
MTCS1	PORT14[4]	P14_04	—	—	MTCS1	—	—	—	—
MTTXD1	PORT14[5]	P14_05	—	—	MTTXD1	—	—	—	—
MTRXD1	PORT14[6]	P14_06	—	INEXINT38	MTRXD1	—	—	—	—
MTSCLK1	PORT14[7]	P14_07	—	—	MTSCLK1	—	—	—	—
GETXC	PORT15[0]	P15_00	GETXC	—	—	TRCLK	—	—	—
GETXEN	PORT15[1]	P15_01	GETXEN	—	—	TRCTL	—	—	—
GETXER	PORT15[2]	P15_02	GETXER	—	—	—	—	—	—
GETXD0	PORT15[3]	P15_03	GETXD0	—	—	—	—	—	—
GETXD1	PORT15[4]	P15_04	GETXD1	—	—	—	—	—	—
GETXD2	PORT15[5]	P15_05	GETXD2	—	—	—	—	—	—
GETXD3	PORT15[6]	P15_06	GETXD3	—	—	—	—	—	—
GETXD4	PORT15[7]	P15_07	GETXD4	—	—	—	—	—	—
GETXD5	PORT15[8]	P15_08	GETXD5	—	—	TRDAT0	—	—	—
GETXD6	PORT15[9]	P15_09	GETXD6	—	—	TRDAT1	—	—	—
GETXD7	PORT15[10]	P15_10	GETXD7	—	—	TRDAT2	—	—	—
GERXC	PORT15[11]	P15_11	GERXC	—	—	TRDAT3	—	—	—
GERXDV	PORT15[12]	P15_12	GERXDV	—	—	TRDAT4	—	—	—
GERXER	PORT15[13]	P15_13	GERXER	—	—	TRDAT5	—	—	—
GERXD0	PORT15[14]	P15_14	GERXD0	—	—	TRDAT6	—	—	—
GERXD1	PORT15[15]	P15_15	GERXD1	—	—	TRDAT7	—	—	—
GERXD2	PORT16[0]	P16_00	GERXD2	—	MTDRV8	TRDAT8	—	—	—
GERXD3	PORT16[1]	P16_01	GERXD3	—	MTDRV9	TRDAT9	—	—	—
GERXD4	PORT16[2]	P16_02	GERXD4	—	MTDRV10	TRDAT10	—	—	—
GERXD5	PORT16[3]	P16_03	GERXD5	—	MTDRV11	TRDAT11	—	—	—
GERXD6	PORT16[4]	P16_04	GERXD6	—	MTDRV12	TRDAT12	—	—	—
GERXD7	PORT16[5]	P16_05	GERXD7	—	MTDRV13	TRDAT13	—	—	—
GECRS	PORT16[6]	P16_06	GECRS	—	MTDRV14	TRDAT14	—	—	—
GECOL	PORT16[7]	P16_07	GECOL	—	MTDRV15	TRDAT15	—	—	—
GEMDC	PORT16[8]	P16_08	GEMDC	—	—	—	—	—	—
GEMDIO	PORT16[9]	P16_09	GEMDIO	—	—	—	—	—	—
GEGTXCLK	PORT16[10]	P16_10	GEGTXCLK	—	—	—	—	—	—
GELINK	PORT16[11]	P16_11	GELINK	—	—	—	—	—	—
GEINT	PORT16[12]	P16_12	GEINT	—	—	—	—	—	—
GECLK	PORT16[13]	P16_13	GECLK	—	—	—	—	—	—
GEPPS	PORT17[0]	P17_00	GEPPS	—	—	—	—	—	—
HDSCL	PORT20[0]	P20_00	HDSCL	—	—	—	—	—	—
HDSDA	PORT20[1]	P20_01	HDSDA	—	—	—	—	—	—
HDHPD	PORT20[2]	P20_02	HDHPD	—	—	—	—	—	—

Table 41.1-3 Correspondence between External Pins (Ports) and Multiplexed Function Pins (5/5)

External Pin	Port Assignment	Multiplexed Pin Function (PF_SEL Multiplexed Pin Switching)							
		Multiplexed Pin 0	Multiplexed Pin 1	Multiplexed Pin 2	Multiplexed Pin 3	Multiplexed Pin 4	Multiplexed Pin 5	Multiplexed Pin 6	Multiplexed Pin 7
MD8	PORT21[0]	P21_00	—	—	—	—	—	—	—

Note: "—" indicates that no multiplexed pin function is assigned and setting is prohibited.

41.1.2 Dedicated Pins

The dedicated pins of this LSI chip are divided into two categories (PEX0, PEX1).

Table 41.1-4 lists the correspondence between the external pins and the IO buffer control functions.

For the control registers, see **Section 41.4.2.225** to **Section 41.4.2.226**.

Supplementary notes:

PF_SEL switching:	Multiplexed function switching control for the external pins
PU/PD switching:	Pull-up/pull-down switching control for the external pins
DRV:	Drive strength switching control for the external pins
SR:	Slew rate switching control for the external pins
DI masking:	Masking control for data input from the external pins
EN masking:	IO buffer input/output enable control for the external pins

Table 41.1-4 Dedicated Pins and Port Assignments

External Pin	Port Assignment	External Pin Control						
		PF_SEL Multiplexed Pin Switching	PU/PD Switching	DRV Switching	SR Switching	DI Masking Control	EN Masking Control	
NAWPN	PEX0[0]	—	Fixed (OFF)	Variable	Variable	—	—	
IM0CLK	PEX0[1]	—	Fixed (OFF)	Variable	Variable	—	—	
IM1CLK	PEX0[2]	—	Fixed (OFF)	Variable	Variable	—	—	
DETCK	PEX0[3]	—	Fixed (PD)	Fixed (X1)	Fixed (slow)	—	—	Input only
DETDI	PEX0[4]	—	Fixed (PU)	Fixed (X1)	Fixed (slow)	—	—	Input only
DETDO	PEX0[5]	—	Fixed (OFF)	Variable	Variable	—	—	
DETMS	PEX0[6]	—	Fixed (PU)	Variable	Variable	—	—	
DETRSTN	PEX0[7]	—	Fixed (PU)	Fixed (X1)	Fixed (slow)	—	—	Input only
DESRSTN	PEX0[8]	—	Fixed (PU)	Fixed (X1)	Fixed (slow)	—	—	Input only
RETEST0	PEX0[9]	—	Fixed (PD)	Fixed (X1)	Fixed (slow)	—	—	Input only
RETEST1	PEX0[10]	—	Fixed (PD)	Fixed (X1)	Fixed (slow)	—	—	Input only
—	PEX0[11]	—	—	—	—	—	—	
PCRSTOUTB	PEX0[12]	—	Fixed (OFF)	Variable	Variable	—	—	
—	PEX0[13]	—	—	—	—	—	—	
USPWEN	PEX0[14]	—	Fixed (OFF)	Variable	Variable	—	—	
USOVC	PEX0[15]	—	Fixed (OFF)	Fixed (X1)	Fixed (slow)	—	—	Input only
—	PEX1[0]	—	—	—	—	—	—	
MD0	PEX1[1]	—	Fixed (OFF)	Fixed (X1)	Fixed (slow)	—	—	Input only
MD1	PEX1[2]	—	Fixed (OFF)	Fixed (X1)	Fixed (slow)	—	—	Input only
MD2	PEX1[3]	—	Fixed (OFF)	Fixed (X1)	Fixed (slow)	—	—	Input only
MD3	PEX1[4]	—	Fixed (OFF)	Fixed (X1)	Fixed (slow)	—	—	Input only
MD4	PEX1[5]	—	Fixed (OFF)	Fixed (X1)	Fixed (slow)	—	—	Input only
MD5	PEX1[6]	—	Fixed (PD)	Fixed (X1)	Fixed (slow)	—	—	Input only
MD6	PEX1[7]	—	Fixed (PD)	Fixed (X1)	Fixed (slow)	—	—	Input only
MD7	PEX1[8]	—	Fixed (OFF)	Fixed (X1)	Fixed (slow)	—	—	Input only

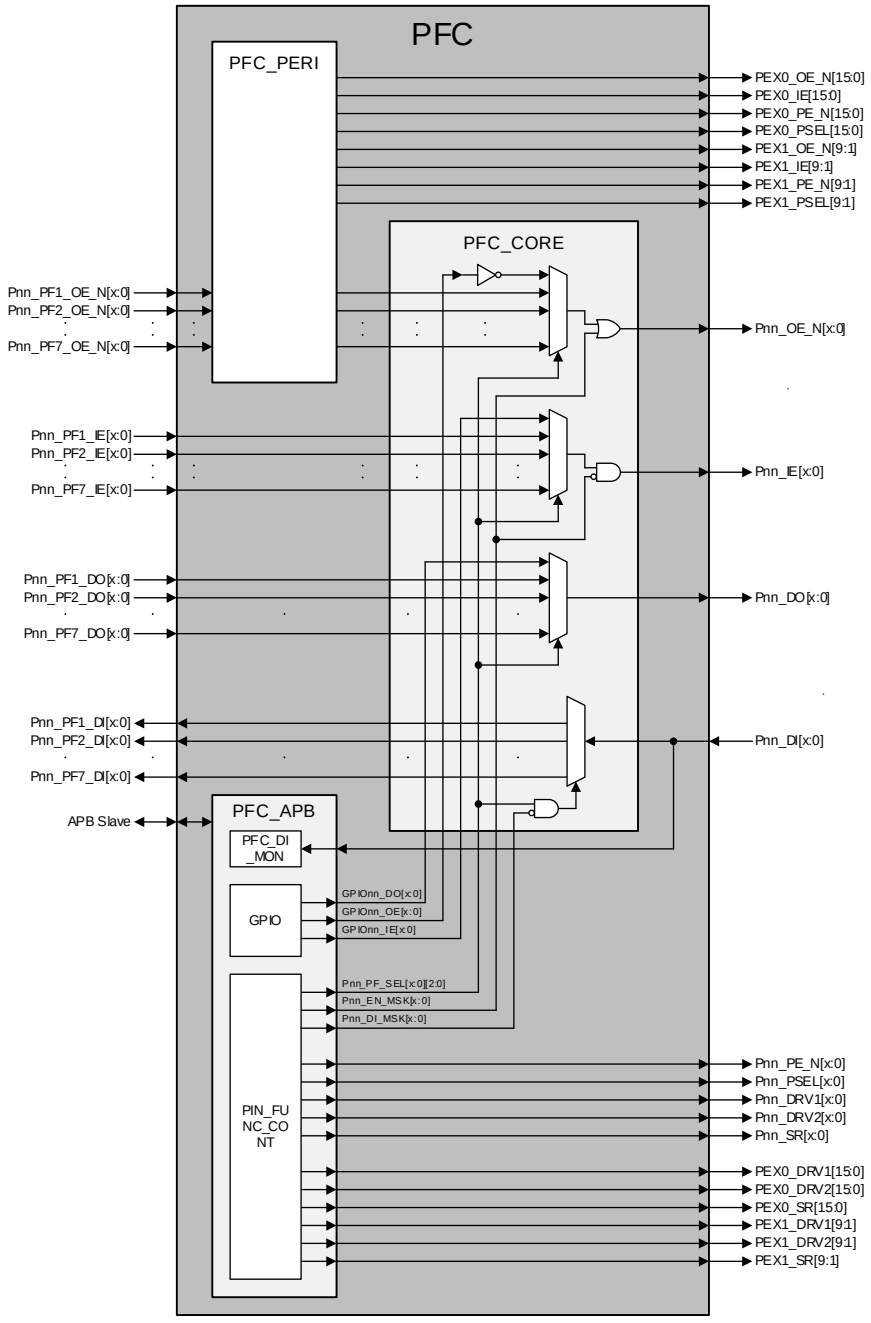
Note: PEX0[11], PEX0[13], and PEX1[0] are the missing numbers because their specifications have been deleted.

Note: "—" indicates that these pins have no function.

41.2 Internal Configuration

Figure 41.2-1 shows the internal configuration of the PFC.

The PFC unit handles switching of the multiplexed pin function and control of the I/O buffer through register control by the APB slave.



Note: nn = 00 to 17, 20 to 21
The value of x differs from port to port.

Figure 41.2-1 Internal Configuration of PFC

- PFC_APB:

  This block handles register control by the APB slave interface.

  It includes the following registers.

  - PFC_DI_MON: A register block for monitoring the input values on the external pins
  - GPIO: A register block for controlling the general-purpose input/output ports
  - PIN_FUNC_CONT: A register block for controlling the following functions

    1. LSI multiplexed pin switching
    2. Pull-up/down control for the LSI pins
    3. Drive strength switching for the LSI pins
    4. Slew rate switching for the LSI pins
    5. Input/output enable masking control for the LSI pins
    6. Masking control for input data from the LSI pins
    7. CSRXD input pin selection
    8. Masking control for the external interrupt signal
    9. Non-version/inversion control for the active sense of the external interrupt signal

- PFC_PERI:

  This block controls the following.

  - Invert the active sense of the active-high output enable signal output by a given unit to make the signal active-low.
  - Output of the I/O buffer control signal in place of the unit that does not output the control signal
  - Selection of the input signal to the CSRXD pin of CSI
  - External interrupt signal masking control
  - External interrupt signal active sense non-inversion/inversion control

- PFC_CORE:

  This block has the following functions.

  - Multiplexed pin function switching for the external pins by the PFC_APB output control signal (Pnn_PFSEL)
    - Selection of the signal output to the corresponding external pin
    - Selection of the output destination of the input signal from the corresponding external pin
  - Forcible disabling of the input/output enable signal of the IO buffer assigned to the multiplexed pins by the PFC_APB output control signal (Pnn_EN_MSK signal) (to prevent glitches which are generated when switching the multiplexed pin function).
  - Forcible masking of input data on the corresponding external pin by the PFC_APB output control signal (Pnn_DI_MSK signal) (to prevent glitches which are generated when switching the multiplexed pin function).

  Note: nn = 00 to 17, 20

41.2.1 Internal Configuration of External Interrupt Signal Active Sense Non-Inversion/Inversion Control and Masking

Non-inversion or inversion of the external interrupt can be controlled by the settings of EXTINT_INV0 to 2 registers.

Additionally, masking of the external interrupt can be controlled by the settings of EXTINT_MSK0 to 2 registers. When the setting is for masking (EXTINT_MSK[n] = 1), the output of the interrupt signal to the interrupt controller (GIC) is fixed at the low level (inactive) regardless of the setting of EXTINT_INV0 to 2 registers and the input value on EXTINT,

Figure 41.2-2 shows the internal configuration of non-inversion/inversion control for the active sense of the external interrupt signal.

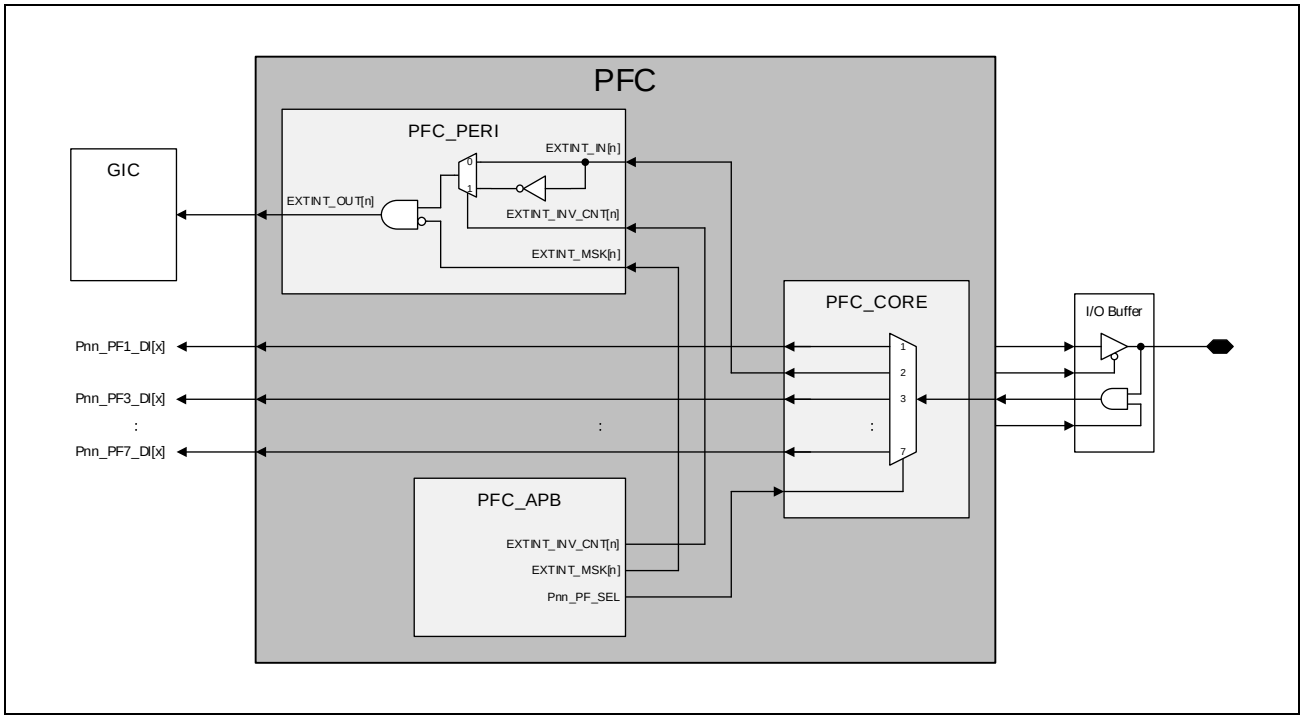


Figure 41.2-2 Internal Configuration of External Interrupt Signal Active Sense Non-Inversion/Inversion Control

41.3 Pin Functions

41.3.1 List of Internal Pins

41.3.1.1 List of Pins for PORT00 and PORT01

Table 41.3-1 lists the internal pins for PORT00 and PORT01.

Table 41.3-1 List of Internal Pins (PORT00, PORT01) (1/2)

Pin Name	I/O	Function
PORT00 I/O Buffer (from/to PAD)		
P00_DO[13:0]	Output	P00 I/O buffer output signal
P00_OE_N[13:0]	Output	P00 I/O buffer output enable signal
P00_DI[13:0]	Input	P00 I/O buffer input signal
P00_IE[13:0]	Output	P00 I/O buffer input enable signal
P00_DRV1[13:0]	Output	P00 I/O buffer drive strength switching signal 1
P00_DRV2[13:0]	Output	P00 I/O buffer drive strength switching signal 2
P00_PE_N[13:0]	Output	P00 I/O buffer pull-up/down enable signal
P00_PSEL[13:0]	Output	P00 I/O buffer pull-up/down switching signal
P00_SR[13:0]	Output	P00 I/O buffer slew rate switching signal
P00_11_IE1	Output	P00[11] I/O buffer returned clock input enable signal
PORT00 Peripheral Pin Function		
P00_PF1_DO[13:0]	Input	P00 multiplexed function 1 output signal
P00_PF2_DO[13:0]	Input	P00 multiplexed function 2 output signal
P00_PF1_OE_N[13:0]	Input	P00 multiplexed function 1 output enable signal
P00_PF2_OE_N[13:0]	Input	P00 multiplexed function 2 output enable signal
P00_PF1_DI[13:0]	Output	P00 multiplexed function 1 input signal
P00_PF2_DI[13:0]	Output	P00 multiplexed function 2 input signal
PORT01 I/O Buffer (from/to PAD)		
P01_DO[15:0]	Output	P01 I/O buffer output signal
P01_OE_N[15:0]	Output	P01 I/O buffer output enable signal
P01_DI[15:0]	Input	P01 I/O buffer input signal
P01_IE[15:0]	Output	P01 I/O buffer input enable signal
P01_DRV1[15:0]	Output	P01 I/O buffer drive strength switching signal 1
P01_DRV2[15:0]	Output	P01 I/O buffer drive strength switching signal 2
P01_PE_N[15:0]	Output	P01 I/O buffer pull-up/down enable signal
P01_PSEL[15:0]	Output	P01 I/O buffer pull-up/down switching signal
P01_SR[15:0]	Output	P01 I/O buffer slew rate switching signal
PORT01 Peripheral Pin Function		
P01_PF1_DO[15:0]	Input	P01 multiplexed function 1 output signal
P01_PF3_DO[15:0]	Input	P01 multiplexed function 3 output signal
P01_PF5_DO[15:0]	Input	P01 multiplexed function 5 output signal
P01_PF6_DO[15:0]	Input	P01 multiplexed function 6 output signal
P01_PF7_DO[15:0]	Input	P01 multiplexed function 7 output signal
P01_PF3_OE[15:0]	Input	P01 multiplexed function 3 output enable signal
P01_PF3_IE[15:0]	Input	P01 multiplexed function 3 input enable signal
P01_PF2_DI[15:0]	Output	P01 multiplexed function 2 input signal

Table 41.3-1 List of Internal Pins (PORT00, PORT01) (2/2)

Pin Name	I/O	Function
P01_PF3_DI[15:0]	Output	P01 multiplexed function 3 input signal
P01_PF7_DI[15:0]	Output	P01 multiplexed function 7 input signal

41.3.1.2 List of Pins for PORT02 and PORT03

Table 41.3-2 lists the internal pins for PORT02 and PORT03.

Table 41.3-2 List of Internal Pins (PORT02, PORT03)

Pin Name	I/O	Function
PORT02 I/O Buffer (from/to PAD)		
P02_DO[7:0]	Output	P02 I/O buffer output signal
P02_OE_N[7:0]	Output	P02 I/O buffer output enable signal
P02_DI[7:0]	Input	P02 I/O buffer input signal
P02_IE[7:0]	Output	P02 I/O buffer input enable signal
P02_DRV1[7:0]	Output	P02 I/O buffer drive strength switching signal 1
P02_DRV2[7:0]	Output	P02 I/O buffer drive strength switching signal 2
P02_PE_N[7:0]	Output	P02 I/O buffer pull-up/down enable signal
P02_PSEL[7:0]	Output	P02 I/O buffer pull-up/down switching signal
P02_SR[7:0]	Output	P02 I/O buffer slew rate switching signal
PORT02 Peripheral Pin Function		
P02_PF2_DI[7:0]	Output	P02 multiplexed function 2 input signal
P02_PF3_DI[7:0]	Output	P02 multiplexed function 3 input signal
PORT03 I/O Buffer (from/to PAD)		
P03_DO[15:0]	Output	P03 I/O buffer output signal
P03_OE_N[15:0]	Output	P03 I/O buffer output enable signal
P03_DI[15:0]	Input	P03 I/O buffer input signal
P03_IE[15:0]	Output	P03 I/O buffer input enable signal
P03_DRV1[15:0]	Output	P03 I/O buffer drive strength switching signal 1
P03_DRV2[15:0]	Output	P03 I/O buffer drive strength switching signal 2
P03_PE_N[15:0]	Output	P03 I/O buffer pull-up/down enable signal
P03_PSEL[15:0]	Output	P03 I/O buffer pull-up/down switching signal
P03_SR[15:0]	Output	P03 I/O buffer slew rate switching signal
PORT03 Peripheral Pin Function		
P03_PF1_DO[15:0]	Input	P03 multiplexed function 1 output signal
P03_PF2_DO[15:0]	Input	P03 multiplexed function 2 output signal
P03_PF4_DO[15:0]	Input	P03 multiplexed function 4 output signal
P03_PF5_DO[15:0]	Input	P03 multiplexed function 5 output signal
P03_PF6_DO[15:0]	Input	P03 multiplexed function 6 output signal
P03_PF7_DO[15:0]	Input	P03 multiplexed function 7 output signal
P03_PF1_OE[15:0]	Input	P03 multiplexed function 1 output enable signal
P03_PF2_OE_N[15:0]	Input	P03 multiplexed function 2 output enable signal
P03_PF1_DI[15:0]	Output	P03 multiplexed function 1 input signal
P03_PF2_DI[15:0]	Output	P03 multiplexed function 2 input signal
P03_PF7_DI[15:0]	Output	P03 multiplexed function 7 input signal

41.3.1.3 List of Pins for PORT04 and PORT05

Table 41.3-3 lists the internal pins for PORT04 and PORT05.

Table 41.3-3 List of Internal Pins (PORT04, PORT05)

Pin Name	I/O	Function
PORT04 I/O Buffer (from/to PAD)		
P04_DO[7:0]	Output	P04 I/O buffer output signal
P04_OE_N[7:0]	Output	P04 I/O buffer output enable signal
P04_DI[7:0]	Input	P04 I/O buffer input signal
P04_IE[7:0]	Output	P04 I/O buffer input enable signal
P04_DRV1[7:0]	Output	P04 I/O buffer drive strength switching signal 1
P04_DRV2[7:0]	Output	P04 I/O buffer drive strength switching signal 2
P04_PE_N[7:0]	Output	P04 I/O buffer pull-up/down enable signal
P04_PSEL[7:0]	Output	P04 I/O buffer pull-up/down switching signal
P04_SR[7:0]	Output	P04 I/O buffer slew rate switching signal
PORT04 Peripheral Pin Function		
P04_PF1_DO[7:0]	Input	P04 multiplexed function 1 output signal
P04_PF4_DO[7:0]	Input	P04 multiplexed function 4 output signal
P04_PF1_OE[7:0]	Input	P04 multiplexed function 1 output enable signal
P04_PF1_DI[7:0]	Output	P04 multiplexed function 1 input signal
PORT05 I/O Buffer (from/to PAD)		
P05_DO[3:0]	Output	P05 I/O buffer output signal
P05_OE_N[3:0]	Output	P05 I/O buffer output enable signal
P05_DI[3:0]	Input	P05 I/O buffer input signal
P05_IE[3:0]	Output	P05 I/O buffer input enable signal
P05_DRV1[3:0]	Output	P05 I/O buffer drive strength switching signal 1
P05_DRV2[3:0]	Output	P05 I/O buffer drive strength switching signal 2
P05_PE_N[3:0]	Output	P05 I/O buffer pull-up/down enable signal
P05_PSEL[3:0]	Output	P05 I/O buffer pull-up/down switching signal
P05_SR[3:0]	Output	P05 I/O buffer slew rate switching signal
PORT05 Peripheral Pin Function		
P05_PF2_DO[3:0]	Input	P05 multiplexed function 2 output signal
P05_PF2_OE_N[3:0]	Input	P05 multiplexed function 2 output enable signal
P05_PF2_DI[3:0]	Output	P05 multiplexed function 2 input signal

41.3.1.4 List of Pins for PORT06 and PORT07

Table 41.3-4 lists the internal pins for PORT06 and PORT07.

Table 41.3-4 List of Internal Pins (PORT06, PORT07)

Pin Name	I/O	Function
PORT06 I/O Buffer (from/to PAD)		
P06_DO[11:0]	Output	P06 I/O buffer output signal
P06_OE_N[11:0]	Output	P06 I/O buffer output enable signal
P06_DI[11:0]	Input	P06 I/O buffer input signal
P06_IE[11:0]	Output	P06 I/O buffer input enable signal
P06_DRV1[11:0]	Output	P06 I/O buffer drive strength switching signal 1
P06_DRV2[11:0]	Output	P06 I/O buffer drive strength switching signal 2
P06_PE_N[11:0]	Output	P06 I/O buffer pull-up/down enable signal
P06_PSEL[11:0]	Output	P06 I/O buffer pull-up/down switching signal
P06_SR[11:0]	Output	P06 I/O buffer slew rate switching signal
PORT06 Peripheral Pin Function		
P06_PF5_DO[11:0]	Input	P06 multiplexed function 5 output signal
P06_PF6_DO[11:0]	Input	P06 multiplexed function 6 output signal
P06_PF7_DO[11:0]	Input	P06 multiplexed function 7 output signal
P06_PF7_DI[11:0]	Output	P06 multiplexed function 7 input signal
PORT07 I/O Buffer (from/to PAD)		
P07_DO[5:0]	Output	P07 I/O buffer output signal
P07_OE_N[5:0]	Output	P07 I/O buffer output enable signal
P07_DI[5:0]	Input	P07 I/O buffer input signal
P07_IE[5:0]	Output	P07 I/O buffer input enable signal
P07_DRV1[5:0]	Output	P07 I/O buffer drive strength switching signal 1
P07_DRV2[5:0]	Output	P07 I/O buffer drive strength switching signal 2
P07_PE_N[5:0]	Output	P07 I/O buffer pull-up/down enable signal
P07_PSEL[5:0]	Output	P07 I/O buffer pull-up/down switching signal
P07_SR[5:0]	Output	P07 I/O buffer slew rate switching signal
PORT07 Peripheral Pin Function		
P07_PF1_DO[5:0]	Input	P07 multiplexed function 1 output signal
P07_PF1_DI[5:0]	Output	P07 multiplexed function 1 input signal

41.3.1.5 List of Pins for PORT08 and PORT09

Table 41.3-5 lists the internal pins for PORT08 and PORT09.

Table 41.3-5 List of Internal Pins (PORT08, PORT09)

Pin Name	I/O	Function
PORT08 I/O Buffer (from/to PAD)		
P08_DO[7:0]	Output	P08 I/O buffer output signal
P08_OE_N[7:0]	Output	P08 I/O buffer output enable signal
P08_DI[7:0]	Input	P08 I/O buffer input signal
P08_IE[7:0]	Output	P08 I/O buffer input enable signal
P08_DRV1[7:0]	Output	P08 I/O buffer drive strength switching signal 1
P08_DRV2[7:0]	Output	P08 I/O buffer drive strength switching signal 2
P08_PE_N[7:0]	Output	P08 I/O buffer pull-up/down enable signal
P08_PSEL[7:0]	Output	P08 I/O buffer pull-up/down switching signal
P08_SR[7:0]	Output	P08 I/O buffer slew rate switching signal
P08_01_IE1	Output	P08[1] I/O buffer returned clock input enable signal
PORT08 Peripheral Pin Function		
P08_PF1_DO[7:0]	Input	P08 multiplexed function 1 output signal
P08_PF2_DO[7:0]	Input	P08 multiplexed function 2 output signal
P08_PF1_OE_N[7:0]	Input	P08 multiplexed function 1 output enable signal
P08_PF1_DI[7:0]	Output	P08 multiplexed function 1 input signal
PORT09 I/O Buffer (from/to PAD)		
P09_DO[7:0]	Output	P09 I/O buffer output signal
P09_OE_N[7:0]	Output	P09 I/O buffer output enable signal
P09_DI[7:0]	Input	P09 I/O buffer input signal
P09_IE[7:0]	Output	P09 I/O buffer input enable signal
P09_DRV1[7:0]	Output	P09 I/O buffer drive strength switching signal 1
P09_DRV2[7:0]	Output	P09 I/O buffer drive strength switching signal 2
P09_PE_N[7:0]	Output	P09 I/O buffer pull-up/down enable signal
P09_PSEL[7:0]	Output	P09 I/O buffer pull-up/down switching signal
P09_SR[7:0]	Output	P09 I/O buffer slew rate switching signal
P09_01_IE1	Output	P09[1] I/O buffer returned clock input enable signal
PORT09 Peripheral Pin Function		
P09_PF1_DO[7:0]	Input	P09 multiplexed function 1 output signal
P09_PF1_OE_N[7:0]	Input	P09 multiplexed function 1 output enable signal
P09_PF1_DI[7:0]	Output	P09 multiplexed function 1 input signal
P09_PF2_DI[7:0]	Output	P09 multiplexed function 2 input signal

41.3.1.6 List of Pins for PORT10 and PORT11

Table 41.3-6 lists the internal pins for PORT10 and PORT11.

Table 41.3-6 List of Internal Pins (PORT10, PORT11)

Pin Name	I/O	Function
PORT10 I/O Buffer (from/to PAD)		
P10_DO[8:0]	Output	P10 I/O buffer output signal
P10_OE_N[8:0]	Output	P10 I/O buffer output enable signal
P10_DI[8:0]	Input	P10 I/O buffer input signal
P10_IE[8:0]	Output	P10 I/O buffer input enable signal
P10_DRV1[8:0]	Output	P10 I/O buffer drive strength switching signal 1
P10_DRV2[8:0]	Output	P10 I/O buffer drive strength switching signal 2
P10_PE_N[8:0]	Output	P10 I/O buffer pull-up/down enable signal
P10_PSEL[8:0]	Output	P10 I/O buffer pull-up/down switching signal
P10_SR[8:0]	Output	P10 I/O buffer slew rate switching signal
PORT10 Peripheral Pin Function		
P10_PF1_DO[8:0]	Input	P10 multiplexed function 1 output signal
P10_PF1_OE[8:0]	Input	P10 multiplexed function 1 output enable signal
P10_PF1_IE[8:0]	Input	P10 multiplexed function 1 input enable signal
P10_PF1_DI[8:0]	Output	P10 multiplexed function 1 input signal
P10_PF2_DI[8:0]	Output	P10 multiplexed function 2 input signal
PORT11 I/O Buffer (from/to PAD)		
P11_DO[8:0]	Output	P11 I/O buffer output signal
P11_OE_N[8:0]	Output	P11 I/O buffer output enable signal
P11_DI[8:0]	Input	P11 I/O buffer input signal
P11_IE[8:0]	Output	P11 I/O buffer input enable signal
P11_DRV1[8:0]	Output	P11 I/O buffer drive strength switching signal 1
P11_DRV2[8:0]	Output	P11 I/O buffer drive strength switching signal 2
P11_PE_N[8:0]	Output	P11 I/O buffer pull-up/down enable signal
P11_PSEL[8:0]	Output	P11 I/O buffer pull-up/down switching signal
P11_SR[8:0]	Output	P11 I/O buffer slew rate switching signal
PORT11 Peripheral Pin Function		
P11_PF1_DO[8:0]	Input	P11 multiplexed function 1 output signal
P11_PF1_OE[8:0]	Input	P11 multiplexed function 1 output enable signal
P11_PF1_IE[8:0]	Input	P11 multiplexed function 1 input enable signal
P11_PF1_DI[8:0]	Output	P11 multiplexed function 1 input signal
P11_PF2_DI[8:0]	Output	P11 multiplexed function 2 input signal

41.3.1.7 List of Pins for PORT12 and PORT13

Table 41.3-7 lists the internal pins for PORT12 and PORT13.

Table 41.3-7 List of Internal Pins (PORT12, PORT13)

Pin Name	I/O	Function
PORT12 I/O Buffer (from/to PAD)		
P12_DO[3:0]	Output	P12 I/O buffer output signal
P12_OE_N[3:0]	Output	P12 I/O buffer output enable signal
P12_DI[3:0]	Input	P12 I/O buffer input signal
P12_IE[3:0]	Output	P12 I/O buffer input enable signal
P12_DRV1[3:0]	Output	P12 I/O buffer drive strength switching signal 1
P12_DRV2[3:0]	Output	P12 I/O buffer drive strength switching signal 2
P12_PE_N[3:0]	Output	P12 I/O buffer pull-up/down enable signal
P12_PSEL[3:0]	Output	P12 I/O buffer pull-up/down switching signal
P12_SR[3:0]	Output	P12 I/O buffer slew rate switching signal
PORT12 Peripheral Pin Function		
P12_PF1_DO[3:0]	Input	P12 multiplexed function 1 output signal
P12_PF2_DI[3:0]	Output	P12 multiplexed function 2 input signal
PORT13 I/O Buffer (from/to PAD)		
P13_DO[11:0]	Output	P13 I/O buffer output signal
P13_OE_N[11:0]	Output	P13 I/O buffer output enable signal
P13_DI[11:0]	Input	P13 I/O buffer input signal
P13_IE[11:0]	Output	P13 I/O buffer input enable signal
P13_DRV1[11:0]	Output	P13 I/O buffer drive strength switching signal 1
P13_DRV2[11:0]	Output	P13 I/O buffer drive strength switching signal 2
P13_PE_N[11:0]	Output	P13 I/O buffer pull-up/down enable signal
P13_PSEL[11:0]	Output	P13 I/O buffer pull-up/down switching signal
P13_SR[11:0]	Output	P13 I/O buffer slew rate switching signal
PORT13 Peripheral Pin Function		
P13_PF3_DO[11:0]	Input	P13 multiplexed function 3 output signal
P13_PF4_DO[11:0]	Input	P13 multiplexed function 4 output signal
P13_PF2_DI[11:0]	Output	P13 multiplexed function 2 input signal
P13_PF3_DI[11:0]	Output	P13 multiplexed function 3 input signal

41.3.1.8 List of Pins for PORT14 and PORT15

Table 41.3-8 lists the internal pins for PORT14 and PORT15.

Table 41.3-8 List of Internal Pins (PORT14, PORT15)

Pin Name	I/O	Function
PORT14 I/O Buffer (from/to PAD)		
P14_DO[7:0]	Output	P14 I/O buffer output signal
P14_OE_N[7:0]	Output	P14 I/O buffer output enable signal
P14_DI[7:0]	Input	P14 I/O buffer input signal
P14_IE[7:0]	Output	P14 I/O buffer input enable signal
P14_DRV1[7:0]	Output	P14 I/O buffer drive strength switching signal 1
P14_DRV2[7:0]	Output	P14 I/O buffer drive strength switching signal 2
P14_PE_N[7:0]	Output	P14 I/O buffer pull-up/down enable signal
P14_PSEL[7:0]	Output	P14 I/O buffer pull-up/down switching signal
P14_SR[7:0]	Output	P14 I/O buffer slew rate switching signal
PORT14 Peripheral Pin Function		
P14_PF3_DO[7:0]	Input	P14 multiplexed function 3 output signal
P14_PF4_DO[7:0]	Input	P14 multiplexed function 4 output signal
P14_PF2_DI[7:0]	Output	P14 multiplexed function 2 input signal
P14_PF3_DI[7:0]	Output	P14 multiplexed function 3 input signal
PORT15 I/O Buffer (from/to PAD)		
P15_DO[15:0]	Output	P15 I/O buffer output signal
P15_OE_N[15:0]	Output	P15 I/O buffer output enable signal
P15_DI[15:0]	Input	P15 I/O buffer input signal
P15_IE[15:0]	Output	P15 I/O buffer input enable signal
P15_DRV1[15:0]	Output	P15 I/O buffer drive strength switching signal 1
P15_DRV2[15:0]	Output	P15 I/O buffer drive strength switching signal 2
P15_PE_N[15:0]	Output	P15 I/O buffer pull-up/down enable signal
P15_PSEL[15:0]	Output	P15 I/O buffer pull-up/down switching signal
P15_SR[15:0]	Output	P15 I/O buffer slew rate switching signal
PORT15 Peripheral Pin Function		
P15_PF1_DO[15:0]	Input	P15 multiplexed function 1 output signal
P15_PF2_DO[15:0]	Input	P15 multiplexed function 2 output signal
P15_PF4_DO[15:0]	Input	P15 multiplexed function 4 output signal
P15_PF5_DO[15:0]	Input	P15 multiplexed function 5 output signal
P15_PF6_DO[15:0]	Input	P15 multiplexed function 6 output signal
P15_PF7_DO[15:0]	Input	P15 multiplexed function 7 output signal
P15_PF1_DI[15:0]	Output	P15 multiplexed function 1 input signal

41.3.1.9 List of Pins for PORT16 and PORT17

Table 41.3-9 lists the internal pins for PORT16 and PORT17.

Table 41.3-9 List of Internal Pins (PORT16, PORT17)

Pin Name	I/O	Function
PORT16 I/O Buffer (from/to PAD)		
P16_DO[13:0]	Output	P16 I/O buffer output signal
P16_OE_N[13:0]	Output	P16 I/O buffer output enable signal
P16_DI[13:0]	Input	P16 I/O buffer input signal
P16_IE[13:0]	Output	P16 I/O buffer input enable signal
P16_DRV1[13:0]	Output	P16 I/O buffer drive strength switching signal 1
P16_DRV2[13:0]	Output	P16 I/O buffer drive strength switching signal 2
P16_PE_N[13:0]	Output	P16 I/O buffer pull-up/down enable signal
P16_PSEL[13:0]	Output	P16 I/O buffer pull-up/down switching signal
P16_SR[13:0]	Output	P16 I/O buffer slew rate switching signal
PORT16 Peripheral Pin Function		
P16_PF1_DO[13:0]	Input	P16 multiplexed function 1 output signal
P16_PF2_DO[13:0]	Input	P16 multiplexed function 2 output signal
P16_PF3_DO[13:0]	Input	P16 multiplexed function 3 output signal
P16_PF4_DO[13:0]	Input	P16 multiplexed function 4 output signal
P16_PF5_DO[13:0]	Input	P16 multiplexed function 5 output signal
P16_PF6_DO[13:0]	Input	P16 multiplexed function 6 output signal
P16_PF7_DO[13:0]	Input	P16 multiplexed function 7 output signal
P16_PF1_OE[13:0]	Input	P16 multiplexed function 1 output enable signal
P16_PF2_OE[13:0]	Input	P16 multiplexed function 2 output enable signal
P16_PF2_IE[13:0]	Input	P16 multiplexed function 2 input enable signal
P16_PF1_DI[13:0]	Output	P16 multiplexed function 1 input signal
P16_PF2_DI[13:0]	Output	P16 multiplexed function 2 input signal
PORT17 I/O Buffer (from/to PAD)		
P17_DO	Output	P17 I/O buffer output signal
P17_OE_N	Output	P17 I/O buffer output enable signal
P17_DI	Input	P17 I/O buffer input signal
P17_IE	Output	P17 I/O buffer input enable signal
P17_DRV1	Output	P17 I/O buffer drive strength switching signal 1
P17_DRV2	Output	P17 I/O buffer drive strength switching signal 2
P17_PE_N	Output	P17 I/O buffer pull-up/down enable signal
P17_PSEL	Output	P17 I/O buffer pull-up/down switching signal
P17_SR	Output	P17 I/O buffer slew rate switching signal
PORT17 Peripheral Pin Function		
P17_PF1_DO	Input	P17 multiplexed function 1 output signal
P17_PF2_DO	Input	P17 multiplexed function 2 output signal
P17_PF5_DO	Input	P17 multiplexed function 5 output signal
P17_PF6_DO	Input	P17 multiplexed function 6 output signal
P17_PF7_DO	Input	P17 multiplexed function 7 output signal

41.3.1.10 List of Pins for PORT20 and PORT21

Table 41.3-10 lists the internal pins for PORT20 and PORT21.

Table 41.3-10 List of Internal Pins (PORT20, PORT21)

Pin Name	I/O	Function
PORT20 I/O Buffer (from/to PAD)		
P20_DO[2:0]	Output	P20 I/O buffer output signal
P20_OE_N[2:0]	Output	P20 I/O buffer output enable signal
P20_DI[2:0]	Input	P20 I/O buffer input signal
P20_IE[2:0]	Output	P20 I/O buffer input enable signal
P20_DRV1[2:0]	Output	P20 I/O buffer drive strength switching signal 1
P20_DRV2[2:0]	Output	P20 I/O buffer drive strength switching signal 2
P20_PE_N[2:0]	Output	P20 I/O buffer pull-up/down enable signal
P20_PSEL[2:0]	Output	P20 I/O buffer pull-up/down switching signal
PORT20 Peripheral Pin Function		
P20_PF1_DO[2:0]	Input	P20 multiplexed function 1 output signal
P20_PF1_OE_N[2:0]	Input	P20 multiplexed function 1 output enable signal
P20_PF1_DI[2:0]	Output	P20 multiplexed function 1 input signal
PORT21 I/O Buffer (from/to PAD)		
P21_DO	Output	P21 I/O buffer output signal
P21_OE_N	Output	P21 I/O buffer output enable signal
P21_DI	Input	P21 I/O buffer input signal
P21_IE	Output	P21 I/O buffer input enable signal
P21_DRV1	Output	P21 I/O buffer drive strength switching signal 1
P21_DRV2	Output	P21 I/O buffer drive strength switching signal 2
P21_PE_N	Output	P21 I/O buffer pull-up/down enable signal
P21_PSEL	Output	P21 I/O buffer pull-up/down switching signal
P21_SR	Output	P21 I/O buffer slew rate switching signal

41.3.1.11 List of Dedicated Pin Control Pins

Table 41.3-11 lists the internal pins which control the dedicated pins.

Table 41.3-11 List of Internal Pins (Dedicated Pin Control)

Pin Name	I/O	Function
Exclusive PORT0 I/O Buffer (to PAD)		
PEX0_OE_N[5:0]	Output	Dedicated 0 I/O buffer output enable signal [5:0]
PEX0_OE_N[6]	Output	Dedicated 0 I/O buffer output enable signal [6]
PEX0_OE_N[15:7]	Output	Dedicated 0 I/O buffer output enable signal [15:7]
PEX0_IE[15:0]	Output	Dedicated 0 I/O buffer input enable signal
PEX0_DRV1[15:0]	Output	Dedicated 0 I/O buffer drive strength switching signal 1
PEX0_DRV2[15:0]	Output	Dedicated 0 I/O buffer drive strength switching signal 2
PEX0_PE_N[15:0]	Output	Dedicated 0 I/O buffer pull-up/down enable signal
PEX0_PSEL[15:0]	Output	Dedicated 0 I/O buffer pull-up/down switching signal
PEX0_SR[15:0]	Output	Dedicated 0 I/O buffer slew rate switching signal
Exclusive PORT0 Peripheral Pin Function		
PEX0_06_OE	Input	Dedicated 0 bit 6 I/O buffer output enable signal
Exclusive PORT1 I/O Buffer (to PAD)		
PEX1_OE_N[9:1]	Output	Dedicated 1 I/O buffer output enable signal
PEX1_IE[9:1]	Output	Dedicated 1 I/O buffer input enable signal
PEX1_DRV1[9:1]	Output	Dedicated 1 I/O buffer drive strength switching signal 1
PEX1_DRV2[9:1]	Output	Dedicated 1 I/O buffer drive strength switching signal 2
PEX1_PE_N[9:1]	Output	Dedicated 1 I/O buffer pull-up/down enable signal
PEX1_PSEL[9:1]	Output	Dedicated 1 I/O buffer pull-up/down switching signal
PEX1_SR[8:1]*1	Output	Dedicated 1 I/O buffer slew rate switching signal

Note 1. The external pin (RSTN) corresponding to PEX1[9] has no slew rate switching function, so the PEX1_SR[9] pin is not also present.

The following describes the internal pin functions of the PFC unit.

41.3.2 PORT00 to PORT21 I/O Buffer (from/to PAD) Control Signal

Pnn_DO[15:0]: PORTnn I/O buffer output signal

Pnn_OE_N[15:0]: PORTnn I/O buffer output enable signal

Pnn_OE_N[m] = 0: Enable output
Pnn_OE_N[m] = 1: Disable output

Pnn_DI[15:0]: PORTnn I/O buffer input signal

Pnn_IE[15:0]: PORTnn I/O buffer input enable signal

Pnn_IE[m] = 0: Disable input
Pnn_IE[m]=1: Enable input

Note: nn = 00 to 17, 20 to 21
m = 0 to 15

Pnn_DRV1[15:0]/ Pnn_DRV2[15:0]: PORTnn I/O buffer drive strength switching signal
The drive strength is switched as listed in the table below.

Table 41.3-12 I/O Buffer Drive Strength Switching

DRV2	DRV1	Drive Strength
0	0	X1
0	1	X2
1	0	X4
1	1	X6

Pnn_PE_N[15:0]/ Pnn_PSEL[15:0]: PORTnn I/O buffer pull-up/down control signal
The pull-up/down is switched as listed in the table below

Table 41.3-13 I/O Buffer Pull-Up/Down Control

PE_N	PSEL	Pull-Up/Down
1	x	No pull-up/down
0	0	Pull-down
0	1	Pull-up

Pnn_SR[15:0]: PORTnn I/O buffer slew rate switching signal

Pnn_SR[m] = 0: Fast slew
Pnn_SR[m] = 1: Slow slew

Note: x: Don't care
nn = 00 to 17, 20 to 21
m = 0 to 15

The IO buffer for the eternal pins NACLE. SD0CLK, and SD1FCLK has functionality for returning the output clock to the inside before the IO buffer. The returned clock is used to ease timing adjustment for the external interfaces of eMMC, SDI0, and SDI1.

The PFC controls enable for the returned clock by using the following signals.

P00_11_IE1: NACLE pin (MMCLK) I/O buffer returned clock (TDOUT) input enable signal

1 is output when the multiplexed function for bit 11 of PORT00 is MMCLK and the setting of the enable masking register (P00_EN_MSK) (described later) is for removing masking; otherwise, 0 is output.

P08_01_IE1: SD0CLK pin I/O buffer returned clock (TDOUT) input enable signal

1 is output when the multiplexed function for bit 1 of PORT08 is SD0CLK and the setting of the enable masking register (P08_EN_MSK) (described later) is for removing masking; otherwise, 0 is output.

P09_01_IE1: SD1FCLK pin I/O buffer returned clock (TDOUT) input enable signal

1 is output when the multiplexed function for bit 1 of PORT09 is SD1FCLK and the setting of the enable masking register (P09_EN_MSK) (described later) is for removing masking; otherwise, 0 is output.

Pnn_mm_IE1 = 0: Disable the returned clock (TDOUT) input
Pnn_mm_IE1 = 1: Enable the returned clock (TDOUT) input

Note: {nn, mm} = {00, 11}, {08, 01}, {09, 01}

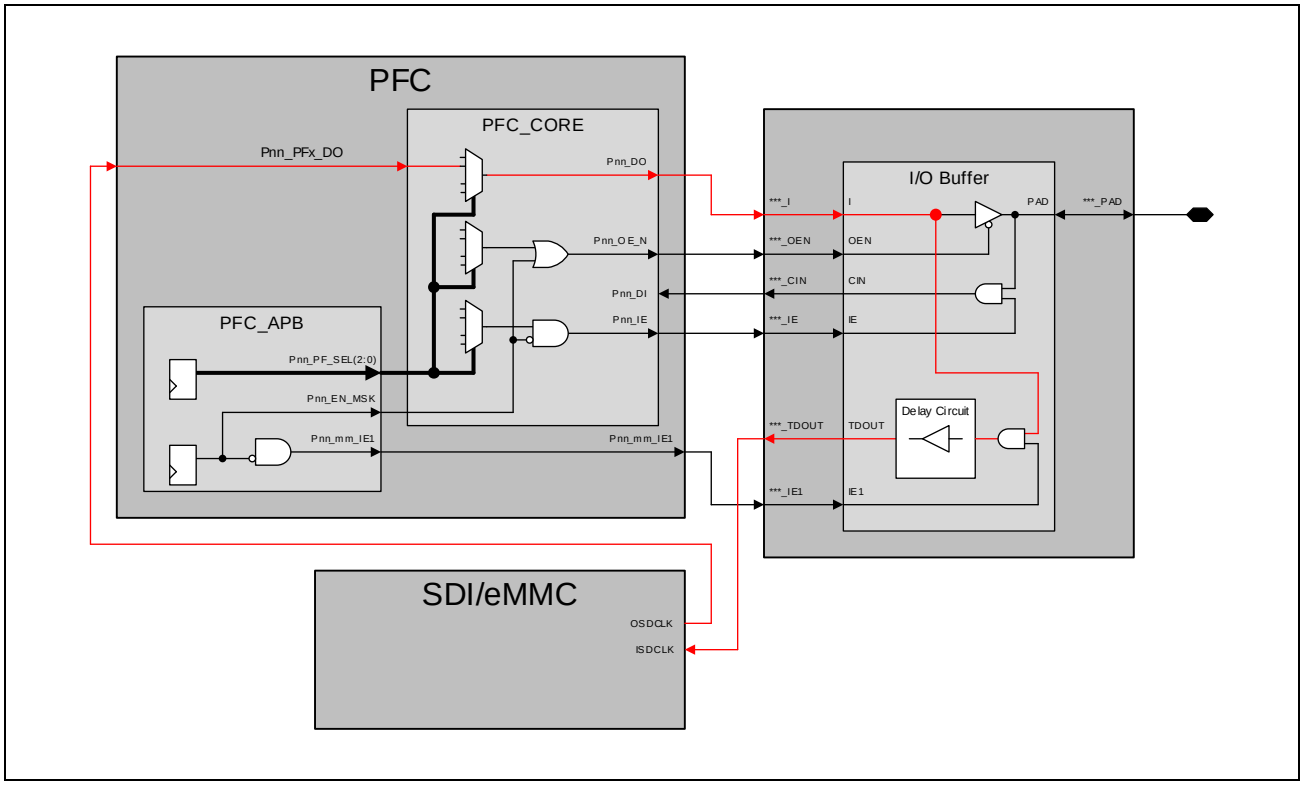


Figure 41.3-1 Schematic Block Diagram of the Returned Clock (TDOUT)

41.3.3 PORT00 to PORT20 Peripheral Pin Function Signals

Pnn_PFx_DO: Data output signal from the internal unit assigned to PORTnn multiplexed function x

Pnn_PFx_OE_N: Internal unit output enable signal assigned to PORTnn multiplexed function x (active low)

Pnn_PFx_OE: Internal unit output enable signal assigned to PORTnn multiplexed function x (active high)

Pnn_PFx_IE: Internal unit input enable signal assigned to PORTnn multiplexed function x

Pnn_PFx_DI: Data input signal to the internal unit assigned to PORTnn multiplexed function x

Note: nn = 00 to 17, 20
x = 1 to 7

NOTE

The Pnn_PFx_DI pin for which the multiplexed function is not selected has the same value as the initial value

For the initial values of the pins, see **Section 41.4.1, List of Registers**.

41.4 Register Descriptions

The following lists the registers of the PFC unit.

For the register base address (<PFC_S0_base>), see the section of Address Map.

41.4.1 List of Registers

41.4.1.1 List of Registers for PORT00 and PORT01

The table below lists the PFC registers for PORT00 and PORT01.

Table 41.4-1 List of PFC Registers (PORT00, PORT01) (1/2)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
PORT00 GPIO Registers 000h-00Ch				
000h	PORT00 GPIO output value control register	PFC_P00_GPIO_DO	0000_0000h	32
004h	PORT00 GPIO output control register	PFC_P00_GPIO_OE	0000_0000h	32
008h	PORT00 GPIO input control register	PFC_P00_GPIO_IE	0000_0000h	32
00Ch	Reserved	—	—	—
PORT00 Pin Function Control Registers 010h-03Ch				
010h	PORT00 function select register 0	PFC_P00_PFSEL0	0000_0000h	32
014h	PORT00 function select register 1	PFC_P00_PFSEL1	0000_0000h	32
018h	PORT00 function select register 2	PFC_P00_PFSEL2	0000_0000h	32
01Ch	PORT00 function select register 3	PFC_P00_PFSEL3	0000_0000h	32
020h	PORT00 input value monitor register	PFC_P00_DI_MON	—	32
024h	PORT00 pull-up/down control register	PFC_P00_PUPD	0556_5555h	32
028h	PORT00 drive strength control register	PFC_P00_DRV	0555_5555h	32
02Ch	PORT00 slew-rate control register	PFC_P00_SR	0000_3FFFh	32
030h	PORT00 input data mask register	PFC_P00_DI_MSK	0000_3FFFh	32
034h	PORT00 input/output enable mask register	PFC_P00_EN_MSK	0000_3FFFh	32
038h-03Ch	Reserved	—	—	—
PORT01 GPIO Registers 040h-04Ch				
040h	PORT01 GPIO output value control register	PFC_P01_GPIO_DO	0000_0000h	32
044h	PORT01 GPIO output control register	PFC_P01_GPIO_OE	0000_0000h	32
048h	PORT01 GPIO input control register	PFC_P01_GPIO_IE	0000_0000h	32
04Ch	Reserved	—	—	—
PORT01 Pin Function Control Registers 050h-07Ch				
050h	PORT01 function select register 0	PFC_P01_PFSEL0	0000_0000h	32
054h	PORT01 function select register 1	PFC_P01_PFSEL1	0000_0000h	32
058h	PORT01 function select register 2	PFC_P01_PFSEL2	0000_0000h	32
05Ch	PORT01 function select register 3	PFC_P01_PFSEL3	0000_0000h	32
060h	PORT01 input value monitor register	PFC_P01_DI_MON	—	32
064h	PORT01 pull-up/down control register	PFC_P01_PUPD	0555_0555h	32
068h	PORT01 drive strength control register	PFC_P01_DRV	5555_5555h	32
06Ch	PORT01 slew-rate control register	PFC_P01_SR	0000_FFFFh	32
070h	PORT01 input data mask register	PFC_P01_DI_MSK	0000_FFFFh	32

Table 41.4-1 List of PFC Registers (PORT00, PORT01) (2/2)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
074h	PORT01 input/output enable mask register	PFC_P01_EN_MSK	0000_FFFFh	32
078h-07Ch	Reserved	—	—	—

CAUTION

Access to the reserved area is prohibited.

41.4.1.2 List of Registers for PORT02 and PORT03

The table below lists the PFC registers for PORT02 and PORT03.

Table 41.4-2 List of PFC Registers (PORT02, PORT03)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
PORT02 GPIO Registers 080h-08Ch				
080h	PORT02 GPIO output value control register	PFC_P02_GPIO_DO	0000_0000h	32
084h	PORT02 GPIO output control register	PFC_P02_GPIO_OE	0000_0000h	32
088h	PORT02 GPIO input control register	PFC_P02_GPIO_IE	0000_0000h	32
08Ch	Reserved	—	—	—
PORT02 Pin Function Control Registers 090h-0BCh				
090h	PORT02 function select register 0	PFC_P02_PFSEL0	0000_0000h	32
094h	PORT02 function select register 1	PFC_P02_PFSEL1	0000_0000h	32
098h-09Ch	Reserved	—	—	—
0A0h	PORT02 input value monitor register	PFC_P02_DI_MON	—	32
0A4h	PORT02 pull-up/down control register	PFC_P02_PUPD	0000_5555h	32
0A8h	PORT02 drive strength control register	PFC_P02_DRV	0000_0000h	32
0Ach	PORT02 slew-rate control register	PFC_P02_SR	0000_00FFh	32
0B0h	PORT02 input data mask register	PFC_P02_DI_MSK	0000_00FFh	32
0B4h	PORT02 input/output enable mask register	PFC_P02_EN_MSK	0000_00FFh	32
0B8h-0BCh	Reserved	—	—	—
PORT03 GPIO Registers 0C0h-0CCh				
0C0h	PORT03 GPIO output value control register	PFC_P03_GPIO_DO	0000_0000h	32
0C4h	PORT03 GPIO output control register	PFC_P03_GPIO_OE	0000_0000h	32
0C8h	PORT03 GPIO input control register	PFC_P03_GPIO_IE	0000_0000h	32
0CCh	Reserved	—	—	—
PORT03 Pin Function Control Registers 0D0h-0FCh				
0D0h	PORT03 function select register 0	PFC_P03_PFSEL0	0000_0000h	32
0D4h	PORT03 function select register 1	PFC_P03_PFSEL1	0000_0000h	32
0D8h	PORT03 function select register 2	PFC_P03_PFSEL2	0000_0000h	32
0DCh	PORT03 function select register 3	PFC_P03_PFSEL3	0000_0000h	32
0E0h	PORT03 input value monitor register	PFC_P03_DI_MON	—	32
0E4h	PORT03 pull-up/down control register	PFC_P03_PUPD	0055_5555h	32
0E8h	PORT03 drive strength control register	PFC_P03_DRV	5555_5555h	32
0Ech	PORT03 slew-rate control register	PFC_P03_SR	0000_FFFFh	32
0F0h	PORT03 input data mask register	PFC_P03_DI_MSK	0000_FFFFh	32
0F4h	PORT03 input/output enable mask register	PFC_P03_EN_MSK	0000_FFFFh	32
0F8h-0FCh	Reserved	—	—	—

CAUTION

Access to the reserved area is prohibited.

41.4.1.3 List of Registers for PORT04 and PORT05

The table below lists the PFC registers for PORT04 and PORT05.

Table 41.4-3 List of PFC Registers (PORT04, PORT05)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
PORT04 GPIO Registers 100h-10Ch				
100h	PORT04 GPIO output value control register	PFC_P04_GPIO_DO	0000_0000h	32
104h	PORT04 GPIO output control register	PFC_P04_GPIO_OE	0000_0000h	32
108h	PORT04 GPIO input control register	PFC_P04_GPIO_IE	0000_0000h	32
10Ch	Reserved	—	—	—
PORT04 Pin Function Control Registers 110h-13Ch				
110h	PORT04 function Select register 0	PFC_P04_PFSEL0	0000_0000h	32
114h	PORT04 function Select register 1	PFC_P04_PFSEL1	0000_0000h	32
118h-11Ch	Reserved	—	—	—
120h	PORT04 input value monitor register	PFC_P04_DI_MON	—	32
124h	PORT04 pull-up/down control register	PFC_P04_PUPD	0000_0000h	32
128h	PORT04 drive strength control register	PFC_P04_DRV	0000_5555h	32
12Ch	PORT04 slew-rate control register	PFC_P04_SR	0000_00FFh	32
130h	PORT04 input data mask register	PFC_P04_DI_MSK	0000_00FFh	32
134h	PORT04 input/output enable mask register	PFC_P04_EN_MSK	0000_00FFh	32
138h-13Ch	Reserved	—	—	—
PORT05 GPIO Registers 140h-14Ch				
140h	PORT05 GPIO output value control register	PFC_P05_GPIO_DO	0000_0000h	32
144h	PORT05 GPIO output control register	PFC_P05_GPIO_OE	0000_0000h	32
148h	PORT05 GPIO input control register	PFC_P05_GPIO_IE	0000_0000h	32
14Ch	Reserved	—	—	—
PORT05 Pin Function Control Registers 150h-17Ch				
150h	PORT05 function select register 0	PFC_P05_PFSEL0	0000_0000h	32
154h-15Ch	Reserved	—	—	—
160h	PORT05 input value monitor register	PFC_P05_DI_MON	—	32
164h	PORT05 pull-up/down control register	PFC_P05_PUPD	0000_0055h	32
168h	PORT05 drive strength control register	PFC_P05_DRV	0000_0000h	32
16Ch	PORT05 slew-rate control register	PFC_P05_SR	0000_000Fh	32
170h	PORT05 input data mask register	PFC_P05_DI_MSK	0000_000Fh	32
174h	PORT05 input/output enable mask register	PFC_P05_EN_MSK	0000_000Fh	32
178h-17Ch	Reserved	—	—	—

CAUTION

Access to the reserved area is prohibited.

41.4.1.4 List of Registers for PORT06 and PORT07

The table below lists the PFC registers for PORT06 and PORT07.

Table 41.4-4 List of PFC Registers (PORT06, PORT07)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
PORT06 GPIO Registers 180h-18Ch				
180h	PORT06 GPIO output value control register	PFC_P06_GPIO_DO	0000_0000h	32
184h	PORT06 GPIO output control register	PFC_P06_GPIO_OE	0000_0000h	32
188h	PORT06 GPIO input control register	PFC_P06_GPIO_IE	0000_0000h	32
18Ch	Reserved	—	—	—
PORT06 Pin Function Control Registers 190h-1BCh				
190h	PORT06 function Select register 0	PFC_P06_PFSEL0	0000_0000h	32
194h	PORT06 function Select register 1	PFC_P06_PFSEL1	0000_0000h	32
198h	PORT06 function Select register 2	PFC_P06_PFSEL2	0000_0000h	32
19Ch	Reserved	—	—	—
1A0h	PORT06 input value monitor register	PFC_P06_DI_MON	—	32
1A4h	PORT06 pull-up/down control register	PFC_P06_PUPD	0055_5555h	32
1A8h	PORT06 drive strength control register	PFC_P06_DRV	0055_5555h	32
1Ach	PORT06 slew-rate control register	PFC_P06_SR	0000_0FFFh	32
1B0h	PORT06 input data mask register	PFC_P06_DI_MSK	0000_0FFFh	32
1B4h	PORT06 input/output enable mask register	PFC_P06_EN_MSK	0000_0FFFh	32
1B8h-1BCh	Reserved	—	—	—
PORT07 GPIO Registers 1C0h-1CCh				
1C0h	PORT07 GPIO output value control register	PFC_P07_GPIO_DO	0000_0000h	32
1C4h	PORT07 GPIO output control register	PFC_P07_GPIO_OE	0000_0000h	32
1C8h	PORT07 GPIO input control register	PFC_P07_GPIO_IE	0000_0000h	32
1CCh	Reserved	—	—	—
PORT07 Pin Function Control Registers 1D0h-1FCh				
1D0h	PORT07 function Select register 0	PFC_P07_PFSEL0	0000_0000h	32
1D4h	PORT07 function Select register 1	PFC_P07_PFSEL1	0000_0000h	32
1D8h-1DCh	Reserved	—	—	—
1E0h	PORT07 input value monitor register	PFC_P07_DI_MON	—	32
1E4h	PORT07 pull-up/down control register	PFC_P07_PUPD	0000_0005h	32
1E8h	PORT07 drive strength control register	PFC_P07_DRV	0000_0555h	32
1Ech	PORT07 slew-rate control register	PFC_P07_SR	0000_003Fh	32
1F0h	PORT07 input data mask register	PFC_P07_DI_MSK	0000_003Fh	32
1F4h	PORT07 input/output enable mask register	PFC_P07_EN_MSK	0000_003Fh	32
1F8h-1FCh	Reserved	—	—	—

CAUTION

Access to the reserved area is prohibited.

41.4.1.5 List of Registers for PORT08 and PORT09

The table below lists the PFC registers for PORT08 and PORT09.

Table 41.4-5 List of PFC Registers (PORT08, PORT09)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
PORT08 GPIO Registers 200h-20Ch				
200h	PORT08 GPIO output value control register	PFC_P08_GPIO_DO	0000_0000h	32
204h	PORT08 GPIO output control register	PFC_P08_GPIO_OE	0000_0000h	32
208h	PORT08 GPIO input control register	PFC_P08_GPIO_IE	0000_0000h	32
20Ch	Reserved	—	—	—
PORT08 Pin Function Control Registers 210h-23Ch				
210h	PORT08 function Select register 0	PFC_P08_PFSEL0	0000_0000h	32
214h	PORT08 function Select register 1	PFC_P08_PFSEL1	0000_0000h	32
218h-21Ch	Reserved	—	—	—
220h	PORT08 input value monitor register	PFC_P08_DI_MON	—	32
224h	PORT08 pull-up/down control register	PFC_P08_PUPD	0000_9555h	32
228h	PORT08 drive strength control register	PFC_P08_DRV	0000_5000h	32
22Ch	PORT08 slew-rate control register	PFC_P08_SR	0000_00FFh	32
230h	PORT08 input data mask register	PFC_P08_DI_MSK	0000_00FFh	32
234h	PORT08 input/output enable mask register	PFC_P08_EN_MSK	0000_00FFh	32
238h-23Ch	Reserved	—	—	—
PORT09 GPIO Registers 240h-24Ch				
240h	PORT09 GPIO output value control register	PFC_P09_GPIO_DO	0000_0000h	32
244h	PORT09 GPIO output control register	PFC_P09_GPIO_OE	0000_0000h	32
248h	PORT09 GPIO input control register	PFC_P09_GPIO_IE	0000_0000h	32
24Ch	Reserved	—	—	—
PORT09 Pin Function Control Registers 250h-27Ch				
250h	PORT09 function select register 0	PFC_P09_PFSEL0	0000_0000h	32
254h	PORT09 function select register 1	PFC_P09_PFSEL1	0000_0000h	32
258h-25Ch	Reserved	—	—	—
260h	PORT09 input value monitor register	PFC_P09_DI_MON	—	32
264h	PORT09 pull-up/down control register	PFC_P09_PUPD	0000_9555h	32
268h	PORT09 drive strength control register	PFC_P09_DRV	0000_5000h	32
26Ch	PORT09 slew-rate control register	PFC_P09_SR	0000_00FFh	32
270h	PORT09 input data mask register	PFC_P09_DI_MSK	0000_00FFh	32
274h	PORT09 input/output enable mask register	PFC_P09_EN_MSK	0000_00FFh	32
278h-27Ch	Reserved	—	—	—

CAUTION

Access to the reserved area is prohibited.

41.4.1.6 List of Registers for PORT10 and PORT11

The table below lists the PFC registers for PORT10 and PORT11.

Table 41.4-6 List of PFC Registers (PORT10, PORT11)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
PORT10 GPIO Registers 280h-28Ch				
280h	PORT10 GPIO output value control register	PFC_P10_GPIO_DO	0000_0000h	32
284h	PORT10 GPIO output control register	PFC_P10_GPIO_OE	0000_0000h	32
288h	PORT10 GPIO input control register	PFC_P10_GPIO_IE	0000_0000h	32
28Ch	Reserved	—	—	—
PORT10 Pin Function Control Registers 290h-2BCh				
290h	PORT10 function select register 0	PFC_P10_PFSEL0	0000_0000h	32
294h	PORT10 function select register 1	PFC_P10_PFSEL1	0000_0000h	32
298h	PORT10 function select register 2	PFC_P10_PFSEL2	0000_0000h	32
29Ch	Reserved	—	—	—
2A0h	PORT10 input value monitor register	PFC_P10_DI_MON	—	32
2A4h	PORT10 pull-up/down control register	PFC_P10_PUPD	0001_5110h	32
2A8h	PORT10 drive strength control register	PFC_P10_DRV	0001_5555h	32
2Ach	PORT10 slew-rate control register	PFC_P10_SR	0000_01FFh	32
2B0h	PORT10 input data mask register	PFC_P10_DI_MSK	0000_01FFh	32
2B4h	PORT10 input/output enable mask register	PFC_P10_EN_MSK	0000_01FFh	32
2B8h-2BCh	Reserved	—	—	—
PORT11 GPIO Registers 2C0h-2CCh				
2C0h	PORT11 GPIO output value control register	PFC_P11_GPIO_DO	0000_0000h	32
2C4h	PORT11 GPIO output control register	PFC_P11_GPIO_OE	0000_0000h	32
2C8h	PORT11 GPIO input control register	PFC_P11_GPIO_IE	0000_0000h	32
2CCh	Reserved	—	—	—
PORT11 Pin Function Control Registers 2D0h-2FCh				
2D0h	PORT11 function select register 0	PFC_P11_PFSEL0	0000_0000h	32
2D4h	PORT11 function select register 1	PFC_P11_PFSEL1	0000_0000h	32
2D8h	PORT11 function select register 2	PFC_P11_PFSEL2	0000_0000h	32
2DCh	Reserved	—	—	—
2E0h	PORT11 input value monitor register	PFC_P11_DI_MON	—	32
2E4h	PORT11 pull-up/down control register	PFC_P11_PUPD	0001_5110h	32
2E8h	PORT11 drive strength control register	PFC_P11_DRV	0001_5555h	32
2Ech	PORT11 slew-rate control register	PFC_P11_SR	0000_01FFh	32
2F0h	PORT11 input data mask register	PFC_P11_DI_MSK	0000_01FFh	32
2F4h	PORT11 input/output enable mask register	PFC_P11_EN_MSK	0000_01FFh	32
2F8h-2FCh	Reserved	—	—	—

CAUTION

Access to the reserved area is prohibited.

41.4.1.7 List of Registers for PORT12 and PORT13

The table below lists the PFC registers for PORT12 and PORT13.

Table 41.4-7 List of PFC Registers (PORT12, PORT13)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
PORT12 GPIO Registers 300h-30Ch				
300h	PORT12 GPIO output value control register	PFC_P12_GPIO_DO	0000_0000h	32
304h	PORT12 GPIO output control register	PFC_P12_GPIO_OE	0000_0000h	32
308h	PORT12 GPIO input control register	PFC_P12_GPIO_IE	0000_0000h	32
30Ch	Reserved	—	—	—
PORT12 Pin Function Control Registers 310h-33Ch				
310h	PORT12 function select register 0	PFC_P12_PFSEL0	0000_0000h	32
314h-31Ch	Reserved	—	—	—
320h	PORT12 input value monitor register	PFC_P12_DI_MON	—	32
324h	PORT12 pull-up/down control register	PFC_P12_PUPD	0000_0054h	32
328h	PORT12 drive strength control register	PFC_P12_DRV	0000_0055h	32
32Ch	PORT12 slew-rate control register	PFC_P12_SR	0000_000Fh	32
330h	PORT12 input data mask register	PFC_P12_DI_MSK	0000_000Fh	32
334h	PORT12 input/output enable mask register	PFC_P12_EN_MSK	0000_000Fh	32
338h-33Ch	Reserved	—	—	—
PORT13 GPIO Registers 340h-34Ch				
340h	PORT13 GPIO output value control register	PFC_P13_GPIO_DO	0000_0000h	32
344h	PORT13 GPIO output control register	PFC_P13_GPIO_OE	0000_0000h	32
348h	PORT13 GPIO input control register	PFC_P13_GPIO_IE	0000_0000h	32
34Ch	Reserved	—	—	—
PORT13 Pin Function Control Registers 350h-37Ch				
350h	PORT13 function select register 0	PFC_P13_PFSEL0	0000_0000h	32
354h	PORT13 function select register 1	PFC_P13_PFSEL1	0000_0000h	32
358h	PORT13 function select register 2	PFC_P13_PFSEL2	0000_0000h	32
35Ch	Reserved	—	—	—
360h	PORT13 input value monitor register	PFC_P13_DI_MON	—	32
364h	PORT13 pull-up/down control register	PFC_P13_PUPD	0055_0000h	32
368h	PORT13 drive strength control register	PFC_P13_DRV	0055_5555h	32
36Ch	PORT13 slew-rate control register	PFC_P13_SR	0000_0FFFh	32
370h	PORT13 input data mask register	PFC_P13_DI_MSK	0000_0FFFh	32
374h	PORT13 input/output enable mask register	PFC_P13_EN_MSK	0000_0FFFh	32
378h-37Ch	Reserved	—	—	—

CAUTION

Access to the reserved area is prohibited.

41.4.1.8 List of Registers for PORT14 and PORT15

The table below lists the PFC registers for PORT14 and PORT15.

Table 41.4-8 List of PFC Registers (PORT14, PORT15)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
PORT14 GPIO Registers 380h-38Ch				
380h	PORT14 GPIO output value control register	PFC_P14_GPIO_DO	0000_0000h	32
384h	PORT14 GPIO output control register	PFC_P14_GPIO_OE	0000_0000h	32
388h	PORT14 GPIO input control register	PFC_P14_GPIO_IE	0000_0000h	32
38Ch	Reserved	—	—	—
PORT14 Pin Function Control Registers 390h-3BCh				
390h	PORT14 function select register 0	PFC_P14_PFSEL0	0000_0000h	32
394h	PORT14 function select register 1	PFC_P14_PFSEL1	0000_0000h	32
398h-39Ch	Reserved	—	—	—
3A0h	PORT14 input value monitor register	PFC_P14_DI_MON	—	32
3A4h	PORT14 pull-up/down control register	PFC_P14_PUPD	0000_1111h	32
3A8h	PORT14 drive strength control register	PFC_P14_DRV	0000_5555h	32
3Ach	PORT14 slew-rate control register	PFC_P14_SR	0000_00FFh	32
3B0h	PORT14 input data mask register	PFC_P14_DI_MSK	0000_00FFh	32
3B4h	PORT14 input/output enable mask register	PFC_P14_EN_MSK	0000_00FFh	32
3B8h-3BCh	Reserved	—	—	—
PORT15 GPIO Registers 3C0h-3CCh				
3C0h	PORT15 GPIO output value control register	PFC_P15_GPIO_DO	0000_0000h	32
3C4h	PORT15 GPIO output control register	PFC_P15_GPIO_OE	0000_0000h	32
3C8h	PORT15 GPIO input control register	PFC_P15_GPIO_IE	0000_0000h	32
3CCh	Reserved	—	—	—
PORT15 Pin Function Control Registers 3D0h-3FCh				
3D0h	PORT15 function select register 0	PFC_P15_PFSEL0	0000_0000h	32
3D4h	PORT15 function select register 1	PFC_P15_PFSEL1	0000_0000h	32
3D8h	PORT15 function select register 2	PFC_P15_PFSEL2	0000_0000h	32
3DCh	PORT15 function select register 3	PFC_P15_PFSEL3	0000_0000h	32
3E0h	PORT15 input value monitor register	PFC_P15_DI_MON	—	32
3E4h	PORT15 pull-up/down control register	PFC_P15_PUPD	5555_5555h	32
3E8h	PORT15 drive strength control register	PFC_P15_DRV	5555_5555h	32
3Ech	PORT15 slew-rate control register	PFC_P15_SR	0000_FFFFh	32
3F0h	PORT15 input data mask register	PFC_P15_DI_MSK	0000_FFFFh	32
3F4h	PORT15 input/output enable mask register	PFC_P15_EN_MSK	0000_FFFFh	32
3F8h-3FCh	Reserved	—	—	—

CAUTION

Access to the reserved area is prohibited.

41.4.1.9 List of Registers for PORT16 and PORT17

The table below lists the PFC registers for PORT16 and PORT17.

Table 41.4-9 List of PFC Registers (PORT16, PORT17)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
PORT16 GPIO Registers 400h-40Ch				
400h	PORT16 GPIO output value control register	PFC_P16_GPIO_DO	0000_0000h	32
404h	PORT16 GPIO output control register	PFC_P16_GPIO_OE	0000_0000h	32
408h	PORT16 GPIO input control register	PFC_P16_GPIO_IE	0000_0000h	32
40Ch	Reserved	—	—	—
PORT16 Pin Function Control Registers 410h-43Ch				
410h	PORT16 function select register 0	PFC_P16_PFSEL0	0000_0000h	32
414h	PORT16 function select register 1	PFC_P16_PFSEL1	0000_0000h	32
418h	PORT16 function select register 2	PFC_P16_PFSEL2	0000_0000h	32
41Ch	PORT16 function select register 3	PFC_P16_PFSEL3	0000_0000h	32
420h	PORT16 input value monitor register	PFC_P16_DI_MON	—	32
424h	PORT16 pull-up/down control register	PFC_P16_PUPD	0555_5555h	32
428h	PORT16 drive strength control register	PFC_P16_DRV	0545_5555h	32
42Ch	PORT16 slew-rate control register	PFC_P16_SR	0000_3FFFh	32
430h	PORT16 input data mask register	PFC_P16_DI_MSK	0000_3FFFh	32
434h	PORT16 input/output enable mask register	PFC_P16_EN_MSK	0000_3FFFh	32
438h-43Ch	Reserved	—	—	—
PORT17 GPIO Registers 440h-44Ch				
440h	PORT17 GPIO output value control register	PFC_P17_GPIO_DO	0000_0000h	32
444h	PORT17 GPIO output control register	PFC_P17_GPIO_OE	0000_0000h	32
448h	PORT17 GPIO input control register	PFC_P17_GPIO_IE	0000_0000h	32
44Ch	Reserved	—	—	—
PORT17 Pin Function Control Registers 450h-47Ch				
450h	PORT17 function select register 0	PFC_P17_PFSEL0	0000_0000h	32
454h-45Ch	Reserved	—	—	—
460h	PORT17 input value monitor register	PFC_P17_DI_MON	—	32
464h	PORT17 pull-up/down control register	PFC_P17_PUPD	0000_0001h	32
468h	PORT17 drive strength control register	PFC_P17_DRV	0000_0001h	32
46Ch	PORT17 slew-rate control register	PFC_P17_SR	0000_0001h	32
470h	PORT17 input data mask register	PFC_P17_DI_MSK	0000_0001h	32
474h	PORT17 input/output enable mask register	PFC_P17_EN_MSK	0000_0001h	32
478h-47Ch	Reserved	—	—	—
Reserved 480h-4FCh				
480h-4FC	Reserved	—	—	—

CAUTION

Access to the reserved area is prohibited.

41.4.1.10 List of Registers for PORT20 and PORT21

The table below lists the PFC registers for PORT20 and PORT21.

Table 41.4-10 List of PFC Registers (PORT20, PORT21)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
PORT20 GPIO Registers 500h-50Ch				
500h	PORT20 GPIO output value control register	PFC_P20_GPIO_DO	0000_0000h	32
504h	PORT20 GPIO output control register	PFC_P20_GPIO_OE	0000_0000h	32
508h	PORT20 GPIO input control register	PFC_P20_GPIO_IE	0000_0000h	32
50Ch	Reserved	—	—	—
PORT20 Pin Function Control Registers 510h-53Ch				
510h	PORT20 function select register 0	PFC_P20_PFSEL0	0000_0000h	32
514h-51Ch	Reserved	—	—	—
520h	PORT20 input value monitor register	PFC_P20_DI_MON	—	32
524h	Reserved	—	—	—
528h	PORT20 drive strength control register	PFC_P20_DRV	0000_0000h	32
52Ch	Reserved	—	—	—
530h	PORT20 input data mask register	PFC_P20_DI_MSK	0000_0007h	32
534h	PORT20 input/output enable mask register	PFC_P20_EN_MSK	0000_0007h	32
538h-53Ch	Reserved	—	—	—
PORT21 GPIO Registers 540h-54Ch				
540h	PORT21 GPIO output value control register	PFC_P21_GPIO_DO	0000_0000h	32
544h	PORT21 GPIO output control register	PFC_P21_GPIO_OE	0000_0000h	32
548h	PORT21 GPIO input control register	PFC_P21_GPIO_IE	0000_0000h	32
54Ch	Reserved	—	—	—
PORT21 Pin Function Control Registers 550h-57Ch				
550h-55Ch	Reserved	—	—	—
560h	PORT21 input value monitor register	PFC_P21_DI_MON	—	32
564h	Reserved	—	—	—
568h	PORT21 drive strength control register	PFC_P21_DRV	0000_0001h	32
56Ch	PORT21 slew-rate control register	PFC_P21_SR	0000_0001h	32
570h-57Ch	Reserved	—	—	—

CAUTION

Access to the reserved area is prohibited.

41.4.1.11 List of Registers for Input Pin Switching and Dedicated Pins

Table 41.4-11 List of PFC registers (Input Pin Switching and Dedicated Pins)

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
Input Pin Function Control Registers 580h-58Ch				
580h	CSRXD input pin switching register	PFC_CSRXD_SEL	0000_0000h	32
588h-58Ch	Reserved	—	—	—
Exclusive Pin Function Control Registers 590h-59Ch				
590h	Dedicated drive strength control register 0	PFC_PEX0_DRV	1140_143Dh	32
594h	Dedicated slew-rate control register 0	PFC_PEX0_SR	0000_DFFFh	32
598h-59Ch	Reserved	—	—	—
External Interrupt Inversion Control Registers 5A0h-5BCh				
5A0h	External interrupt signal polarity invert control register 0	PFC_EXTINT_INV0	0000_0000h	32
5A4h	External interrupt signal polarity invert control register 1	PFC_EXTINT_INV1	0000_0000h	32
5A8h	External interrupt signal polarity invert control register 2	PFC_EXTINT_INV2	0000_0000h	32
5Ach	Reserved	—	—	—
5B0h	External interrupt signal mask control register 0	PFC_EXTINT_MSK0	0000_FFFFh	32
5B4h	External interrupt signal mask control register 1	PFC_EXTINT_MSK1	0000_FFFFh	32
5B8h	External interrupt signal mask control register 2	PFC_EXTINT_MSK2	0000_007Fh	32
5BCh	Reserved	—	—	—
Reserved 5C0h-7FCh				
5C0h-7FCh	Reserved	—	—	—

CAUTION

Access to the reserved area is prohibited.

41.4.2 Register Descriptions

The function description of each register is given below.

41.4.2.1 PORT00 GPIO Output Value Control Register (PFC_P00_GPIO_DO)

This register controls the output value of GPIO PORT00.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0000h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	DO_WE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DO[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-12 PFC_P00_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29 to 16	DO_WE[13:00]	Enables write to DO[13:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 0	DO[13:00]	Set the GPIO PORT00 bit[13:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.2 PORT00 GPIO Output Control Register (PFC_P00_GPIO_OE)

This register controls whether GPIO PORT00 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0004h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	OE_WE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	OE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-13 PFC_P00_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29 to 16	OE_WE[13:00]	Enables write to OE[13:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 0	OE[13:00]	Control the output of GPIO PORT00 bit[13:00]. 0b: Disable output. 1b: Enable output.

41.4.2.3 PORT00 GPIO Input Control Register (PFC_P00_GPIO_IE)

This register controls whether GPIO PORT00 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0008h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IE_WE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	IE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-14 PFC_P00_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29 to 16	IE_WE[13:00]	Enables write to IE[13:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 0	IE[13:00]	Control the input of GPIO PORT0 pin bit[13:00]. 0b: Disable input. 1b: Enable input.

41.4.2.4 PORT00 Function Select Register 0 (PFC_P00_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT00.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0010h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-15 PFC_P00_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT00 (refer to **Table 41.4-16**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-15 PFC_P00_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT00 (refer to **Table 41.4-16**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT00 (see **Table 41.4-16**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT00 (see **Table 41.4-16**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-16 Assignment list of PORT00 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO00[3]	NADAT3 (NAND)	MMDAT3 (eMMC)	—	—	—	—	—
PF02	GPIO00[2]	NADAT2 (NAND)	MMDAT2 (eMMC)	—	—	—	—	—
PF01	GPIO00[1]	NADAT1 (NAND)	MMDAT1 (eMMC)	—	—	—	—	—
PF00	GPIO00[0]	NADAT0 (NAND)	MMDAT0 (eMMC)	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.5 PORT00 Function Select Register 1 (PFC_P00_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT00.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0014h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-17 PFC_P00_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT00 (see **Table 41.4-18**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-17 PFC_P00_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT00 (see **Table 41.4-18**) 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT00 (see **Table 41.4-18**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT00 (see **Table 41.4-18**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-18 Assignment list of PORT00 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO00[7]	NADAT7 (NAND)	MMDAT7 (eMMC)	—	—	—	—	—
PF06	GPIO00[6]	NADAT6 (NAND)	MMDAT6 (eMMC)	—	—	—	—	—
PF05	GPIO00[5]	NADAT5 (NAND)	MMDAT5 (eMMC)	—	—	—	—	—
PF04	GPIO00[4]	NADAT4 (NAND)	MMDAT4 (eMMC)	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.6 PORT00 Function Select Register 2 (PFC_P00_PFSEL2)

This register controls function selection of the multi-purpose pin in PORT00.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0018h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE11			—	PF_WE10			—	PF_WE09			—	PF_WE08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF11			—	PF10			—	PF09			—	PF08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-19 PFC_P00_PFSEL2 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE11	Enables write to PF11. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE10	Enables write to PF10. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE09	Enables write to PF09. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE08	Enables write to PF08. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF11	Select the function of multi-purpose pin 11 bit in PORT00 (see **Table 41.4-20**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-19 PFC_P00_PFSEL2 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF10	Select the function of multi-purpose pin 10 bit in PORT00 (see **Table 41.4-20**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF09	Select the function of multi-purpose pin 09 bit in PORT00 (see **Table 41.4-20**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF08	Select the function of multi-purpose pin 08 bit in PORT00 (see **Table 41.4-20**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-20 Assignment list of PORT00 multifunction pin by PF11 to 08

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF11	GPIO00[11]	NACLE (NAND)	MMCLK (eMMC)	—	—	—	—	—
PF10	GPIO00[10]	NAWEN (NAND)	MMCMD (eMMC)	—	—	—	—	—
PF09	GPIO00[9]	NAREN (NAND)	—	—	—	—	—	—
PF08	GPIO00[8]	NACEN (NAND)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.7 PORT00 Function Select Register 3 (PFC_P00_PFSEL3)

This register controls function selection of the multi-purpose pin in PORT00.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 001Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	PF_WE13			—	PF_WE12		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	PF13			—	PF12		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-21 PFC_P00_PFSEL3 Register Contents

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b. The write value should always be 0b.
22 to 20	PF_WE13	Enables write to PF13. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE12	Enables write to PF12. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 7	—	Reserved. These bits are read as 0b. The write value should always be 0b.
6 to 4	PF13	Select the function of multi-purpose pin 13 bit in PORT00 (see **Table 41.4-22**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF12	Select the function of multi-purpose pin 12 bit in PORT00 (see **Table 41.4-22**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-22 Assignment list of PORT00 multifunction pin by PF13 to 12

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF13	GPIO00[13]	NARBN(NAND)	—	—	—	—	—	—
PF12	GPIO00[12]	NAALE(NAND)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.8 PORT00 Input Value Monitor Register (PFC_P00_DI_MON)

This register is a read-only register that monitors the input value of the PORT00 input pin (P00_DI).

Writing is ignored.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0020h

Initial Value: 0000_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DI[13:00]													
Initial Value	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-23 PFC_P00_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved. These bits are read as 0b.
13 to 0	DI[13:00]	The input value of PORT00 input pin bit[13:00].

41.4.2.9 PORT00 Pull-Up/Down Control Register (PFC_P00_PUPD)

This register controls pulling up and down of the PORT00 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0024h

Initial Value: 0556_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	PUPD13		PUPD12		PUPD11		PUPD10		PUPD09		PUPD08	
Initial Value	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	0
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-24 PFC_P00_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 0	PUPD[13:00]	Control PORT00 pin bit[13:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.10 PORT00 Drive Strength Control Register (PFC_P00_DRV)

This register controls the drive strength of the PORT00 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0028h

Initial Value: 0555_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	DRV13		DRV12		DRV11		DRV10		DRV09		DRV08	
Initial Value	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	0
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-25 PFC_P00_DRV Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 0	DRV[13:00]	Control the PORT00 pin bit[13:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.11 PORT00 Slew-rate Control Register (PFC_P00_SR)

This register controls the slew-rate of the PORT00 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 002Ch

Initial Value: 0000_3FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	SR_WE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	SR[13:00]													
Initial Value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-26 PFC_P00_SR Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29 to 16	SR_WE[13:00]	Enables write to SR[13:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 0	SR[13:00]	Set the PORT00 pin bit[13:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.12 PORT00 Input Data Mask Register (PFC_P00_DI_MSK)

This register controls masking of input data of the PORT00 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0030h

Initial Value: 0000_3FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	DI_MSK_WE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DI_MSK[13:00]													
Initial Value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-27 PFC_P00_DI_MSK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29 to 16	DI_MSK_WE[13:00]	Enables write to DI_MSK[13:00]. (n=00 to 13) Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 0	DI_MSK[13:00]	Set the PORT00 DI_MSK pin value bit[13:00]. (n=00 to 13) 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.13 PORT00 Input/Output Enable Mask Register (PFC_P00_EN_MSK)

This register controls masking of input/output enable for the PORT00 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0034h

Initial Value: 0000_3FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	EN_MSK_WE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	EN_MSK[13:00]													
Initial Value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-28 PFC_P00_EN_MSK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29 to 16	EN_MSK_WE[13:00]	Enables write to EN_MSK[13:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 0	EN_MSK[13:00]	Set the PORT00 EN_MSK pin bit[13:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.14 PORT01 GPIO Output Value Control Register (PFC_P01_GPIO_DO)

This register controls the output value of PORT01 GPIO.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0040h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DO_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DO[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-29 PFC_P01_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 16	DO_WE[15:00]	Enables write to DO[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	DO[15:00]	Set the GPIO PORT01 bit[15:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.15 PORT01 GPIO Output Control Register (PFC_P01_GPIO_OE)

This register controls whether GPIO PORT01 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0044h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OE_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-30 PFC_P01_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 16	OE_WE[15:00]	Enables write to OE[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	OE[15:00]	Control the output of GPIO PORT01 bit[15:00]. 0b: Disable output. 1b: Enable output.

41.4.2.16 PORT01 GPIO Input Control Register (PFC_P01_GPIO_IE)

This register controls whether GPIO PORT01 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0048h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IE_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-31 PFC_P01_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 16	IE_WE[15:00]	Enables write to IE[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	IE[15:00]	Control the input of GPIO PORT01 pin bit[15:00]. 0b: Disable input. 1b: Enable input.

41.4.2.17 PORT01 Function Select Register 0 (PFC_P01_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT01.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0050h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-32 PFC_P01_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT01 (see **Table 41.4-33**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-32 PFC_P01_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT01 (see **Table 41.4-33**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT01 (see **Table 41.4-33**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT01 (see **Table 41.4-33**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-33 Assignment list of PORT01 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO01[3]	PM3(PWM)	INEXINT11 (GIC)	—	—	—	—	—
PF02	GPIO01[2]	PM2(PWM)	INEXINT10 (GIC)	—	—	—	—	—
PF01	GPIO01[1]	PM1(PWM)	INEXINT9 (GIC)	—	—	—	—	—
PF00	GPIO01[0]	PM0(PWM)	INEXINT8 (GIC)	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.18 PORT01 Function Select Register 1 (PFC_P01_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT01.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0054h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-34 PFC_P01_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT01 (see **Table 41.4-35**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-34 PFC_P01_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT01 (see **Table 41.4-35**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT01 (see **Table 41.4-35**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT01 (see **Table 41.4-35**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-35 Assignment list of PORT01 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO01[7]	PM7(PWM)	INEXINT15 (GIC)	GMCLK1 (CPG)	—	—	—	—
PF06	GPIO01[6]	PM6(PWM)	INEXINT14 (GIC)	GMCLK0 (CPG)	—	—	—	SDTCS3 (ESI)
PF05	GPIO01[5]	PM5(PWM)	INEXINT13 (GIC)	GFPLS0 (GFT)	—	—	—	SDTCS2 (ESI)
PF04	GPIO01[4]	PM4(PWM)	INEXINT12 (GIC)	—	—	—	—	SDTCS1 (ESI)

Remarks: —: Setting prohibited

41.4.2.19 PORT01 Function Select Register 2 (PFC_P01_PFSEL2)

This register controls function selection of the multi-purpose pin in PORT01.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0058h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE11			—	PF_WE10			—	PF_WE09			—	PF_WE08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF11			—	PF10			—	PF09			—	PF08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-36 PFC_P01_PFSEL2 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE11	Enables write to PF11. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE10	Enables write to PF10. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE09	Enables write to PF09. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE08	Enables write to PF08. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF11	Select the function of multi-purpose pin 11 bit in PORT01 (see **Table 41.4-37**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-36 PFC_P01_PFSEL2 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF10	Select the function of multi-purpose pin 10 bit in PORT01 (see **Table 41.4-37**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF09	Select the function of multi-purpose pin 09 bit in PORT01 (see **Table 41.4-37**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF08	Select the function of multi-purpose pin 08 bit in PORT01 (see **Table 41.4-37**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-37 Assignment list of PORT01 multifunction pin by PF11 to 08

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF11	GPIO01[11]	PM11(PWM)	INEXINT19 (GIC)	—	—	—	—	—
PF10	GPIO01[10]	PM10(PWM)	INEXINT18 (GIC)	—	—	—	—	—
PF09	GPIO01[9]	PM9(PWM)	INEXINT17 (GIC)	—	—	—	—	—
PF08	GPIO01[8]	PM8(PWM)	INEXINT16 (GIC)	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.20 PORT01 Function Select Register 3 (PFC_P01_PFSEL3)

This register controls function selection of the multi-purpose pin in PORT01.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 005Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE15			—	PF_WE14			—	PF_WE13			—	PF_WE12		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF15			—	PF14			—	PF13			—	PF12		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-38 PFC_P01_PFSEL3 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE15	Enables write to PF15. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE14	Enables write to PF14. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE13	Enables write to PF13. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE12	Enables write to PF12. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF15	Select the function of multi-purpose pin 15 bit in PORT01 (see **Table 41.4-39**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-38 PFC_P01_PFSEL3 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF14	Select the function of multi-purpose pin 14 bit in PORT01 (see **Table 41.4-39**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF13	Select the function of multi-purpose pin 13 bit in PORT01 (see **Table 41.4-39**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF12	Select the function of multi-purpose pin 12 bit in PORT01 (see **Table 41.4-39**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-39 Assignment list of PORT01 multifunction pin by PF15 to 12

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF15	GPIO01[15]	PM15(PWM)	INEXINT23 (GIC)	GMCLK1 (CPG)	—	—	—	—
PF14	GPIO01[14]	PM14(PWM)	INEXINT22 (GIC)	GMCLK0 (CPG)	—	—	—	—
PF13	GPIO01[13]	PM13(PWM)	INEXINT21 (GIC)	GFPLS1 (GFT)	—	—	—	—
PF12	GPIO01[12]	PM12(PWM)	INEXINT20 (GIC)	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.21 PORT01 Input Value Monitor Register (PFC_P01_DI_MON)

This register is a read-only register that monitors the input value of the PORT01 input pin (P01_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0060h

Initial Value: 0000_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DI[15:00]															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-40 PFC_P01_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15 to 0	DI[15:00]	The input value of PORT01 input pin bit[15:00].

41.4.2.22 PORT01 Pull-Up/Down Control Register (PFC_P01_PUPD)

This register controls pulling up and down of the PORT01 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0064h

Initial Value: 0555_0555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPD15		PUPD14		PUPD13		PUPD12		PUPD11		PUPD10		PUPD09		PUPD08	
Initial Value	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-41 PFC_P01_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 0	PUPD[15:00]	Control PORT01 pin bit[15:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.23 PORT01 Drive Strength Control Register (PFC_P01_DRV)

This register controls the drive strength of the PORT01 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0068h

Initial Value: 5555_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DRV15		DRV14		DRV13		DRV12		DRV11		DRV10		DRV09		DRV08	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-42 PFC_P01_DRV Register Contents

Bit Position	Bit Name	Description
31 to 0	DRV[15:00]	Control the PORT01 pin bit[15:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.24 PORT01 Slew-rate Control Register (PFC_P01_SR)

This register controls the slew-rate of the PORT01 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 006Ch

Initial Value: 0000_FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SR_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SR[15:00]															
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-43 PFC_P01_SR Register Contents

Bit Position	Bit Name	Description
31 to 16	SR_WE[15:00]	Enables write to SR[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	SR[15:00]	Set the PORT01 pin bit[15:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.25 PORT01 Input Data Mask Register (PFC_P01_DI_MSK)

This register controls masking of input data of the PORT01 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0070h

Initial Value: 0000_FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DI_MSK_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DI_MSK[15:00]															
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-44 PFC_P01_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 16	DI_MSK_WE[15:00]	Enables write to DI_MSK[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	DI_MSK[15:00]	Set the PORT01 DI_MSK pin value bit[15:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.26 PORT01 Input/Output Enable Mask Register (PFC_P01_EN_MSK)

This register controls masking of input/output enable for the PORT01 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0074h

Initial Value: 0000_FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EN_MSK_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN_MSK[15:00]															
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-45 PFC_P01_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 16	EN_MSK_WE[15:00]	Enables write to EN_MSK[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	EN_MSK[15:00]	Set the PORT01 EN_MSK pin bit[15:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.27 PORT02 GPIO Output Value Control Register (PFC_P02_GPIO_DO)

This register controls the output value of GPIO PORT02.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0080h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DO_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DO[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-46 PFC_P02_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	DO_WE[07:00]	Enables write to DO[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	DO[07:00]	Set the GPIO PORT02 bit[07:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.28 PORT02 GPIO Output Control Register (PFC_P02_GPIO_OE)

This register controls whether GPIO PORT02 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0084h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	OE_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	OE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-47 PFC_P02_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	OE_WE[07:00]	Enables write to OE[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	OE[07:00]	Control the output of GPIO PORT02 bit[07:00]. 0b: Disable output. 1b: Enable output.

41.4.2.29 PORT02 GPIO Input Control Register (PFC_P02_GPIO_IE)

This register controls whether GPIO PORT02 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0088h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	IE_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-48 PFC_P02_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	IE_WE[07:00]	Enables write to IE[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	IE[07:00]	Control the input of GPIO PORT02 pin bit[07:00]. 0b: Disable input. 1b: Enable input.

41.4.2.30 PORT02 Function Select Register 0 (PFC_P02_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT02.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0090h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-49 PFC_P02_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT02 (see **Table 41.4-50**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-49 PFC_P02_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT02 (see **Table 41.4-50**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT02 (see **Table 41.4-50**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT02 (see **Table 41.4-50**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-50 Assignment list of PORT02 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF3	GPIO02[3]	—	INEXINT3 (GIC)	—	—	—	—	—
PF2	GPIO02[2]	—	INEXINT2 (GIC)	—	—	—	—	—
PF1	GPIO02[1]	—	INEXINT1 (GIC)	—	—	—	—	—
PF0	GPIO02[0]	—	INEXINT0 (GIC)	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.31 PORT02 Function Select Register 1 (PFC_P02_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT02.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0094h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-51 PFC_P02_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT02 (see **Table 41.4-52**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-51 PFC_P02_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT02 (see **Table 41.4-52**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT02 (see **Table 41.4-52**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT02 (see **Table 41.4-52**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-52 Assignment list of PORT02 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO02[7]	—	INEXINT7 (GIC)	—	—	—	—	—
PF06	GPIO02[6]	—	INEXINT6 (GIC)	—	—	—	—	—
PF05	GPIO02[5]	—	INEXINT5 (GIC)	—	—	—	—	—
PF04	GPIO02[4]	—	INEXINT4 (GIC)	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.32 PORT02 Input Value Monitor Register (PFC_P02_DI_MON)

This register is a read-only register that monitors the input value of the PORT02 input pin (P02_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00A0h

Initial Value: 0000_00xxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DI[07:00]							
Initial Value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-53 PFC_P02_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	DI[07:00]	The input value of PORT02 input pin bit[07:00].

41.4.2.33 PORT02 Pull-Up/Down Control Register (PFC_P02_PUPD)

This register controls pulling up and down of the PORT02 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00A4h

Initial Value: 0000_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-54 PFC_P02_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15 to 0	PUPD[07:00]	Control PORT02 pin bit[07:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.34 PORT02 Drive Strength Control Register (PFC_P02_DRV)

This register controls the drive strength of the PORT02 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00A8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-55 PFC_P02_DRV Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15 to 0	DRV[07:00]	Control the PORT02 pin bit[07:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.35 PORT02 Slew-rate Control Register (PFC_P02_SR)

This register controls the slew-rate of the PORT02 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00ACh

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SR_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SR[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-56 PFC_P02_SR Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	SR_WE[07:00]	Enables write to SR[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	SR[07:00]	Set the PORT02 pin bit[07:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.36 PORT02 Input Data Mask Register (PFC_P02_DI_MSK)

This register controls masking of input data of the PORT02 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00B0h

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DI_MSK_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DI_MSK[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-57 PFC_P02_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	DI_MSK_WE[07:00]	Enables write to DI_MSK[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	DI_MSK[07:00]	Set the PORT02 DI_MSK pin value bit[07:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.37 PORT02 Input/Output Enable Mask Register (PFC_P02_EN_MSK)

This register controls masking of input/output enable for the PORT02 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00B4h

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	EN_MSK_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	EN_MSK[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-58 PFC_P02_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	EN_MSK_WE[07:00]	Enables write to EN_MSK[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	EN_MSK[07:00]	Set the PORT02 EN_MSK pin bit[07:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.38 PORT03 GPIO Output Value Control Register (PFC_P03_GPIO_DO)

This register controls the output value of PORT03 GPIO.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00C0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DO_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DO[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-59 PFC_P03_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 16	DO_WE[15:00]	Enables write to DO[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	DO[15:00]	Set the GPIO PORT03 bit[15:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.39 PORT03 GPIO Output Control Register (PFC_P03_GPIO_OE)

This register controls whether GPIO PORT03 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00C4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OE_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-60 PFC_P03_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 16	OE_WE[15:00]	Enables write to OE[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	OE[15:00]	Control the output of GPIO PORT03 bit[15:00]. 0b: Disable output. 1b: Enable output.

41.4.2.40 PORT03 GPIO Input Control Register (PFC_P03_GPIO_IE)

This register controls whether GPIO PORT03 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00C8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IE_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-61 PFC_P03_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 16	IE_WE[15:00]	Enables write to IE[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	IE[15:00]	Control the input of GPIO PORT03 pin bit[15:00]. 0b: Disable input. 1b: Enable input.

41.4.2.41 PORT03 Function Select Register 0 (PFC_P03_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT03.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00D0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-62 PFC_P03_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT03 (see **Table 41.4-63**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-62 PFC_P03_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT03 (see **Table 41.4-63**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT03 (see **Table 41.4-63**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT03 (see **Table 41.4-63**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-63 Assignment list of PORT03 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO03[3]	CSCS0 (CSI0)	UARTS0N (UART0)	—	—	—	—	—
PF02	GPIO03[2]	CSSCLK0 (CSI0)	UACTS0N (UART0)	—	—	—	—	—
PF01	GPIO03[1]	CSRXD0 (CSI0)	UARX0 (UART0)	—	—	—	—	—
PF00	GPIO03[0]	CSTXD0 (CSI0)	UATX0 (UART0)	CSRXD0 (CSI0)	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.42 PORT03 Function Select Register 1 (PFC_P03_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT03.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00D4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-64 PFC_P03_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT03 (see **Table 41.4-65**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-64 PFC_P03_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT03 (see **Table 41.4-65**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT03 (see **Table 41.4-65**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT03 (see **Table 41.4-65**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-65 Assignment list of PORT03 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO03[7]	CSCS1 (CSI1)	UARTS1N (UART1)	—	TRDAT14 (CST)	—	—	—
PF06	GPIO03[6]	CSSCLK1 (CSI1)	UACTS1N (UART1)	—	TRDAT15 (CST)	—	—	—
PF05	GPIO03[5]	CSRXD1 (CSI1)	UARX1 (UART1)	—	—	—	—	—
PF04	GPIO03[4]	CSTXD1 (CSI1)	UATX1 (UART1)	CSRXD1 (CSI1)	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.43 PORT03 Function Select Register 2 (PFC_P03_PFSEL2)

This register controls function selection of the multi-purpose pin in PORT03.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00D8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE11			—	PF_WE10			—	PF_WE09			—	PF_WE08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF11			—	PF10			—	PF09			—	PF08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-66 PFC_P03_PFSEL2 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE11	Enables write to PF11. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE10	Enables write to PF10. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE09	Enables write to PF09. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE08	Enables write to PF08. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF11	Select the function of multi-purpose pin 11 bit in PORT03 (see **Table 41.4-67**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-66 PFC_P03_PFSEL2 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF10	Select the function of multi-purpose pin 10 bit in PORT03 (see **Table 41.4-67**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF09	Select the function of multi-purpose pin 09 bit in PORT03 (see **Table 41.4-67**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF08	Select the function of multi-purpose pin 08 bit in PORT03 (see **Table 41.4-67**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-67 Assignment list of PORT03 multifunction pin by PF11 to 08

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF11	GPIO03[11]	CSCS2 (CSI2)	I2SCL3 (IIC3)	—	TRDAT10 (CST)	—	—	—
PF10	GPIO03[10]	CSSCLK2 (CSI2)	I2SDA3 (IIC3)	—	TRDAT11 (CST)	—	—	—
PF09	GPIO03[9]	CSRXD2 (CSI2)	I2SCL2 (IIC2)	—	TRDAT12 (CST)	—	—	—
PF08	GPIO03[8]	CSTXD2 (CSI2)	I2SDA2 (IIC2)	CSRXD2 (CSI2)	TRDAT13 (CST)	—	—	—

Remarks: —: Setting prohibited

41.4.2.44 PORT03 Function Select Register 3 (PFC_P03_PFSEL3)

This register controls function selection of the multi-purpose pin in PORT03.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00DCh

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE15			—	PF_WE14			—	PF_WE13			—	PF_WE12		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF15			—	PF14			—	PF13			—	PF12		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-68 PFC_P03_PFSEL3 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE15	Enables write to PF15. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE14	Enables write to PF14. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE13	Enables write to PF13. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE12	Enables write to PF12. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF15	Select the function of multi-purpose pin 15 bit in PORT03 (see **Table 41.4-69**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-68 PFC_P03_PFSEL3 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF14	Select the function of multi-purpose pin 14 bit in PORT03 (see **Table 41.4-69**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF13	Select the function of multi-purpose pin 13 bit in PORT03 (see **Table 41.4-69**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF12	Select the function of multi-purpose pin 12 bit in PORT03 (see **Table 41.4-69**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-69 Assignment list of PORT03 multifunction pin by PF15 to 12

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF15	GPIO03[15]	CSCS3 (CSI3)	—	—	TRDAT6 (CST)	—	—	SDTCS0 (ESI)
PF14	GPIO03[14]	CSSCLK3 (CSI3)	—	—	TRDAT7 (CST)	—	—	SDTSCLK (ESI)
PF13	GPIO03[13]	CSRXD3 (CSI3)	—	—	TRDAT8 (CST)	—	—	SDTRXD (ESI)
PF12	GPIO03[12]	CSTXD3 (CSI3)	CSRXD3 (CSI3)	—	TRDAT9 (CST)	—	—	SDTTXD (ESI)

Remarks: —: Setting prohibited

41.4.2.45 PORT03 Input Value Monitor Register (PFC_P03_DI_MON)

This register is a read-only register that monitors the input value of the PORT03 input pin (P03_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00E0h

Initial Value: 0000_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DI[15:00]															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-70 PFC_P03_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15 to 0	DI[15:00]	The input value of PORT03 input pin bit[15:00].

41.4.2.46 PORT03 Pull-Up/Down Control Register (PFC_P03_PUPD)

This register controls pulling up and down of the PORT03 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00E4h

Initial Value: 0055_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPD15		PUPD14		PUPD13		PUPD12		PUPD11		PUPD10		PUPD09		PUPD08	
Initial Value	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-71 PFC_P03_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 0	PUPD[15:00]	Control PORT03 pin bit[15:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.47 PORT03 Drive Strength Control Register (PFC_P03_DRV)

This register controls the drive strength of the PORT03 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00E8h

Initial Value: 5555_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DRV15		DRV14		DRV13		DRV12		DRV11		DRV10		DRV09		DRV08	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-72 PFC_P03_DRV Register Contents

Bit Position	Bit Name	Description
31 to 0	DRV[15:00]	Control the PORT03 pin bit[15:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.48 PORT03 Slew-rate Control Register (PFC_P03_SR)

This register controls the slew-rate of the PORT03 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00ECh

Initial Value: 0000_FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SR_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SR[15:00]															
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-73 PFC_P03_SR Register Contents

Bit Position	Bit Name	Description
31 to 16	SR_WE[15:00]	Enables write to SR[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	SR[15:00]	Set the PORT03 pin bit[15:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.49 PORT03 Input Data Mask Register (PFC_P03_DI_MSK)

This register controls masking of input data of the PORT03 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00F0h

Initial Value: 0000_FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DI_MSK_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DI_MSK[15:00]															
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-74 PFC_P03_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 16	DI_MSK_WE[15:00]	Enables write to DI_MSK[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	DI_MSK[15:00]	Set the PORT03 DI_MSK pin value bit[15:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.50 PORT03 Input/Output Enable Mask Register (PFC_P03_EN_MSK)

This register controls masking of input/output enable for the PORT03 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00F4h

Initial Value: 0000_FFFFh

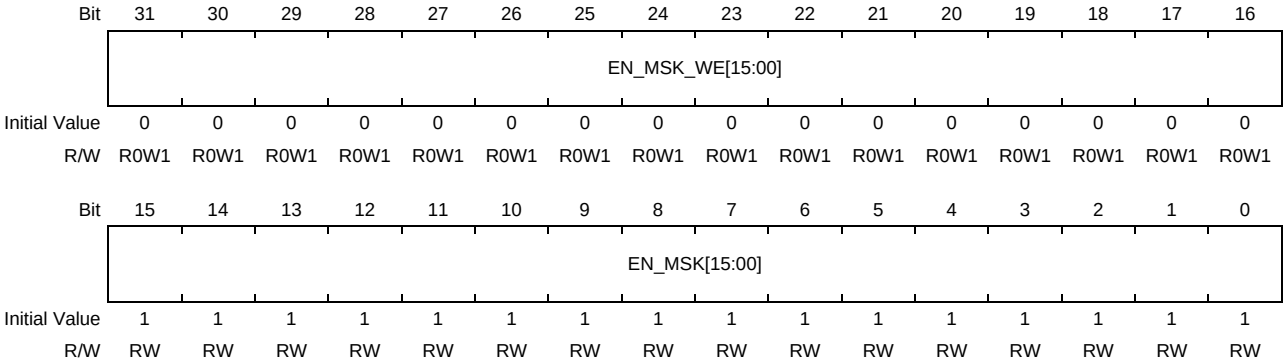


Table 41.4-75 PFC_P03_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 16	EN_MSK_WE[15:00]	Enables write to EN_MSK[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	EN_MSK[15:00]	Set the PORT03 EN_MSK pin bit[15:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.51 PORT04 GPIO Output Value Control Register (PFC_P04_GPIO_DO)

This register controls the output value of GPIO PORT04.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0100h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DO_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DO[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-76 PFC_P04_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	DO_WE[07:00]	Enables write to DO[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	DO[07:00]	Set the GPIO PORT04 bit[07:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.52 PORT04 GPIO Output Control Register (PFC_P04_GPIO_OE)

This register controls whether GPIO PORT04 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0104h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	OE_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	OE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-77 PFC_P04_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	OE_WE[07:00]	Enables write to OE[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	OE[07:00]	Control the output of GPIO PORT04 bit[07:00]. 0b: Disable output. 1b: Enable output.

41.4.2.53 PORT04 GPIO Input Control Register (PFC_P04_GPIO_IE)

This register controls whether GPIO PORT04 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0108h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	IE_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-78 PFC_P04_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	IE_WE[07:00]	Enables write to IE[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	IE[07:00]	Control the input of GPIO PORT04 pin bit[07:00]. 0b: Disable input. 1b: Enable input.

41.4.2.54 PORT04 Function Select Register 0 (PFC_P04_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT04.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0110h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-79 PFC_P04_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT04 (see **Table 41.4-80**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-79 PFC_P04_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT04 (see **Table 41.4-80**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT04 (see **Table 41.4-80**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT04 (see **Table 41.4-80**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-80 Assignment list of PORT04 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO04[3]	CSCS4 (CSI4)	—	—	TRDAT2 (CST)	—	—	—
PF02	GPIO04[2]	CSSCLK4 (CSI4)	—	—	TRDAT3 (CST)	—	—	—
PF01	GPIO04[1]	CSRXD4 (CSI4)	—	—	TRDAT4 (CST)	—	—	—
PF00	GPIO04[0]	CSTXD4 (CSI4)	CSRXD4 (CSI4)	—	TRDAT5 (CST)	—	—	—

Remarks: —: Setting prohibited

41.4.2.55 PORT04 Function Select Register 1 (PFC_P04_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT04.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0114h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-81 PFC_P04_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT04 (see **Table 41.4-82**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-81 PFC_P04_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT04 (see **Table 41.4-82**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT04 (see **Table 41.4-82**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT04 (see **Table 41.4-82**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-82 Assignment list of PORT04 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO04[7]	CSCS5 (CSI5)	—	—	TRCTL (CST)	—	—	—
PF06	GPIO04[6]	CSSCLK5 (CSI5)	—	—	TRCLK (CST)	—	—	—
PF05	GPIO04[5]	CSRXD5 (CSI5)	—	—	TRDAT0 (CST)	—	—	—
PF04	GPIO04[4]	CSTXD5 (CSI5)	CSRXD5 (CSI5)	—	TRDAT1 (CST)	—	—	—

Remarks: —: Setting prohibited

41.4.2.56 PORT04 Input Value Monitor Register (PFC_P04_DI_MON)

This register is a read-only register that monitors the input value of the PORT04 input pin (P04_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 00120h

Initial Value: 0000_00xxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DI[07:00]							
Initial Value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-83 PFC_P04_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	DI[07:00]	The input value of PORT04 input pin bit[07:00].

41.4.2.57 PORT04 Pull-Up/Down Control Register (PFC_P04_PUPD)

This register controls pulling up and down of the PORT04 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0124h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-84 PFC_P04_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15 to 0	PUPD[07:00]	Control PORT04 pin bit[07:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.58 PORT04 Drive Strength Control Register (PFC_P04_DRV)

This register controls the drive strength of the PORT04 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0128h

Initial Value: 0000_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-85 PFC_P04_DRV Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15 to 0	DRV[07:00]	Control the PORT04 pin bit[07:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.59 PORT04 Slew-rate Control Register (PFC_P04_SR)

This register controls the slew-rate of the PORT04 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 012Ch

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SR_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SR[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-86 PFC_P04_SR Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	SR_WE[07:00]	Enables write to SR[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	SR[07:00]	Set the PORT04 pin bit[07:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.60 PORT04 Input Data Mask Register (PFC_P04_DI_MSK)

This register controls masking of input data of the PORT04 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0130h

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DI_MSK_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DI_MSK[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-87 PFC_P04_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	DI_MSK_WE[07:00]	Enables write to DI_MSK[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	DI_MSK[07:00]	Set the PORT04 DI_MSK pin value bit[07:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.61 PORT04 Input/Output Enable Mask Register (PFC_P04_EN_MSK)

This register controls masking of input/output enable for the PORT04 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0134h

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	EN_MSK_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	EN_MSK[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-88 PFC_P04_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	EN_MSK_WE[07:00]	Enables write to EN_MSK[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	EN_MSK[07:00]	Set the PORT04 EN_MSK pin bit[07:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.62 PORT05 GPIO Output Value Control Register (PFC_P05_GPIO_DO)

This register controls the output value of GPIO PORT05.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0140h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	DO_WE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	DO[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 41.4-89 PFC_P05_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	DO_WE[03:00]	Enables write to DO[03:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3 to 0	DO[03:00]	Set the GPIO PORT05 bit[03:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.63 PORT05 GPIO Output Control Register (PFC_P05_GPIO_OE)

This register controls whether GPIO PORT05 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0144h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	OE_WE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	OE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 41.4-90 PFC_P05_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	OE_WE[03:00]	Enables write to of OE[03:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3 to 0	OE[03:00]	Control the output of GPIO PORT05 bit[03:00]. 0b: Disable output. 1b: Enable output.

41.4.2.64 PORT05 GPIO Input Control Register (PFC_P05_GPIO_IE)

This register controls whether GPIO PORT05 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0148h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	IE_WE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	IE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 41.4-91 PFC_P05_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	IE_WE[03:00]	Enables write to IE[03:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3 to 0	IE[03:00]	Control the input of GPIO PORT05 pin bit[03:00]. 0b: Disable input. 1b: Enable input.

41.4.2.65 PORT05 Function Select Register 0 (PFC_P05_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT05.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0150h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-92 PFC_P05_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT05 (see **Table 41.4-93**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-92 PFC_P05_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT05 (see **Table 41.4-93**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT05 (see **Table 41.4-93**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT05 (see **Table 41.4-93**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-93 Assignment list of PORT05 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO05[3]	—	I2SCL1 (IIC1)	—	—	—	—	—
PF02	GPIO05[2]	—	I2SDA1 (IIC1)	—	—	—	—	—
PF01	GPIO05[1]	—	I2SCL0 (IIC0)	—	—	—	—	—
PF00	GPIO05[0]	—	I2SDA0 (IIC0)	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.66 PORT05 Input Value Monitor Register (PFC_P05_DI_MON)

This register is a read-only register that monitors the input value of the PORT05 input pin (P02_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0160h

Initial Value: 0000_000xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	DI[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-94 PFC_P05_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 4	—	Reserved. These bits are read as 0b.
3 to 0	DI[03:00]	The input value of PORT05 input pin bit[03:00].

41.4.2.67 PORT05 Pull-Up/Down Control Register (PFC_P05_PUPD)

This register controls pulling up and down of the PORT05 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0164h

Initial Value: 0000_0055h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-95 PFC_P05_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	PUPD[03:00]	Control PORT05 pin bit[03:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.68 PORT05 Drive Strength Control Register (PFC_P05_DRV)

This register controls the drive strength of the PORT05 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0168h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DRV03		DRV02		DRV01		DRV00	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-96 PFC_P05_DRV Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	DRV[03:00]	Control the PORT05 pin bit[03:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.69 PORT05 Slew-rate Control Register (PFC_P05_SR)

This register controls the slew-rate of the PORT05 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 016Ch

Initial Value: 0000_000Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	SR_WE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	SR[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 41.4-97 PFC_P05_SR Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	SR_WE[03:00]	Enables write to SR[03:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3 to 0	SR[03:00]	Set the PORT05 pin bit[03:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.70 PORT05 Input Data Mask Register (PFC_P05_DI_MSK)

This register controls masking of input data of the PORT05 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0170h

Initial Value: 0000_000Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	DI_MSK_WE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	DI_MSK[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 41.4-98 PFC_P05_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	DI_MSK_WE[03:00]	Enables write to DI_MSK[03:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3 to 0	DI_MSK[03:00]	Set the PORT05 DI_MSK pin value bit[03:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.71 PORT05 Input/Output Enable Mask Register (PFC_P05_EN_MSK)

This register controls masking of input/output enable for the PORT05 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0174h

Initial Value: 0000_000Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	EN_MSK_WE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	EN_MSK[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 41.4-99 PFC_P05_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	EN_MSK_WE[03:00]	Enables write to EN_MSK[03:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3 to 0	EN_MSK[03:00]	Set the PORT05 EN_MSK pin bit[03:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.72 PORT06 GPIO Output Value Control Register (PFC_P06_GPIO_DO)

This register controls the output value of PORT06 GPIO.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0180h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	DO_WE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DO[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-100 PFC_P06_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 16	DO_WE[11:00]	Enables write to DO[11:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	DO[11:00]	Set the GPIO PORT06 bit[11:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.73 PORT06 GPIO Output Control Register (PFC_P06_GPIO_OE)

This register controls whether GPIO PORT06 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0184h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	OE_WE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	OE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-101 PFC_P06_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 16	OE_WE[11:00]	Enables write to OE[11:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	OE[11:00]	Control the output of GPIO PORT06 bit[11:00]. 0b: Disable output. 1b: Enable output.

41.4.2.74 PORT06 GPIO Input Control Register (PFC_P06_GPIO_IE)

This register controls whether GPIO PORT06 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0188h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	IE_WE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	IE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-102 PFC_P06_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 16	IE_WE[11:00]	Enables write to IE[11:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	IE[11:00]	Control the input of GPIO PORT06 pin bit[11:00]. 0b: Disable input. 1b: Enable input.

41.4.2.75 PORT06 Function Select Register 0 (PFC_P06_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT06.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0190h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-103 PFC_P06_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT06 (see **Table 41.4-104**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-103 PFC_P06_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT06 (see **Table 41.4-104**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT06 (see **Table 41.4-104**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT06 (see **Table 41.4-104**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-104 Assignment list of PORT06 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO06[3]	—	—	—	—	—	—	—
PF02	GPIO06[2]	—	—	—	—	—	—	—
PF01	GPIO06[1]	—	—	—	—	—	—	—
PF00	GPIO06[0]	—	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.76 PORT06 Function Select Register 1 (PFC_P06_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT06.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0194h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-105 PFC_P06_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT06 (see **Table 41.4-106**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-105 PFC_P06_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT06 (see **Table 41.4-106**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT06 (see **Table 41.4-106**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT06 (see **Table 41.4-106**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-106 Assignment list of PORT06 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO06[7]	—	—	—	—	—	—	—
PF06	GPIO06[6]	—	—	—	—	—	—	—
PF05	GPIO06[5]	—	—	—	—	—	—	—
PF04	GPIO06[4]	—	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.77 PORT06 Function Select Register 2 (PFC_P06_PFSEL2)

This register controls function selection of the multi-purpose pin in PORT06.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0198h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE11			—	PF_WE10			—	PF_WE09			—	PF_WE08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF11			—	PF10			—	PF09			—	PF08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-107 PFC_P06_PFSEL2 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE11	Enables write to PF11. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE10	Enables write to PF10. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE09	Enables write to PF09. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE08	Enables write to PF08. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF11	Select the function of multi-purpose pin 11 bit in PORT06 (see **Table 41.4-108**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-107 PFC_P06_PFSEL2 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF10	Select the function of multi-purpose pin 10 bit in PORT06 (see **Table 41.4-108**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF09	Select the function of multi-purpose pin 09 bit in PORT06 (see **Table 41.4-108**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF08	Select the function of multi-purpose pin 08 bit in PORT06 (see **Table 41.4-108**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-108 Assignment list of PORT06 multifunction pin by PF11 to 08

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF11	GPIO06[11]	—	—	—	—	—	—	—
PF10	GPIO06[10]	—	—	—	—	—	—	—
PF09	GPIO06[9]	—	—	—	—	—	—	—
PF08	GPIO06[8]	—	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.78 PORT06 Input Value Monitor Register (PFC_P06_DI_MON)

This register is a read-only register that monitors the input value of the PORT06 input pin (P06_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01A0h

Initial Value: 0000_0xxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DI[11:00]											
Initial Value	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-109 PFC_P06_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 12	—	Reserved. These bits are read as 0b.
11 to 0	DI[11:00]	The input value of PORT06 input pin bit[11:00].

41.4.2.79 PORT06 Pull-Up/Down Control Register (PFC_P06_PUPD)

This register controls pulling up and down of the PORT06 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01A4h

Initial Value: 0055_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	PUPD11		PUPD10		PUPD09		PUPD08	
Initial Value	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-110 PFC_P06_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 0	PUPD[11:00]	Control PORT06 pin bit[11:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.80 PORT06 Drive Strength Control Register (PFC_P06_DRV)

This register controls the drive strength of the PORT06 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01A8h

Initial Value: 0055_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DRV11		DRV10		DRV09		DRV08	
Initial Value	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-111 PFC_P06_DRV Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 0	DRV[11:00]	Control the PORT06 pin bit[11:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.81 PORT06 Slew-rate Control Register (PFC_P06_SR)

This register controls the slew-rate of the PORT06 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01ACh

Initial Value: 0000_0FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	SR_WE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SR[11:00]											
Initial Value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-112 PFC_P06_SR Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 16	SR_WE[11:00]	Enables write to SR[11:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	SR[11:00]	Set the PORT06 pin bit[11:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.82 PORT06 Input Data Mask Register (PFC_P06_DI_MSK)

This register controls masking of input data of the PORT06 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01B0h

Initial Value: 0000_0FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	DI_MSK_WE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DI_MSK[11:00]											
Initial Value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-113 PFC_P06_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 16	DI_MSK_WE[11:00]	Enables write to DI_MSK[11:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	DI_MSK[11:00]	Set the PORT06 DI_MSK pin value bit[11:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.83 PORT06 Input/Output Enable Mask Register (PFC_P06_EN_MSK)

This register controls masking of input/output enable for the PORT06 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01B4h

Initial Value: 0000_0FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	EN_MSK_WE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	EN_MSK[11:00]											
Initial Value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-114 PFC_P06_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 16	EN_MSK_WE[11:00]	Enables write to EN_MSK[11:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	EN_MSK[11:00]	Set the PORT06 EN_MSK pin bit[11:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.84 PORT07 GPIO Output Value Control Register (PFC_P07_GPIO_DO)

This register controls the output value of PORT07 GPIO.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01C0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	DO_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	DO[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 41.4-115 PFC_P07_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b. The write value should always be 0b.
21 to 16	DO_WE[05:00]	Enables write to DO[05:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b. The write value should always be 0b.
5 to 0	DO[05:00]	Set the GPIO PORT07 bit[05:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.85 PORT07 GPIO Output Control Register (PFC_P07_GPIO_OE)

This register controls whether GPIO PORT07 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01C4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	OE_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	OE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 41.4-116 PFC_P07_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b. The write value should always be 0b.
21 to 16	OE_WE[05:00]	Enables write to OE[05:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b. The write value should always be 0b.
5 to 0	OE[05:00]	Control the output of GPIO PORT07 bit[05:00]. 0b: Disable output. 1b: Enable output.

41.4.2.86 PORT07 GPIO Input Control Register (PFC_P07_GPIO_IE)

This register controls whether GPIO PORT07 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01C8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	IE_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	IE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 41.4-117 PFC_P07_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b. The write value should always be 0b.
21 to 16	IE_WE[05:00]	Enables write to IE[05:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b. The write value should always be 0b.
5 to 0	IE[05:00]	Control the input of GPIO PORT07 pin bit[05:00]. 0b: Disable input. 1b: Enable input.

41.4.2.87 PORT07 Function Select Register 0 (PFC_P07_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT07.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01D0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-118 PFC_P07_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT07 (see **Table 41.4-119**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-118 PFC_P07_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT07 (see **Table 41.4-119**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT07 (see **Table 41.4-119**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT07 (see **Table 41.4-119**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-119 Assignment list of PORT07 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO07[3]	AUDO (AUI)	—	—	—	—	—	—
PF02	GPIO07[2]	AUDI (AUI)	—	—	—	—	—	—
PF01	GPIO07[1]	AUBICK (AUI)	—	—	—	—	—	—
PF00	GPIO07[0]	AULRCK (AUI)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.88 PORT07 Function Select Register 1 (PFC_P07_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT07.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01D4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-120 PFC_P07_PFSEL1 Register Contents

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 7	—	Reserved. These bits are read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT07 (see **Table 41.4-121**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT07 (see **Table 41.4-121**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-121 Assignment list of PORT07 multifunction pin by PF05 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF05	GPIO07[5]	AUPLLCLK (AUI)	—	—	—	—	—	—
PF04	GPIO07[4]	AUMCLK (AUI)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.89 PORT07 Input Value Monitor Register (PFC_P07_DI_MON)

This register is a read-only register that monitors the input value of the PORT07 input pin (P07_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01E0h

Initial Value: 0000_00xxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	DI[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-122 PFC_P07_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 6	—	Reserved. These bits are read as 0b.
5 to 0	DI[05:00]	The input value of PORT07 input pin bit[05:00].

41.4.2.90 PORT07 Pull-Up/Down Control Register (PFC_P07_PUPD)

This register controls pulling up and down of the PORT07 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01E4h

Initial Value: 0000_0005h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-123 PFC_P07_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	PUPD[05:00]	Control PORT07 pin bit[05:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.91 PORT07 Drive Strength Control Register (PFC_P07_DRV)

This register controls the drive strength of the PORT07 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01E8h

Initial Value: 0000_0555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-124 PFC_P07_DRV Register Contents

Bit Position	Bit Name	Description
31 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	DRV[05:00]	Control the PORT07 pin bit[05:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.92 PORT07 Slew-rate Control Register (PFC_P07_SR)

This register controls the slew-rate of the PORT07 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01ECh

Initial Value: 0000_03Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	SR_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	SR[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 41.4-125 PFC_P07_SR Register Contents

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b. The write value should always be 0b.
21 to 16	SR_WE[05:00]	Enables write to SR[05:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b. The write value should always be 0b.
5 to 0	SR[05:00]	Set the PORT07 pin bit[05:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.93 PORT07 Input Data Mask Register (PFC_P07_DI_MSK)

This register controls masking of input data of the PORT07 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01F0h

Initial Value: 0000_003Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	DI_MSK_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	DI_MSK[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 41.4-126 PFC_P07_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b. The write value should always be 0b.
21 to 16	DI_MSK_WE[05:00]	Enables write to DI_MSK[05:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b. The write value should always be 0b.
5 to 0	DI_MSK[05:00]	Set the PORT07 DI_MSK pin value bit[05:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.94 PORT07 Input/Output Enable Mask Register (PFC_P07_EN_MSK)

This register controls masking of input/output enable for the PORT07 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 01F4h

Initial Value: 0000_003Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	EN_MSK_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	EN_MSK[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 41.4-127 PFC_P07_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b. The write value should always be 0b.
21 to 16	EN_MSK_WE[05:00]	Enables write to EN_MSK[05:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b. The write value should always be 0b.
5 to 0	EN_MSK[05:00]	Set the PORT07 EN_MSK pin bit[05:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.95 PORT08 GPIO Output Value Control Register (PFC_P08_GPIO_DO)

This register controls the output value of GPIO PORT08.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0200h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DO_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DO[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-128 PFC_P08_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	DO_WE[07:00]	Enables write to DO[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	DO[07:00]	Set the GPIO PORT08 bit[07:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.96 PORT08 GPIO Output Control Register (PFC_P08_GPIO_OE)

This register controls whether GPIO PORT08 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0204h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	OE_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	OE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-129 PFC_P08_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	OE_WE[07:00]	Enables write to OE[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	OE[07:00]	Control the output of GPIO PORT08 bit[07:00]. 0b: Disable output. 1b: Enable output.

41.4.2.97 PORT08 GPIO Input Control Register (PFC_P08_GPIO_IE)

This register controls whether GPIO PORT08 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0208h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	IE_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-130 PFC_P08_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	IE_WE[07:00]	Enables write to IE[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	IE[07:00]	Control the input of GPIO PORT08 pin bit[07:00]. 0b: Disable input. 1b: Enable input.

41.4.2.98 PORT08 Function Select Register 0 (PFC_P08_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT08.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0210h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-131 PFC_P08_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT08 (see **Table 41.4-132**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-131 PFC_P08_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT08 (see **Table 41.4-132**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT08 (see **Table 41.4-132**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT08 (see **Table 41.4-132**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-132 Assignment list of PORT08 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO08[3]	SD0DAT1 (SDI0)	—	—	—	—	—	—
PF02	GPIO08[2]	SD0DAT0 (SDI0)	—	—	—	—	—	—
PF01	GPIO08[1]	SD0CLK (SDI0)	—	—	—	—	—	—
PF00	GPIO08[0]	SD0CMD (SDI0)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.99 PORT08 Function Select Register 1 (PFC_P08_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT08.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0214h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-133 PFC_P08_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT08 (see **Table 41.4-134**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-133 PFC_P08_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT08 (see **Table 41.4-134**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT08 (see **Table 41.4-134**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT08 (see **Table 41.4-134**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-134 Assignment list of PORT08 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO08[7]	SD0CD (SDI0)	—	—	—	—	—	—
PF06	GPIO08[6]	SD0WP (SDI0)	—	—	—	—	—	—
PF05	GPIO08[5]	SD0DAT3 (SDI0)	—	—	—	—	—	—
PF04	GPIO08[4]	SD0DAT2 (SDI0)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.100 PORT08 Input Value Monitor Register (PFC_P08_DI_MON)

This register is a read-only register that monitors the input value of the PORT08 input pin (P08_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0220h

Initial Value: 0000_00xxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DI[07:00]							
Initial Value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-135 PFC_P08_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	DI[07:00]	The input value of PORT08 input pin bit[07:00].

41.4.2.101 PORT08 Pull-Up/Down Control Register (PFC_P08_PUPD)

This register controls pulling up and down of the PORT08 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0224h

Initial Value: 0000_9555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-136 PFC_P08_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15 to 0	PUPD[07:00]	Control PORT08 pin bit[07:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.102 PORT08 Drive Strength Control Register (PFC_P08_DRV)

This register controls the drive strength of the PORT08 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0228h

Initial Value: 0000_5000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-137 PFC_P08_DRV Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15 to 0	DRV[07:00]	Control the PORT08 pin bit[07:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.103 PORT08 Slew-rate Control Register (PFC_P08_SR)

This register controls the slew-rate of the PORT08 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 022Ch

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SR_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SR[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-138 PFC_P08_SR Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	SR_WE[07:00]	Enables write to SR[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	SR[07:00]	Set the PORT08 pin bit[07:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.104 PORT08 Input Data Mask Register (PFC_P08_DI_MSK)

This register controls masking of input data of the PORT08 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0230h

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DI_MSK_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DI_MSK[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-139 PFC_P08_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	DI_MSK_WE[07:00]	Enables write to DI_MSK[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	DI_MSK[07:00]	Set the PORT08 DI_MSK pin value bit[07:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.105 PORT08 Input/Output Enable Mask Register (PFC_P08_EN_MSK)

This register controls masking of input/output enable for the PORT08 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0234h

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	EN_MSK_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	EN_MSK[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-140 PFC_P08_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	EN_MSK_WE[07:00]	Enables write to EN_MSK[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	EN_MSK[07:00]	Set the PORT08 EN_MSK pin bit[07:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.106 PORT09 GPIO Output Value Control Register (PFC_P09_GPIO_DO)

This register controls the output value of GPIO PORT09.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0240h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DO_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DO[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-141 PFC_P09_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	DO_WE[07:00]	Enables write to DO[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	DO[07:00]	Set the GPIO PORT09 bit[07:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.107 PORT09 GPIO Output Control Register (PFC_P09_GPIO_OE)

This register controls whether GPIO PORT09 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0244h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	OE_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	OE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-142 PFC_P09_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	OE_WE[07:00]	Enables write to OE[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	OE[07:00]	Control the output of GPIO PORT09 bit[07:00]. 0b: Disable output. 1b: Enable output.

41.4.2.108 PORT09 GPIO Input Control Register (PFC_P09_GPIO_IE)

This register controls whether GPIO PORT09 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0248h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	IE_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-143 PFC_P09_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	IE_WE[07:00]	Enables write to IE[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	IE[07:00]	Control the input of GPIO PORT09 pin bit[07:00]. 0b: Disable input. 1b: Enable input.

41.4.2.109 PORT09 Function Select Register 0 (PFC_P09_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT09.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0250h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-144 PFC_P09_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT09 (see **Table 41.4-145**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-144 PFC_P09_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT09 (see **Table 41.4-145**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT09 (see **Table 41.4-145**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT09 (see **Table 41.4-145**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-145 Assignment list of PORT09 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO09[3]	SD1FDAT1 (SDI1)	—	—	—	—	—	—
PF02	GPIO09[2]	SD1FDAT0 (SDI1)	—	—	—	—	—	—
PF01	GPIO09[1]	SD1FCLK (SDI1)	—	—	—	—	—	—
PF00	GPIO09[0]	SD1FCMD (SDI1)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.110 PORT09 Function Select Register 1 (PFC_P09_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT09.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0254h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-146 PFC_P09_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT09 (see **Table 41.4-147**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-146 PFC_P09_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT09 (see **Table 41.4-147**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT09 (see **Table 41.4-147**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT09 (see **Table 41.4-147**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-147 Assignment list of PORT09 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO09[7]	SD1FCD (SDI1)	INEXINT25 (GIC)	—	—	—	—	—
PF06	GPIO09[6]	SD1FWP (SDI1)	INEXINT24 (GIC)	—	—	—	—	—
PF05	GPIO09[5]	SD1FDAT3 (SDI1)	—	—	—	—	—	—
PF04	GPIO09[4]	SD1FDAT2 (SDI1)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.111 PORT09 Input Value Monitor Register (PFC_P09_DI_MON)

This register is a read-only register that monitors the input value of the PORT09 input pin (P09_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0260h

Initial Value: 0000_00xxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DI[07:00]							
Initial Value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-148 PFC_P09_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	DI[07:00]	The input value of PORT09 input pin bit[07:00].

41.4.2.112 PORT09 Pull-Up/Down Control Register (PFC_P09_PUPD)

This register controls pulling up and down of the PORT09 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0264h

Initial Value: 0000_9555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-149 PFC_P09_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15 to 0	PUPD[07:00]	Control PORT09 pin bit[07:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.113 PORT09 Drive Strength Control Register (PFC_P09_DRV)

This register controls the drive strength of the PORT09 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0268h

Initial Value: 0000_5000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-150 PFC_P09_DRV Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15 to 0	DRV[07:00]	Control the PORT09 pin bit[07:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.114 PORT09 Slew-rate Control Register (PFC_P09_SR)

This register controls the slew-rate of the PORT09 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 026Ch

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SR_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SR[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-151 PFC_P09_SR Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	SR_WE[07:00]	Enables write to SR[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	SR[07:00]	Set the PORT09 pin bit[07:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.115 PORT09 Input Data Mask Register (PFC_P09_DI_MSK)

This register controls masking of input data of the PORT09 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0270h

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DI_MSK_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DI_MSK[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-152 PFC_P09_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	DI_MSK_WE[07:00]	Enables write to DI_MSK[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	DI_MSK[07:00]	Set the PORT09 DI_MSK pin value bit[07:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.116 PORT09 Input/Output Enable Mask Register (PFC_P09_EN_MSK)

This register controls masking of input/output enable for the PORT09 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0274h

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	EN_MSK_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	EN_MSK[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-153 PFC_P09_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	EN_MSK_WE[07:00]	Enables write to EN_MSK[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	EN_MSK[07:00]	Set the PORT09 EN_MSK pin bit[07:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.117 PORT10 GPIO Output Value Control Register (PFC_P10_GPIO_DO)

This register controls the output value of PORT10 GPIO.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0280h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DO_WE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DO[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-154 PFC_P10_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b. The write value should always be 0b.
24 to 16	DO_WE[08:00]	Enables write to DO[08:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	DO[08:00]	Set the GPIO PORT10 bit[08:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.118 PORT10 GPIO Output Control Register (PFC_P10_GPIO_OE)

This register controls whether GPIO PORT10 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0284h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	OE_WE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	OE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-155 PFC_P10_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b. The write value should always be 0b.
24 to 16	OE_WE[08:00]	Enables write to OE[08:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	OE[08:00]	Control the output of GPIO PORT10 bit[08:00]. 0b: Disable output. 1b: Enable output.

41.4.2.119 PORT10 GPIO Input Control Register (PFC_P10_GPIO_IE)

This register controls whether GPIO PORT10 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0288h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	IE_WE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	IE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-156 PFC_P10_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b. The write value should always be 0b.
24 to 16	IE_WE[08:00]	Enables write to IE[08:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	IE[08:00]	Control the input of GPIO PORT10 pin bit[08:00]. 0b: Disable input. 1b: Enable input.

41.4.2.120 PORT10 Function Select Register 0 (PFC_P10_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT10.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0290h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-157 PFC_P10_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT10 (see **Table 41.4-158**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-157 PFC_P10_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT10 (see **Table 41.4-158**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT10 (see **Table 41.4-158**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT10 (see **Table 41.4-158**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-158 Assignment list of PORT10 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO10[3]	IM0TXD (STG)	—	—	—			
PF02	GPIO10[2]	IM0CS (STG)	—	—	—			
PF01	GPIO10[1]	IM0HS (STG)	—	—	—			
PF00	GPIO10[0]	IM0VS (STG)	—	—	—			

Remarks: —: Setting prohibited

41.4.2.121 PORT10 Function Select Register 1 (PFC_P10_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT10.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0294h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-159 PFC_P10_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT10 (see **Table 41.4-160**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-159 PFC_P10_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT10 (see **Table 41.4-160**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT10 (see **Table 41.4-160**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT10 (see **Table 41.4-160**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-160 Assignment list of PORT10 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO10[7]	IM0SIG1 (STG)	INEXINT27 (GIC)	—	—	—	—	—
PF06	GPIO10[6]	IM0SIG0 (STG)	INEXINT26 (GIC)	—	—	—	—	—
PF05	GPIO10[5]	IM0SCLK (STG)	—	—	—	—	—	—
PF04	GPIO10[4]	IM0RXD (STG)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.122 PORT10 Function Select Register 2 (PFC_P10_PFSEL2)

This register controls function selection of the multi-purpose pin in PORT10.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0298h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	PF_WE08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	PF08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 41.4-161 PFC_P10_PFSEL2 Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b. The write value should always be 0b.
18 to 16	PF_WE08	Enables write to PF08. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b. The write value should always be 0b.
2 to 0	PF08	Select the function of multi-purpose pin 08 bit in PORT10 (see **Table 41.4-162**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-162 Assignment list of PORT10 multifunction pin by PF08

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF08	GPIO10[8]	IM0SIG2 (STG)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.123 PORT10 Input Value Monitor Register (PFC_P10_DI_MON)

This register is a read-only register that monitors the input value of the PORT10 input pin (P10_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02A0h

Initial Value: 0000_0xxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DI[08:00]								
Initial Value	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-163 PFC_P10_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 9	—	Reserved. These bits are read as 0b.
8 to 0	DI[08:00]	The input value of PORT10 input pin bit[08:00].

41.4.2.124 PORT10 Pull-Up/Down Control Register (PFC_P10_PUPD)

This register controls pulling up and down of the PORT10 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02A4h

Initial Value: 0001_5110h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PUPD08	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-164 PFC_P10_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 18	—	Reserved. These bits are read as 0b. The write value should always be 0b.
17 to 0	PUPD[08:00]	Control PORT10 pin bit[08:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.125 PORT10 Drive Strength Control Register (PFC_P10_DRV)

This register controls the drive strength of the PORT10 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02A8h

Initial Value: 0001_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV08	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-165 PFC_P10_DRV Register Contents

Bit Position	Bit Name	Description
31 to 18	—	Reserved. These bits are read as 0b. The write value should always be 0b.
17 to 0	DRV[08:00]	Control the PORT10 pin bit[08:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.126 PORT10 Slew-rate Control Register (PFC_P10_SR)

This register controls the slew-rate of the PORT10 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02ACh

Initial Value: 0000_01FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	SR_WE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SR[08:00]								
Initial Value	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-166 PFC_P10_SR Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b. The write value should always be 0b.
24 to 16	SR_WE[08:00]	Enables write to SR[08:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	SR[08:00]	Set the PORT10 pin bit[08:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.127 PORT10 Input Data Mask Register (PFC_P10_DI_MSK)

This register controls masking of input data of the PORT10 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02B0h

Initial Value: 0000_01FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DI_MSK_WE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DI_MSK[08:00]								
Initial Value	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-167 PFC_P10_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b. The write value should always be 0b.
24 to 16	DI_MSK_WE[08:00]	Enables write to DI_MSK[08:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	DI_MSK[08:00]	Set the PORT10 DI_MSK pin value bit[08:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.128 PORT10 Input/Output Enable Mask Register (PFC_P10_EN_MSK)

This register controls masking of input/output enable for the PORT10 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02B4h

Initial Value: 0000_01FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	EN_MSK_WE08	EN_MSK_WE07	EN_MSK_WE06	EN_MSK_WE05	EN_MSK_WE04	EN_MSK_WE03	EN_MSK_WE02	EN_MSK_WE01	EN_MSK_WE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	EN_MSK08	EN_MSK07	EN_MSK06	EN_MSK05	EN_MSK04	EN_MSK03	EN_MSK02	EN_MSK01	EN_MSK00
Initial Value	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-168 PFC_P10_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b. The write value should always be 0b.
24 to 16	EN_MSK_WE[08:00]	Enables write to EN_MSK[08:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	EN_MSK[08:00]	Set the PORT10 EN_MSK pin bit[08:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.129 PORT11 GPIO Output Value Control Register (PFC_P11_GPIO_DO)

This register controls the output value of PORT11 GPIO.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02C0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DO_WE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DO[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-169 PFC_P11_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b. The write value should always be 0b.
24 to 16	DO_WE[08:00]	Enables write to DO[08:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	DO[08:00]	Set the GPIO PORT11 bit[08:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.130 PORT11 GPIO Output Control Register (PFC_P11_GPIO_OE)

This register controls whether GPIO PORT11 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02C4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	OE_WE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	OE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-170 PFC_P11_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b. The write value should always be 0b.
24 to 16	OE_WE[08:00]	Enables write to OE[08:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	OE[08:00]	Control the output of GPIO PORT11 bit[08:00]. 0b: Disable output. 1b: Enable output.

41.4.2.131 PORT11 GPIO Input Control Register (PFC_P11_GPIO_IE)

This register controls whether GPIO PORT11 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02C8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	IE_WE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	IE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-171 PFC_P11_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b. The write value should always be 0b.
24 to 16	IE_WE[08:00]	Enables write to IE[08:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	IE[08:00]	Control the input of GPIO PORT11 pin bit[08:00]. 0b: Disable input. 1b: Enable input.

41.4.2.132 PORT11 Function Select Register 0 (PFC_P11_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT11.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02D0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-172 PFC_P11_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT11 (see **Table 41.4-173**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-172 PFC_P11_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT11 (see **Table 41.4-173**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT11 (see **Table 41.4-173**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT11 (see **Table 41.4-173**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-173 Assignment list of PORT11 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO11[3]	IM1TXD (STG)	—	—	—	—	—	—
PF02	GPIO11[2]	IM1CS (STG)	—	—	—	—	—	—
PF01	GPIO11[1]	IM1HS (STG)	—	—	—	—	—	—
PF00	GPIO11[0]	IM1VS (STG)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.133 PORT11 Function Select Register 1 (PFC_P11_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT11.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02D4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-174 PFC_P11_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT11 (see **Table 41.4-175**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-174 PFC_P11_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT11 (see **Table 41.4-175**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT11 (see **Table 41.4-175**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT11 (see **Table 41.4-175**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-175 Assignment list of PORT11 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO11[7]	IM1SIG1 (STG)	INEXINT29 (GIC)	—	—	—	—	—
PF06	GPIO11[6]	IM1SIG0 (STG)	INEXINT28 (GIC)	—	—	—	—	—
PF05	GPIO11[5]	IM1SCLK (STG)	—	—	—	—	—	—
PF04	GPIO11[4]	IM1RXD (STG)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.134 PORT11 Function Select Register 2 (PFC_P11_PFSEL2)

This register controls function selection of the multi-purpose pin in PORT11.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02D8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	PF_WE08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	PF08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 41.4-176 PFC_P11_PFSEL2 Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b. The write value should always be 0b.
18 to 16	PF_WE08	Enables write to PF08. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b. The write value should always be 0b.
2 to 0	PF08	Select the function of multi-purpose pin 08 bit in PORT11 (see **Table 41.4-177**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-177 Assignment list of PORT11 multifunction pin by PF08

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF08	GPIO11[8]	IM1SIG2 (STG)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.135 PORT11 Input Value Monitor Register (PFC_P11_DI_MON)

This register is a read-only register that monitors the input value of the PORT11 input pin (P11_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02E0h

Initial Value: 0000_0xxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DI[08:00]								
Initial Value	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-178 PFC_P11_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	DI[08:00]	The input value of PORT11 input pin bit[08:00].

41.4.2.136 PORT11 Pull-Up/Down Control Register (PFC_P11_PUPD)

This register controls pulling up and down of the PORT11 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02E4h

Initial Value: 0001_5110h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PUPD08	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-179 PFC_P11_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 18	—	Reserved. These bits are read as 0b. The write value should always be 0b.
17 to 0	PUPD[08:00]	Control PORT11 pin bit[08:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.137 PORT11 Drive Strength Control Register (PFC_P11_DRV)

This register controls the drive strength of the PORT11 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02E8h

Initial Value: 0001_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV08	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-180 PFC_P11_DRV Register Contents

Bit Position	Bit Name	Description
31 to 18	—	Reserved. These bits are read as 0b. The write value should always be 0b.
17 to 0	DRV[08:00]	Control the PORT11 pin bit[08:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.138 PORT11 Slew-rate Control Register (PFC_P11_SR)

This register controls the slew-rate of the PORT11 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02ECh

Initial Value: 0000_01FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	SR_WE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SR[08:00]								
Initial Value	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-181 PFC_P11_SR Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b. The write value should always be 0b.
24 to 16	SR_WE[08:00]	Enables write to SR[08:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	SR[08:00]	Set the PORT11 pin bit[08:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.139 PORT11 Input Data Mask Register (PFC_P11_DI_MSK)

This register controls masking of input data of the PORT11 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02F0h

Initial Value: 0000_01FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DI_MSK_WE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DI_MSK[08:00]								
Initial Value	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-182 PFC_P11_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b. The write value should always be 0b.
24 to 16	DI_MSK_WE[08:00]	Enables write to DI_MSK[08:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	DI_MSK[08:00]	Set the PORT11 DI_MSK pin value bit[08:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.140 PORT11 Input/Output Enable Mask Register (PFC_P11_EN_MSK)

This register controls masking of input/output enable for the PORT11 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 02F4h

Initial Value: 0000_01FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	EN_MSK_WE[08:00]								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	EN_MSK[08:00]								
Initial Value	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-183 PFC_P11_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b. The write value should always be 0b.
24 to 16	EN_MSK_WE[08:00]	Enables write to EN_MSK[08:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b. The write value should always be 0b.
8 to 0	EN_MSK[08:00]	Set the PORT11 EN_MSK pin bit[08:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.141 PORT12 GPIO Output Value Control Register (PFC_P12_GPIO_DO)

This register controls the output value of GPIO PORT12.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0300h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	DO_WE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	DO[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 41.4-184 PFC_P12_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	DO_WE[03:00]	Enables write to DO[03:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3 to 0	DO[03:00]	Set the GPIO PORT12 bit[03:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.142 PORT12 GPIO Output Control Register (PFC_P12_GPIO_OE)

This register controls whether GPIO PORT12 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0304h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	OE_WE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	OE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 41.4-185 PFC_P12_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	OE_WE[03:00]	Enables write to OE[03:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3 to 0	OE[03:00]	Control the output of GPIO PORT12 bit[03:00]. 0b: Disable output. 1b: Enable output.

41.4.2.143 PORT12 GPIO Input Control Register (PFC_P12_GPIO_IE)

This register controls whether GPIO PORT12 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0308h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	IE_WE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	IE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 41.4-186 PFC_P12_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	IE_WE[03:00]	Enables write to IE[03:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3 to 0	IE[03:00]	Control the input of GPIO PORT12 pin bit[03:00]. 0b: Disable input. 1b: Enable input.

41.4.2.144 PORT12 Function Select Register 0 (PFC_P12_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT12.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0310h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-187 PFC_P12_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT12 (see **Table 41.4-188**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-187 PFC_P12_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT12 (see **Table 41.4-188**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT12 (see **Table 41.4-188**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT12 (see **Table 41.4-188**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-188 Assignment list of PORT12 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO12[3]	IMSTSIG1 (STG)	INEXINT33(GIC)	—	—	—	—	—
PF02	GPIO12[2]	IMSTSIG0 (STG)	INEXINT32(GIC)	—	—	—	—	—
PF01	GPIO12[1]	IMSHUT1 (STG)	INEXINT31(GIC)	—	—	—	—	—
PF00	GPIO12[0]	IMSHUT0 (STG)	INEXINT30(GIC)	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.145 PORT12 Input Value Monitor Register (PFC_P12_DI_MON)

This register is a read-only register that monitors the input value of the PORT12 input pin (P02_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0320h

Initial Value: 0000_000xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	DI[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-189 PFC_P12_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 4	—	Reserved. These bits are read as 0b.
3 to 0	DI[03:00]	The input value of PORT12 input pin bit[03:00].

41.4.2.146 PORT12 Pull-Up/Down Control Register (PFC_P12_PUPD)

This register controls pulling up and down of the PORT12 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0324h

Initial Value: 0000_0054h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-190 PFC_P12_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	PUPD[03:00]	Control PORT12 pin bit[03:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.147 PORT12 Drive Strength Control Register (PFC_P12_DRV)

This register controls the drive strength of the PORT12 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0328h

Initial Value: 0000_0055h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DRV03		DRV02		DRV01		DRV00	
Initial Value	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-191 PFC_P12_DRV Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	DRV[03:00]	Control the PORT12 pin bit[03:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.148 PORT12 Slew-rate Control Register (PFC_P12_SR)

This register controls the slew-rate of the PORT12 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 032Ch

Initial Value: 0000_000Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	SR_WE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	SR[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 41.4-192 PFC_P12_SR Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	SR_WE[03:00]	Enables write to SR[03:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3 to 0	SR[03:00]	Set the PORT12 pin bit[03:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.149 PORT12 Input Data Mask Register (PFC_P12_DI_MSK)

This register controls masking of input data of the PORT12 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0330h

Initial Value: 0000_000Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	DI_MSK_WE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	DI_MSK[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 41.4-193 PFC_P12_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	DI_MSK_WE[03:00]	Enables write to DI_MSK[03:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3 to 0	DI_MSK[03:00]	Set the PORT12 DI_MSK pin value bit[03:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.150 PORT12 Input/Output Enable Mask Register (PFC_P12_EN_MSK)

This register controls masking of input/output enable for the PORT12 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0334h

Initial Value: 0000_000Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	EN_MSK_WE[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	EN_MSK[03:00]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 41.4-194 PFC_P12_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19 to 16	EN_MSK_WE[03:00]	Enables write to EN_MSK[03:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b. The write value should always be 0b.
3 to 0	EN_MSK[03:00]	Set the PORT12 EN_MSK pin bit[03:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.151 PORT13 GPIO Output Value Control Register (PFC_P13_GPIO_DO)

This register controls the output value of PORT13 GPIO.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0340h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	DO_WE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DO[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-195 PFC_P13_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 16	DO_WE[11:00]	Enables write to DO[11:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	DO[11:00]	Set the GPIO PORT13 bit[11:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.152 PORT13 GPIO Output Control Register (PFC_P13_GPIO_OE)

This register controls whether GPIO PORT13 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0344h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	OE_WE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	OE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-196 PFC_P13_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 16	OE_WE[11:00]	Enables write to OE[11:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	OE[11:00]	Control the output of GPIO PORT13 bit[11:00]. 0b: Disable output. 1b: Enable output.

41.4.2.153 PORT13 GPIO Input Control Register (PFC_P13_GPIO_IE)

This register controls whether GPIO PORT13 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0348h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	IE_WE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	IE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-197 PFC_P13_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 16	IE_WE[11:00]	Enables write to IE[11:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	IE[11:00]	Control the input of GPIO PORT13 pin bit[11:00]. 0b: Disable input. 1b: Enable input.

41.4.2.154 PORT13 Function Select Register 0 (PFC_P13_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT13.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0350h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-198 PFC_P13_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF_WE03	Select the function of multi-purpose pin 03 bit in PORT13 (see **Table 41.4-199**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-198 PFC_P13_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF_WE02	Select the function of multi-purpose pin 02 bit in PORT13 (see **Table 41.4-199**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF_WE01	Select the function of multi-purpose pin 01 bit in PORT13 (see **Table 41.4-199**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF_WE00	Select the function of multi-purpose pin 00 bit in PORT13 (see **Table 41.4-199**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-199 Assignment list of PORT13 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO13[3]	—	—	MTDRV3 (MTR)	—	—	—	—
PF02	GPIO13[2]	—	—	MTDRV2 (MTR)	—	—	—	—
PF01	GPIO13[1]	—	—	MTDRV1 (MTR)	—	—	—	—
PF00	GPIO13[0]	—	—	MTDRV0 (MTR)	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.155 PORT13 Function Select Register 1 (PFC_P13_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT13.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0354h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-200 PFC_P13_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF_WE07	Select the function of multi-purpose pin 07 bit in PORT13 (see **Table 41.4-201**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-200 PFC_P13_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF_WE06	Select the function of multi-purpose pin 06 bit in PORT13 (see **Table 41.4-201**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF_WE05	Select the function of multi-purpose pin 05 bit in PORT13 (see **Table 41.4-201**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF_WE04	Select the function of multi-purpose pin 04 bit in PORT13 (see **Table 41.4-201**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-201 Assignment list of PORT13 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO13[7]	—	—	MTDRV7 (MTR)	—	—	—	—
PF06	GPIO13[6]	—	—	MTDRV6 (MTR)	—	—	—	—
PF05	GPIO13[5]	—	—	MTDRV5 (MTR)	—	—	—	—
PF04	GPIO13[4]	—	—	MTDRV4 (MTR)	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.156 PORT13 Function Select Register 2 (PFC_P13_PFSEL2)

This register controls function selection of the multi-purpose pin in PORT13.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0358h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE11			—	PF_WE10			—	PF_WE09			—	PF_WE08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF11			—	PF10			—	PF09			—	PF08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-202 PFC_P13_PFSEL2 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE11	Enables write to PF11. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE10	Enables write to PF10. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE09	Enables write to PF09. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE08	Enables write to PF08. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF_WE11	Select the function of multi-purpose pin 11 bit in PORT13 (see **Table 41.4-203**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-202 PFC_P13_PFSEL2 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF_WE10	Select the function of multi-purpose pin 10 bit in PORT13 (see **Table 41.4-203**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF_WE09	Select the function of multi-purpose pin 09 bit in PORT13 (see **Table 41.4-203**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF_WE08	Select the function of multi-purpose pin 08 bit in PORT13 (see **Table 41.4-203**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-203 Assignment list of PORT13 multifunction pin by PF11 to 08

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF11	GPIO13[11]	—	INEXINT36 (GIC)	MTDCPLS3 (MTR)	—	—	—	—
PF10	GPIO13[10]	—	INEXINT35 (GIC)	MTDCPLS2 (MTR)	—	—	—	—
PF09	GPIO13[9]	—	INEXINT34 (GIC)	MTDCPLS1 (MTR)	—	—	—	—
PF08	GPIO13[8]	—	—	MTDCPLS0 (MTR)	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.157 PORT13 Input Value Monitor Register (PFC_P13_DI_MON)

This register is a read-only register that monitors the input value of the PORT13 input pin (P13_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0360h

Initial Value: 0000_0xxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DI[11:00]											
Initial Value	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-204 PFC_P13_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 12	—	Reserved. These bits are read as 0b.
11 to 0	DI[11:00]	The input value of PORT13 input pin bit[11:00].

41.4.2.158 PORT13 Pull-Up/Down Control Register (PFC_P13_PUPD)

This register controls pulling up and down of the PORT13 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0364h

Initial Value: 0055_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	PUPD11		PUPD10		PUPD09		PUPD08	
Initial Value	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-205 PFC_P13_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 0	PUPD[11:00]	Control PORT13 pin bit[11:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.159 PORT13 Drive Strength Control Register (PFC_P13_DRV)

This register controls the drive strength of the PORT13 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0368h

Initial Value: 0055_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DRV11		DRV10		DRV09		DRV08	
Initial Value	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-206 PFC_P13_DRV Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 0	DRV[11:00]	Control the PORT13 pin bit[11:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.160 PORT13 Slew-rate Control Register (PFC_P13_SR)

This register controls the slew-rate of the PORT13 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 036Ch

Initial Value: 0000_0FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	SR_WE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SR[11:00]											
Initial Value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-207 PFC_P13_SR Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 16	SR_WE[11:00]	Enables write to SR[11:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	SR[11:00]	Set the PORT13 pin bit[11:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.161 PORT13 Input Data Mask Register (PFC_P13_DI_MSK)

This register controls masking of input data of the PORT13 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0370h

Initial Value: 0000_0FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	DI_MSK_WE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DI_MSK[11:00]											
Initial Value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-208 PFC_P13_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 16	DI_MSK_WE[11:00]	Enables write to DI_MSK[11:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	DI_MSK[11:00]	Set the PORT13 DI_MSK pin value bit[11:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.162 PORT13 Input/Output Enable Mask Register (PFC_P13_EN_MSK)

This register controls masking of input/output enable for the PORT13 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0374h

Initial Value: 0000_0FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	EN_MSK_WE[11:00]											
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	EN_MSK[11:00]											
Initial Value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-209 PFC_P13_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 16	EN_MSK_WE[11:00]	Enables write to EN_MSK[11:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b. The write value should always be 0b.
11 to 0	EN_MSK[11:00]	Set the PORT13 EN_MSK pin bit[11:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.163 PORT14 GPIO Output Value Control Register (PFC_P14_GPIO_DO)

This register controls the output value of GPIO PORT14.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0380h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DO_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DO[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-210 PFC_P14_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	DO_WE[07:00]	Enables write to DO[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	DO[07:00]	Set the GPIO PORT14 bit[07:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.164 PORT14 GPIO Output Control Register (PFC_P14_GPIO_OE)

This register controls whether GPIO PORT14 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0384h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	OE_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	OE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-211 PFC_P14_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	OE_WE[07:00]	Enables write to OE[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	OE[07:00]	Control the output of GPIO PORT14 bit[07:00]. 0b: Disable output. 1b: Enable output.

41.4.2.165 PORT14 GPIO Input Control Register (PFC_P14_GPIO_IE)

This register controls whether GPIO PORT14 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0388h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	IE_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	IE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-212 PFC_P14_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	IE_WE[07:00]	Enables write to IE[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	IE[07:00]	Control the input of GPIO PORT14 pin bit[07:00]. 0b: Disable input. 1b: Enable input.

41.4.2.166 PORT14 Function Select Register 0 (PFC_P14_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT14.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0390h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-213 PFC_P14_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT14 (see **Table 41.4-214**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-213 PFC_P14_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT14 (see **Table 41.4-214**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT14 (see **Table 41.4-214**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT14 (see **Table 41.4-214**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-214 Assignment list of PORT14 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO14[3]	—	—	MTSCLK0 (MTR)	—	—	—	—
PF02	GPIO14[2]	—	INEXINT37 (GIC)	MTRXD0 (MTR)	—	—	—	—
PF01	GPIO14[1]	—	—	MTTXD0 (MTR)	—	—	—	—
PF00	GPIO14[0]	—	—	MTCS0 (MTR)	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.167 PORT14 Function Select Register 1 (PFC_P14_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT14.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0394h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-215 PFC_P14_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT14 (see **Table 41.4-216**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-215 PFC_P14_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT14 (see **Table 41.4-216**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT14 (see **Table 41.4-216**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT14 (see **Table 41.4-216**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-216 Assignment list of PORT14 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO14[7]	—	—	MTSCLK1 (MTR)	—	—	—	—
PF06	GPIO14[6]	—	INEXINT38 (GIC)	MTRXD1 (MTR)	—	—	—	—
PF05	GPIO14[5]	—	—	MTTXD1 (MTR)	—	—	—	—
PF04	GPIO14[4]	—	—	MTCS1 (MTR)	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.168 PORT14 Input Value Monitor Register (PFC_P14_DI_MON)

This register is a read-only register that monitors the input value of the PORT14 input pin (P14_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03A0h

Initial Value: 0000_00xxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DI[07:00]							
Initial Value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-217 PFC_P14_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 0	DI[07:00]	The input value of PORT14 input pin bit[07:00].

41.4.2.169 PORT14 Pull-Up/Down Control Register (PFC_P14_PUPD)

This register controls pulling up and down of the PORT14 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03A4h

Initial Value: 0000_1111h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-218 PFC_P14_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15 to 0	PUPD[07:00]	Control PORT14 pin bit[07:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.170 PORT14 Drive Strength Control Register (PFC_P14_DRV)

This register controls the drive strength of the PORT14 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03A8h

Initial Value: 0000_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-219 PFC_P14_DRV Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b. The write value should always be 0b.
15 to 0	DRV[07:00]	Control the PORT14 pin bit[07:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.171 PORT14 Slew-rate Control Register (PFC_P14_SR)

This register controls the slew-rate of the PORT14 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03ACh

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SR_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SR[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-220 PFC_P14_SR Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	SR_WE[07:00]	Enables write to SR[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	SR[07:00]	Set the PORT14 pin bit[07:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.172 PORT14 Input Data Mask Register (PFC_P14_DI_MSK)

This register controls masking of input data of the PORT14 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03B0h

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DI_MSK_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DI_MSK[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-221 PFC_P14_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	DI_MSK_WE[07:00]	Enables write to DI_MSK[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	DI_MSK[07:00]	Set the PORT14 DI_MSK pin value bit[07:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.173 PORT14 Input/Output Enable Mask Register (PFC_P14_EN_MSK)

This register controls masking of input/output enable for the PORT14 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03B4h

Initial Value: 0000_00FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	EN_MSK_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	EN_MSK[07:00]							
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-222 PFC_P14_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	EN_MSK_WE[07:00]	Enables write to EN_MSK[07:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b. The write value should always be 0b.
7 to 0	EN_MSK[07:00]	Set the PORT14 EN_MSK pin bit[07:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.174 PORT15 GPIO Output Value Control Register (PFC_P15_GPIO_DO)

This register controls the output value of PORT15 GPIO.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03C0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DO_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DO[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-223 PFC_P15_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 16	DO_WE[15:00]	Enables write to DO[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	DO[15:00]	Set the GPIO PORT15 bit[15:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.175 PORT15 GPIO Output Control Register (PFC_P15_GPIO_OE)

This register controls whether GPIO PORT15 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03C4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OE_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-224 PFC_P15_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 16	OE_WE[15:00]	Enables write to OE[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	OE[15:00]	Control the output of GPIO PORT15 bit[15:00]. 0b: Disable output. 1b: Enable output.

41.4.2.176 PORT15 GPIO Input Control Register (PFC_P15_GPIO_IE)

This register controls whether GPIO PORT15 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03C8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IE_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-225 PFC_P15_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 16	IE_WE[15:00]	Enables write to IE[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	IE[15:00]	Control the input of GPIO PORT15 pin bit[15:00]. 0b: Disable input. 1b: Enable input.

41.4.2.177 PORT15 Function Select Register 0 (PFC_P15_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT15.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03D0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-226 PFC_P15_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT15 (see **Table 41.4-227**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-226 PFC_P15_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT15 (see **Table 41.4-227**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT15 (see **Table 41.4-227**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT15 (see **Table 41.4-227**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-227 Assignment list of PORT15 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO15[3]	GETXD0 (ETHER)	—	—	—	—	—	—
PF02	GPIO15[2]	GETXER (ETHER)	—	—	—	—	—	—
PF01	GPIO15[1]	GETXEN (ETHER)	—	—	TRCTL (CST)	—	—	—
PF00	GPIO15[0]	GETXC (ETHER)	—	—	TRCLK (CST)	—	—	—

Remarks: —: Setting prohibited

41.4.2.178 PORT15 Function Select Register 1 (PFC_P15_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT15.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03D4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-228 PFC_P15_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT15 (see **Table 41.4-229**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-228 PFC_P15_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT15 (see **Table 41.4-229**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT15 (see **Table 41.4-229**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT15 (see **Table 41.4-229**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-229 Assignment list of PORT15 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO15[7]	GETXD4 (ETHER)	—	—	—	—	—	—
PF06	GPIO15[6]	GETXD3 (ETHER)	—	—	—	—	—	—
PF05	GPIO15[5]	GETXD2 (ETHER)	—	—	—	—	—	—
PF04	GPIO15[4]	GETXD1 (ETHER)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.179 PORT15 Function Select Register 2 (PFC_P15_PFSEL2)

This register controls function selection of the multi-purpose pin in PORT15.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03D8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE11			—	PF_WE10			—	PF_WE09			—	PF_WE08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF11			—	PF10			—	PF09			—	PF08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-230 PFC_P15_PFSEL2 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE11	Enables write to PF11. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE10	Enables write to PF10. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE09	Enables write to PF09. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE08	Enables write to PF08. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF11	Select the function of multi-purpose pin 11 bit in PORT15 (see **Table 41.4-231**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-230 PFC_P15_PFSEL2 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF10	Select the function of multi-purpose pin 10 bit in PORT15 (see **Table 41.4-231**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF09	Select the function of multi-purpose pin 09 bit in PORT15 (see **Table 41.4-231**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF08	Select the function of multi-purpose pin 08 bit in PORT15 (see **Table 41.4-231**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-231 Assignment list of PORT15 multifunction pin by PF11 to 08

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF11	GPIO15[11]	GERXC (ETHER)	—	—	TRDAT3 (CST)	—	—	—
PF10	GPIO15[10]	GETXD7 (ETHER)	—	—	TRDAT2 (CST)	—	—	—
PF09	GPIO15[9]	GETXD6 (ETHER)	—	—	TRDAT1 (CST)	—	—	—
PF08	GPIO15[8]	GETXD5 (ETHER)	—	—	TRDAT0 (CST)	—	—	—

Remarks: —: Setting prohibited

41.4.2.180 PORT15 Function Select Register 3 (PFC_P15_PFSEL3)

This register controls function selection of the multi-purpose pin in PORT15.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03DCh

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE15			—	PF_WE14			—	PF_WE13			—	PF_WE12		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF15			—	PF14			—	PF13			—	PF12		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-232 PFC_P15_PFSEL3 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE15	Enables write to PF15. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE14	Enables write to PF14. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE13	Enables write to PF13. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE12	Enables write to PF12. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF15	Select the function of multi-purpose pin 15 bit in PORT15 (see **Table 41.4-233**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-232 PFC_P15_PFSEL3 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF14	Select the function of multi-purpose pin 14 bit in PORT15 (see **Table 41.4-233**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF13	Select the function of multi-purpose pin 13 bit in PORT15 (see **Table 41.4-233**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF12	Select the function of multi-purpose pin 12 bit in PORT15 (see **Table 41.4-233**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-233 Assignment list of PORT15 multifunction pin by PF15 to 12

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF15	GPIO15[15]	GERXD1 (ETHER)	—	—	TRDAT7 (CST)	—	—	—
PF14	GPIO15[14]	GERXD0 (ETHER)	—	—	TRDAT6 (CST)	—	—	—
PF13	GPIO15[13]	GERXER (ETHER)	—	—	TRDAT5 (CST)	—	—	—
PF12	GPIO15[12]	GERXDV (ETHER)	—	—	TRDAT4 (CST)	—	—	—

Remarks: —: Setting prohibited

41.4.2.181 PORT15 Input Value Monitor Register (PFC_P15_DI_MON)

This register is a read-only register that monitors the input value of the PORT15 input pin (P15_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03E0h

Initial Value: 0000_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DI[15:00]															
Initial Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-234 PFC_P15_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15 to 0	DI[15:00]	The input value of PORT15 input pin bit[15:00].

41.4.2.182 PORT15 Pull-Up/Down Control Register (PFC_P15_PUPD)

This register controls pulling up and down of the PORT15 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03E4h

Initial Value: 5555_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPD15		PUPD14		PUPD13		PUPD12		PUPD11		PUPD10		PUPD09		PUPD08	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-235 PFC_P15_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 0	PUPD[15:00]	Control PORT15 pin bit[15:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.183 PORT15 Drive Strength Control Register (PFC_P15_DRV)

This register controls the drive strength of the PORT15 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03E8h

Initial Value: 5555_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DRV15		DRV14		DRV13		DRV12		DRV11		DRV10		DRV09		DRV08	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-236 PFC_P15_DRV Register Contents

Bit Position	Bit Name	Description
31 to 0	DRV[15:00]	Control the PORT15 pin bit[15:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.184 PORT15 Slew-rate Control Register (PFC_P15_SR)

This register controls the slew-rate of the PORT15 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03ECh

Initial Value: 0000_FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SR_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SR[15:00]															
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-237 PFC_P15_SR Register Contents

Bit Position	Bit Name	Description
31 to 16	SR_WE[15:00]	Enables write to SR[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	SR[15:00]	Set the PORT15 pin bit[15:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.185 PORT15 Input Data Mask Register (PFC_P15_DI_MSK)

This register controls masking of input data of the PORT15 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03F0h

Initial Value: 0000_FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DI_MSK_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DI_MSK[15:00]															
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-238 PFC_P15_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 16	DI_MSK_WE[15:00]	Enables write to DI_MSK[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	DI_MSK[15:00]	Set the PORT15 DI_MSK pin value bit[15:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.186 PORT15 Input/Output Enable Mask Register (PFC_P15_EN_MSK)

This register controls masking of input/output enable for the PORT15 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 03F4h

Initial Value: 0000_FFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EN_MSK_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN_MSK[15:00]															
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-239 PFC_P15_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 16	EN_MSK_WE[15:00]	Enables write to EN_MSK[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	EN_MSK[15:00]	Set the PORT15 EN_MSK pin bit[15:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.187 PORT16 GPIO Output Value Control Register (PFC_P16_GPIO_DO)

This register controls the output value of GPIO PORT16.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0400h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	DO_WE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DO[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-240 PFC_P16_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29 to 16	DO_WE[13:00]	Enables write to DO[13:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 0	DO[13:00]	Set the GPIO PORT16 bit[13:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.188 PORT16 GPIO Output Control Register (PFC_P16_GPIO_OE)

This register controls whether GPIO PORT16 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0404h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	OE_WE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	OE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-241 PFC_P16_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29 to 16	OE_WE[13:00]	Enables write to OE[13:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 0	OE[13:00]	Control the output of GPIO PORT16 bit[13:00]. 0b: Disable output. 1b: Enable output.

41.4.2.189 PORT16 GPIO Input Control Register (PFC_P16_GPIO_IE)

This register controls whether GPIO PORT16 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0408h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	IE_WE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	IE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-242 PFC_P16_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29 to 16	IE_WE[13:00]	Enables write to IE[13:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 0	IE[13:00]	Control the input of GPIO PORT16 pin bit[13:00]. 0b: Disable input. 1b: Enable input.

41.4.2.190 PORT16 Function Select Register 0 (PFC_P16_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT16.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0410h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE03			—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF03			—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-243 PFC_P16_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE03	Enables write to PF03. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF03	Select the function of multi-purpose pin 03 bit in PORT16 (see **Table 41.4-244**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-243 PFC_P16_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT16 (see **Table 41.4-244**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT16 (see **Table 41.4-244**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT16 (see **Table 41.4-244**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-244 Assignment list of PORT16 multifunction pin by PF03 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF03	GPIO16[3]	GERXD5 (ETHER)	—	MTDRV11 (MTR)	TRDAT11 (CST)	—	—	—
PF02	GPIO16[2]	GERXD4 (ETHER)	—	MTDRV10 (MTR)	TRDAT10 (CST)	—	—	—
PF01	GPIO16[1]	GERXD3 (ETHER)	—	MTDRV9 (MTR)	TRDAT9 (CST)	—	—	—
PF00	GPIO16[0]	GERXD2 (ETHER)	—	MTDRV8 (MTR)	TRDAT8 (CST)	—	—	—

41.4.2.191 PORT16 Function Select Register 1 (PFC_P16_PFSEL1)

This register controls function selection of the multi-purpose pin in PORT16.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0414h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE07			—	PF_WE06			—	PF_WE05			—	PF_WE04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF07			—	PF06			—	PF05			—	PF04		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-245 PFC_P16_PFSEL1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE07	Enables write to PF07. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE06	Enables write to PF06. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE05	Enables write to PF05. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE04	Enables write to PF04. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF07	Select the function of multi-purpose pin 07 bit in PORT16 (see **Table 41.4-246**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-245 PFC_P16_PFSEL1 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF06	Select the function of multi-purpose pin 06 bit in PORT16 (see **Table 41.4-246**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF05	Select the function of multi-purpose pin 05 bit in PORT16 (see **Table 41.4-246**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF04	Select the function of multi-purpose pin 04 bit in PORT16 (see **Table 41.4-246**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-246 Assignment list of PORT16 multifunction pin by PF07 to 04

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF07	GPIO16[7]	GECOL (ETHER)	—	MTDRV15 (MTR)	TRDAT15 (CST)	—	—	—
PF06	GPIO16[6]	GECRS (ETHER)	—	MTDRV14 (MTR)	TRDAT14 (CST)	—	—	—
PF05	GPIO16[5]	GERXD7 (ETHER)	—	MTDRV13 (MTR)	TRDAT13 (CST)	—	—	—
PF04	GPIO16[4]	GERXD6 (ETHER)	—	MTDRV12 (MTR)	TRDAT12 (CST)	—	—	—

41.4.2.192 PORT16 Function Select Register 2 (PFC_P16_PFSEL2)

This register controls function selection of the multi-purpose pin in PORT16.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0418h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PF_WE11			—	PF_WE10			—	PF_WE09			—	PF_WE08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PF11			—	PF10			—	PF09			—	PF08		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-247 PFC_P16_PFSEL2 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30 to 28	PF_WE11	Enables write to PF11. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 24	PF_WE10	Enables write to PF10. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE09	Enables write to PF09. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE08	Enables write to PF08. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b. The write value should always be 0b.
14 to 12	PF11	Select the function of multi-purpose pin 11 bit in PORT16 (see **Table 41.4-248**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
11	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-247 PFC_P16_PFSEL2 Register Contents (2/2)

Bit Position	Bit Name	Description
10 to 8	PF10	Select the function of multi-purpose pin 10 bit in PORT16 (see **Table 41.4-248**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.
6 to 4	PF09	Select the function of multi-purpose pin 09 bit in PORT16 (see **Table 41.4-248**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF08	Select the function of multi-purpose pin 08 bit in PORT16 (see **Table 41.4-248**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-248 Assignment list of PORT16 multifunction pin by PF11 to 08

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF11	GPIO16[11]	GELINK (ETHER)	—	—	—	—	—	—
PF10	GPIO16[10]	GEGTXCLK (ETHER)	—	—	—	—	—	—
PF09	GPIO16[9]	GEMDIO (ETHER)	—	—	—	—	—	—
PF08	GPIO16[8]	GEMDC (ETHER)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.193 PORT16 Function Select Register 3 (PFC_P16_PFSEL3)

This register controls function selection of the multi-purpose pin in PORT16.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 041Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	PF_WE13			—	PF_WE12		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	PF13			—	PF12		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-249 PFC_P16_PFSEL3 Register Contents

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b. The write value should always be 0b.
22 to 20	PF_WE13	Enables write to PF13. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE12	Enables write to PF12. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 7	—	Reserved. These bits are read as 0b. The write value should always be 0b.
6 to 4	PF13	Select the function of multi-purpose pin 13 bit in PORT16 (see **Table 41.4-250**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF12	Select the function of multi-purpose pin 12 bit in PORT16 (see **Table 41.4-250**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-250 Assignment list of PORT16 multifunction pin by PF13 to 12

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF13	GPIO16[13]	GECLK (ETHER)	—	—	—	—	—	—
PF12	GPIO16[12]	GEINT (ETHER)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.194 PORT16 Input Value Monitor Register (PFC_P16_DI_MON)

This register is a read-only register that monitors the input value of the PORT16 input pin (P16_DI).

Writing is ignored.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0420h

Initial Value: 0000_xxxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DI[13:00]													
Initial Value	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-251 PFC_P16_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 14	—	Reserved. These bits are read as 0b.
13 to 0	DI[13:00]	The input value of PORT16 input pin bit[13:00].

41.4.2.195 PORT16 Pull-Up/Down Control Register (PFC_P16_PUPD)

This register controls pulling up and down of the PORT16 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0424h

Initial Value: 0555_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	PUPD13		PUPD12		PUPD11		PUPD10		PUPD09		PUPD08	
Initial Value	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPD07		PUPD06		PUPD05		PUPD04		PUPD03		PUPD02		PUPD01		PUPD00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 41.4-252 PFC_P16_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 0	PUPD[13:00]	Control PORT16 pin bit[13:00] I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.196 PORT16 Drive Strength Control Register (PFC_P16_DRV)

This register controls the drive strength of the PORT16 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0428h

Initial Value: 0545_5555h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	DRV13		DRV12		DRV11		DRV10		DRV09		DRV08	
Initial Value	0	0	0	0	0	1	0	1	0	1	0	0	0	1	0	1
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRV07		DRV06		DRV05		DRV04		DRV03		DRV02		DRV01		DRV00	
Initial Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-253 PFC_P16_DRV Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27 to 0	DRV[13:00]	Control the PORT16 pin bit[13:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.197 PORT16 Slew-rate Control Register (PFC_P16_SR)

This register controls the slew-rate of the PORT16 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 042Ch

Initial Value: 0000_3FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	SR_WE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	SR[13:00]													
Initial Value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-254 PFC_P16_SR Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29 to 16	SR_WE[13:00]	Enables write to SR[13:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 0	SR[13:00]	Set the PORT16 pin bit[13:00] SR value. 0b: Fast slew 1b: Slow slew

41.4.2.198 PORT16 Input Data Mask Register (PFC_P16_DI_MSK)

This register controls masking of input data of the PORT16 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0430h

Initial Value: 0000_3FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	DI_MSK_WE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DI_MSK[13:00]													
Initial Value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-255 PFC_P16_DI_MSK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29 to 16	DI_MSK_WE[13:00]	Enables write to DI_MSK[13:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 0	DI_MSK[13:00]	Set the PORT16 DI_MSK pin value bit[13:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.199 PORT16 Input/Output Enable Mask Register (PFC_P16_EN_MSK)

This register controls masking of input/output enable for the PORT16 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0434h

Initial Value: 0000_3FFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	EN_MSK_WE[13:00]													
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	EN_MSK[13:00]													
Initial Value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-256 PFC_P16_EN_MSK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29 to 16	EN_MSK_WE[13:00]	Enables write to EN_MSK[13:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 0	EN_MSK[13:00]	Set the PORT16 EN_MSK pin bit[13:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.200 PORT17 GPIO Output Value Control Register (PFC_P17_GPIO_DO)

This register controls the output value of GPIO PORT17.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0440h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DO_WE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DO00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 41.4-257 PFC_P17_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b. The write value should always be 0b.
16	DO_WE00	Enables write to DO00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	DO00	Set the GPIO PORT17 bit 0 value. 0b: Output the low level. 1b: Output the high level.

41.4.2.201 PORT17 GPIO Output Control Register (PFC_P17_GPIO_OE)

This register controls whether GPIO PORT17 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0444h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OE_WE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 41.4-258 PFC_P17_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b. The write value should always be 0b.
16	OE_WE00	Enables write to OE00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	OE00	Control the output of GPIO PORT17 bit 0. 0b: Disable output. 1b: Enable output.

41.4.2.202 PORT17 GPIO Input Control Register (PFC_P17_GPIO_IE)

This register controls whether GPIO PORT17 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0448h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IE_WE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 41.4-259 PFC_P17_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b. The write value should always be 0b.
16	IE_WE00	Enables write to IE00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	IE00	Control the input of GPIO PORT17 pin bit 0. 0b: Disable input. 1b: Enable input.

41.4.2.203 PORT17 Function Select Register 0 (PFC_P17_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT17.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0450h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 41.4-260 PFC_P17_PFSEL0 Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT17 (see **Table 41.4-261**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-261 Assignment list of PORT17 multifunction pin by PF00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF00	GPIO17[0]	GEPPS (ETHER)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.204 PORT17 Input Value Monitor Register (PFC_P17_DI_MON)

This register is a read-only register that monitors the input value of the PORT17 input pin (P02_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0460h

Initial Value: 0000_000xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DI00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-262 PFC_P17_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 1	—	Reserved. These bits are read as 0b.
0	DI00	The input value of PORT17 input pin bit 0.

41.4.2.205 PORT17 Pull-Up/Down Control Register (PFC_P17_PUPD)

This register controls pulling up and down of the PORT17 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0464h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PUPD00	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Table 41.4-263 PFC_P17_PUPD Register Contents

Bit Position	Bit Name	Description
31 to 2	—	Reserved. These bits are read as 0b. The write value should always be 0b.
1, 0	PUPD00	Control PORT17 pin bit 0 I/O buffer pull-up/down. x1b: No pull-up/down 00b: Pull-down 10b: Pull-up (x: Don't care)

41.4.2.206 PORT17 Drive Strength Control Register (PFC_P17_DRV)

This register controls the drive strength of the PORT17 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0468h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV00	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Table 41.4-264 PFC_P17_DRV Register Contents

Bit Position	Bit Name	Description
31 to 2	—	Reserved. These bits are read as 0b. The write value should always be 0b.
1, 0	DRV00	Control the PORT17 pin bit 0 I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.207 PORT17 Slew-rate Control Register (PFC_P17_SR)

This register controls the slew-rate of the PORT17 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 046Ch

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SR_WE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SR00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 41.4-265 PFC_P17_SR Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b. The write value should always be 0b.
16	SR_WE00	Enables write to SR00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	SR00	Set the PORT17 pin bit 0 SR value. 0b: Fast slew 1b: Slow slew

41.4.2.208 PORT17 Input Data Mask Register (PFC_P17_DI_MSK)

This register controls masking of input data of the PORT17 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0470h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DI_MSK_WE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DI_MSK00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 41.4-266 PFC_P17_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b. The write value should always be 0b.
16	DI_MSK_WE00	Enables write to DI_MSK00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	DI_MSK00	Set the PORT17 DI_MSK pin value bit 0. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.209 PORT17 Input/Output Enable Mask Register (PFC_P17_EN_MSK)

This register controls masking of input/output enable for the PORT17 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0474h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EN_MSK_WE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EN_MSK00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 41.4-267 PFC_P17_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b. The write value should always be 0b.
16	EN_MSK_WE00	Enables write to EN_MSK00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	EN_MSK00	Set the PORT17 EN_MSK pin bit 0 value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.210 PORT20 GPIO Output Value Control Register (PFC_P20_GPIO_DO)

This register controls the output value of GPIO PORT20.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0500h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	DO_WE[02:00]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DO[02:00]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 41.4-268 PFC_P20_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b. The write value should always be 0b.
18 to 16	DO_WE[02:00]	Enables write to DO[02:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b. The write value should always be 0b.
2 to 0	DO[02:00]	Set the GPIO PORT20 bit[02:00] value. 0b: Output the low level. 1b: Output the high level.

41.4.2.211 PORT20 GPIO Output Control Register (PFC_P20_GPIO_OE)

This register controls whether GPIO PORT20 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0504h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	OE_WE[02:00]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	OE[02:00]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 41.4-269 PFC_P20_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b. The write value should always be 0b.
18 to 16	OE_WE[02:00]	Enables write to OE[02:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b. The write value should always be 0b.
2 to 0	OE[02:00]	Control the output of GPIO PORT20 bit[02:00]. 0b: Disable output. 1b: Enable output.

41.4.2.212 PORT20 GPIO Input Control Register (PFC_P20_GPIO_IE)

This register controls whether GPIO PORT20 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0508h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	IE_WE[02:00]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	IE[02:00]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 41.4-270 PFC_P20_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b. The write value should always be 0b.
18 to 16	IE_WE[02:00]	Enables write to IE[02:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b. The write value should always be 0b.
2 to 0	IE[02:00]	Control the input of GPIO PORT20 pin bit[02:00]. 0b: Disable input. 1b: Enable input.

41.4.2.213 PORT20 Function Select Register 0 (PFC_P20_PFSEL0)

This register controls function selection of the multi-purpose pin in PORT20.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0510h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	PF_WE02			—	PF_WE01			—	PF_WE00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	PF02			—	PF01			—	PF00		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 41.4-271 PFC_P20_PFSEL0 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 27	—	Reserved. These bits are read as 0b. The write value should always be 0b.
26 to 24	PF_WE02	Enables write to PF02. Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22 to 20	PF_WE01	Enables write to PF01. Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18 to 16	PF_WE00	Enables write to PF00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 11	—	Reserved. These bits are read as 0b. The write value should always be 0b.
10 to 8	PF02	Select the function of multi-purpose pin 02 bit in PORT20 (see **Table 41.4-272**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
7	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-271 PFC_P20_PFSEL0 Register Contents (2/2)

Bit Position	Bit Name	Description
6 to 4	PF01	Select the function of multi-purpose pin 01 bit in PORT20 (see **Table 41.4-272**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7
3	—	Reserved. This bit is read as 0b. The write value should always be 0b.
2 to 0	PF00	Select the function of multi-purpose pin 00 bit in PORT20 (see **Table 41.4-272**). 000b: Function 0 001b: Function 1 010b: Function 2 011b: Function 3 100b: Function 4 101b: Function 5 110b: Function 6 111b: Function 7

Table 41.4-272 Assignment list of PORT20 multifunction pin by PF02 to 00

	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
PF02	GPIO20[2]	HDHPD (HMI)	—	—	—	—	—	—
PF01	GPIO20[1]	HDSDA (HMI)	—	—	—	—	—	—
PF00	GPIO20[0]	HDSCL (HMI)	—	—	—	—	—	—

Remarks: —: Setting prohibited

41.4.2.214 PORT20 Input Value Monitor Register (PFC_P20_DI_MON)

This register is a read-only register that monitors the input value of the PORT20 input pin (P02_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0520h

Initial Value: 0000_000xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DI[02:00]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-273 PFC_P20_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 3	—	Reserved. These bits are read as 0b.
2 to 0	DI[02:00]	The input value of PORT20 input pin bit[02:00].

41.4.2.215 PORT20 Drive Strength Control Register (PFC_P20_DRV)

This register controls the drive strength of the PORT20 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0528h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	DRV02		DRV01		DRV00	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 41.4-274 PFC_P20_DRV Register Contents

Bit Position	Bit Name	Description
31 to 6	—	Reserved. These bits are read as 0b. The write value should always be 0b.
5 to 0	DRV[02:00]	Control the PORT20 pin bit[02:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.216 PORT20 Input Data Mask Register (PFC_P20_DI_MSK)

This register controls masking of input data of the PORT20 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0530h

Initial Value: 0000_0007h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	DI_MSK_WE[02:00]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DI_MSK[02:00]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 41.4-275 PFC_P20_DI_MSK Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b. The write value should always be 0b.
18 to 16	DI_MSK_WE[02:00]	Enables write to DI_MSK[02:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b. The write value should always be 0b.
2 to 0	DI_MSK[02:00]	Set the PORT20 DI_MSK pin value bit[02:00]. 0b: Remove masking of the input data. 1b: Mask the input data.

41.4.2.217 PORT20 Input/Output Enable Mask Register (PFC_P20_EN_MSK)

This register controls masking of input/output enable for the PORT20 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0534h

Initial Value: 0000_0007h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	EN_MSK_WE[02:00]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	EN_MSK[02:00]		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 41.4-276 PFC_P20_EN_MSK Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b. The write value should always be 0b.
18 to 16	EN_MSK_WE[02:00]	Enables write to EN_MSK[02:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b. The write value should always be 0b.
2 to 0	EN_MSK[02:00]	Set the PORT20 EN_MSK pin bit[02:00] value. 0b: Remove masking of the input/output enable. 1b: Mask the input/output enable.

41.4.2.218 PORT21 GPIO Output Value Control Register (PFC_P21_GPIO_DO)

This register controls the output value of GPIO PORT21.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0540h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DO_WE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DO00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 41.4-277 PFC_P21_GPIO_DO Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b. The write value should always be 0b.
16	DO_WE00	Enables write to DO00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	DO00	Set the GPIO PORT21 bit 0 value. 0b: Output the low level. 1b: Output the high level.

41.4.2.219 PORT21 GPIO Output Control Register (PFC_P21_GPIO_OE)

This register controls whether GPIO PORT21 output is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0544h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OE_WE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 41.4-278 PFC_P21_GPIO_OE Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b. The write value should always be 0b.
16	OE_WE00	Enables write to OE00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	OE00	Control the output of GPIO PORT21 bit 0. 0b: Disable output. 1b: Enable output.

41.4.2.220 PORT21 GPIO Input Control Register (PFC_P21_GPIO_IE)

This register controls whether GPIO PORT21 input is enabled or disabled.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0548h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IE_WE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 41.4-279 PFC_P21_GPIO_IE Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b. The write value should always be 0b.
16	IE_WE00	Enables write to IE00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	IE00	Control the input of GPIO PORT21 pin bit 0. 0b: Disable input. 1b: Enable input.

41.4.2.221 PORT21 Input Value Monitor Register (PFC_P21_DI_MON)

This register is a read-only register that monitors the input value of the PORT21 input pin (P02_DI).

Writing is ignored.

Immediately after reset, this register becomes 0000_0000h.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0560h

Initial Value: 0000_000xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DI00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 41.4-280 PFC_P21_DI_MON Register Contents

Bit Position	Bit Name	Description
31 to 1	—	Reserved. These bits are read as 0b.
0	DI0	The input value of PORT21 input pin bit 0.

41.4.2.222 PORT21 Drive Strength Control Register (PFC_P21_DRV)

This register controls the drive strength of the PORT21 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0568h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DRV00	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Table 41.4-281 PFC_P21_DRV Register Contents

Bit Position	Bit Name	Description
31 to 2	—	Reserved. These bits are read as 0b. The write value should always be 0b.
1, 0	DRV00	Control the PORT21 pin bit 0 I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

41.4.2.223 PORT21 Slew-rate Control Register (PFC_P21_SR)

This register controls the slew-rate of the PORT21 pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 056Ch

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SR_WE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SR00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 41.4-282 PFC_P21_SR Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b. The write value should always be 0b.
16	SR_WE00	Enables write to SR00. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b. The write value should always be 0b.
0	SR00	Set the PORT21 pin bit 0 SR value. 0b: Fast slew 1b: Slow slew

41.4.2.224 CSRXD Input Port Control Register (PFC_CSRXD_SEL)

This register controls input switching on the CSI CSRXD pin.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0580h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	RXD_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	RXD5	RXD4	RXD3	RXD2	RXD1	RXD0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 41.4-283 PFC_CSRXD_SEL Register Contents

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b. The write value should always be 0b.
21 to 16	RXD_WE[05:00]	Enables write to RXD[05:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b. The write value should always be 0b.
5	RXD5	Select input pin to CSRXD5. 0b: Select CSRXD5 (P04_05 function 1). 1b: Select CSTXD5 (P04_04 function 2).
4	RXD4	Select input pin to CSRXD4. 0b: Select CSRXD4 (P04_01 function 1) 1b: Select CSTXD4 (P04_00 function 2)
3	RXD3	Select input pin to CSRXD3. 0b: Select CSRXD3 (P03_13 function 1). 1b: Select CSTXD3 (P03_12 function 2).
2	RXD2	Select input pin to CSRXD2. 0b: Select CSRXD2 (P03_09 function 1). 1b: Select CSTXD2 (P03_08 function 3).
1	RXD1	Select input pin to CSRXD1. 0b: Select CSRXD1 (P03_05 function 1). 1b: Select CSTXD1 (P03_04 function 3).
0	RXD0	Select input pin to CSRXD0. 0b: Select CSRXD0 (P03_01 function 1). 1b: Select CSTXD0 (P03_00 function 3).

41.4.2.225 Dedicated Port Drive Strength Control Register 0 (PFC_PEX0_DRV)

This register controls the drive strength of the dedicated port.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0590h

Initial Value: 1140_143Dh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	DRV14		—	—	DRV12		—	—	—	—	—	—	—	—
Initial Value	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0
R/W	R	R	RW	RW	R	R	RW	RW	RW	RW	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DRV06		DRV05		—	—	—	—	DRV02		DRV01		DRV00	
Initial Value	0	0	0	1	0	1	0	0	0	0	1	1	1	1	0	1
R/W	R	R	RW	RW	RW	RW	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 41.4-284 PFC_PEX0_DRV Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b. The write value should always be 0b.
29, 28	DRV14	Control the dedicated terminal bit 14 I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6
27, 26	—	Reserved. These bits are read as 0b. The write value should always be 0b.
25, 24	DRV12	Control the dedicated terminal bit12 I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6
23,22	—	When read, the value read is undefined. Since these bits are for use with the ISP support package, writing to these bits is prohibited.
21 to 14	—	Reserved. These bits are read as 0b. The write value should always be 0b.
13 to 10	DRV[06:05]	Control the dedicated terminal bit[06:05] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6
9 to 6	—	Reserved. These bits are read as 0b. The write value should always be 0b.
5 to 0	DRV[02:00]	Control the dedicated terminal bit[02:00] I/O buffer drive strength. 00b: X1 01b: X2 10b: X4 11b: X6

Note: The correspondence table of each field name and dedicated terminal is shown in **Table 41.4-285**.

Table 41.4-285 Correspondence table of PEX0_DRV register fields and dedicated pins

Field name	Terminal name
DRV14	USPWEN
DRV12	PCRSTOUTB
DRV06	DETMS
DRV05	DETDO
DRV02	IM1CLK
DRV01	IM0CLK
DRV00	NAWPN

41.4.2.226 Dedicated Port Slew-rate Control Register 0 (PFC_PEX0_SR)

This register controls the slew-rate of the dedicated port.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 0594h

Initial Value: 0000_DFFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	SR_WE14	—	SR_WE12	—	—	—	—	—	SR_WE06	SR_WE05	—	—	SR_WE02	SR_WE01	SR_WE00
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R	R0W1	R0W1	R	R	R	R	R0W1	R0W1	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SR14	—	SR12	—	—	—	—	—	SR06	SR05	—	—	SR02	SR01	SR00
Initial Value	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	RW	R	RW	RW	R	R	R	R	RW	RW	R	R	RW	RW	RW

Table 41.4-286 PFC_PEX0_SR Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30	SR_WE14	Enables write to SR14. Write only. Read as 0b. 0b: Write disable 1b: Write enable
29	—	Reserved. This bit is read as 0b. The write value should always be 0b.
28	SR_WE12	Enables write to SR12. Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26 to 23	—	Reserved. These bits are read as 0b. The write value should always be 0b.
22, 21	SR_WE[06:05]	Enables write to SR[06:05]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
20, 19	—	Reserved. These bits are read as 0b. The write value should always be 0b.
18 to 16	SR_WE[02:00]	Enables write to SR[02:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 1b. The write value should always be 1b.
14	SR14	Set the dedicated terminal bit 14 SR value. 0b: Fast slew 1b: Slow slew
13	—	Reserved. This bit is read as 0b. The write value should always be 0b.

Table 41.4-286 PFC_PEX0_SR Register Contents (2/2)

Bit Position	Bit Name	Description
12	SR12	Set the dedicated terminal bit12 SR value. 0b: Fast slew 1b: Slow slew
11	—	When read, the value read is undefined. Since this bit is for use with the ISP support package, writing to this bit is prohibited.
10 to 7	—	Reserved. These bits are read as 1b. The write value should always be 1b.
6, 5	SR[06:05]	Set the dedicated terminal bit[06:05] SR value. 0b: Fast slew 1b: Slow slew
4, 3	—	Reserved. These bits are read as 1b. The write value should always be 1b.
2 to 0	SR[02:00]	Set the dedicated terminal bit[02:00] SR value. 0b: Fast slew 1b: Slow slew

Note: The correspondence table of each field name and dedicated terminal is shown in **Table 41.4-287**.

Table 41.4-287 Correspondence table of PEX0_SR register fields and dedicated pins

Field name	Terminal name
SR14	USPWEN
SR12	PCRSTOUTB
SR06	DETMS
SR05	DETDO
SR02	IM1CLK
SR01	IM0CLK
SR00	NAWPN

41.4.2.227 External Interrupt Signal Polarity Invert Control Register 0 (PFC_EXTINT_INV0)

This register controls whether the polarity of the external interrupt signal is inverted.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 05A0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INV_WE[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INV[15:00]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-288 PFC_EXTINT_INV0 Register Contents

Bit Position	Bit Name	Description
31 to 16	INV_WE[15:00]	Enables write to INV_WE[15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	INV[15:00]	Controls whether the polarity of the external interrupt terminal bit[15:00] is inverted. 0b: Not inverted 1b: Inverted

41.4.2.228 External Interrupt Signal Polarity Invert Control Register 1 (PFC_EXTINT_INV1)

This register controls whether the polarity of the external interrupt signal is inverted.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 05A4h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INV_WE[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INV[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 41.4-289 PFC_EXTINT_INV1 Register Contents

Bit Position	Bit Name	Description
31 to 16	INV_WE[31:16]	Enables write to INV_WE[31:16]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	INV[31:16]	Controls whether the polarity of the external interrupt terminal bit[31:16] is inverted. 0b: Not inverted 1b: Inverted

41.4.2.229 External Interrupt Signal Polarity Invert Control Register 2 (PFC_EXTINT_INV2)

This register controls whether the polarity of the external interrupt signal is inverted.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 05A8h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	INV_WE[38:32]						
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	INV[38:32]						
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW

Table 41.4-290 PFC_EXTINT_INV2 Register Contents

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b. The write value should always be 0b.
22 to 16	INV_WE[38:32]	Enables write to INV_WE[38:32]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 7	—	Reserved. These bits are read as 0b. The write value should always be 0b.
6 to 0	INV[38:32]	Controls whether the polarity of the external interrupt terminal bit[38:32] is inverted. 0b: Not inverted 1b: Inverted

41.4.2.230 External Interrupt Signal Mask Control Register 0 (PFC_EXTINT_MSK0)

This register controls masking of the external interrupt signal.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 05B0h

Initial Value: 0000_FFFFh

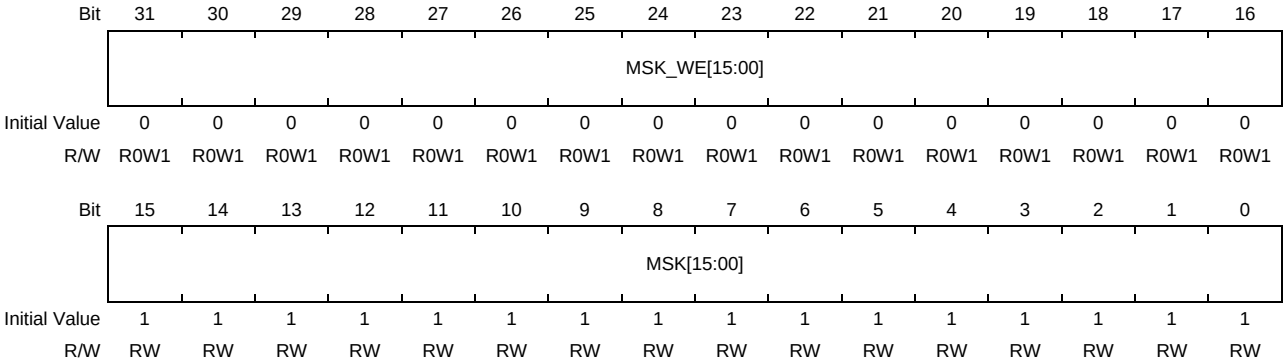


Table 41.4-291 PFC_EXTINT_MSK0 Register Contents

Bit Position	Bit Name	Description
31 to 16	MSK_WE[15:00]	Enables write to MSK [15:00]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	MSK[15:00]	Controls masking of the external interrupt terminal bit[15:00]. 0b: Remove masking of the external interrupt signal. 1b: Mask the external interrupt signal.

Note: Bits whose multiplexed function is other than external interrupt should always mask the external interrupt signal.

41.4.2.231 External Interrupt Signal Mask Control Register 1 (PFC_EXTINT_MSK1)

This register controls masking of the external interrupt signal.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 05B4h

Initial Value: 0000_FFFFh

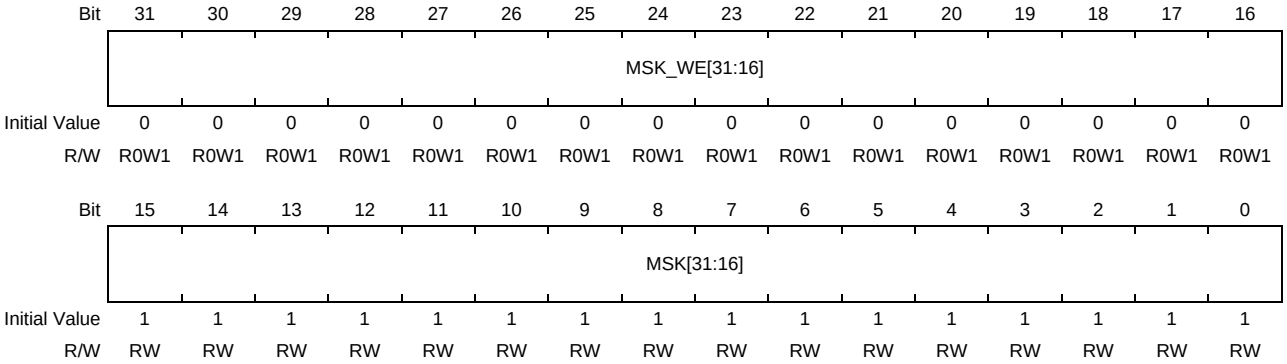


Table 41.4-292 PFC_EXTINT_MSK1 Register Contents

Bit Position	Bit Name	Description
31 to 16	MSK_WE[31:16]	Enables write to MSK [31:16]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 0	MSK[31:16]	Controls masking of the external interrupt terminal bit[31:16]. 0b: Remove masking of the external interrupt signal. 1b: Mask the external interrupt signal.

Note: Bits whose multiplexed function is other than external interrupt should always mask the external interrupt signal.

41.4.2.232 External Interrupt Signal Mask Control Register 2 (PFC_EXTINT_MSK2)

This register controls masking of the external interrupt signal.

Access Size: 32 bits

Address(es): <PFC_S0_base> + 05B8h

Initial Value: 0000_007Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	MSK_WE[38:32]						
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	MSK[38:32]						
Initial Value	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW

Table 41.4-293 PFC_EXTINT_MSK2 Register Contents

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b. The write value should always be 0b.
22 to 16	MSK_WE[38:32]	Enables write to MSK [38:32]. Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 7	—	Reserved. These bits are read as 0b. The write value should always be 0b.
6 to 0	MSK[38:32]	Controls masking of the external interrupt terminal bit[38:32]. 0b: Remove masking of the external interrupt signal. 1b: Mask the external interrupt signal.

Note: Bits whose multiplexed function is other than external interrupt should always mask the external interrupt signal.

41.5 Functional Description

This section describes the functions of the PFC unit.

The prefix (PFC_) of the register names is omitted in this and subsequent sections.

41.5.1 General-Purpose Input/Output Port (GPIO) Function

The PFC unit supports the general-purpose input/output port (GPIO) function.

When the multiplexed pin function in use is GPIO, the following register settings allow input/output control for the corresponding external pins.

The output level of the corresponding external pins can be changed by controlling the following registers.

- Pnn_GPIO_DO register: External pin output value control
- Pnn_GPIO_OE register: External pin output enable control

By controlling the following register, the input level of the corresponding external pins can be monitored via the Pnn_DI_MON register.

- Pnn_GPIO_IE register: External pin input enable control

Note: nn = 00 to 17, 20, 21

41.5.2 Multiplexed Pin Function Switching

The PFC unit is able to switch the multiplexed pin function for the external pins by the following register setting.

Table 41.1-3 lists the correspondence between the external pins and the assigned multiplexed pin functions.

- Pnn_PFSELx register: Multiplexed pin function switching

The PFC unit has the following registers to prevent propagation of glitches, which are generated when switching the multiplexed pin function by the Pnn_PFSEL0 to 3 registers, to the external pins and internal propagation of glitches.

- Pnn_DI_MSK register: Forcibly masking the inputs from the external pins (IO buffer).
- Pnn_EN_MSK register: Forcibly masking the input/output enable for the external pins (IO buffer).

Note: nn = 00 to 17, 20
x = 0 to 3

41.5.2.1 Pnn_EN_MSK (Input/Output Enable Masking) Register

The Pnn_EN_MSK register is used to prevent propagation of glitches, which are generated when switching the multiplexed pin function by the Pnn_PFSEL0 to 3 registers (for multiplexed pin function switching), to the external pins.

Setting the Pnn_EN_MSK register for masking forcibly disables the output enable signal (Pnn_OE_N) and input enable signal (Pnn_IE) for the I/O buffer of the corresponding eternal pins.

Figure 41.5-1 shows an example of output waveforms of Pnn_DO, Pnn_OE_N, and Pnn_IE when switching the multiplexed pin function.

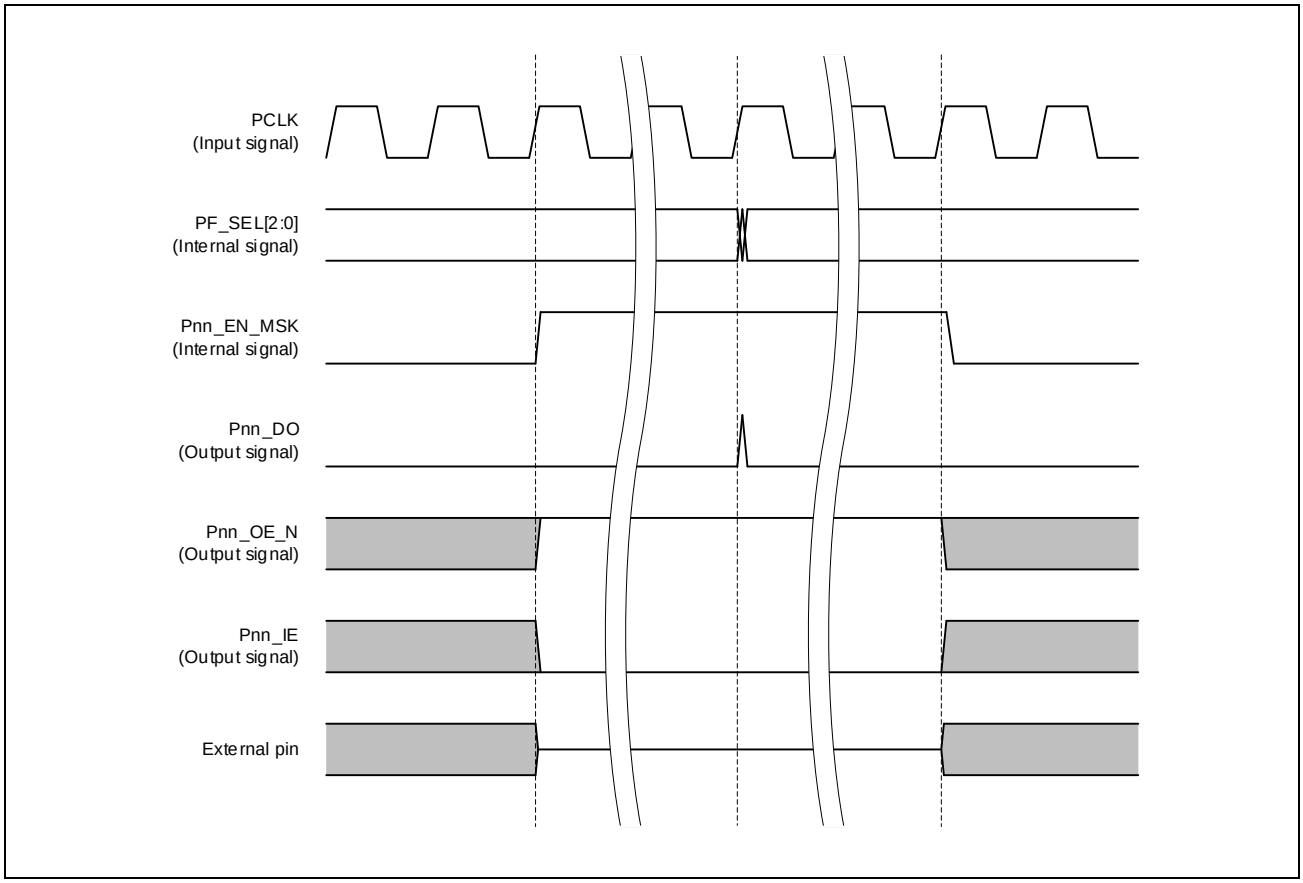


Figure 41.5-1 Example of Output Waveforms of Data and Enable Signals when Switching the Multiplexed Pin Function

41.5.2.2 Pnn_DI_MSK (Input Data Masking) Register

The Pnn_DI_MSK register is used to prevent internal propagation of glitches which are generated due to the effects of skew on Pnn_OE_N and Pnn_IE when setting input/output enable masking described in **Section 41.5.2.1, Pnn_EN_MSK (Input/Output Enable Masking)**. Setting the Pnn_DI_MSK register for masking forcibly masks the signals to be supplied to the internal unit.

The value of Pnn_PFx_DI when masking input data is the same value as the initial value. The initial values of the pins are listed in **Section 41.3.1, List of Pins**.

Figure 41.5-2 shows an example of output waveforms of Pnn_DO, Pnn_OE_N, and Pnn_IE when switching the multiplexed pin function.

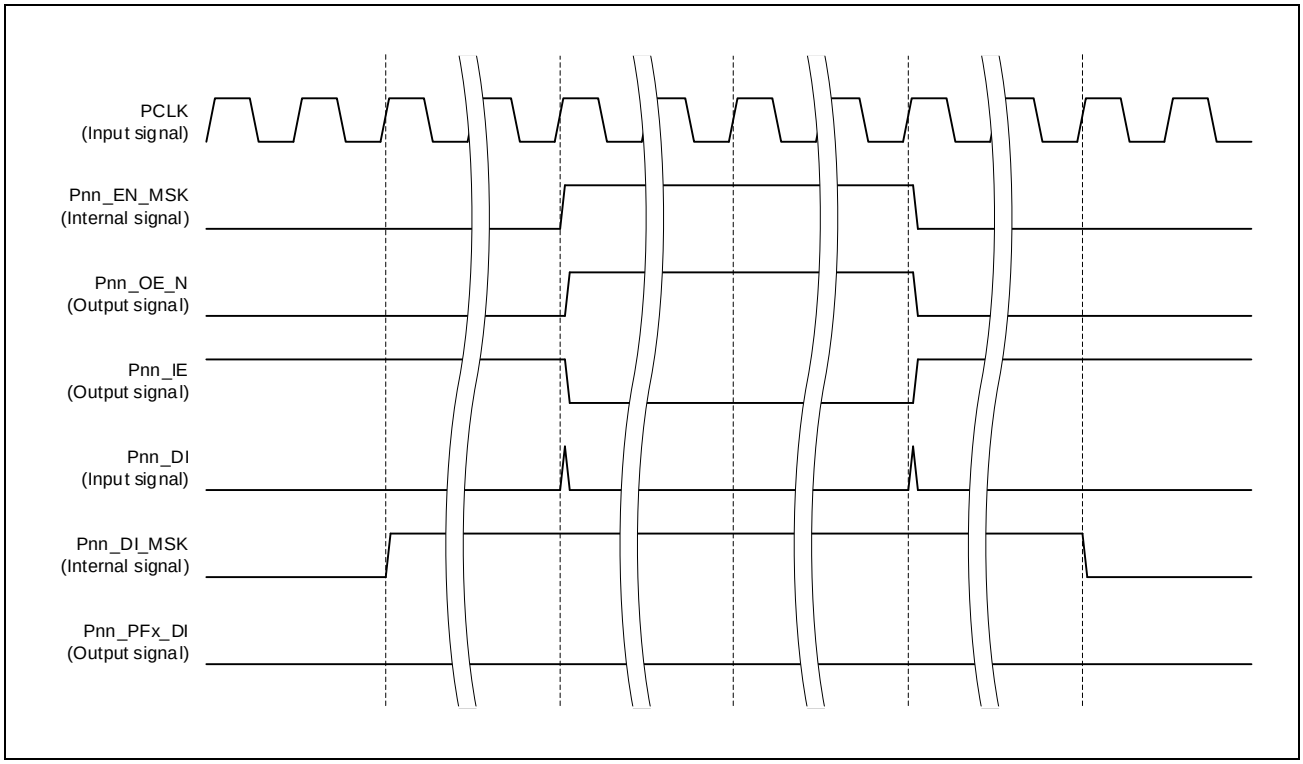


Figure 41.5-2 Example of Output Waveforms of Data when Switching Input/Output Enable Masking

41.5.3 Pin Function Control

The PFC unit is able to switch the pull-up/down, drive strength, and slew rate of the I/O buffer by using the following registers.

- Pnn_PUPD register: Pull-up/down switching
- Pnn_DRV register: Drive strength switching
- Pnn_SR register: Slew rate switching

Note: nn = 00 to 17, 20, 21

41.5.4 CSRXD Input Pin Selection

The setting of the Pnn_PFSELy register allows external pins CSRXDx and CSTXDx to switch the multiplexed pin function to the serial data input for the CSIx unit (CSRXDx). Switching the multiplexed pin function to the serial data input for the CSIx unit (CSRXDx) also requires setting the following registers in addition to changing the setting of the Pnn_PFSELy register.

- RXDx of the CSRXD_SEL register: Selection of the input for the CSIx unit (Select external pin CSRXDx or CSTXDx)

Note: nn = 03, 04
x = 0 to 5, y = 0 to 3

41.5.5 External Interrupt Signal Active Sense Inversion Control

The PFC unit is able to control whether or not to invert the active sense of the external interrupt signal.

Target: Pins whose multiplexed function is INEXINTn.

Note: n = 0 to 38

When the external interrupt signal is active low, the active sense of this signal can be inverted by using this function. The active-high interrupt signal can be conveyed to the interrupt controller (GIC) in accord with the specification of the interrupt controller (GIC)..

This can be controlled by the following register setting.

- EXTINT_INVx register: External interrupt signal active sense control

Note: x = 0 to 2

41.5.6 External Interrupt Signal Masking Control

The PFC unit is able to control whether or not to mask the external interrupt signal.

This function is used to prevent glitches when switching the multiplexed pin function and false detection of interrupts due to switching of the setting for active sense inversion of the interrupt.

Target: Pins whose multiplexed function is INEXINTn

CAUTION

Bits whose multiplexed function is other than external interrupt should always mask the external interrupt signal.

This can be controlled by the following register setting.

- EXTINT_MSKx register: External interrupt signal masking control

Note: n = 0 to 38
x = 0 to 2

41.6 Operating Procedure

41.6.1 Procedure for Writing to the Registers

The 16 higher-order bits of the bank address switching register are write enable and the 16 lower-order bits are normal data registers, so changing only the value of the specified bits is possible without read-modify-write operation.

When changing the value, write 1 to the bit plus 16 of the bit to be changed.

Example: To set bit[0] to 1b, write 0001_0001h. To set it to 0b, write 0001_0000h. The value of bit[15:0] is not changed when 0000_xxxxh is written. (x: Don't care)

- PORTnn GPIO output value control register (Pnn_GPIO_DO)
- PORTnn GPIO output control register (Pnn_GPIO_OE)
- PORTnn GPIO input control register (Pnn_GPIO_IE)
- PORTmm Function Select registers 0 to 3 (Pmm_PFSEL0 to 3)
- PORTnn slew rate switching register (Pnn_SR)
- CSRXD input pin switching register (CSRXD_SEL)
- External interrupt signal active sense inversion control registers 0 to 2 (EXTINT_INV0 to 2)
- External Interrupt Signal Mask Control registers 0 to 2 (EXTINT_MSK0 to 2)
- PORTmm input data masking register (Pmm_DI_MSK)
- PORTmm input/output enable masking register (Pmm_EN_MSK)

When read, the 16 higher-order bits are always read as 0b.

The following registers have no enable function for writing.

- PORTnn Pull-Up/Down Control register (Pnn_PUPD)
- PORTnn Drive Strength Control register (Pnn_DRV)
- Dedicated Drive Strength Control register (PEX0_DRV)

The following registers are read only and writing to these registers has no effect.

- PORTnn Input Value Monitor register (Pnn_DI_MON)

Note: nn = 00 to 17, 20, 21
mm = 00 to 17, 20

41.6.2 Initial Settings of Multiplexed Pins

41.6.2.1 Initial States of Pins

After release from the system reset, the individual pins are set as listed in **Table 41.6-1**.

Table 41.6-1 Settings after Release from the System Reset

Setting Item	Setting after Release from System Reset
Drive strength	The setting depends on the pin.*1
Pull-up/pull-down	The setting depends on the pin.*2
Multiplexed function	GPIO
Input data masking	Enable (masking enabled)
Input/output enable masking	Enable (masking enabled)
Slew rate	Slow slew

Note 1. For the settings for each pin, see the description of Pnn_DRV in **Section 41.4.2, Register Descriptions**.

Note 2. For the settings for each pin, see the description of Pnn_PUPD in **Section 41.4.2, Register Descriptions**.
nn = 00 to 17, 20, 21

Figure 41.6-1 shows the states of the pins at that time.

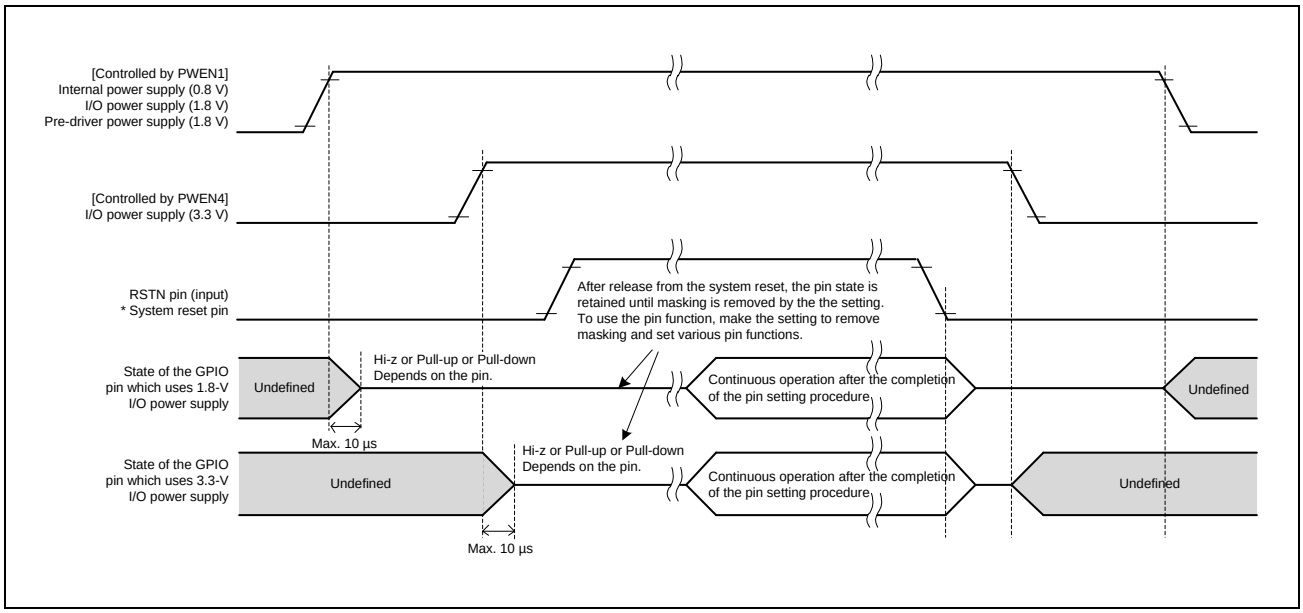


Figure 41.6-1 GPIO Pin States after Release from Reset and Setting

41.6.2.2 Procedure for Initial Settings of Pins

The following describes the procedure for controlling the pin functions and pin characteristics.

1. Set input data for masking (set the target bit of the Pnn_DI_MSK register of PFC).
2. Set input/output enable for masking (set the target bit of the Pnn_EN_MSK register of PFC).
3. Set pull-up or pull-down (set the target bit of the Pnn_PUPD register of PFC).
4. Set the drive strength (set the target bit of the Pnn_DRV register of PFC).
5. Select the multiplexed pin function (set the target bit of the Pnn_PFSEL register of PFC).
6. Remove masking of input/output enable (set the target bit of the Pnn_EN_MSK register of PFC).
7. Remove masking of input data (set the target bit of the Pnn_DI_MSK register of PFC).

For the setting registers, see **Section 41.4.2, Register Descriptions** and **Section 41.5.2, Multiplexed Pin Function Switching**.

When switching the multiplexed pin function to the function other than GPIO, follow the procedure described in **Section 41.6.3, Multiplexed Function Switching Procedure**.

41.6.3 Multiplexed Function Switching Procedure

Since the 3-bit select signal is used for switching of the multiplexed pin function, glitches may be generated due to skew on the select signal. Therefore, the following procedure must be observed to prevent propagation of glitches when switching the multiplexed pin function.

CAUTION

When switching the multiplexed pin function, only do so while the function of the related unit is stopped. Furthermore, operation of the unit after switching the multiplexed pin function must only be started after reading the register of this unit which was most recently set (to secure the time until the setting is reflected in the external pin).

41.6.3.1 Procedure for Switching Pins which Do Not Include External Interrupts (INEXINT0 to 38) as Multiplexed Function

1. Use the Pmm_DI_MSK register for setting to mask input data on the pins for multiplexed function switching.
2. Use the Pmm_EN_MSK register for setting to mask input/output enable for the pins for multiplexed function switching.
3. Use the Pmm_PFSEL0 to 3 registers to switch the multiplexed function.
4. Use the Pmm_EN_MSK register for setting to remove masking of input/output enable.
5. Use the Pmm_DI_MSK register for setting to remove masking of input data.

Note: mm = 00 to 17, 20

41.6.3.2 Procedure for Switching Pins which Include External Interrupts (INEXINT0 to 38) as Multiplexed Function

(1) Procedure for switching the multiplexed function other than external interrupt to external interrupt

1. Use the EXTINT_INV0 to 2 registers to set whether or not to invert the active sense of the external interrupt signal.
2. Set the multiplexed function as external interrupt through the procedure described in **Section 41.6.3.1, Procedure for Switching Pins which Do Not Include External Interrupts (INEXINT0 to 38) as Multiplexed Function**.
3. Use the EXTINT_MSK0 to 2 registers to remove masking of the external interrupt signal.

(2) Procedure for switching the multiplexed function from external interrupt to the function other than external interrupt

1. Use the EXTINT_MSK0 to 2 registers for setting to mask the external interrupt signal on the pins for multiplexed function switching.
2. Set the multiplexed function through the procedure described in **Section 41.6.3.1, Procedure for Switching Pins which Do Not Include External Interrupts (INEXINT0 to 38) as Multiplexed Function**.

(3) Procedure for switching the multiplexed function other than external interrupt to the function other than external interrupt

1. Set the multiplexed function through the procedure in **Section 41.6.3.1, Procedure for Switching Pins which Do Not Include External Interrupts (INEXINT0 to 38) as Multiplexed Function**.

41.6.4 CSRXD Input Pin Selection

Switching the multiplexed function to serial data input for the CSIx unit (CSRXDx) requires the following two steps.

- Set the multiplexed function to CSRXDx through the procedure described in **Section 41.6.3.1, Procedure for Switching Pins which Do Not Include External Interrupts (INEXINT0 to 38) as Multiplexed Function**.
- Use the CSRXD_SEL register to select the corresponding pins.

The above two steps can be performed in any order.

Note: x = 0 to 5

Example setting: When changing the external pin CSRXD0 to the serial data input for CSI0

- Set the multiplexed function of external pin CSRXD0 to CSRXD0 through the procedure described in **Section 41.6.3.1, Procedure for Switching Pins which Do Not Include External Interrupts (INEXINT0 to 38) as Multiplexed Function**.
- Set the CSRXD_SEL register to 0001_0000h.

41.6.5 Procedure for Switching the Active Sense of the External Interrupt Signal

Set whether or not to invert the active sense of the external interrupt signal as follows.

- When using an active-high signal as external interrupt signal:
  The setting is for non-inversion of the active sense.
- When using an active-low signal as external interrupt signal:
  The setting is for inversion of the active sense.

Furthermore, when switching the active sense of the signal while external interrupt is selected as the multiplexed function, the following procedure must be observed to prevent false detection of external interrupts.

1. Use the EXTINT_MSK0 to 2 registers to mask the external interrupt on the target pins for active sense switching.
2. Use the EXTINT_INV0 to 2 registers to set whether or not to invert the active sense of the external interrupt signal.
3. Use the EXTINT_MSK0 to 2 registers to remove masking of the external interrupt on the target pins for active sense switching.

41.7 Usage Notes

- When setting the pin functions and pin characteristics, read the registers after writing to them and check that the values have been set before using the pins.
- For the pins for which the multiplexed function other than external interrupt is selected, always mask the external interrupt signal.
- For the MD4-MD7 pins, provide a mechanism for switching the high and low level for the input outside the LSI chip.

Section 42 Motor Controller (MTR)

This section describes the functions of the motor controller (MTR).

42.1 Functional Overview

The MTR is a unit for optical motor control.

- Driving pulse output for stepping motors
- 4-wire clock synchronous serial communications

For information on motor control, contact a Renesas Electronics sales representative.

Section 43 Environment Sensor Interface (ESI)

This section describes the functions of the environment sensor interface (ESI).

43.1 Functional Overview

The ESI repeatedly communicates with external devices at desired set intervals and transfers the acquired data to memory (DRAM) in order by using the DMA function.

The ESI is also connected to an A/D converter (ADCA, ADCB) and transfers the acquired results of AD conversion to memory (DRAM).

The ESI is connected to the external devices via a 4-wire clock synchronous serial interface (SPI).

Specifications of SPI communications

- Method of communications: SPI (CS/SCLK/TXD/RXD)
- Operating mode: Master mode only
- Serial clock: Up to 24 MHz (24/N MHz (N = 1 to 48))
- Chip select lines: 4 (CS0/CS1/CS2/CS3)
- Selection of the active sense of CS, CLK, and data and timing adjustment.
- Either LSB first or MSB first is selectable for the transmission and reception of data.

For information on the environment sensor interface (ESI), contact a Renesas Electronics sales representative.

Section 44 Display Control

This section describes the overview of the display control of this LSI.

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

44.1 Connection Configuration

The display control is composed of a display control unit (DCU), an HDMI Tx interface (HDMI), and an LCD control interface (LCI). **Figure 44.1-1** shows the internal connection configuration with the DCU, HDMI, and LCI.

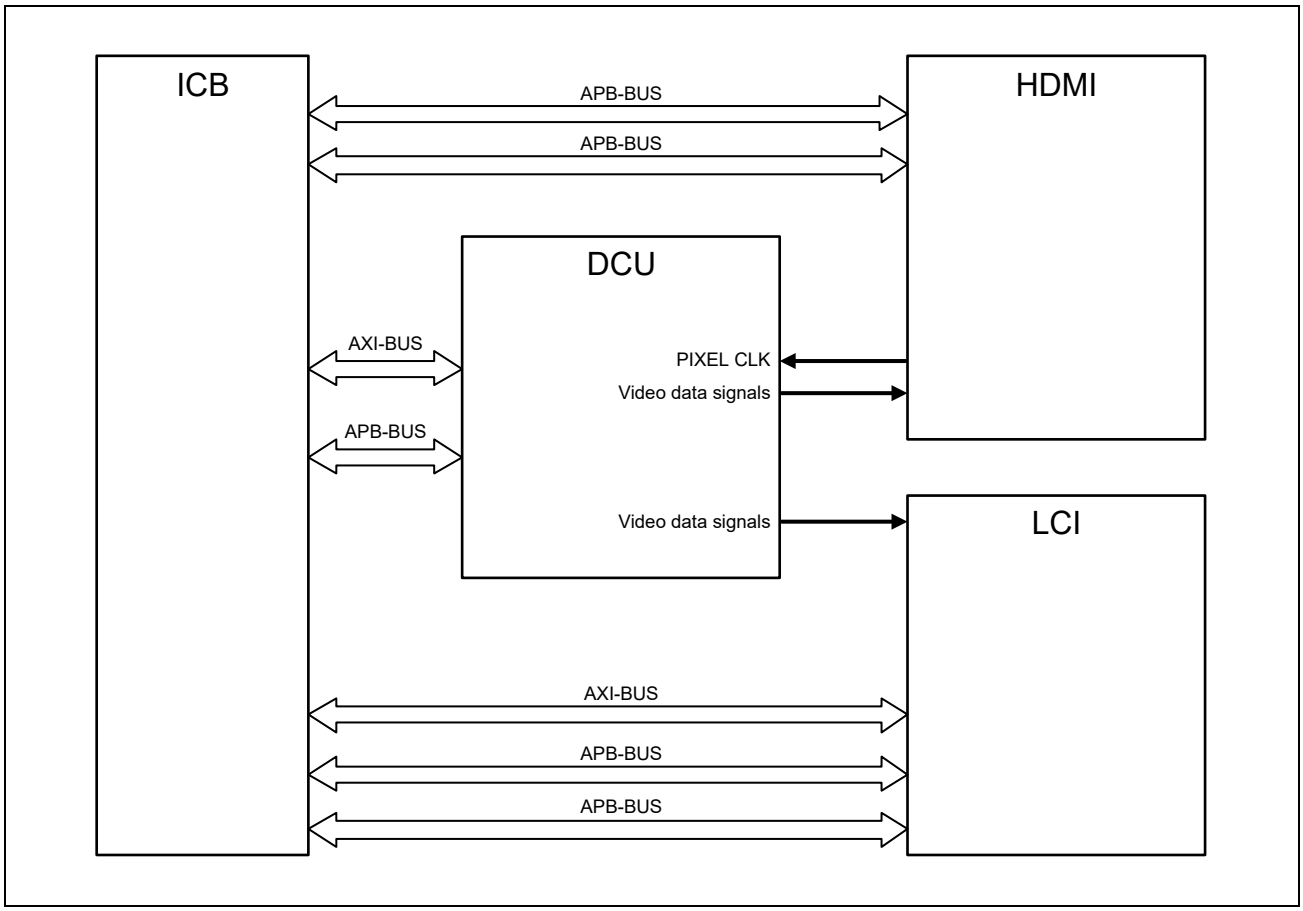


Figure 44.1-1 Internal Connection Configuration with DCU, HDMI, and LCI

44.2 Display Control Unit (DCU)

This section describes the functions of the display control unit (DCU).

44.2.1 Functional Overview

The DCU is a control unit for reading display data from the external LPDDR4 based on the display output timing.

The MIPI DSI display output and HDMI display output are handled through the LCD control interface (LCI) and the HDMI Tx interface, respectively.

44.2.2 Features

- Maximum display size
  - MIPI DSI: 1920 × 1080 p × 60 fps, 1080 × 1920 p × 60 fps
  - HDMI: 1920 × 1080 p × 60 fps
- Resolution conversion
  - Image frame: Reduction by linear interpolation
  - Graphics frame: Expansion by simple interpolation
- Picture compositing
  - The image frame is assigned as the background and the graphics frame is assigned as the foreground.
  - For a single MIPI DSI or HDMI display
    - Two display areas (DRAMs) are used for each of the image and graphics screens.
    - Two image frames can be combined at a specified level, after which a composite is output with the given alpha values.
  - For simultaneous display via the MIPI DSI and HDMI
    - One display area (DRAM) is used for each of the image and graphics screens.
    - A composite is output with the given alpha values.
- Image frame adjustment
  - Brightness and chroma
- Dedicated image adjustment for the MIPI DSI
  - Color gain, color temperature, gamma correction, and YUV to RGB conversion
- Dedicated image adjustment for HDMI
  - Color gain, color conversion, and brightness offset

44.2.3 Operating Procedure

For the HDMI, an API for display in the HDMI device in combination with the DCU is defined. For details, refer to the ISP control software specification. For the LCI, contact a Renesas Electronics sales representative as it is supported individually.

44.3 LCD Control Interface (LCI)

This section describes the functions of the LCD control interface (LCI).

44.3.1 Functional Overview

The LCI is composed of a link and a MIPI D-PHY Tx circuit for a MIPI Display Serial Interface (DSI). It handles display output that is conformant with the following MIPI specifications.

- MIPI Alliance Specification for Display Serial Interface, Version 1.3.1
- MIPI Alliance Specification for D-PHY, Version 1.1

44.4 HDMI Tx Interface (HDMI)

This section describes the functions of the HDMI Tx interface.

44.4.1 Functional Overview

The HDMI handles display output that is conformant with the HDMI specification, version 1.4a and the DVI specification, version 1.0.

44.4.2 Features

Table 44.4-1 lists the functions of the HDMI

Table 44.4-1 List of the Functions

Block Name	Category	Item	Specification
LINK	Image	Resolution	1280 × 720p 1920 × 1080p
		Output format	YUV 444, YUV422
		Color depth (per primary color)	8 bits
		Color space converter	BT601 to BT709 conversion
	Audio	Interface	I2S
		Number of channels	2 ch.
		Sampling frequency	32 kHz, 44.1 kHz, 48 kHz
		Encoding method	LPCM (Linear PCM)
		Number of quantization bits	16 bits, 24 bits
	Interrupt		Hot plug detection (sink device detection) VSYNC detection Error detection interrupt
PHY	Operating frequency		Up to 2.97 Gbps

The following functions are not supported.

- CEC, HDCP, HEAC

Table 44.4-2 lists the image formats supported by the HDMI.

Table 44.4-2 List of the Supported Image Formats

Image Size	Frame Rate (Hz)
1280 × 720 p	60.000
1920 × 1080 p	60.000

Section 45 Trusted Secure IP

For the security functions, contact a Renesas Electronics sales representative.

Section 46 A/D Converter (ADCA, ADCB)

This section describes the functions of the A/D converter units A and B (ADCA, ADCB).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

46.1 Functional Overview

This LSI chip incorporates two 12-bit successive-approximation A/D converter units. Up to 12 channels of analog input are selectable for unit A and up to eight channels are selectable for unit B. The A/D converter units A and B operate independently.

- Number of units: 2
- Input channels: 12 (unit A) and 8 (unit B)
- Resolution: 12 bits
- Sampling rate: 600 kS/s
- Operating modes
  - Single scan
  - Continuous scan
  - ESI continuous scan

Section 47 Temperature Sensor (TSU)

This section describes the functions of the temperature sensor (TSU).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

47.1 Functional Overview

This LSI has two channels, ch. 0 and ch. 1, of TSU.

The temperature in this LSI can be obtained by reading the digital values to which the temperature sensor outputs were converted by the A/D converters.

Section 48 Clock Pulse Generator (CPG)

This section describes the functions of the clock pulse generator (CPG).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

48.1 Functional Overview

The CPG includes a clock generation block, a reset generation block, and an APB IF block, and supplies clocks and resets to the respective units.

Table 48.1-1 is an overview of the functions.

Table 48.1-1 Function Overview

Item	Specification
Clock generation and control functions	• This function divides the external input clock (oscillator (OSC48M) 48 MHz) or the PLL output clock to generate the clock to be supplied to the respective unit. • Six PLLs are installed. The roles of these PLLs are as follows.*1 PLL1 (SSCG-PLL): For CA53 PLL2 (SSCG-PLL): For SYSTEM BUS/ISP PLL3 (SSCG-PLL): For LPDDR4 PLL4 (Fractional-PLL): For STG, MTR, ADC PLL6 (SSCG-PLL): For DRP-AI PLL7 (SSCG-PLL): For the display control • The PLL oscillation frequency setting, clock division ratio setting, and output clock selection can be set by registers. • This function generates bus clock enable signals for individual units that require bus clock enable.
Reset generation and control functions	• This function generates a reset from the respective reset factors. The types of resets are as follows. 1. System reset 2. Debugger reset 3. Software control reset (individual unit reset by setting CPG register)

Note 1. In this LSI, PLL1, PLL2, PLL4, PLL6, and PLL7 are for use with the ISP support package. Therefore, do not write to the target registers. In addition, the target registers of PLL3 should not be rewritten because changing the LPDDR4 operation frequency after startup is prohibited.

Some tables and figures of this section are color-coded as information of the power domain.

The color coding by power domain is shown in **Table 48.1-2**.

Table 48.1-2 Color Coding by Power Domain

Power Domain	Description
PD_AWO	The power domain that is always powered on
PD_MEM	The power domain of the LPDDR4 systems
PD_VIDEO0	The power domain of the VIDEO0 systems
PD_VIDEO1	The power domain of the VIDEO1 systems
PD_RFX	The power domain of the RAMB systems
PD_DRPA	The power domain of the DRA-AI systems
PD_CA53	The power domain of the CA53 systems

48.2 Pin Functions

Table 48.2-1 lists the external pins of the CPG.

Table 48.2-1 List of External I/O Pins

Pin Name	I/O	Function
RSTN	Input	External system reset
DESRSTN	Input	System reset from the debugger
DETRSTN	Input	System reset from the debugger TAP reset from the debugger
DETCK	Input	JTAG clock input (50 MHz)
GMCLK0	Output	GM clock output 0
GMCLK1	Output	GM clock output 1
AUPLLCLK	Input	Audio master clock input (Max. 12.288 MHz)
AUMCLK	Output	Audio master clock output (12 MHz)

Note: The external pins are connected through the external connection unit.

48.3 Clocks

48.3.1 Clock System Diagram

Figure 48.3-1 shows a simplified clock system diagram.

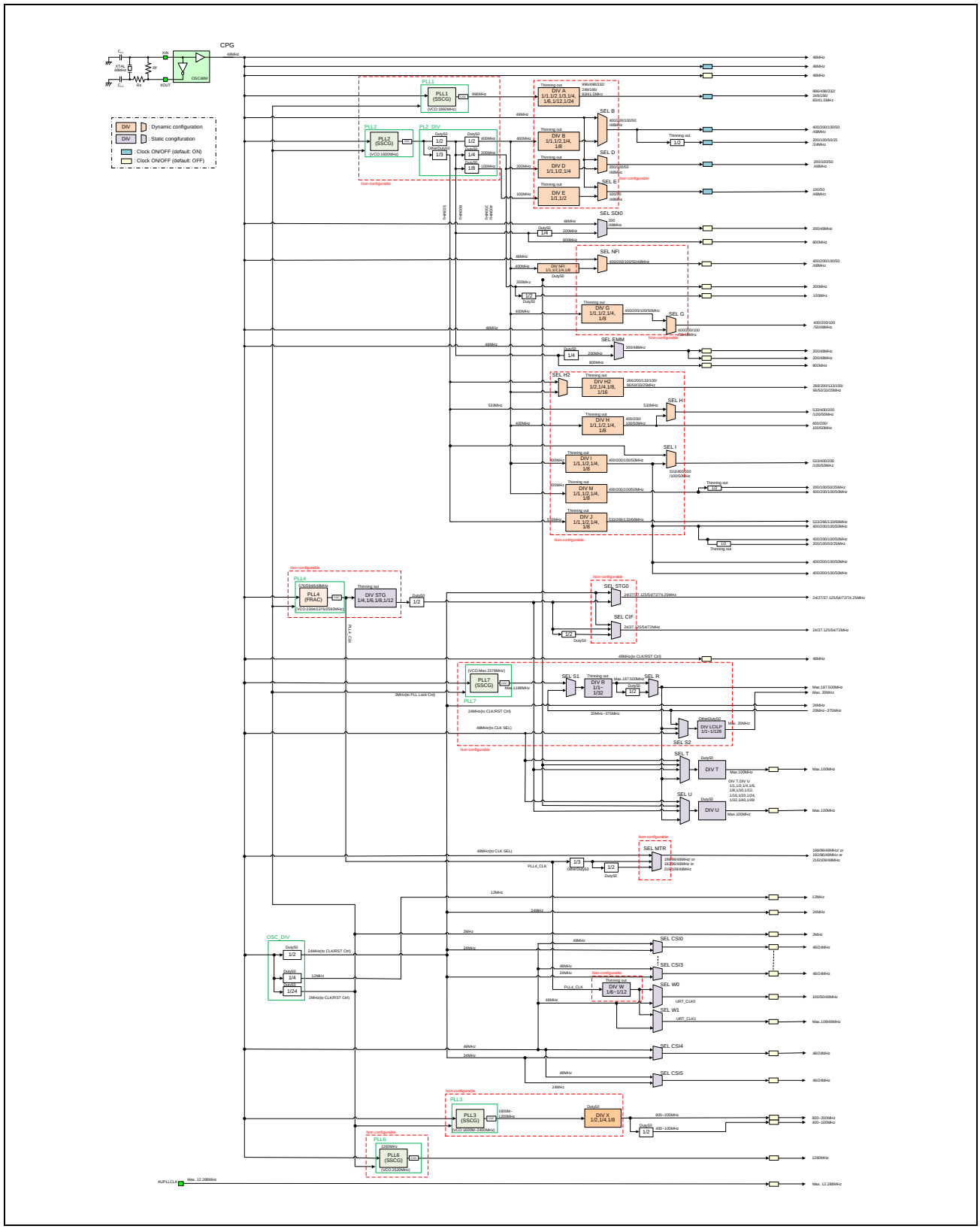


Figure 48.3-1 CPG Simplified Clock System Diagram

48.3.2 List of Clock Signals

Table 48.3-1 is a list of clock signals.

Table 48.3-1 List of Clock Signals (1/4)

Unit	Signal Name	Frequency [MHz]	Initial Value [MHz]	Clock Source	Value after Reset	Description
PMC	PMC_CORE_CLOCK	48	48	OSC48M	ON	PMC core clock
CST	CST_CS_CLK	400/200/100/50/48	200	SEL B	ON	CoreSight main clock
	CST_TS_CLK	48	48	OSC48M	ON	CST timestamp clock
	CST_TRACECLK	100/50/48	100	SEL E	ON	CST trace clock
	CST_SB_CLK	200/100/50/48	200	SEL D	ON	Clock for CST DebugAPB (system bus ↔ CoreSight)
	CST_AHB_CLK	48	48	OSC48M	ON	Clock for CST AHB (authentication circuit ↔ CoreSight)
	CST_APB_CA53_CLK	400/200/100/50/48	200	SEL B	ON	Clock for CST CA53_DebugAPB
	CST_ATB_SB_CLK	200/100/50/48	200	SEL D	ON	System bus synchronization clock for CST ATB bus
	CST_TS_SB_CLK	200/100/50/48	200	SEL D	ON	Timestamp clock for CST system bus
GIC	GIC_CLK	200/100/50/25/24	100	SEL B/2	ON	GIC common clock (for AXI and other I/Fs)
DMAC	DMAA_ACLK	200/100/50/48	200	SEL D	ON	DMAC AXI clock
RAMA	RAMA_ACLK	400/200/100/50/48	200	SEL B	ON	RAMA AXI clock
ROM	ROM_ACLK	200/100/50/48	200	SEL D	ON	ROM AXI clock
PCIe*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
SDI0*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
SDI1*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
eMMC*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
NAND*1	—	—	—	—	—	—
	—	—	—	—	—	—
USB*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
SEC	SEC_ACLK	200/100/50/48	200	SEL D	ON	Clock for SEC ACLK
	SEC_PCLK	200/100/50/48	200	SEL D	ON	Clock for SEC PCLK
	SEC_TCLK	200/100/50/48	200	SEL D	ON	Clock for SEC TCLK and TSIPG

Table 48.3-1 List of Clock Signals (2/4)

Unit	Signal Name	Frequency [MHz]	Initial Value [MHz]	Clock Source	Value after Reset	Description
ETHER*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
AUI*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
ADCA*1	—	—	—	—	—	—
	—	—	—	—	—	—
ADCB*1	—	—	—	—	—	—
	—	—	—	—	—	—
MTR*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
ISP*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
CPU Peripheral	CPERI_GRPA_PCLK	100/50/48	100	SEL E	Stop0	CPU Peripheral group A (TIM0-7) APB clock
	CPERI_GRPB_PCLK	100/50/48	100	SEL E	Stop0	CPU Peripheral group B (TIM8-15) APB clock
	CPERI_GRPC_PCLK	100/50/48	100	SEL E	Stop0	CPU Peripheral group C (TIM16-23) APB clock
	CPERI_GRPD_PCLK	100/50/48	100	SEL E	Stop0	CPU Peripheral group D (TIM24-31) APB clock
	CPERI_GRPE_PCLK	100/50/48	100	SEL E	Stop0	CPU Peripheral group E (PWM0-7) APB clock
	CPERI_GRPF_PCLK	100/50/48	100	SEL E	Stop0	CPU Peripheral group F (PWM8-15) APB clock
	CPERI_GRPG_PCLK	100/50/48	100	SEL E	Stop0	CPU Peripheral group G (CSI0-3) APB clock
	CPERI_GRPH_PCLK	100/50/48	100	SEL E	Stop0	CPU Peripheral group H (CSI4-5) APB clock
TIM	TIM_CLK[7:0]	2	2	OSC48M/24	Stop0	TIM clock
	TIM_CLK[15:8]	2	2	OSC48M/24	Stop0	TIM clock
	TIM_CLK[23:16]	2	2	OSC48M/24	Stop0	TIM clock
	TIM_CLK[31:24]	2	2	OSC48M/24	Stop0	TIM clock
PWM	PWM_CLK[7:0]	48	48	OSC48M	Stop0	PWM clock
	PWM_CLK[15:8]	48	48	OSC48M	Stop0	PWM clock
CSI	CSI_CLK[5:0]	48/24	24	SEL CSIx	Stop0	Master clock in CSI master mode
IIC	IIC_PCLK[0]	100/50/48	100	SEL E	Stop0	IIC APB clock
	IIC_PCLK[1]	100/50/48	100	SEL E	Stop0	IIC APB clock
UART	URT_PCLK	100/50/48	100	SEL E	Stop0	UART0,1 common APB clock
	URT_CLK[1:0]	max108/48	48	SEL W0/W1	Stop0	UART serial clock
WDT	WDT_PCLK[0]	100/50/48	100	SEL E	ON	WDT0 APB clock
	WDT_PCLK[1]	100/50/48	100	SEL E	ON	WDT1 APB clock
	WDT_CLK[0]	48	48	OSC48M	ON	WDT0 clock
	WDT_CLK[1]	48	48	OSC48M	ON	WDT1 clock

Table 48.3-1 List of Clock Signals (3/4)

Unit	Signal Name	Frequency [MHz]	Initial Value [MHz]	Clock Source	Value after Reset	Description
PFC	PFC_PCLK	48	48	OSC48M	ON	PFC APB clock
GRP*1	—	—	—	—	—	—
DCU*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
LCI*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
HDMI*1	—	—	—	—	—	—
SYC	SYC_CNT_CLK	24	24	OSC48M/2	Stop0	SYC clock
SYS	SYS_CLK	48	48	OSC48M	ON	SYS clock
TSU0	TSU0_PCLK	48	48	OSC48M	ON	TSU0 APB clock
TSU1	TSU1_PCLK	48	48	OSC48M	ON	TSU1 APB clock
ESI*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
CIF*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
CA53	CA53_CLK	996/498/332/249/166/83/41.5	249	DIV A	ON	CA53 main clock
	CA53_APCLK_DBG	400/200/100/50/48	200	SEL B	ON	Clock for CA53 Debug APB
	CA53_ACLK	400/200/100/50/48	200	SEL B	ON	Clock for CA53 ACE (AXI)
	CA53_ATCLK	400/200/100/50/48	200	SEL B	ON	Clock for CA53 ATB (AMBA Trace Bus)
	CA53_TSCLK	48	48	OSC48M	ON	Clock for CA53 timestamp
	CA53_APCLK_REG	200/100/50/48	200	SEL D	ON	Clock for CA53 register access (GLUE) APB
LPDDR4 *1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
STG*1	—	—	—	—	—	—
	—	—	—	—	—	—
ISP*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
GPA*1	—	—	—	—	—	—
JPG*1	—	—	—	—	—	—
	—	—	—	—	—	—
VCD*1	—	—	—	—	—	—
	—	—	—	—	—	—

Table 48.3-1 List of Clock Signals (4/4)

Unit	Signal Name	Frequency [MHz]	Initial Value [MHz]	Clock Source	Value after Reset	Description
ISP*1	—	—	—	—	—	—
	—	—	—	—	—	—
	—	—	—	—	—	—
GPA*1	—	—	—	—	—	—
MTD*1	—	—	—	—	—	—
	—	—	—	—	—	—
RAMB	RAMB_ACLK[3:0]	400/200/100/50/48	400	SEL G	Stop0	RAMB AXI clock
DRP-AI	DRPA_ACLK	400/200/100/50/48	200	SEL B	Stop0	DRP-AI AXI clock
	DRPA_DCLK	1260	1260	PLL6	Stop0	DRP-AI divided clock
	DRPA_INITCLK	48	48	OSC48M	Stop0	DRP-AI reset assert clock
ICB	ICB_ACLK1	400/200/100/50/48	200	SEL B	ON	ICB main clock
	ICB_CST_CS_CLK	400/200/100/50/48	200	SEL B	ON	CST_CS_CLK for ICB
	ICB_DRPA_ACLK	400/200/100/50/48	200	SEL B	ON	DRPA_ACLK for ICB
	ICB_GIC_CLK	200/100/50/25/24	100	SEL B/2	ON	GIC_CLK for ICB
	ICB_MPCLK1	200/100/50/48	200	SEL D	ON	ICB PD_AWO Middle Frequency clock
	ICB_CST_ATB_SB_CLK	200/100/50/48	200	SEL D	ON	ON CST_ATB_SB_CLK for ICB
	ICB_SPCLK1	100/50/48	100	SEL E	ON	ICB PD_AWO Slow Frequency clock
	ICB_DCI_CLKAXI	400/200/100/50	400	DIV I	ON	DCI_CLKAXI for ICB
	ICB_CLK100_1	100	100	PLL2/16	ON	ICB PD_AWO fixed 100 MHz clock
	ICB_ETH0_CLK_AXI	200	200	PLL2/8	ON	ETH0_CLK_AXI for ICB
	ICB_CLK48	48	48	OSC48M	ON	ICB PD_AWO domain fixed 48 MHz clock
	ICB_SYC_CNT_CLK	24	24	OSC48M/2	ON	SYC_CNT_CLK for ICB
	ICB_CLK48_2	48	48	OSC48M	Stop0	ICB PD_MEM fixed 48 MHz clock
	ICB_MMC_ACLK	400~100	400	DIV X/2	Stop0	MMC_ACL for ICB
	ICB_CLK48_3	48	48	OSC48M	Stop0	ICB PD_VIDEO0 fixed 48 MHz clock
	ICB_MPCLK3	200/100/50/48	200	SEL D	Stop0	ICB PD_VIDEO0 Middle Frequency clock
	ICB_CIMA_CLK	533/400/200/100/50	400	SEL H	Stop0	CIMA_CLK for ICB
	ICB_CIMB_CLK	400/200/100/50	400	DIV H	Stop0	CIMB_CLK for ICB
	ICB_CLK48_4L	48	48	OSC48M	Stop0	ICB PD_VIDEO1_0 fixed 48 MHz clock
	ICB_CLK48_4R	48	48	OSC48M	Stop0	ICB PD_VIDEO1_1 fixed 48 MHz clock
	ICB_MPCLK4	200/100/50/48	200	SEL D	Stop0	ICB PD_VIDEO1 Middle Frequency clock
	ICB_VD_ACLK4	400/200/100/50	400	DIV I	Stop0	ACLK for ICB PD_VIDEO1
	ICB_BIMA_CLK	533/400/200/100/50	400	SEL I	Stop0	BIMA_CLK for ICB
	ICB_VCD_PCLK4	200/100/50/25	200	DIV I/2	Stop0	VCD APB clock for ICB
	ICB_MTD_CLKAXI	400/200/100/50	400	DIV M	Stop0	MTD_CLKAXI for ICB
	ICB_CLK48_5	48	48	OSC48M	Stop0	ICB PD_RFX fixed 48 MHz clock
	ICB_RFX_ACLK5	400/200/100/50/48	400	SEL G	Stop0	ICB PD_RFX AXI clock
	ICB_RFX_PCLK5	200/100/50/48	200	SEL G	Stop0	ICB PD_RFX APB clock
JTAG	TCK	Max. 50	50	DETCK	ON	JTAG clock output (50 MHz)
External output clock	AUMCLK	12	12	OSC48M/4	Stop0	Audio master clock output (12 MHz)
	GMCLK0	Max. 100	48	DIV T	Stop0	GM clock output 0
	GMCLK1	Max. 100	48	DIV U	Stop0	GM clock output 1

Note 1. For more information, contact a Renesas Electronics sales representative.

48.4 Reset

48.4.1 Reset System Diagram

Figure 48.4-1 shows the reset system diagram.

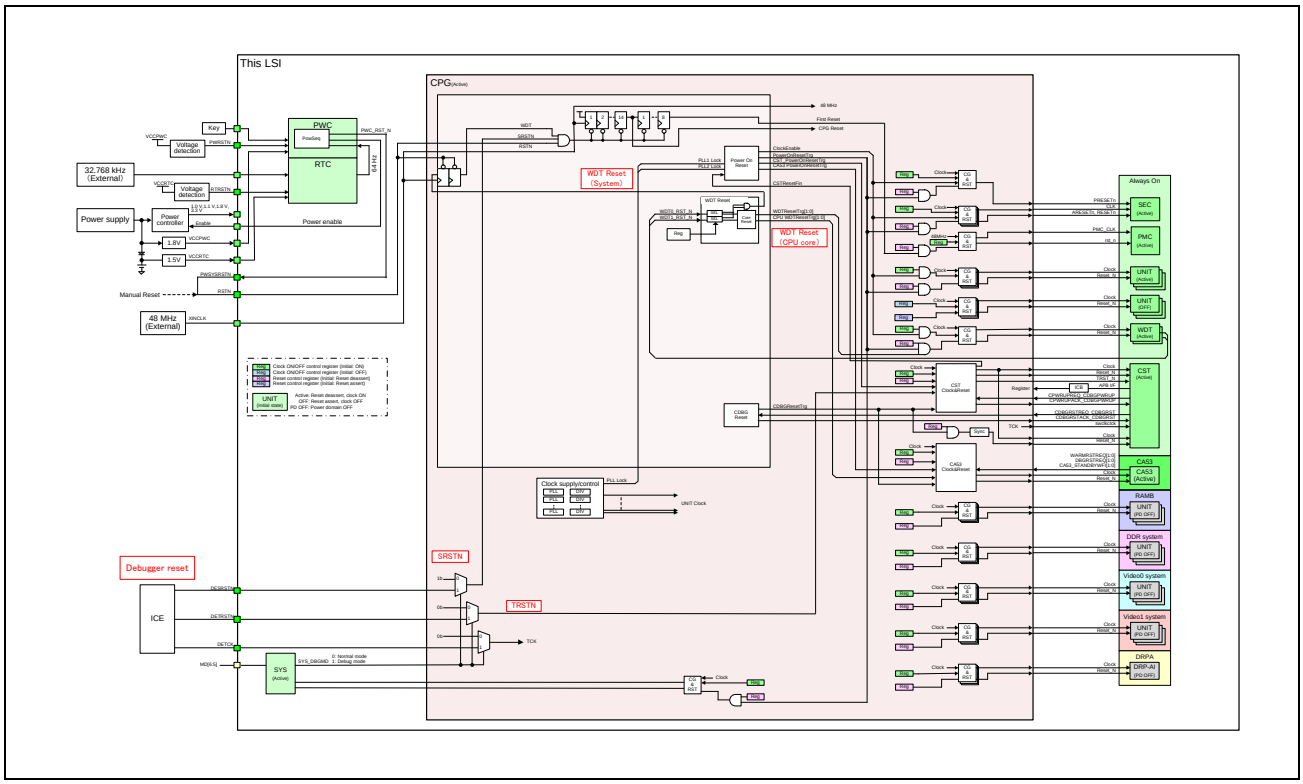


Figure 48.4-1 Reset System Diagram

48.4.2 List of Reset Signals

Table 48.4-1 lists the reset signals for respective units.

Table 48.4-1 List of Reset Signals (1/4)

Unit	Signal Name	Reset Control Type*1	Minimum Assertion Period*2	De-assertion Delay for Target Unit*2	Description	Remarks
CA53	CA53_NCPUPORESET[0]	CA53 Reset	3*CA53_CLK	11*CA53_CLK	CA53 Processor powerup reset (Core 0)	
	CA53_NCPUPORESET[1]		3*CA53_CLK	11*CA53_CLK	CA53 Processor powerup reset (Core 1)	
	CA53_NCORERESET[0]		3*CA53_CLK	11*CA53_CLK	CA53 Individual core reset (Core 0)	
	CA53_NCORERESET[1]		3*CA53_CLK	11*CA53_CLK	CA53 Individual core reset (Core 1)	
	CA53_NPRESETDBG		3*CA53_CLK	The later of 8*CA53_CLK or 4*CA53_ATCLK+4*CA53_CLK or 4*CA53_APCLK_DBG+4*CA53_CLK or 4*CA53_TSCLK+4*CA53_CLK	CA53 APB reset	
	CA53_L2RESET		3*CA53_CLK	11*CA53_CLK	CA53 L2 memory system reset	
	CA53_NMISCRESET_HM		1*CA53_CLK	4*CA53_CLK	CA53 MISC reset(HM)	
	CA53_NMISCRESET_SM		1*CA53_APCLK_REG	3*CA53_APCLK_REG	CA53 MISC reset (SM)	
	CA53_NARESET		2*CA53_ACLK	4*CA53_ACLK+4*CA53_CLK	CA53 AXI reset	
RAMB	RAMB_ARESETN[3:0]	TYPE-B	A+5*RAMB_ACLK	A+7*RAMB_ACLK	RAMB reset	Common to RAMB[3:0]
CST	CST_NTRST	CST Reset	—	—	CST reset	
	CST_NPOTRST		—	—	CST reset	
	CST_CS_RESETN		1*CST_CS_CLK	1*CST_CS_CLK	CST reset	
	CST_TS_RESETN		1*CST_TS_CLK	1*CST_TS_CLK	CST reset	
	CST_TRESETN		1*CST_TRACECLK	1*CST_TRACECLK	CST reset	
	CST_SB_RESETN		1*CST_SB_CLK	1*CST_SB_CLK	CST reset	
	CST_AHB_RESETN		1*CST_AHB_CLK	1*CST_AHB_CLK	CST reset	
	CST_APB_CA53_RESETN		1*CST_APB_CA53_CLK	1*CST_APB_CA53_CLK	CST reset	
	CST_ATB_SB_RESETN		1*CST_ATB_SB_CLK	1*CST_ATB_SB_CLK	CST reset	
	CST_TS_SB_RESETN		1*CST_TS_SB_CLK	1*CST_TS_SB_CLK	CST reset	
PMC	PMC_RESET_N	TYPE-B	A+4*PMC_CORE_CLOCK	A+4*PMC_CORE_CLOCK	PMC reset	
CPG	CPG internal reset	TYPE-A	—	—	—	Reset by CPG_PLLn_CCTRL_RST (n: 1 to 4, 7)
GIC	GIC_NRESET	TYPE-B	A+5*GIC_CLK	A+7*GIC_CLK	GIC reset	Common to RST_N
DMAC	DMAA_ARESETN	TYPE-B	A+5*DMAA_ACLK	A+7*DMAA_ACLK	DMAC reset	
RAMA	RAMA_ARESETN	TYPE-B	A+5*RAMA_ACLK	A	RAMA reset	
ROM	ROM_ARESETN	TYPE-B	A+5*ROM_ACLK	A+7*ROM_ACLK	ROM reset	
PCIe*3	—	—	—	—	—	

Table 48.4-1 List of Reset Signals (2/4)

Unit	Signal Name	Reset Control Type*1	Minimum Assertion Period*2	De-assertion Delay for Target Unit*2	Description	Remarks
SDI0*3	—	—	—	—	—	
SDI1*3	—	—	—	—	—	
eMMC*3	—	—	—	—	—	
NAND*3	—	—	—	—	—	
	—	—	—	—	—	
USB*3	—	—	—	—	—	
	—	—	—	—	—	
	—	—	—	—	—	
	—	—	—	—	—	
SEC	SEC_ARESETN	TYPE-A	—	—	SEC AXI reset	
	SEC_PRESETN	TYPE-A	—	—	SEC APB reset	
	SEC_RSTB	TYPE-B	A+8*SEC_TCLK	A+4*SEC_TCLK	SEC reset	
ETHER*3	—	—	—	—	—	
AUI*3	—	—	—	—	—	
MTR*3	—	—	—	—	—	
ADCA*3	—	—	—	—	—	
ADCB*3	—	—	—	—	—	
ISP*3	—	—	—	—	—	
TIM	TIM_GPA_PRESETN	TYPE-A	—	2*CPERI_GRPA_PCLK+2*TIM_CLK	TIM group A reset (Common to [7:0])	Common to TIM[7:0]
	TIM_GPB_PRESETN	TYPE-A	—	2*CPERI_GRPB_PCLK+2*TIM_CLK	TIM group B reset (Common to [15:8])	Common to TIM[15:8]
	TIM_GPC_PRESETN	TYPE-A	—	2*CPERI_GRPC_PCLK+2*TIM_CLK	TIM group C reset (Common at [23:16])	Common to TIM[23:16]
	TIM_GPD_PRESETN	TYPE-A	—	2*CPERI_GRPD_PCLK+2*TIM_CLK	TIM group D reset (Common [31:24])	Common to TIM[31:24]
PWM	PWM_GPE_PRESETN	TYPE-B	The later of A+5*CPERI_GRPE_PCLK or A+ 5* PWM_CLK	The later of A+6*CPERI_GRPE_PCLK or A+ 6* PWM_CLK	PWM group E reset (Common to [7:0])	Common to PWM[7:0]
	PWM_GPF_PRESETN	TYPE-B	The later of A+5*CPERI_GRPF_PCLK or A+5* PWM_CLK	The later of A+6*CPERI_GRPF_PCLK or A+6* PWM_CLK	PWM group F reset (Common to [15:8])	Common to PWM[15:8]
CSI	CSI_GPG_PRESETN	TYPE-B	A+6*CPERI_GRPG_PCLK	A+6*CPERI_GRPG_PCLK	CSI group G reset (Common to [3:0])	Common to CSI[3:0]
	CSI_GPH_PRESETN	TYPE-B	A+6*CPERI_GRPH_PCLK	A+6*CPERI_GRPH_PCLK	CSI group H reset (Common to [5:4])	Common to CSI[5:4]
IIC	IIC_GPA_PRESETN	TYPE-A	—	—	IIC group A reset (Common to [1:0])	Common to IIC[1:0]
	IIC_GPB_PRESETN	TYPE-A	—	—	IIC group B reset (Common to [3:2])	Common to IIC[3:2]

Table 48.4-1 List of Reset Signals (3/4)

Unit	Signal Name	Reset Control Type*1	Minimum Assertion Period*2	De-assertion Delay for Target Unit*2	Description	Remarks
UART	URT_PRESETN	TYPE-B	The later of A+6*URT_PCLK or A+6*URT_CLK	The later of A+6*URT_PCLK or A+6*URT_CLK	UART0,1 common reset	Common to UART[1:0]
WDT	WDT_PRESETN[1:0]	TYPE-B	The later of A+5*WDT_PCLK or A+5*WDT_CLK	The later of A+6*WDT_PCLK or A+6*WDT_CLK	WDT0,1 reset	WDT[0] WDT[1]
PFC	PFC_PRESETN	TYPE-A	—	1*PFC_PCLK	PFC reset	
GRP*3	—	—	—	—	—	
CIF*3	—	—	—	—	—	
DCU*3	—	—	—	—	—	
LCI*3	—	—	—	—	—	
	—	—	—	—	—	
HDMI*3	—	—	—	—	—	
	—	—	—	—	—	
SYC	SYC_RST_N	TYPE-B	A+5*SYC_CNT_CLK	A+7*SYC_CNT_CLK	SYC reset (synchronous)	
SYS	SYS_RST_N	TYPE-A	—	1*SYS_CLK	SYS reset	
TSU0	TSU0_RESETN	TYPE-A	—	—	TSU0 reset	
TSU1	TSU1_RESETN	TYPE-A	—	—	TSU1 reset	
ESI	SDT_RSTSYSAX	TYPE-A	—	—	ESI reset	
LPDDR4 *3	—	—	Software sequence		—	
	—	—			—	
	—	—			—	
	—	—			—	
	—	—			—	
	—	—			—	
STG*3	—	—	—	—	—	
ISP*3	—	—	—	—	—	
	—	—	—	—	—	
GPA*3	—	—	—	—	—	
JPG*3	—	—	—	—	—	
VCD*3	—	—	—	—	—	
ISP*3	—	—	—	—	—	
	—	—	—	—	—	
GPA*3	—	—	—	—	—	
MTD*3	—	—	—	—	—	

Table 48.4-1 List of Reset Signals (4/4)

Unit	Signal Name	Reset Control Type*1	Minimum Assertion Period*2	De-assertion Delay for Target Unit*2	Description	Remarks
DRP-AI	DRPA_ARESETN	TYPE-B	A+14*DRPA_INITCLK	A+7*DRPA_INITCLK	DRP-AI reset	
ICB	ICB_PD_AWO_RST_N	TYPE-A	—	—	ICB AWO domain reset	
	ICB_PD_MMC_RST_N	TYPE-A	—	—	ICB MMC domain reset	
	ICB_PD_VD0_RST_N	TYPE-A	—	—	ICB VIDEO_0 domain reset	
	ICB_PD_VD1_RST_N	TYPE-A	—	—	ICB VIDEO_1 domain reset	
	ICB_PD_RFX_RST_N	TYPE-A	—	—	ICB RAMB domain reset	

Note: The definitions and supplementary explanations of reset control types “TYPE-A” and “TYPE-B” are shown below.

TYPE-A: A type which does not require clock supply at the time of a reset.

TYPE-B: A type which requires clock supply at the time of a reset.

For details of the reset control types, see **Section 48.6.2.5(1), Reset Control TYPE-A** and **Section 48.6.2.5(2), Reset Control TYPE-B**.

Schematic views of the procedures by the register settings are shown in **Figure 48.4-2** and **Figure 48.4-3**.

The numbers in the “Reg” waveforms in the figures are the steps of the register settings.

Note 1. A is a constant.
A: 729.17 ns (35 cycles at 48 MHz)

Note 2. The definitions of the minimum assertion period and de-assertion transmission period are shown in **Figure 48.4-2** and **Figure 48.4-3**.
When the reset is asserted by the CPG register, set the reset release after the minimum assertion period has elapsed.
In addition, access the unit after at least “de-assertion delay of the target unit” has elapsed.

Note 3. For more information, contact a Renesas Electronics sales representative.

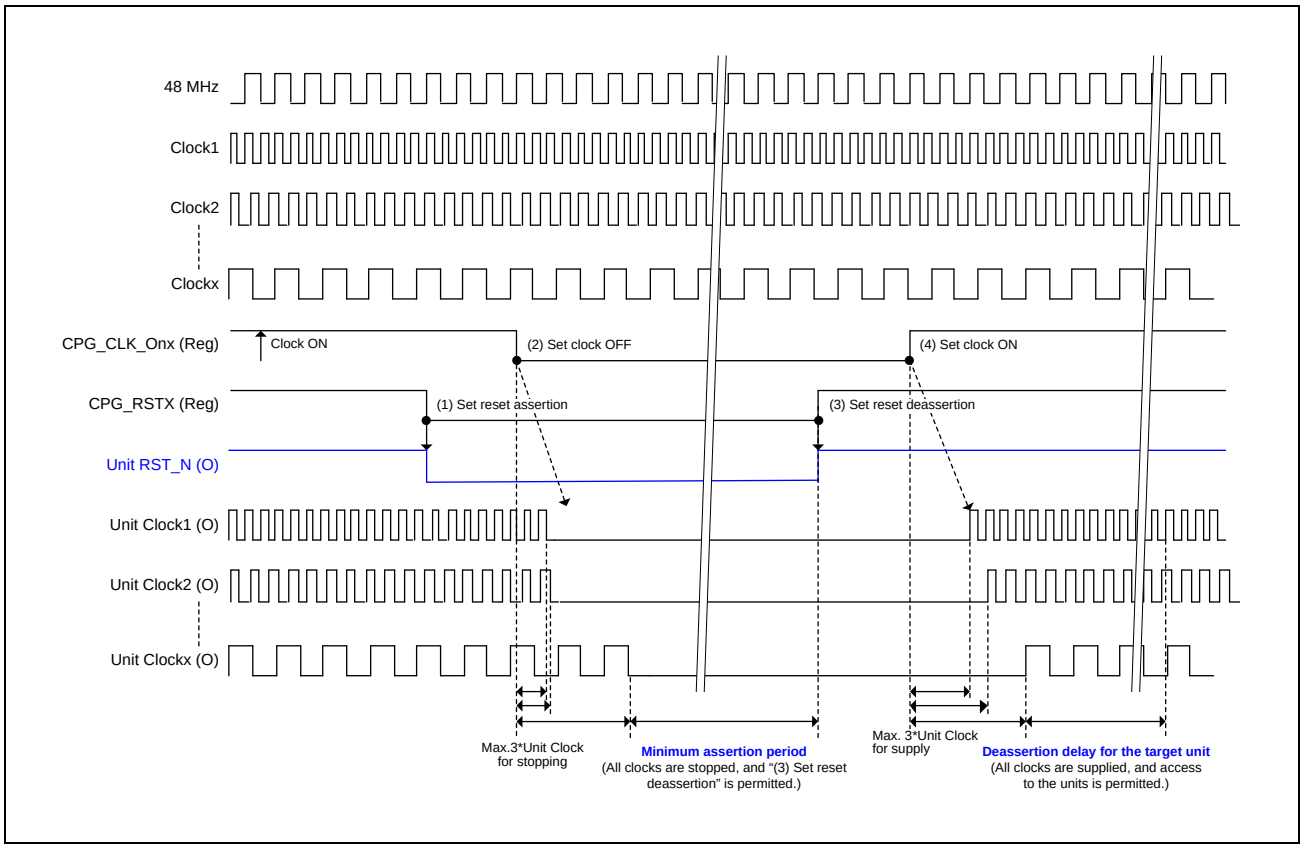


Figure 48.4-2 Minimum Assertion Period, Deassertion Delay Definition for Target Unit (TYPE-A)

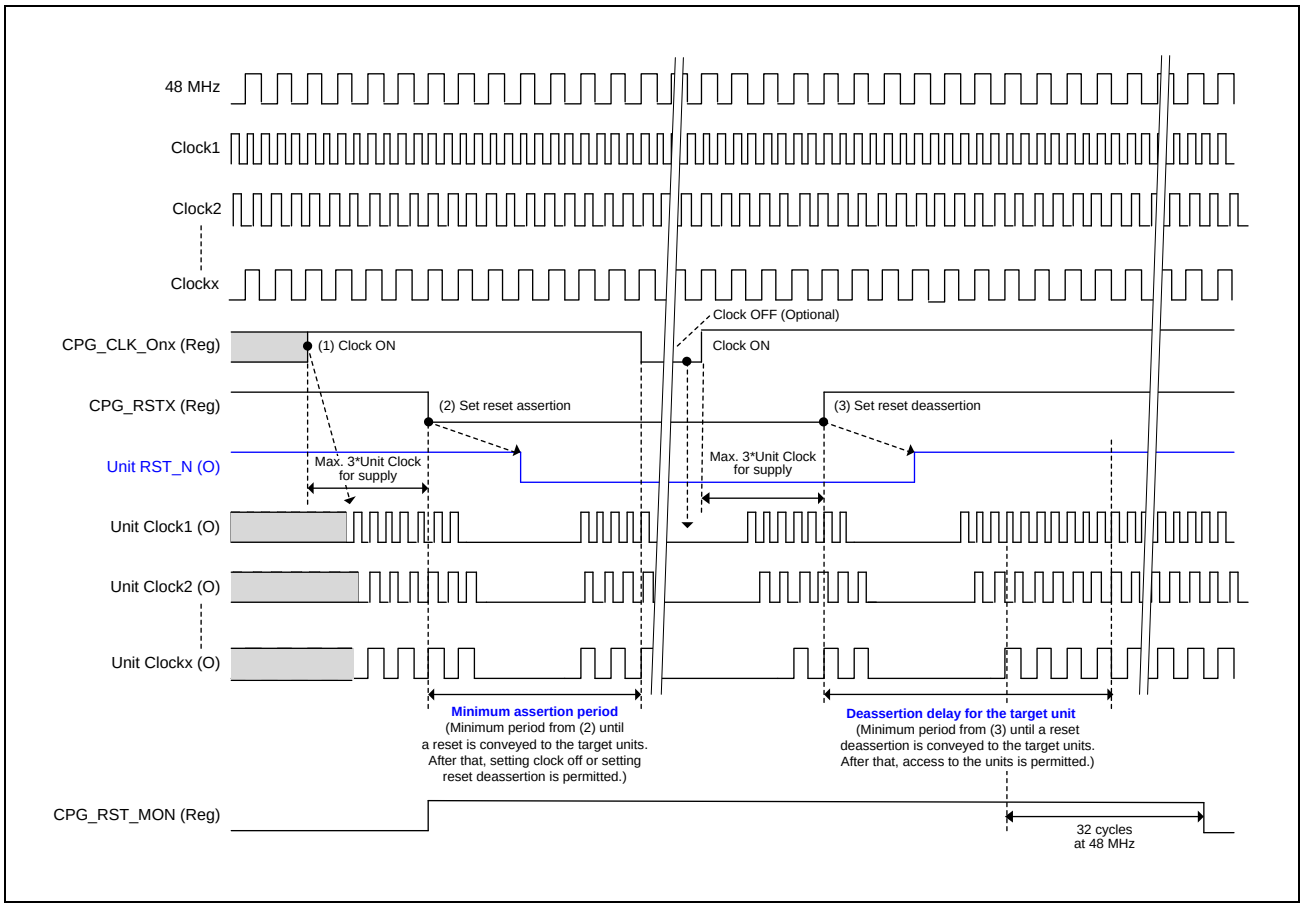


Figure 48.4-3 Minimum Assertion Period, Deassertion Delay Definition for Target Unit (TYPE-B)

48.5 Register Description

For the base address of the register (<CPG_S0_base>), see the Address Map section.

48.5.1 List of Registers

The following table is a list of registers in this unit.

Table 48.5-1 List of Registers (1/4)

Offset Address	Resister Name	Abbreviation	Initial Value	Access Unit (bits)
SSCG PLL(PLL1-3,6,7) Control Registers 000h-0FFh				
000h	PLL1 (SSCG) Standby Control Register	CPG_PLL1_STBY	0000_0005h	32
004h	PLL1 (SSCG) Output Clock Setting Register 1	CPG_PLL1_CLK1	0000_14C2h	32
008h	PLL1 (SSCG) Output Clock Setting Register 2	CPG_PLL1_CLK2	0015_0801h	32
00Ch	PLL1 (SSCG) Monitor Register	CPG_PLL1_MON	0000_0011h	32
010h	PLL2 (SSCG) Standby Control Register	CPG_PLL2_STBY	0000_0005h	32
014h	PLL2 (SSCG) Output Clock Setting Register 1	CPG_PLL2_CLK1	0000_1903h	32
018h	PLL2 (SSCG) Output Clock Setting Register 2	CPG_PLL2_CLK2	000E_0E00h	32
01Ch	PLL2 (SSCG) Monitor Register	CPG_PLL2_MON	0000_0011h	32
020h	PLL3 (SSCG) Standby Control Register	CPG_PLL3_STBY	0000_0004h	32
024h	PLL3 (SSCG) Output Clock Setting Register 1	CPG_PLL3_CLK1	0000_1903h	32
028h	PLL3 (SSCG) Output Clock Setting Register 2	CPG_PLL3_CLK2	000E_0E00h	32
02Ch	PLL3 (SSCG) Monitor Register	CPG_PLL3_MON	0000_0000h	32
030h	PLL6 (SSCG) Standby Control Register	CPG_PLL6_STBY	0000_0000h	32
034h	PLL6 (SSCG) Output Clock Setting Register 1	CPG_PLL6_CLK1	0000_1A42h	32
038h	PLL6 (SSCG) Output Clock Setting Register 2	CPG_PLL6_CLK2	0015_0A01h	32
03Ch	PLL6 (SSCG) Monitor Register	CPG_PLL6_MON	0000_0000h	32
040h	PLL7 (SSCG) Standby Control Register	CPG_PLL7_STBY	0000_0004h	32
044h	PLL7 (SSCG) Output Clock Setting Register 1	CPG_PLL7_CLK1	0000_18C2h	32
048h	PLL7 (SSCG) Output Clock Setting Register 2	CPG_PLL7_CLK2	0015_0A01h	32
04Ch	PLL7 (SSCG) Monitor Register	CPG_PLL7_MON	0000_0000h	32
050h-0FCh	Reserved	—	—	32
Fractional PLL(PLL4) Control Registers 100h-17Fh				
100h	PLL4 (SSCG) Standby Control Register	CPG_PLL4_STBY	0000_0000h	32
104h	PLL4 (SSCG) Output Clock Setting Register 1	CPG_PLL4_CLK1	0000_1802h	32
108h	PLL4 (SSCG) Output Clock Setting Register 2	CPG_PLL4_CLK2	0000_0002h	32
10Ch	PLL4 (SSCG) Monitor Register	CPG_PLL4_MON	0000_0000h	32
110h-17Ch	Reserved	—	—	32
PLL(PLL1-4,7) Clock Control Reset Registers 180h-1FFh				
180h	PLL1 Clock Control Circuit Reset Register	CPG_PLL1_CCTRL_RST	0000_0001h	32
184h	PLL2 Clock Control Circuit Reset Register	CPG_PLL2_CCTRL_RST	0000_3EFFh	32
188h	PLL3 Clock Control Circuit Reset Register	CPG_PLL3_CCTRL_RST	0000_0003h	32
18Ch	PLL4 Clock Control Circuit Reset Register	CPG_PLL4_CCTRL_RST	0000_003Fh	32
190h	Reserved	—	—	32
194h	Reserved	—	—	32
198h	PLL7 Clock Control Circuit Reset Register	CPG_PLL7_CCTRL_RST	0000_0007h	32
19Ch-1FCh	Reserved	—	—	32

Table 48.5-1 List of Registers (2/4)

Offset Address	Resister Name	Abbreviation	Initial Value	Access Unit (bits)
Frequency Dynamic Change Control Registers 200h-2FFh				
200h	CA53 Clock Division Ratio Setting Register	CPG_CA53_DDIV	0000_0003h	32
204h	System Division Ratio Setting Register	CPG_SYS_DDIV	0000_0001h	32
208h	Reserved	—	—	32
20Ch	NFI Clock Division Ratio Setting Register	CPG_NFI_DDIV	0000_0000h	32
210h	MMC/DDI Clock Division Ratio Setting Register	CPG_MMCDDI_DDIV	0000_0000h	32
214h	PLL/48 MHz Clock Source Setting Register	CPG_CLK48_DSEL	0000_003Fh	32
218h	ISP Clock Division Ratio Setting Register 1	CPG_ISP_DDIV1	0000_0000h	32
21Ch	ISP Clock Division Ratio Setting Register 2	CPG_ISP_DDIV2	0000_0000h	32
220h	ISP Clock Source Setting Register	CPG_ISP_DSEL	0000_0000h	32
224h	Clock Status Monitor Register	CPG_CLKSTATUS	0000_0000h	32
228h-2FCh	Reserved	—	—	32
Frequency Static Change Control Registers 300h-3FFh				
300h	SDI/EMM Clock Source Setting Register	CPG_SDIEMM_SSEL	0000_0001h	32
304h	STG Clock Division Ratio Setting Register	CPG_STG_SDIV	0000_0000h	32
308h	STG/CIF Clock Source Setting Register	CPG_STGCIF_SSEL	0000_0000h	32
30Ch	Display Clock Division Ratio Setting Register 1	CPG_DISP_SDIV1	0000_0000h	32
310h	Display Clock Division Ratio Setting Register 2	CPG_DISP_SDIV2	0000_0000h	32
314h	Display Clock Source Setting Register 1	CPG_DISP_SSEL1	0000_0000h	32
318h	Display Clock Source Setting Register 2	CPG_DISP_SSEL2	0000_0000h	32
31Ch	GMCLK Clock Division Ratio Setting Register	CPG_GMCLK_SDIV	0000_0000h	32
320h	GMCLK Clock Source Setting Register	CPG_GMCLK_SSEL	0000_0000h	32
324h	MTR Clock Source Setting Register	CPG_MTR_SSEL	0000_0000h	32
328h	UART_REF Clock Division Ratio Setting Register	CPG_URT_RCLK_SDIV	0000_0000h	32
32Ch	UART_REF Clock Source Setting Register	CPG_URT_RCLK_SSEL	0000_0000h	32
330h	CSI_REF Clock Source Setting Register	CPG_CSI_RCLK_SSEL	0000_0000h	32
334h-3FCh	Reserved	—	—	32
Clock Control Registers 400h-4FFh				
400h	Clock ON/OFF Control Register 1 (AWO SYSTEM Clock Control)	CPG_CLK_ON1	0000_FFFEh	32
404h	Clock ON/OFF Control Register 2 (AWO CoreSight Clock Control)	CPG_CLK_ON2	0000_001Fh	32
408h	Clock ON/OFF Control Register 3 (AWO Storage Clock Control)	CPG_CLK_ON3	0000_0000h	32
40Ch	Clock ON/OFF Control Register 4 (AWO PCIe,USB,ETHER Clock Control)	CPG_CLK_ON4	0000_0000h	32
410h	Clock ON/OFF Control Register 5 (AWO ESI,GRP,CIF,DCU Clock Control)	CPG_CLK_ON5	0000_0000h	32
414h	Clock ON/OFF Control Register 6 (AWO HDMI,LCI Clock Control)	CPG_CLK_ON6	0000_0000h	32
418h	Clock ON/OFF Control Register 7 (AWO AUI, General purpose clock, MTR, ISP Clock Control)	CPG_CLK_ON7	0000_0000h	32
41Ch	Clock ON/OFF Control Register 8 (AWO ADC, SYC Clock Control)	CPG_CLK_ON8	0000_2000h	32
420h	Clock ON/OFF Control Register 9 (AWO Peripheral Group A Clock Control)	CPG_CLK_ON9	0000_0000h	32

Table 48.5-1 List of Registers (3/4)

Offset Address	Resister Name	Abbreviation	Initial Value	Access Unit (bits)
424h	Clock ON/OFF Control Register 10 (AWO Peripheral Group B Clock Control)	CPG_CLK_ON10	0000_0000h	32
428h	Clock ON/OFF Control Register 11 (AWO Peripheral Group C Clock Control)	CPG_CLK_ON11	0000_F000h	32
42Ch	Clock ON/OFF Control Register 12 (AWO Peripheral Group D Clock Control)	CPG_CLK_ON12	0000_0000h	32
430h	Clock ON/OFF Control Register 13 (AWO Peripheral Group E Clock Control)	CPG_CLK_ON13	0000_0000h	32
434h	Clock ON/OFF Control Register 14 (AWO Peripheral Group F Clock Control)	CPG_CLK_ON14	0000_0000h	32
438h	Clock ON/OFF Control Register 15 (AWO Peripheral Group G,H Clock Control)	CPG_CLK_ON15	0000_0000h	32
43Ch	Clock ON/OFF Control Register 16 (ICB Clock Control 1)	CPG_CLK_ON16	0000_FC1Dh	32
440h	Clock ON/OFF Control Register 17 (ICB Clock Control 2)	CPG_CLK_ON17	0000_0001h	32
444h	Clock ON/OFF Control Register 18 (ICB Clock Control 3)	CPG_CLK_ON18	0000_0000h	32
448h	Clock ON/OFF Control Register 19 (PD CA53 Clock Control)	CPG_CLK_ON19	0000_003Fh	32
44Ch	Clock ON/OFF Control Register 20 (PD DRPA Clock Control)	CPG_CLK_ON20	0000_0000h	32
450h-454h	Reserved	—	—	32
458h	Clock ON/OFF Control Register 23 (RAMB Clock Control)	CPG_CLK_ON23	0000_0000h	32
45Ch	Clock ON/OFF Control Register 24 (PD VIDEO0 Clock Control)	CPG_CLK_ON24	0000_0000h	32
460h	Clock ON/OFF Control Register 25 (PD VIDEO1_0 Clock Control)	CPG_CLK_ON25	0000_0000h	32
464h	Clock ON/OFF Control Register 26 (PD VIDEO1_1 Clock Control)	CPG_CLK_ON26	0000_0000h	32
468h	Clock ON/OFF Control Register 27 (PD MEM Clock Control)	CPG_CLK_ON27	0000_0000h	32
46Ch-4FCh	Reserved	—	—	32
Reset Control Registers 500h-5FFh				
500h	WDT Reset Range Select Register	CPG_WDT_RST	0000_0000h	32
504h	Reset Mask Register	CPG_RST_MSK	0000_0000h	32
508h-5FCh	Reserved	—	—	32
Reset Control Registers 600h-67Fh				
600h	Reset Control Register 1 (AWO System Reset Control)	CPG_RST1	0000_FFFEh	32
604h	Reset Control Register 2 (AWO CoreSight Reset Control)	CPG_RST2	0000_07FFh	32
608h	Reset Control Register 3 (AWO Storage, PCIe, USB, ETHER Reset Control)	CPG_RST3	0000_0000h	32
60Ch	Reset Control Register 4 (AWO ESI, GRP, DCU, CIF, HDMI, LCI Reset Control)	CPG_RST4	0000_0000h	32
610h	Reset Control Register 5 (AWO AUI,MTR,ISP,ADC,SYC Reset Control)	CPG_RST5	0000_0400h	32
614h	Reset Control Register 6 (AWO Peripheral Reset Control)	CPG_RST6	0000_3000h	32

Table 48.5-1 List of Registers(4/4)

Offset Address	Resister Name	Abbreviation	Initial Value	Access Unit (bits)
618h	Reset Control Register 7 (ICB Reset Control)	CPG_RST7	0000_0001h	32
61Ch	Reset Control Register 8 (PD CA53 Reset Control)	CPG_RST8	0000_01FFh	32
620h	Reset Control Register 9 (PD DRPA Reset Control)	CPG_RST9	0000_0000h	32
624h-628h	Reserved	—	—	32
62Ch	Reset Control Register 12 (RAMB Reset Control)	CPG_RST12	0000_0000h	32
630h	Reset Control Register 13 (PD VIDEO0 Reset Control)	CPG_RST13	0000_0000h	32
634h	Reset Control Register 14 (PD VIDEO1 Reset Control)	CPG_RST14	0000_0000h	32
638h	Reset Control Register 15 (PD MEM Reset Control)	CPG_RST15	0000_0000h	32
63Ch-67Ch	Reserved	—	—	32
Reset Monitor Registers 680h-6FFh				
680h	Reset Monitor Register	CPG_RST_MON	37E7_EFC0h	32
684h-6FCh	Reserved	—	—	32
Reserved Registers 700h-7FFh				
700h-7FCh	Reserved	—	—	32
CPG Power Domain Reset Control Registers 800h-8FFh				
800h	CPG Power Domain Reset Control Register	CPG_PD_RST	0000_0000h	32
804h-8FCh	Reserved	—	—	32

48.5.2 Register Descriptions

The function description of each register is given below.

48.5.2.1 PLLm Standby Control Register (CPG_PLLm_STBY) (m = 1, 2, 3, 6, 7)

This register controls the power saving mode, standby, and SSC ON/OFF of SSCG PLLm.

In this LSI, PLL1, PLL2, PLL4, PLL6, and PLL7 are for use with the ISP support package. Therefore, do not write to the target registers. In addition, the target registers of PLL3 should not be rewritten because changing the LPDDR4 operation frequency after startup is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0000h (m = 1)
<CPG_S0_base> + 0010h (m = 2)
<CPG_S0_base > + 0020h (m = 3)
<CPG_S0_base> + 0030h (m = 6)
<CPG_S0_base> + 0040h (m = 7)

Initial Value: 0000_0005h (m = 1)
0000_0005h (m = 2)
0000_0004h (m = 3)
0000_0000h (m = 6)
0000_0004h (m = 7)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	SSC_MODE_WEN	—	SSC_EN_WEN	—	RESETB_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R0W1	R	R0W1	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	SSC_MODE[1:0]		—	SSC_EN	—	RESETB
Initial Value m = 1, 2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
Initial Value m = 3, 7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Initial Value m = 6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W	R	R	R	R	R	R	R	R	R	RW	RW	R	RW	R	RW

Table 48.5-2 CPG_PLLm_STBY Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 21	—	Reserved. These bits are read as 0b.
20	SSC_MODE_WEN	Enables write for SSC_MODE[1:0] (bits 5-4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. These bits are read as 0b.
18	SSC_EN_WEN	Enables write for SSC_EN (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	—	Reserved. This bit is read as 0b..

Table 48.5-2 CPG_PLLm_STBY Register Contents (2/2)

Bit Position	Bit Name	Description
16	RESETB_WEN	Enables write for RESETB (bit 0). This bit is read as 0b 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b.
5, 4	SSC_MODE[1:0]	SSC Center/Up/Down Spread setting (follow **Table 48.5-3**). Set SSC_MODE_WEN (bit20) to 1 simultaneously when writing to this register. 00b: Down spread 01b: Up spread 10b: Center spread 11b: Prohibited
3	—	Reserved. This bit is read as 0b.
2	SSC_EN	SSC ON/OFF setting (follow **Table 48.5-3**). Set SSC_EN_WEN (bit 18) to 1 simultaneously when writing to this register. 0b: SSC off 1b: SSC on
1	—	Reserved. This bit is read as 0b.
0	RESETB	PLL reset setting (follow **Table 48.5-3**). Set RESETB_WEN (bit 16) to 1 simultaneously when writing to this register. 0b: Reset state 1b: Active (reset release) state

Table 48.5-3 Mode setting table

Mode		Field		
		RESETB	SSC_EN	SSC_MODE[1:0]
Reset state		0b	—	—
SSC OFF		1b	0b	—
SSC ON	Down spread		1b	00b
	Up spread			01b
	Center spread			10b
Prohibited				11b

Note: In the case of Up spread or Center spread, the setting exceeding the maximum frequency is prohibited.

48.5.2.2 PLLm Output Clock Setting Register 1 (CPG_PLLm_CLK1) (m = 1, 2, 3, 6, 7)

This register sets the K, M, P divided value of SSCG PLLm.

In this LSI, PLL1, PLL2, PLL4, PLL6, and PLL7 are for use with the ISP support package. Therefore, do not write to the target registers. In addition, the target registers of PLL3 should not be rewritten because changing the LPDDR4 operation frequency after startup is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0004h (m = 1)
<CPG_S0_base> + 0014h (m = 2)
<CPG_S0_base> + 0024h (m = 3)
<CPG_S0_base> + 0034h (m = 6)
<CPG_S0_base> + 0044h (m = 7)

Initial Value: 0000_14C2h (m = 1)
0000_1903h (m = 2)
0000_1903h (m = 3)
0000_1A42h (m = 6)
0000_18C2h (m = 7)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DIV_K															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIV_M										DIV_P					
Initial Value m = 1	0	0	0	1	0	1	0	0	1	1	0	0	0	0	1	0
Initial Value m = 2, 3	0	0	0	1	1	0	0	1	0	0	0	0	0	0	1	1
Initial Value m = 6	0	0	0	1	1	0	1	0	0	1	0	0	0	0	1	0
Initial Value m = 7	0	0	0	1	1	0	0	0	1	1	0	0	0	0	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 48.5-4 CPG_PLLm_CLK1 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 16	DIV_K	This is a Delta-Signa Modulator (DSM) value setting register.*4 The value that satisfies the range from -32768 to 32767 (decimal) and also satisfies the constraint of Note 1 may be set in 2's complement. 1000_0000_0000_0000b: "K" = -32768 1000_0000_0000_0001b: "K" = -32767 1000_0000_0000_0010b: "K" = -32766 ⋮ 0111_1111_1111_1101b: "K" = +32765 0111_1111_1111_1110b: "K" = +32766 0111_1111_1111_1111b: "K" = +32767

Table 48.5-4 CPG_PLLm_CLK1 Register Contents (2/2)

Bit Position	Bit Name	Description
15 to 6	DIV_M	This is a main divider value setting register.*4 The value that satisfies the range from 64 to 533 (decimal) and also satisfies the constraints of Note 1 and Note 2 may be set in unsigned 2's complement. 11_1111_1111b to 10_0001_1011b ("M" = 534): Prohibited 01_0000_1010b: Division Value "M" = 533 01_0000_1010b: Division Value "M" = 532 ⋮ 00_0010_0001b: Division Value "M" = 65 00_0010_0000b: Division Value "M" = 64 00_0011_1111b to 00_0000_0000b: Prohibited
5 to 0	DIV_P	This is a pre divider value setting register.*4 The value that satisfies the range from 2 to 8 and also satisfies the constraints of Note 1 and Note 2 may be set. 11_1111b to 00_1001b: Prohibited 00_1000b: Division Value "P" = 8 (F_{FREF} = 6 MHz) 00_0111b: Division Value "P" = 7 (F_{FREF} = 6.86 MHz) ⋮ 00_0011b: Division Value "P" = 3 (F_{FREF} = 16 MHz) 00_0010b: Division Value "P" = 2 (F_{FREF} = 24 MHz) 00_0001b to 00_0000b: Prohibited

Note 1. PLL Oscillation frequency (F_{FVCO}) and output frequency (F_{FOUT}) may be calculated with the following formula.

- Formula

$$F_{FVCO} = \frac{\left(m+\frac{k}{65536}\right)\times F_{Fin}}{p}$$

$$F_{FOUT} = \frac{\left(m+\frac{k}{65536}\right)\times F_{Fin}}{p\times 2^{s}} \quad *3$$

- Restriction

  F_{Fin}: 48 MHz

  6 MHz ≤ F_{FREF} = F_{FIN}/p ≤ 24 MHz

  1600 MHz ≤ FFVCO ≤ 3200 MHz

Note 2. F_{FVCO}, F_{Fout} of DIV_K, DIV_M, DIV_P, DIV_S*3 should be set within the following PLL settable range. SSCG frequency modulation function not exceeding the MAX limit is available.

Table 48.5-5 Mode setting table (FFVCO)

SSCG PLL	F_{FVCO} Min	F_{FVCO} Default configuration	F_{FVCO} Max
PLL1	—	1992 MHz (Frequency fixed)	—
PLL2	—	1600 MHz (Frequency fixed)	—
PLL3	1600 MHz	1600 MHz	2400 MHz
PLL6	—	2520 MHz (Frequency fixed)	—
PLL7	1896 MHz	2376 MHz	2376 MHz

Table 48.5-6 Mode setting table (FFOUT)

SSCG PLL	FFOUT Min	FFOUT Default configuration	FFOUT Max
PLL1	—	996 MHz (Frequency fixed)	—
PLL2	—	1600 MHz (Frequency fixed)	—
PLL3	1200 MHz	1600 MHz	1600 MHz
PLL6	—	1260 MHz (Frequency fixed)	—
PLL7	948 MHz	1188 MHz	1188 MHz

Note 3. See **48.5.2.3, PLLm Output Clock Setting Register 2 (CPG_PLLm_CLK2) (m = 1, 2, 3, 6, 7)** as DIV_S ("S").

Note.4 When the setting is changed, the PLL reset is required.

48.5.2.3 PLLm Output Clock Setting Register 2 (CPG_PLLm_CLK2) (m = 1, 2, 3, 6, 7)

This register sets the divided value and SSC modulation value (MFR, MMR) of SSCG PLLm.

In this LSI, PLL1, PLL2, PLL4, PLL6, and PLL7 are for use with the ISP support package. Therefore, do not write to the target registers. In addition, the target registers of PLL3 should not be rewritten because changing the LPDDR4 operation frequency after startup is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0008h (m = 1)
<CPG_S0_base> + 0018h (m = 2)
<CPG_S0_base> + 0028h (m = 3)
<CPG_S0_base> + 0038h (m = 6)
<CPG_S0_base> + 0048h (m = 7)

Initial Value: 0015_0801h (m = 1)
000E_0E00h (m = 2)
000E_0E00h (m = 3)
0015_0A01h (m = 6)
0015_0A01h (m = 7)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	MFR							
Initial Value m = 1, 6, 7	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1
Initial Value m = 2, 3	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	MRR						—	—	—	—	—	DIV_S		
Initial Value m = 1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1
Initial Value m = 2, 3	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0
Initial Value m = 6, 7	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	R	R	R	RW	RW	RW

Table 48.5-7 CPG_PLLm_CLK2 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b.
23 to16	MFR	Modulation frequency setting register. When the setting is changed, the PLL reset is required. A range of values is set from 0 to 255 (decimal).*1 1111_1111b: “MFR” = 255 1111_1110b: “MFR” = 254 ⋮ 0000_0001b: “MFR” = 1 0000_0000b: “MFR” = 0
15, 14	—	Reserved. These bits are read as 0b.

Table 48.5-7 CPG_PLLm_CLK2 Register Contents (2/2)

Bit Position	Bit Name	Description
13 to 8	MRR	Modulation rate setting register. When the setting is changed, the PLL reset is required. A range of values is set from 1 to 63 (decimal).*1 11_1111b: “MRR” = 63 11_1110b: “MRR” = 62 ⋮ 00_0010b: “MRR” = 2 00_0001b: “MRR” = 1 00_0000b: Prohibited
7 to 3	—	Reserved. These bits are read as 0b.
2 to 0	DIV_S	Divider S setting register.*2 A range of values is set from 0 to 6 (decimal). 111b: Prohibited 110b: Division Value “S” = 6 (Division Ratio = 64) 101b: Division Value “S” = 5 (Division Ratio = 32) 100b: Division Value “S” = 4 (Division Ratio = 16) 011b: Division Value “S” = 3 (Division Ratio = 8) 010b: Division Value “S” = 2 (Division Ratio = 4) 001b: Division Value “S” = 1 (Division Ratio = 2) 000b: Division Value “S” = 0 (Division Ratio = 1)

Note 1. Modulation frequency (MF) and Modulation rate (pk-pk) (MR) can be calculated with the following formula.

- Formula

$$MF = \frac{(F_{Fin})}{p \times mfr \times (2^5)}$$

$$MR = \frac{mfr \times mrr}{m \times 2^6} \times 100[\%]$$

- Restriction

Ffin: 48 MHz

0000_0000b ≤ MFR[7:0] ≤ 1111_1111b

00_0001b ≤ MRR[5:0] ≤ 11_1111b

0 ≤ mrr ≤ mfr ≤ 512

Note 2. See **48.5.2.2, PLLm Output Clock Setting Register 1 (CPG_PLLm_CLK1) (m = 1, 2, 3, 6, 7)** as DIV_M(M), DUV_P(P). The initial values of PLL1, 2, 3, 6, and 7 register settings and output clocks are listed in **Table 48.5-8** and **Table 48.5-9**.

Table 48.5-8 Mode setting table (FFVCO)

	CPG_PLLm_STBY (m = 1, 2, 3, 6, 7)		
	SSC_MODE	SSC_EN	RESETB
PLL	Bits 5, 4	Bit 2	Bit 0
PLL1	0h (Down spread)	1 (SSC ON)	1 (Active)
PLL2	0h (Down spread)	1 (SSC ON)	1 (Active)
PLL3	0h (Down spread)	1 (SSC ON)	0 (Reset state)
PLL6	0h (Down spread)	0 (SSC OFF)	0 (Reset state)
PLL7	0h (Down spread)	1 (SSC ON)	0 (Reset state)

	CPG_PLLm_CLK1 (m = 1, 2, 3, 6, 7)			CPG_PLLm_CLK2 (m = 1, 2, 3, 6, 7)		
	DIV_K	DIV_M	DIV_P	DIV_S	MFR	MRR
PLL	Bits 31-16	Bits 15-6	Bits 5-0	Bits 2-0	Bits 23-16	Bits 13-8
PLL1	0000h (K = 0)	53h (M = 83)	2h (P = 2)	1h (S = 1)	15h (mfr = 21)	08h (mrr = 8)
PLL2	0000h (K = 0)	64h (M = 100)	3h (P = 3)	0h (S = 0)	0Eh (mfr = 14)	0Eh (mrr = 14)
PLL3	0000h (K = 0)	64h (M = 100)	3h (P = 3)	0h (S = 0)	0Eh (mfr = 14)	0Eh (mrr = 14)
PLL6	0000h (K = 0)	69h (M = 105)	2h (P = 2)	1h (S = 1)	15h (mfr = 21)	0Ah (mrr = 10)
PLL7	0000h (K = 0)	63h (M = 99)	2h (P = 2)	1h (S = 1)	15h (mfr = 21)	0Ah (mrr = 10)

Table 48.5-9 Output clock (Initial value)

PLL	PLL action mode	Frequency (F_{FOUT}) [MHz]	SSC	Fmod [kHz]	Spread	Modulation depth [%]
PLL1	Active	996	ON	35.71	Down spread	3.16
PLL2	Active	1600	ON	35.71	Down spread	3.06
PLL3	Reset state	1600	ON	35.71	Down spread	3.06
PLL6	Reset state	1260	OFF	35.71	Down spread	3.13
PLL7	Reset state	1188	ON	35.71	Down spread	3.31

48.5.2.4 PLLm Monitor Register (CPG_PLLm_MON) (m = 1, 2, 3, 6, 7)

This register is for monitoring the state of SSCG PLLm.

In this LSI, PLL1, PLL2, PLL4, PLL6, and PLL7 are for use with the ISP support package. Therefore, do not write to the target registers. In addition, the target registers of PLL3 should not be rewritten because changing the LPDDR4 operation frequency after startup is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 000Ch (m = 1)
<CPG_S0_base> + 001Ch (m = 2)
<CPG_S0_base> + 002Ch (m = 3)
<CPG_S0_base> + 003Ch (m = 6)
<CPG_S0_base> + 004Ch (m = 7)

Initial Value: 0000_0011h (m = 1)
0000_0011h (m = 2)
0000_0000h (m = 3)
0000_0000h (m = 6)
0000_0000h (m = 7)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PLL_LOCK	—	—	—	PLL_RESETB
Initial Value m = 1, 2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
Initial Value m = 3, 6, 7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 48.5-10 CPG_PLLm_MON Register Contents

Bit Position	Bit Name	Description
31 to 5	—	Reserved. These bits are read as 0b.
4	PLL_LOCK	SSC PLL lock monitoring 0b: PLL unlock 1b: PLL lock
3 to 1	—	Reserved. These bits are read as 0b.
0	PLL_RESETB	SSC PLL action mode monitoring 0b: Reset state (standby mode) 1b: Normal mode

48.5.2.5 PLL4 Standby Control Register (CPG_PLL4_STBY)

This register controls the standby of Fractional PLL4.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0100h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RESETB_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RESETB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 48.5-11 CPG_PLL4_STBY Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b.
16	RESETB_WEN	Enables write for RESETB (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b.
0	RESETB	PLL reset setting. Set RESETB_WEN (bit 16) to 1 simultaneously when writing to this register. 0b: Reset state 1b: Active (reset release state)

48.5.2.6 PLL4 Output Clock Setting Register 1 (CPG_PLL4_CLK1)

This register sets the K, M, P divided value of Fractional PLL4.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0104h

Initial Value: 0000_1802h

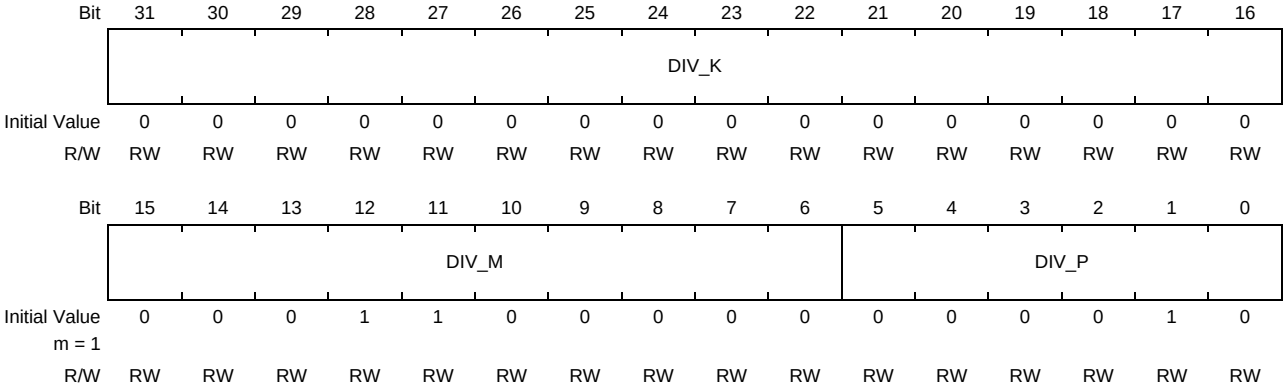


Table 48.5-12 CPG_PLL4_CLK1 Register Contents

Bit Position	Bit Name	Description
31 to 16	DIV_K	This is a Delta-Signa Modulator (DSM) value setting register.*4 The value that satisfies the range from -32768 to 32767 (decimal) and also satisfies the constraint of Note 1 may be set in 2's complement. 1000_0000_0000_0000b: "K" = -32768 1000_0000_0000_0001b: "K" = -32767 1000_0000_0000_0010b: "K" = -32766 ⋮ 0111_1111_1111_1101b: "K" = +32765 0111_1111_1111_1110b: "K" = +32766 0111_1111_1111_1111b: "K" = +32767
15 to 6	DIV_M	This is a main divider value setting register.*4 The value that satisfies the range from 64 to 533 (decimal) and satisfies the constraints of Note 1 and Note 2 may be set in unsigned 2's complement. 11_1111_1111b to 10_0001_1011b ("M" = 534): Prohibited 01_0000_1010b: Division Value "M" = 533 01_0000_1010b: Division Value "M" = 532 ⋮ 00_0010_0001b: Division Value "M" = 65 00_0010_0000b: Division Value "M" = 64 00_0011_1111b to 00_0000_0000b: Prohibited
5 to 0	DIV_P	This is a pre divider value setting register.*4 The value that satisfies the range from 2 to 8 and also satisfies the constraints of Note 1 and Note 2 may be set. 11_1111b to 00_1001b: Prohibited 00_1000b: Division Value "P" = 8 (F_{FREF} = 6 MHz) 00_0111b: Division Value "P" = 7 (F_{FREF} = 6.86 MHz) ⋮ 00_0011b: Division Value "P" = 3 (F_{FREF} = 16 MHz) 00_0010b: Division Value "P" = 2 (F_{FREF} = 24 MHz) 00_0001b to 00_0000b: Prohibited

Note 1. PLL Oscillation frequency (F_{FVCO}) and output frequency (F_{FOUT}) can be calculated with the following formula.

- Formula

$$F_{FVCO} = \frac{\left(m+\frac{k}{65536}\right)\times F_{Fin}}{p}$$

$$F_{FOUT} = \frac{\left(m+\frac{k}{65536}\right)\times F_{Fin}}{p\times 2^{s}} \quad *3$$

- Restriction

  F_{Fin}: 48 MHz

  6 MHz ≤ F_{FREF} = F_{FIN}/p ≤ 24 MHz

  1600 MHz ≤ FFVCO ≤ 3200 MHz

Note 2. FFVCO, FFout of DIV_K, DIV_M, DIV_P, DIV_S*3 should be set within the following PLL settable range.

Table 48.5-13 Mode setting table (FFVCO)

SSCG PLL	F_{FVCO} Min	F_{FVCO} Default configuration	F_{FVCO} Max
PLL4	2304 MHz	2304 MHz	2592 MHz

Table 48.5-14 Mode setting table (FFOUT)

SSCG PLL	F_{FOUT} Min	F_{FOUT} Default configuration	F_{FOUT} Max
PLL4	576 MHz	576 MHz	648 MHz

Note 3. See **48.5.2.7, PLL4 Output Clock Setting Register 2 (CPG_PLL4_CLK2)** as DIV_S (“S”)

Note.4 When the setting is changed, the PLL reset is required.

48.5.2.7 PLL4 Output Clock Setting Register 2 (CPG_PLL4_CLK2)

This register sets the divided value of Fractional PLL4.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0108h

Initial Value: 0000_0002h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DIV_S		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 48.5-15 CPG_PLL4_CLK2 Register Contents

Bit Position	Bit Name	Description
31 to 3	—	Reserved. These bits are read as 0b.
2 to 0	DIV_S	Divider S setting register. A range of values is set from 0 to 6 (decimal). 111b: Prohibited 110b: Division Value “S” = 6 (Division Ratio = 64) 101b: Division Value “S” = 5 (Division Ratio = 32) 100b: Division Value “S” = 4 (Division Ratio = 16) 011b: Division Value “S” = 3 (Division Ratio = 8) 010b: Division Value “S” = 2 (Division Ratio = 4) 001b: Division Value “S” = 1 (Division Ratio = 2) 000b: Division Value “S” = 0 (Division Ratio = 1)

Note: The initial values of PLL4 register settings and output clocks are listed in **Table 48.5-16** and **Table 48.5-17**.

Table 48.5-16 Register initial value

	CPG_PLL4_STBY
	RESETB
PLL	Bit 0
PLL4	0 (Reset state)

	CPG_PLL4_CLK1		
	DIV_K	DIV_M	DIV_P
PLL	Bits 31-16	Bits 15-6	Bits 5-0
PLL4	0000h (K = 0)	60h (M = 96)	2h (P = 2)

	CPG_PLL4_CLK1
	DIV_S
PLL	Bits 2-0
PLL4	2h (S = 2)

Table 48.5-17 Output clock (F_{Fout}) (Initial value)

PLL	PLL action mode	Frequency [MHz]
PLL4	Reset state	576

48.5.2.8 PLL4 Monitor Register (CPG_PLL4_MON)

This register is for monitoring the state of Fractional PLL4.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 010Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PLL_LOCK	—	—	—	PLL_RESETB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 48.5-18 CPG_PLL4_MON Register Contents

Bit Position	Bit Name	Description
31 to 5	—	Reserved. These bits are read as 0b.
4	PLL_LOCK	Fractional PLL lock monitoring 0b: PLL unlock 1b: PLL lock
3 to 1	—	Reserved. These bits are read as 0b.
0	PLL_RESETB	Fractional PLL action mode monitoring 0b: Reset state (standby mode) 1b: Normal mode

48.5.2.9 PLL1 Clock Control Circuit Reset Register (CPG_PLL1_CCTRL_RST)

This register resets the clock control circuit of PLL1.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0180h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	P1_0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	P1_0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 48.5-19 CPG_PLL1_CCTRL_RST Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b.
16	P1_0_RST WEN	Enables write for P1_0_RSTB (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b.
0	P1_0_RSTB	Reset the PLL1 clock control circuit (DIV A). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)

48.5.2.10 PLL2 Clock Control Circuit Reset Register (CPG_PLL2_CCTRL_RST)

This register resets the clock control circuit of PLL2.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0184h

Initial Value: 0000_3EFFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	P2_13_RSTB	P2_12_RSTB	P2_11_RSTB	P2_10_RSTB	P2_9_RSTB	—	P2_7_RSTB	—	P2_5_RSTB	P2_4_RSTB	P2_3_RSTB	P2_2_RSTB	P2_1_RSTB	P2_0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	P2_13_RSTB	P2_12_RSTB	P2_11_RSTB	P2_10_RSTB	P2_9_RSTB	—	P2_7_RSTB	—	P2_5_RSTB	P2_4_RSTB	P2_3_RSTB	P2_2_RSTB	P2_1_RSTB	P2_0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 48.5-20 CPG_PLL2_CCTRL_RST Register Contents (1/3)

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29	P2_13_RST WEN	Enables write for P2_13_RSTB (bit 13). Write only. Read as 0b. 0b: Write disable 1b: Write enable
28	P2_12_RST WEN	Enables write for P2_12_RSTB (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	P2_11_RST WEN	Enables write for P2_11_RSTB (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26	P2_10_RST WEN	Enables write for P2_10_RSTB (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25	P2_9_RST WEN	Enables write for P2_9_RSTB (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	—	Reserved. This bit is read as 0b..
23	P2_7_RST WEN	Enables write for P2_7_RSTB (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	—	Reserved. This bit is read as 0b. The write value should always be 0b.
21	P2_5_RST WEN	Enables write for P2_5_RSTB (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	P2_4_RST WEN	Enables write for P2_4_RSTB (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	P2_3_RST WEN	Enables write for P2_3_RSTB (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-20 CPG_PLL2_CCTRL_RST Register Contents (2/3)

Bit Position	Bit Name	Description
18	P2_2_RST WEN	Enables write for P2_2_RSTB (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	P2_1_RST WEN	Enables write for P2_1_RSTB (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	P2_0_RST WEN	Enables write for P2_0_RSTB (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b.
13	P2_13_RSTB	Reset the PLL2 clock control circuit (DIV H2). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
12	P2_12_RSTB	Reset the PLL2 clock control circuit (DIV U). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
11	P2_11_RSTB	Reset the PLL2 clock control circuit (DIV T). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
10	P2_10_RSTB	Reset the PLL2 clock control circuit (1/2 frequency divider with DIV M as source clock (decimation). 1/2 frequency divider with DIV_I for JPG0_CLK as source clock (decimation). 1/2 frequency divider with DIV_I for VCD_PCLK as source clock (decimation)). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
9	P2_9_RSTB	Reset the PLL2 clock control circuit (DIV I, DIV M). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
8	—	Reserved. This bit is read as 0b.
7	P2_7_RSTB	Reset the PLL2 clock control circuit (DIV H). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
6	—	Reserved. This bit is read as 0b. The write access is prohibited.
5	P2_5_RSTB	Reset the PLL2 clock control circuit (1/2 frequency divider (Duty50) with DIV8 (200 MHz) of PL2_DIV as source clock). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
4	P2_4_RSTB	Reset the PLL2 clock control circuit (DIV_NFI). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
3	P2_3_RSTB	Reset the PLL2 clock control circuit (1/4 frequency divider (Duty50) with DIV2 (800 MHz) of PL2_DIV as source clock). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
2	P2_2_RSTB	Reset the PLL2 clock control circuit (1/2 frequency divider with SEL B as source clock (decimation)). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
1	P2_1_RSTB	Reset the PLL2 clock control circuit (DIV B, DIV D, DIV E, DIVSEL G). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)

Table 48.5-20 CPG_PLL2_CCTRL_RST Register Contents (3/3)

Bit Position	Bit Name	Description
0	P2_0_RSTB	Reset the PLL2 clock control circuit (PL2_DIV). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)

48.5.2.11 PLL3 Clock Control Circuit Reset Register (CPG_PLL3_CCTRL_RST)

This register resets the clock control circuit of PLL3.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0188h

Initial Value: 0000_0003h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	P3_1_RST WEN	P3_0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	P3_1_RSTB	P3_0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Table 48.5-21 CPG_PLL3_CCTRL_RST Register Contents

Bit Position	Bit Name	Description
31 to 18	—	Reserved. These bits are read as 0b.
17	P3_1_RST WEN	Enables write for P3_1_RSTB (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	P3_0_RST WEN	Enables write for P3_0_RSTB (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 2	—	Reserved. These bits are read as 0b.
1	P3_1_RSTB	Reset the PLL3 clock control circuit (1/2 frequency divider with DIV X as source clock). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
0	P3_0_RSTB	Reset the PLL3 clock control circuit (DIV X). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)

48.5.2.12 PLL4 Clock Control Circuit Reset Register (CPG_PLL4_CCTRL_RST)

This register resets the clock control circuit of PLL4.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 018Ch

Initial Value: 0000_003Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	P4_5_RST WEN	P4_4_RST WEN	P4_3_RST WEN	P4_2_RST WEN	P4_1_RST WEN	P4_0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	P4_5_RSTB	P4_4_RSTB	P4_3_RSTB	P4_2_RSTB	P4_1_RSTB	P4_0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 48.5-22 CPG_PLL4_CCTRL_RST Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b.
21	P4_5_RST WEN	Enables write for P4_5_RSTB (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	P4_4_RST WEN	Enables write for P4_4_RSTB (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	P4_3_RST WEN	Enables write for P4_3_RSTB (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	P4_2_RST WEN	Enables write for P4_2_RSTB (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	P4_1_RST WEN	Enables write for P4_1_RSTB (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	P4_0_RST WEN	Enables write for P4_0_RSTB (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b.
5	P4_5_RSTB	Reset the PLL4 clock control circuit (DIV W). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
4	P4_4_RSTB	Reset the PLL4 clock control circuit (1/2 frequency divider (Duty50) with output clock of 1/3 frequency divider (OtherDuty50) with PLL4 as source clock). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)

Table 48.5-22 CPG_PLL4_CCTRL_RST Register Contents (2/2)

Bit Position	Bit Name	Description
3	P4_3_RSTB	Reset the PLL4 clock control circuit (1/3 frequency divider (OtherDuty50) with PLL4 as source clock). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
2	P4_2_RSTB	Reset the PLL4 clock control circuit (1/2 frequency divider (Duty50) that is supplied output clock of 1/2 frequency divider with DIV_STG as source clock). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
1	P4_1_RSTB	Reset the PLL4 clock control circuit (1/2 frequency divider (Duty50) with DIV_STG as source clock). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
0	P4_0_RSTB	Reset the PLL4 clock control circuit (DIV STG). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)

48.5.2.13 PLL7 Clock Control Circuit Reset Register (CPG_PLL7_CCTRL_RST)

This register resets the clock control circuit of PLL7.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0198h

Initial Value: 0000_0007h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	P7_2_RST WEN	P7_1_RST WEN	P7_0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	P7_2_RSTB	P7_1_RSTB	P7_0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 48.5-23 CPG_PLL7_CCTRL_RST Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b.
18	P7_2_RST WEN	Enables write for P7_2_RSTB (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	P7_1_RST WEN	Enables write for P7_1_RSTB (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	P7_0_RST WEN	Enables write for P7_0_RSTB (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b.
2	P7_2_RSTB	Reset the PLL7 clock control circuit (DIV LCLIP). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
1	P7_1_RSTB	Reset the PLL7 clock control circuit (1/2 frequency divider (Duty50) with DIV R as source clock). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)
0	P7_0_RSTB	Reset the PLL7 clock control circuit (DIV R). 0b: Reset ON (reset state) 1b: Reset OFF (reset release)

48.5.2.14 CA53 Clock Division Ratio Setting Register (CPG_CA53_DDIV)

This register sets the division ratio of CA53 core clock (DIV A).

The source clock is PLL1 (996 MHz). This register may be switched dynamically.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0200h

Initial Value: 0000_0003h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DIVA_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DIVA_SET		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 48.5-24 CPG_CA53_DDIV Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b.
16	DIVA_WEN	Enables write for DIVA_SET (bits 2-0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b.
2 to 0	DIVA_SET	Division setting of CA53 core clock. 000b: 1/1 (996 MHz) 001b: 1/2 (498 MHz) 010b: 1/3 (332 MHz) 011b: 1/4 (249 MHz) 100b: 1/6 (166 MHz) 101b: 1/12 (83 MHz) 110b: 1/24 (41.5 MHz) 111b: Prohibited (when 1/24 is set)

NOTE

Even if there is no change in the set value, writing ‘1’ to “_WEN” located in the upper 16 bits of the register starts the clock switching control. Therefore, it is necessary to wait until the switching is completed when monitoring their status (CPG_CLKSTATUS). (The clock stops temporarily when switching.)

48.5.2.15 System Division Ratio Setting Register (CPG_SYS_DDIV)

This register sets the division ratio of the system clock (DIV B, D, E).

The source clock is the clock divided by PLL2 (1600 MHz). This register may be switched dynamically.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0204h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DIVE_WEN	—	—	—	DIVD_WEN	—	—	—	DIVB_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R	R	R	R0W1	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DIVE_SET	—	—	DIVD_SET		—	—	DIVB_SET	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	RW	R	R	RW	RW	R	R	RW	RW

Table 48.5-25 CPG_SYS_DDIV Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24	DIVE_WEN	Enables write for DIVE_SET (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23 to 21	—	Reserved. These bits are read as 0b.
20	DIVD_WEN	Enables write for DIVD_SET (bits 5-4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19 to 17	—	Reserved. These bits are read as 0b.
16	DIVB_WEN	Enables write for DIVB_SET (bits 2-0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b.
8	DIVE_SET	Division setting of CPG_SPCLK. 0b: 1/1 (CPG_SPCLK: 100 MHz) 1b: 1/2 (CPG_SPCLK: 50 MHz)
7, 6	—	Reserved. These bits are read as 0b.
5, 4	DIVD_SET	Division setting of CPG_MPCLK. 00b: 1/1 (CPG_MPCLK: 200 MHz) 01b: 1/2 (CPG_MPCLK: 100 MHz) 10b: 1/4 (CPG_MPCLK: 50 MHz) 11b: Prohibited (when 1/4 is set)
3, 2	—	Reserved. These bits are read as 0b.
1, 0	DIVB_SET	Division setting of ICB_ACLK, GIC_CLK. 00b: 1/1 (ICB_ACLK: 400 MHz, GIC_CLK: 200 MHz) 01b: 1/2 (ICB_ACLK: 200 MHz, GIC_CLK: 100 MHz) 10b: 1/4 (ICB_ACLK: 100 MHz, GIC_CLK: 50 MHz) 11b: 1/8 (ICB_ACLK: 50 MHz, GIC_CLK: 25 MHz)

NOTE

Even if there is no change in the set value, writing ‘1’ to “_WEN” located in the upper 16 bits of the register starts the clock switching control. Therefore, it is necessary to wait until the switching is completed when monitoring their status (CPG_CLKSTATUS). (The clock stops temporarily when switching.)

48.5.2.16 NFI Clock Division Ratio Setting Register (CPG_NFI_DDIV)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.17 MMC/DDI Clock Division Ratio Setting Register (CPG_MMCDDI_DDIV)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.18 PLL/48 MHz Clock Source Setting Register (CPG_CLK48_DSEL)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.19 ISP Clock Division Ratio Setting Register 1 (CPG_ISP_DDIV1)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.20 ISP Clock Division Ratio Setting Register 2 (CPG_ISP_DDIV2)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.21 ISP Clock Source Setting Register (CPG_ISP_DSEL)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.22 Clock Status Monitor Register (CPG_CLKSTATUS)

This register monitors the clock change completion status of the dynamic changeable divider and selector.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0224h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	SELI_STS	SELH2_STS	SELH_STS	—	—	SELNFI_STS	SELG_STS	—	SELE_STS	SELD_STS	SELB_STS
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	DIVH2_STS	DIVM_STS	—	DIVI_STS	DIVH_STS	DIVX_STS	DIVNFI_STS	DIVG_STS	—	DIVE_STS	DIVD_STS	DIVB_STS	DIVA_STS
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 48.5-26 CPG_CLKSTATUS Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 27	—	Reserved. These bits are read as 0b.
26	SELI_STS	SELI clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
25	SELH2_STS	SELH2 clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
24	SELH_STS	SELH clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
23, 22	—	Reserved. These bits are read as 0b.
21	SELNFI_STS	SELNFI clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
20	SELG_STS	SELG clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
19	—	Reserved. When read, the value read is undefined.
18	SELE_STS	SELE clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
17	SELD_STS	SELD clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
16	SELB_STS	SELB clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
15 to 13	—	Reserved. These bits are read as 0b.
12	DIVH2_STS	DIVH2 clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)

Table 48.5-26 CPG_CLKSTATUS Register Contents (2/2)

Bit Position	Bit Name	Description
11	DIVM_STS	DIVM clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
10	—	Reserved. When read, the value read is undefined.
9	DIVI_STS	DIVI clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
8	DIVH_STS	DIVH clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
7	DIVX_STS	DIVX clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
6	DIVNFI_STS	DIVNFI clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
5	DIVG_STS	DIVG clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
4	—	Reserved. When read, the value read is undefined.
3	DIVE_STS	DIVE clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
2	DIVD_STS	DIVD clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
1	DIVB_STS	DIVB clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)
0	DIVA_STS	DIVA clock change completion status monitoring. 0b: Clock change completion 1b: Clock change incompletion (busy status)

48.5.2.23 SDI/EMM Clock Source Setting Register (CPG_SDIEMM_SSEL)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.24 STG Clock Division Ratio Setting Register (CPG_STG_SDIV)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.25 STG/CIF Clock Source Setting Register (CPG_STGCIF_SSEL)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.26 Display Clock Division Ratio Setting Register 1 (CPG_DISP_SDIV1)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.27 Display Clock Division Ratio Setting Register 2 (CPG_DISP_SDIV2)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.28 Display Clock Source Setting Register 1 (CPG_DISP_SSEL1)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.29 Display Clock Source Setting Register 2 (CPG_DISP_SSEL2)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.30 GMCLK Clock Division Ratio Setting Register (CPG_GMCLK_SDIV)

This register sets the division ratio of the GMCLK0 and 1 clocks.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 031Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DIVU_WEN	—	—	—	—	—	—	—	DIVT_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DIVU_SET				—	—	—	—	DIVT_SET			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	R	R	R	R	RW	RW	RW	RW

Table 48.5-27 CPG_GMCLK_SDIV Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24	DIVU_WEN	Enables write for DIVU_SET (bits 11-8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23 to 17	—	Reserved. These bits are read as 0b.
16	DIVT_WEN	Enables write for DIVT_SET (bits 3-0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b.
11 to 8	DIVU_SET	DIV U (GMCLK1) division ratio setting. (Source clock SEL U) 0000b: 1/1 0001b: 1/2 0010b: 1/4 0011b: 1/6 0100b: 1/8 0101b: 1/10 0110b: 1/12 0111b: 1/16 1000b: 1/20 1001b: 1/24 1010b: 1/32 1011b: 1/40 1100b: 1/48 Other than those above: Prohibited (when 1/1 is set)
7 to 4	—	Reserved. These bits are read as 0b.

Table 48.5-27 CPG_GMCLK_SDIV Register Contents (2/2)

Bit Position	Bit Name	Description
3 to 0	DIVT_SET	DIV T (GMCLK0) division ratio setting. (Source clock SEL T) 0000b: 1/1 0001b: 1/2 0010b: 1/4 0011b: 1/6 0100b: 1/8 0101b: 1/10 0110b: 1/12 0111b: 1/16 1000b: 1/20 1001b: 1/24 1010b: 1/32 1011b: 1/40 1100b: 1/48 Other than those above: Prohibited (when 1/1 is set)

48.5.2.31 GMCLK Clock Source Setting Register (CPG_GMCLK_SSEL)

This register switches the source clock of GMCLK0 and 1.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0320h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	SELU_WEN	—	—	—	—	—	—	—	SELT_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SELU_SET		—	—	—	—	—	—	SELT_SET	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	R	R	R	R	R	R	RW	RW

Table 48.5-28 CPG_GMCLK_SSEL Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24	SELU_WEN	Enables write for SELU_SET (bits 9-8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23 to 17	—	Reserved. These bits are read as 0b.
16	SELT_WEN	Enables write for SELT_SET (bits 1-0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 10	—	Reserved. These bits are read as 0b.
9, 8	SELU_SET	SEL U (GMCLK1) clock switching setting. 00b: 48 MHz clock 01b: 100 MHz clock 10b: PL4_SELCK clock 11b: DISPCLK (PLL7)
7 to 2	—	Reserved. These bits are read as 0b.
1, 0	SELT_SET	SEL T (GMCLK0) clock switching setting. 00b: 48 MHz clock 01b: 100 MHz clock 10b: PL4_SELCK clock 11b: DISPCLK (PLL7)

48.5.2.32 MTR Clock Source Setting Register (CPG_MTR_SSEL)

For more information on this register, contact a Renesas Electronics sales representative.

48.5.2.33 UART_REF Clock Division Ratio Setting Register (CPG_URT_RCLK_SDIV)

This register sets the division ratio of the sourced clock of UART0 and 1.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0328h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DIVW_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DIVW_SET		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 48.5-29 CPG_URT_RCLK_SDIV Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b.
16	DIVW_WEN	Enables write for DIVW_SET (bits 2-0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b.
2 to 0	DIVW_SET	DIV W division ratio setting (source clock PLL4) 000b: 1/6 001b: 1/7 010b: 1/8 011b: 1/9 100b: 1/10 101b: 1/11 110b: 1/12 111b: Prohibited (when 1/12 is set)

48.5.2.34 UART_REF Clock Source Setting Register (CPG_URT_RCLK_SSEL)

This register switches the source clock of UART0 and 1.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 032Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	SELW1_WEN	—	—	—	SELW0_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R0W1	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	SELW1_SET	—	—	—	SELW0_SET
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	R	R	R	RW

Table 48.5-30 CPG_URT_RCLK_SSEL Register Contents

Bit Position	Bit Name	Description
31 to 21	—	Reserved. These bits are read as 0b.
20	SELW1_WEN	Enables write for SELW1_SET (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19 to 17	—	Reserved. These bits are read as 0b.
16	SELW0_WEN	Enables write for SELW0_SET (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 5	—	Reserved. These bits are read as 0b.
4	SELW1_SET	UART1 clock switching setting. 0b: 48 MHz clock 1b: DIV W clock
3 to 1	—	Reserved. These bits are read as 0b.
0	SELW0_SET	UART0 clock switching setting. 0b: 48 MHz clock 1b: DIV W clock

48.5.2.35 CSI_REF Clock Source Setting Register (CPG_CSI_RCLK_SSEL)

This register switches the source clock of CSI[0-5].

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as ‘0’.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0330h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	SELCSI5_WEN*	SELCSI4_WEN	SELCSI3_WEN*	SELCSI2_WEN*	SELCSI1_WEN*	SELCSI0_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	SELCSI5_SET	SELCSI4_SET	SELCSI3_SET	SELCSI2_SET	SELCSI1_SET	SELCSI0_SET
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 48.5-31 CPG_CSI_RCLK_SSEL Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b.
21*	SELCSI5_WEN	Enables write for SELCSI5_SET (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	SELCSI4_WEN	Enables write for SELCSI4_SET (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19*	SELCSI3_WEN	Enables write for SELCSI3_SET (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18*	SELCSI2_WEN	Enables write for SELCSI2_SET (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17*	SELCSI1_WEN	Enables write for SELCSI1_SET (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	SELCSI0_WEN	Enables write for SELCSI0_SET (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b.
5	SELCSI5_SET	CSI5 clock switching setting. 0b: 24 MHz clock 1b: 48 MHz clock
4	SELCSI4_SET	CSI4 clock switching setting. 0b: 24 MHz clock 1b: 48 MHz clock
3	SELCSI3_SET	CSI3 clock switching setting. 0b: 24 MHz clock 1b: 48 MHz clock

Table 48.5-31 CPG_CSI_RCLK_SSEL Register Contents (2/2)

Bit Position	Bit Name	Description
2	SELCSI2_SET	CSI2 clock switching setting. 0b: 24 MHz clock 1b: 48 MHz clock
1	SELCSI1_SET	CSI1 clock switching setting. 0b: 24 MHz clock 1b: 48 MHz clock
0	SELCSI0_SET	CSI0 clock switching setting. 0b: 24 MHz clock 1b: 48 MHz clock

48.5.2.36 Clock ON/OFF Control Register 1 (CPG_CLK_ON1)

This register turns each unit clock on or off (AWO SYSTEM clock control).

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as '0'.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0400h

Initial Value: 0000_FFFEh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CLK15_ONWEN*	CLK14_ONWEN*	—	—	CLK11_ONWEN*	CLK10_ONWEN*	CLK9_ONWEN*	CLK8_ONWEN*	CLK7_ONWEN*	CLK6_ONWEN	CLK5_ONWEN*	CLK4_ONWEN*	—	CLK2_ONWEN*	CLK1_ONWEN*	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLK15_ON	CLK14_ON	—	—	CLK11_ON	CLK10_ON	CLK9_ON	CLK8_ON	CLK7_ON	CLK6_ON	CLK5_ON	CLK4_ON	—	CLK2_ON	CLK1_ON	—
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R

Table 48.5-32 CPG_CLK_ON1 Register Contents (1/2)

Bit Position	Bit Name	Description
31*	CLK15_ONWEN	Enables write for CLK15_ON (bit 15). Write only. Read as 0b. 0b: Write disable 1b: Write enable
30*	CLK14_ONWEN	Enables write for CLK14_ON (bit 14). Write only. Read as 0b. 0b: Write disable 1b: Write enable
29, 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27*	CLK11_ONWEN	Enables write for CLK11_ON (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26*	CLK10_ONWEN	Enables write for CLK10_ON (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25*	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24*	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23*	CLK7_ONWEN	Enables write for CLK7_ON (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	CLK6_ONWEN	Enables write for CLK6_ON (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21*	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-32 CPG_CLK_ON1 Register Contents (2/2)

Bit Position	Bit Name	Description
20*	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18*	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17*	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	—	Reserved. This bit is read as 0b.
15	CLK15_ON	TSU1_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
14	CLK14_ON	TSU0_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
13, 12	—	Reserved. When read, the value read is undefined.
11	CLK11_ON	DMAA_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
10	CLK10_ON	SEC_TCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
9	CLK9_ON	SEC_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	SEC_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7	CLK7_ON	ROM_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
6	CLK6_ON	RAMA_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
5	CLK5_ON	GIC_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	PMC_CORE_CLOCK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3	—	Reserved. When read, the value read is undefined.
2	CLK2_ON	PFC_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
1	CLK1_ON	SYS_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	—	Reserved. This bit is read as 0b.

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.37 Clock ON/OFF Control Register 2 (CPG_CLK_ON2)

This register turns each unit clock on or off (AWO CoreSight clock control).

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0404h

Initial Value: 0000_001Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	CLK4_ONWEN	—	CLK2_ONWEN	CLK1_ONWEN	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	CLK4_ON	—	CLK2_ON	CLK1_ON	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW

Table 48.5-33 CPG_CLK_ON2 Register Contents

Bit Position	Bit Name	Description
31 to 21	—	Reserved. These bits are read as 0b.
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b. The write value should always be 0b.
18	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 5	—	Reserved. These bits are read as 0b.
4	CLK4_ON	CST_ATB_SB_CLK, CST_TS_SB_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3	—	Reserved. When read, the value read is undefined.
2	CLK2_ON	CST_AHB_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
1	CLK1_ON	CST_SB_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	CLK0_ON	CST_TRACECLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.38 Clock ON/OFF Control Register 3 (CPG_CLK_ON3)

This register turns each unit clock on or off (AWO storage system clock control).

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0408h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	CLK13_ONWEN	CLK12_ONWEN	CLK11_ONWEN	CLK10_ONWEN	CLK9_ONWEN	CLK8_ONWEN	CLK7_ONWEN	CLK6_ONWEN	CLK5_ONWEN	CLK4_ONWEN	CLK3_ONWEN	CLK2_ONWEN	CLK1_ONWEN	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CLK13_ON	CLK12_ON	CLK11_ON	CLK10_ON	CLK9_ON	CLK8_ON	CLK7_ON	CLK6_ON	CLK5_ON	CLK4_ON	CLK3_ON	CLK2_ON	CLK1_ON	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 48.5-34 CPG_CLK_ON3 Register Contents (1/3)

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29	CLK13_ONWEN	Enables write for CLK13_ON (bit 13). Write only. Read as 0b. 0b: Write disable 1b: Write enable
28	CLK12_ONWEN	Enables write for CLK12_ON (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	CLK11_ONWEN	Enables write for CLK11_ON (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26	CLK10_ONWEN	Enables write for CLK10_ON (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	CLK7_ONWEN	Enables write for CLK7_ON (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	CLK6_ONWEN	Enables write for CLK6_ON (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-34 CPG_CLK_ON3 Register Contents (2/3)

Bit Position	Bit Name	Description
19	CLK3_ONWEN	Enables write for CLK3_ON (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b.
13	CLK13_ON	NFI_NF_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
12	CLK12_ON	NFI_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
11	CLK11_ON	EMM_CLK_HS switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
10	CLK10_ON	EMM_IMCLK2 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
9	CLK9_ON	EMM_IMCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	EMM_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7	CLK7_ON	SDI1_CLK_HS switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
6	CLK6_ON	SDI1_IMCLK2 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
5	CLK5_ON	SDI1_IMCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	SDI1_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3	CLK3_ON	SDI0_CLK_HS switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
2	CLK2_ON	SDI0_IMCLK2 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

Table 48.5-34 CPG_CLK_ON3 Register Contents (3/3)

Bit Position	Bit Name	Description
1	CLK1_ON	SDI0_IMCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	CLK0_ON	SDI0_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.39 Clock ON/OFF Control Register 4 (CPG_CLK_ON4)

This register turns each unit clock on or off (AWO PCIe, USB, and ETHER clock control).

Access Size: 32 bits

Address(es): <CPG_S0_base> + 040Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	CLK9_ONWEN	CLK8_ONWEN	—	CLK6_ONWEN	CLK5_ONWEN	CLK4_ONWEN	—	CLK2_ONWEN	CLK1_ONWEN	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CLK9_ON	CLK8_ON	—	CLK6_ON	CLK5_ON	CLK4_ON	—	CLK2_ON	CLK1_ON	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	R	RW	RW	RW	R	RW	RW	RW

Table 48.5-35 CPG_CLK_ON4 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 26	—	Reserved. These bits are read as 0b.
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b.
22	CLK6_ONWEN	Enables write for CLK6_ON (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b.
18	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 10	—	Reserved. These bits are read as 0b.
9	CLK9_ON	ETH0_CLK_GPTP_EXTERN switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

Table 48.5-35 CPG_CLK_ON4 Register Contents (2/2)

Bit Position	Bit Name	Description
8	CLK8_ON	ETH0_CLK_AXI, ETH0_CLK_CHI switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7	—	Reserved. This bit is read as 0b.
6	CLK6_ON	USB_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
5	CLK5_ON	USB_ACLK_P switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	USB_ACLK_H switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3	—	Reserved. This bit is read as 0b.
2	CLK2_ON	PCI_APB_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
1	CLK1_ON	PCI_CLK_PMU switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	CLK0_ON	PCI_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching of ETH0_CLK_AXI and ETH0_CLK_CHI is reflected after register setting (synchronization with 48 MHz) and 2 * ETH0_CLK_CHI + 4 * ETH0_CLK_AXI. On/off switching of other clocks is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.40 Clock ON/OFF Control Register 5 (CPG_CLK_ON5)

This register turns each unit clock on or off (AWO ESI, GRP, CIF, and DCU clock control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0410h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CLK12_ONWEN	—	—	CLK9_ONWEN	CLK8_ONWEN	—	CLK6_ONWEN	CLK5_ONWEN	CLK4_ONWEN	CLK3_ONWEN	CLK2_ONWEN	CLK1_ONWEN	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R0W1	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CLK12_ON	—	—	CLK9_ON	CLK8_ON	—	CLK6_ON	CLK5_ON	CLK4_ON	CLK3_ON	CLK2_ON	CLK1_ON	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	RW	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 48.5-36 CPG_CLK_ON5 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 29	—	Reserved. These bits are read as 0b.
28	CLK12_ONWEN	Enables write for CLK12_ON (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27, 26	—	Reserved. These bits are read as 0b.
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b. The write value should always be 0b.
22	CLK6_ONWEN	Enables write for CLK6_ON (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	CLK3_ONWEN	Enables write for CLK3_ON (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-36 CPG_CLK_ON5 Register Contents (2/2)

Bit Position	Bit Name	Description
17	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 13	—	Reserved. These bits are read as 0b.
12	CLK12_ON	DCI_CLKDCI2 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
11, 10	—	Reserved. These bits are read as 0b.
9	CLK9_ON	DCI_CLKAPB switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	DCI_CLKAXI switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7	—	Reserved. When read, the value read is undefined.
6	CLK6_ON	CIF_APB_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
5	CLK5_ON	CIF_P1_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	CIF_P0_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3	CLK3_ON	GRP_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
2	CLK2_ON	SDT_CLK48 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
1	CLK1_ON	SDT_CLKAPB switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1 Clock ON (Clock supply state)
0	CLK0_ON	SDT_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.41 Clock ON/OFF Control Register 6 (CPG_CLK_ON6)

This register turns each unit clock on or off (AWO HDMI and LCI clock control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0414h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	CLK11_ONWEN	CLK10_ONWEN	CLK9_ONWEN	CLK8_ONWEN	—	—	—	—	—	—	—	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CLK11_ON	CLK10_ON	CLK9_ON	CLK8_ON	—	—	—	—	—	—	—	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	R	R	R	R	R	R	R	RW

Table 48.5-37 CPG_CLK_ON6 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b.
27	CLK11_ONWEN	Enables write for CLK11_ON (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26	CLK10_ONWEN	Enables write for CLK10_ON (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23 to 17	—	Reserved. These bits are read as 0b.
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b.
11	CLK11_ON	LCI_LPCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
10	CLK10_ON	LCI_VCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
9	CLK9_ON	LCI_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	LCI_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

Table 48.5-37 CPG_CLK_ON6 Register Contents (2/2)

Bit Position	Bit Name	Description
7 to 1	—	Reserved. These bits are read as 0b.
0	CLK0_ON	HMI_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.42 Clock ON/OFF Control Register 7 (CPG_CLK_ON7)

This register turns each unit clock on or off (AWO AUI, general purpose clock, and ISP clock control)

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as '0'.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0418h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	CLK14_ONWEN*	CLK13_ONWEN*	CLK12_ONWEN*	—	CLK10_ONWEN*	CLK9_ONWEN*	CLK8_ONWEN*	—	—	CLK5_ONWEN	CLK4_ONWEN	CLK3_ONWEN*	CLK2_ONWEN*	CLK1_ONWEN*	CLK0_ONWEN*
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	CLK14_ON	CLK13_ON	CLK12_ON	—	CLK10_ON	CLK9_ON	CLK8_ON	—	—	CLK5_ON	CLK4_ON	CLK3_ON	CLK2_ON	CLK1_ON	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	RW	RW	RW	R	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 48.5-38 CPG_CLK_ON7 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b.
30*	CLK14_ONWEN	Enables write for CLK14_ON (bit 14). Write only. Read as 0b. 0b: Write disable 1b: Write enable
29*	CLK13_ONWEN	Enables write for CLK13_ON (bit 13). Write only. Read as 0b. 0b: Write disable 1b: Write enable
28*	CLK12_ONWEN	Enables write for CLK12_ON (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b.
26*	CLK10_ONWEN	Enables write for CLK10_ON (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25*	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24*	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23, 22	—	Reserved. These bits are read as 0b.
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-38 CPG_CLK_ON7 Register Contents (2/2)

Bit Position	Bit Name	Description
19*	CLK3_ONWEN	Enables write for CLK3_ON (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18*	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17*	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16*	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b.
14	CLK14_ON	GFT_MCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
13	CLK13_ON	GFT_CLKAPB switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
12	CLK12_ON	GFT_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
11	—	Reserved. This bit is read as 0b.
10	CLK10_ON	MTR_CLKAPB switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
9	CLK9_ON	MTR_CLK1 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	MTR_CLK0 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7, 6	—	Reserved. These bits are read as 0b.
5	CLK5_ON	General purpose clock GMCLK1 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	General purpose clock GMCLK0 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3	CLK3_ON	AUMCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
2	CLK2_ON	AUI_CLKAPB switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
1	CLK1_ON	AUI_CLKAXI switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	CLK0_ON	AUI_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.43 Clock ON/OFF Control Register 8 (CPG_CLK_ON8)

This register turns each unit clock on or off (AWO ADC and SYC clock control).

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as '0'.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 041Ch

Initial Value: 0000_2000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CLK12_ONWEN	—	—	—	—	—	—	—	—	CLK3_ONWEN*	CLK2_ONWEN*	CLK1_ONWEN*	CLK0_ONWEN*
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CLK12_ON	—	—	—	—	—	—	—	—	CLK3_ON	CLK2_ON	CLK1_ON	CLK0_ON
Initial Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 48.5-39 CPG_CLK_ON8 Register Contents (1/2)

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29	—	Reserved. This bit is read as 0b. The write value should always be 0b.
28	CLK12_ONWEN	Enables write for CLK12_ON (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b.
26 to 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19*	CLK3_ONWEN	Enables write for CLK3_ON (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18*	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17*	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16*	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b.
13	—	Reserved. When read, the value read is undefined.
12	CLK12_ON	SYC_CNT_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
11	—	Reserved. This bit is read as 0b.
10 to 4	—	Reserved. When read, the value read is undefined.
3	CLK3_ON	ATGB_CLKAPB switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

Table 48.5-39 CPG_CLK_ON8 Register Contents (2/2)

Bit Position	Bit Name	Description
2	CLK2_ON	ATGB_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
1	CLK1_ON	ATGA_CLKAPB switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	CLK0_ON	ATGA_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.44 Clock ON/OFF Control Register 9 (CPG_CLK_ON9)

This register turns each unit clock on or off (AWO Peripheral Group A clock control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0420h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CLK12_ONWEN	CLK11_ONWEN	CLK10_ONWEN	CLK9_ONWEN	CLK8_ONWEN	CLK7_ONWEN	CLK6_ONWEN	CLK5_ONWEN	CLK4_ONWEN	—	—	—	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CLK12_ON	CLK11_ON	CLK10_ON	CLK9_ON	CLK8_ON	CLK7_ON	CLK6_ON	CLK5_ON	CLK4_ON	—	—	—	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	RW

Table 48.5-40 CPG_CLK_ON9 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 29	—	Reserved. These bits are read as 0b.
28	CLK12_ONWEN	Enables write for CLK12_ON (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	CLK11_ONWEN	Enables write for CLK11_ON (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26	CLK10_ONWEN	Enables write for CLK10_ON (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	CLK7_ONWEN	Enables write for CLK7_ON (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	CLK6_ONWEN	Enables write for CLK6_ON (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19 to 17	—	Reserved. These bits are read as 0b.

Table 48.5-40 CPG_CLK_ON9 Register Contents (2/2)

Bit Position	Bit Name	Description
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 13	—	Reserved. These bits are read as 0b.
12	CLK12_ON	IIC_PCLK[0] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
11	CLK11_ON	TIM_CLK[7] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
10	CLK10_ON	TIM_CLK[6] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
9	CLK9_ON	TIM_CLK[5] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	TIM_CLK[4] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7	CLK7_ON	TIM_CLK[3] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
6	CLK6_ON	TIM_CLK[2] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
5	CLK5_ON	TIM_CLK[1] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	TIM_CLK[0] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3 to 1	—	Reserved. These bits are read as 0b.
0	CLK0_ON	CPERI_GRPA_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.45 Clock ON/OFF Control Register 10 (CPG_CLK_ON10)

This register turns each unit clock on or off (AWO Peripheral Group B clock control).

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as '0'.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0424h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CLK12_ONWEN*	CLK11_ONWEN	CLK10_ONWEN	CLK9_ONWEN	CLK8_ONWEN	CLK7_ONWEN	CLK6_ONWEN	CLK5_ONWEN	CLK4_ONWEN	—	—	—	CLK0_ONWEN*
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CLK12_ON	CLK11_ON	CLK10_ON	CLK9_ON	CLK8_ON	CLK7_ON	CLK6_ON	CLK5_ON	CLK4_ON	—	—	—	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	RW

Table 48.5-41 CPG_CLK_ON10 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 29	—	Reserved. These bits are read as 0b.
28*	CLK12_ONWEN	Enables write for CLK12_ON (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	CLK11_ONWEN	Enables write for CLK11_ON (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26	CLK10_ONWEN	Enables write for CLK10_ON (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	CLK7_ONWEN	Enables write for CLK7_ON (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	CLK6_ONWEN	Enables write for CLK6_ON (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19 to 17	—	Reserved. These bits are read as 0b.

Table 48.5-41 CPG_CLK_ON10 Register Contents (2/2)

Bit Position	Bit Name	Description
16*	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 13	—	Reserved. These bits are read as 0b.
12	CLK12_ON	IIC_PCLK[1] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
11	CLK11_ON	TIM_CLK[15] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
10	CLK10_ON	TIM_CLK[14] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
9	CLK9_ON	TIM_CLK[13] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	TIM_CLK[12] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7	CLK7_ON	TIM_CLK[11] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
6	CLK6_ON	TIM_CLK[10] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
5	CLK5_ON	TIM_CLK[9] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	TIM_CLK[8] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3 to 1	—	Reserved. These bits are read as 0b.
0	CLK0_ON	CPERI_GRPB_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.46 Clock ON/OFF Control Register 11 (CPG_CLK_ON11)

This register turns each unit clock on or off (AWO Peripheral Group C clock control).

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as '0'.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0428h

Initial Value: 0000_F000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CLK15_ONWEN*	CLK14_ONWEN*	CLK13_ONWEN	CLK12_ONWEN	CLK11_ONWEN	CLK10_ONWEN	CLK9_ONWEN	CLK8_ONWEN	CLK7_ONWEN	CLK6_ONWEN	CLK5_ONWEN	CLK4_ONWEN	—	—	—	CLK0_ONWEN*
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLK15_ON	CLK14_ON	CLK13_ON	CLK12_ON	CLK11_ON	CLK10_ON	CLK9_ON	CLK8_ON	CLK7_ON	CLK6_ON	CLK5_ON	CLK4_ON	—	—	—	CLK0_ON
Initial Value	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	RW

Table 48.5-42 CPG_CLK_ON11 Register Contents (1/2)

Bit Position	Bit Name	Description
31*	CLK15_ONWEN	Enables write for CLK15_ON (bit 15). Write only. Read as 0b. 0b: Write disable 1b: Write enable
30*	CLK14_ONWEN	Enables write for CLK14_ON (bit 14). Write only. Read as 0b. 0b: Write disable 1b: Write enable
29	CLK13_ONWEN	Enables write for CLK13_ON (bit 13). Write only. Read as 0b. 0b: Write disable 1b: Write enable
28	CLK12_ONWEN	Enables write for CLK12_ON (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	CLK11_ONWEN	Enables write for CLK11_ON (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26	CLK10_ONWEN	Enables write for CLK10_ON (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	CLK7_ONWEN	Enables write for CLK7_ON (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	CLK6_ONWEN	Enables write for CLK6_ON (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-42 CPG_CLK_ON11 Register Contents (2/2)

Bit Position	Bit Name	Description
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19 to 17	—	Reserved. These bits are read as 0b.
16*	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	CLK15_ON	WDT_CLK[1] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
14	CLK14_ON	WDT_PCLK[1] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
13	CLK13_ON	WDT_CLK[0] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
12	CLK12_ON	WDT_PCLK[0] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
11	CLK11_ON	TIM_CLK[23] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
10	CLK10_ON	TIM_CLK[22] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
9	CLK9_ON	TIM_CLK[21] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	TIM_CLK[20] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7	CLK7_ON	TIM_CLK[19] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
6	CLK6_ON	TIM_CLK[18] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
5	CLK5_ON	TIM_CLK[17] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	TIM_CLK[16] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3 to 1	—	Reserved. These bits are read as 0b.
0	CLK0_ON	CPERI_GRPC_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.47 Clock ON/OFF Control Register 12 (CPG_CLK_ON12)

This register turns each unit clock on or off (AWO Peripheral Group D clock control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 042Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	CLK11_ONWEN	CLK10_ONWEN	CLK9_ONWEN	CLK8_ONWEN	CLK7_ONWEN	CLK6_ONWEN	CLK5_ONWEN	CLK4_ONWEN	—	—	—	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CLK11_ON	CLK10_ON	CLK9_ON	CLK8_ON	CLK7_ON	CLK6_ON	CLK5_ON	CLK4_ON	—	—	—	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	RW

Table 48.5-43 CPG_CLK_ON12 Register Contents (1/2)

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29, 28	—	Reserved. These bits are read as 0b. The write value should always be 0b.
27	CLK11_ONWEN	Enables write for CLK11_ON (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26	CLK10_ONWEN	Enables write for CLK10_ON (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	CLK7_ONWEN	Enables write for CLK7_ON (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	CLK6_ONWEN	Enables write for CLK6_ON (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19 to 17	—	Reserved. These bits are read as 0b.
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-43 CPG_CLK_ON12 Register Contents (2/2)

Bit Position	Bit Name	Description
15, 14	—	Reserved. These bits are read as 0b.
13, 12	—	Reserved. When read, the value read is undefined.
11	CLK11_ON	TIM_CLK[31] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
10	CLK10_ON	TIM_CLK[30] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
9	CLK9_ON	TIM_CLK[29] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	TIM_CLK[28] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7	CLK7_ON	TIM_CLK[27] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
6	CLK6_ON	TIM_CLK[26] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
5	CLK5_ON	TIM_CLK[25] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	TIM_CLK[24] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3 to 1	—	Reserved. These bits are read as 0b.
0	CLK0_ON	CPERI_GRPD_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.48 Clock ON/OFF Control Register 13 (CPG_CLK_ON13)

This register turns each unit clock on or off (AWO Peripheral Group E clock control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0430h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	CLK11_ONWEN	CLK10_ONWEN	CLK9_ONWEN	CLK8_ONWEN	CLK7_ONWEN	CLK6_ONWEN	CLK5_ONWEN	CLK4_ONWEN	—	—	—	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CLK11_ON	CLK10_ON	CLK9_ON	CLK8_ON	CLK7_ON	CLK6_ON	CLK5_ON	CLK4_ON	—	—	—	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	RW

Table 48.5-44 CPG_CLK_ON13 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b.
27	CLK11_ONWEN	Enables write for CLK11_ON (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26	CLK10_ONWEN	Enables write for CLK10_ON (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	CLK7_ONWEN	Enables write for CLK7_ON (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	CLK6_ONWEN	Enables write for CLK6_ON (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19 to 17	—	Reserved. These bits are read as 0b.
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b.

Table 48.5-44 CPG_CLK_ON13 Register Contents (2/2)

Bit Position	Bit Name	Description
11	CLK11_ON	PWM_CLK[7] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
10	CLK10_ON	PWM_CLK[6] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
9	CLK9_ON	PWM_CLK[5] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	PWM_CLK[4] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7	CLK7_ON	PWM_CLK[3] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
6	CLK6_ON	PWM_CLK[2] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
5	CLK5_ON	PWM_CLK[1] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	PWM_CLK[0] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3 to 1	—	Reserved. These bits are read as 0b.
0	CLK0_ON	CPERI_GRPE_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.49 Clock ON/OFF Control Register 14 (CPG_CLK_ON14)

This register turns each unit clock on or off (AWO Peripheral Group F clock control).

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as '0'.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0434h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	CLK11_ONWEN*	CLK10_ONWEN	CLK9_ONWEN	CLK8_ONWEN	CLK7_ONWEN	CLK6_ONWEN	CLK5_ONWEN	CLK4_ONWEN	—	—	—	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CLK11_ON	CLK10_ON	CLK9_ON	CLK8_ON	CLK7_ON	CLK6_ON	CLK5_ON	CLK4_ON	—	—	—	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	RW

Table 48.5-45 CPG_CLK_ON14 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b.
27*	CLK11_ONWEN	Enables write for CLK11_ON (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26	CLK10_ONWEN	Enables write for CLK10_ON (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	CLK7_ONWEN	Enables write for CLK7_ON (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	CLK6_ONWEN	Enables write for CLK6_ON (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19 to 17	—	Reserved. These bits are read as 0b.

Table 48.5-45 CPG_CLK_ON14 Register Contents (2/2)

Bit Position	Bit Name	Description
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 12	—	Reserved. These bits are read as 0b.
11	CLK11_ON	PWM_CLK[15] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
10	CLK10_ON	PWM_CLK[14] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
9	CLK9_ON	PWM_CLK[13] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	PWM_CLK[12] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7	CLK7_ON	PWM_CLK[11] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
6	CLK6_ON	PWM_CLK[10] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
5	CLK5_ON	PWM_CLK[9] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	PWM_CLK[8] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3 to 1	—	Reserved. These bits are read as 0b.
0	CLK0_ON	CPERI_GRPF_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.50 Clock ON/OFF Control Register 15 (CPG_CLK_ON15)

This register turns each unit clock on or off (AWO Peripheral Group G and H clock control).

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as '0'.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0438h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	CLK13_ONWEN*	CLK12_ONWEN	CLK11_ONWEN*	CLK10_ONWEN*	CLK9_ONWEN*	CLK8_ONWEN	—	CLK6_ONWEN*	CLK5_ONWEN	CLK4_ONWEN*	—	—	CLK1_ONWEN*	CLK0_ONWEN*
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R	R	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CLK13_ON	CLK12_ON	CLK11_ON	CLK10_ON	CLK9_ON	CLK8_ON	—	CLK6_ON	CLK5_ON	CLK4_ON	—	—	CLK1_ON	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	RW	RW	RW	R	R	RW	RW

Table 48.5-46 CPG_CLK_ON15 Register Contents (1/2)

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29*	CLK13_ONWEN	Enables write for CLK13_ON (bit 13). Write only. Read as 0b. 0b: Write disable 1b: Write enable
28	CLK12_ONWEN	Enables write for CLK12_ON (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27*	CLK11_ONWEN	Enables write for CLK11_ON (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26*	CLK10_ONWEN	Enables write for CLK10_ON (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25*	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. These bits are read as 0b.
22*	CLK6_ONWEN	Enables write for CLK6_ON (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20*	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-46 CPG_CLK_ON15 Register Contents (2/2)

Bit Position	Bit Name	Description
19, 18	—	Reserved. These bits are read as 0b.
17*	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16*	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b.
13	CLK13_ON	CSI_CLK[5] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
12	CLK12_ON	CSI_CLK[4] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
11	CLK11_ON	CSI_CLK[3] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
10	CLK10_ON	CSI_CLK[2] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
9	CLK9_ON	CSI_CLK[1] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	CSI_CLK[0] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7	—	Reserved. This bit is read as 0b.
6	CLK6_ON	URT_CLK[1] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
5	CLK5_ON	URT_CLK[0] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	URT_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3, 2	—	Reserved. These bits are read as 0b.
1	CLK1_ON	CPERI_GRPH_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	CLK0_ON	CPERI_GRPG_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.51 Clock ON/OFF Control Register 16 (CPG_CLK_ON16)

This register turns each unit clock on or off (ICB clock control 1).

Changing this register is prohibited because doing so causes system deadlock.

For details, see **Section 48.8.11, Register Control of CPG_CLK_ON16 and CPG_CLK_ON17**.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 043Ch

Initial Value: 0000_FC1Dh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CLK15_ONWEN	CLK14_ONWEN	CLK13_ONWEN	CLK12_ONWEN	CLK11_ONWEN	CLK10_ONWEN	CLK9_ONWEN	—	CLK7_ONWEN	CLK6_ONWEN	CLK5_ONWEN	CLK4_ONWEN	CLK3_ONWEN	CLK2_ONWEN	—	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLK15_ON	CLK14_ON	CLK13_ON	CLK12_ON	CLK11_ON	CLK10_ON	CLK9_ON	—	CLK7_ON	CLK6_ON	CLK5_ON	CLK4_ON	CLK3_ON	CLK2_ON	—	CLK0_ON
Initial Value	1	1	1	1	1	1	0	0	0	0	0	1	1	1	0	1
R/W	RW	RW	RW	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	R	RW

Table 48.5-47 CPG_CLK_ON16 Register Contents (1/3)

Bit Position	Bit Name	Description
31	CLK15_ONWEN	Enables write for CLK15_ON (bit 15). Write only. Read as 0b. 0b: Write disable 1b: Write enable
30	CLK14_ONWEN	Enables write for CLK14_ON (bit 14). Write only. Read as 0b. 0b: Write disable 1b: Write enable
29	CLK13_ONWEN	Enables write for CLK13_ON (bit 13). Write only. Read as 0b. 0b: Write disable 1b: Write enable
28	CLK12_ONWEN	Enables write for CLK12_ON (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	CLK11_ONWEN	Enables write for CLK11_ON (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26	CLK10_ONWEN	Enables write for CLK10_ON (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	—	Reserved. This bit is read as 0b.
23	CLK7_ONWEN	Enables write for CLK7_ON (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	CLK6_ONWEN	Enables write for CLK6_ON (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-47 CPG_CLK_ON16 Register Contents (2/3)

Bit Position	Bit Name	Description
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	CLK3_ONWEN	Enables write for CLK3_ON (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	—	Reserved. This bit is read as 0b.
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	CLK15_ON	ICB_SYC_CNT_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
14	CLK14_ON	ICB_DCI_CLKAXI switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
13	CLK13_ON	ICB_ETH0_CLK_AXI switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
12	CLK12_ON	ICB_CLK100_1 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
11	CLK11_ON	ICB_CST_CS_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
10	CLK10_ON	ICB_CST_ATB_SB_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
9	CLK9_ON	ICB_CLK48_5 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	—	Reserved. This bit is read as 0b.
7	CLK7_ON	ICB_CLK48_4L, ICB_CLK48_4R switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
6	CLK6_ON	ICB_CLK48_3 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
5	CLK5_ON	ICB_CLK48_2 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	ICB_CLK48 switches ON/OFF. *Note*: Setting to OFF is prohibited due to deadlock. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

Table 48.5-47 CPG_CLK_ON16 Register Contents (3/3)

Bit Position	Bit Name	Description
3	CLK3_ON	ICB_SPCLK1 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
2	CLK2_ON	ICB_MPCLK1 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
1	—	Reserved. This bit is read as 0b.
0	CLK0_ON	ICB_ACLK1, ICB_GIC_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- ICB_ACLK1 and ICB_GIC_CLK on/off switching is reflected after register setting (synchronization with 48 MHz) and 2 * ICB_GIC_CLK + 4 * ICB_ACLK1. Other clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.52 Clock ON/OFF Control Register 17 (CPG_CLK_ON17)

This register turns each unit clock on or off (ICB clock control 2).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0440h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	CLK8_ONWEN	—	—	—	CLK4_ONWEN	—	—	—	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R	R0W1	R	R0W1	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CLK8_ON	—	—	—	CLK4_ON	—	—	—	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	RW	R	RW	R	RW	R	R	R	RW

Table 48.5-48 CPG_CLK_ON17 Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	—	Reserved. This bit is read as 0b.
22	—	Reserved. This bit is read as 0b. The write value should always be 0b.
21	—	Reserved. This bit is read as 0b.
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19 to 17	—	Reserved. These bits are read as 0b.
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b.
8	CLK8_ON	ICB_MMC_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7	—	Reserved. This bit is read as 0b.
6	—	Reserved. When read, the value read is undefined.
5	—	Reserved. This bit is read as 0b.
4	CLK4_ON	ICB_RFX_ACLK, ICB_RFX_PCLK5 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3 to 1	—	Reserved. These bits are read as 0b.
0	CLK0_ON	ICB_DRPA_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- ICB_RFX_ACLK, ICB_RFX_PCLK5 on/off switching is reflected after register setting (synchronization with 48 MHz) and 2*ICB_RFX_PCLK5+4*ICB_RFX_ACLK. Other clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.53 Clock ON/OFF Control Register 18 (CPG_CLK_ON18)

This register turns each unit clock on or off (ICB clock control 3).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0444h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	CLK13_ONWEN	CLK12_ONWEN	CLK11_ONWEN	—	CLK9_ONWEN	CLK8_ONWEN	—	—	—	—	—	CLK2_ONWEN	CLK1_ONWEN	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CLK13_ON	CLK12_ON	CLK11_ON	—	CLK9_ON	CLK8_ON	—	—	—	—	—	CLK2_ON	CLK1_ON	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	R	R	R	RW	RW	RW

Table 48.5-49 CPG_CLK_ON18 Register Contents (1/2)

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29	CLK13_ONWEN	Enables write for CLK13_ON (bit 13). Write only. Read as 0b. 0b: Write disable 1b: Write enable
28	CLK12_ONWEN	Enables write for CLK12_ON (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	CLK11_ONWEN	Enables write for CLK11_ON (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26	—	Reserved. This bit is read as 0b. The write value should always be 0b.
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23 to 19	—	Reserved. These bits are read as 0b.
18	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15, 14	—	Reserved. These bits are read as 0b.

Table 48.5-49 CPG_CLK_ON18 Register Contents (2/2)

Bit Position	Bit Name	Description
13	CLK13_ON	ICB_VCD_PCLK4 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
12	CLK12_ON	ICB_MPCLK4 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
11	CLK11_ON	ICB_VD_ACLK4 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
10	—	Reserved. When read, the value read is undefined.
9	CLK9_ON	ICB_FCD_CLKAXI switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	ICB_BIMA_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7 to 3	—	Reserved. These bits are read as 0b.
2	CLK3_ON	ICB_CIMB_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
1	CLK1_ON	ICB_CIMA_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	CLK0_ON	ICB_MPCLK3 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.54 Clock ON/OFF Control Register 19 (CPG_CLK_ON19)

This register turns each unit clock on or off (CA53 system PD CA53 clock control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0448h

Initial Value: 0000_003Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CLK5_ONWEN	CLK4_ONWEN	CLK3_ONWEN	CLK2_ONWEN	CLK1_ONWEN	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	CLK5_ON	CLK4_ON	CLK3_ON	CLK2_ON	CLK1_ON	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 48.5-50 CPG_CLK_ON19 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b.
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	CLK3_ONWEN	Enables write for CLK3_ON (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b.
5	CLK5_ON	CA53_APCLK_REG switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	CA53_TSCLK, CST_TS_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3	CLK3_ON	CA53_ATCLK, CST_CS_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

Table 48.5-50 CPG_CLK_ON19 Register Contents (2/2)

Bit Position	Bit Name	Description
2	CLK2_ON	CA53_APCLK_DBG, CST_APB_CA53_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
1	CLK1_ON	CA53_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	CLK0_ON	CA53_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- CA53_CLK on/off switching is reflected after register setting (synchronization with 48 MHz) and 10*CA53_CLK. Other clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.55 Clock ON/OFF Control Register 20 (CPG_CLK_ON20)

This register turns each unit clock on or off (DRP system PD DRPA clock control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 044Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	CLK2_ONWEN	CLK1_ONWEN	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	CLK2_ON	CLK1_ON	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 48.5-51 CPG_CLK_ON20 Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b.
18	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b.
2	CLK2_ON	DRPA_INITCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
1	CLK1_ON	DRPA_DCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	CLK0_ON	DRPA_ACLK(MCLK) switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- DRPA_DCLK on/off switching is reflected after register setting (synchronization with 48 MHz) and 4*DRPA_DCLK. Other clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.56 Clock ON/OFF Control Register 23 (CPG_CLK_ON23)

This register turns each unit clock on or off (RAMB system PD peripheral unit clock control).

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0458h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R0W1	R0W1	R0W1	R	R	R0W1	R0W1	R	R	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	RW	RW	R	R	RW	RW	R	R	RW	RW

Table 48.5-52 CPG_CLK_ON23 Register Contents

Bit Position	Bit Name	Description
31 to 27	—	Reserved. These bits are read as 0b.
26 to 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23, 22	—	Reserved. These bits are read as 0b.
21, 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19, 18	—	Reserved. These bits are read as 0b.
17	—	Reserved. This bit is read as 0b. The write value should always be 0b.
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 11	—	Reserved. These bits are read as 0b.
10 to 8	—	Reserved. When read, the value read is undefined.
7, 6	—	Reserved. These bits are read as 0b.
5, 4	—	Reserved. When read, the value read is undefined.
3, 2	—	Reserved. These bits are read as 0b.
1	—	Reserved. When read, the value read is undefined.
0	CLK0_ON	RAMB_ACLK[3:0] switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.57 Clock ON/OFF Control Register 24 (CPG_CLK_ON24)

This register turns each unit clock on or off (Video0 system PD ISP, GPA, and STG clock control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 045Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CLK5_ONWEN	CLK4_ONWEN	CLK3_ONWEN	CLK2_ONWEN	CLK1_ONWEN	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	CLK5_ON	CLK4_ON	CLK3_ON	CLK2_ON	CLK1_ON	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 48.5-53 CPG_CLK_ON24 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b.
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	CLK3_ONWEN	Enables write for CLK3_ON (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b.
5	CLK5_ON	STG_CLK0 switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	STG_CLKAXI switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3	CLK3_ON	FAFA_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

Table 48.5-53 CPG_CLK_ON24 Register Contents (2/2)

Bit Position	Bit Name	Description
2	CLK2_ON	CIMB_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
1	CLK1_ON	CIMA_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	CLK0_ON	CIMA_CLKAPB switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.58 Clock ON/OFF Control Register 25 (CPG_CLK_ON25)

This register turns each unit clock on or off (Video1 system PD ISP, GPA, and MTD clock control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0460h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CLK5_ONWEN	CLK4_ONWEN	CLK3_ONWEN	—	CLK1_ONWEN	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	CLK5_ON	CLK4_ON	CLK3_ON	—	CLK1_ON	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	R	RW	RW

Table 48.5-54 CPG_CLK_ON25 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b.
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	CLK3_ONWEN	Enables write for CLK3_ON (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	—	Reserved. This bit is read as 0b.
17	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b.
5	CLK5_ON	FCD_CLKAXI switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
4	CLK4_ON	FCD_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3	CLK3_ON	FAFB_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
2	—	Reserved. This bit is read as 0b.

Table 48.5-54 CPG_CLK_ON25 Register Contents (2/2)

Bit Position	Bit Name	Description
1	CLK1_ON	BIMA_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	CLK0_ON	BIMA_CLKAPB switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.59 Clock ON/OFF Control Register 26 (CPG_CLK_ON26)

This register turns each unit clock on or off (Video1 system PD ISP, VCD, and JPG clock control)

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0464h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	CLK9_ONWEN	CLK8_ONWEN	—	—	CLK5_ONWEN	CLK4_ONWEN	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CLK9_ON	CLK8_ON	—	—	CLK5_ON	CLK4_ON	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	R

Table 48.5-55 CPG_CLK_ON26 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b.
27, 26	—	Reserved. These bits are read as 0b. The write value should always be 0b.
25	CLK9_ONWEN	Enables write for CLK9_ON (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	CLK8_ONWEN	Enables write for CLK8_ON (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23, 22	—	Reserved. These bits are read as 0b.
21	CLK5_ONWEN	Enables write for CLK5_ON (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19 to 17	—	Reserved. These bits are read as 0b. The write value should always be 0b.
16 to 12	—	Reserved. These bits are read as 0b.
11, 10	—	Reserved. When read, the value read is undefined.
9	CLK9_ON	JPG0_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
8	CLK8_ON	JPG0_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
7, 6	—	Reserved. These bits are read as 0b.
5	CLK5_ON	VCD_ACLK, VCD_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

Table 48.5-55 CPG_CLK_ON26 Register Contents (2/2)

Bit Position	Bit Name	Description
4	CLK4_ON	RIM_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3 to 1	—	Reserved. When read, the value read is undefined.
0	—	Reserved. This bit is read as 0b.

NOTES

- VCD_ACLK, VCD_PCLK on/off switching is reflected after register setting (synchronization with 48 MHz) and 2 * VCD_PCLK + 4 * VCD_ACLK. Other clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.60 Clock ON/OFF Control Register 27 (CPG_CLK_ON27)

This register turns each unit clock on or off (LPDDR4 system PD MMC, DDI clock control).

This register should not be rewritten because changing the LPDDR4 operation frequency after startup is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0468h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	CLK4_ONWEN	—	CLK2_ONWEN	CLK1_ONWEN	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	CLK4_ON	—	CLK2_ON	CLK1_ON	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	R	RW	RW	RW

Table 48.5-56 CPG_CLK_ON27 Register Contents

Bit Position	Bit Name	Description
31 to 21	—	Reserved. These bits are read as 0b.
20	CLK4_ONWEN	Enables write for CLK4_ON (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b.
18	CLK2_ONWEN	Enables write for CLK2_ON (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	CLK1_ONWEN	Enables write for CLK1_ON (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	CLK0_ONWEN	Enables write for CLK0_ON (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 5	—	Reserved. These bits are read as 0b.
4	CLK4_ON	DDI_APBCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
3	—	Reserved. This bit is read as 0b.
2	CLK2_ON	MMC_PCLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
1	CLK1_ON	MMC_ACLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)
0	CLK0_ON	MMC_CORE_DDRC_CORE_CLK switches ON/OFF. 0b: Clock OFF (Clock stopped state) 1b: Clock ON (Clock supply state)

NOTES

- Clock on/off switching is reflected after register setting (synchronization with 48 MHz) and synchronization to each clock (3 cycles later).
- The clock gating on/off timing depends on the frequency of the clock for synchronization.

48.5.2.61 WDT Reset Range Select Register (CPG_WDT_RST)

This register sets the reset range on reset occurrence.

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as '0'.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0500h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WDTRST1_WEN*	WDTRST0_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WDTRST1	WDTRST0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 48.5-57 CPG_WDT_RST Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b.
18	—	Reserved. This bit is read as 0b. The write value should always be 0b.
17*	WDTRST1_WEN	Enables write for WDTRST1 (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	WDTRST0_WEN	Enables write for WDTRST0 (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b.
2	—	Reserved. When read, the value read is undefined.
1	WDTRST1	Select the setting of the generated reset to system reset 2 or WDT CA53 Warm reset (Core 1). *Note*: WDT CA53 Warm reset (Core 1) prohibited. 0b: System reset 1b: WDT CA53 Warm reset (Core 1)
0	WDTRST0	Select the setting of the generated reset to system reset 2 or WDT CA53 Warm reset (Core 0). *Note*: WDT CA53 Warm reset (Core 0) prohibited. 0b: System reset 1b: WDT CA53 Warm reset (Core 0)

NOTE

A warm reset should follow the procedure (e.g. termination the bus transaction). A reset which is generated due to a WDT timeout occurs at an unexpected timing (e.g. software runaway). For this reason, if a WDT timeout reset occurs without software interaction, the setting for a warm reset is prohibited because warm booting may not be possible.

48.5.2.62 Reset Mask Register (CPG_RST_MSK)

This register masks the CA53 warm reset.

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0504h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	DBG1MSK_WEN	DBG0MSK_WEN	WARM1MSK_WEN	WARM0MSK_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	DBG1MSK	DBG0MSK	WARM1MSK	WARM0MSK
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 48.5-58 CPG_RST_MSK Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b.
19	DBG1MSK_WEN	Enables write for DBG1MSK (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	DBG0MSK_WEN	Enables write for DBG0MSK (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	WARM1MSK_WEN	Enables write for WARM1MSK (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	WARM0MSK_WEN	Enables write for WARM0MSK (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b.
3	DBG1MSK	Sets masking of CA53 core 1 warm reset caused with CA53_DBGRSTREQ[1]. 0b: Set mask 1b: Not set mask
2	DBG0MSK	Sets masking of CA53 core 0 warm reset caused with CA53_DBGRSTREQ[0]. 0b: Set mask 1b: Not set mask
1	WARM1MSK	Sets masking of CA53 core 1 warm reset caused with CA53_WARMRSTREQ[1]. 0b: Set mask 1b: Not set mask
0	WARM0MSK	Sets masking of CA53 core 0 warm reset caused with CA53_WARMRSTREQ[0]. 0b: Set mask 1b: Not set mask

48.5.2.63 Reset Control Register 1 (CPG_RST1)

This register controls each unit reset (AWO system reset control).

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as ‘0’.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0600h

Initial Value: 0000_FFFEh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	UNIT14_RST WEN*	UNIT13_RST WEN*	UNIT12_RST WEN*	—	UNIT10_RST WEN*	UNIT9_RST WEN*	UNIT8_RST WEN*	UNIT7_RST WEN*	UNIT6_RST WEN*	UNIT5_RST WEN	—	—	UNIT2_RST WEN*	UNIT1_RST WEN*	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	UNIT14_RSTB	UNIT13_RSTB	UNIT12_RSTB	—	UNIT10_RSTB	UNIT9_RSTB	UNIT8_RSTB	UNIT7_RSTB	UNIT6_RSTB	UNIT5_RSTB	—	—	UNIT2_RSTB	UNIT1_RSTB	—
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R

Table 48.5-59 CPG_RST1 Register Contents (1/2)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b. The write value should always be 0b.
30*	UNIT14_RST WEN	Enables write for UNIT14_RST (bit 14). Write only. Read as 0b. 0b: Write disable 1b: Write enable
29*	UNIT13_RST WEN	Enables write for UNIT13_RST (bit 13). Write only. Read as 0b. 0b: Write disable 1b: Write enable
28*	UNIT12_RST WEN	Enables write for UNIT12_RST (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b. The write value should always be 0b.
26*	UNIT10_RST WEN	Enables write for UNIT10_RST (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25*	UNIT9_RST WEN	Enables write for UNIT9_RST (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24*	UNIT8_RST WEN	Enables write for UNIT8_RST (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23*	UNIT7_RST WEN	Enables write for UNIT7_RST (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22*	UNIT6_RST WEN	Enables write for UNIT6_RST (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	UNIT5_RST WEN	Enables write for UNIT5_RST (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-59 CPG_RST1 Register Contents (2/2)

Bit Position	Bit Name	Description
20, 19	—	Reserved. These bits are read as 0b. The write value should always be 0b.
18*	UNIT2_RST WEN	Enables write for UNIT2_RST (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17*	UNIT1_RST WEN	Enables write for UNIT1_RST (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	—	Reserved. This bit is read as 0b.
15	—	Reserved. When read, the value read is undefined.
14	UNIT14_RSTB	Control the reset terminal PMC_RESET_N (TYPE-B). *Note*: If set to ON, operation is not supported. '0b' is prohibited. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
13	UNIT13_RSTB	Control the reset terminal TSU1_RESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
12	UNIT12_RSTB	Control the reset terminal TSU0_RESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
11	—	Reserved. When read, the value read is undefined.
10	UNIT10_RSTB	Control the reset terminal SEC_RSTB (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
9	UNIT9_RSTB	Control the reset terminals SEC_PRESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
8	UNIT8_RSTB	Control the reset terminal SEC_ARESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
7	UNIT7_RSTB	Control the reset terminal DMAA_ARESETN (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
6	UNIT6_RSTB	Control the reset terminal ROM_ARESETN (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
5	UNIT5_RSTB	Control the reset terminal RAMA_ARESETN (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
4, 3	—	Reserved. When read, the value read is undefined.
2	UNIT2_RSTB	Control the reset terminal PFC_PRESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
1	UNIT1_RSTB	Control the reset terminal SYS_RST_N (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
0	—	Reserved. These bits are read as 0b.

48.5.2.64 Reset Control Register 2 (CPG_RST2)

This register controls each unit reset (AWO CoreSight reset control).

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0604h

Initial Value: 0000_07FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	UNIT10_RST WEN	—	UNIT8_RST WEN	UNIT7_RST WEN	UNIT6_RST WEN	UNIT5_RST WEN	UNIT4_RST WEN	UNIT3_RST WEN	UNIT2_RST WEN	UNIT1_RST WEN	UNIT0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	UNIT10_RSTB	—	UNIT8_RSTB	UNIT7_RSTB	UNIT6_RSTB	UNIT5_RSTB	UNIT4_RSTB	UNIT3_RSTB	UNIT2_RSTB	UNIT1_RSTB	UNIT0_RSTB
Initial Value	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 48.5-60 CPG_RST2 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 27	—	Reserved. These bits are read as 0b.
26	UNIT10_RST WEN	Enables write for UNIT10_RST (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25	—	Reserved. This bit is read as 0b. The write value should always be 0b.
24	UNIT8_RST WEN	Enables write for UNIT8_RST (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	UNIT7_RST WEN	Enables write for UNIT7_RST (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	UNIT6_RST WEN	Enables write for UNIT6_RST (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	UNIT5_RST WEN	Enables write for UNIT5_RST (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	UNIT4_RST WEN	Enables write for UNIT4_RST (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	UNIT3_RST WEN	Enables write for UNIT3_RST (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	UNIT2_RST WEN	Enables write for UNIT2_RST (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	UNIT1_RST WEN	Enables write for UNIT1_RST (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-60 CPG_RST2 Register Contents (2/2)

Bit Position	Bit Name	Description
16	UNIT0_RST WEN	Enables write for UNIT0_RST (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 11	—	Reserved. These bits are read as 0b.
10	UNIT10_RSTB	Control the reset terminal CST_ATB_SB_RESETN. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
9	—	Reserved. When read, the value read is undefined.
8	UNIT8_RSTB	Control the reset terminal CST_APB_CA53_RESETN. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
7	UNIT7_RSTB	Control the reset terminal CST_TS_SB_RESETN. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
6	UNIT6_RSTB	Control the reset terminal CST_AHB_RESETN. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
5	UNIT5_RSTB	Control the reset terminal CST_SB_RESETN. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
4	UNIT4_RSTB	Control the reset terminal CST_TRESETN. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
3	UNIT3_RSTB	Control the reset terminal CST_TS_RESETN. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
2	UNIT2_RSTB	Control the reset terminal CST_CS_RESETN. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
1	UNIT1_RSTB	Control the reset terminals CST_NPOTRST, CST_NTRST. *Note*: If set to ON, the debugger cannot access TAP, so use is prohibited. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
0	UNIT0_RSTB	Control the reset terminal CST_NTRST. *Note*: If set to ON, the debugger cannot access TAP, so use is prohibited. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

48.5.2.65 Reset Control Register 3 (CPG_RST3)

This register controls each unit reset (AWO storage system PCIe, USB, and ETHER reset control).

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0608h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	UNIT12_RST WEN	UNIT11_RST WEN	UNIT10_RST WEN	UNIT9_RST WEN	UNIT8_RST WEN	UNIT7_RST WEN	—	UNIT5_RST WEN	UNIT4_RST WEN	—	UNIT2_RST WEN	UNIT1_RST WEN	UNIT0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	UNIT12_RSTB	UNIT11_RSTB	UNIT10_RSTB	UNIT9_RSTB	UNIT8_RSTB	UNIT7_RSTB	—	UNIT5_RSTB	UNIT4_RSTB	—	UNIT2_RSTB	UNIT1_RSTB	UNIT1_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	RW	RW	RW	RW	RW	RW	R	RW	RW	R	RW	RW	RW

Table 48.5-61 CPG_RST3 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 29	—	Reserved. These bits are read as 0b.
28	UNIT12_RST WEN	Enables write for UNIT12_RST (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	UNIT11_RST WEN	Enables write for UNIT11_RST (bit 11). Write only. Read as 0b. 0b: Write disable 1b: Write enable
26	UNIT10_RST WEN	Enables write for UNIT10_RST (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25	UNIT9_RST WEN	Enables write for UNIT9_RST (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24	UNIT8_RST WEN	Enables write for UNIT8_RST (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	UNIT7_RST WEN	Enables write for UNIT7_RST (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	—	Reserved. This bit is read as 0b.
21	UNIT5_RST WEN	Enables write for UNIT5_RST (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	UNIT4_RST WEN	Enables write for UNIT4_RST (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b.
18	UNIT2_RST WEN	Enables write for UNIT2_RST (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-61 CPG_RST3 Register Contents (2/2)

Bit Position	Bit Name	Description
17	UNIT1_RST WEN	Enables write for UNIT1_RST (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	UNIT0_RST WEN	Enables write for UNIT0_RST (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 13	—	Reserved. These bits are read as 0b.
12	UNIT12_RSTB	Control the reset terminal PCI_ARESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
11	UNIT11_RSTB	Control the reset terminal ETH0_RST_HW_N (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
10	UNIT10_RSTB	Control the reset terminal USB_ARESETN_H (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
9	UNIT9_RSTB	Control the reset terminals USB_ARESETN_P (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
8	UNIT8_RSTB	Control the reset terminal USB_DRD_RESET (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
7	UNIT7_RSTB	Control the reset terminal USB_PRESET_N (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
6	—	Reserved. This bit is read as 0b.
5	UNIT5_RSTB	Control the reset terminal NFI_REG_RST_N (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
4	UNIT4_RSTB	Control the reset terminals NFI_MARESETN (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
3	—	Reserved. This bit is read as 0b.
2	UNIT2_RSTB	Control the reset terminal EMM_IXRST (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
1	UNIT1_RSTB	Control the reset terminal SDI1_IXRST (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
0	UNIT0_RSTB	Control the reset terminal SDI0_IXRST (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

48.5.2.66 Reset Control Register 4 (CPG_RST4)

This register controls each unit reset (AWO ESI, GRP, DCU, CIF, HDMI, and LCI reset control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 060Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	UNIT7_RST WEN	UNIT6_RST WEN	UNIT5_RST WEN	UNIT4_RST WEN	UNIT3_RST WEN	UNIT2_RST WEN	UNIT1_RST WEN	UNIT0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	UNIT7_RSTB	UNIT6_RSTB	UNIT5_RSTB	UNIT4_RSTB	UNIT3_RSTB	UNIT2_RSTB	UNIT1_RSTB	UNIT0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW

Table 48.5-62 CPG_RST4 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 24	—	Reserved. These bits are read as 0b.
23	UNIT7_RST WEN	Enables write for UNIT7_RST (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	UNIT6_RST WEN	Enables write for UNIT6_RST (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	UNIT5_RST WEN	Enables write for UNIT5_RST (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	UNIT4_RST WEN	Enables write for UNIT4_RST (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	UNIT3_RST WEN	Enables write for UNIT3_RST (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	UNIT2_RST WEN	Enables write for UNIT2_RST (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	UNIT1_RST WEN	Enables write for UNIT1_RST (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	UNIT0_RST WEN	Enables write for UNIT0_RST (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 8	—	Reserved. These bits are read as 0b.
7	UNIT7_RSTB	Control the reset terminal LCI_ARESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

Table 48.5-62 CPG_RST4 Register Contents (2/2)

Bit Position	Bit Name	Description
6	UNIT6_RSTB	Control the reset terminal LCI_PRESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
5	UNIT5_RSTB	Control the reset terminal HMI_PRESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
4	UNIT4_RSTB	Control the reset terminal HMI_RST_N (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
3	UNIT3_RSTB	Control the reset terminal DCU_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
2	UNIT2_RSTB	Control the reset terminal CIF_RST_N (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
1	UNIT1_RSTB	Control the reset terminals GRP_RESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
0	UNIT0_RSTB	Control the reset terminal SDT_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

48.5.2.67 Reset Control Register 5 (CPG_RST5)

This register controls each unit reset (AWO AUI, MTR, ISP, ADC, and SYC reset control)

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as '0'.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0610h

Initial Value: 0000_0400h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	UNIT9_RST WEN	—	—	—	UNIT5_RST WEN*	UNIT4_RST WEN*	—	UNIT2_RST WEN*	UNIT1_RST WEN*	UNIT0_RST WEN*
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	UNIT9_RSTB	—	—	—	UNIT5_RSTB	UNIT4_RSTB	—	UNIT2_RSTB	UNIT1_RSTB	UNIT0_RSTB
Initial Value	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	R	RW	RW	RW

Table 48.5-63 CPG_RST5 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 27	—	Reserved. These bits are read as 0b.
26	—	Reserved. This bit is read as 0b. The write value should always be 0b.
25	UNIT9_RST WEN	Enables write for UNIT9_RST (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24 to 22	—	Reserved. These bits are read as 0b. The write value should always be 0b.
21*	UNIT5_RST WEN	Enables write for UNIT5_RST (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20*	UNIT4_RST WEN	Enables write for UNIT4_RST (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	—	Reserved. This bit is read as 0b.
18*	UNIT2_RST WEN	Enables write for UNIT2_RST (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17*	UNIT1_RST WEN	Enables write for UNIT1_RST (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16*	UNIT0_RST WEN	Enables write for UNIT0_RST (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 11	—	Reserved. These bits are read as 0b.
10	—	Reserved. When read, the value read is undefined.
9	UNIT9_RSTB	Control the reset terminal SYC_RST_N (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
8 to 6	—	Reserved. When read, the value read is undefined.

Table 48.5-63 CPG_RST5 Register Contents (2/2)

Bit Position	Bit Name	Description
5	UNIT5_RSTB	Control the reset terminal ATGB_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
4	UNIT4_RSTB	Control the reset terminal ATGA_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
3	—	Reserved. This bit is read as 0b.
2	UNIT2_RSTB	Control the reset terminal GFT_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
1	UNIT1_RSTB	Control the reset terminal MTR_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
0	UNIT0_RSTB	Control the reset terminal AUI_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

48.5.2.68 Reset Control Register 6 (CPG_RST6)

This register controls each unit reset (AWO Peripheral reset control).

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as ‘0’.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0614h

Initial Value: 0000_3000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	UNIT13_RST WEN	UNIT12_RST WEN	—	UNIT10_RST WEN*	UNIT9_RST WEN*	UNIT8_RST WEN*	UNIT7_RST WEN	UNIT6_RST WEN*	UNIT5_RST WEN*	UNIT4_RST WEN*	UNIT3_RST WEN*	UNIT2_RST WEN	UNIT1_RST WEN	UNIT0_RST WEN*
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R0W1	R0W1	R0W1	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	UNIT13_RSTB	UNIT12_RSTB	—	UNIT10_RSTB	UNIT9_RSTB	UNIT8_RSTB	UNIT7_RSTB	UNIT6_RSTB	UNIT5_RSTB	UNIT4_RSTB	UNIT3_RSTB	UNIT2_RSTB	UNIT1_RSTB	UNIT0_RSTB
Initial Value	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 48.5-64 CPG_RST6 Register Contents (1/3)

Bit Position	Bit Name	Description
31	—	Reserved. This bit is read as 0b.
30	—	Reserved. This bit is read as 0b. The write value should always be 0b.
29	UNIT13_RST WEN	Enables write for UNIT13_RST (bit 13). Write only. Read as 0b. 0b: Write disable 1b: Write enable
28	UNIT12_RST WEN	Enables write for UNIT12_RST (bit 12). Write only. Read as 0b. 0b: Write disable 1b: Write enable
27	—	Reserved. This bit is read as 0b.
26*	UNIT10_RST WEN	Enables write for UNIT10_RST (bit 10). Write only. Read as 0b. 0b: Write disable 1b: Write enable
25*	UNIT9_RST WEN	Enables write for UNIT9_RST (bit 9). Write only. Read as 0b. 0b: Write disable 1b: Write enable
24*	UNIT8_RST WEN	Enables write for UNIT8_RST (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	UNIT7_RST WEN	Enables write for UNIT7_RST (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22*	UNIT6_RST WEN	Enables write for UNIT6_RST (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21*	UNIT5_RST WEN	Enables write for UNIT5_RST (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable

Table 48.5-64 CPG_RST6 Register Contents (2/3)

Bit Position	Bit Name	Description
20*	UNIT4_RST WEN	Enables write for UNIT4_RST (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19*	UNIT3_RST WEN	Enables write for UNIT3_RST (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	UNIT2_RST WEN	Enables write for UNIT2_RST (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	UNIT1_RST WEN	Enables write for UNIT1_RST (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16*	UNIT0_RST WEN	Enables write for UNIT0_RST (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15	—	Reserved. This bit is read as 0b.
14	—	Reserved. When read, the value read is undefined.
13	UNIT13_RSTB	Control the reset terminal WDT_PRESETN[1] (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
12	UNIT12_RSTB	Control the reset terminal WDT_PRESETN[0] (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
11	—	Reserved. This bit is read as 0b.
10	UNIT10_RSTB	Control the reset terminal URT_PRESETN (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
9	UNIT9_RSTB	Control the reset terminal IIC_GPB_PRESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
8	UNIT8_RSTB	Control the reset terminal IIC_GPA_PRESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
7	UNIT7_RSTB	Control the reset terminal CSI_GPH_PRESETN (TYPE-B) 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
6	UNIT6_RSTB	Control the reset terminal CSI_GPG_PRESETN (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
5	UNIT5_RSTB	Control the reset terminal PWM_GPF_PRESETN (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
4	UNIT4_RSTB	Control the reset terminal PWM_GPE_PRESETN (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
3	UNIT3_RSTB	Control the reset terminal TIM_GPD_PRESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
2	UNIT2_RSTB	Control the reset terminal TIM_GPC_PRESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

Table 48.5-64 CPG_RST6 Register Contents (3/3)

Bit Position	Bit Name	Description
1	UNIT1_RSTB	Control the reset terminals TIM_GPB_PRESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
0	UNIT0_RSTB	Control the reset terminal TIM_GPA_PRESETN (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

48.5.2.69 Reset Control Register 7 (CPG_RST7)

This register controls each unit reset (ICB reset control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0618h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	UNIT4_RST WEN	UNIT3_RST WEN	UNIT2_RST WEN	UNIT1_RST WEN	UNIT0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	UNIT4_RSTB	UNIT3_RSTB	UNIT2_RSTB	UNIT1_RSTB	UNIT0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW

Table 48.5-65 CPG_RST7 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 21	—	Reserved. These bits are read as 0b.
20	UNIT4_RST WEN	Enables write for UNIT4_RST (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	UNIT3_RST WEN	Enables write for UNIT3_RST (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	UNIT2_RST WEN	Enables write for UNIT2_RST (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	UNIT1_RST WEN	Enables write for UNIT1_RST (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	UNIT0_RST WEN	Enables write for UNIT0_RST (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 5	—	Reserved. These bits are read as 0b.
4	UNIT4_RSTB	Control the reset terminal ICB_PD_RFX_RST_N (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
3	UNIT3_RSTB	Control the reset terminal ICB_PD_VD1_RST_N (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
2	UNIT2_RSTB	Control the reset terminal ICB_PD_VD0_RST_N (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
1	UNIT1_RSTB	Control the reset terminals ICB_PD_MMC_RST_N (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

Table 48.5-65 CPG_RST7 Register Contents (2/2)

Bit Position	Bit Name	Description
0	UNIT0_RSTB	Control the reset terminal ICB_PD_AWO_RST_N. *Note*: Setting to ON is prohibited due to deadlock. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

48.5.2.70 Reset Control Register 8 (CPG_RST8)

This register controls each unit reset (CA53 system PD CA53 reset control).

Access Size: 32 bits

Address(es): <CPG_S0_base> + 061Ch

Initial Value: 0000_01FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	UNIT8_RST WEN	UNIT7_RST WEN	UNIT6_RST WEN	UNIT5_RST WEN	UNIT4_RST WEN	UNIT3_RST WEN	UNIT2_RST WEN	UNIT1_RST WEN	UNIT0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	UNIT8_RSTB	UNIT7_RSTB	UNIT6_RSTB	UNIT5_RSTB	UNIT4_RSTB	UNIT3_RSTB	UNIT2_RSTB	UNIT1_RSTB	UNIT0_RSTB
Initial Value	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 48.5-66 CPG_RST8 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24	UNIT8_RST WEN	Enables write for UNIT8_RST (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	UNIT7_RST WEN	Enables write for UNIT7_RST (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	UNIT6_RST WEN	Enables write for UNIT6_RST (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	UNIT5_RST WEN	Enables write for UNIT5_RST (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	UNIT4_RST WEN	Enables write for UNIT4_RST (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	UNIT3_RST WEN	Enables write for UNIT3_RST (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	UNIT2_RST WEN	Enables write for UNIT2_RST (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	UNIT1_RST WEN	Enables write for UNIT1_RST (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	UNIT0_RST WEN	Enables write for UNIT0_RST (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 9	—	Reserved. These bits are read as 0b.

Table 48.5-66 CPG_RST8 Register Contents (2/2)

Bit Position	Bit Name	Description
8	UNIT8_RSTB	Control the reset terminal CA53_NARESET. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
7	UNIT7_RSTB	Control the reset terminal CA53_NMISCRESET_SM. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
6	UNIT6_RSTB	Control the reset terminal CA53_NMISCRESET_HM. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
5	UNIT5_RSTB	Control the reset terminal CA53_L2RESET. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
4	UNIT4_RSTB	Control the reset terminal CA53_NPRESETDBG. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
3	UNIT3_RSTB	Control the reset terminal CA53_NCORERESET[1]. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
2	UNIT2_RSTB	Control the reset terminal CA53_NCORERESET[0]. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
1	UNIT1_RSTB	Control the reset terminals CA53_NCPUPORESET[1]. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
0	UNIT0_RSTB	Control the reset terminal CA53_NCPUPORESET[0]. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

48.5.2.71 Reset Control Register 9 (CPG_RST9)

This register controls each unit reset (DRP-AI system PD DRPA reset control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0620h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UNIT0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UNIT0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 48.5-67 CPG_RST9 Register Contents

Bit Position	Bit Name	Description
31 to 17	—	Reserved. These bits are read as 0b.
16	UNIT0_RST WEN	Enables write for UNIT0_RST (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 1	—	Reserved. These bits are read as 0b.
0	UNIT0_RSTB	Control the reset terminal DRPA_ARESETN (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

48.5.2.72 Reset Control Register 12 (CPG_RST12)

This register controls each unit reset (RAMB system PD RFX reset control).

Access Size: 32 bits

Address(es): <CPG_S0_base> + 062Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UNIT0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UNIT0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 48.5-68 CPG_RST12 Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b.
19 to 17	—	Reserved. These bits are read as 0b. The write value should always be 0b.
16	UNIT0_RST WEN	Enables write for UNIT0_RST (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b.
3 to 1	—	Reserved. When read, the value read is undefined.
0	UNIT0_RSTB	Control the reset terminals RAMB_ARESETN[3:0] (TYPE-B) 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

48.5.2.73 Reset Control Register 13 (CPG_RST13)

This register controls each unit reset (Video0 system PD Video0 reset control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0630h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	UNIT3_RST WEN	UNIT2_RST WEN	UNIT1_RST WEN	UNIT0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	UNIT3_RSTB	UNIT2_RSTB	UNIT1_RSTB	UNIT0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW

Table 48.5-69 CPG_RST13 Register Contents

Bit Position	Bit Name	Description
31 to 20	—	Reserved. These bits are read as 0b.
19	UNIT3_RST WEN	Enables write for UNIT3_RST (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	UNIT2_RST WEN	Enables write for UNIT2_RST (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	UNIT1_RST WEN	Enables write for UNIT1_RST (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	UNIT0_RST WEN	Enables write for UNIT0_RST (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 4	—	Reserved. These bits are read as 0b.
3	UNIT3_RSTB	Control the reset terminal STG_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
2	UNIT2_RSTB	Control the reset terminal FAFA_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
1	UNIT1_RSTB	Control the reset terminal CIMB_RSTSYSAX (TYPE-A) 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
0	UNIT0_RSTB	Control the reset terminals CIMA_RSTSYSAX (TYPE-A) 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

48.5.2.74 Reset Control Register 14 (CPG_RST14)

This register controls each unit reset (Video1 system PD Video1 reset control).

This register is for use with the ISP support package. Therefore, changing this register is prohibited.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0634h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	UNIT8_RST WEN	UNIT7_RST WEN	UNIT6_RST WEN	—	—	UNIT3_RST WEN	UNIT2_RST WEN	—	UNIT0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	UNIT8_RSTB	UNIT7_RSTB	UNIT6_RSTB	—	—	UNIT3_RSTB	UNIT2_RSTB	—	UNIT0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	R	RW

Table 48.5-70 CPG_RST14 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 26	—	Reserved. These bits are read as 0b.
25	—	Reserved. This bit is read as 0b. The write value should always be 0b.
24	UNIT8_RST WEN	Enables write for UNIT8_RST (bit 8). Write only. Read as 0b. 0b: Write disable 1b: Write enable
23	UNIT7_RST WEN	Enables write for UNIT7_RST (bit 7). Write only. Read as 0b. 0b: Write disable 1b: Write enable
22	UNIT6_RST WEN	Enables write for UNIT6_RST (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21, 20	—	Reserved. These bits are read as 0b. The write value should always be 0b.
19	UNIT3_RST WEN	Enables write for UNIT3_RST (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	UNIT2_RST WEN	Enables write for UNIT2_RST (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	—	Reserved. This bit is read as 0b.
16	UNIT0_RST WEN	Enables write for UNIT0_RST (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 10	—	Reserved. These bits are read as 0b.
9	—	Reserved. When read, the value read is undefined.
8	UNIT8_RSTB	Control the reset terminal JPG_XRESET (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

Table 48.5-70 CPG_RST14 Register Contents (2/2)

Bit Position	Bit Name	Description
7	UNIT7_RSTB	Control the reset terminal VCD_RESETN (TYPE-B). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
6	UNIT6_RSTB	Control the reset terminal RIM_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
5, 4	—	Reserved. When read, the value read is undefined.
3	UNIT3_RSTB	Control the reset terminal FCD_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
2	UNIT2_RSTB	Control the reset terminal FAFB_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
1	—	Reserved. This bit is read as 0b.
0	UNIT0_RSTB	Control the reset terminal BIMA_RSTSYSAX (TYPE-A). 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

48.5.2.75 Reset Control Register 15 (CPG_RST15)

This register controls each unit reset (DDR system PD MMC and DDI reset control).

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0638h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	UNIT6_RST WEN	UNIT5_RST WEN	UNIT4_RST WEN	UNIT3_RST WEN	UNIT2_RST WEN	—	UNIT0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	UNIT6_RSTB	UNIT5_RSTB	UNIT4_RSTB	UNIT3_RSTB	UNIT2_RSTB	—	UNIT0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	R	RW

Table 48.5-71 CPG_RST15 Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 23	—	Reserved. These bits are read as 0b.
22	UNIT6_RST WEN	Enables write for UNIT6_RST (bit 6). Write only. Read as 0b. 0b: Write disable 1b: Write enable
21	UNIT5_RST WEN	Enables write for UNIT5_RST (bit 5). Write only. Read as 0b. 0b: Write disable 1b: Write enable
20	UNIT4_RST WEN	Enables write for UNIT4_RST (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19	UNIT3_RST WEN	Enables write for UNIT3_RST (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18	UNIT2_RST WEN	Enables write for UNIT2_RST (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17	—	Reserved. This bit is read as 0b.
16	UNIT0_RST WEN	Enables write for UNIT0_RST (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 7	—	Reserved. These bits are read as 0b.
6	UNIT6_RSTB	Control the reset terminal DDI_RESETN_APB*1. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
5	UNIT5_RSTB	Control the reset terminal DDI_RESET*1. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
4	UNIT4_RSTB	Control the reset terminal DDI_PWROK*1. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

Table 48.5-71 CPG_RST15 Register Contents (2/2)

Bit Position	Bit Name	Description
3	UNIT3_RSTB	Control the reset terminal MMC_PRESETN*1. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
2	UNIT2_RSTB	Control the reset terminal MMC_ARESETN_N*1. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
1	—	Reserved. This bit is read as 0b.
0	UNIT0_RSTB	Control the reset terminal MMC_CORE_DDRC_RSTN*1. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

Note 1. MMC and DDI resets are deasserted with the software sequence of the other procedure. Refer to the PMC section for details.

48.5.2.76 Reset Monitor Register (CPG_RST_MON)

This register monitors each unit reset.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0680h

Initial Value: 37E7_EFC0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	JPG0_RST_MON	—	URT_RST_MON	CSI_RST_MON2	CSI_RST_MON1	PWM_RST_MON1	PWM_RST_MON0	—	WDT1_RST_MON	WDT0_RST_MON	VCD_RST_MON	RAMB_RST_MON	—
Initial Value	0	0	1	1	0	1	1	1	1	1	1	0	0	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	DRPA_RST_MON	SYC_RST_MON	—	ETH0_RST_MON	NFI_RST_MON2	NFI_RST_MON1	EMM_RST_MON	SDI1_RST_MON	SDI0_RST_MON	SEC_RST_MON	DMAA_RST_MON	ROM_RST_MON	RAMA_RST_MON	GIC_RST_MON	—
Initial Value	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 48.5-72 CPG_RST_MON Register Contents (1/2)

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29	—	Reserved. When read, the value read is undefined.
28	JPG0_RST_MON	Monitor the reset state of JPG. 0b: Reset release 1b: Reset state
27	—	Reserved. This bit is read as 0b.
26	URT_RST_MON	Monitor the reset state of UART0, 1. 0b: Reset release 1b: Reset state
25	CSI_RST_MON2	Monitor the reset state of CSI4, 5. 0b: Reset release 1b: Reset state
24	CSI_RST_MON1	Monitor the reset state of CSI0-3. 0b: Reset release 1b: Reset state
23	PWM_RST_MON1	Monitor the reset state of PWM8-15. 0b: Reset release 1b: Reset state
22	PWM_RST_MON0	Monitor the reset state of PWM0-7. 0b: Reset release 1b: Reset state
21	—	Reserved. When read, the value read is undefined.
20	WDT1_RST_MON	Monitor the reset state of WDT1. 0b: Reset release 1b: Reset state
19	WDT0_RST_MON	Monitor the reset state of WDT0. 0b: Reset release 1b: Reset state

Table 48.5-72 CPG_RST_MON Register Contents (2/2)

Bit Position	Bit Name	Description
18	VCD_RST_MON	Monitor the reset state of VCD. 0b: Reset release 1b: Reset state
17	RAMB_RST_MON	Monitor the reset state of RAMB. 0b: Reset release 1b: Reset state
16,15	—	Reserved. When read, the value read is undefined.
14	DRPA_RST_MON	Monitor the reset state of DRPA. 0b: Reset release 1b: Reset state
13	SYC_RST_MON	Monitor the reset state of SYC. 0b: Reset release 1b: Reset state
12	—	Reserved. This bit is read as 0b.
11	ETH0_RST_MON	Monitor the reset state of ETHER. 0b: Reset release 1b: Reset state
10	NFI_RST_MON2	Monitor the reset state of NFI_REG_RST_N. 0b: Reset release 1b: Reset state
9	NFI_RST_MON1	Monitor the reset state of NFI_MARESETN. 0b: Reset release 1b: Reset state
8	EMM_RST_MON	Monitor the reset state of eMMC. 0b: Reset release 1b: Reset state
7	SDI1_RST_MON	Monitor the reset state of SDI1. 0b: Reset release 1b: Reset state
6	SDI0_RST_MON	Monitor the reset state of SDI0. 0b: Reset release 1b: Reset state
5	SEC_RST_MON	Monitor the reset state of SEC (SEC_RSTB). 0b: Reset release 1b: Reset state
4	DMAA_RST_MON	Monitor the reset state of DMAC. 0b: Reset release 1b: Reset state
3	ROM_RST_MON	Monitor the reset state of ROM. 0b: Reset release 1b: Reset state
2	RAMA_RST_MON	Monitor the reset state of RAMA. 0b: Reset release 1b: Reset state
1	GIC_RST_MON	Monitor the reset state of GIC. 0b: Reset release 1b: Reset state
0	—	Reserved. When read, the value read is undefined.

48.5.2.77 CPG Power Domain Reset Control Register (CPG_PD_RST)

This register controls each power domain reset of the CPG module.

This register is for use with the ISP support package. Therefore, the bits marked with * should be written as ‘0’.

Access Size: 32 bits

Address(es): <CPG_S0_base> + 0800h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	PD_RFX_RSTB_WEN*	PD_VD1B_RSTB_WEN*	PD_VD1A_RSTB_WEN*	PD_VD0_RSTB_WEN*	PD_MEM_RSTB_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PD_RFX_RSTB	PD_VD1B_RSTB	PD_VD1A_RSTB	PD_VD0_RSTB	PD_MEM_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW

Table 48.5-73 CPG_PD_RST Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 21	—	Reserved. These bits are read as 0b.
20*	PD_RFX_RSTB_WEN	Enables write for PD_RFX_RSTB (bit 4). Write only. Read as 0b. 0b: Write disable 1b: Write enable
19*	PD_VD1B_RSTB_WEN	Enables write for PD_VD1B_RSTB (bit 3). Write only. Read as 0b. 0b: Write disable 1b: Write enable
18*	PD_VD1A_RSTB_WEN	Enables write for PD_VD1A_RSTB (bit 2). Write only. Read as 0b. 0b: Write disable 1b: Write enable
17*	PD_VD0_RSTB_WEN	Enables write for PD_VD0_RSTB (bit 1). Write only. Read as 0b. 0b: Write disable 1b: Write enable
16	PD_MEM_RSTB_WEN	Enables write for PD_MEM_RSTB (bit 0). Write only. Read as 0b. 0b: Write disable 1b: Write enable
15 to 5	—	Reserved. These bits are read as 0b.
4	PD_RFX_RSTB	Control the reset of the CPG module arranged in the PD_RFX power domain. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
3	PD_VD1B_RSTB	Control the reset of the CPG module arranged in the PD_VIDEO1B power domain. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
2	PD_VD1A_RSTB	Control the reset of the CPG module arranged in the PD_VIDEO1A power domain. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

Table 48.5-73 CPG_PD_RST Register Contents (2/2)

Bit Position	Bit Name	Description
1	PD_VD0_RSTB	Control the reset of CPG module arranged in the PD_VIDEO0 power domain. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)
0	PD_MEM_RSTB	Control the reset of CPG module arranged in the PD_MEM power domain. *Note*: PD_MEM layer is arranged in PD_AWO power domain. 0b: Reset ON (Reset state) 1b: Reset OFF (Reset release)

48.6 Functional Description

48.6.1 Clock Generation and Control Function

48.6.1.1 SSCG PLL Control, Setting, and Monitoring

The SSCG PLL is controlled by the internal registers of the CPG.

Also, the states of the PLLs can be monitored by the output signals and internal registers of the CPG.

The SSCG PLL is for use with the ISP support package, so changing the setting is prohibited.

48.6.1.2 FRAC PLL Control, Setting, and Monitoring

The FRAC PLL is controlled by the internal registers of the CPG.

Also, the states of the PLLs can be monitored by the output signals and internal registers of the CPG.

The FRAC (Fractional) PLL is for use with the ISP support package, so changing the setting is prohibited.

48.6.1.3 Clock Dividers and Selectors

The CPG uses several dividers and selectors to supply the clock signal according to the specification of a given unit.

A divider and selector can be divided into two types: a type which can be switched without stopping the clock signal for the unit (dynamic switching) and a type which requires switching after stopping the clock signal for the unit.

The types of divider and selector are as follows.

- Fixed divider
- Dynamic switching variable divider (decimation type)
- Dynamic switching variable divider (Duty50 type)
- Dynamic switching selector
- Static switching variable divider
- Static switching selector

For the connection specifications of the respective dividers, selectors, and PLLs, see **Section 48.3.1, Clock System Diagram**.

(1) Fixed Divider

A divider which provides a fixed division value. It is connected between the output of the PLL and the variable divider.

The division value is selectable from 1/2, 1/3, 1/4, 1/8, 1/16, and 1/24.

Figure 48.6-1 is an example of connection of the 1/2 fixed divider.

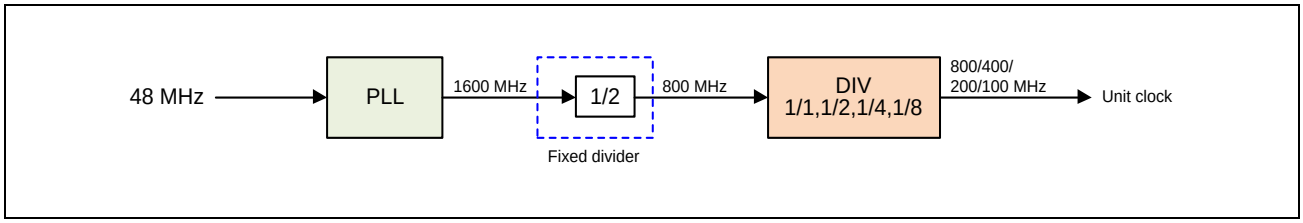


Figure 48.6-1 Example of Connection of the Fixed Divider

Figure 48.6-2 is a timing chart of various fixed dividers. The 1/2 fixed divider has two types, decimation type and Duty50 type.

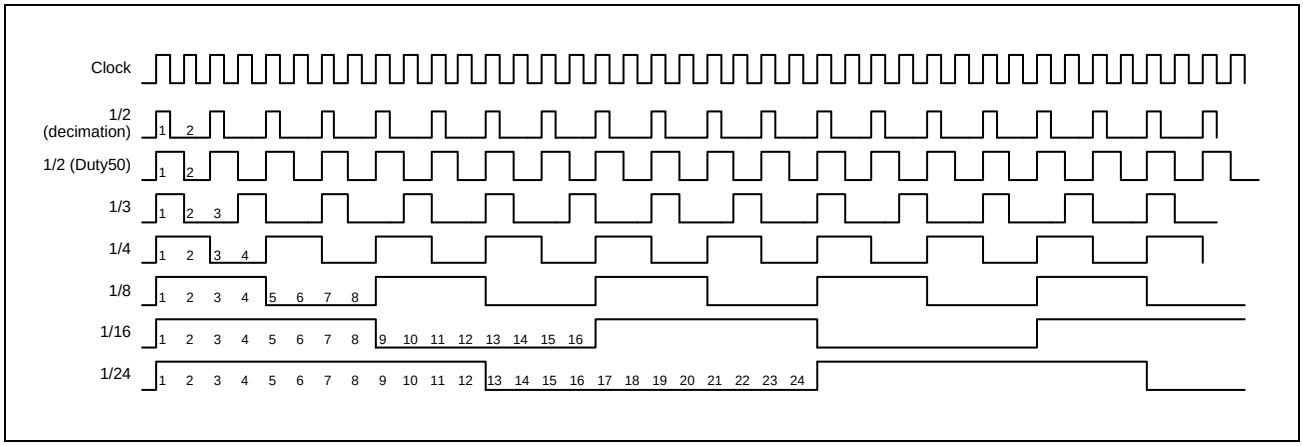


Figure 48.6-2 Timing Chart of the Fixed Dividers

(2) Dynamic Switching Variable Divider (Decimation Type)

A divider which allows switching of the clock signal without generating glitches when changing the division setting.

This divider can switch the clock signal without stopping the clock supply to a unit.

It generates a clock signal by decimating the source oscillation clock.

The division value is 1/1, 1/2, 1/3, 1/4, 1/6, 1/8, 1/12, 1/16, or 1/24 and the division value differs with a unit to be connected.

Clock switching requires a fixed time in order to prevent generation of glitches at the time of clock switching.

Whether switching is in progress can be monitored.

Figure 48.6-3 is a schematic view of the allocation of the divider and **Figure 48.6-4** and **Figure 48.6-5** show the timing charts.

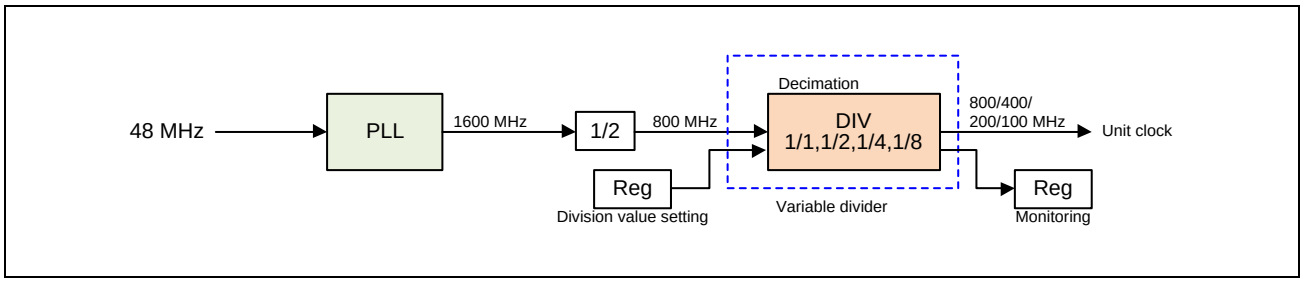


Figure 48.6-3 Schematic View of the Allocation of the Dynamic Switching Variable Divider (Decimation Type)

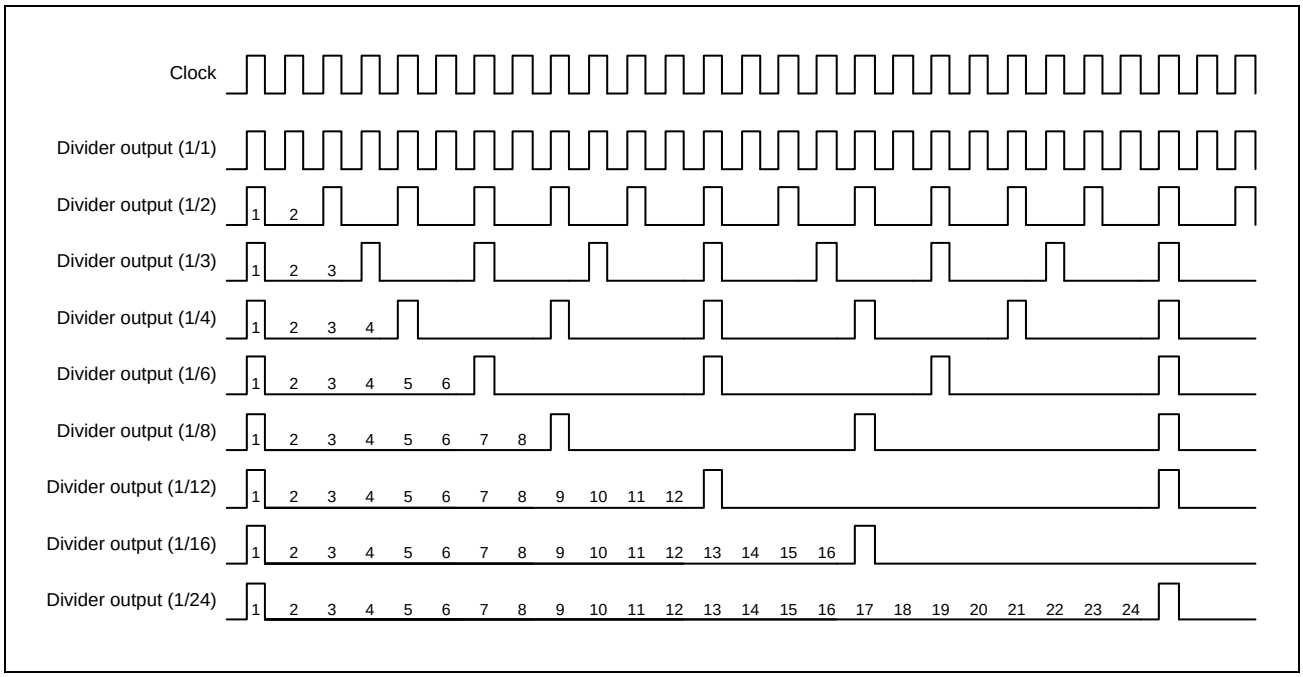
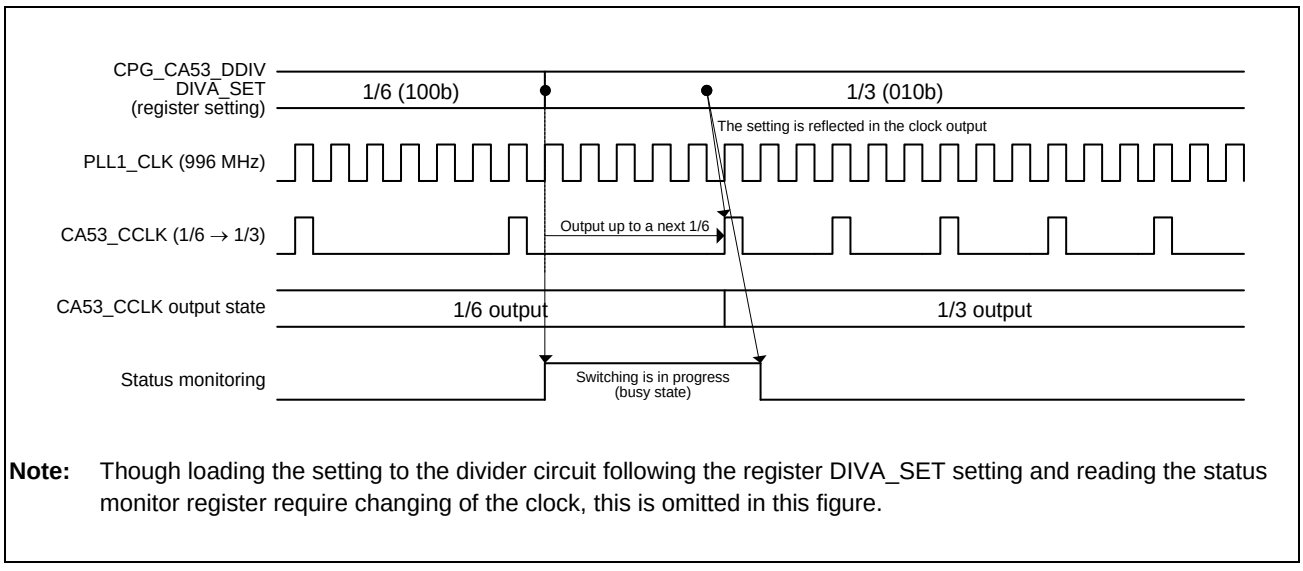


Figure 48.6-4 Timing Chart of the Dynamic Switching Variable Divider (Decimation Type)



Note: Though loading the setting to the divider circuit following the register DIVA_SET setting and reading the status monitor register require changing of the clock, this is omitted in this figure.

Figure 48.6-5 Timing Chart of Clock Switching of the Dynamic Switching Variable Divider (Decimation Type)

(3) Dynamic Switching Variable Divider (Duty50 Type)

A divider which allows switching of the clock signal without generating glitches when changing the division setting.

This divider can switch the clock signal without stopping the clock supply to a unit.

It generates a clock signal of duty 50%.

The division value is 1/1, 1/2, 1/4, 1/8, 1/16, or 1/32 and the division value differs with a unit to be connected.

Clock switching requires a fixed time in order to prevent generation of glitches at the time of clock switching.

Whether switching is in progress can be monitored.

Figure 48.6-6 is a schematic view of the allocation of the divider and **Figure 48.6-7** and **Figure 48.6-8** show the timing charts.

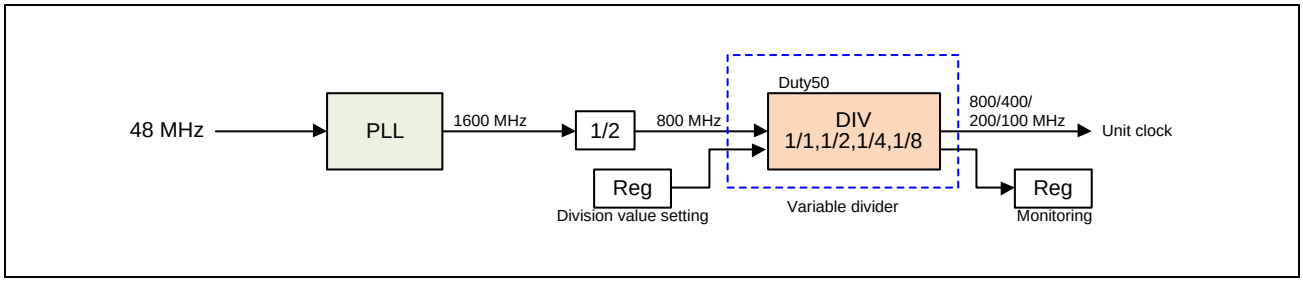


Figure 48.6-6 Schematic View of the Allocation of the Dynamic Switching Variable Divider (Duty50 Type)

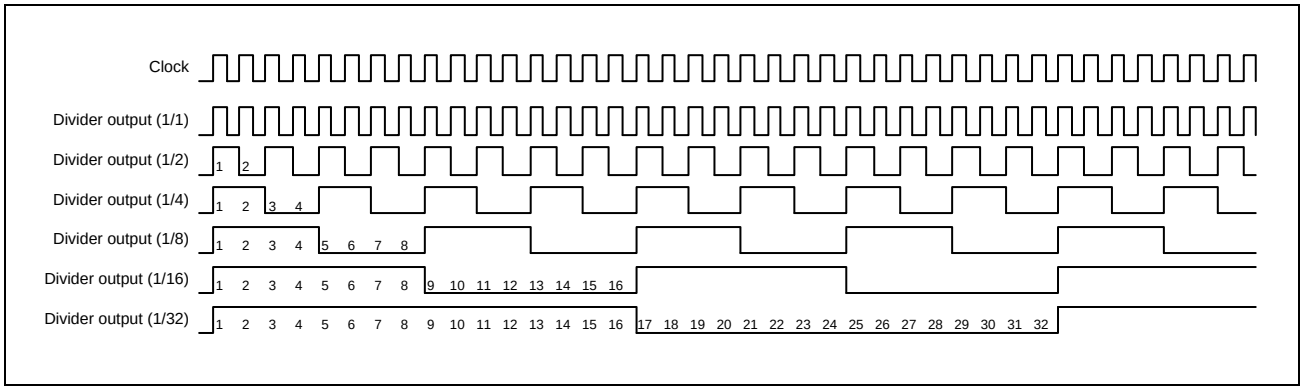
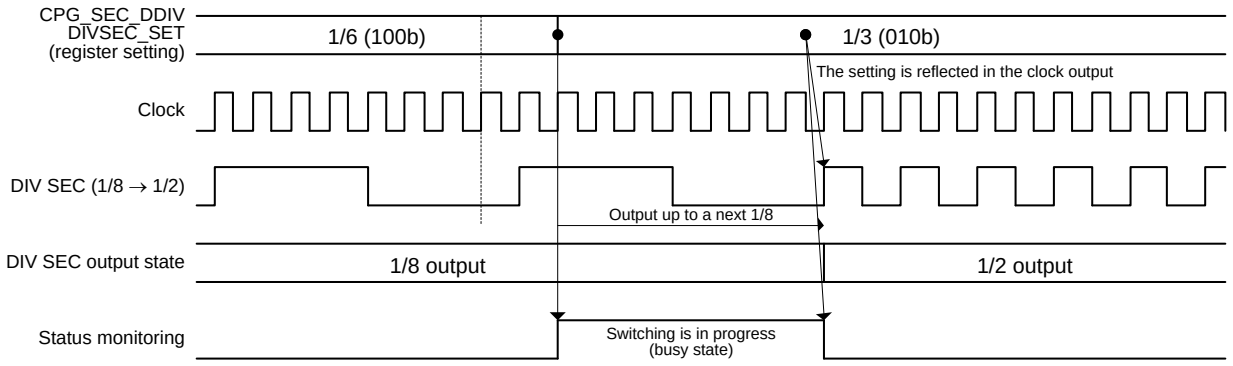


Figure 48.6-7 Timing Chart of the Dynamic Switching Variable Divider (Duty50 Type)



Note: Though loading the setting to the divider circuit following the register DIVA_SET setting and reading the status monitor register require changing of the clock, this is omitted in this figure.

Figure 48.6-8 Timing Chart of Clock Switching of the Dynamic Switching Variable Divider (Duty50 Type)

(4) Dynamic Switching Selector

A selector which allows changing the selection of the clock signal without generating glitches when changing the clock selection.

This selector can switch the clock signal without stopping the clock supply to a unit.

Clock switching requires a fixed time in order to prevent generation of glitches at the time of clock switching.

Whether switching is in progress can be monitored.

When switching the clock signal, make sure that the input clock signals of the selector are enabled.

Switching the clock signal while either of the input clock signals is stopped is prohibited.

Figure 48.6-9 is a schematic view of the allocation of the selector and **Figure 48.6-10** shows the timing chart.

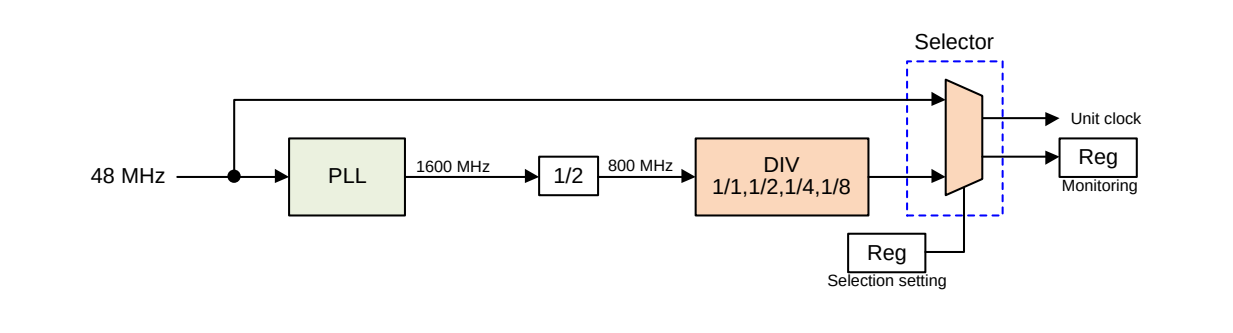
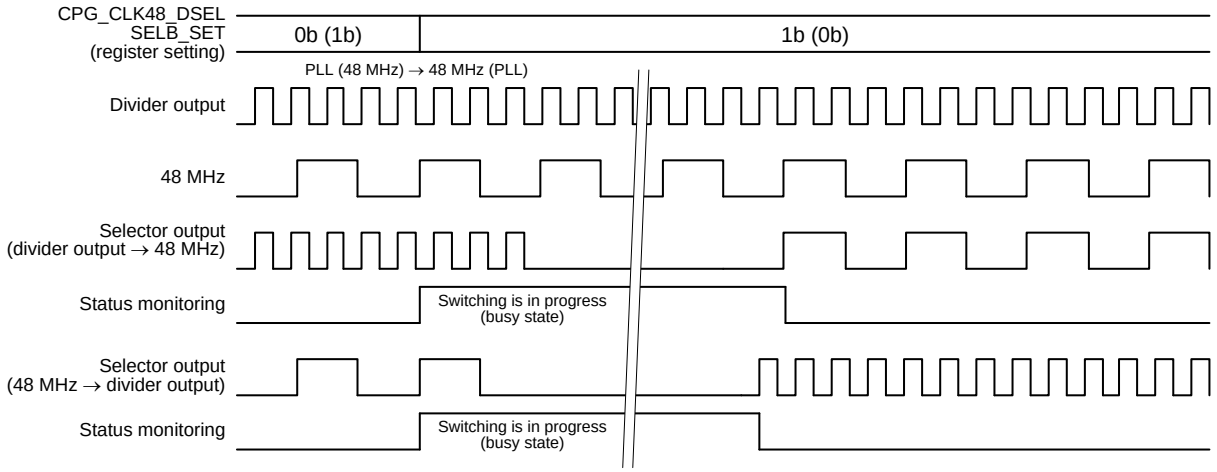


Figure 48.6-9 Schematic View of the Allocation of the Dynamic Switching Selector



Note: Though loading the setting to the divider circuit following the register SELB_SET setting and reading the status monitor register require changing of the clock, this is omitted in this figure.

Figure 48.6-10 Timing Chart of Clock Switching of the Dynamic Switching Selector

Table 48.6-1 lists the related register.

Regarding the setting for switching, see the subsequent sections.

Table 48.6-1 List of the Divider and Selector Switching Monitoring Register

Register Name	Abbreviation	Function
Clock status monitoring register	CPG_CLKSTATUS1,2	Monitoring clock switching of the divider and selector

(5) Static Switching Variable Divider (Decimation Type, Duty50 Type, OtherDuty50 Type)

A glitch is generated as the division setting is immediately reflected in the clock output.

Accordingly, changing the setting requires stopping the clock supply to a unit.

Monitoring is not used because the setting is immediately reflected in the output.

There are three types of divider available: clock decimation type, Duty50 type which outputs a clock signal of duty 50%, and OtherDuty50 type which outputs a clock signal whose width at high level is shorter than the width at low level for one pulse at the time of odd-number division.

Figure 48.6-11 is a schematic view of the allocation of the divider and **Figure 48.6-12** shows the timing chart.

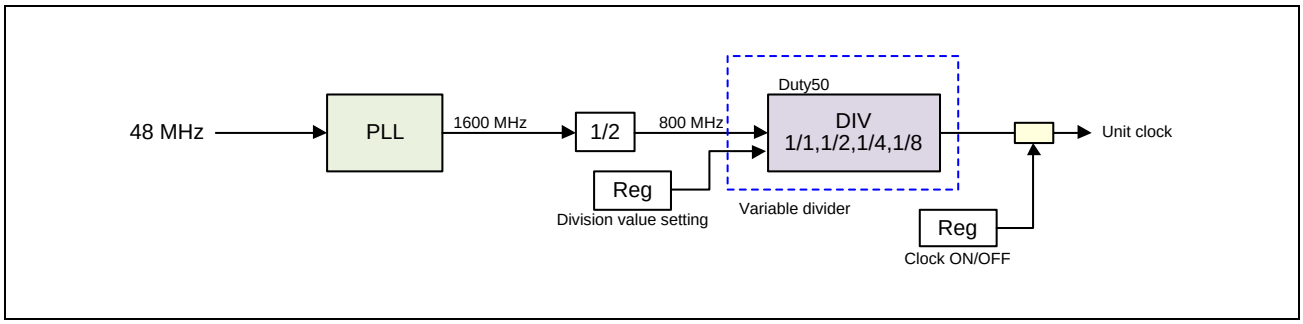


Figure 48.6-11 Schematic View of the Allocation of the Static Switching Variable Divider

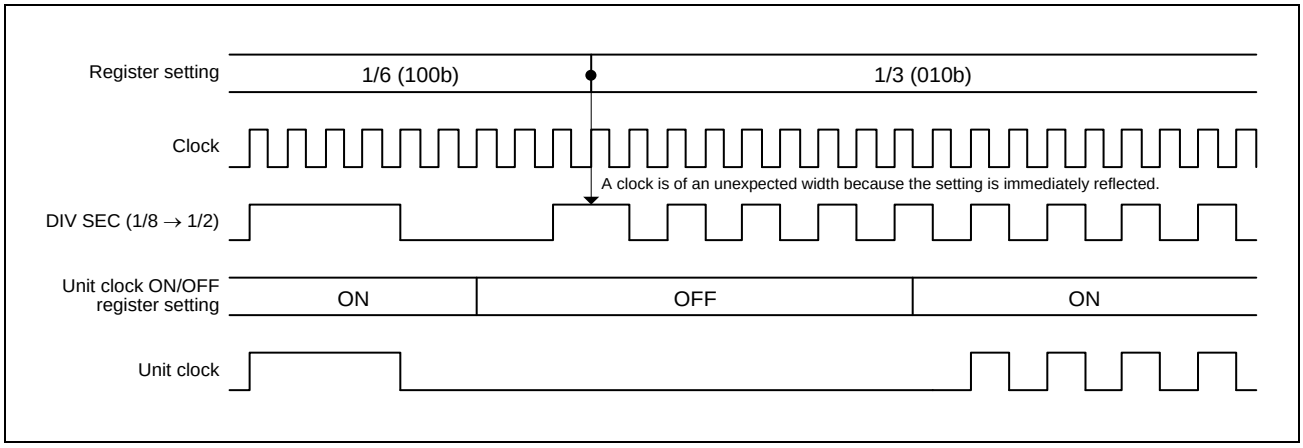


Figure 48.6-12 Timing Chart of Clock Switching of the Static Switching Variable Divider

(6) Static Switching Selector

A glitch is generated as the change to the clock selection setting is immediately reflected in the clock output.

Accordingly, changing the setting requires stopping the clock supply to a unit.

Monitoring is not used because the setting is immediately reflected in the output.

Figure 48.6-13 is a schematic view of the allocation of the selector and **Figure 48.6-14** shows the timing chart.

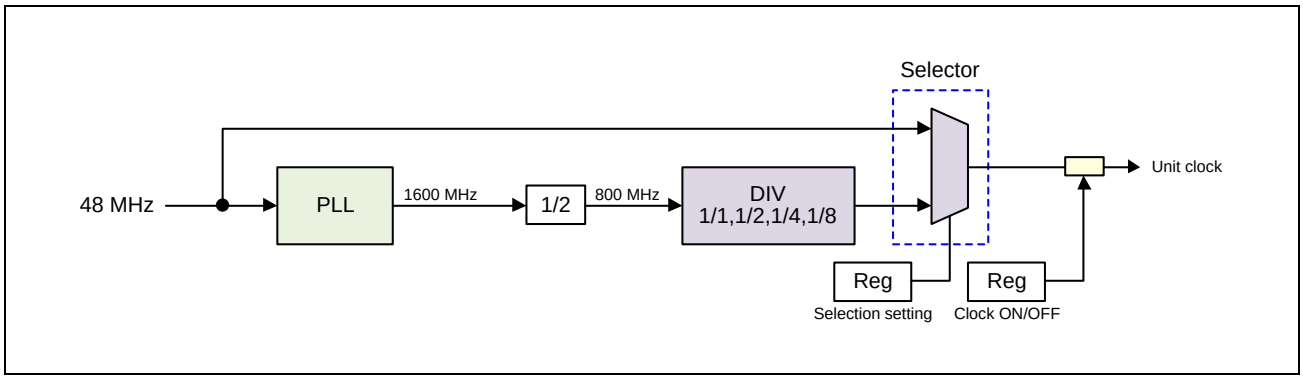


Figure 48.6-13 Schematic View of the Allocation of the Static Switching Selector

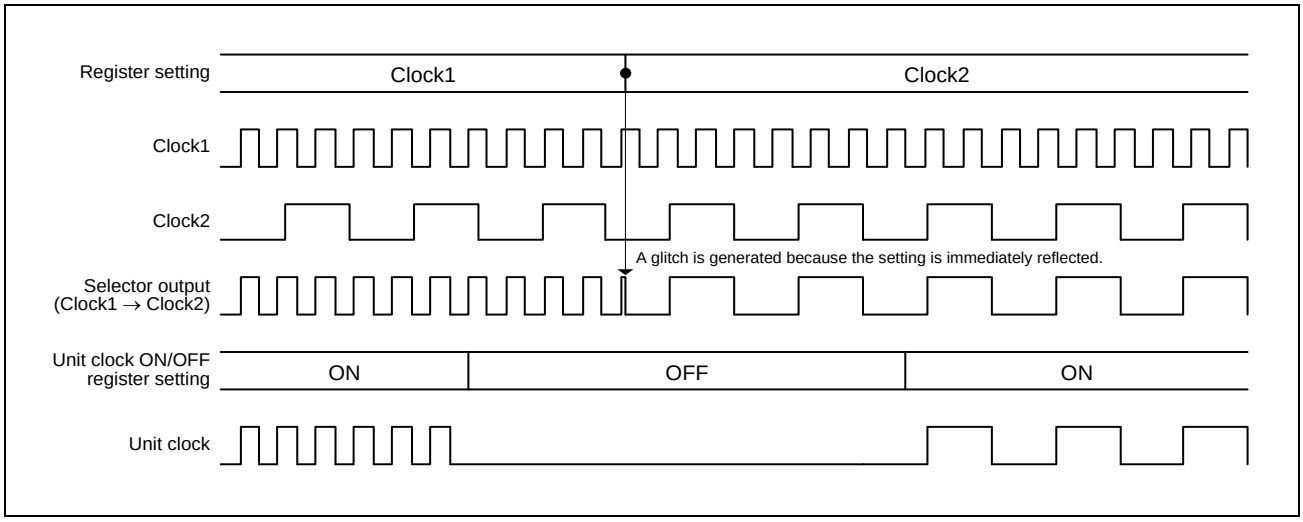


Figure 48.6-14 Timing Chart of Clock Switching of the Static Switching Selector

48.6.1.4 CA53 Control System

An independent system dedicated for Arm Cortex-A53 (CA53).

A clock frequency of 996 MHz is generated by PLL1 based on 48 MHz input externally to the CPG, and it is divided by the divider (DIV A) and then supplied to CA53. A schematic view of the allocation with PLL1 is as shown in **Figure 48.6-15**. For the overall block diagram of the CA53 control system, see **Section 48.3.1, Clock System Diagram**.

This system is for use with the ISP support package, so changing the setting is prohibited.

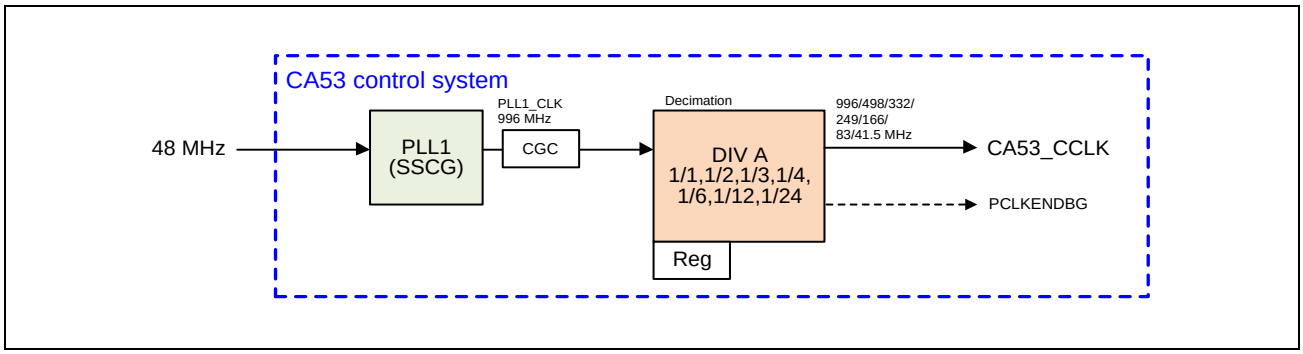


Figure 48.6-15 Block Diagram of the CA53 Control System (PLL1 Peripheral)

48.6.1.5 System Bus/Storage/ISP Control System

A clock frequency of 1600 MHz is generated by PLL2 based on 48 MHz input externally to the CPG or the frequency-divided clock and 48 MHz and the clock signal which is frequency divided by a given divider is supplied to a given unit. For some units, the clock signal is supplied by switching the output clock from PLL2 and 48 MHz.

Also, PLL6 is provided for use in the supply of DCLK (DRPA_DCLK) for DRP-AI and it generates 1260 MHz.

For the block diagram of the system bus control system, storage control system, ISP (video 0) control system, and ISP (video 1) control system, see **Section 48.3.1, Clock System Diagram**.

The system bus and ISP control systems are for use with the ISP support package, so changing the setting is prohibited.

(1) Storage Control System

The storage control clocks comprise a switchable clock signal for NAND and a fixed clock signal.

For clock switching, the divider DIV NFI and the selector SEL SDI0, SEL EMM, or SEL NFI are used.

DIV NFI and SEL NFI are the variable divider and selector in which dynamic switching of the clock frequency is possible. The setting can be changed without generating glitches even while the clock signal is supplied to the unit.

Also, SEL NFI can be used to switch the DIV NFI clock and 48 MHz.

The setting for switching SEL NFI must be made at the same time as that for the other selectors which allow dynamic switching. However, the other selectors are for use with the ISP support package, so changing the settings of these selectors is prohibited.

SEL SDI0 and SEL EMM are set in common by using the register described in **Section 48.5.2.23, SDI/EMM Clock Source Setting Register (CPG_SDIEMM_SSEL)** and can switch 200 MHz and 48 MHz. Since these selectors are for static switching, be sure to switch the clock supply to the target unit off before making the register settings.

Table 48.6-2 lists the available output frequencies for DIV NFI and SEL NFI and **Table 48.6-3** lists the available output frequencies for SEL SDI0. For the setting procedures for DIV NFI, SEL NFI, SEL SDIO/SEL EMM, see **Section 48.5.2.16, NFI Clock Division Ratio Setting Register (CPG_NFI_DDIV)**, **Section 48.5.2.18, PLL/48 MHz Clock Source Setting Register (CPG_CLK48**_DSEL), and **Section 48.5.2.23, SDI/EMM Clock Source Setting Register (CPG_SDIEMM_SSEL)**.

Table 48.6-2 List of NFI_NF_CLK Output Frequency Settings

	Register Setting		Output Frequency
Division Ratio	SELNFI_SET (SEL NFI Setting)	DIVNFI_SET (DIV NFI Setting)	NFI_NF_CLK
1/1	1	00b	400 MHz
1/2		01b	200 MHz
1/4		10b	100 MHz
1/8		11b	50 MHz
Switching 48 MHz	0	—	48 MHz

Table 48.6-3 List of SDI0_CCLK and EMM_CCLK Output Frequency Settings

Register Setting	Output Frequency
SELSDI_SET (SEL SDI0 Setting)	SDI0_CCLK
0	48 MHz
1	200 MHz

Table 48.6-4 lists the related registers.

Table 48.6-4 List of the DIV NFI and SEL NFI Setting Registers

Register Name	Abbreviation	Function
Clock division ratio setting (NFI) register	CPG_NFI_DDIV	NFI clock setting
Clock source setting (PLL/48MHz) register	CPG_CLK48_DSEL	Switching the PLL clock and 48 MHz
Clock source setting (SDI/EMM) register	CPG_SDIEMM_SSEL	SDI0/1 and EMM clock setting

48.6.1.6 LPDDR4 Control System

An independent system dedicated for LPDDR4, MMC, and DDI.

A clock frequency of 1600 to 1200 MHz is generated by PLL3 based on 48 MHz input externally to the CPG, and it is divided by the divider (DIV X) and then supplied to LPDDR4.

Since changing the operating frequency of LPDDR4 after startup is prohibited, do not change the setting.

A schematic view of the allocation with PLL3 is as shown in **Figure 48.6-16**. For the overall block diagram of the LPDDR4 control system, see **Section 48.3.1, Clock System Diagram**.

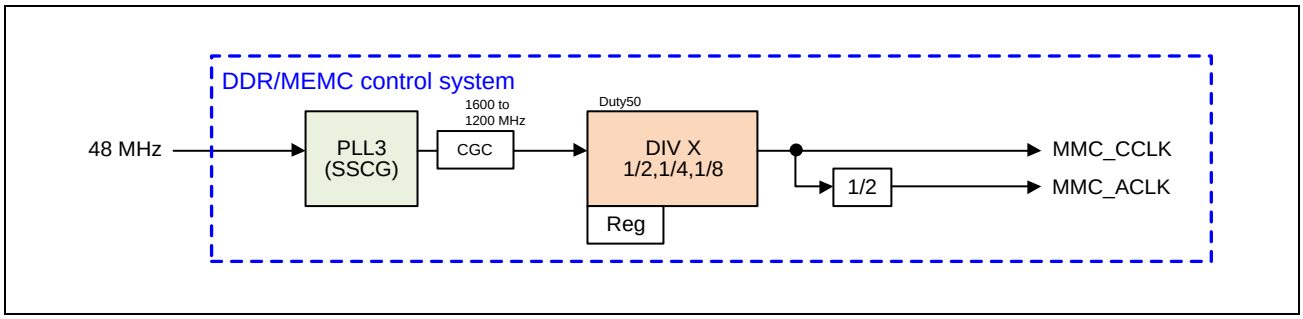


Figure 48.6-16 Block Diagram of the LPDDR4 Control System (PLL3 Peripheral)

48.6.1.7 STG Control System

A clock frequency which is generated by PLL4 based on 24 MHz and 48MHz obtained by dividing 48 MHz input externally to the CPG is switched by the selector (SEL STG0) and then supplied to STG.

A reference clock for PLLs is supplied to an external CMOS image sensor via STG.

This system is for use with the ISP support package, so changing the setting is prohibited.

For the block diagram of the STG control system, see **Section 48.3.1, Clock System Diagram**.

48.6.1.8 Display Control System

A clock signal is generated for the display control units, DCU, and HDMI, and LCI.

This system is for use with the ISP support package, so changing the setting is prohibited.

For the block diagram of the display control system, see **Section 48.3.1, Clock System Diagram**.

48.6.1.9 General-Purpose Clock Control System

For the general-purpose clock (GMCLK0/1), a clock source is selected from the following by the selector (SEL T/U) and a clock signal obtained by frequency division by the divider (DIV T/U) is output.

- Reference clock 48 MHz
- 100 MHz
- PLL4_SELCK
- DISPCLK (PLL7)

For the block diagram of the general-purpose clock control system, see **Section 48.3.1, Clock System Diagram**.

(1) About the Clock Setting

SEL T/U and DIV T/U are the selector and divider for static switching. Be sure to switch the clock supply to the target unit off before making the register settings.

To provide flexibility as a general-purpose clock, the division ratio settings for DIV T/U are available in 13 steps.

Table 48.6-5 and **Table 48.6-6** list the available frequency division settings and output frequencies.

For the setting procedures for SEL T/U and DIV T/U, see **Section 48.5.2.30, GMCLK Clock Division Ratio Setting Register (CPG_GMCLK_SDIV)** and **Section 48.5.2.31, GMCLK Clock Source Setting Register (CPG_GMCLK_SSEL)**.

Table 48.6-5 List of SEL T/U Output Clock Settings

SELT_SET SELU_SET	SEL T SEL U
00b	48 MHz
01b	100 MHz
10b	PL4_SELCK
11b	DISPCLK (PLL7)

Table 48.6-6 List of DIV T/U Frequency Division Settings

DIVT_SET DIVU_SET	DIV T DIV U
0h	SEL T(U)/1
1h	SEL T(U)/2
2h	SEL T(U)/4
3h	SEL T(U)/6
4h	SEL T(U)/8
5h	SEL T(U)/10
6h	SEL T(U)/12
7h	SEL T(U)/16
8h	SEL T(U)/20
9h	SEL T(U)/24
Ah	SEL T(U)/32
Bh	SEL T(U)/40
Ch	SEL T(U)/48
Other than the above	Setting prohibited

Table 48.6-7 lists the related registers.

Table 48.6-7 List of the General-Purpose Clock Control System Setting Registers

Register Name	Abbreviation	Function
Clock division ratio setting (GMCLK) register	CPG_GMCLK_SDIV	DIV T/U division ratio setting
Clock source setting (GMCLK) register	CPG_GMCLK_SSEL	SEL T/U output clock setting

48.6.1.10 ADC and MTR Clocks

ADC and MTR clocks are configured to supply the fixed clock signal produced by frequency division of 48 MHz by 4 and to select and supply the clock signal produced by frequency division of the reference clock 48 MHz and PLL4, respectively.

These clocks are for use with the ISP support package, so changing the settings is prohibited.

For the block diagram, see **Section 48.3.1, Clock System Diagram**.

48.6.1.11 CPU Peripheral Control System

There are the TIM (32 ch.), IIC (4 ch.), WDT (2 ch.), PWM (16 ch.), CSI (6 ch.), and UART (2 ch.) as CPU peripheral units and each unit consists of eight groups from group A to H.

Table 48.6-8 shows the group configuration.

Table 48.6-8 Group Configuration

Group	Unit
Group A	TIM0 to TIM7
	IIC[1:0]
Group B	TIM[15:8]
	IIC[3:2]
Group C	TIM[23:16]
	WDT[1:0]
Group D	TIM[31:24]
Group E	PWM[7:0]
Group F	PWM[15:8]
Group G	CSI[3:0]
	UART[1:0]
Group H	CSI[5:4]

The configuration block diagrams of the respective groups are shown on the following pages.

(1) Group A/B

Groups A and B consist of eight TIMs and two IICs, respectively.

Figure 48.6-17 shows the block diagram.

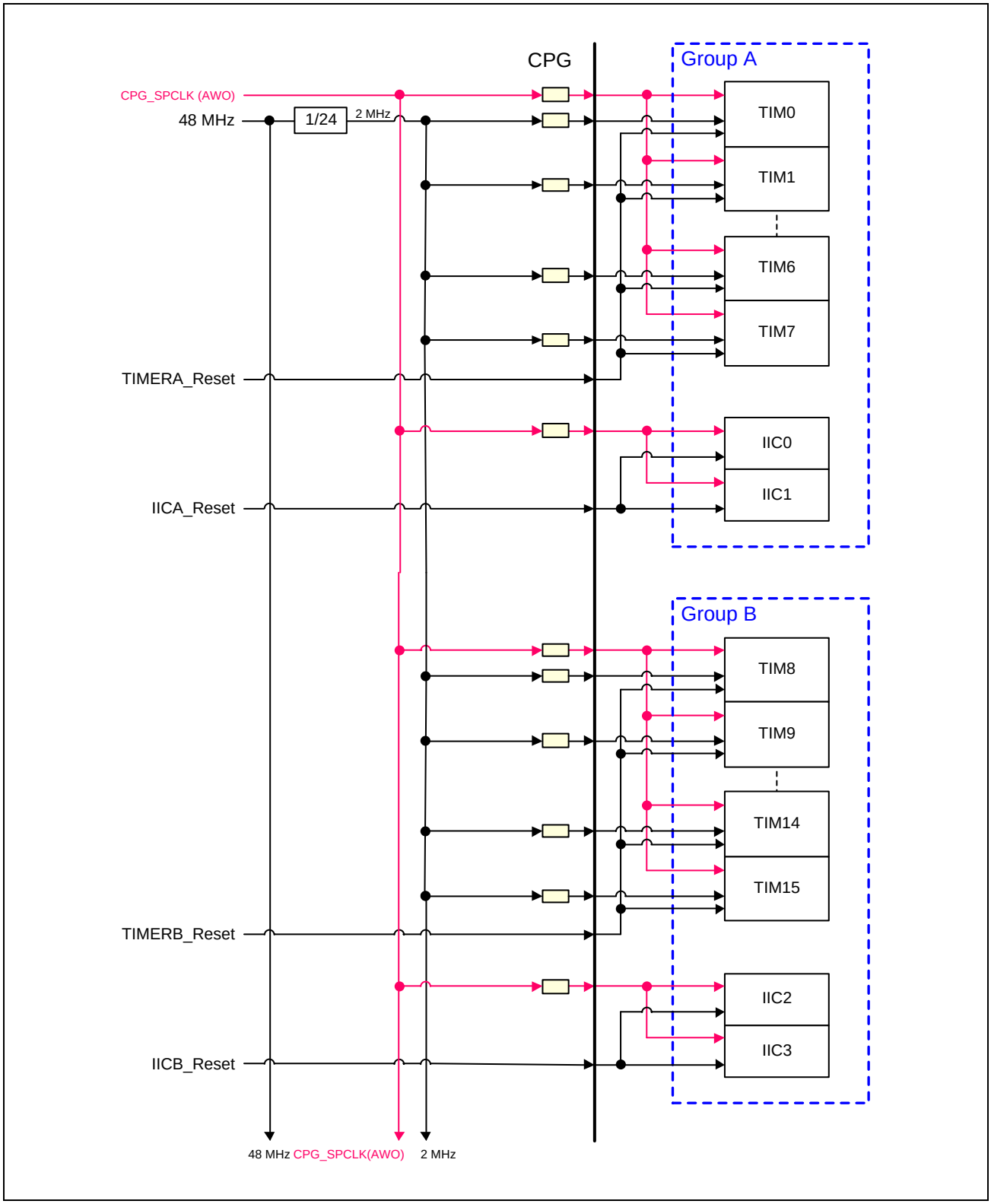


Figure 48.6-17 Block Diagram of Groups A and B

(2) Group C/D

Group C consists of eight TIMs and two WDTs and group D consists of eight TIMs.

Figure 48.6-18 shows the block diagram.

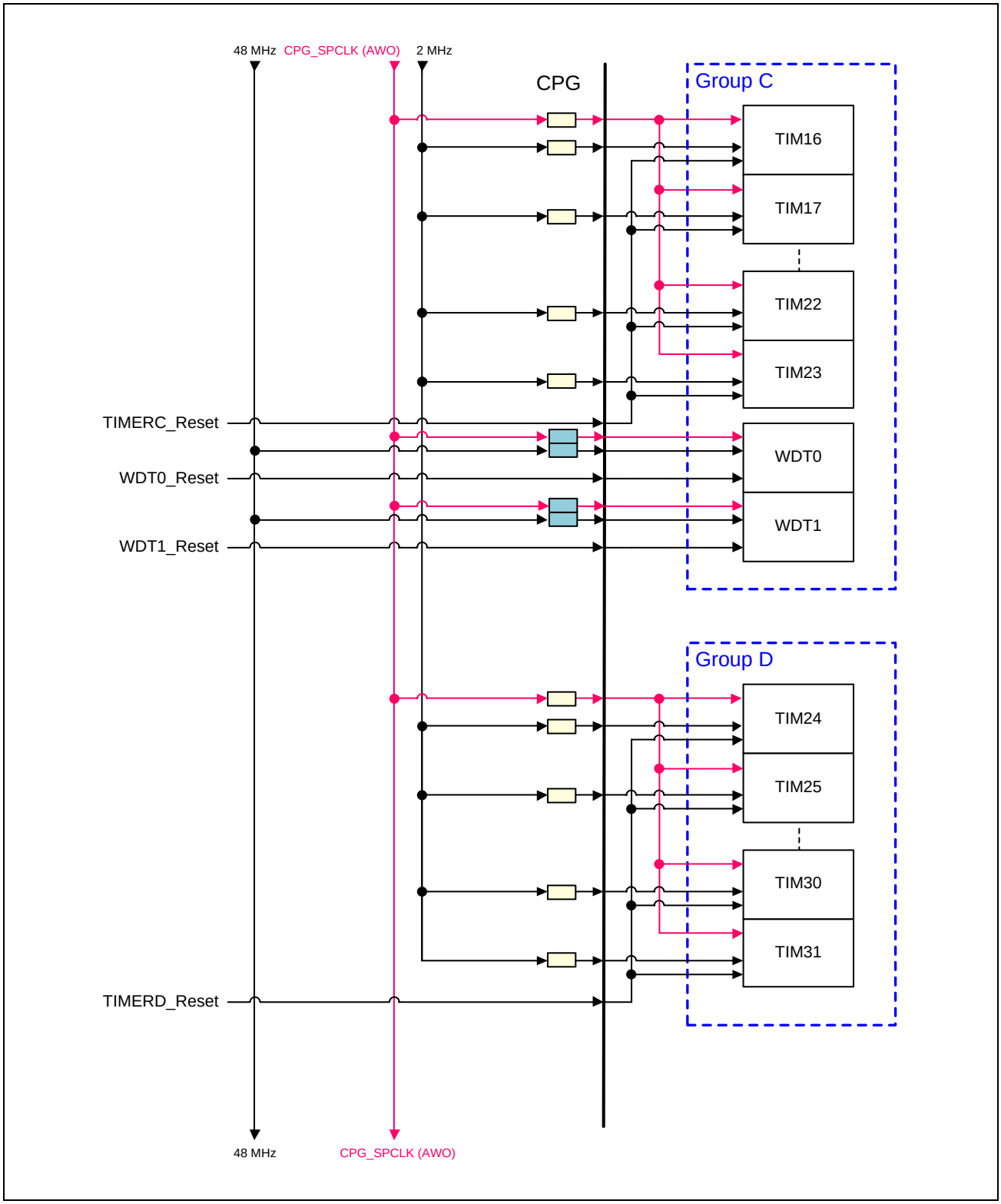


Figure 48.6-18 Block Diagram of Groups C and D

(3) Group E/F

Groups E and F consist of eight PWMs, respectively.

Figure 48.6-19 shows the block diagram.

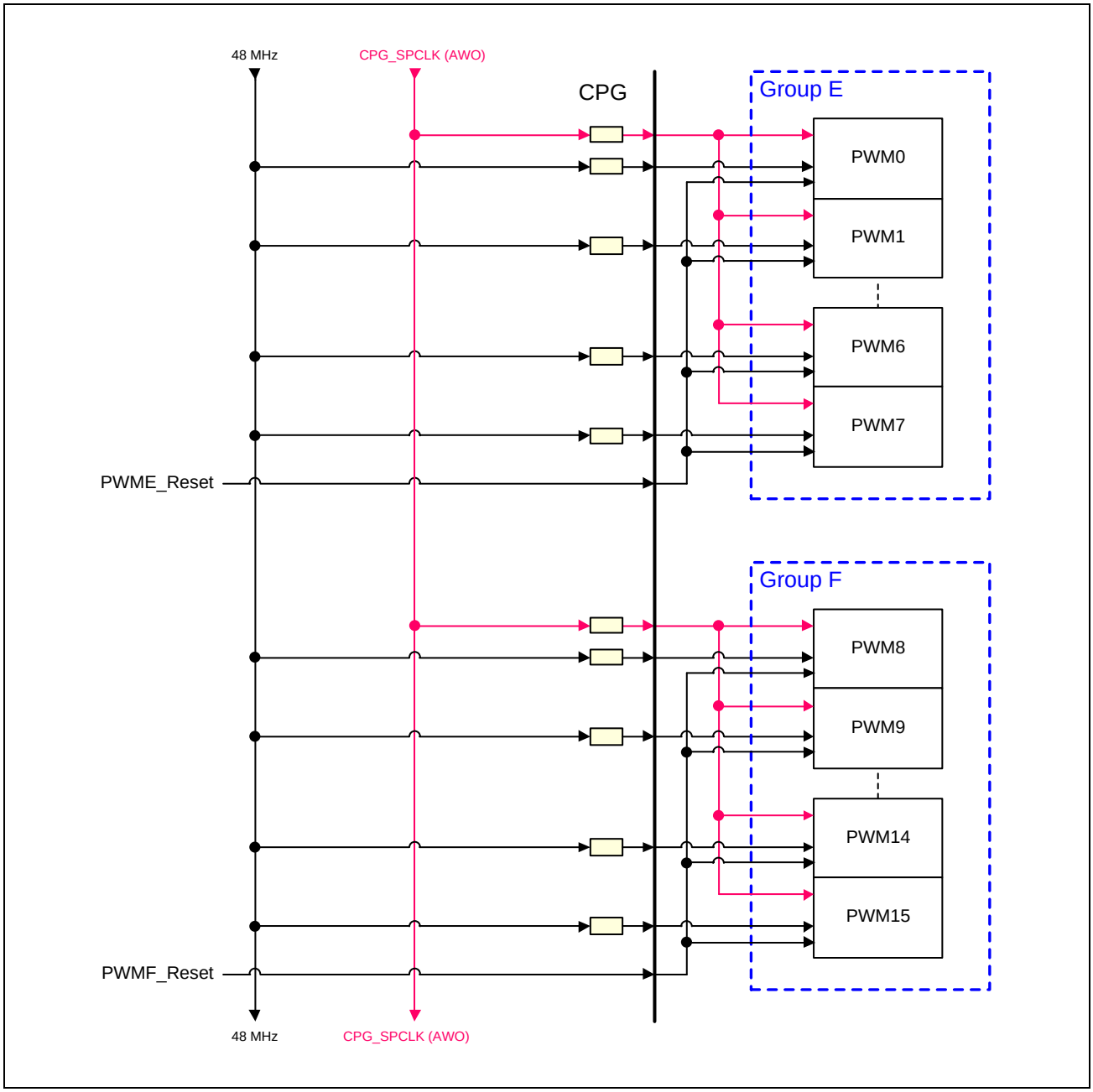


Figure 48.6-19 Block Diagram of Groups E and F

(4) Group G/H

Group G consists of four CSIs and two UARTs and group H consists of two CSIs.

Figure 48.6-20 shows the block diagram.

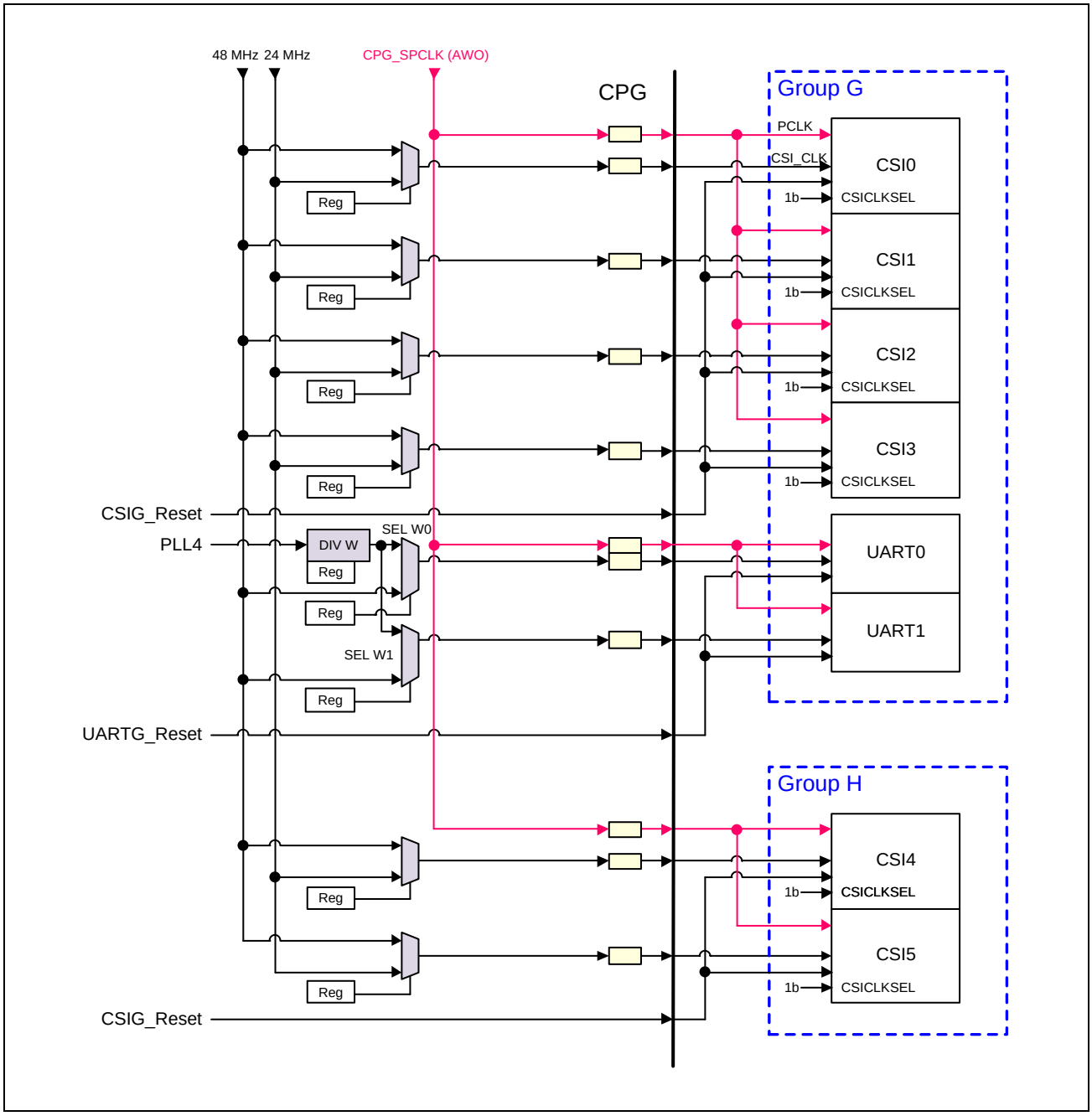


Figure 48.6-20 Block Diagram of Groups G and H

(5) About the UART Master Clock Setting

The clock signal produced by frequency division of the reference clock 48 MHz and PLL4 by the divider (DIV W) is supplied as a clock for communications.

The UART is already used with the ISP support package, so do not change the setting.

(6) About the CSI Frequency Division Setting

The reference clock 48 MHz and 24MHz are selected by the selector (SEL CSI0 to 5) and supplied to a given CSI.

SEL CSI is the selector for static switching. Be sure to switch the clock supply to the target unit off before making the register settings.

Additionally, be sure to set CSI_CLK to supply the frequency no greater than PCLK/2 (CPERI_GRPG_PCLK/2, CPERI_GRPH_PCLK/2).

PCLK is supplied from the output clock CPG_SPCLK (100/50/48 MHz) set by DIV E/SEL E.

Table 48.6-9 lists the SEL CSI selector settings.

Table 48.6-9 List of SEL CSI Output Clock Settings

SEL CSIn (n = 0 to 5)	Output Clock
0	24 MHz
1	48 MHz

48.6.1.12 Unit Clock On/Off Control

The clocks for the respective units can be switched on and off.

Table 48.6-10 lists the related registers.

Table 48.6-10 List of Clock On/Off Setting Registers

Register Name	Abbreviation	Function
Clock ON/OFF control register	CPG_CLK_ON1 to 27	Unit clock on/off setting

48.6.2 Reset Generation and Control Function

48.6.2.1 List of Resets

Table 48.6-11 lists the resets of this LSI chip.

Table 48.6-11 List of Resets

No. *1	Reset Name		Reset Application Range	Source	Description
1	System reset		Overall chip*2	RSTN = L	System reset by the external pin RSTN (generated when the external pin RSTN = L)
				DESRSTN = L & DETRSTN = L or H	System reset from the debugger
				WDT_RST_N[n] = L (n: 0, 1)*3	System reset by the timeout of WDT (generated when WDT_RST_N[n] = L)
2	Debugger reset	Debugger reset (TRSTN)	TAP within the CST	DESRSTN = H & DETRSTN = L	TAP reset from the debugger (generated when the external pin DESRSTN = H and DETRSTN = L)
		Debugger reset (cdbgrstreq)	CA53, debugging function, CST (excluding the register section)	CST_CDBGRSTREQ_CDBGRST = H	Debugging function reset from the debugger (generated when writing 1 to the register bit CDBGRSTREQ in the CST from the debugger)
3	Software control reset	—	Reset per unit	The given reset control bit of CPG_RST1-15 is 0	Reset per unit by the CPG register setting (generated when the given reset control bit of CPG_RST1-15 is 0)

Note 1. No. 1 to 3 are resets by hardware control of the CPG.

Note 2. RTC and PWC are excluded.

Note 3. This is the case when the register CPG_WDT_RST setting is for system reset 2. The dedicated watchdog timers are incorporated respectively in CA53 core 0 and core 1 and a system reset is applied when the counter of either watchdog timer overflows. **Table 48.6-12** lists the correspondence of connection between the CPG and WDT.
For details, see **Section 48.8.14, Reset Range Selection Setting by a WDT Timeout**.

Table 48.6-12 Connection of the Watchdog Timer Reset

Internal Pin of the CPG Unit			Supply Source Unit	
Pin Name	I/O	Active	Unit	Pin Name
WDT_RST_N[0]	Input	Low	WDT0	WDTRSTB
WDT_RST_N[1]	Input	Low	WDT1	WDTRSTB

48.6.2.2 List of Resets to be Applied

Table 48.6-13 lists the resets to be applied for the respective units.

The numbers and symbols in the figure are as follows.

1. System reset
2a. Debugger reset (TRSTN)
2b. Debugger reset (cdbgrstreq)
3a. CA53 SW warm reset (core 0)
3b. CA53 SW Warm Reset (core 1)
4. CA53 SW warm reset (core 1)

The meanings of the symbols in the figure are as follows.

✓: Resets to be asserted or de-asserted in response to the generation of any of the above reset sources

—: Resets not to be asserted or de-asserted in response to the generation of any of the above reset sources

Reg: Depends on the software (the reset control register 1-15 (CPG_RST1-15) setting).

Table 48.6-13 List of Resets to be Applied (1/3)

UNIT	Signal Name	1		2a		2b		3a		3b		4	
		Assert	De-assert	Assert	De-assert	Assert	De-assert	Assert	De-assert	Assert	De-assert	Assert	De-assert
CA53	CA53_NCPUPORESET[0]	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
	CA53_NCPUPORESET[1]	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
	CA53_NCORERESET[0]	✓	✓	—	—	—	—	✓	✓	—	—	Reg	Reg
	CA53_NCORERESET[1]	✓	✓	—	—	—	—	—	—	✓	✓	Reg	Reg
	CA53_NPRESETDBG	✓	✓	—	—	✓	✓	—	—	—	—	Reg	Reg
	CA53_L2RESET	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
	CA53_NMISCRESET_HM	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
	CA53_NMISCRESET_SM	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
	CA53_NARESET	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
RAMB	RAMB_ARESETN[3:0]	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
CST	CST_NTRST	✓	*1	✓	*1	—	—	—	—	—	—	Reg	Reg
	CST_NPOTRST	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
	CST_CS_RESETN	✓	✓	—	—	✓	✓	—	—	—	—	Reg	Reg
	CST_TS_RESETN	✓	✓	—	—	✓	✓	—	—	—	—	Reg	Reg
	CST_TRESETN	✓	✓	—	—	✓	✓	—	—	—	—	Reg	Reg
	CST_SB_RESETN	✓	✓	—	—	✓	✓	—	—	—	—	Reg	Reg
	CST_AHB_RESETN	✓	✓	—	—	✓	✓	—	—	—	—	Reg	Reg
	CST_APB_CA53_RESETN	✓	✓	—	—	✓	✓	—	—	—	—	Reg	Reg
	CST_ATB_SB_RESETN	✓	✓	—	—	✓	✓	—	—	—	—	Reg	Reg
	CST_TS_SB_RESETN	✓	✓	—	—	✓	✓	—	—	—	—	Reg	Reg
PMC	PMC_RESET_N	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
CPG	PG internal reset	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
GIC	GIC_NRESET	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
DMAC	DMAA_ARESETN	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg

Table 48.6-13 List of Resets to be Applied (2/3)

UNIT	Signal Name	1		2a		2b		3a		3b		4	
		Assert	De-assert	Assert	De-assert	Assert	De-assert	Assert	De-assert	Assert	De-assert	Assert	De-assert
RAMA	RAMA_ARESETN	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
ROM	ROM_ARESETN	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
PCIe*2	—	—	—	—	—	—	—	—	—	—	—	—	—
SDI0*2	—	—	—	—	—	—	—	—	—	—	—	—	—
SID1*2	—	—	—	—	—	—	—	—	—	—	—	—	—
eMMC*2	—	—	—	—	—	—	—	—	—	—	—	—	—
NAND*2	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
USB*2	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
SEC	SEC_ARESETN	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
	SEC_PRESETN	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
	SEC_RSTB	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
ETHER*2	—	—	—	—	—	—	—	—	—	—	—	—	—
AUI*2	—	—	—	—	—	—	—	—	—	—	—	—	—
MTR*2	—	—	—	—	—	—	—	—	—	—	—	—	—
ADCA*2	—	—	—	—	—	—	—	—	—	—	—	—	—
ADCB*2	—	—	—	—	—	—	—	—	—	—	—	—	—
ISP*2	—	—	—	—	—	—	—	—	—	—	—	—	—
TIM	TIM_GPA_PRESETN	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
	TIM_GPB_PRESETN	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
	TIM_GPC_PRESETN	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
	TIM_GPD_PRESETN	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
PWM	PWM_GPE_PRESETN	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
	PWM_GPF_PRESETN	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
CSI	CSI_GPG_PRESETN	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
	CSI_GPH_PRESETN	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
IIC	IIC_GPA_PRESETN	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
	IIC_GPB_PRESETN	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
UART	URT_PRESETN	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
WDT0	WDT_PRESETN[0]	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
WDT1	WDT_PRESETN[1]	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
PFC	PFC_PRESETN	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
GRP*2	—	—	—	—	—	—	—	—	—	—	—	—	—
CIF*2	—	—	—	—	—	—	—	—	—	—	—	—	—
DCU*2	—	—	—	—	—	—	—	—	—	—	—	—	—
LCI*2	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
HDMI*2	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
SYC	SYC_RST_N	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
SYS	SYS_RST_N	✓	○	—	—	—	—	—	—	—	—	Reg	Reg

Table 48.6-13 List of Resets to be Applied (3/3)

Unit	Signal Name	1		2a		2b		3a		3b		4	
		Assert	De-assert	Assert	De-assert	Assert	De-assert	Assert	De-assert	Assert	De-assert	Assert	De-assert
TSU0	TSU0_RESETN	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
TSU1	TSU1_RESETN	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
ESI*2	—	—	—	—	—	—	—	—	—	—	—	—	—
LPDDR4 *2	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
STG*2	—	—	—	—	—	—	—	—	—	—	—	—	—
ISP*2	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
GPA*2	—	—	—	—	—	—	—	—	—	—	—	—	—
JPG*2	—	—	—	—	—	—	—	—	—	—	—	—	—
VCD*2	—	—	—	—	—	—	—	—	—	—	—	—	—
ISP*2	—	—	—	—	—	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	—
GPA*2	—	—	—	—	—	—	—	—	—	—	—	—	—
MTD*2	—	—	—	—	—	—	—	—	—	—	—	—	—
DRP-AI	DRPA_ARESETN	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
ICB	ICB_PD_AWO_RST_N	✓	✓	—	—	—	—	—	—	—	—	Reg	Reg
	ICB_PD_MMC_RST_N	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
	ICB_PD_VD0_RST_N	✓	—	—	—	—	—	—	—	—	—	Reg	Reg
	ICB_PD_VD1_RST_N	✓	—	—	—	—	—	—	—	—	—	Reg	Reg

Note 1. SYS_DBGMD = 00 (normal mode): The signal is fixed to the low level (not de-asserted)
1 (debug mode): DETRSTN and CPG_RST2 bit 0 and CST_NPOTRST

Note 2. For more information, contact a Renesas Electronics sales representative.

48.6.2.3 Handling of the Signal for Debugging by the Operating Mode

The SYS_DBGMD signal from the SYS identifies normal mode (0) or debug mode (0) to control the states of SRSTN, TRSTN, and TCK.

SYS_DBGMD is determined by decoding the state of the external pin MD[6:5] by the combinational circuit within the SYS.

For MD[6:5], turn power on while the logic is determined before turning power for this LSI on.

Figure 48.6-21 shows the block diagram and **Table 48.6-14** lists the states of SRSTN, TRSTN, and TCK in respective modes.

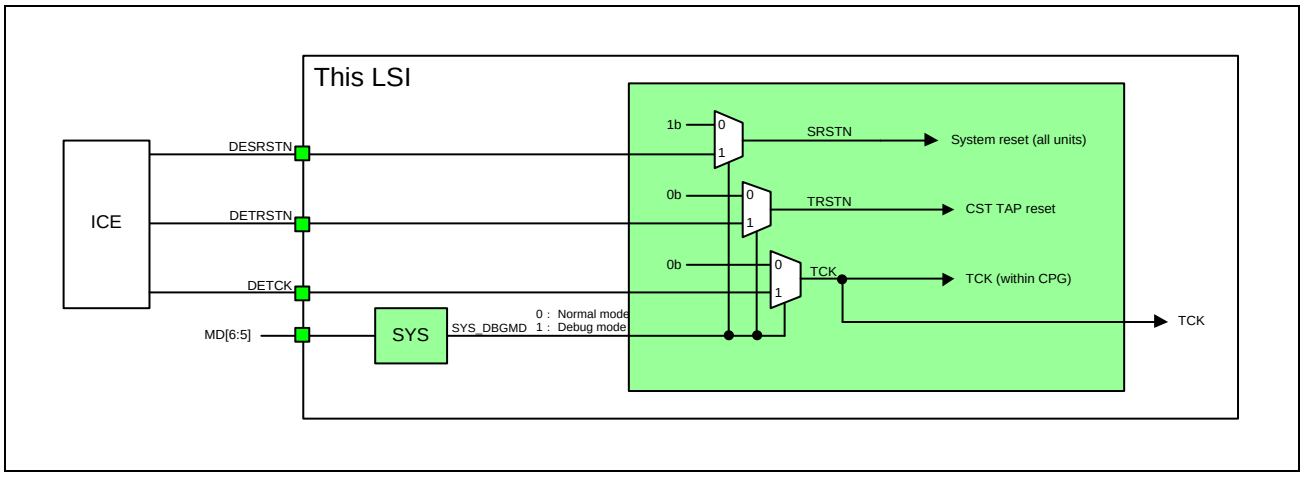


Figure 48.6-21 Block Diagram

Table 48.6-14 States of SRSTN, TRSTN, and TCK

Mode	SYS_DBGMD	SRSTN	TRSTN	TCK
Normal mode	0	Fixed to 1	Fixed to 0	Fixed to 0
Debug mode	1	DESRSTN	DETRSTN	DETCK

48.6.2.4 Software Control Reset

Resetting can be controlled per unit by the CA53 and debugger (via AXI-AP of the CST in the case of the debugger) accessing the reset control register of the CPG.

Figure 48.6-22 shows the schematic diagram.

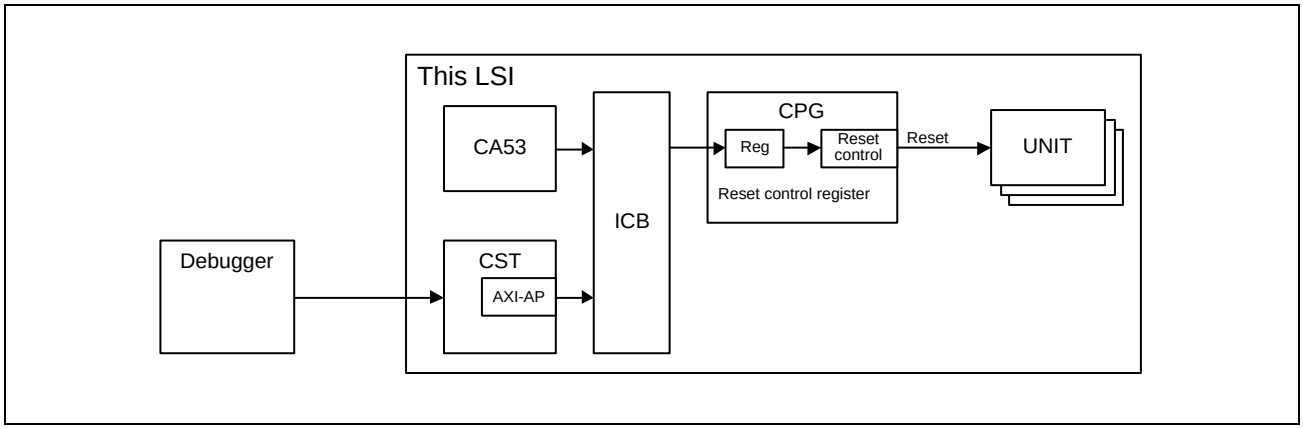


Figure 48.6-22 Schematic Diagram of Software Control Reset

48.6.2.5 Unit Reset Control

The individual units can be reset or released from the reset state by the setting of the reset control register of the CPG (CPG_RST1 to 15).

The method of resetting includes reset control TYPE-A and TYPE-B, and whether TYPE-A or TYPE-B is to be used depends the reset specification of the given units.

Figure 48.6-23 is a schematic view of connections of the respective units and reset control TYPE-A and TYPE-B.

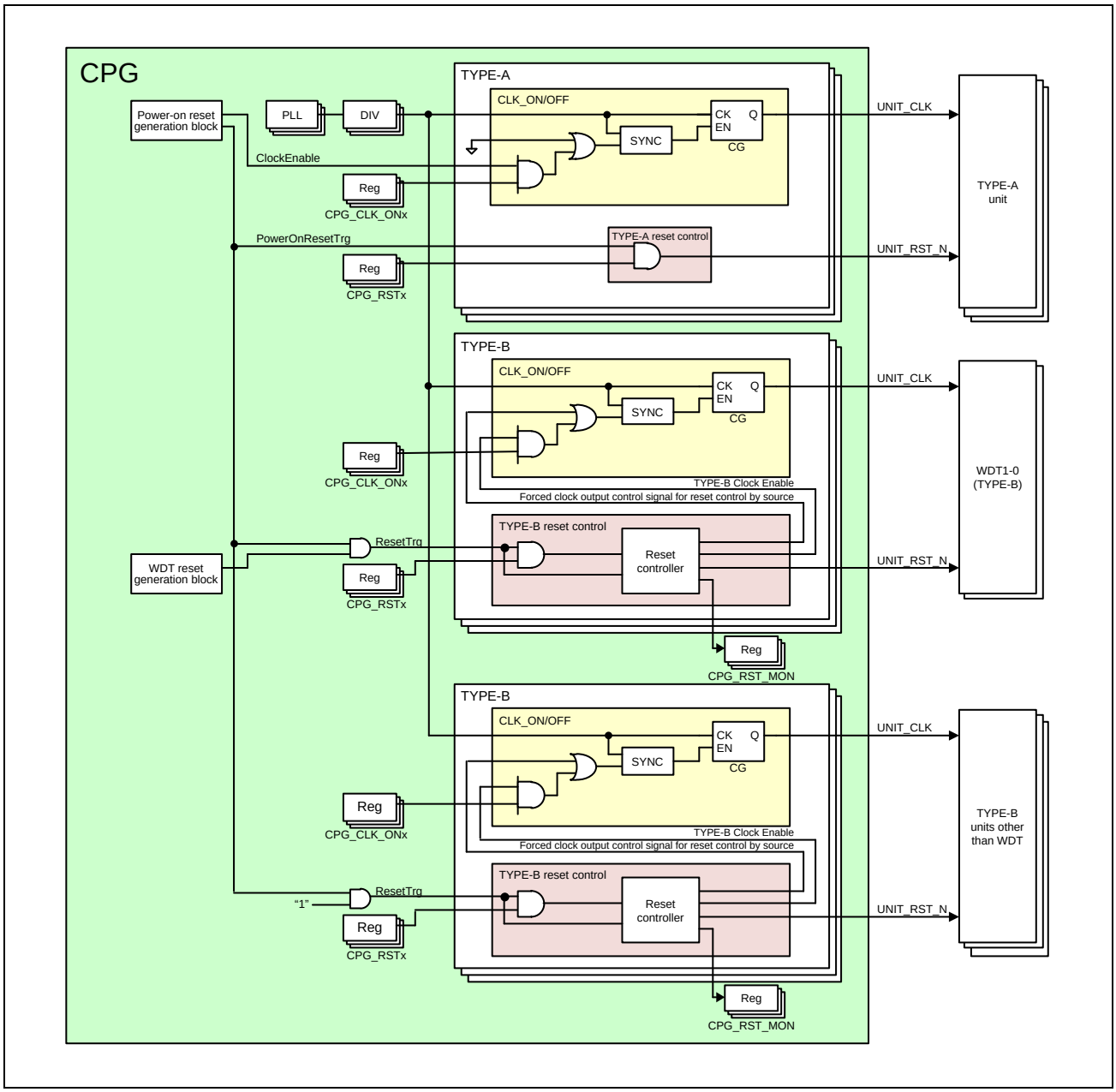


Figure 48.6-23 Schematic View of Connections of Reset Control TYPE-A and TYPE-B

(1) Reset Control TYPE-A

In the case of resetting by TYPE-A, stop the clock signal for the target unit by using the clock ON/OFF control register of the CPG (CPG_CLK_ON1 to 27) before de-asserting the reset signal in order to avoid contention between the timing of de-assertion of the reset and the clock signal.

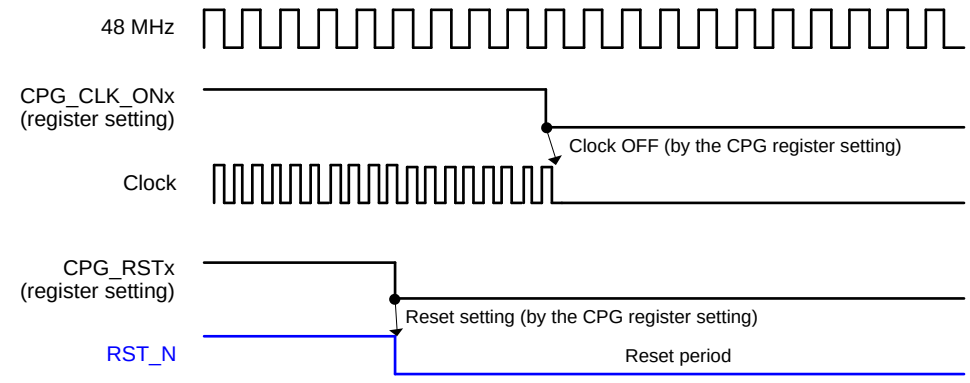
After de-asserting the reset, supply the clock signal after an interval of at least one access cycle.

Switching the clock on or off is not required at the time of a reset.

The reset signal output to a given unit from the CPG can control resetting by the corresponding register bit of the CPG reset control register (CPG_RST1 to 15).

When a system reset occurs, the reset signal is de-asserted after the clock has been stopped by hardware control. The control is returned to the CPG register following the de-assertion of the reset signal.

Figure 48.6-24 and **Figure 48.6-25** show the timing charts and **Table 48.6-16** lists the correspondence between the resets and clocks for the respective units.



Note: Stopping the clock is not required when the reset is asserted.

Figure 48.6-24 Timing of Asserting the TYPE-A Reset by the CPG Register

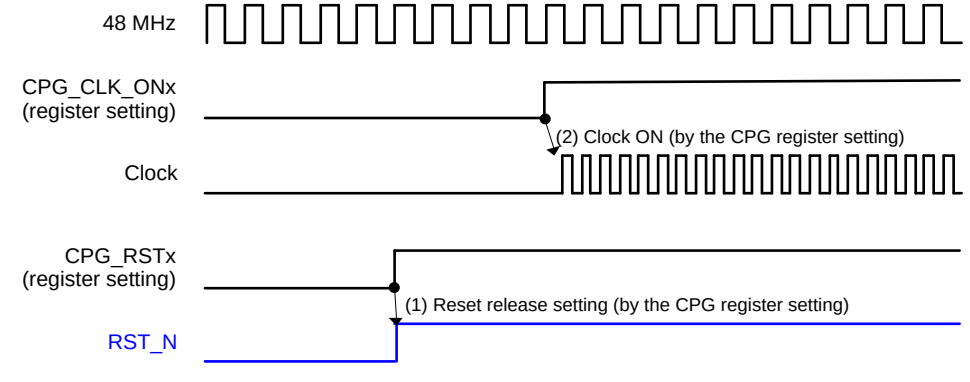


Figure 48.6-25 Timing of De-asserting the TYPE-A Reset by the CPG Register

Table 48.6-15 lists the related registers.

Table 48.6-15 List of the TYPE-A Reset Setting Registers

Register Name	Abbreviation	Function
Clock ON/OFF control register	CPG_CLK_ON1-27	Unit clock on/off setting
Reset control register	CPG_RST1-15	Unit reset setting

Figure 48.6-26 is a timing diagram when a system reset occurs.

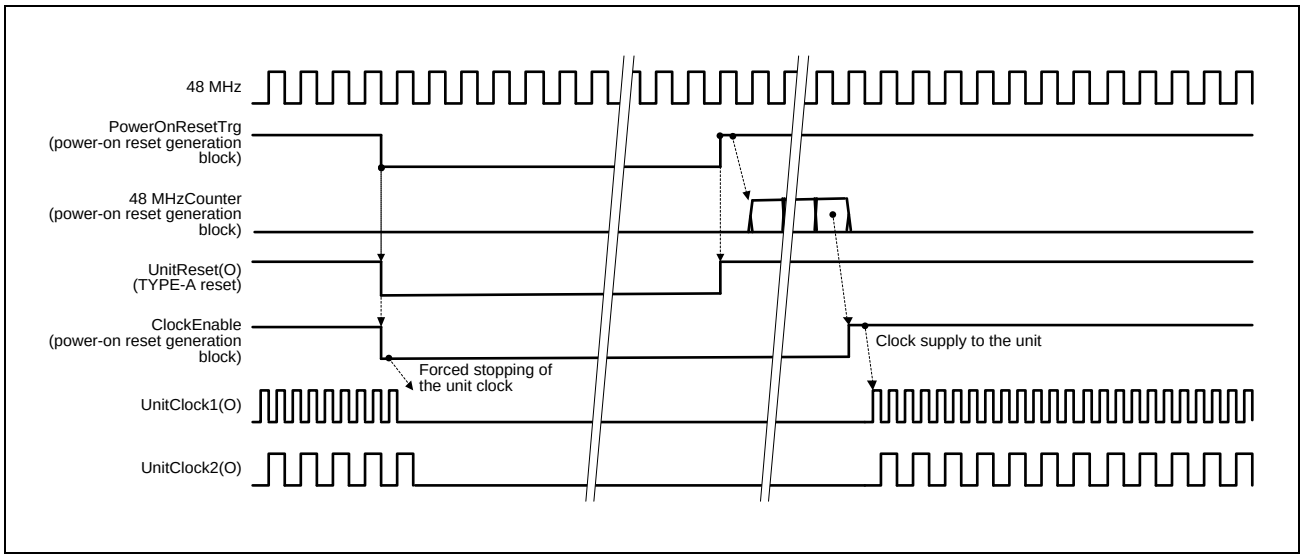


Figure 48.6-26 TYPE-A Reset Timing by a System Reset

Table 48.6-16 Correspondence between the TYPE-A Reset Control Resets and Clocks (1/3)

Unit	Reset			Corresponding Clock			Remarks
		Register			Register		
	Signal Name	(1)	(2)	Signal Name	(3)	(4)	
PCIe*1	—	—	—	—	—	—	
				—	—	—	
USB*1	—	—	—	—	—	—	
	—	—	—	—	—	—	
	—	—	—	—	—	—	
	—	—	—	—	—	—	
SEC	SEC_ARESETN	1	8	SEC_ACLK	1	8	
	SEC_PRESETN	1	9	SEC_PCLK	1	9	
AUI*1	—	—	—	—	—	—	
				—	—	—	
				—	—	—	
MTR*1	—	—	—	—	—	—	
				—	—	—	
				—	—	—	
ADCA*1	—	—	—	—	—	—	
				—	—	—	
ADCB*1	—	—	—	—	—	—	
				—	—	—	
ISP*1	—	—	—	—	—	—	
				—	—	—	
				—	—	—	
TIM7-0	TIM_GPA_PRESETN	6	0	CPERI_GRPA_PCLK	9	0	
				TIM_CLK[7:0]	9	11-4	
TIM15-8	TIM_GPB_PRESETN	6	1	CPERI_GRPB_PCLK	10	0	
				TIM_CLK[15:8]	10	11-4	
TIM23-16	TIM_GPC_PRESETN	6	2	CPERI_GRPC_PCLK	11	0	
				TIM_CLK[23:16]	11	11-4	
TIM31-24	TIM_GPD_PRESETN	6	3	CPERI_GRPD_PCLK	12	0	
				TIM_CLK[31:24]	12	11-4	
IIC1-0	IIC_GPA_PRESETN	6	8	IIC_PCLK[0]	9	12	
IIC3-2	IIC_GPB_PRESETN	6	9	IIC_PCLK[1]	10	12	
PFC	PFC_PRESETN	1	2	PFC_PCLK	1	2	
GRP*1	—	—	—	—	—	—	
CIF*1	—	—	—	—	—	—	
				—	—	—	
				—	—	—	
DCU*1	—	—	—	—	—	—	
				—	—	—	
				—	—	—	

Table 48.6-1 Correspondence between the TYPE-A Reset Control Resets and Clocks (2/3)

Unit	Reset			Corresponding Clock			Remarks
		Register			Register		
	Signal Name	(1)	(2)	Signal Name	(3)	(4)	
LCI*1	—	—	—	—	—	—	
				—	—	—	
				—	—	—	
	—	—	—	—	—	—	
HDMI*1	—	—	—	—	—	—	
	—	—	—	—	—	—	
SYS	SYS_RST_N	1	1	SYS_CLK	1	1	
TSU0	TSU0_RESETN	1	12	TSU0_PCLK	1	14	
TSU1	TSU1_RESETN	1	13	TSU1_PCLK	1	15	
ESI*1	—	—	—	—	—	—	
				—	—	—	
				—	—	—	
LPDDR4 *1	—	—	—	—			
	—	—	—				
	—	—	—				
	—	—	—				
	—	—	—				
	—	—	—				
STG*1	—	—	—	—	—	—	
				—	—	—	
ISP*1	—	—	—	—	—	—	
				—	—	—	
	—	—	—	—	—	—	
GPA*1	—	—	—	—	—	—	
ISP*1	—	—	—	—	—	—	
				—	—	—	
	—	—	—	—	—	—	
GPA*1	—	—	—	—	—	—	
MTD*1	—	—	—	—	—	—	
				—	—	—	

Table 48.6-2 Correspondence between the TYPE-A Reset Control Resets and Clocks (3/3)

Unit	Reset			Corresponding Clock			Remarks
		Register			Register		
	Signal Name	(1)	(2)	Signal Name	(3)	(4)	
ICB	ICB_PD_AWO_RST_N	7	0	ICB_ACLK1	16	0	ICB_GIC_CLK is interlinked with ICB_ACLK1 (separate control is not possible).
				ICB_GIC_CLK			
				ICB_CST_CS_CLK	16	11	
				ICB_DRPA_ACLK	17	0	
				ICB_MPCLK1	16	2	
				ICB_CST_ATB_SB_CLK	16	10	
				ICB_SPCLK1	16	3	
				ICB_DCI_CLKAXI	16	14	
				ICB_CLK100_1	16	12	
				ICB_ETH0_CLK_AXI	16	13	
				ICB_CLK48	16	4	
				ICB_SYC_CNT_CLK	16	15	
	ICB_PD_MMC_RST_N	7	1	ICB_CLK48_2	16	5	
				ICB_MMC_ACLK	17	8	
	ICB_PD_VD0_RST_N	7	2	ICB_CLK48_3	16	6	
				ICB_MPCLK3	18	0	
				ICB_CIMA_CLK	18	1	
				ICB_CIMB_CLK	18	2	
	ICB_PD_VD1_RST_N	7	3	ICB_CLK48_4L	16	7	ICB_CLK48_4L and ICB_CLK48_4R are controlled simultaneously (separate control is not possible).
				ICB_CLK48_4R			
				ICB_MPCLK4	18	12	
				ICB_VD_ACLK4	18	11	
				ICB_BIMA_CLK	18	8	
				ICB_VCD_PCLK4	18	13	
				ICB_FCD_CLKAXI	18	9	
	ICB_PD_RFX_RST_N	7	4	ICB_CLK48_5	16	9	
				ICB_RFX_ACLK ICB_RFX_PCLK5	17	4	ICB_RFX_PCLK5 and ICB_RFX_ACLK are controlled simultaneously (separate control is not possible).

Note: (1) Reset control register (CPG_RST1-15) number
(2) Reset control register control bit
(3) Clock ON/OFF control register (CPG_CLK_ON1-27)
(4) Clock ON/OFF control register control bit

Note 1. For more information, contact a Renesas Electronics sales representative.

(2) Reset Control TYPE-B

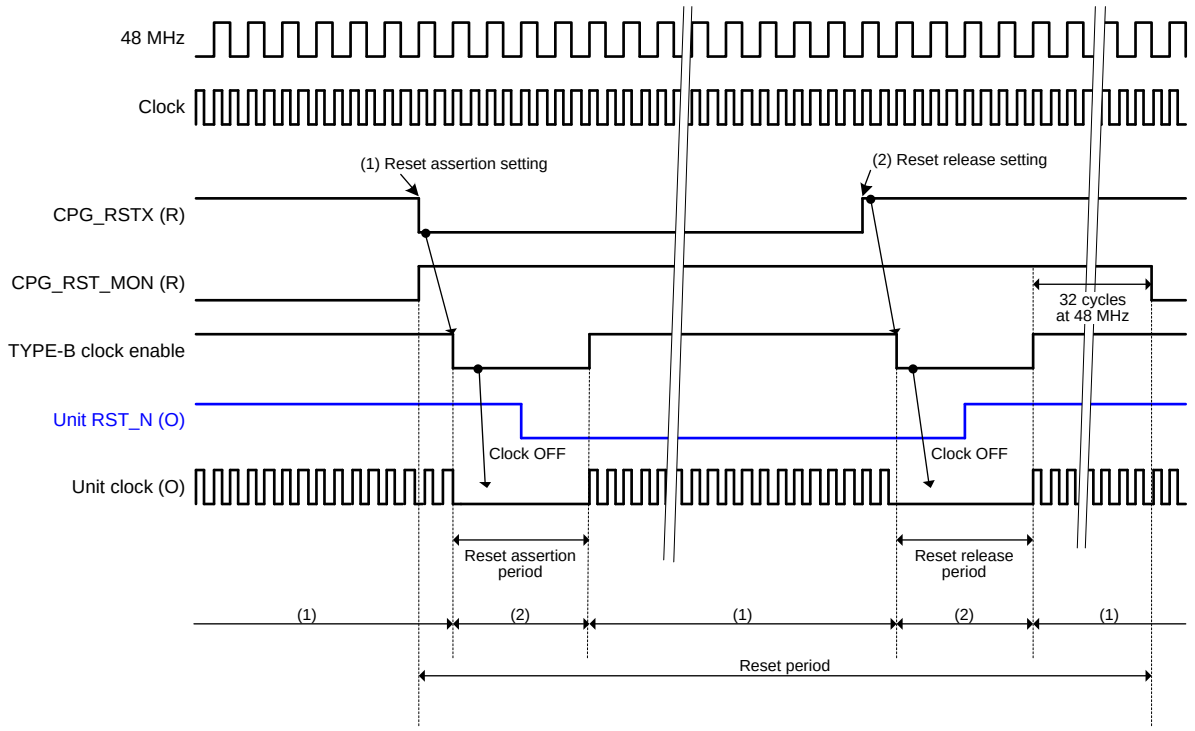
Units incorporated in this LSI includes the units which require clock supply during a reset (target units*[1]). Therefore, even if the clock is switched off by the clock ON/OFF control register of the CPG at the time of a reset in response to the corresponding reset source, the clock is forcibly supplied over a certain period by hardware control.

For these units, control is required to stop the clock for several clock cycles, in order to avoid contention between the timing of a reset and release from the reset and the clock edge. Otherwise, switch the clock on or off by the CPG register.

In the case of resetting by TYPE-B, there is a delay over a certain period until the CPG output is released from the reset after reset release has been set. The reset state of the CPG output can be checked by reading the internal register of the CPG (CPG_RST_MON). Read the CPG_RST_MON register to check that the target unit is released from the reset state before operating this unit.

Note 1. Target units
DMAC, RAMA/B, GIC, ROM, SDI0/1, eMMC, NAND, SEC, ETHER, PWM, CSI, UART, WDT, SYC, VCD,DRP-AI, PMC, JPG

Figure 48.6-27 shows the timing chart.



Note: (1) Clock ON/OFF control by CPG_CLK_ONx
(2) Masking the clock by the reset control circuit with a change in (assertion or de-assertion of) the reset signal (clock OFF)

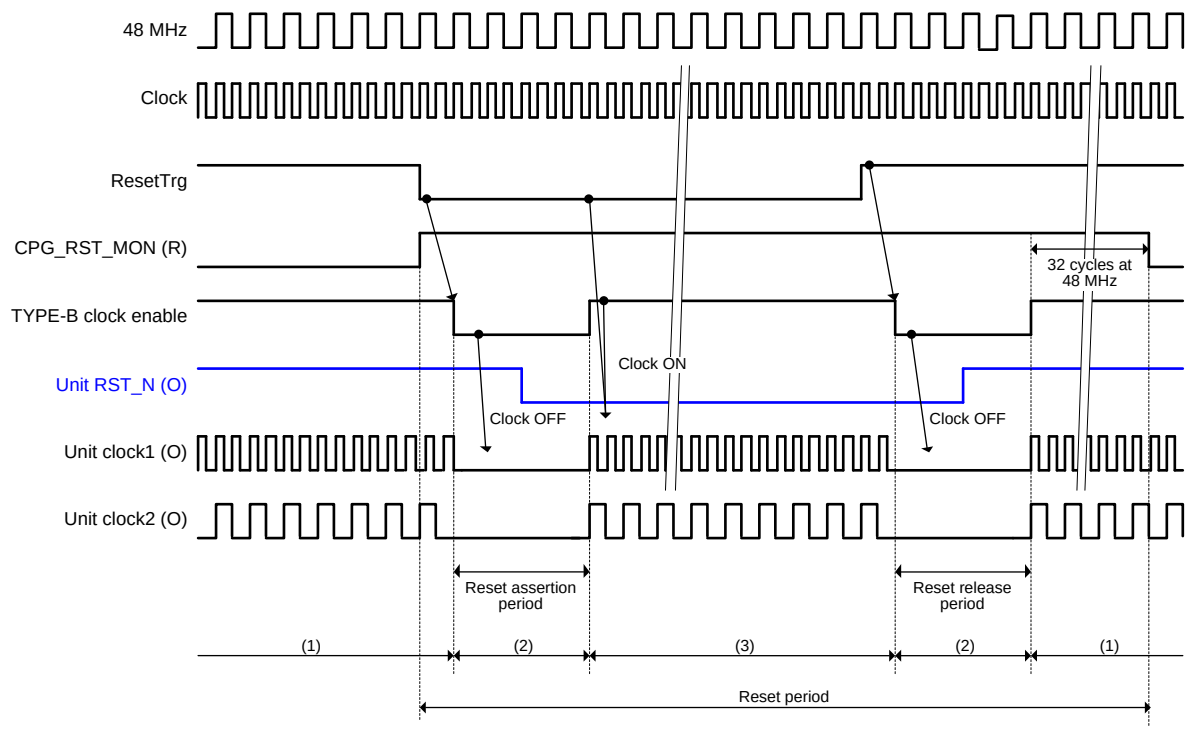
Figure 48.6-27 TYPE-B Reset Timing by the CPG Register

Table 48.6-17 lists the related registers.

Table 48.6-17 List of the TYPE-B Reset Setting Registers

Register Name	Abbreviation	Function
Clock ON/OFF control register	CPG_CLK_ON1-27	Unit clock on/off setting
Reset control register	CPG_RST1-15	Unit reset setting
Reset monitor register	CPG_RST_MON	Unit reset monitoring

Figure 48.6-28 is a timing diagram when a system reset occurs.



Note: (1) Clock ON/OFF control by CPG_CLK_ONx
(2) Masking the clock by the reset control circuit with a change in (assertion or de-assertion of) the reset signal (clock OFF)
(3) Forced clock supply when the reset is asserted

Figure 48.6-28 TYPE-B Reset Timing by the Reset Source

Table 48.6-18 Correspondence between the TYPE-B Reset Control Resets and Clocks

Unit	Reset			Corresponding Clock			Remarks
		Register			Register		
	Signal Name	(1)	(2)	Signal Name	(3)	(4)	
RAMB	RAMB_ARESETN[3:0]	12	0	RAMB_ACLK	23	0	
PMC	PMC_RESET_N	1	14	PMC_CORE_CLOCK	1	4	
GIC	GIC_NRESET	1	4	GIC_CLK	1	5	
DMAC	DMAA_ARESETN	1	7	DMAA_ACLK	1	11	
RAMA	RAMA_ARESETN	1	5	RAMA_ACLK	1	6	
ROM	ROM_ARESETN	1	6	ROM_ACLK	1	7	
SDI0*1	—	—	—	—	—	—	
SDI1*1	—	—	—	—	—	—	
eMMC*1	—	—	—	—	—	—	
NAND*1	—	—	—	—	—	—	
				—	—	—	
	—	—	—	—	—	—	
				—	—	—	
SEC	SEC_RSTB	1	10	SEC_TCLK	1	10	
ETHER*1	—	—	—	—	—	—	
				—			
PWM7-0	PWM_GPE_PRESETN	6	4	CPERI_GRPE_PCLK	13	0	
				PWM_CLK[7:0]	13	11-4	
PWM15-8	PWM_GPF_PRESETN	6	5	CPERI_GRPF_PCLK	14	0	
				PWM_CLK[15:8]	14	11-4	
CSI3-0	CSI_GPG_PRESETN	6	6	CPERI_GRPG_PCLK	15	0	
CSI5-4	CSI_GPH_PRESETN	6	7	CPERI_GRPH_PCLK	15	1	
UART1-0	URT_PRESETN	6	10	URT_PCLK	15	4	
				URT_CLK[1:0]	15	6-5	
WDT0	WDT_PRESETN[0]	6	12	WDT_PCLK[0]	11	12	
				WDT_CLK[0]	11	13	
WDT1	WDT_PRESETN[1]	6	13	WDT_PCLK[1]	11	14	
				WDT_CLK[1]	11	15	
SYC	SYC_RST_N	5	9	SYC_CNT_CLK	8	12	
JPG*1	—	—	—	—	—	—	
				—	—	—	
				—	—	—	
VCD*1	—	—	—	—	—	—	
				—			
DRP-AI	DRPA_ARESETN	9	0	DRPA_INITCLK	20	2	

Note: (1) Reset control register (CPG_RST1-15) number
(2) Reset control register control bit
(3) Clock ON/OFF control register (CPG_CLK_ON1-27)
(4) Clock ON/OFF control register control bit

Note 1. For more information, contact a Renesas Electronics sales representative.

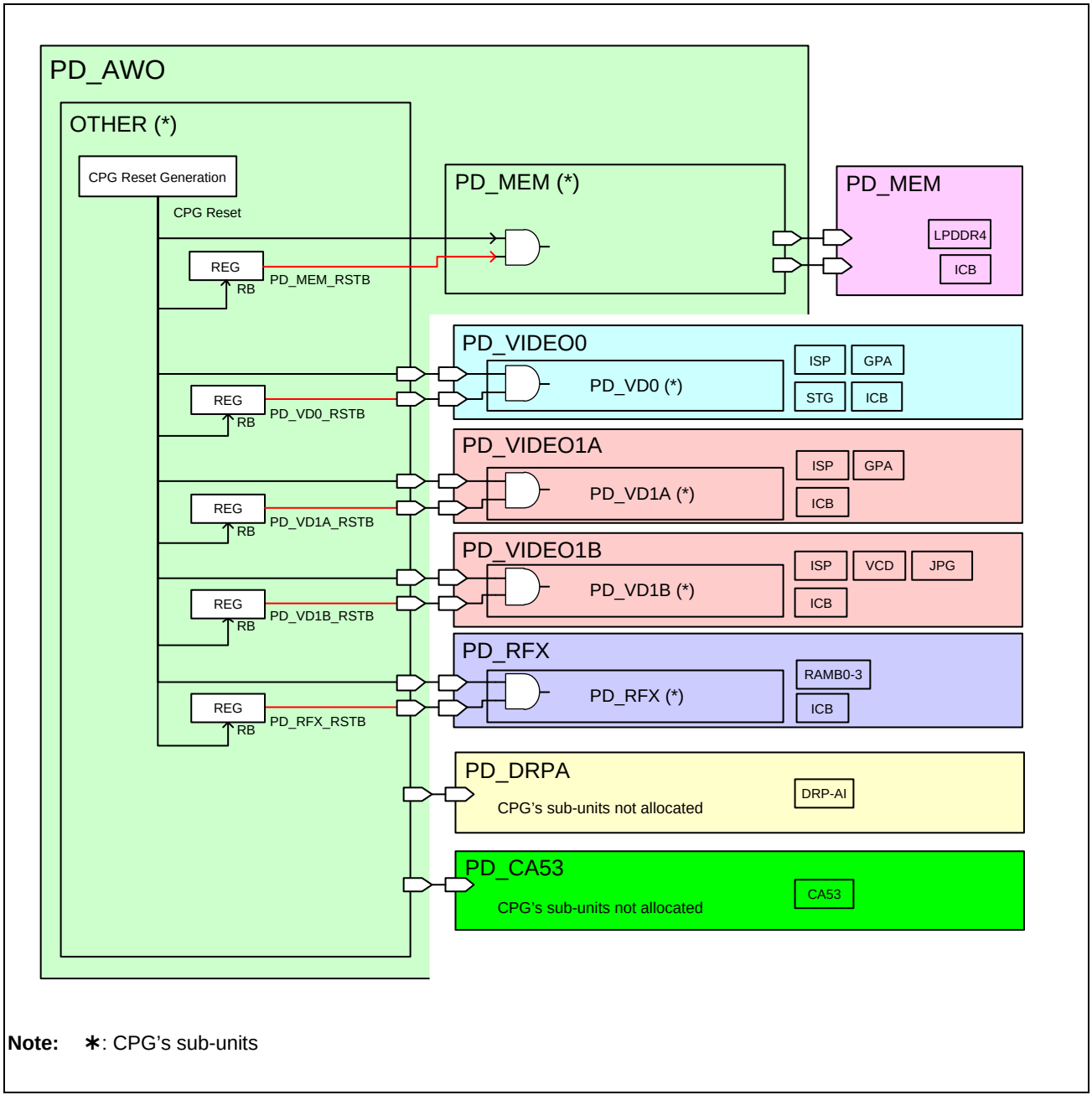
48.6.2.6 Software Reset Control for the CPG's Sub-Units Allocated in the Power Domain

Though most of the sub-units of the CPG are allocated in the PD_AWO power domain, some sub-units of the CPG which control resetting of the clock signal are allocated in the power domain to which the units as the destinations for the clock and reset supply belong.

"CPG Reset" from the CPG reset generation block in **Figure 48.6-29** is only asserted when a system reset occurs, and it is not asserted when the power domain is switched from off to on by PMC control during normal operation.

Therefore, when switching the power domain from off to on during normal operation, the sub-units allocated in the power domain other than PD_AWO must be initialized by a software reset with the CPG register.

Note that the power domains PD_VIDEO0, PD_VIDEO1A/B, PD_RFX, PD_DRPA, and PD_CA53 are already used with the ISP support package, so do not reset them.



Note: ∗: CPG's sub-units

Figure 48.6-29 Block Diagram of the Allocation of the Power Domains of the CPG's Sub-Units

■ Initialization of the CPG's Sub-Units

The sub-units of the CPG which are allocated in the power domain other than PD_AWO within the CPG are reset by setting the corresponding bit of the CPG power domain reset control register (CPG_PD_RST) to 0 and released from the reset state by setting the same bit to 1.

Table 48.6-19 lists the reset settings for the sub-units of the CPG.

Table 48.6-19 List of the Reset Settings for the CPG's Sub-Units

Field Name	Reset Range
PD_MEM_RSTB	CPG's sub-unit PD_MEM allocated in the power domain PD_AWO
PD_VD0_RSTB	CPG's sub-unit PD_VD0 allocated in the power domain PD_VIDEO0
PD_VD1A_RSTB	CPG's sub-unit PD_VD1A allocated in the power domain PD_VIDEO1A
PD_VD1B_RSTB	CPG's sub-unit PD_VD1A allocated in the power domain PD_VIDEO1B
PD_RFX_RSTB	CPG's sub-unit PD_RFX allocated in the power domain PD_RFX

Note that the mode setting registers are included in the sub-units OTHER of the CPG.

The sub-units OTHER of the CPG are only initialized at the time of a system reset.

Table 48.6-20 gives the reset range for the functions of the CPG's sub-units.

Table 48.6-20 Reset Effect Range for the Functions of the CPG's Sub-Units

Field Name	Reset Effect Range	
PD_MEM_RSTB	PLL/PLL control	PLL3, PLL3 control section
	Divider (division ratio variable)	DIV_X*1
	Divider (division ratio fixed)	DIV_X_DIV2
	Division ratio initialization	DIV_X_REG_SYNC
	Clock on/off	MMC_CORE_DDRC_CORE_CLK, MMC_ACLK, MMC_PCLK, DDI_APBCLK, ICB_MMC_ACLK

Note 1. The CPG_MMCDDI_DDIV register value is changed with the PLL3 clock within the CPG's sub unit PD_MEM after it is retained with the Xtal clock and the changed value is initialized when PD_MEM_RSTB is set to 0.
For the CPG_MMCDDI_DDIV register, set the frequency division ratio after PD_MEM_RSTB is set to 1 and PLL3 is locked.

Table 48.6-21 lists the related registers.

Table 48.6-21 List of the CPG's Sub-Unit Software Reset Control Register Allocated in the Power Domain

Register Name	Abbreviation	Function
CPG power domain reset control register	CPG_PD_RST	Reset control per power domain of the CPU's sub-units

48.7 Operating Procedure

48.7.1 Procedure for Writing to the Registers

The following registers consist of the 16 higher-order bits which are write enable and the 16 lower-order bits which are normal data registers, so changing only the value of the specified bits is possible without read-modify-write operations.

When changing the value, write 1 to the bit plus 16 of the bit to be changed.

Example)
To set bit[0] to 1b, write 0001_0001h. To set it to 0b, write 0001_0000h. The value of bit[15:0] is not changed when 0000_xxxxh is written.

- Clock division ratio (NAND) register (CPG_NFI_DDIV)
- Clock source setting (PLL/48MHz) register (CPG_CLK48_DSEL)
- Clock source setting (SDI/eMMC) register (CPG_SDIEMM_SSEL)
- Clock division ratio setting (GMCLK) register (CPG_GMCLK_SDIV)
- lock source setting (GMCLK) register (CPG_GMCLK_SSEL)
- Clock source setting (CSI_REF) register (CPG_CSI_RCLK_SSEL)
- Clock ON/OFF control register n (CPG_CLK_ONn) n = 1 to 27
- WDT reset range select register (CPG_WDT_RST)
- Reset mask register (CPG_RST_MSK)
- Reset control register n (CPG_RSTn) n = 1 to 15
- CPG power domain reset control register (CPG_PD_RST)

CAUTION

When read, the 16 higher-order bits are always read as 0.

The following registers are read-only, so writing has no effect.

- Clock status monitor register (CPG_CLKSTATUS)
- Reset monitor register (CPG_RST_MON)

48.7.2 Procedure for Setting the Division Ratio for the Dynamic Switching Divider

Follow the procedure below when setting the frequency division ratio for the divider which allows dynamic switching.

* The procedure for switching DIV NFI is described as an example.

1. Checking the state of DIV NFI (checking that it is not in the busy state)

   Check the following bit of the clock status monitor register (CPG_CLKSTATUS).

   - Checking the state of DIV NFI: Bit 6 (DIVNFI_STS) must be 0 (switching is completed).

   * Wait until the above condition is satisfied.

2. Setting the frequency division ratio for DIV NFI

   Set the following bits of the clock division ratio setting (NAND) register (CPG_NFI_DDIV).

   - Setting the frequency division ratio: Bits 1 and 0 (DIVNFI_SET) = any value; bit 16 (DIVNFI_WEN) = 1

3. Checking the state of DIV NFI (checking that it is not in the busy state)

   Check the following bit of the clock status monitor register (CPG_CLKSTATUS).

   - Checking the state of DIV NFI: Bit 6 (DIVNFI_STS) must be 0 (switching is completed).

   * Wait until the above condition is satisfied.

The procedure above is applicable to the following registers.

- Clock division ratio setting (NAND) register (CPG_NFI_DDIV)

The following register is for monitoring the state.

- Clock status monitor register (CPG_CLKSTATUS)

Even when the setting has not been changed, writing 1 to “xx_WEN” allocated in the 16 higher-order bits of the register starts clock switching, so a wait is required until the completion of switching by the status monitor (CPG_CLKSTATUS) (the clock is stopped once at the time of switching).

48.7.3 Procedure for Setting the Static Switching Divider and the Selector

Follow the procedure below when setting the frequency division ratio for the static switching divider and setting the clock for the selector. Basically, the procedure is as follows: Switching the corresponding clock off → Setting for switching → Switching the clock on.

* The procedure for switching GMCLK0 (DIV T, SEL T) is described as an example.

1. Setting for switching the general-purpose clock (GMCLK0) off

   Set the following bit of the clock ON/OFF control register 7 (CPG_CLK_ON7).

   - Setting for switching the clock off: Bit 4 (CLK4_ON) = 0; bit 20 (CLK4_ONWEN) = 1

2. Setting the frequency division ratio for DIV T

   Set the following bits of the clock division ratio setting (GMCLK) register (CPG_GMCLK_SDIV) while the clock supply is stopped after at least three cycles of the general-purpose clock have elapsed*[1].

   - Setting the frequency division ratio: Bits 3 to 0 (DIVT_SET) = any value*[2]; bit 16 (DIVT_WEN) = 1

3. Setting the SEL T selector

   Set the following bits of the clock source setting (GMCLK) register (CPG_GMCLK_SSEL).

   - Setting the frequency division ratio: Bits 1 and 0 (SELT_SET) = any value; bit 16 (SELT_WEN) = 1

4. Setting for switching the general-purpose clock (GMCLK0) on*[2]

   Set the following bits of the clock ON/OFF control register 7 (CPG_CLK_ON7)

   - Setting for switching the clock on: Bit 4 (CLK4_ON) = 1; bit 20 (CLK4_ONWEN) = 1

Note 1. Reflection of the setting for switching the clock on or off in the clock pin depends on the clock. See “Clock ON/OFF Control Register 1 to 27 (CPG_CLK_ON 1 to CPG_CLK_ON27)”, and **Section 48.8.8, Interval of Access to the Clock ON/OFF Control Registers**.

Note 2. The static switching divider requires up to one cycle of the clock before switching for reflection of the register value.
Accordingly, after setting the frequency division ratio, insert a wait of at least one cycle of the clock corresponding to the setting before switching.

The procedure above is applicable to the following registers.

- Clock source setting (SDI/eMMC) register (CPG_SDIEMM_SSEL)
- Clock division ratio setting (GMCLK) register (CPG_GMCLK_SDIV)
- Clock source setting (GMCLK) register (CPG_GMCLK_SSEL)
- Clock source setting (CSI_REF) register (CPG_CSI_RCLK_SSEL)

CAUTION

The setting for switching the clock on or off in steps 1 and 4 will be applied to the destination for propagation of the clock for which the setting is to be changed.

Check the clock source setting and change the setting after switching the target clock off.

If the clock source setting is changed without switching the clock off, the stable clock will not be output.

48.7.4 Setting Procedure for Switching the Clock On or Off

Follow the procedure below when making the setting for switching the clock on or off.

* The procedure is described, taking the SDI0 clock (SDI0_ACLK) as an example.

[Setting for Switching the Clock On]

1. Setting for switching the SDI0 clock (SDI0_ACLK) on

Set the following bits of the clock ON/OFF control register 3 (CPG_CLK_ON3).

- Setting for switching the clock on: bit 0 (CLK0_ON) = 1; bit 16 (CLK0_ONWEN) = 1

The clock is output after three cycles of the SDI0 clock (SDI0_ACLK) have elapsed*1 following the setting.

[Setting for Switching the Clock Off]

1. Setting for switching the SDI0 clock (SDI0_ACLK) off

Set the following bits of the clock ON/OFF control register 3 (CPG_CLK_ON3).

- Setting for switching the clock off: bit 0 (CLK0_ON) = 0; bit 16 (CLK0_ONWEN) = 1

The clock is stopped after three cycles of the SDI0 clock (SDI0_ACLK) have elapsed*1 following the setting.

Note 1. Reflection of the setting for switching the clock on or off in the clock pin depends on the clock. See “Clock ON/OFF Control Register 1 to 27 (CPG_CLK_ON 1 to CPG_CLK_ON27)”.

The procedure above is applicable to the following registers.

- Clock ON/OFF control register n (CPG_CLK_ONn) n = 1 to 27

48.7.5 Reset Setting Procedure (TYPE-A Reset)

Follow the procedure below when setting TYPE-A reset control.

The procedure is as follows: Reset → Switching the corresponding clock off → Release from the reset state → Switching the clock on.

* The procedure is described, taking the IIC as an example.

1. Asserting the IIC reset (IIC_GPA_PRESETN, IIC_GRB_PRESETN)

   Set the following bits of the reset control register 6 (CPG_RST6).

   - Bit 8 (UNIT8_RSTB) = 0b; bit 24 (UNIT24_RST WEN) = 1b
   - Bit 9 (UNIT9_RSTB) = 0b; bit 25 (UNIT25_RST WEN) = 1b

2. Setting the IIC clock (IIC_PCLK[1:0]) off

   Set the following bits of the clock ON/OFF control register 9 (CPG_CLK_ON9).

   - Bit 12 (CLK12_ON) =0b; bit 28 (CLK28_ONWEN) = 1b

   Set the following bits of the clock ON/OFF control register 10 (CPG_CLK_ON10).

   - Bit 12 (CLK12_ON) = 0b; bit 28 (CLK28_ONWEN) = 1b

3. De-asserting the IIC reset (IIC_GPA_PRESETN, IIC_GRB_PRESETN)

   Set the following bits of the reset control register 6 (CPG_RST6) while the clock supply is stopped after at least three cycles of the IIC clock have elapsed*[1].

   - Bit 8 (UNIT8_RSTB) =1b; bit 24 (UNIT24_RST WEN) = 1b
   - Bit 9 (UNIT9_RSTB) =1b; bit 25 (UNIT25_RST WEN) = 1b

4. Setting the IIC clock (IIC_PCLK[1:0]) on

   Set the following bits of the clock ON/OFF control register 9 (CPG_CLK_ON9).

   - Bit 12 (CLK12_ON) = 1b; bit 28 (CLK28_ONWEN) = 1b

   Set the following bits of the clock ON/OFF control register 10 (CPG_CLK_ON10).

   - Bit 12 (CLK12_ON) = 1b; bit 28 (CLK28_ONWEN) = 1b

5. Waiting for stabilization

   The unit is accessible following the elapse of a delay in the de-assertion for the target unit described in **Table 48.4-1, List of Reset Signals (1/4)** after up to three cycles of the IIC clock have elapsed*[1].

Note 1. The time until the setting for switching the clock on or off is reflected depends on the clock frequency to be used. When the “De-assertion Delay for Target Unit” column in the **Table 48.4-1, List of Reset Signals (1/4)** has an entry, start access to a given unit after a unit clock cycle delay (the latest clock) + a delay in the de-assertion for the target unit have elapsed.

The procedure above is applicable to the following registers.

- Reset control register n (CPG_RSTn) n = 1 to 15
- Clock ON/OFF control register n (CPG_CLK_ONn) n = 1 to 27

This operating procedure applies to the reset pins indicated as TYPE-A under the “Reset Control Type” column in **Table 48.4-1, List of Reset Signals (1/4)**.

48.7.6 Reset Setting Procedure (TYPE-B Reset)

Follow the procedure below when setting TYPE-B reset control.

The procedure is as follows: Switching the corresponding clock on → Reset → Release from the reset state → Checking.

The procedure is described in the following two patterns, taking resetting of the DMAC as an example.

1) When not switching the clock off during a reset
2) When switching the clock off during a reset

Note that switching the clock on or off during a reset is as desired.

1) When not switching the clock off during a reset

1. Setting for switching the DMAC clock (DMAA_ACLK) on

   Set the following bits of the clock ON/OFF control register 1 (CPG_CLK_ON1).

   - Setting for switching the clock on: Bit 11 (CLK11_ON) = 1; bit 27 (CLK11_ONWEN) = 1

2. Asserting the DMAC reset

   Set the following bits of the reset control register 1 (CPG_RST1) while the clock is supplied after at least three cycles of the DMAC clock have elapsed*[1].

   - Asserting the reset: Bit 7 (UNIT7_RSTB) = 0; bit 23 (UNIT7_RST WEN) = 1

3. De-asserting the DMAC reset

   Set the following bits of the reset control register 1 (CPG_RST1) after at least 729.17 ns +5*DMAA_ACLK (the minimum assertion period in **Table 48.4-1, List of Reset Signals (1/4)**) have elapsed following the reset setting.

   - De-asserting the reset: Bit 7 (UNIT7_RSTB) = 1; bit 23 (UNIT7_RST WEN) = 1

4. Checking the completion of de-assertion of the DMAC reset

   Check that bit 4 (DMAA_RST_MON) of the reset monitor register (CPG_RST_MON) = 0.

Note 1. Reflection of the setting for switching the clock on or off in the clock pin depends on the clock. See the description of “Clock ON/OFF Control Register 1 to 27 (CPG_CLK_ON 1 to CPG_CLK_ON27)”.

2) When switching the clock off during a reset

1. Setting for switching the DMAC clock (DMAA_ACLK) on

Set the following bits of the clock ON/OFF control register 1 (CPG_CLK_ON1).

- Setting for switching the clock on: Bit 11 (CLK11_ON) = 1; bit 27 (CLK11_ONWEN) = 1

2. Asserting the DMAC reset

Set the following bits of the reset control register 1 (CPG_RST1) while the clock is supplied after at least three cycles of the DMAC clock have elapsed*.[1]

- Asserting the reset: Bit 7 (UNIT7_RSTB) = 0; bit 23 (UNIT7_RST WEN) = 1

3. Setting for switching the DMAC clock (DMAA_ACLK) off

Set the following bits of the clock ON/OFF control register 1 (CPG_CLK_ON1) after at least 729.17 ns + 5*DMAA_ACLK (the minimum assertion period in **Table 48.4-1, List of Reset Signals (1/4)**) have elapsed following the reset setting.

- Setting for switching the clock off: Bit 11 (CLK11_ON) = 0; bit 27 (CLK11_ONWEN) = 1

The clock is stopped after three cycles of the DMAC clock have elapsed following the setting.

4. Setting for switching the DMAC clock (DMAA_ACLK) on

Set the following bits of the clock ON/OFF control register 1 (CPG_CLK_ON1).

- Setting for switching the clock on: Bit 11 (CLK11_ON) = 1; bit 27 (CLK11_ONWEN) = 1

The clock is output after three cycles of the DMAC clock have elapsed following the setting.

5. De-asserting the DMAC reset

Set the following bits of the reset control register 1 (CPG_RST1) after the resumption of the clock output.

- De-asserting the reset: Bit 7 (UNIT7_RSTB) = 1; bit 23 (UNIT7_RST WEN) = 1

6. Checking the completion of de-assertion of the DMAC reset

Check that bit 4 (DMAA_RST_MON) of the reset monitor register (CPG_RST_MON) = 0.

Note 1. Reflection of the setting for switching the clock on or off in the clock pin depends on the clock. See the description of “Clock ON/OFF Control Register 1 to 27 (CPG_CLK_ON 1 to CPG_CLK_ON27)”.

The procedure above is applicable to the following registers.

- Reset control register n (CPG_RSTn) n = 1 to 15
- Clock ON/OFF control register n (CPG_CLK_ONn) n = 1 to 27
- Reset monitor register (CPG_RST_MON)

This operating procedure applies to the reset pins indicated as TYPE-B under the “Reset Control Type” column in **Table 48.4-1, List of Reset Signals (1/4)**.

48.8 Usage Notes

48.8.1 Note on Clock Control

Access to the units which have stopped the clock supply is prohibited.

48.8.2 Note on Reset Control

While the ICB is reset, access to the power domain to which that ICB belongs is prohibited.

When the ICB is released from the reset, it is disconnected if its power is off. The ICB must be accessed after checking that it has been released from the disconnection. For details, see the section of PMC.

48.8.3 Notes on External Pin Reset

The external pin reset RSTN, DESRSTN, and DETRSTN should be asserted for no less than 10 μs. When a system reset is initiated by RSTN, DESRSTN, or DETRSTN, the external power switch of PD_MEM is also turned off. Accordingly, secure the period for assertion of RSTN, DESRSTN, and DETRSTN such that the power supply voltage of PD_MEM falls below 0.1 V within 10 μs or to continue until the power supply voltage falls below 0.1 V. In addition, to switch the power supply for PD_MEM on or off by using the external power switch, make sure that the power supply voltage is cut off within the above period or secure enough time for the assertion of RSTN, DESRSTN, and DETRSTN so that the power supply voltage has been cut off.

48.8.4 Restriction on the Dynamic Division Ratio Setting (Changing the Frequency)

Even when the setting has not been changed in the register setting for the dynamic divider, writing 1 to “xx_WEN” allocated in the 16 higher-order bits of the register starts clock switching. Poll the status monitor register (CPG_CLKSTATUS) to check the completion of switching (the clock is stopped once at the time of switching).

48.8.5 Restriction on the Dynamic Division Ratio Setting (the Input Clock)

When changing the frequency for the dynamic divider, make sure that the input clock for the divider is stable.

The corresponding frequency changing registers are listed below.

- DIV NFI (clock division ratio setting (NAND) register (CPG_NFI_DDIV))

48.8.6 Restriction on the Dynamic Switching Selector (Clock Switching)

Even when the setting has not been changed in the register setting for the dynamic selector, writing 1 to “xx_WEN” allocated in the 16 higher-order bits of the register starts clock switching. Poll the status monitor register (CPG_CLKSTATUS) to check the completion of switching (the clock is stopped once at the time of switching).

48.8.7 Restriction on the Dynamic Switching Selector (the Input Clock)

When switching the clock signal, make sure that the input clock signals of the selector are enabled.

Switching the clock signal while either of the input clock signals is stopped is prohibited.

For the selector for which the output from the dynamic divider is a clock source, switching must be done while the clock output from the divider is stable.

The corresponding clock switching registers are listed below.

- SEL E (clock source setting (PLL/48 MHz) register (CPG_CLK48_DSEL))
- SEL NFI (clock source setting (PLL/48 MHz) register (CPG_CLK48_DSEL))

48.8.8 Interval of Access to the Clock ON/OFF Control Registers

Clock on/off switching is reflected after synchronization with each clock following the register setting (synchronization with 48 MHz). Therefore, when clock on/off switching is to be set for the clock signals at the frequency lower than 48 MHz or those set to a frequency lower than 48 MHz, reflection of clock on/off switching takes time longer than cycles for register access.

Table 48.8-1 lists the ON/OFF registers for the clock signals at the frequency lower than 48 MHz (those set to lower frequencies). For access to the same register bits with a lower frequency setting than 48 MHz, insert a wait by software to wait for at least the number of clock cycles listed in this table.

Table 48.8-1 List of ON/OFF Registers for the Clocks Less than 48 MHz

Register			Clock Name	Number of Clock Cycles	Frequency (MHz)	Wait Time (ns)*1
Name	Abbreviation	Bit				
Clock ON/OFF control register 1	CPG_CLK_ON1	5	GIC_CLK	3*GIC_CLK	200/100/50/25/24	125
Clock ON/OFF control register 5	CPG_CLK_ON5	4	CIF_P0_CLK	3*CIF_P0_CLK	—*3	120
		5	CIF_P1_CLK	3*CIF_P1_CLK	—*3	120
Clock ON/OFF control register 6	CPG_CLK_ON6	10	LCI_VCLK	3*LCI_VCLK	—*3	413.79
		11	LCI_LPCLK	3*LCI_LPCLK	—*3	1500
Clock ON/OFF control register 7	CPG_CLK_ON7	14	GFT_MCLK	3*GFT_MCLK	—*3	244.14
Clock ON/OFF control register 8	CPG_CLK_ON8	12	SYC_CNT_CLK	3*SYC_CNT_CLK	24	125
Clock ON/OFF control register 9	CPG_CLK_ON9	11-4	TIM_CLK[7:0]	3*TIM_CLK[7:0]	2	1500
Clock ON/OFF control register 10	CPG_CLK_ON10	11-4	TIM_CLK[15:8]	3*TIM_CLK[15:8]	2	1500
Clock ON/OFF control register 11	CPG_CLK_ON11	11-4	TIM_CLK[23:16]	3*TIM_CLK[23:16]	2	1500
Clock ON/OFF control register 12	CPG_CLK_ON12	11-4	TIM_CLK[31:24]	3*TIM_CLK[31:24]	2	1500
Clock ON/OFF control register 15	CPG_CLK_ON15	13-8	CSI_CLK[5:0]	3*CSI_CLK[5:0]	48/24	125
		6-5	URT_CLK[1:0]	3*URT_CLK[1:0]	max108/48	62.5
Clock ON/OFF control register 16	CPG_CLK_ON16	0	ICB_GIC_CLK	2*ICB_GIC_CLK(1) + 4*ICB_ACLK1(2)	(1) 200/100/50/25/24 (2) 400/200/100/50/48*2	166.67
		15	ICB_SYC_CNT_CLK	3*ICB_SYC_CNT_CLK	24	125
Clock ON/OFF control register 19	CPG_CLK_ON19	0	CA53_CLK	10*CA53_CLK	996/498/332/249/166/83/41.5	240.96
Clock ON/OFF control register 18	CPG_CLK_ON18	13	ICB_VCD_PCLK4	3*ICB_VCD_PCLK4	—*3	120
Clock ON/OFF control register 25	CPG_CLK_ON25	4	FCD_CLK	3*FCD_CLK	—*3	120
Clock ON/OFF control register 26	CPG_CLK_ON26	8	JPG0_CLK	3*JPG0_CLK	—*3	120
		5	VCD_PCLK	2*VCD_PCLK(1) +4*VCD_ACLK(2)	—*3	160

Note 1. The maximum time until a change to the clock frequency is reflected (the number of clock cycles × the minimum frequency period).
A change to the set frequency is completed after at least the time listed in the “Wait Time” column has elapsed, regardless of the changed value of the register setting.

Note 2. (1) and (2) are interlinked at the frequencies divided by a slash (/).

Note 3. For more information, contact a Renesas Electronics sales representative.

48.8.9 Restriction on the CSI Clocks

A restriction applies to the relation between the two CSI clocks (PCLK, CSI_CLK) and the CSI_CLK frequency must be set to no greater than half the PCLK frequency.

The variable bus clock SPCLK (100/50/48 MHz) is connected to PCLK of the CSI. CSI_CLK connects the clock switched to 48 or 24 MHz. Therefore, when using SPCLK at 50 MHz or 48 MHz, be sure to set all CSI_CLK from CSI0 to 5 to 24 MHz.

The related registers are listed below.

- System division ratio setting register (CPG_SYS_DDIV)
  DIV E (SPCLK 100/50 MHz switching) (bit 8)
- Clock source setting (PLL/48MHz) register (CPG_CLK48_DSEL)
  SEL E (SPCLK PLL/48 MHz switching) (bit 2)
- Clock source setting (CSI_REF) register (CPG_CSI_RCLK_SSEL)
  SEL CSI5-0 (CSI_CLK 48/24 MHz switching) (bits 5 to 0)
- Clock ON/OFF control register 15 (CPG_CLK_ON15)
  CSI_CLK ON/OFF setting (bits 13 to 8)

48.8.10 Register Control for CPG_CLK_ON16 and CPG_CLK_ON17

Access to the units subject to a reset is prohibited during the “Minimum Assertion Period” or the period of “De-assertion Delay for Target Unit” listed in **Table 48.4-1, List of Reset Signals (1/4)**.

48.8.11 Register Control of CPG_CLK_ON16 and CPG_CLK_ON17

Since stopping the ICB clock for the PD1_AWO power domain causes the system to be deadlocked, the target bits of the CPG_CLK_ON16 and CPG_CLK_ON17 registers must always be left as 1b.

- Setting for switching the ICB_CLK48 clock off
- Setting for asserting the ICB_PD_AWO_RST_N reset (setting CPG_RST7.UNIT0_RSTB to 0)

If the above settings have been made, restore the values by an external reset.

- CPG: CPG_CLK_ON16 register

Bit 0:	ICB_ACLK1, ICB_GIC_CLK;	Bit 2:	ICB_MPCLK1
Bit 3:	ICB_SPCLK1;	Bit 4:	ICB_CLK48
Bit 10:	ICB_CST_ATB_SB_CLK;	Bit 11:	ICB_CST_CS_CLK
Bit 12:	ICB_CLK100_1;	Bit 13:	ICB_ETH0_CLK_AXI
Bit 14:	ICB_DCI_CLKAXI;	Bit 15:	ICB_SYC_CNT_CLK

- CPG: CPG_CLK_ON17 register

  Bit 0: ICB_DRPA_ACLK

48.8.12 Restriction on Bit 5 (CLK5_ON) of the CPG_CLK_ON19 Register

This register is a clock control register for access to the APB registers of the soft macro within CA53 (CA53_SM). Since the clock supply is required when CA53 is operating, independently of the operating mode, debug mode or normal mode, bit 5 (CLK5_ON) of the CPG_CLK_ON19 register must always be left as 1b.

48.8.13 CPG_CLK48_DSEL Clock Swiching Setting

Switch SEL B, SEL D, SEL E, SELG, and SEL NFI simultaneously.

Operation when they are switched individually is not guaranteed.

(The clock source setting (PLL/48MHz) register (CPG_CLK48_DSEL) bits 0 to 5)

48.8.14 Reset Range Selection Setting by a WDT Timeout

Though the reset range by a WDT timeout can be set as system reset 2 or a CPU core warm reset by using the register (CPG_WDT_RST), a warm reset must be applied by following the procedure such as completion of the bus transaction. A reset by a WDT timeout is generated at an unexpected time, i.e., when software runs out of control.

Therefore, when a WDT timeout reset occurs without interlinked operation with software, a warm boot may not be done correctly, so the following settings are prohibited.

- WDT CA53 warm reset (core 0) setting (setting CPG_WDT_RST.WDTRST0 to 1)
- WDT CA53 warm reset (core 1) setting (setting CPG_WDT_RST.WDTRST1 to 1)

48.8.15 Restrictions on the CPG Reset Control Registers

Table 48.8-2 lists the restrictions on reset control by software. Setting the corresponding bits of the reset control registers to 0b is prohibited (resetting by software is prohibited).

Table 48.8-2 Restrictions on the CPG Reset Control Registers

Corresponding Bit of the Reset Control Register for which the Setting 0b is Prohibited	Register Function	Supplementary Note
CPG_RST1 register		
Bit 14 (UNIT14_RSTB)	PMC_RESET_N (TYPE-B) reset pin control	—
Bit 1 (UNIT1_RSTB)	SYS_RST_N (TYPE-A) reset pin control	
CPG_RST2 register		
Bit 10 (UNIT10_RSTB)	CST_ATB_SB_RESETN reset pin control	In debug mode, setting the corresponding bits of the reset control registers in the CPG to 0b is prohibited.
Bit 8 (UNIT8_RSTB)	CST_APB_CA53_RESETN reset pin control	
Bit 7 (UNIT7_RSTB)	CST_TS_SB_RESETN reset pin control	
Bit 6 (UNIT6_RSTB)	CST_AHB_RESETN reset pin control	
Bit 5 (UNIT5_RSTB)	CST_SB_RESETN reset pin control	
Bit 4 (UNIT4_RSTB)	CST_TRESETN reset pin control	
Bit 3 (UNIT3_RSTB)	CST_TS_RESETN reset pin control	
Bit 2 (UNIT2_RSTB)	CST_CS_RESETN reset pin control	
Bit 1 (UNIT1_RSTB)	CST_NPOTRST and CST_NTRST reset pin control	
Bit 0 (UNIT0_RSTB)	CST_NTRST reset pin control	
CPG_RST7 register		
Bit 0 (UNIT0_RSTB)	ICB_PD_AWO_RST_N reset pin control	

48.8.16 Restriction on the UART Clock Frequency

Since a 16x baud rate clock is used for 1-bit sampling, the UART serial clock (URT_CLK[1:0]) must be set to at least 16 times the data transfer rate (baud rate) to be used (up to 108 MHz). For example, in a use case where the data transfer rate of the UART is 5 Mbps, set URT_CLK[1:0] to at least 80 MHz (up to 108 MHz).

48.8.17 Restriction on the Frqeuencies of the General-Purpose Clocks (GMCLK0, GMCLK1)

The clock frequencies of GMCLK0 and GMCLK1 must be set to no greater than 100 MHz.

48.8.18 Point for Caution when Changing the Clock Setting

Operation when the clock setting is changed while the unit is operating cannot be guaranteed.

* The CA53 clock (CA53_CLK) is excluded.

Section 49 Interconnect Bus (ICB)

This section describes the functions of the interconnect bus (ICB).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

49.1 Functional Overview

Table 49.1-1 is a list of the ICB functions.

Table 49.1-1 List of Functions

Function	Overview
Access between master and slave	• Selecting an access path • Transaction conversion
Scheduler	• Arbitration
QoS	• Priority control
Bus separation	• Detection and notification of the bus isolation status of the target power domain
Observability	
Scheduler statistics measurement	• Measures the amount of data transferred and the number of transactions that pass through the scheduler.
StatAlarm detection	• Scheduler match the conditions.
TraceAlarm detection	• Detecting that a specific transaction has passed through the scheduler
ErrorLogging detection	• Detecting error responses to the master port
ATB I/F output	• The information on StatAlarm and TraceAlarm detection is output via ATB I/F.
Interrupt	• The interrupt notification of StatAlarm, TraceAlarm, and ErrorLogging detections

Table 49.1-2 List of Abbreviations

Abbreviation	Description
NIU	Network interface unit
INIU	Initiator NIU that interfaces with the master unit
TNIU	Target NIU that interfaces with the slave unit
NSP	Network socket protocol
NoC	Network on-chip
NTTP	Noc transaction and transport protocol

49.2 Internal Configuration

Figure 49.2-1 shows the internal configuration of the ICB unit, which consists of the following elements

- ICB_MAIN, the main body of NoC, and ICB_REG for low-speed register access
- Initiator NIU (INIU) that interfaces with the master unit
- Target NIU (TNIU) that interfaces with the slave unit
- LPDDR4 scheduler
- Switch and Link of connection elements between INIU and TNIU
- Observability to observe error responses and statistical information
- The elements in this unit are located in the power domain[*1] that is related to the ICB_PD domain.

Note 1. Power domain: PD_AWO, PD_MEM, PD_VIDEO0, PD_VIDEO1, and PD_RFX

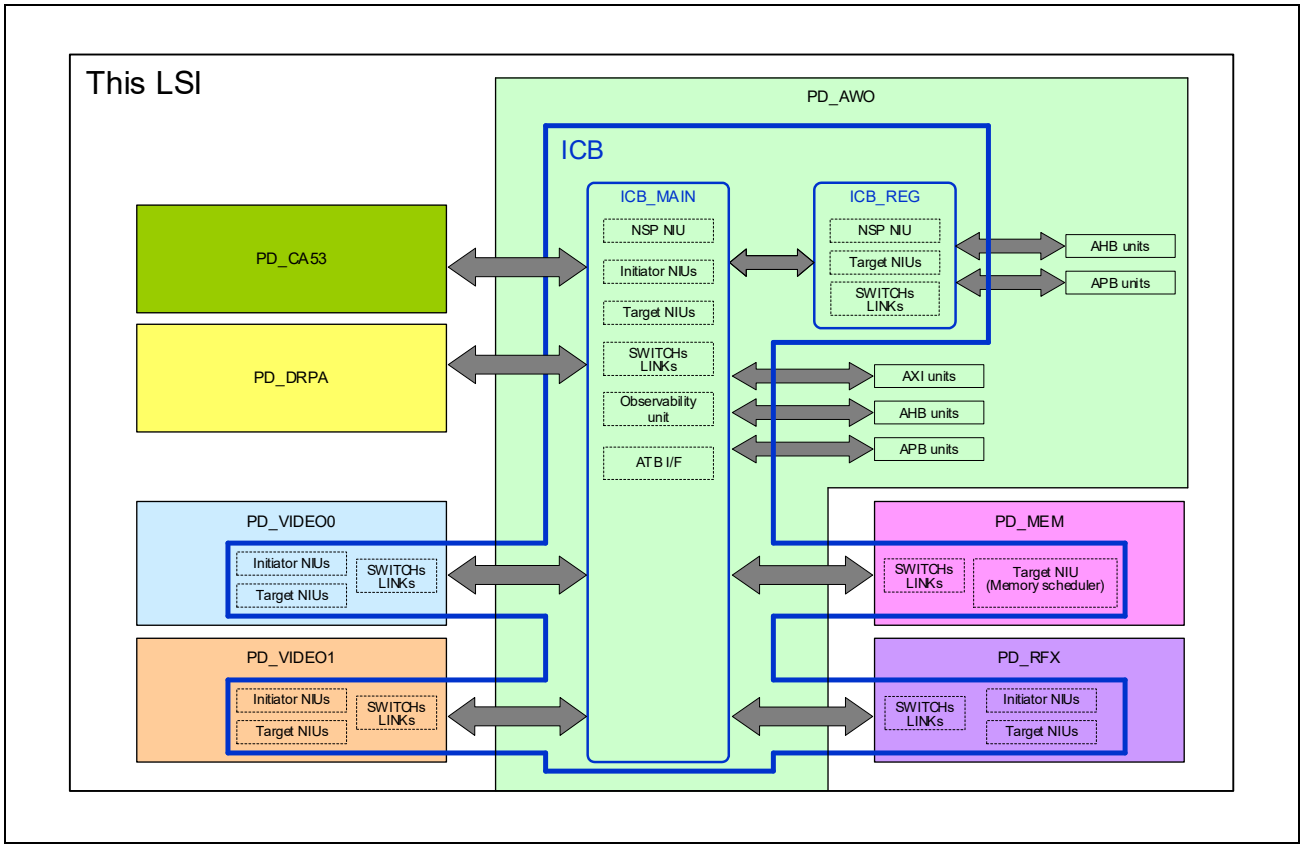


Figure 49.2-1 Internal Configuration

Section 50 External Power Sequence Controller (PWC)

This section describes the functions of the external power sequence controller (PWC).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

50.1 Functional Overview

The PWC is a controller for external power supplies (regulators and power switches).

- Generating an external power supply on/off sequence
- Generating an on/off signal for the LPDDR4 core power supply (LPVDD)
- Generating control signals for external I/O power supplies of the SD host interfaces
- Processing of key input signals (key inputs are used as triggers for the power-on sequence)

50.2 Connection Configuration

Figure 50.2-1 is a connection configuration of the PWC.

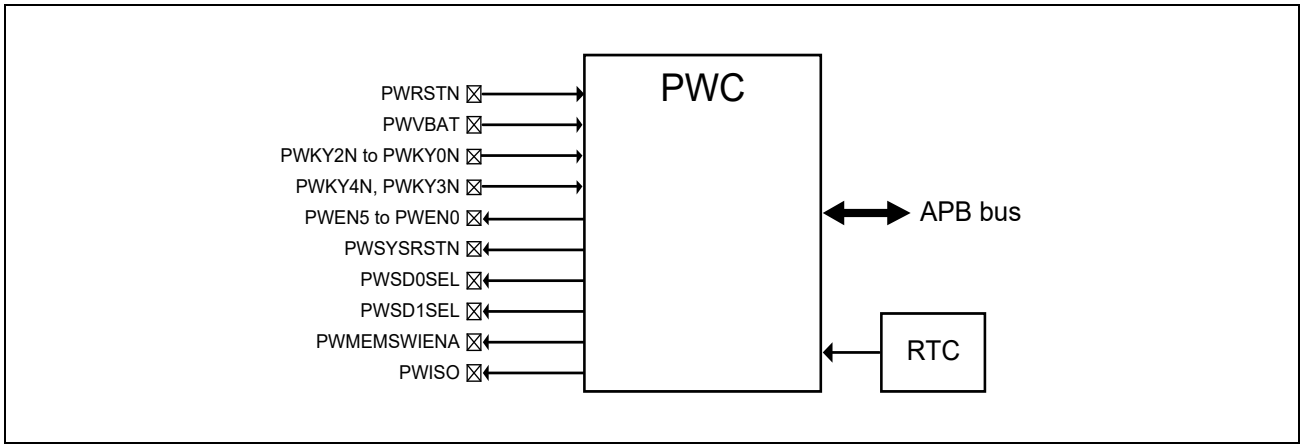


Figure 50.2-1 Connection Configuration of the PWC

50.3 Pin Functions

Table 50.3-1 lists the external pins of the PWC.

Table 50.3-1 List of External Pins

Pin Name	I/O	Function
PWRSTN	Input	RTC reset input (active low)
PWVBAT	Input	Battery voltage detection
PWKY2N to PWKY0N	Input	Input power keys 2 to 0 (active low)
PWKY4N, PWKY3N	Input	Input power keys 4, 3
PWEN5 to PWEN0	Output	Power enable 5 to 0 (active high)
PWSYSRSTN	Output	System reset output. Connected to the RSTN pin to use the power control function of PWC.
PWSD0SEL	Output	PWC SDI0 interface power supply selection
PWSD1SEL	Output	PWC SDI1 interface power supply selection
PWMEMSWIENA	Output	Enable signal output pin for controlling the LPVDD power supply on/off
PWISO	Output	RTC separation output pin. Open drain output. Connected to the RTISO pin and pulled up (with 10kΩ to 100kΩ) to a 1.5-V power supply.*1

Note 1. The PWISO and RTISO pins are connected to this LSI, and these nodes should be pulled up with a 10-kΩ to 100-kΩ resistor. The schematic diagram is shown in **Section 2, Pin**. For details, refer to **Section 2**.

50.4 Register Description

For more information, contact a Renesas Electronics sales representative.

50.5 Functional Description

- External power supply on/off sequence generation

  The PWC outputs enable signals (PWENn (n: 0 to 5)) to control the various external power supplies (regulators and power switches) required by this LSI chip and a system reset signal (PWSYSRSTN) for this chip.

Figure 50.5-1 shows an example of a system configuration for external power supplies.

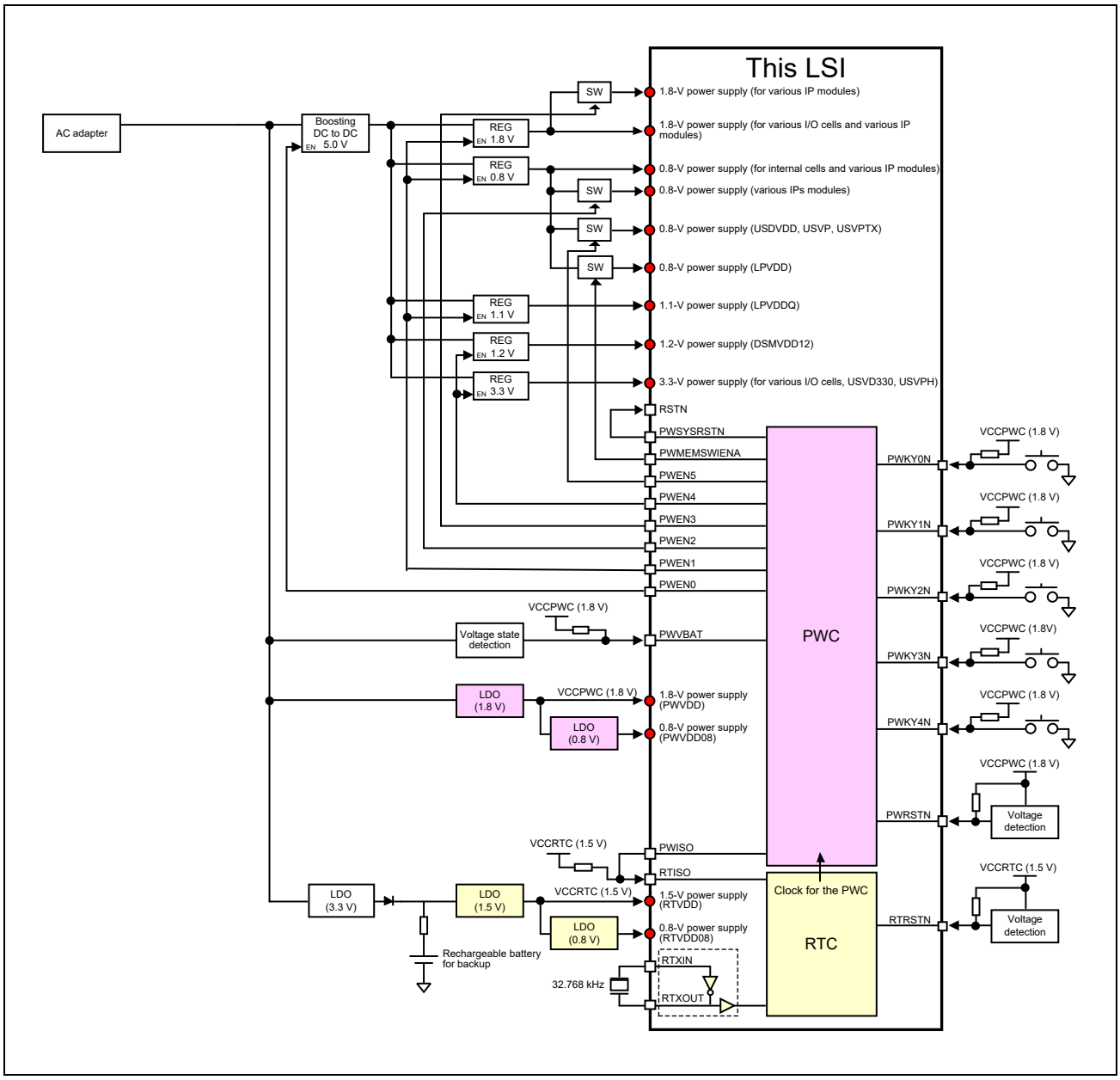


Figure 50.5-1 Example System Configuration for External Power Supplies

Note: This figure is an example and does not guarantee the operation of the external circuitry it shows. Follow the procedures described in **Section 54, Electrical Characteristics**.

– PWENn (n: 0 to 5) output pins:
Being connected to the control pins of the external power supplies (regulators), these output pins control the rising and falling of the various power supply voltages.

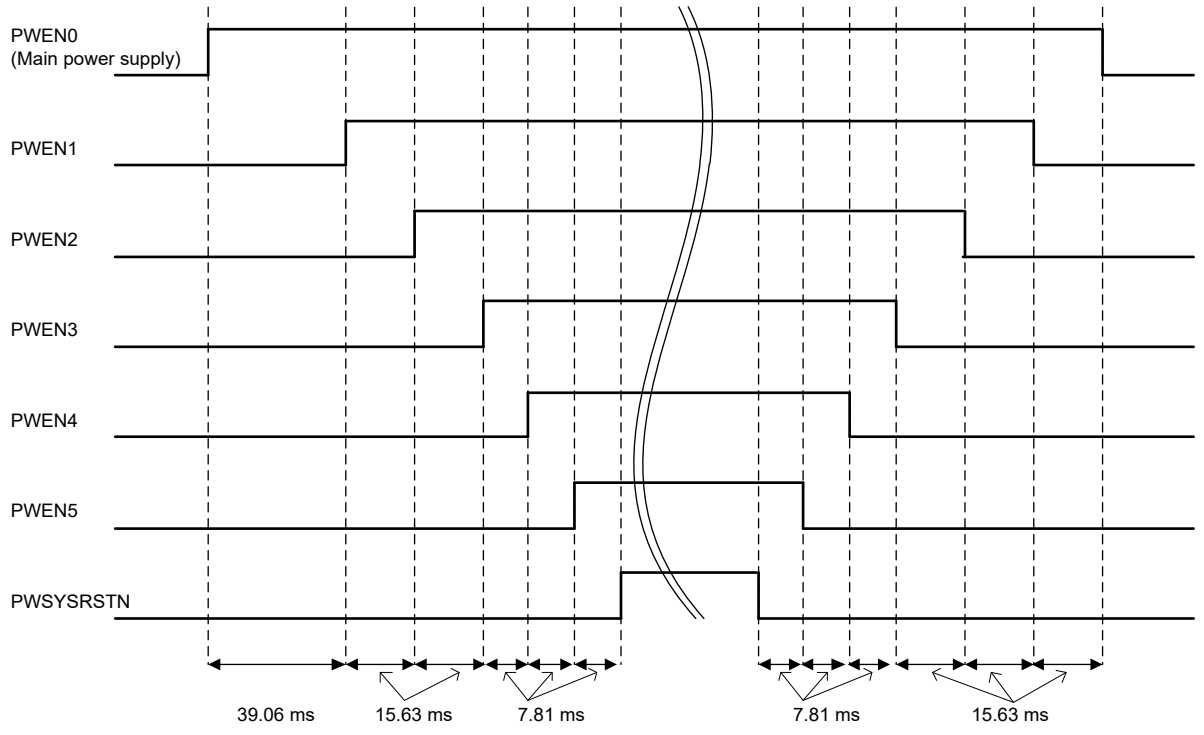
Table 50.5-1 Functions of PWENn (n: 0 to 5) Pins

Output Pin	Function
PWEN0	Used to control the on/off state of the main external power supply (regulator).
PWEN1	Used to control the on/off status of the external power supply (regulator) for timing 1*1
PWEN2	Used to control the on/off status of the external power supply (regulator) for timing 2*1
PWEN3	Used to control the on/off status of the external power supply (regulator) for timing 3*1
PWEN4	Used to control the on/off status of the external power supply (regulator) for timing 4*1
PWEN5	Used to control the on/off status of the external power supply (regulator) for timing 5*1

Note 1. See the description in **Section 54, Electrical Characteristics**.

– PWSYSRSTN output pin:
Connecting this output to the system reset control pin (the RSTN input pin) of this LSI chip allows reset control of the chip.

Figure 50.5-2 shows the timing of the outputs from the PWENn (n: 0 to 5) and PWSYSRSTN pins.



Note: Placing the low level on the PWRSTN pin during the operations turns the voltages on all of the pins shown to the low level at the same time, causing non-compliance with the correct power-off sequence in this figure.

Figure 50.5-2 Timing of the Outputs from the PWENn (n: 0 to 5) and PWSYSRSTN Pins

Control of the external power supplies by an external PMIC (power management IC) or similar without using the PWENn (n: 0 to 5) outputs of the PWC is also possible. For details on the specifications for the relative timing of rising and falling voltages on the power supply pins of this LSI chip, see the description in **Section 54, Electrical Characteristics**.

- Generating an on/off signal for the LPDDR4 core power supply (LPVDD)
  - PWMEMSWIENA output pin: Enable signal output pin for controlling the LPVDD power supply on/off

  LPVDD is the power supply for the on-chip LPDDR memory controller unit (power supply domain PD_MEM (0.8-V power supply system)), and turning on/off the LPVDD power supply is individually controlled by the System FW of this LSI after booting.

  Supply 0.8-V power to LPVDD through the power switch. Connect the PWMEMSWIENA pin to the enable pin of this power switch.

- Generating control signals for external I/O power supplies of the SD host interfaces

  Control signals PWSDnSEL (n: 0, 1) are output for switching of the IO power supply voltages (between 1.8 V and 3.3 V).

  With a multi-output regulator for these IO power supplies, the IO voltages can be switched from 3.3 V to 1.8 V or from 1.8 V to 3.3 V by using signals on the PWSDnSEL (n: 0, 1) pins.
  - PWSD0SEL output pin: For switching the IO power supply voltage of SD host interface SDI0
  - PWSD1SEL output pin: For switching the IO power supply voltage of SD host interface SDI1

- Processing of key input signals

  Changes in the input levels on the PWKYnN (n: 0 to 4) pins can be detected and used as the sources of triggers for the power-on sequence of the PWC from a power-off state.

Section 51 Internal Power Domain Controller (PMC)

This section describes the functions of the internal power domain controller (PMC).

This manual is a simplified version. For more information, contact a Renesas Electronics sales representative.

51.1 Functional Overview

51.1.1 List of Functions

Table 51.1-1 is a list of the functions of the PMC.

Table 51.1-1 List of Functions

Function (Major Category)	Functions	Description
Internal power domain on/fff control*1	Internal power domain on/fff control	Controls the on/off state of the internal power domain. • Controls the SoC external power switch for PD_MEM • Controls the SoC internal power switches for PD_VIDEO0, PD_VIDEO1, PD_RFX, PD_DRPA, and PD_CA53.
	Isolation cell control*2	This function fixes the level of the signal output from the power-off domain.
	Bus idle request control	Controls the separation/connection of the buses of the units in PD_MEM, PD_VIDEO0, PD_VIDEO1, and PD_RFX from ICB.
Interrupt control	Interrupt output control	• Interrupt signal output (Internal power domain on/off control completed, bus separation completed) • Clearing of interrupt sources • Mask control of interrupt pins
CPU standby control	CPU standby detection	Allows the CPU to execute a WFI instruction to detect its transition to the standby state and indicate this in response to an interrupt (SPI).
	CPU RAM standby control	Controls the standby state of the SRAM (cache) after a transition of the CPU of CA53 to the standby state (retention/shutdown).

Note 1. The software controls a series of processes from controlling the internal power domain on/off to controlling the isolation cells.

Note 2. The isolation cell prevents undefined propagation and through-current from power-off units to power-on units.

51.1.2 Internal Power Domain

The internal power domain of this LSI is divided into seven different power domain areas, including the always-on domain (PD_AWO: Power Domain Always On). **Figure 51.1-1** shows te power domain of this LSI. This diagram is a schematic for explanation purposes only. The main function of the PMC is to power on and off these domains. Among these domains, PD_CA53, PD_VIDEO0, PD_VIDEO1, PD_RFX, and PD_DRPA are used in the ISP support package. Therefore, rewriting the related registers is prohibited.

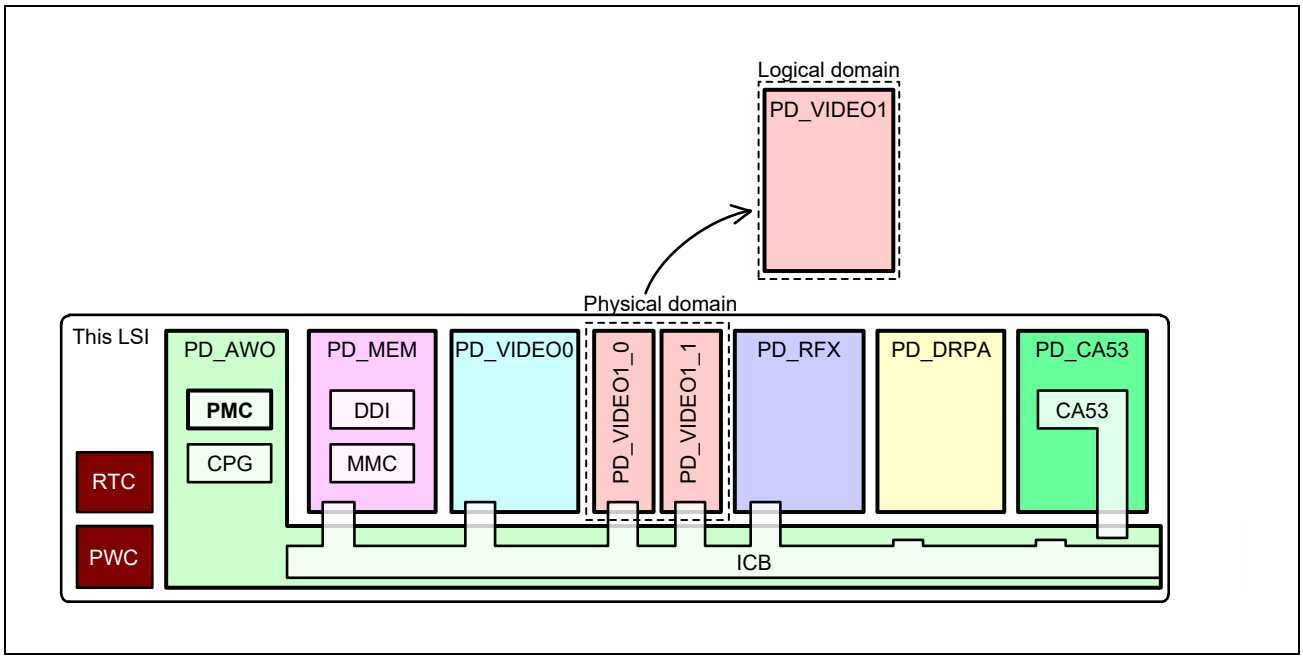


Figure 51.1-1 Power Domains to be Controlled

There are six power domains that the PMC can power on/off: PD_MEM, PD_VIDEO0, PD_VIDEO1, PD_RFX, PD_DRPA, and PD_CA53, except for PD_AWO. PD_VIDEO1 is physically distributed in two areas (PD_VIDEO1_0 and PD_VIDEO1_1). PD_VIDEO1_0 and PD_VIDEO1_1 cannot be individually controlled for power domain on/off.

In addition to the above, there are two other power domains, RTC 0.8V and PWC 0.8V. PD_AWO's power domain on/off is controlled by PWC, not by PMC.

Table 51.1-2 shows the on/off status of the respective power domains after the system reset is released.

Table 51.1-2 Power Domain and Initial State

	PD_AWO	PD_MEM	PD_VIDEO0	PD_VIDEO1	PD_RFX	PD_DRPA	PD_CA53
Initial state	Power on	Power off	Power off	Power off	Power off	Power off	Power on

Note: The table shows the initial value settings of the PMC control registers.

51.2 Register Description

For details on the base address of the register (<PMC_S0_base>), see the Address Map section.

51.2.1 List of Registers

Table 51.2-1 is a list of registers. The registers should be accessed in 32-bit units.

Table 51.2-1 List of Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
000h	Power Supply Enable Register	PMC_SPLY_ENA	0000_0000h	32
004h	Power Domain Status Monitor Register	PMC_MAIN_STS	0000_0080h	32
008h	Reserved	—	—	—
00Ch	Reserved	—	—	—
010h	Reserved	—	—	—
014h	PD_MEM Power-on/off Time Setting Register	PMC_PD_MEM_TIM	0BB7_0BB7h	32
018h	Reserved	—	—	—
01Ch	PD_MEM Isolation Enable Register	PMC_PD_MEM_ISOEN	0000_8001h	32
020h	PD_VIDEO0 Isolation Enable Register	PMC_PD_VIDEO0_ISOEN	0000_8001h	32
024h	PD_VIDEO1 Isolation Enable Register	PMC_PD_VIDEO1_ISOEN	0000_8001h	32
028h	PD_RFX Isolation Enable Register	PMC_PD_RFX_ISOEN	0000_8001h	32
02Ch	PD_DRPA Isolation Enable Register	PMC_PD_DRPA_ISOEN	0000_8001h	32
030h	Reserved	—	—	—
034h	PD_CA53 Isolation Enable Register	PMC_PD_CA53_ISOEN	0000_8000h	32
038h	Idle Request Register	PMC_IDLE_REQ	0000_001Eh	32
03Ch	Idle Request Status Register	PMC_IDLE_STS	0000_001Eh	32
040h	CPU Standby Monitor Register	PMC_CPU_MON	0000_0000h	32
044h	Interrupt Status Register	PMC_INT_STS	0000_0000h	32
048h	Interrupt Clear Register	PMC_INT_CLR	0000_0000h	32
04Ch	Interrupt Mask Register	PMC_INT_MSK	0000_003Fh	32
050h to 08Ch	Reserved	—	—	—
090h	CA53 SRAM SDM Configuration Register	PMC_CA53_SDM_CFG	0000_0000h	32
094h	CA53 SRAM RS Control Register	PMC_CA53_RS_CTL	0000_0000h	32
098h	CA53 SRAM RS Status Register	PMC_CA53_RS_STS	0000_0000h	32
Reserved				
09Ch to FFCh	Reserved	—	—	—

51.2.2 Register Descriptions

The function description of each register is given below.

51.2.2.1 Power Supply Enable Register (PMC_SPLY_ENA)

PMC_SPLY_ENA controls the power on/off process for the specified power domain.

Set this register after confirming that PD_BUSY of the PMC_MAIN_STS register is 0. When this register is read, the last written value can be read.

Note: After starting the power on/off process, an interrupt occurs when the power switch is turned on/off. Isolation processing is not performed.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0000h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	ON	—	PD_NUM		
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	R	RW	RW	RW

Table 51.2-2 PMC_SPLY_ENA Register Contents

Bit Position	Bit Name	Description
31 to 5	—	Reserved. These bits are read as 0b.
4	ON	Writing to this register starts the process of turning on/off the power domain. This bit selects whether the power is turned on or off. When read, the last written value is returned. 0b: Power off 1b: Power on
3	—	Reserved. This bit is read as 0b.
2 to 0	PD_NUM	These bits specify the power domain to be turned on/off. When read, the last written value is returned. 000b: There is no processing target. The power on/off process does not start. . 001b: The processing target is PD_MEM. 010b: The processing target is PD_VIDEO0 011b: The processing target is PD_VIDEO1 100b: The processing target is PD_RFX 101b: The processing target is PD_DRPA 110b: Setting prohibited 111b: The processing target is PD_CA53

51.2.2.2 Power Domain Status Monitor Register (PMC_MAIN_STS)

PMC_MAIN_STS indicates the power on/off state of each power domain.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0004h

Initial Value: 0000_0080h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD_BUSY	—	—	—	—	—	—	—	PD_CA53_ON	—	PD_DRPA_ON	PD_RFX_ON	PD_VIDEO1_ON	PD_VIDEO0_ON	PD_MEM_ON	—
Initial Value	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 51.2-3 PMC_MAIN_STS Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15	PD_BUSY	This bit indicates the status of power-on or power-off sequence processing. When processing is written to the PMC_SPLY_ENA register, it becomes 1b. Then, it returns to 0b after processing is completed. 0b: Either the power on or power off sequence is stopped. Power on/off processing requests become possible. 1b: The power on or power off sequence is in progress. Other power on/off processing requests are not accepted.
14 to 8	—	Reserved. These bits are read as 0b.
7	PD_CA53_ON*1	This bit returns the power switch status of power domain PD_CA53. 0b: Power off 1b: Power on
6	—	Reserved. When read, the value read is undefined.
5	PD_DRPA_ON*1	This bit returns the power switch status of power domain PD_DRPA 0b: Power off 1b: Power on
4	PD_RFX_ON*1	This bit returns the power switch status of power domain PD_RFX. 0b: Power off 1b: Power on
3	PD_VIDEO1_ON*1	This bit returns the power switch status of power domain PD_VIDEO1. 0b: Power off 1b: Power on
2	PD_VIDEO0_ON*1	This bit returns the power switch status of power domain PD_VIDEO0 0b: Power off 1b: Power on
1	PD_MEM_ON*1	This bit returns the power switch status of power domain PD_MEM. 0b: Power off 1b: Power on
0	—	Reserved. This bit is read as 0b.

Note 1. The value is confirmed when PD_BUSY = 0. The value is indeterminate while PD_BUSY = 1.

51.2.2.3 PD_MEM Power-on/off Time Setting Register (PMC_PD_MEM_TIM)

PMC_PD_MEM_TIM sets the time required for the external power switch response of power domain PD_MEM.

The maximum time that can be set to the PD_ON_TIM and PD_OFF_TIM bits is 21.8453 msec.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0014h

Initial Value: 0BB7_0BB7h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PD_OFF_TIM															
Initial Value	0	0	0	0	1	0	1	1	1	0	1	1	0	1	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD_ON_TIM															
Initial Value	0	0	0	0	1	0	1	1	1	0	1	1	0	1	1	1
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 51.2-4 PMC_PD_MEM_TIM Register Contents

Bit Position	Bit Name	Description
31 to 16	PD_OFF_TIM	These bits set the time required to power off the power domain PD_MEM in units of 16 PCLK (48 MHz) clocks. The time setting is (PD_OFF_TIM setting value + 1) × 16 PCLK cycles. (Ex) 0000h: 1 × 16 PCLK period (333.3 nsec) 0001h: 2 × 16 PCLK period (666.7 nsec) 0002h: 3 × 16 PCLK period (1 µsec) 001Dh: 30 × 16 PCLK period (10 µsec) 012Bh: 300 × 16 PCLK period (100 µsec) 0BB7h: 3,000 × 16 PCLK period (1 msec) 752Fh: 30,000 × 16 PCLK period (10 msec) FFFEh: 65,535 × 16 PCLK period (21.8450 msec) FFFFh: 65,536 × 16 PCLK period (21.8453 msec)
15 to 0	PD_ON_TIM	These bits set the time required to power on the power domain PD_MEM in units of 16 PCLK (48 MHz) clocks. It means (PD_ON_TIM + 1) × 16 clock time. (Ex) 0000h: 1 × 16 PCLK period (333.3 nsec) 0001h: 2 × 16 PCLK period (666.7 nsec) 0002h: 3 × 16 PCLK period (1 µsec) 001Dh: 30 × 16 PCLK period (10 µsec) 012Bh: 300 × 16 PCLK period (100 µsec) 0BB7h: 3,000 × 16 PCLK period (1 msec) 752Fh: 30,000 × 16 PCLK period (10 msec) FFFEh: 65,535 × 16 PCLK period (21.8450 msec) FFFFh: 65,536 × 16 PCLK period (21.8453 msec)

51.2.2.4 PD_MEM Isolation Enable Register (PMC_PD_MEM_ISOEN)

The isolation cell prevents the undefined value from propagating when the power domain PD_MEM is turned off.

PMC_PD_MEM_ISOEN sets the level of the isolation enable signal. After writing to the PD_ISOEN bit, the time to stabilize the internal state is required. When the PD_ISO_DONE bit is '1b', the internal state is stable.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 001Ch

Initial Value: 0000_8001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD_ISO_DONE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PD_ISO_EN
Initial Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 51.2-5 PMC_PD_MEM_ISOEN Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15	PD_ISO_DONE	This bit indicates the isolation status inside the SoC. 0b: The internal state of the SoC is unstable during the isolation process. 1b: SoC internal isolation is stable.
14 to 1	—	Reserved. These bits are read as 0b.
0	PD_ISO_EN	This bit sets the power domain PD_MEM isolation. 0b: Release the fixed output signal (isolation). 1b: Fix the output signal (isolation).

51.2.2.5 PD_VIDEO0 Isolation Enable Register (PMC_PD_VIDEO0_ISOEN)

The isolation cell prevents the undefined value from propagating when the power domain PD_VIDEO0 is turned off.

PMC_PD_VIDEO0_ISOEN sets the level of the isolation enable signal. After writing to the PD_ISOEN bit, the time to stabilize the internal state is required. When the PD_ISO_DONE bit is ‘1b’, the internal state is stable.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0020h

Initial Value: 0000_8001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD_ISO_DONE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PD_ISO_EN
Initial Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 51.2-6 PMC_PD_VIDEO0_ISOEN Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15	PD_ISO_DONE	This bit indicates the isolation status inside the SoC. 0b: The internal state of the SoC is unstable during the isolation process. 1b: SoC internal isolation is stable.
14 to 1	—	Reserved. These bits are read as 0b.
0	PD_ISO_EN	This bit sets the power domain PD_VIDEO0 isolation. 0b: Release the fixed output signal (isolation). 1b: Fix the output signal (isolation).

51.2.2.6 PD_VIDEO1 Isolation Enable Register (PMC_PD_VIDEO1_ISOEN)

The isolation cell prevents the undefined value from propagating when the power domain PD_VIDEO1 is turned off.

PMC_PD_VIDEO1_ISOEN sets the level of the isolation enable signal. After writing to the PD_ISOEN bit, the time to stabilize the internal state is required. When the PD_ISO_DONE bit is ‘1b’, the internal state is stable.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0024h

Initial Value: 0000_8001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD_ISO_DONE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PD_ISO_EN
Initial Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 51.2-7 PMC_PD_VIDEO1_ISOEN Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15	PD_ISO_DONE	This bit indicates the isolation status inside the SoC. 0b: The internal state of the SoC is unstable during the isolation process. 1b: SoC internal isolation is stable.
14 to 1	—	Reserved. These bits are read as 0b.
0	PD_ISO_EN	This bit sets the power domain PD_VIDEO1 isolation. 0b: Release the fixed output signal (isolation). 1b: Fix the output signal (isolation).

51.2.2.7 PD_RFX Isolation Enable Register (PMC_PD_RFX_ISOEN)

The isolation cell prevents the undefined value from propagating when the power domain PD_RFX is turned off.

PMC_PD_RFX_ISOEN sets the level of the isolation enable signal. After writing to the PD_ISOEN bit, the time to stabilize the internal state is required. When the PD_ISO_DONE bit is '1b', the internal state is stable.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0028h

Initial Value: 0000_8001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD_ISO_DONE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PD_ISO_EN
Initial Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 51.2-8 PMC_PD_RFX_ISOEN Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15	PD_ISO_DONE	This bit indicates the isolation status inside the SoC. 0b: The internal state of the SoC is unstable during the isolation process. 1b: SoC internal isolation is stable.
14 to 1	—	Reserved. These bits are read as 0b.
0	PD_ISO_EN	This bit sets the power domain PD_RFX isolation. 0b: Release the fixed output signal (isolation). 1b: Fix the output signal (isolation).

51.2.2.8 PD_DRPA Isolation Enable Register (PMC_PD_DRPA_ISOEN)

The isolation cell prevents the undefined value from propagating when the power domain PD_DRPA is turned off.

PMC_PD_DRPA_ISOEN sets the level of the isolation enable signal. After writing to the PD_ISOEN bit, the time to stabilize the internal state is required. When the PD_ISO_DONE bit is ‘1b’, the internal state is stable.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 002Ch

Initial Value: 0000_8001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD_ISO_DONE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PD_ISO_EN
Initial Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 51.2-9 PMC_PD_DRPA_ISOEN Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15	PD_ISO_DONE	This bit indicates the isolation status inside the SoC. 0b: The internal state of the SoC is unstable during the isolation process. 1b: SoC internal isolation is stable.
14 to 1	—	Reserved. These bits are read as 0b.
0	PD_ISO_EN	This bit sets the power domain PD_DRPA isolation. 0b: Release the fixed output signal (isolation). 1b: Fix the output signal (isolation).

51.2.2.9 PD_CA53 Isolation Enable Register (PMC_PD_CA53_ISOEN)

The isolation cell prevents the undefined value from propagating when the power domain PD_DRPA is turned off.

PMC_PD_DRPA_ISOEN sets the level of the isolation enable signal. After writing to the PD_ISOEN bit, the time to stabilize the internal state is required. When the PD_ISO_DONE bit is '1b', the internal state is stable.

Note: The initial value of PD_ISO_EN is 0b, but the isolation is enabled immediately after the system reset is released. Isolation is released immediately before CA53 boots.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0034h

Initial Value: 0000_8000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD_ISO_DONE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PD_ISO_EN
Initial Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 51.2-10 PMC_PD_CA53_ISOEN Register Contents

Bit Position	Bit Name	Description
31 to 16	—	Reserved. These bits are read as 0b.
15	PD_ISO_DONE	This bit indicates the isolation status inside the SoC. 0b: The internal state of the SoC is unstable during the isolation process. 1b: SoC internal isolation is stable.
14 to 1	—	Reserved. These bits are read as 0b.
0	PD_ISO_EN	This bit sets the power domain PD_CA53 isolation. 0b: Release the fixed output signal (isolation). 1b: Fix the output signal (isolation).

51.2.2.10 Idle Request Register (PMC_IDLE_REQ)

PMC_IDLE_REQ controls a request to separate the bus master port and bus slave port of the unit in the power domain PD_*#NAME* (PD_MEM, VIDEO0, VIDEO1, RFX).

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0038h

Initial Value: 0000_001Eh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	PD_RFX_WEN	PD_VIDEO1_WEN	PD_VIDEO0_WEN	PD_MEM_WEN	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PD_RFX_IDLE_REQ	PD_VIDEO1_IDLE_REQ	PD_VIDEO0_IDLE_REQ	PD_MEM_IDLE_REQ	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	R

Table 51.2-11 PMC_IDLE_REQ Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 21	—	Reserved. These bits are read as 0b.
20	PD_RFX_WEN	PD_RFX_IDLE_REQ is allowed to be written. This bit is read as 0b. 0b: Write disable 1b: Write enable
19	PD_VIDEO1_WEN	PD_VIDEO1_IDLE_REQis allowed to be written. This bit is read as 0b. 0b: Write disable 1b: Write enable
18	PD_VIDEO0_WEN	PD_VIDEO0_IDLE_REQ is allowed to be written. This bit is read as 0b. 0b: Write disable 1b: Write enable
17	PD_MEM_WEN	PD_MEM_IDLE_REQis allowed to be written. This bit is read as 0b. 0b: Write disable 1b: Write enable
16 to 5	—	Reserved. These bits are read as 0b.
4	PD_RFX_IDLE_REQ	This bit controls the separation (operation stop) and connection (operation restart) of the units in PD_RFX. 0b: Connect the bus. 1b: Isolate the bus.
3	PD_VIDEO1_IDLE_REQ	This bit controls the separation (operation stop) and connection (operation restart) of the units in PD_VIDEO1. 0b: Connect the bus. 1b: Isolate the bus.
2	PD_VIDEO0_IDLE_REQ	This bit controls the separation (operation stop) and connection (operation restart) of the units in PD_VIDEO0. 0b: Connect the bus. 1b: Isolate the bus.

Table 51.2-11 PMC_IDLE_REQ Register Contents (2/2)

Bit Position	Bit Name	Description
1	PD_MEM_IDLE_REQ	This bit controls the separation (operation stop) and connection (operation restart) of the units in PD_MEM. 0b: Connect the bus. 1b: Isolate the bus.
0	—	Reserved. This bit is read as 0b.

51.2.2.11 Idle Request Status Register (PMC_IDLE_STS)

PMC_IDLE_STS indicates the status of bus separation and connection.

Physical power domains PD_VIDEO1_0 and PD_VIDEO1_1 return the status of the logical power domain PD_VIDEO1.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 003Ch

Initial Value: 0000_001Eh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	PD_RFX_ACT_DONE	PD_VIDEO1_ACT_DONE	PD_VIDEO0_ACT_DONE	PD_MEM_ACT_DONE	—	—	—	—	PD_RFX_IDLE_DONE	PD_VIDEO1_IDLE_DONE	PD_VIDEO0_IDLE_DONE	PD_MEM_IDLE_DONE	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 51.2-12 PMC_IDLE_STS Register Contents

Bit Position	Bit Name	Description
31 to 13	—	Reserved. These bits are read as 0b.
12	PD_RFX_ACT_DONE	This bit returns the status of PD_RFX bus connection processing. 0b: Disconnected 1b: Connection
11	PD_VIDEO1_ACT_DONE	This bit returns the status of PD_VIDEO1 bus connection processing. 0b: Disconnected 1b: Connection
10	PD_VIDEO0_ACT_DONE	This bit returns the status of PD_VIDEO0 bus connection processing. 0b: Disconnected 1b: Connection
9	PD_MEM_ACT_DONE	This bit returns the status of PD_MEM bus connection processing. 0b: Disconnected 1b: Connection
8 to 5	—	Reserved. These bits are read as 0b.
4	PD_RFX_IDLE_DONE	This bit returns the status of PD_RFX bus separation processing. 0b: Unseparated 1b: Separation
3	PD_VIDEO1_IDLE_DONE	This bit returns the status of PD_VIDEO1 bus separation processing. 0b: Unseparated 1b: Separation
2	PD_VIDEO0_IDLE_DONE	This bit returns the status of PD_VIDEO0 bus separation processing. 0b: Unseparated 1b: Separation
1	PD_MEM_IDLE_DONE	This bit returns the status of PD_MEM bus separation processing. 0b: Unseparated 1b: Separation
0	—	Reserved. This bit is read as 0b.

51.2.2.12 CPU Standby Monitor Register (PMC_CPU_MON)

Monitors the standby state of the CA53 core 0, core 1 and L2 cache.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0040h

Initial Value: 0000_0000h*1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	L2_STBY	CPU1_STBY	CPU0_STBY	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note 1. The values that can be read by the CPU after a cold boot of CA53 are shown.

Table 51.2-13 PMC_CPU_MON Register Contents

Bit	Bit Name	Description
31 to 6	—	Reserved. These bits are read as 0b.
5	L2_STBY	Reads whether CA53 is in the standby state (L2 Wait for Interrupt). 0b: Normal state 1b: Standby state
4	CPU1_STBY	Reads whether CA53 core 1 is in the standby state (Core Wait for Interrupt). 0b: Normal state 1b: Standby state
3	CPU0_STBY	Reads whether CA53 core 0 is in the standby state (Core Wait for Interrupt). 0b: Normal state 1b: Standby state
2	—	Reserved. When read, the value read is undefined.
1, 0	—	Reserved. These bits are read as 0b.

51.2.2.13 Interrupt Status Register (PMC_INT_STS)

PMC_INT_STS indicates the interrupt factor occurred or not. This register changes even when an interrupt is masked (see PMC_INT_MSK register).

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0044h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	L2_STBY	CPU1_STBY	CPU0_STBY	—	IDLE_DONE	PD_DONE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 51.2-14 PMC_INT_STS Register Contents

Bit Position	Bit Name	Description
31 to 6	—	Reserved. These bits are read as 0b.
5	L2_STBY	Reads whether there is a standby (L2 Wait for Interrupt) detection interrupt for CA53. 0b: No interrupt factor has occurred. Or the interrupt factor has been released. 1b: An interrupt factor has occurred.
4	CPU1_STBY	Reads whether there is a standby (Core Wait for Interrupt) detection interrupt for core 1 of CA53. 0b: No interrupt factor has occurred. Or the interrupt factor has been released. 1b: An interrupt factor has occurred.
3	CPU0_STBY	Reads whether there is a standby (Core Wait for Interrupt) detection interrupt for core 0 of CA53. 0b: No interrupt factor has occurred. Or the interrupt factor has been released. 1b: An interrupt factor has occurred.
2	—	Reserved. When read, the value read is undefined.
1	IDLE_DONE	Reads whether there is a bus separation completion interrupt for any power domain. 0b: No interrupt factor has occurred. Or the interrupt factor has been released. 1b: An interrupt factor has occurred.
0	PD_DONE	Reads whether there is a power domain power on/off process completion interrupt. 0b: No interrupt factor has occurred. Or the interrupt factor has been released. 1b: An interrupt factor has occurred.

51.2.2.14 Interrupt Clear Register (PMC_INT_CLR)

PMC_INT_CLR clears the interrupt source of Interrupt Status Register (PMC_INT_STS).

Writing ‘1b’ to the bit field of this register clears the corresponding bit in the interrupt status register PMC_INT_STS. Writing a ‘0b’ does not change the corresponding bit in the interrupt status register PMC_INT_STS. If an interrupt request is detected simultaneously with the clearing of the interrupt source, the interrupt request has priority and the specified bit is set to 1b.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0048h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	L2_STBY	CPU1_STBY	CPU0_STBY	—	IDLE_DONE	PD_DONE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Table 51.2-15 PMC_INT_CLR Register Contents

Bit Position	Bit Name	Description
31 to 6	—	Reserved. These bits are read as 0b.
5	L2_STBY	Writing 1b clears the CA53 standby (L2 Wait for Interrupt) detection interrupt source.
4	CPU1_STBY	Writing 1b clears the CA53 core 1 standby (Core Wait for Interrupt) detection interrupt source.
3	CPU0_STBY	Writing 1b clears the CA53 core 0 standby (Core Wait for Interrupt) detection interrupt source.
2	—	Reserved. This bit is read as 0b. The write value should always be 0b.
1	IDLE_DONE	When 1b is written, the bus interrupt completion interrupt source of any power domain is cleared.
0	PD_DONE	Writing 1b clears the power domain power on/off process completion interrupt source.

51.2.2.15 Interrupt Mask Register (PMC_INT_MSK)

PMC_INT_MSK sets the interrupt output mask.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 004Ch

Initial Value: 0000_003Fh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	L2_WEN	CPU1_WEN	CPU0_WEN	—	IDLE_WEN	PD_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	L2_STBY	CPU1_STBY	CPU0_STBY	—	IDLE_DONE	PD_DONE
Initial Value	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW

Table 51.2-16 PMC_INT_MSK Register Contents (1/2)

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b.
21	L2_WEN	Writing to L2_STBY (bit 5) is permitted. 0b: Write disable 1b: Write enable
20	CPU1_WEN	Writing to CPU1_STBY(bit 4) is permitted. 0b: Write disable 1b: Write enable
19	CPU0_WEN	Writing to CPU0_STBY(bit 3) is permitted. 0b: Write disable 1b: Write enable
18	—	Reserved. These bits are read as 0b. The write value should always be 0b.
17	IDLE_WEN	Writing to IDLE_DONE (bit 1) is permitted. 0b: Write disable 1b: Write enable
16	PD_WEN	Writing to PD_DONE (bit 0) is permitted. 0b: Write disable 1b: Write enable
15 to 6	—	Reserved. These bits are read as 0b.
5	L2_STBY	This bit masks the CA53 standby (L2 Wait for Interrupt) detection interrupt. 0b: Unmasked state 1b: Mask state
4	CPU1_STBY	This bit masks the standby (Core Wait for Interrupt) detection interrupt of CA53 core 1. 0b: Unmasked state 1b: Mask state
3	CPU0_STBY	This bit masks the standby (Core Wait for Interrupt) detection interrupt of CA53 core 0. 0b: Unmasked state 1b: Mask state
2	—	Reserved. When read, the value read is undefined.

Table 51.2-16 PMC_INT_MSK Register Contents (2/2)

Bit Position	Bit Name	Description
1	IDLE_DONE	This bit masks the completion interrupt for bus separation of any power domain. 0b: Unmasked state 1b: Mask state
0	PD_DONE	This bit masks the power domain power on/off completion interrupt. 0b: Unmasked state 1b: Mask state

51.2.2.16 CA53 SRAM SDM Configuration Register (PMC_CA53_SDM_CFG)

Sets whether to retain or discard the SRAM data when the CA53 SRAM (L1 / L2 cache) is set to the standby state. Do not change the standby state of SRAM for 333 nsec before and after changing the setting of this register.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0090h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2_WEN	C1L1_WEN	C0L1_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2	C1L1	C0L1
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 51.2-17 PMC_CA53_SDM_CFG Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b.
18	L2_WEN	Writing to L2 (bit 2) is permitted. 0b can be read. 0b: Write disable 1b: Write enable
17	C1L1_WEN	Writing to C1L1 (bit 1) is permitted. 0b can be read. 0b: Write disable 1b: Write enable
16	C0L1_WEN	Writing to C0L1 (bit 0) is permitted. 0b can be read. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b.
2	L2	Set the data handling when the CA53 L2 cache is set to the standby state. 0b: Reserved. 1b: Change to the shutdown state (discard data).
1	C1L1	Set the data handling when the CA53 core 1 L1 cache is set to the standby state. 0b: Reserved. 1b: Change to the shutdown state (discard data).
0	C0L1	Set the data handling when the CA53 core 0 L1 cache is set to the standby state. 0b: Reserved. 1b: Change to the shutdown state (discard data)

51.2.2.17 CA53 SRAM RS Control Register (PMC_CA53_RS_CTL)

Controls the standby state of SRAM (cache) of CA53.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0094h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2_WEN	C1L1_WEN	C0L1_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2	C1L1	C0L1
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 51.2-18 PMC_CA53_RS_CTL Register Contents

Bit Position	Bit Name	Description
31 to 19	—	Reserved. These bits are read as 0b.
18	L2_WEN	Writing to L2 (bit 2) is permitted. 0b can be read. 0b: Write disable 1b: Write enable
17	C1L1_WEN	Writing to C1L1 (bit 1) is permitted. 0b can be read. 0b: Write disable 1b: Write enable
16	C0L1_WEN	Writing to C0L1 (bit 0) is permitted. 0b can be read. 0b: Write disable 1b: Write enable
15 to 3	—	Reserved. These bits are read as 0b.
2	L2	Set the L2 cache of CA53 to the standby state or restore it to the normal state. 0b: Change to the normal state (release from the standby state). 1b: Change to the standby state.
1	C1L1	Set the L1 cache of CA53 core 1 to the standby state or restore it to the normal state. 0b: Change to the normal state (release from the standby state). 1b: Change to the standby state.
0	C0L1	Set L1 cache of CA53 core 0 to the standby state or restore it to the normal state. 0b: Change to the normal state (release from the standby state). 1b: Change to the standby state.

51.2.2.18 CA53 SRAM RS Status Register (PMC_CA53_RS_STS)

Reading this register returns the level value of the CA53_L2_SRAM_RS and CA53_L1_SRAM_RS [1:0] pins.

Access Size: 32 bits

Address(es): <PMC_S0_base> + 0098h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2	C1L1	C0L1
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 51.2-19 PMC_CA53_RS_STS Register Contents

Bit Position	Bit Name	Description
31 to 3	—	Reserved. These bits are read as 0b.
2	L2	Reads the L2 cache status of CA53. 0b: Normal state 1b: Standby state
1	C1L1	Reads the L1 cache status of CA53 core 1. 0b: Normal state 1b: Standby state
0	C0L1	Reads the L1 cache status of CA53 core 0. 0b: Normal state 1b: Standby state

51.3 Functional Description

51.3.1 Connection Overview

Figure 51.3-1 shows an overview of the peripheral connections for power control of the PMC.

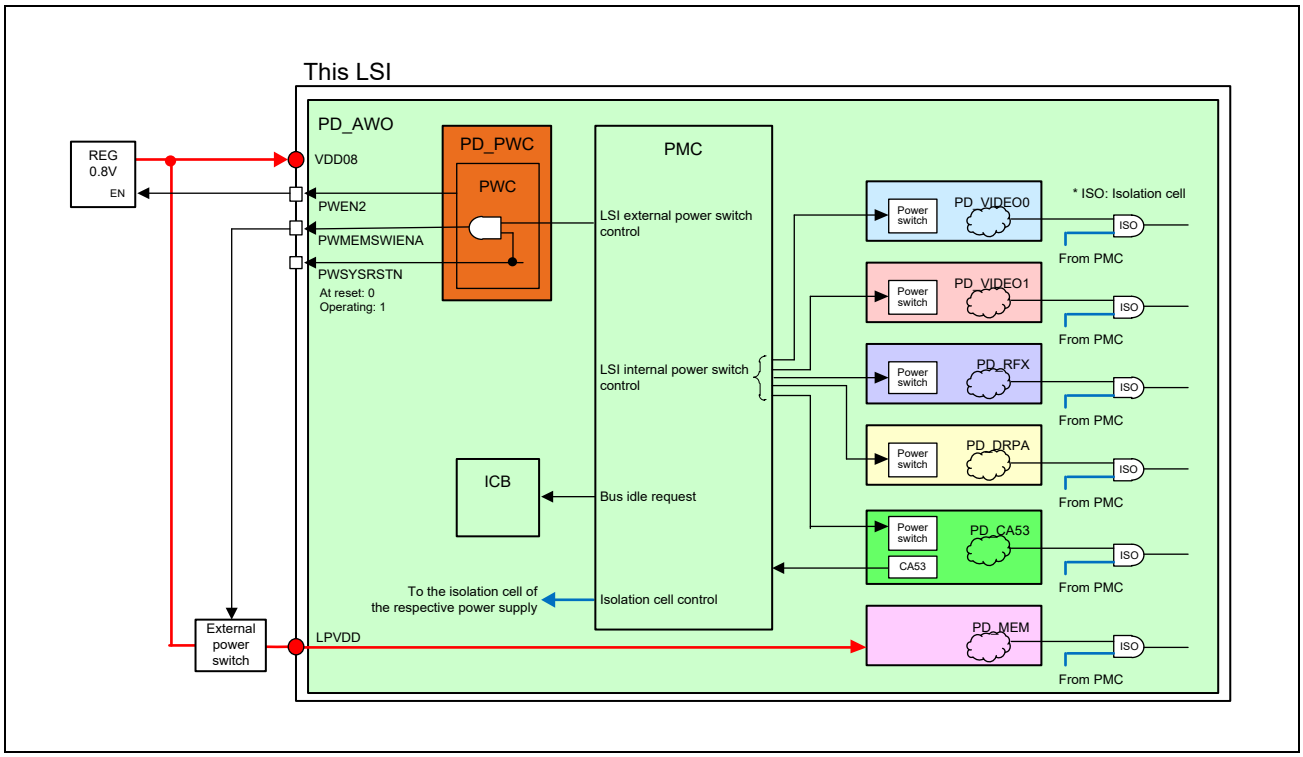


Figure 51.3-1 Overview of Control Signal Connection

51.3.2 Internal Power Domain On/Off Control

Figure 51.3-2 shows a block diagram of the internal power domain on/off control function.

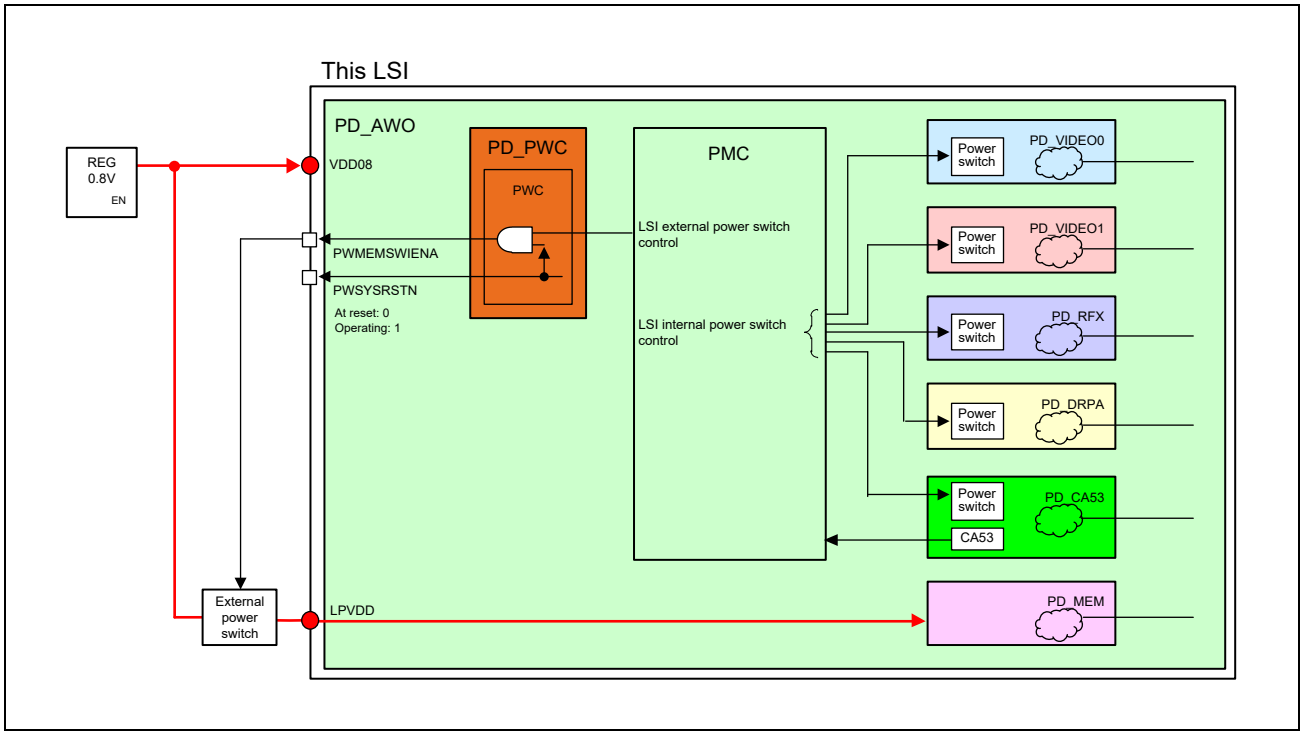


Figure 51.3-2 Internal Power Domain On/Off Control

51.3.2.1 Internal Power Domain On/Off Control

The power domain on/off control is performed by PMC_SPLY_ENA. The power domain to be controlled is set by the PD_NUM bit.

It is possible to confirm that the power domain on/off process is in progress with PMC_MAIN_STS. When the power domain on/off process is completed, the PD_*#NAME*_ON bit is set to 1 (power on) or 0 (power off).

CAUTION

As shown in **Figure 51.3-2**, power domains other than PD_MEM have internal power switches and can be controlled on/off by registers. In the other hand, PD_MEM controls the on/off state of the power domain by controlling an external power switch. The external power switch can be controlled by the enable signal output from the PWMEMSWIENA pin via the PWC.

51.3.2.2 Internal Power Domain On/Off Completion Interrupt

The completion of the power domain on/off process can be notified as an interrupt. The interrupt factor can be checked by reading PMC_INT_STS. The default state after a reset is masked. Therefore, cancel the mask setting of PMC_INT_MSK if an interrupt is to be notified.

After the interrupt signal is detected by the CPU, clear the interrupt notification with PD_DONE in PMC_INT_CLR.

51.3.2.3 Internal Power Domain On/Off Time Setting

Since PD_MEM uses an external power switch, the power domain on/off time must be set in advance according to the startup time of the external power supply. The setting is made by PMC_PD_MEM_TIM. After the set time has elapsed, an interrupt is notified by PMC_INT_STS.

51.3.2.4 Related Registers

Table 51.3-1 Power On/Off Control Related Registers

Register Abbreviation	Bit Name	Function
PMC_SPLY_ENA	ON	Controls power on/off.
	PD_NUM	Specifies the target domain for power on/off.
PMC_MAIN_STS	PD_BUSY	Indicates the status of the power-on or power-off sequence process.
	PD_*#NAME*_ON	Reads the power status (on/off) of the respective power domain.
PMC_PD_MEM_TIM	PD_OFF_TIM	Sets the margin time until the external power switch is turned off.
	PD_ON_TIM	Sets the margin time until the external power switch is turned on.
PMC_INT_STS	IDLE_DONE	Reads the bus separation completion interrupt status.
	PD_DONE	Notifies the completion of power on/off control.
PMC_INT_CLR	IDLE_DONE	Clears the bus separation completion interrupt.
	PD_DONE	Clears the power-on/off control completion interrupt.
PMC_INT_MSK	IDLE_DONE	Masks the notification of bus separation completion interrupt.
	PD_DONE	Masks the notification of power on/off control completion interrupt.

Note: *#NAME* = MEM, VIDEO0, VIDEO1, RFX, DRPA, CA53

51.3.3 Isolation Cell Control

Figure 51.3-3 shows a block diagram of the isolation cell control function.

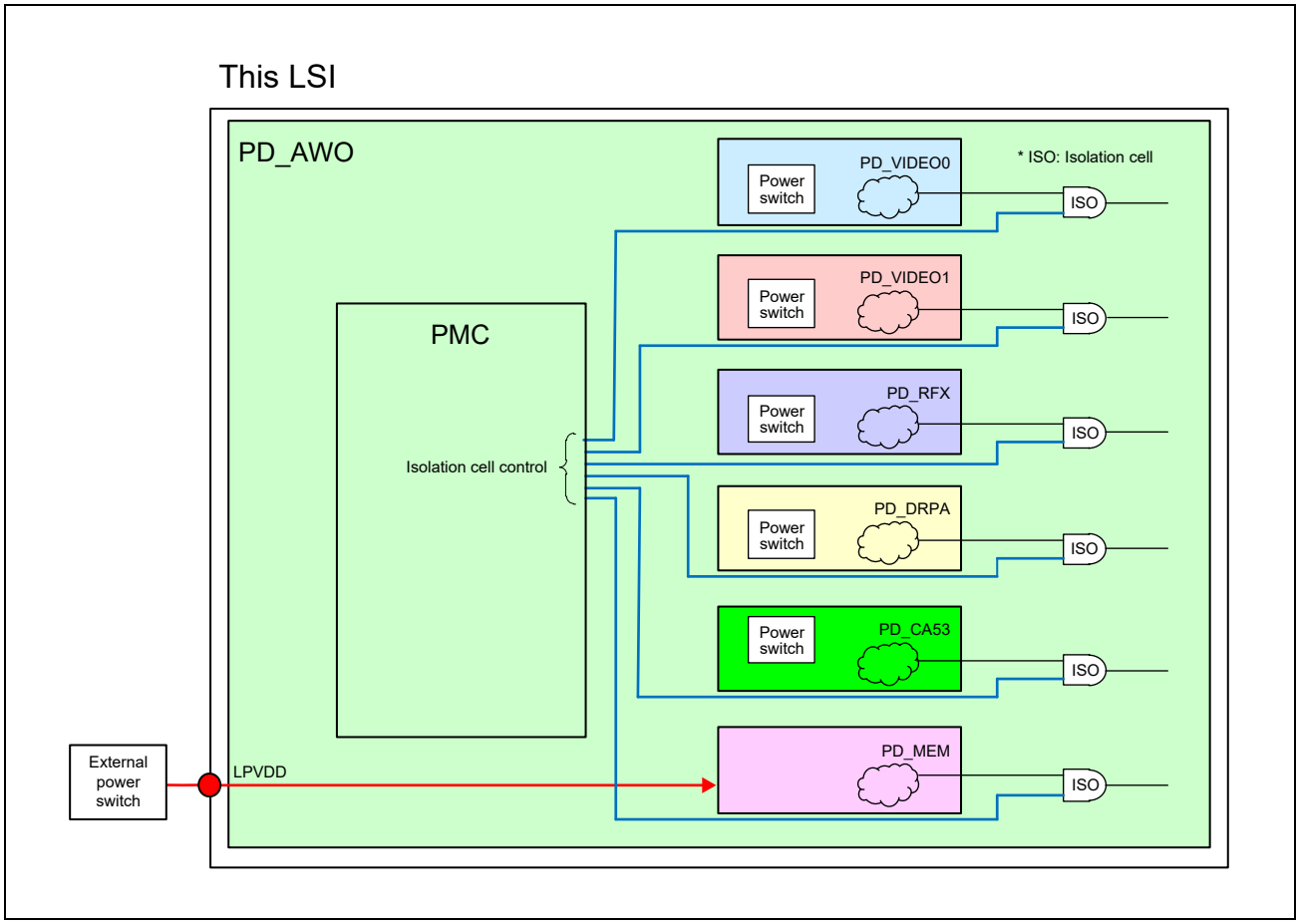


Figure 51.3-3 Isolation Cell Control

51.3.3.1 Isolation Settings

When the power switch is turned off, the undefined propagation output from the power domain must be suppressed (isolated). The isolation is set by PMC_PD_*#NAME*_ISOEN. The PD_ISO_DONE bit indicates that the isolation has stabilized.

51.3.3.2 Isolation Release

The isolation is released by PMC_PD_*#NAME*_ISOEN. After releasing the isolation, 104 nsec (5clk@PCLK) is required for the internal signal level to be stabilized.

Make sure that the PD_ISO_DONE bit in PMC_PD_*#NAME*_ISOEN is set to 1 before starting the unit operation for the respective power domain.

51.3.3.3 Related Registers

Table 51.3-2 Isolation Control Related Registers

Register Abbreviation	Bit Name	Function
PMC_PD_*#NAME*_ISOEN	PD_ISO_DONE	Checks the isolation stability state.
	PD_ISO_EN	Enables the isolation.

Note: *#NAME* = MEM, VIDEO0, VIDEO1, RFX, DRPA, CA53

51.3.4 Bus Idle Request Control

The interconnected bus (ICB) has a function to logically separate the bus I/F from the units in the power supply domains PD_MEM, PD_VIDEO0, PD_VIDEO1, and PD_RFX. When the ICB receives a bus isolation request from this unit, it notifies the completion of all bus transactions (bus idle) in the relevant power domain.

In the case of an accidental access to a bus-separated unit, the ICB returns an error response instead of the slave. This prevents the bus from deadlocking.

CAUTION

Although only the AXI slave port of MMC has the bus isolation function of the power domain PD_MEM, the APB register slave port of MMC and the APB register slave port of DDI do not have the bus isolation function.

Therefore, do not access the APB register slave port of the MMC and the APB register slave port of the DDI in the bus isolated state.

51.3.4.1 Bus Separation

The bus separation is requested to the ICB by PMC_IDLE_REQ. The completion of all bus transactions (completion of bus separation) in the corresponding power domain can be checked by reading PMC_IDLE_STS.

The completion of the bus separation can also be notified as an interrupt. The interrupt factor can be checked by reading PMC_INT_STS. The default state after a reset is masked. Therefore, cancel the mask setting of PMC_INT_MSK if an interrupt is to be notified.

51.3.4.2 Bus Connection

The bus separation request withdrawal (bus connection request) sets the PD_#*NAME*_IDLE_REQ bit in PMC_IDLE_REQ to 0. The bus connection status can be checked with PMC_IDLE_STS.

CAUTION

The function to notify the completion of bus connection as an interrupt is not provided. However, if a bus separation request is withdrawn (PD_#*NAME*_IDLE_REQ is set to 0) and a bus separation state is entered at the same time, a bus separation process completion interrupt may be generated.

51.3.4.3 Related Registers

Table 51.3-3 Bus Idle Request Control Related Registers

Register Abbreviation	Bit Name	Function
PMC_IDLE_REQ	PD_#*NAME*_IDLE_REQ	Requests bus isolation for units in the power domain.
PMC_IDLE_STS	PD_#*NAME*_ACT_DONE	The status of the bus connection can be checked during bus processing for a bus separation request.
	PD_#*NAME*_IDLE_DONE	The status of bus separation can be checked during bus processing for a bus separation request.
PMC_INT_STS	IDLE_DONE	Reads the bus separation completion interrupt status.
	PD_DONE	Notifies the completion of power on/off control.
PMC_INT_CLR	IDLE_DONE	Clears the bus separation completion interrupt.
	PD_DONE	Clears the power-on/off control completion interrupt.
PMC_INT_MSK	IDLE_DONE	Masks the notification of bus isolation completion interrupt.
	PD_DONE	Masks the notification of power on/off control completion interrupt.

Note: #*NAME* = MEM, VIDEO0, VIDEO1, RFX

CAUTION

Table 51.3-4 lists the enable/disable state of bus access and power-off for various states of the PD_#*NAME*_IDLE_REQ bit in PMC_IDLE_REQ and the PD_#*NAME*_IDLE_DONE and PD_#*NAME*_ACT_DONE bits in PMC_IDLE_STS.

Table 51.3-4 Bus Idle Request Status

	PD_#*NAME*_IDLE_REQ	PD_#*NAME*_ACT_DONE	PD_#*NAME*_IDLE_DONE	Bus Access	Power-off
Bus connection	0	1	0	Enabled	Disabled
Bus separation in progress	1	0	0	Disabled	Disabled
Bus separation	1	0	1	Disabled	Enabled
Bus connection in progress	0	0	0	Disabled	Disabled
Bus (re)connection	0	1	0	Enabled	Disabled

Note: #*NAME* = MEM, VIDEO0, VIDEO1, RFX

51.3.5 CPU Standby Detection

51.3.5.1 Functional Description

The CPU standby detection function detects that core 0 or core 1 of CA53 has entered the standby state by executing a WFI instruction and outputs an interrupt request INT_PMC.

The standby state of the CPU is detected by the CA53_STANDBYWFI[1:0] and CA53_STANDBYWFIL2 signals of CA53. The interrupt status can be checked by the L2_STBY, CPU1_STBY, and CPU0_STBY bits of PMC_INT_STS. Also, the CA53_STANDBYWFI[1:0] and CA53_STANDBYWFIL2 signals of CA53 can be monitored by using the PMC_CPU_MON register.

51.3.5.2 Related Registers

Table 51.3-5 CPU Standby Detection Related Registers

Register Abbreviation	Bit Name	Function
PMC_INT_STS	L2_STBY	Indicates the interrupt status of the L2 cache.
	CPU1_STBY	Indicates the interrupt status of CPU core 1.
	CPU0_STBY	Indicates the interrupt status of CPU core 0.
PMC_CPU_MON	L2_STBY	Indicates the standby state of the L2 cache.
	CPU1_STBY	Indicates the standby state of CPU core 1.
	CPU0_STBY	Indicates the standby state of CPU core 0.

51.3.6 CPU Standby Control

51.3.6.1 Functional Description

CPU standby control is for controlling standby of the CPU SRAM. This LSI can only handle standby control for core 1. Standby control for core 0 and the L2 cache is prohibited.

51.3.6.2 Related Registers

Two registers are used to set software standby control for the SRAM (L2 cache, core 0 L1 cache, core 1 L1 cache) of CA53.

[Setting the mode for standby of the SRAM]

- PMC_CA53_SDM_CFG register:
  - L2 bit
    0: Reserved
    1: Shutdown
  - C1L1 bit
    0: Reserved
    1: Shutdown
  - C0L1 bit
    0: Reserved
    1: Shutdown

[Setting standby of the SRAM]

- PMC_CA53_RS_CTL register:
  - L2 bit
    0: Normal
    1: Standby
  - C1L1 bit
    0: Normal
    1: Standby
  - C0L1 bit
    0: Normal
    1: Standby

51.3.6.3 CA53 standby level

The standby state of CA53 has the following levels. When making the settings, core 0 of CA53 is set as a master CPU and core 1 as a slave CPU.

Table 51.3-6 CA53 Standby Level

Operating Mode		Master Core		Slave Core		L2 Cache	Core mode
		Logic	L1 Cache	Logic	L1 Cache		
Run	Normal	Normal	Normal	Normal	Normal	Dual core	—
Standby mode	Standby LV1	Normal	Normal	Individual core shutdown	Normal	Normal	Single core
	Standby LV2	Normal	Normal	Individual core shutdown	standby (shutdown)	Normal	Single core
Power Off		Power Off	Power Off	Power Off	Power Off	Power Off	—

Note:

– Normal: The normal operating state in which the clock is operating.

– Individual core shutdown: For individual core shutdown mode, refer to steps 1 to 7 of the power down sequence in the “Individual core shutdown mode” section in “2.4.2 Power modes” of *the ARM Cortex-A53 MPCore Processor Technical Reference Manual*. Since this LSI does not have a power-off function for individual cores, it only covers the state up to the point where Wait for interrupt is executed in response to a cache flush.

– Standby (shutdown): A state in which the SRAM has entered shutdown mode.

– Power Off: A state in which power is not supplied to the power domain (PD_CA53).

51.3.6.4 CA53 Standby State Transition Diagram

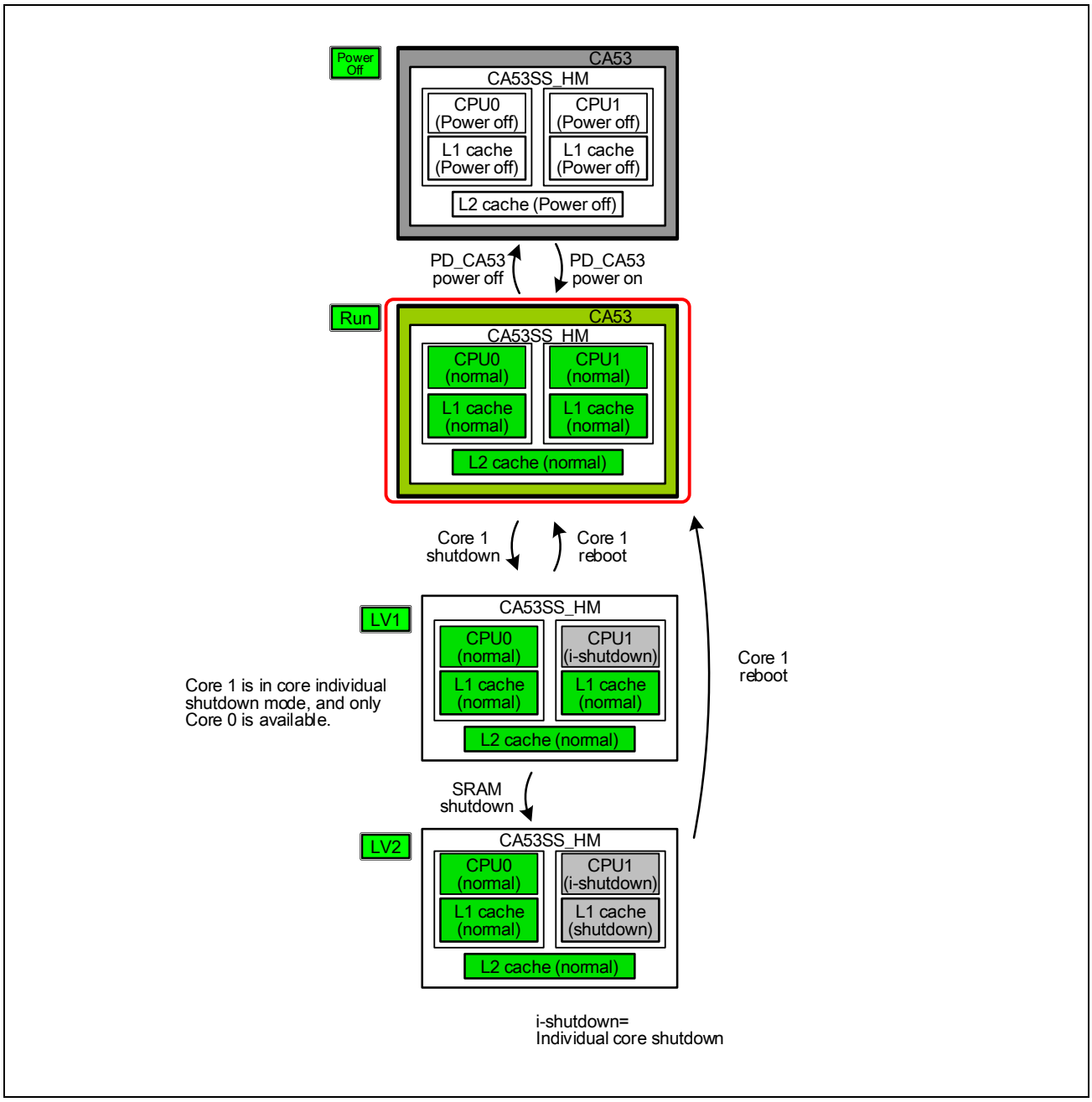


Figure 51.3-4 CA53 Standby Level State Transition Diagram

51.4 Operating Procedure

For more information, contact a Renesas Electronics sales representative.

51.5 Constraints

The PMC has the following constraints.

Table 51.5-1 Functional Constraints

Classification	Item	Constraints
Power domain control	Multiple power domain control	While the power-on/off process is in progress, writing a power-on or power-off command to the PMC_SPLY_ENA register will be ignored. The process being executed will continue without stopping. The ignored command will not be started after the completion of the process being executed.
	Power domain control	When an instruction to start power-on control is given to the power domain in the power-on state, the power-on process is performed and an interrupt is output. In a similar way, when an instruction to start power-off control is given to a power domain in the power-off state, the power-off process is performed and an interrupt is output. The power on/off status will not change.
	Power on/off time for power domain PD_MEM	The PMC_PD_MEM_TIM register, that holds the time required to power on/off the power domain PD_MEM, can be set to a value of up to 21.8 msec. Do not use an external power switch that takes more than 21.8 msec to turn on/off.
	Power domain access	The bus access to the power off power domain is prohibited.

Section 52 System Configuration (SYS)

This section describes the functions of the system configuration (SYS).

52.1 Functional Overview

The SYS controls the overall configuration of the chip.

Table 52.1-1 Functions of SYS in Outline

Category	Function	Description
System configulation unit	System configulation	• Bank address settings for DMAC • Bank address settings of the units for ICB • ETHER AxCACHE[1] (C bit) control function • RAMA initialization control • MD[7:0] pin monitoring • LSI version register • General-purpose 32-bit readable/writable registers • Observability counting stop control for ICB • WDT counter stop control • Reading of the temperature sensor reference value

52.2 Pin Functions

52.2.1 List of Internal Pins

52.2.1.1 List of DMAC DMAC0 Bank Address Pins

Table 52.2-1 lists the internal pins (bank address pins for DMAC DMAC0).

Table 52.2-1 List of Internal Pins

Pin Name	I/O	Function
DMAA DMAC0 Bank Address Signals		
DMAA_DMAC0_CH0_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch0 bank address control pin (for the source)
DMAA_DMAC0_CH0_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch0 bank address control pin (for the destination)
DMAA_DMAC0_CH0_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch0 bank address control pin (for the descriptor)
DMAA_DMAC0_CH1_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch1 bank address control pin (for the source)
DMAA_DMAC0_CH1_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch1 bank address control pin (for the destination)
DMAA_DMAC0_CH1_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch1 bank address control pin (for the descriptor)
DMAA_DMAC0_CH2_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 ch2 bank address control pin (for the source)
DMAA_DMAC0_CH2_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch2 bank address control pin (for the destination)
DMAA_DMAC0_CH2_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch2 bank address control pin (for the descriptor)
DMAA_DMAC0_CH3_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch3 bank address control pin (for the source)
DMAA_DMAC0_CH3_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch3 bank address control pin (for the destination)
DMAA_DMAC0_CH3_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch3 bank address control pin (for the descriptor)
DMAA_DMAC0_CH4_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch4 bank address control pin (for the source)
DMAA_DMAC0_CH4_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch4 bank address control pin (for the destination)
DMAA_DMAC0_CH4_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch4 bank address control pin (for the descriptor)
DMAA_DMAC0_CH5_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch5 bank address control pin (for the source)
DMAA_DMAC0_CH5_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch5 bank address control pin (for the destination)
DMAA_DMAC0_CH5_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch5 bank address control pin (for the descriptor)
DMAA_DMAC0_CH6_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch6 bank address control pin (for the source)
DMAA_DMAC0_CH6_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch6 bank address control pin (for the destination)
DMAA_DMAC0_CH6_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch6 bank address control pin (for the descriptor)
DMAA_DMAC0_CH7_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch7 bank address control pin (for the source)
DMAA_DMAC0_CH7_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch7 bank address control pin (for the destination)
DMAA_DMAC0_CH7_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC0 Ch7 bank address control pin (for the descriptor)

52.2.1.2 List of DMAC DMAC1 Bank Address Pins

Table 52.2-2 lists the internal pins (bank address pins for DMAC DMAC1).

Table 52.2-2 List of Internal Pins

Pin Name	I/O	Function
DMAC DMAC1 Bank Address Signals		
DMAA_DMAC1_CH0_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch0 bank address control pin (for the source)
DMAA_DMAC1_CH0_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch0 bank address control pin (for the destination)
DMAA_DMAC1_CH0_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch0 bank address control pin (for the descriptor)
DMAA_DMAC1_CH1_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch1 bank address control pin (for the source)
DMAA_DMAC1_CH1_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch1 bank address control pin (for the destination)
DMAA_DMAC1_CH1_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch1 bank address control pin (for the descriptor)
DMAA_DMAC1_CH2_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch2 bank address control pin (for the source)
DMAA_DMAC1_CH2_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch2 bank address control pin (for the destination)
DMAA_DMAC1_CH2_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch2 bank address control pin (for the descriptor)
DMAA_DMAC1_CH3_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch3 bank address control pin (for the source)
DMAA_DMAC1_CH3_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch3 bank address control pin (for the destination)
DMAA_DMAC1_CH3_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch3 bank address control pin (for the descriptor)
DMAA_DMAC1_CH4_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch4 bank address control pin (for the source)
DMAA_DMAC1_CH4_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch4 bank address control pin (for the destination)
DMAA_DMAC1_CH4_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch4 bank address control pin (for the descriptor)
DMAA_DMAC1_CH5_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch5 bank address control pin (for the source)
DMAA_DMAC1_CH5_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch5 bank address control pin (for the destination)
DMAA_DMAC1_CH5_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch5 bank address control pin (for the descriptor)
DMAA_DMAC1_CH6_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch6 bank address control pin (for the source)
DMAA_DMAC1_CH6_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch6 bank address control pin (for the destination)
DMAA_DMAC1_CH6_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch6 bank address control pin (for the descriptor)
DMAA_DMAC1_CH7_SRC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch7 bank address control pin (for the source)
DMAA_DMAC1_CH7_DST_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch7 bank address control pin (for the destination)
DMAA_DMAC1_CH7_DESC_BANK_ADDR[1:0]	Output	DMAC_DMAC1 Ch7 bank address control pin (for the descriptor)

52.2.1.3 List of Bank Address Pins of IP Modules for ICB

Table 52.2-3 lists the internal pins (bank address pins of the IP modules for the ICB).

Table 52.2-3 List of Internal Pins

Pin Name	I/O	Function
Peripheral Block Bank Address Signals		
EMM_BANK_ADDR[1:0]	Output	Bank address control pin for eMMC
SDI0_BANK_ADDR[1:0]	Output	Bank address control pin for SDI0
SDI1_BANK_ADDR[1:0]	Output	Bank address control pin for SDI1
USB_M0_BANK_ADDR[1:0]	Output	Bank address control pin for USB Host
USB_M1_BANK_ADDR[1:0]	Output	Bank address control pin for USB Function
PCI_BANK_ADDR[1:0]	Output	Bank address control pin for PCIe
ETH0_BANK_ADDR[1:0]	Output	Bank address control pin for ETHER
GRP_BANK_ADDR[1:0]	Output	Bank address control pin for GRP
VCD_BANK_ADDR[1:0]	Output	Bank address control pin for VCD
DRPA_M0_BANK_ADDR[1:0]	Output	Bank address control pin for DRP-AI M0
DRPA_M1_BANK_ADDR[1:0]	Output	Bank address control pin for DRP-AI M1
DRPA_M2_BANK_ADDR[1:0]	Output	Bank address control pin for DRP-AI M2
DRPA_M3_BANK_ADDR[1:0]	Output	Bank address control pin for DRP-AI M3

52.2.1.4 I/F Pins for ICB

Table 52.2-4 lists the internal pins (for the ICB).

Table 52.2-4 List of Internal Pins

Pin Name	I/O	Function
ETH AxCACHE[1] Signals		
ETH0_ARCACHE_1	Output	AR Ch cacheable bit control pin for ETHER
ETH0_AWCACHE_1	Output	AR Ch cacheable bit control pin for ETHER
ICB Observability Control Signals		
ICB_OBS_SUSP[8:0]	Output	OBS counting stop control pin

52.2.1.5 List of I/F Pins with PCIe

Table 52.2-5 lists the internal pins (I/F pins with the PCIe).

Table 52.2-5 List of Internal Pins (1/2)

Pin Name	I/O	Function
PCIe I/F Signal (1/2)		
FLR_REQ[1:0]	Input	Function Level Reset request Notifying the FLR request from the root Bit 0: Function 0 Bit 1: Function 1
FLR_RESET[1:0]	Output	Reset input for the Function Level Reset execution instruction Notifying the root of execution of FLR in response to FLR_REQ Bit 0: Function 0 Bit 1: Function 1
INTX_EP_F0	Output	INTX signal for function 0
INTX_EP_F1	Output	INTX signal for function 1
UI_EXTMSI_VAL0	Output	MSI interrupt notification pin
UI_EXTMSI_VAL1	Output	MSI interrupt notification pin
UI_EXTMSI_VAL2	Output	MSI interrupt notification pin
UI_EXTMSI_VAL3	Output	MSI interrupt notification pin
UI_EXTMSI_VAL4	Output	MSI interrupt notification pin
UI_EXTMSI_VEC0[4:0]	Output	MSI interrupt vector specification pin
UI_EXTMSI_VEC1[4:0]	Output	MSI interrupt vector specification pin
UI_EXTMSI_VEC2[4:0]	Output	MSI interrupt vector specification pin
UI_EXTMSI_VEC3[4:0]	Output	MSI interrupt vector specification pin
UI_EXTMSI_VEC4[4:0]	Output	MSI interrupt vector specification pin
UI_EXTMSI_FUNC0[2:0]	Output	MSI interrupt function number specification pin
UI_EXTMSI_FUNC1[2:0]	Output	MSI interrupt function number specification pin
UI_EXTMSI_FUNC2[2:0]	Output	MSI interrupt function number specification pin
UI_EXTMSI_FUNC3[2:0]	Output	MSI interrupt function number specification pin
UI_EXTMSI_FUNC4[2:0]	Output	MSI interrupt function number specification pin
ALLOW_ENTER_L1	Output	ASPM L1 state transition enable 0: Transition is inhibited. 1: Transition is enabled.
PME_TIM	Output	PM_PME message transmission clock (does not have a clock attribute)
PCI I/F Signal (2/2)		
TURN_OFF_EVENT	Input	PME_Turn_Off message reception notification pin
TURN_OFF_EVENT_ACK	Output	Turn off preparation completion notification pin
D3_EVENT_F0	Input	Non-D0 state transition request reception notification pin (for function 0)
D3_EVENT_F1	Input	Non-D0 state transition request reception notification pin (for function 1)
D3_EVENT_ACK_F0	Output	Non-D0 state transition preparation completion notification pin (for function 0)
D3_EVENT_ACK_F1	Output	Non-D0 state transition preparation completion notification pin (for function 1)
CFG_PMCSR_PME_STATUS_F0	Output	Power management event setting pin (for function 0)

Table 52.2-5 List of Internal Pins (2/2)

Pin Name	I/O	Function
CFG_PMCSR_PME_STATUS_F1	Output	Power management event setting pin (for function 1)
CFG_PMCSR_PME_STATUS_WRITECLEAR_F0	Input	PME status clearing notification pin (for function 0)
CFG_PMCSR_PME_STATUS_WRITECLEAR_F1	Input	PME status clearing notification pin (for function 1)
MODE_PORT	Output	Device type setting pin 0: Endpoint 1: Root complex
MODE_PORT_ENABLE_B	Output	Macro off mode setting pin 0: Normal operation 1: Macro off
PCI_LANE_SEL[1:0]	Output	Lane setting pin when accessing PMA registers 0x: Lane 0 1x: Lane 1 (x: Don’t care)

52.2.1.6 RAMA-ECC Initialization Control Pins

Table 52.2-6 lists the internal pins (I/F pins with RAMA).

Table 52.2-6 List of Internal Pins

Pin Name	I/O	Function
RAMA ECC Initialize Control Signals		
RAMA_VECCEN	Output	Switches enabling and disabling of error correction by the ECC. 0: ECC is disabled. 1: ECC is enabled.
RAMA_INIT	Output	RAMA ECC code area initialization control
RAMA_INIT_END	Input	RAMA ECC code area initialization end flag

52.2.1.7 MD0 to MD7 Pins

Table 52.2-7 lists the internal pins (MD0 to MD7 pins).

Table 52.2-7 List of Internal Pins

Pin Name	I/O	Function
Mode Signals		
MD0	Input	Boot device selection [0]
MD1	Input	Boot device selection [1]
MD2	Input	Boot device selection [2]
MD3	Input	Boot device write interface select
MD4	Input	Boot mode selection [0] (reserved)
MD5	Input	Boot mode selection [1]
MD6	Input	Boot mode selection [2]
MD7	Input	Boot mode selection [3] (reserved)

52.2.1.8 List of WDT-I/F Pins

Table 52.2-8 lists the internal pins (WDT-I/F pins).

Table 52.2-8 List of Internal Pins

Pin Name	I/O	Function
WDT Counter Stop Control Signals		
CST_HLTDBG[1:0]	Input	Trigger Pin for WDT (input from CST) 0: Counting by the WDT is possible. 1: Stops counting by the WDT.
WDT_CNTSTOP[1:0]	Output	WDT Counting Stop Control (output to WDT) 0: Counting by the WDT is possible. 1: Stops counting by the WDT.

The following describes the internal pin functions of the SYS.

52.2.2 Bank Address Switching Pins

52.2.2.1 Bank Addresses for DMAC

These pins are connected to the DMAC and extend the area which can be accessed by the instruction from the SYS from 32 bits (4 GB) to 34 bits (16 GB).

DMAA_DMAC0_CHn_SRC_BANK_ADDR[1:0]

DMAC DMAC0 Channel N Source Bank Address

Note: n = 0 to 7

DMAA_DMAC0_CHn_DST_BANK_ADDR[1:0]

DMAC DMAC0 Channel N Destination Bank Address

Note: n = 0 to 7

DMAA_DMAC0_CHn_DESC_BANK_ADDR[1:0]

DMAC DMAC0 Channel N Descriptor Bank Address

Note: n = 0 to 7

DMAA_DMAC1_CHn_SRC_BANK_ADDR[1:0]

DMAC DMAC1 Channel N Source Bank Address

Note: n = 0 to 7

DMAA_DMAC1_CHn_DST_BANK_ADDR[1:0]

DMAC DMAC1 Channel N Destination Bank Address

Note: n = 0 to 7

DMAA_DMAC1_CHn_DESC_BANK_ADDR[1:0]

DMAC DMAC1 Channel N Descriptor Bank Address

Note: n = 0 to 7

52.2.2.2 Bank Addresses for ICB

EMM_BANK_ADDR[1:0]

eMMC Bank Address
This pin is connected to the ICB and extends the area which can be accessed by eMMC from 32 bits (4 GB) to 34 bits (16 GB).

SDI0_BANK_ADDR[1:0]

SDI0 Bank Address
This pin is connected to the ICB and extends the area which can be accessed by SDI0 from 32 bits (4 GB) to 34 bits (16 GB).

SDI1_BANK_ADDR[1:0]

SDI1 Bank Address
This pin is connected to the ICB and extends the area which can be accessed by SDI1 from 32 bits (4 GB) to 34 bits (16 GB).

USB_M0_BANK_ADDR[1:0]

USB Host Bank Address
This pin is connected to the ICB and extends the area which can be accessed by a USB host from 32 bits (4 GB) to 34 bits (16 GB).

USB_M1_BANK_ADDR[1:0]

USB Peripheral Bank Address
This pin is connected to the ICB and extends the area which can be accessed by a USB peripheral from 32 bits (4 GB) to 34 bits (16 GB).

PCI_BANK_ADDR[1:0]

PCIe Bank Address
This pin is connected to the ICB and extends the area which can be accessed by the PCIe from 32 bits (4 GB) to 34 bits (16 GB).

ETH_BANK_ADDR[1:0]

ETHER Bank Address
This pin is connected to the ICB and extends the area which can be accessed by the ETHER from 32 bits (4 GB) to 34 bits (16 GB).

GRP_BANK_ADDR[1:0]

GRP Bank Address
This pin is connected to the ICB and extends the area which can be accessed by the GRP from 32 bits (4 GB) to 34 bits (16 GB).

VCD_BANK_ADDR[1:0]

VCD Bank Address
This pin is connected to the ICB and extends the area which can be accessed by the VCD from 32 bits (4 GB) to 34 bits (16 GB).

DRPA_M0_BANK_ADDR[1:0]

DRP-AI M0 Bank Address
This pin is connected to the ICB and extends the area which can be accessed by DRP-AI M0 from 32 bits (4 GB) to 34 bits (16 GB).

DRPA_M1_BANK_ADDR[1:0]

DRP-AI M1 Bank Address
This pin is connected to the ICB and extends the area which can be accessed by DRP-AI M1 from 32 bits (4 GB) to 34 bits (16 GB).

DRPA_M2_BANK_ADDR[1:0]

DRP-AI M2 Bank Address
This pin is connected to the ICB and extends the area which can be accessed by DRP-AI M2 from 32 bits (4 GB) to 34 bits (16 GB).

DRPA_M3_BANK_ADDR[1:0]

DRP-AI M3 Bank Address
This pin is connected to the ICB and extends the area which can be accessed by DRP-AI M3 from 32 bits (4 GB) to 34 bits (16 GB).

52.2.3 I/F Pins for ICB

52.2.3.1 ETH AxCACHE[1]

ETH0_ARCACHE_1

ETHER AR Channel Cacheable Bit Control Pin
This pin is connected to the ICB and controls ARCACHE[1] (cacheable bit) for the AR channel of the ETHER.

ETH0_AWCACHE_1

ETHER AW Channel Cacheable Bit Control Pin
This pin is connected to the ICB and controls AWCACHE[1] (cacheable bit) for the AW channel of the ETHER.

52.2.3.2 Observability

ICB_OBS_SUSP[8:0]

ICB Observability Counting Stop Pin

Bit 8: StatSuspend for Scheduler Output Ports

Bit 7: StatSuspend for Scheduler Input Port #8

Bit 6: StatSuspend for Scheduler Input Port #7

Bit 5: StatSuspend for Scheduler Input Port #6

Bit 4: StatSuspend for Scheduler Input Port #5

Bit 3: StatSuspend for Scheduler Input Port #4

Bit 2: StatSuspend for Scheduler Input Port #3

Bit 1: StatSuspend for Scheduler Input Port #2

Bit 0: StatSuspend for Scheduler Input Port #1

52.2.4 I/F Pins with PCIe

The following pins are connected to the pins with the same name as the PCIe unit.

For details of the pin functions, refer to the section of PCIe.

52.2.4.1 Function Level Reset

FLR_REQ[1:0]

Function Level Reset request notification pin supplied from the PCIe (active high) (for endpoint).
Each bit corresponds to the function number.

FLR_RESET[1:0]

Reset pin for the Function Level Reset execution instruction for output to the PCIe (active high) (for endpoint).
Each bit corresponds to the function number.

52.2.4.2 Interrupt Control Pins

These are legacy interrupt and Assert_INTx/Deassert_INTx control pins and MSI transmission pins.

INTX_EP_F0

INTx interrupt signal pin (for endpoint) for output to the PCIe for function 0.

INTX_EP_F1

INTx interrupt signal pin (for endpoint) for output to the PCIe for function 1.

UI_EXTMSI_VAL0/1/2/3/4

Interrupt notification pins for output to the PCIe (for endpoint).
These are output pins for issuing an MSI specified by the user to the other-party RC.

UI_EXTMSI_VEC0/1/2/3/4 [4:0]

Interrupt vector specification pin for output to the PCIe (for endpoint).
Specifies the vector section of the MSI to be issued by UI_EXTMSI_VAL.

UI_EXTMSI_FUNC0/1/2/3/4 [2:0]

Interrupt function number specification pin for output to the PCIe (for endpoint).
Specifies the function number of the MSI to be issued by UI_EXTMSI_VAL.

52.2.4.3 Power Management Control (PMC) Pins

ALLOW_ENTER_L1

ASPM L1 state enable setting pin for output to the PCIe.

PME_TIM

PM_PME message clock pin for output to the PCIe (only for endpoint).

TURN_OFF_EVENT

PME_Turn_Off message reception flag pin supplied from the PCIe (only for endpoint).

TURN_OFF_EVENT_ACK

Acknowledge pin for output to the PCIe (only for endpoint).

D3_EVENT_F0

Non-D0 state transition request reception pin supplied from the PCIe (only for endpoint) for function 0.

D3_EVENT_F1

Non-D0 state transition request reception pin supplied from the PCIe (only for endpoint) for function 1.

D3_EVENT_ACK_F0

Acknowledge pin for output to the PCIe (only for endpoint) for function 0.

D3_EVENT_ACK_F1

Acknowledge pin for output to the PCIe (only for endpoint) for function 1.

CFG_PMCSR_PME_STATUS_F0

Power management event setting pin for output to the PCIe (only for endpoint) for function 0.

CFG_PMCSR_PME_STATUS_F1

Power management event setting pin for output to the PCIe (only for endpoint) for function 1.

CFG_PMCSR_PME_STATUS_WRITECLEAR_F0

PME_STATUS clearing pin supplied from the PCIe (only for endpoint) for function 0.

CFG_PMCSR_PME_STATUS_WRITECLEAR_F1

PME_STATUS clearing pin supplied from the PCIe (only for endpoint) for function 1.

52.2.4.4 Macro Control Pins

MODE_PORT

Device type setting pin for output to the PCIe.
This pin is for setting operation as an endpoint or root complex.

0: Endpoint (upstream port)
1: Root complex (downstream port)

CAUTION

Since the MODE_PORT pin is for determining the operating mode of the PCIe, changing the setting during PCIe operation is prohibited.
Be sure to make the setting during the PCIe reset period.

MODE_PORT_ENABLE_B

Macro off mode setting pin for output to the PCIe.
This is a disable pin for the macro including the SerDes hard macro.
By asserting this signal, input of the reference clock is disabled. This allows a minimum power consumption. The signal is fixed to 0 in normal operation.

0: Normal operation
1: Macro off

CAUTION

The macro off setting of the PCIe unit can also be made from a register of the PCIe.
When using the setting from a register of the PCIe, fix the value to 0.

PCM_LANE_SEL[1:0]

Lane setting pin for output to the PCIe when accessing PMA registers.

0x: Lane 0
1x: Lane 1

(x: Don’t care)

52.2.5 RAMA-ECC Initialization Control Pins

RAMA_VECCEN

This pin switches enabling and disabling of error correction by the ECC.

0: ECC is disabled.
1: ECC is enabled.

For details of this pin function, refer to the section of RAMA.

RAMA_INIT/RAMA_INIT_END

When RAMA_INIT is driven from low to high and CLK is input, RAMA_INIT_END changes from 0 to 1, and the data in the internal RAM and the whole area of the ECC code are initialized.
For details of this pin function, refer to the section of RAMA.

- RAMA_INIT

  0: Initialization is disabled.
  1: Initialization is enabled.

- RAMA_INIT_END

  0: Initialization is in progress (this setting only has effect while RAMA_INIT is 1).
  1: Initialization is completed.

52.2.6 MD0 to MD7 Pins

MD2 to MD0

Boot device selection pins

MD3

Boot device write interface select

MD4

Boot mode switching pin (reserved)

MD6 and MD5

Boot mode switching pins

MD7

Boot mode switching pin (reserved)

52.2.7 WDT Counting Stop Control Pins

CST_HLTDBG[1:0]

Counting Control input Pin for the WDT from the CST.
This pin controls counting by the WDT.

0: Counting by the WDT is possible.
1: Stops counting by the WDT.

WDT_CNTSTOP[1:0]

Counting Control Pin for the WDT
This pin outputs the logical OR of the values of the signal CST_HLTDBG[1:0] from the CST and the internal register WDT_CNTSTOP of the SYS.

0: Counting by the WDT is possible.
1: Stops counting by the WDT.

52.3 Register Descriptions

The following lists the registers of the SYS.

For the register base address (<SYS_S0_base >), see the section of Address Map.

52.3.1 List of Registers

The registers of the SYS are listed below.

52.3.1.1 List of Bank Address Swtiching Registers

Table 52.3-1 lists the bank address switching registers of the SYS.

Table 52.3-1 List of SYS Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
DMAA DMAC0 Bank Address Control Registers 000h-00Ch				
000h	DMAA_DMAC0 Ch0&Ch1 Bank Address Control Register	SYS_DMAA0_CH01_BANK	0000_0000h	32
004h	DMAA_DMAC0 Ch2&Ch3 Bank Address Control Register	SYS_DMAA0_CH23_BANK	0000_0000h	32
008h	DMAA_DMAC0 Ch4&Ch5 Bank Address Control Register	SYS_DMAA0_CH45_BANK	0000_0000h	32
00Ch	DMAA_DMAC0 Ch6&Ch7 Bank Address Control Register	SYS_DMAA0_CH67_BANK	0000_0000h	32
DMAA DMAC1 Bank Address Control Registers 010h-01Ch				
010h	DMAA_DMAC1 Ch0&Ch1 Bank Address Control Register	SYS_DMAA1_CH01_BANK	0000_0000h	32
014h	DMAA_DMAC1 Ch2&Ch3 Bank Address Control Register	SYS_DMAA1_CH23_BANK	0000_0000h	32
018h	DMAA_DMAC1 Ch4&Ch5 Bank Address Control Register	SYS_DMAA1_CH45_BANK	0000_0000h	32
01Ch	DMAA_DMAC1 Ch6&Ch7 Bank Address Control Register	SYS_DMAA1_CH67_BANK	0000_0000h	32
Reserved 020h-02Ch				
020h-02Ch	Reserved	—	—	—
Peripheral Block Bank Address Control Registers 030h-03Ch				
030h	Peripheral IPs 0 Bank Address Control Register	SYS_PERI0_BANK	0000_0000h	32
034h	Peripheral IPs 1 Bank Address Control Register	SYS_PERI1_BANK	0000_0000h	32
038h	DRP Bank Address Control Register	SYS_DRP_BANK	0000_0000h	32
03Ch	Reserved	—	—	—

52.3.1.2 List of PCIe-I/F Control Registers

Table 52.3-2 lists the PCIe-I/F control registers of the SYS.

Table 52.3-2 List of SYS Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
PCIe I/F Control Registers 040h-0FCh				
040h	PCI Function Level Reset request confirmation register	PCI_FLR_REQ	—	32
044h	PCI FLR execution instruction reset register*2	PCI_FLR_RST	0000_0000h	32
048h	PCI INTX control register	PCI_INTX_EP	0000_0000h	32
04Ch	PCI MSI issuing register*2	PCI_EXTMSI_VAL	0000_0000h	32
050h	PCI issued MSI setting register 0*2,*3	PCI_EXTMSI_SET0	0000_0000h	32
054h	PCI issued MSI setting register 1*2,*3	PCI_EXTMSI_SET1	0000_0000h	32
058h	PCI issued MSI setting register 2*2,*3	PCI_EXTMSI_SET2	0000_0000h	32
05Ch	PCI issued MSI setting register 3*2,*3	PCI_EXTMSI_SET3	0000_0000h	32
060h	PCI issued MSI setting register 4*2,*3	PCI_EXTMSI_SET4	0000_0000h	32
064h	PCI ASPM L1 state transition enable register*2	PCI_ALLOW_ENTER_L1	0000_0000h	32
068h	Reserved	—	—	32
06Ch	PCI PM_PME message transmission clock register	PCI_PME_TIM	0000_0000h	32
070h	PCI PME_Turn_Off message reception confirmation register	PCI_TURN_OFF_EVENT	—	32
074h	PCI turn off preparation completion register*2	PCI_TURN_OFF_EVENT_ACK	0000_0000h	32
080h	PCI non-D0 state transition request reception confirmation register	PCI_D3_EVENT	—	32
084h	PCI non-D0 state transition preparation completion notification register*2	PCI_D3_EVENT_ACK	0000_0000h	32
088h	PCI PME assertion source notification register*2	PCI_PME_STS	0000_0000h	32
08Ch	PCI PME status clearing confirmation register	PCI_PME_STS_CLR	—	32
090h	PCI device type setting register*1	PCI_MODE	0000_0000h	32
094h	PCI macro off mode setting register	PCI_MODE_EN_B	0000_0000h	32
098h-09Ch	Reserved	—	—	—
0A0h	PCI target lane setting register	PCI_LANE_SEL	0000_0000h	32
0A4h-0FCh	Reserved	—	—	—

Note 1. This register determines the operating mode of the PCIe (as endpoint or root complex). Changing the setting during PCIe operation is prohibited. Be sure to make the setting during the PCIe reset period.

Note 2. The register values are output after synchronization with the PCI_ACLK clock. Be sure to supply the PCI_ACLK clock before setting values in the registers.

Note 3. If the frequency of the PCI_ACLK clock is 48 MHz or 50 MHz, consecutive writing to the same address is prohibited (read the register value before writing a value again).

52.3.1.3 List of Device Status and RAMA Initialization Control Registers

Table 52.3-3 lists the MD pin monitor register, LSI version register, and RAMA initialization control registers of the SYS.

Table 52.3-3 List of SYS Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
MD Port Monitor Registers 100h				
100h	MD[7:0] Port Monitor Register	SYS_MD_MON	—	32
LSI Version Registers 104h				
104h	LSI Version Register	SYS_VERSION	0000_0011h	32
Reserved 108h-10Ch				
108h-10Ch	Reserved	—	—	—
RAMA ECC Initialize Control Registers 110h-17Ch-12Ch				
110h	RAMA ECC Enable Control Register	SYS_RAMA_ECC_CNT	0000_0001h	32
114h	RAMA ECC Code Region Initialization Control Register	SYS_RAMA_INIT	0000_0000h	32
118h	RAMA ECC Code Region Initialization End Flag Register	SYS_RAMA_INIT_END	—	32
11Ch-12Ch	Reserved	—	—	—

52.3.1.4 List of Registers for WDT Debugging

Table 52.3-4 is a list of registers for WDT in the SYS.

Table 52.3-4 List of SYS Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
WDT Counter Stop Control Registers 130h-1FCh				
130h	WDT Counter Stop Control Register	SYS_WDT_CNTSTOP	0000_0000h	32
134h	CST Trigger Signal Monitor Register for WDT	SYS_CST_HLTDBG_MON	—	32
138h-1FCh	Reserved	—	—	—

52.3.1.5 List of General-Purpose 32-Bit Readable/Writable Registers

Table 52.3-5 lists the general-purpose 32-bit readable/writable registers of the SYS.

Table 52.3-5 List of SYS Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
General Registers 200h-20Ch				
200h	General-purpose 32bit Read/Write Register 0	SYS_GEN_REG0	0000_0000h	32
204h	General-purpose 32bit Read/Write Register 1	SYS_GEN_REG1	0000_0000h	32
208h	General-purpose 32bit Read/Write Register 2	SYS_GEN_REG2	0000_0000h	32
20Ch	Reserved	—	—	—
Reserved 210h-21Ch				
210h-21Ch	Reserved	—	—	—

52.3.1.6 List of ICB-I/F Control Registers

Table 52.3-6 lists the SYS registers for ICB I/F control.

Table 52.3-6 List of SYS Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
ICB-I/F Control Registers 220h-2FCh				
220h	ETH AxCACHE[1](C bit) Control Register	SYS_ETH_CACHE_C_CNT	0000_0022h	32
224h-22Ch	Reserved	—	—	—
230h	OBS Count Stop Control Register for ICB	SYS_ICB_OBS_SUSP	0000_01FFh	32
Reserved 234h-2FCh				
234h-2FCh	Reserved	—	—	—

52.3.1.7 List of Temperature Sensor Reference Value Reading Registers

Table 52.3-7 lists the temperature sensor reference value reading registers of the SYS.

Table 52.3-7 List of SYS Registers

Offset Address	Register Name	Abbreviation	Initial Value	Access Unit (bits)
Temperature Sensor Reference Value Reading Registers 300h-35Ch				
300h-32C	Reserved	—	—	—
330h	TSU0 TS0_LT_DAT[11:0] Signal Monitor Register	SYS_TS0LT_DAT_MON	—	32
334h	Reserved	—	—	—
338h	TSU0 TS0_HT_DAT[11:0] Signal Monitor Register	SYS_TS0HT_DAT_MON	—	32
33Ch	Reserved	—	—	—
340h	TSU1 TS1_LT_DAT[11:0] Signal Monitor Register	SYS_TS1LT_DAT_MON	—	32
344h	Reserved	—	—	—
348h	TSU1 TS1_HT_DAT[11:0] Signal Monitor Register	SYS_TS1HT_DAT_MON	—	32
34Ch	Reserved	—	—	—
350h	TSU0/1 TS_LT_TEMP[11:0] Signal Monitor Register	SYS_TSLT_TEMP_MON	—	32
354h	Reserved	—	—	—
358h	TSU0/1 TS_HT_TEMP[11:0] Signal Monitor Register	SYS_TSHT_TEMP_MON	—	32
35Ch	Reserved	—	—	—
Reserved 360h-3FCh				
360h-3FCh	Reserved	—	—	—

52.3.2 Register Descriptions

The function description of each register is given below.

52.3.2.1 DMAA_DMAC0 Ch0&Ch1 Bank Address Control Register (SYS_DMAA0_CH01_BANK)

This register controls the bank addresses of DMAC0 ch. 0 and ch. 1.

Set the BA field to 01b or 00b.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0000h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	BA_WE[13:08]						—	—	BA_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BA[13:12]		BA[11:10]		BA[09:08]		—	—	BA[05:04]		BA[03:02]		BA[01:00]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 52.3-8 SYS_DMAA0_CH01_BANK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29 to 24	BA_WE[13:08]	Enables write to BA[13:08]. Write only. These bits are read as 0b. 0b: Invalid write to BA[13:08] 1b: Valid write to BA[13:08]
23, 22	—	Reserved. These bits are read as 0b.
21 to 16	BA_WE[05:00]	Enables write to BA[05:00]. Write only. These bits are read as 0b. 0b: Invalid write to BA[05:00] 1b: Valid write to BA[05:00]
15, 14	—	Reserved. These bits are read as 0b.
13, 12	BA[13:12]	Control DMAC_DMAC0 ch1 bank address. (Descriptor)
11, 10	BA[11:10]	Control DMAC_DMAC0 ch1 bank address. (Destination)
9, 8	BA[09:08]	Control DMAC_DMAC0 ch1 bank address. (Source)
7, 6	—	Reserved. These bits are read as 0b.
5, 4	BA[05:04]	Control DMAC_DMAC0 ch0 bank address. (Descriptor)
3, 2	BA[03:02]	Control DMAC_DMAC0 ch0 bank address. (Destination)
1, 0	BA[01:00]	Control DMAC_DMAC0 ch0 bank address. (Source)

52.3.2.2 DMAA_DMAC0 Ch2&Ch3 Bank Address Control Register (SYS_DMAA0_CH23_BANK)

This register controls the bank addresses of DMAC0 ch. 2 and ch. 3.

Set the BA field to 01b or 00b.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0004h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	BA_WE[13:08]						—	—	BA_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BA[13:12]		BA[11:10]		BA[09:08]		—	—	BA[05:04]		BA[03:02]		BA[01:00]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 52.3-9 SYS_DMAA0_CH23_BANK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29 to 24	BA_WE[13:08]	Enables write to BA[13:08]. Write only. These bits are read as 0b. 0b: Invalid write to BA[13:08] 1b: Valid write to BA[13:08]
23, 22	—	Reserved. These bits are read as 0b.
21 to 16	BA_WE[05:00]	Enables write to BA[05:00]. Write only. These bits are read as 0b. 0b: Invalid write to BA[05:00] 1b: Valid write to BA[05:00]
15, 14	—	Reserved. These bits are read as 0b.
13, 12	BA[13:12]	Control DMAC_DMAC0 ch3 bank address. (Descriptor)
11, 10	BA[11:10]	Control DMAC_DMAC0 ch3 bank address. (Destination)
9, 8	BA[09:08]	Control DMAC_DMAC0 ch3 bank address. (Source)
7, 6	—	Reserved. These bits are read as 0b.
5, 4	BA[05:04]	Control DMAC_DMAC0 ch2 bank address. (Descriptor)
3, 2	BA[03:02]	Control DMAC_DMAC0 ch2 bank address. (Destination)
1, 0	BA[01:00]	Control DMAC_DMAC0 ch2 bank address. (Source)

52.3.2.3 DMAA_DMAC0 Ch4&Ch5 Bank Address Control Register (SYS_DMAA0_CH45_BANK)

This register controls the bank addresses of DMAC0 ch. 4 and ch. 5.

Set the BA field to 01b or 00b.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0008h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	BA_WE[13:08]						—	—	BA_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BA[13:12]		BA[11:10]		BA[09:08]		—	—	BA[05:04]		BA[03:02]		BA[01:00]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 52.3-10 SYS_DMAA0_CH45_BANK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29 to 24	BA_WE[13:08]	Enables write to BA[13:08]. Write only. These bits are read as 0b. 0b: Invalid write to BA[13:08] 1b: Valid write to BA[13:08]
23, 22	—	Reserved. These bits are read as 0b.
21 to 16	BA_WE[05:00]	Enables write to BA[05:00]. Write only. These bits are read as 0b. 0b: Invalid write to BA[05:00] 1b: Valid write to BA[05:00]
15, 14	—	Reserved. These bits are read as 0b.
13, 12	BA[13:12]	Control DMAC_DMAC0 ch5 bank address. (Descriptor)
11, 10	BA[11:10]	Control DMAC_DMAC0 ch5 bank address. (Destination)
9, 8	BA[09:08]	Control DMAC_DMAC0 ch5 bank address. (Source)
7, 6	—	Reserved. These bits are read as 0b.
5, 4	BA[05:04]	Control DMAC_DMAC0 ch4 bank address. (Descriptor)
3, 2	BA[03:02]	Control DMAC_DMAC0 ch4 bank address. (Destination)
1, 0	BA[01:00]	Control DMAC_DMAC0 ch4 bank address. (Source)

52.3.2.4 DMAA_DMAC0 Ch6&Ch7 Bank Address Control Register (SYS_DMAA0_CH67_BANK)

This register controls the bank addresses of DMAC0 ch. 6 and ch. 7.

Set the BA field to 01b or 00b.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 000Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	BA_WE[13:08]						—	—	BA_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BA[13:12]		BA[11:10]		BA[09:08]		—	—	BA[05:04]		BA[03:02]		BA[01:00]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 52.3-11 SYS_DMAA0_CH67_BANK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29 to 24	BA_WE[13:08]	Enables write to BA[13:08]. Write only. These bits are read as 0b. 0b: Invalid write to BA[13:08] 1b: Valid write to BA[13:08]
23, 22	—	Reserved. These bits are read as 0b.
21 to 16	BA_WE[05:00]	Enables write to BA[05:00]. Write only. These bits are read as 0b. 0b: Invalid write to BA[05:00] 1b: Valid write to BA[05:00]
15, 14	—	Reserved. These bits are read as 0b.
13, 12	BA[13:12]	Control DMAC_DMAC0 ch7 bank address. (Descriptor)
11, 10	BA[11:10]	Control DMAC_DMAC0 ch7 bank address. (Destination)
9, 8	BA[09:08]	Control DMAC_DMAC0 ch7 bank address. (Source)
7, 6	—	Reserved. These bits are read as 0b.
5, 4	BA[05:04]	Control DMAC_DMAC0 ch6 bank address. (Descriptor)
3, 2	BA[03:02]	Control DMAC_DMAC0 ch6 bank address. (Destination)
1, 0	BA[01:00]	Control DMAC_DMAC0 ch6 bank address. (Source)

52.3.2.5 DMAA_DMAC1 Ch0&Ch1 Bank Address Control Register (SYS_DMAA1_CH01_BANK)

This register controls the bank addresses of DMAC1 ch. 0 and ch. 1.

Set the BA field to 01b or 00b.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0010h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	BA_WE[13:08]						—	—	BA_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BA[13:12]		BA[11:10]		BA[09:08]		—	—	BA[05:04]		BA[03:02]		BA[01:00]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 52.3-12 SYS_DMAA1_CH01_BANK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29 to 24	BA_WE[13:08]	Enables write to BA[13:08]. Write only. These bits are read as 0b. 0b: Invalid write to BA[13:08] 1b: Valid write to BA[13:08]
23, 22	—	Reserved. These bits are read as 0b.
21 to 16	BA_WE[05:00]	Enables write to BA[05:00]. Write only. These bits are read as 0b. 0b: Invalid write to BA[05:00] 1b: Valid write to BA[05:00]
15, 14	—	Reserved. These bits are read as 0b.
13, 12	BA[13:12]	Control DMAC_DMAC1 ch1 bank address. (Descriptor)
11, 10	BA[11:10]	Control DMAC_DMAC1 ch1 bank address. (Destination)
9, 8	BA[09:08]	Control DMAC_DMAC1 ch1 bank address. (Source)
7, 6	—	Reserved. These bits are read as 0b.
5, 4	BA[05:04]	Control DMAC_DMAC1 ch0 bank address. (Descriptor)
3, 2	BA[03:02]	Control DMAC_DMAC1 ch0 bank address. (Destination)
1, 0	BA[01:00]	Control DMAC_DMAC1 ch0 bank address. (Source)

52.3.2.6 DMAA_DMAC1 Ch2&Ch3 Bank Address Control Register (SYS_DMAA1_CH23_BANK)

This register controls the bank addresses of DMAC1 ch. 2 and ch. 3.

Set the BA field to 01b or 00b.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0014h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	BA_WE[13:08]						—	—	BA_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BA[13:12]		BA[11:10]		BA[09:08]		—	—	BA[05:04]		BA[03:02]		BA[01:00]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 52.3-13 SYS_DMAA1_CH23_BANK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29 to 24	BA_WE[13:08]	Enables write to BA[13:08]. Write only. These bits are read as 0b. 0b: Invalid write to BA[13:08] 1b: Valid write to BA[13:08]
23, 22	—	Reserved. These bits are read as 0b.
21 to 16	BA_WE[05:00]	Enables write to BA[05:00]. Write only. These bits are read as 0b. 0b: Invalid write to BA[05:00] 1b: Valid write to BA[05:00]
15, 14	—	Reserved. These bits are read as 0b.
13, 12	BA[13:12]	Control DMAC_DMAC1 ch3 bank address. (Descriptor)
11, 10	BA[11:10]	Control DMAC_DMAC1 ch3 bank address. (Destination)
9, 8	BA[09:08]	Control DMAC_DMAC1 ch3 bank address. (Source)
7, 6	—	Reserved. These bits are read as 0b.
5, 4	BA[05:04]	Control DMAC_DMAC1 ch2 bank address. (Descriptor)
3, 2	BA[03:02]	Control DMAC_DMAC1 ch2 bank address. (Destination)
1, 0	BA[01:00]	Control DMAC_DMAC1 ch2 bank address. (Source)

52.3.2.7 DMAA_DMAC1 Ch4&Ch5 Bank Address Control Register (SYS_DMAA1_CH45_BANK)

This register controls the bank addresses of DMAC1 ch. 4 and ch. 5.

Set the BA field to 01b or 00b.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0018h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	BA_WE[13:08]						—	—	BA_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BA[13:12]		BA[11:10]		BA[09:08]		—	—	BA[05:04]		BA[03:02]		BA[01:00]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 52.3-14 SYS_DMAA1_CH45_BANK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29 to 24	BA_WE[13:08]	Enables write to BA[13:08]. Write only. These bits are read as 0b. 0b: Invalid write to BA[13:08] 1b: Valid write to BA[13:08]
23, 22	—	Reserved. These bits are read as 0b.
21 to 16	BA_WE[05:00]	Enables write to BA[05:00]. Write only. These bits are read as 0b. 0b: Invalid write to BA[05:00] 1b: Valid write to BA[05:00]
15, 14	—	Reserved. These bits are read as 0b.
13, 12	BA[13:12]	Control DMAC_DMAC1 ch5 bank address. (Descriptor)
11, 10	BA[11:10]	Control DMAC_DMAC1 ch5 bank address. (Destination)
9, 8	BA[09:08]	Control DMAC_DMAC1 ch5 bank address. (Source)
7, 6	—	Reserved. These bits are read as 0b.
5, 4	BA[05:04]	Control DMAC_DMAC1 ch4 bank address. (Descriptor)
3, 2	BA[03:02]	Control DMAC_DMAC1 ch4 bank address. (Destination)
1, 0	BA[01:00]	Control DMAC_DMAC1 ch4 bank address. (Source)

52.3.2.8 DMAA_DMAC1 Ch6&Ch7 Bank Address Control Register (SYS_DMAA1_CH67_BANK)

This register controls the bank addresses of DMAC1 ch. 6 and ch. 7.

Set the BA field to 01b or 00b.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 001Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	BA_WE[13:08]						—	—	BA_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BA[13:12]		BA[11:10]		BA[09:08]		—	—	BA[05:04]		BA[03:02]		BA[01:00]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 52.3-15 SYS_DMAA1_CH67_BANK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29 to 24	BA_WE[13:08]	Enables write to BA[13:08]. Write only. These bits are read as 0b. 0b: Invalid write to BA[13:08] 1b: Valid write to BA[13:08]
23, 22	—	Reserved. These bits are read as 0b.
21 to 16	BA_WE[05:00]	Enables write to BA[05:00]. Write only. These bits are read as 0b. 0b: Invalid write to BA[05:00] 1b: Valid write to BA[05:00]
15, 14	—	Reserved. These bits are read as 0b.
13, 12	BA[13:12]	Control DMAC_DMAC1 ch7 bank address. (Descriptor)
11, 10	BA[11:10]	Control DMAC_DMAC1 ch7 bank address. (Destination)
9, 8	BA[09:08]	Control DMAC_DMAC1 ch7 bank address. (Source)
7, 6	—	Reserved. These bits are read as 0b.
5, 4	BA[05:04]	Control DMAC_DMAC1 ch6 bank address. (Descriptor)
3, 2	BA[03:02]	Control DMAC_DMAC1 ch6 bank address. (Destination)
1, 0	BA[01:00]	Control DMAC_DMAC1 ch6 bank address. (Source)

52.3.2.9 Peripheral IPs 0 Bank Address Control Register (SYS_PERI0_BANK)

This register controls the bank addresses of the IPs for ICB.

Set the BA field to 01b or 00b.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0030h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	BA_WE[13:08]						—	—	BA_WE[05:00]					
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BA[13:12]		BA[11:10]		BA[09:08]		—	—	BA[05:04]		BA[03:02]		BA[01:00]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

Table 52.3-16 SYS_PERI0_BANK Register Contents

Bit Position	Bit Name	Description
31, 30	—	Reserved. These bits are read as 0b.
29 to 24	BA_WE[13:08]	Enables write to BA[13:08]. Write only. These bits are read as 0b. 0b: Invalid write to BA[13:08] 1b: Valid write to BA[13:08]
23, 22	—	Reserved. These bits are read as 0b.
21 to 16	BA_WE[05:00]	Enables write to BA[05:00]. Write only. These bits are read as 0b. 0b: Invalid write to BA[05:00] 1b: Valid write to BA[05:00]
15, 14	—	Reserved. These bits are read as 0b.
13, 12	BA[13:12]	Control PCIe bank address.
11, 10	BA[11:10]	Control USB Peri bank address.
9, 8	BA[09:08]	Control USB Host bank address.
7, 6	—	Reserved. These bits are read as 0b.
5, 4	BA[05:04]	Control SDI1 bank address.
3, 2	BA[03:02]	Control SDI0 bank address.
1, 0	BA[01:00]	Control eMMC bank address.

52.3.2.10 Peripheral IPs 1 Bank Address Control Register (SYS_PERI1_BANK)

This register controls the bank addresses of the IPs for ICB.

Set the BA field to 01b or 00b.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0034

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	BA_WE[11:10]		—	—	BA_WE[07:06]		—	—	—	—	BA_WE[01:00]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R0W1	R0W1	R	R	R0W1	R0W1	R	R	R	R	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	BA[11:10]		—	—	BA[07:06]		—	—	—	—	BA[01:00]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	RW	RW	R	R	RW	RW	R	R	R	R	RW	RW

Table 52.3-17 SYS_PERI1_BANK Register Contents

Bit Position	Bit Name	Description
31 to 28	—	Reserved. These bits are read as 0b.
27, 26	BA_WE[11:10]	Enables write to BA[11:10]. Write only. These bits are read as 0b. 0b: Invalid write to BA[11:10] 1b: Valid write to BA[11:10]
25, 24	—	Reserved. These bits are read as 0b.
23, 22	BA_WE[07:06]	Enables write to BA[07:06]. Write only. These bits are read as 0b. 0b: Invalid write to BA[07:06] 1b: Valid write to BA[07:06]
21 to 18	—	Reserved. These bits are read as 0b.
17, 16	BA_WE[01:00]	Enables write to BA[01:00]. Write only. These bits are read as 0b. 0b: Invalid write to BA[01:00] 1b: Valid write to BA[01:00]
15 to 12	—	Reserved. These bits are read as 0b.
11, 10	BA[11:10]	Control VCD bank address.
9, 8	—	Reserved. These bits are read as 0b.
7, 6	BA[07:06]	Control GRP bank address.
5 to 2	—	Reserved. These bits are read as 0b.
1, 0	BA[01:00]	Control ETHER bank address.

52.3.2.11 DRP Bank Address Control Register (SYS_DRP_BANK)

This register controls the bank addresses of DRP for ICB.

Set the BA field to 01b or 00b.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0038h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	BA_WE[07:00]							
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	BA[07:06]		BA[05:04]		BA[03:02]		BA[01:00]	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 52.3-18 SYS_DRP_BANK Register Contents

Bit Position	Bit Name	Description
31 to 26	—	Reserved. These bits are read as 0b.
25, 24	—	Reserved. These bits are read as 0b. The write value should always be 0b.
23 to 16	BA_WE[09:00]	Enables write to BA[09:00]. Write only. These bits are read as 0b. 0b: Invalid write to BA[01:00] 1b: Valid write to BA[01:00]
15 to 10	—	Reserved. These bits are read as 0b.
9, 8	—	Reserved. When read, the value read is undefined. Since these bits are for use with the ISP support package, writing to these bits is prohibited.
7, 6	BA[07:06]	Control DRP-AI M3 bank address.
5, 4	BA[05:04]	Control DRP-AI M2 bank address.
3, 2	BA[03:02]	Control DRP-AI M1 bank address.
1, 0	BA[01:00]	Control DRP-AI M0 bank address.

52.3.2.12 PCI Function Level Reset Request Confirmation Register (PCI_FLR_REQ)

This register is for monitoring to check the FLR_REQ pin (Function Level Reset (FLR) request) supplied from the PCIe.

Writing to this register has no effect.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0040h

Initial Value: 0000_000xh (The initial value of the LSB two bits depends on the state of the FLR request signal.)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FLR_REQ	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-19 PCI_FLR_REQ Register Contents

Bit Position	Bit Name	Description
31 to 2	Reserved	These bits are always read as 0.
1	FLR_REQ[1]	Function Level Reset request (function 1) 0b: No request is present. 1b: A request is present.
0	FLR_REQ[0]	Function Level Reset request (function 0) 0b: No request is present. 1b: A request is present.

52.3.2.13 PCI FLR Execution Instruction Reset Register (PCI_FLR_RST)

This register controls the FLR_RESET pin (Function Level Reset execution instruction) for output to the PCIe.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0044h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FLR_RESET	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Table 52.3-20 PCI_FLR_RST Register Contents

Bit Position	Bit Name	Description
31 to 2	Reserved	These bits are always read as 0.
1	FLR_RESET[1]	Reset output for the Function Level Reset execution instruction (function 1) 0b: Release from the reset 1b: Reset
0	FLR_RESET[0]	Reset output for the Function Level Reset execution instruction (function 0) 0b: Release from the reset 1b: Reset

NOTE

The value of this register is output from the FLR_RESET[1:0] pin after synchronization with the AXI clock (PCI_ACLK) of the PCIe. Therefore, the register value is not reflected in the FLR_RESET[1:0] pin while the AXI clock of the PCIe is stopped. It is reflected in the FLR_RESET[1:0] pin after operation of the AXI clock of the PCIe.

52.3.2.14 PCI INTX Control Register (PCI_INTX_EP)

This register controls the INTX pins (INTX_EP_F0 and INTX_EP_F1) for output to the PCIe.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0048h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	INTX_F1	—	—	—	INTX_F0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	R	R	R	RW

Table 52.3-21 PCI_INTX_EP Register Contents

Bit Position	Bit Name	Description
31 to 5	Reserved	These bits are always read as 0b.
4	INTX_F1	INTX output control for function 1
3 to 1	Reserved	These bits are always read as 0b.
0	INTX_F0	INTX output control for function 0

52.3.2.15 PCI MSI Issuing Register (PCI_EXTMSI_VAL)

This register controls the MSI interrupt notification pins (UI_EXTMSI_VAL0/1/2/3/4) for output to the PCIe.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 004Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VAL4
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	VAL3	—	—	—	VAL2	—	—	—	VAL1	—	—	—	VAL0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	RW	R	R	R	RW	R	R	R	RW	R	R	R	RW

Table 52.3-22 PCI_EXTMSI_VAL Register Contents

Bit Position	Bit Name	Description
31 to 17	Reserved	These bits are always read as 0b.
16	VAL4	MSI interrupt notification 4 Controls the output value on the UI_EXTMSI_VAL4 pin.
15 to 13	Reserved	These bits are always read as 0b.
12	VAL3	MSI interrupt notification 3 Controls the output value on the UI_EXTMSI_VAL3 pin.
11 to 9	Reserved	These bits are always read as 0b.
8	VAL2	MSI interrupt notification 2 Controls the output value on the UI_EXTMSI_VAL2 pin.
7 to 5	Reserved	These bits are always read as 0b.
4	VAL1	MSI interrupt notification 1 Controls the output value on the UI_EXTMSI_VAL1 pin.
3 to 1	Reserved	These bits are always read as 0b.
0	VAL0	MSI interrupt notification 0 Controls the output value on the UI_EXTMSI_VAL0 pin.

NOTE

The value of this register is output from the UI_EXTMSI_VAL4/3/2/1/0 pin after synchronization with the AXI clock (PCI_ACLK) of the PCIe. Therefore, the register value is not reflected in the UI_EXTMSI_VAL4/3/2/1/0 pin while the AXI clock of the PCIe is stopped. It is reflected in the UI_EXTMSI_VAL4/3/2/1/0 pin after operation of the AXI clock of the PCIe.

52.3.2.16 PCI Issued MSI Setting Register 0 (PCI_EXTMSI_SET0)

This register controls the pins for UI_EXTMSI_VAL0 (UI_EXTMSI_VEC0 and UI_EXTMSI_FUNC0) for output to the PCIe.

CAUTION

The value of this register is output from the UI_EXTMSI_FUNC0[2:0] or UI_EXTMSI_VEC0[4:0] pin after synchronization with the AXI clock (PCI_ACLK) of the PCIe. Therefore, writing to this register is prohibited while PCI_ACLK is stopped. When writing to this register, only do so while PCI_ACLK is operating.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0050h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	FUNC			—	—	—	VEC				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	RW	RW	R	R	R	RW	RW	RW	RW	RW

Table 52.3-23 PCI_EXTMSI_SET0 Register Contents

Bit Position	Bit Name	Description
31 to 11	Reserved	These bits are always read as 0b.
10 to 8	FUNC[2:0]	Specifying the function number of MSI (0 or 1) Controls the output value on the UI_EXTMSI_FUNC0[2:0] pin.
7 to 5	Reserved	These bits are always read as 0b.
4 to 0	VEC[4:0]	Specifying the vector value of MSI Controls the output value on the UI_EXTMSI_VEC0[4:0] pin.

52.3.2.17 PCI Issued MSI Setting Register 1 (PCI_EXTMSI_SET1)

This register controls the pins for UI_EXTMSI_VAL1 (UI_EXTMSI_VEC1 and UI_EXTMSI_FUNC1) for output to the PCIe.

CAUTION

The value of this register is output from the UI_EXTMSI_FUNC1[2:0] or UI_EXTMSI_VEC1[4:0] pin after synchronization with the AXI clock (PCI_ACLK) of the PCIe. Therefore, writing to this register is prohibited while PCI_ACLK is stopped. When writing to this register, only do so while PCI_ACLK is operating.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0054h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	FUNC			—	—	—	VEC				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	RW	RW	R	R	R	RW	RW	RW	RW	RW

Table 52.3-24 PCI_EXTMSI_SET1 Register Contents

Bit Position	Bit Name	Description
31 to 11	Reserved	These bits are always read as 0b.
10 to 8	FUNC[2:0]	Specifying the function number of MSI (0 or 1) Controls the output value on the UI_EXTMSI_FUNC1[2:0] pin.
7 to 5	Reserved	These bits are always read as 0b.
4 to 0	VEC[4:0]	Specifying the vector value of MSI Controls the output value on the UI_EXTMSI_VEC1[4:0] pin.

52.3.2.18 PCI Issued MSI Setting Register 2 (PCI_EXTMSI_SET2)

This register controls the pins for UI_EXTMSI_VAL2 (UI_EXTMSI_VEC2 and UI_EXTMSI_FUNC2) for output to the PCIe.

CAUTION

The value of this register is output from the UI_EXTMSI_FUNC2[2:0] or UI_EXTMSI_VEC2[4:0] pin after synchronization with the AXI clock (PCI_ACLK) of the PCIe. Therefore, writing to this register is prohibited while PCI_ACLK is stopped. When writing to this register, only do so while PCI_ACLK is operating.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0058h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	FUNC			—	—	—	VEC				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	RW	RW	R	R	R	RW	RW	RW	RW	RW

Table 52.3-25 PCI_EXTMSI_SET2 Register Contents

Bit Position	Bit Name	Description
31 to 11	Reserved	These bits are always read as 0b.
10 to 8	FUNC[2:0]	Specifying the function number of MSI (0 or 1) Controls the output value on the UI_EXTMSI_FUNC2[2:0] pin.
7 to 5	Reserved	These bits are always read as 0b.
4 to 0	VEC[4:0]	Specifying the vector value of MSI Controls the output value on the UI_EXTMSI_VEC2[4:0] pin.

52.3.2.19 PCI Issued MSI Setting Register 3 (PCI_EXTMSI_SET3)

This register controls the pins for UI_EXTMSI_VAL3 (UI_EXTMSI_VEC3 and UI_EXTMSI_FUNC3) for output to the PCIe.

CAUTION

The value of this register is output from the UI_EXTMSI_FUNC3[2:0] or UI_EXTMSI_VEC3[4:0] pin after synchronization with the AXI clock (PCI_ACLK) of the PCIe. Therefore, writing to this register is prohibited while PCI_ACLK is stopped. When writing to this register, only do so while PCI_ACLK is operating.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 005Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	FUNC			—	—	—	VEC				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	RW	RW	R	R	R	RW	RW	RW	RW	RW

Table 52.3-26 PCI_EXTMSI_SET3 Register Contents

Bit Position	Bit Name	Description
31 to 11	Reserved	These bits are always read as 0b.
10 to 8	FUNC[2:0]	Specifying the function number of MSI (0 or 1) Controls the output value on the UI_EXTMSI_FUNC3[2:0] pin.
7 to 5	Reserved	These bits are always read as 0b.
4 to 0	VEC[4:0]	Specifying the vector value of MSI Controls the output value on the UI_EXTMSI_VEC3[4:0] pin.

52.3.2.20 PCI Issued MSI Setting Register 4 (PCI_EXTMSI_SET4)

This register controls the pins for UI_EXTMSI_VAL4 (UI_EXTMSI_VEC4 and UI_EXTMSI_FUNC4) for output to the PCIe.

CAUTION

The value of this register is output from the UI_EXTMSI_FUNC4[2:0] or UI_EXTMSI_VEC4[4:0] pin after synchronization with the AXI clock (PCI_ACLK) of the PCIe. Therefore, writing to this register is prohibited while PCI_ACLK is stopped. When writing to this register, only do so while PCI_ACLK is operating.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0060h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	FUNC			—	—	—	VEC				
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	RW	RW	RW	R	R	R	RW	RW	RW	RW	RW

Table 52.3-27 PCI_EXTMSI_SET4 Register Contents

Bit Position	Bit Name	Description
31 to 11	Reserved	These bits are always read as 0b.
10 to 8	FUNC[2:0]	Specifying the function number of MSI (0 or 1) Controls the output value on the UI_EXTMSI_FUNC4[2:0] pin.
7 to 5	Reserved	These bits are always read as 0b.
4 to 0	VEC[4:0]	Specifying the vector value of MSI Controls the output value on the UI_EXTMSI_VEC4[4:0] pin.

52.3.2.21 PCI ASPM L1 State Transition Enable Register (PCI_ALLOW_ENTER_L1)

This register controls the ASPM L1 state enable setting pin (ALLOW_ENTER_L1) for output to the PCIe.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0064h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 52.3-28 PCI_ALLOW_ENTER_L1 Register Contents

Bit Position	Bit Name	Description
31 to 1	Reserved	These bits are always read as 0b.
0	EN	0b: Controls transition from ASPM L0 to the ASPM L1 state. 1b: Enables transition from ASPM L0 to the ASPM L1 state.

NOTE

The value of this register is output from the ALLOW_ENTER_L1 pin after synchronization with the AXI clock (PCI_ACLK) of the PCIe. Therefore, the register value is not reflected in the ALLOW_ENTER_L1 pin while the AXI clock of the PCIe is stopped. It is reflected in the ALLOW_ENTER_L1 pin after operation of the AXI clock of the PCIe.

52.3.2.22 PCI PM_PME Message Transmission Clock Register (PCI_PME_TIM)

This register controls the PM_PME message transmission clock pin (PME_TIM) for output to the PCIe.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 006Ch

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PME_TIM
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 52.3-29 PCI_PME_TIM Register Contents

Bit Position	Bit Name	Description
31 to 1	Reserved	These bits are always read as 0b.
0	PME_TIM	Controls the PM_PME message transmission clock pin.

52.3.2.23 PCI PME_Turn_Off Message Reception Confirmation Register (PCI_TURN_OFF_EVENT)

This register is for monitoring the PME_Turn_Off message reception notification flag confirmation pin (TURN_OFF_EVENT) supplied from the PCIe.

Writing to this register has no effect.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0070h

Initial Value: 0000_000xh (The initial value of the LSB one bit depends on the PME_Turn_Off message reception notification flag.)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FLG
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-30 PCI_TURN_OFF_EVENT Register Contents

Bit Position	Bit Name	Description
31 to 1	Reserved	These bits are always read as 0b.
0	FLG	PME_Turn_Off message reception notification flag

52.3.2.24 PCI Turn Off Preparation Completion Register (PCI_TURN_OFF_EVENT_ACK)

This register controls the turn off preparation completion notification pin (TURN_OFF_EVENT_ACK) for output to the PCIe.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0074h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ACK
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 52.3-31 PCI_TURN_OFF_EVENT_ACK Register Contents

Bit Position	Bit Name	Description
31 to 1	Reserved	These bits are always read as 0b.
0	ACK	Notifying the completion of preparation for PME_Turn_Off.

NOTE

The value of this register is output from the TURN_OFF_EVENT_ACK pin after synchronization with the AXI clock (PCI_ACLK) of the PCIe. Therefore, the register value is not reflected in the TURN_OFF_EVENT_ACK pin while the AXI clock of the PCIe is stopped. It is reflected in the TURN_OFF_EVENT_ACK pin after operation of the AXI clock of the PCIe.

52.3.2.25 PCI Non-D0 State Transition Request Reception Confirmation Register (PCI_D3_EVENT)

This register is for monitoring the non-D0 state transition request reception notification flag confirmation pins ((D3_EVENT_F0/1) supplied from the PCIe.

Writing to this register has no effect.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0080h

Initial Value: 0000_00xxh (The initial value of bit 0 and bit 4 depends on the non-D0 state transition request reception notification flag.)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	F1	—	—	—	F0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	—	0	0	0	—
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-32 PCI_D3_EVENT Register Contents

Bit Position	Bit Name	Description
31 to 5	Reserved	These bits are always read as 0b.
4	F1	Non-D0 state transition request reception notification flag for function 1
3 to 1	Reserved	These bits are always read as 0b.
0	F0	Non-D0 state transition request reception notification flag for function 0

52.3.2.26 PCI Non-D0 State Transition Preparation Completion Notification Register

This register controls the pins which notify the completion of preparation for a power state transition (D3_EVENT_ACK_F0/1) for output to the PCIe.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0084h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	F1	—	—	—	F0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	R	R	R	RW

Table 52.3-33 PCI_D3_EVENT_ACK Register Contents

Bit Position	Bit Name	Description
31 to 5	Reserved	These bits are always read as 0b.
4	F1	Non-D0 state transition request reception notification flag for function 1
3 to 1	Reserved	These bits are always read as 0b.
0	F0	Non-D0 state transition request reception notification flag for function 0

NOTE

The value of this register is output from the D3_EVENT_ACK_F1/0 pin after synchronization with the AXI clock (PCI_ACLK) of the PCIe. Therefore, the register value is not reflected in the D3_EVENT_ACK_F1/0 pin while the AXI clock of the PCIe is stopped. It is reflected in the D3_EVENT_ACK_F1/0 pin after operation of the AXI clock of the PCIe.

52.3.2.27 PCI PME Assertion Source Notification Register (PCI_PME_STS)

This register controls the power management event setting pins (CFG_PMCSR_PME_STATUS_F0/1) for output to the PCIe.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0088h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	F1	—	—	—	F0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	RW	R	R	R	RW

Table 52.3-34 PCI_PME_STS Register Contents

Bit Position	Bit Name	Description
31 to 5	Reserved	These bits are always read as 0b.
4	F1	Controls the Power Management Event setting pin for function 1.
3 to 1	Reserved	These bits are always read as 0b.
0	F0	Controls the Power Management Event setting pin for function 0.

NOTE

The value of this register is output from the CFG_PMCSR_PME_STATUS_F1/0 pin after synchronization with the AXI clock (PCI_ACLK) of the PCIe. Therefore, the register value is not reflected in the CFG_PMCSR_PME_STATUS_F1/0 pin while the AXI clock of the PCIe is stopped. It is reflected in the CFG_PMCSR_PME_STATUS_F1/0 pin after operation of the AXI clock of the PCIe.

52.3.2.28 PCI PME Status Clearing Confirmation Register (PCI_PME_STS_CLR)

This register is for monitoring the ME_STATUS clearing flag confirmation pins (CFG_PMCSR_PME_STATUS_WRITECLEAR_F0/1) supplied from the PCIe.

Writing to this register has no effect.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 008Ch

Initial Value: 0000_00xxh (The initial value of bit 0 and bit 4 depends on the PME_STATUS clearing flag.)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	F1	—	—	—	F0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	—	0	0	0	—
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-35 PCI_PME_STS_CLR Register Contents

Bit Position	Bit Name	Description
31 to 5	Reserved	These bits are always read as 0b.
4	F1	PME_STATUS clearing flag for function 1
3 to 1	Reserved	These bits are always read as 0b.
0	F0	PME_STATUS clearing flag for function 0

52.3.2.29 PCI Device Type Setting Register (PCI_MODE)

This register controls the device type setting pin (MODE_PORT) for output to the PCIe.

CAUTION

Since this register is for determining the operating mode of the PCIe, changing the setting during PCIe operation is prohibited.
Be sure to make the setting during the PCIe reset period.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0090h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TYPE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 52.3-36 PCI_MODE Register Contents

Bit Position	Bit Name	Description
31 to 1	Reserved	These bits are always read as 0b.
0	TYPE	Device type setting 0b: Endpoint 1b: Root complex

52.3.2.30 PCI Macro Off Mode Setting Register (PCI_MODE_EN_B)

This register controls the macro off mode setting pin (MODE_PORT_ENABLE_B) for output to the PCIe.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0094h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EN_B
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 52.3-37 PCI_MODE_EN_B Register Contents

Bit Position	Bit Name	Description
31 to 1	Reserved	These bits are always read as 0b.
0	EN_B	Macro off mode setting 0b: Normal operation 1b: Macro off

CAUTION

The macro off setting of the PCIe unit can also be made from a register of the PCIe.
When using the setting from a register of the PCIe, fix the value to 0b.

52.3.2.31 PCI Target Lane Setting Register (PCI_LANE_SEL)

This register controls the output target lane setting pin (PCI_LANE_SEL). The value of the SEL bit is notified to the PCIe via the PCI_LANE_SEL pin.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 00A0h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SEL	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW

Table 52.3-38 PCI_LANE_SEL Register Contents

Bit Position	Bit Name	Description
31 to 2	Reserved	These bits are always read as 0b.
1, 0	SEL	Target lane setting when accessing PMA registers (400h-7FFh) 0xb: Lane 0 1xb: Lane 1 (x: Don't care) Set these bits before accessing PCI PMA registers (400-7FFh).

52.3.2.32 MD[7:0] Port Monitor Register (SYS_MD_MON)

This register a read-only register that monitors the MD7 to MD0 pins. Writing to this register has no effect.

The initial value is determined by the state of the MD7 to MD0 pins.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0100h

Initial Value: 0000_00xxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0
Initial Value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-39 SYS_MD_MON Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7	MD7	MD7 pin monitoring
6	MD6	MD6 pin monitoring
5	MD5	MD5 pin monitoring
4	MD4	MD4 pin monitoring
3	MD3	MD3 pin monitoring
2	MD2	MD2 pin monitoring
1	MD1	MD1 pin monitoring
0	MD0	MD0 pin monitoring

52.3.2.33 LSI Version Register (SYS_VERSION)

This register indicates the version number of the LSI. Writing to this register has no effect.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0104h

Initial Value: 0000_0011h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MAJOR[3:0]				MINOR[3:0]			
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-40 SYS_VERSION Register Contents

Bit Position	Bit Name	Description
31 to 8	—	Reserved. These bits are read as 0b.
7 to 4	MAJOR[3:0]	LSI major version number
3 to 0	MINOR[3:0]	LSI minor version number

52.3.2.34 RAMA ECC Enable Control Register (SYS_RAMA_ECC_CNT)

This register controls the ECC of RAMA.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0110h

Initial Value: 0000_0001h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	RW	R	R	R	R	R	R	R	RW

Table 52.3-41 SYS_RAMA_ECC_CNT Register Contents

Bit Position	Bit Name	Description
31 to 9	—	Reserved. These bits are read as 0b.
8	—	Reserved. When read, the value read is undefined. The write calue should always be 0b.
7 to 1	—	Reserved. These bits are read as 0b.
0	EN	Setting whether RAMA ECC is enabled or disabled. 0b: ECC is disabled. 1b: ECC is enabled. The value of this bit is notified to VECCEN pin of the RAMA via RAMA_VECCEN pin.

52.3.2.35 RAMA ECC Code Region Initialization Control Register (SYS_RAMA_INIT)

This register initializes the RAMA ECC code region.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0114h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INIT
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Table 52.3-42 SYS_RAMA_INIT Register Contents

Bit Position	Bit Name	Description
31 to 1	—	Reserved. These bits are read as 0b.
0	INIT	RAMA ECC code region initialization control 0b: Initialization is disabled. 1b: Initialization is enabled. The value of this bit is notified to RAM_INIT pin of the RAMA via RAMA_INIT pin.

52.3.2.36 RAMA ECC Code Region Initialization End Flag Register (SYS_RAMA_INIT_END)

This register is a read-only register that indicates the end of initialization of the RAMA ECC code region. Writing to this register has no effect.

The initial value of the LSB one bit is determined by the state of the RAMA ECC code region initialization end flag.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0118h

Initial Value: 0000_000xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	END
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-43 SYS_RAMA_INIT_END Register Contents

Bit Position	Bit Name	Description
31 to 1	—	Reserved. These bits are read as 0b.
0	END	RAMA ECC code region initialization end flag 0b: Initializing (this setting has only effect if RAM_INIT is 1b). 1b: Initialization is completed. This bit monitors RAM_INITEND pin value of the RAMA via RAMA_INIT_END pin.

52.3.2.37 WDT Counter Stop Control Register (SYS_WDT_CNTSTOP)

This register controls stopping of the WDT counter.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0130h

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CH1	CH0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW

Table 52.3-44 SYS_WDT_CNTSTOP Register Contents

Bit Position	Bit Name	Description
31 to 3	—	Reserved. These bits are read as 0b. The write value should always be 0b.
2	—	Reserved. When read, the value read is undefined. The write value should always be 0b.
1	CH1	Reserved. When read, the value read is undefined. Since this bit is for use with the ISP support package, writing to this bit is prohibited.
0	CH0	WDT0 counter stop control 0b: Counting by the WDT is enabled 1b: Counting by the WDT is disabled.

Note: Controlling stopping of the WDT is also possible from the CST.

52.3.2.38 CST Trigger Signal Monitor Register for WDT (SYS_CST_HLTDBG_MON)

This register is a read-only register for monitoring the WDT trigger pin (CST_HLTDBG[2:0]) input from the CST.

Writing to this register has no effect.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0134h

Initial Value: 0000_000xh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	TEST	MON1	MON0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-45 SYS_CST_HLTDBG_MON Register Contents

Bit Position	Bit Name	Description
31 to 3	—	Reserved. These bits are read as 0b.
2	TEST	Reserved. The value read is invalid.
1	MON1	Trigger pin monitoring for WDT1. 0b: Monitoring of the WDT trigger pin is enabled 1b: Monitoring of the WDT trigger pin is disabled.
0	MON0	Trigger pin monitoring for WDT0. 0b: Monitoring of the WDT trigger pin is enabled 1b: Monitoring of the WDT trigger pin is disabled.

52.3.2.39 General-Purpose 32Bit Read/Write Register m (SYS_GEN_REGm) (m = 0 to 2)

This register is a general-purpose 32-bit read/write register.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0200h (m = 0)
<SYS_S0_base> + 0204h (m = 1)
<SYS_S0_base> + 0208h (m = 2)

Initial Value: 0000_0000h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BIT[31:16]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BIT[15:0]															
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 52.3-46 SYS_GEN_REGm Register Contents

Bit Position	Bit Name	Description
31 to 0	BIT[31:0]	A readable/writable register. There are no special functions.

52.3.2.40 ETH AxCACHE[1](C bit) Control Register (SYS_ETH_CACHE_C_CNT)

This register controls ARCACHE[1] and AWCACHE[1] of ETHER.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0220h

Initial Value: 0000_0022h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	E0_WC_WE	—	—	—	E0_RC_WE	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R0W1	R	R	R	R0W1	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	E0_WC	—	—	—	E0_RC	—
Initial Value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
R/W	R	R	R	R	R	R	R	R	R	R	RW	R	R	R	RW	R

Table 52.3-47 SYS_ETH_CACHE_C_CNT Register Contents

Bit Position	Bit Name	Description
31 to 22	—	Reserved. These bits are read as 0b.
29	E0_WC_WE	Enables write to E0_WC. Write only. These bits are read as 0b. 0b: Invalid write to E0_WC 0b: Valid write to E0_WC
20 to 18	—	Reserved. These bits are read as 0b.
17	E0_RC_WE	Enables write to E0_RC Write only. These bits are read as 0b. 0b: Invalid write to E0_RC 1b: Valid write to E0_RC
16 to 6	—	Reserved. These bits are read as 0b.
5	E0_WC	Controls AWCACHE[1] (C bit) of ETHER.
4 to 2	—	Reserved. These bits are read as 0b.
1	E0_RC	Controls ARCACHE[1] (C bit) of ETHER.
0	—	Reserved. This bit is read as 0b.

52.3.2.41 OBS Count Stop Control Register for ICB (SYS_ICB_OBS_SUSP)

This register controls the ICB observability (OBS) counting stop.

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0230h

Initial Value: 0000_01FFh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	SUSP[8:0]_WE								
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SUSP8	SUSP[7:0]							
Initial Value	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Table 52.3-48 SYS_ICB_OBS_SUSP Register Contents

Bit Position	Bit Name	Description
31 to 25	—	Reserved. These bits are read as 0b.
24 to 16	SUSP[8:0]_WE	Enables write to SUSP[8:0]. Write only. These bits are read as 0b. 0b: Disables write to E0_WC. 1b: Enables write to E0_WC..
15 to 9	—	Reserved. These bits are read as 0b.
8	SUSP8	StatSuspend for the Scheduler output port. 0b: OBS count enable 1b: OBS count stop
7 to 0	SUSP[7:0]	StatSuspend for the Scheduler input port #8 to #1. 0b: OBS count enable 1b: OBS count stop

52.3.2.42 TSU0 TS0_LT_DAT[11:0] Signal Monitor Register (SYS_TS0LT_DAT_MON)

This register is a read-only register for monitoring the TSU0 TS0_LT_DAT[11:0] signal.

Writing to this register has no effect. The initial value of the LSB 12 bits is determined by the state of TS0_LT_DAT[11:0].

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0330h

Initial Value: 0000_0xxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TS0LT_DAT											
Initial Value	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-49 TS0LT_DAT_MON Register Contents

Bit Position	Bit Name	Description
31 to 12	Reserved	Reserved. These bits are read as 0b.
11 to 0	TS0LT_DAT[11:0]	TS0_LT_DAT[11:0] monitoring for TSU0.

52.3.2.43 TSU0 TS0_HT_DAT[11:0] Signal Monitor Register (SYS_TS0HT_DAT_MON)

This register is a read-only register for monitoring the TSU0 TS0_LT_DAT[11:0] signal.

Writing to this register has no effect. The initial value of the LSB 12 bits is determined by the state of TS0_HT_DAT[11:0].

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0338h

Initial Value: 0000_0xxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TS0HT_DAT											
Initial Value	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-50 TS0HT_DAT_MON Register Contents

Bit Position	Bit Name	Description
31 to 12	Reserved	Reserved. These bits are read as 0b.
11 to 0	TS0HT_DAT[11:0]	TS0_HT_DAT[11:0] monitoring for TSU0.

52.3.2.44 TSU1 TS1_LT_DAT[11:0] Signal Monitor Register (SYS_TS1LT_DAT_MON)

This register is a read-only register for monitoring the TSU1 TS1_LT_DAT[11:0] signal.

Writing to this register has no effect. The initial value of the LSB 12 bits is determined by the state of TS1_LT_DAT[11:0].

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0340h

Initial Value: 0000_0xxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TS1LT_DAT											
Initial Value	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-51 TS1LT_DAT_MON Register Contents

Bit Position	Bit Name	Description
31 to 12	Reserved	Reserved. These bits are read as 0b.
11 to 0	TS1LT_DAT[11:0]	TS1_LT_DAT[11:0] monitoring for TSU1.

52.3.2.45 TSU1 TS1_HT_DAT[11:0] Signal Monitor Register (SYS_TS1HT_DAT_MON)

This register is a read only register for monitoring the TSU1 TS1_HT_DAT[11:0] signal.

Writing to this register has no effect. The initial value of the LSB 12 bits is determined by the state of TS1_HT_DAT[11:0].

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0348h

Initial Value: 0000_0xxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TS1HT_DAT											
Initial Value	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-52 TS1HT_DAT_MON Register Contents

Bit Position	Bit Name	Description
31 to 12	Reserved	Reserved. These bits are read as 0b.
11 to 0	TS1HT_DAT[11:0]	TS1_HT_DAT[11:0] monitoring for TSU1.

52.3.2.46 TSU0/1 TS_LT_TEMP[11:0] Signal Monitor Register (SYS_TSLT_TEMP_MON)

This register is a read only register for monitoring the TSU0/1 TS_LT_TEMP[11:0] signal.

Writing to this register has no effect. The initial value of the LSB 12 bits is determined by the state of TS_LT_TEMP[11:0].

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0350h

Initial Value: 0000_0xxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TSLT_TEMP											
Initial Value	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-53 TSLT_TEMP_MON Register Contents

Bit Position	Bit Name	Description
31 to 12	Reserved	Reserved. These bits are read as 0b.
11 to 0	TSLT_TEMP[11:0]	TS_LT_TEMP[11:0] monitoring for TSU0/1.

52.3.2.47 TSU0/1 TS_HT_TEMP[11:0] Signal Monitor Register (SYS_TSHT_TEMP_MON)

This register is a read only register for monitoring the TSU0/1 TS_HT_TEMP[11:0] signal.

Writing to this register has no effect. The initial value of the LSB 12 bits is determined by the state of TS_HT_TEMP[11:0].

Access Size: 32 bits

Address(es): <SYS_S0_base> + 0358h

Initial Value: 0000_0xxxh

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TSHT_TEMP											
Initial Value	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 52.3-54 TSHT_TEMP_MON Register Contents

Bit Position	Bit Name	Description
31 to 12	Reserved	Reserved. These bits are read as 0b.
11 to 0	TSHT_TEMP[11:0]	TS_HT_TEMP[11:0] monitoring for TSU0/1.

52.4 Functional Description

This section describes the functions of the SYS unit.

The prefix (SYS_) of the register names is omitted in this and subsequent sections.

52.4.1 Bank Address Switching

The SYS has a bank switching register to extend the two higher-order bits of the addresses of the following IP modules which have only 32-bit (4-GB) address spaces. It makes 4 or more Gbytes of the address space accessible by switching the bank address.

Target unit 1: DRP-AI, eMMC, SDI0/1, ETHER, PCIe, USB, GRP, VCD
Target unit 2: DMAC

The specific functions are as follows.

- Target unit 1

  Two bits for switching the bank address from the SYS are output to the ICB (common to the AR and AW channels).

- Target unit 2

  Two bits for switching the bank address from the SYS are output to the DMAC (individually for the source, destination, and descriptor per DMAC number and channel of the DMAC).

The following restrictions apply to bank address switching.

(1) When changing the bank address, only do so after all transactions by the target master have been completed.

Note: For the DMAC, changing the extended address for the corresponding DMAC number and channel is possible if the corresponding DMAC number and channel are not operating.

(2) When starting a transaction by the target master following bank address switching, only do so after reading the bank address switching register to check its setting.

(3) Access which spans across 32-bit address boundaries is prohibited.

(4) Setting 11b and 10b is prohibited.

Table 52.4-1 shows the correspondence between the bank addresses and the accessible address spaces.

Table 52.4-1 Correspondence between the Bank Addresses and the Accessible Address Spaces

Bank Address[1:0]	Address Space
11b	Setting prohibited
10b	Setting prohibited
01b	01_FFFF_FFFFh
	:
	01_0000_0000h
00b	00_FFFF_FFFFh
	:
	00_0000_0000h

52.4.2 I/F Pins for ICB

52.4.2.1 ETH AxCACHE[1]

The SYS has a register to output the ARCACHE[1] and AWCACHE[1] signals in place of the ETHER and is able to control cacheable access by the ETHER.

The following restrictions apply to changing the settings of the cacheable bits.

- ARCACHE[1]:
  Changing the setting of the cacheable bit is only possible when all read transactions by the AXI master of ETHER have been completed.
- AWCACHE[1]:
  Changing the setting of the cacheable bit is only possible when all write transactions by the AXI master of ETHER have been completed.
- When starting a read transaction by the AXI master of ETHER following switching of ARCACHE[1], only do so after reading the ETH AxCACHE[1] (C bit) control register to check its setting.
- When starting a write transaction by the AXI master of ETHER following switching of AWCACHE[1], only do so after reading the ETH AxCACHE[1] (C bit) control register to check its setting.

52.4.2.2 Observability

The SYS has a register to output the ICB observability (OBS) counting stop control signal and is able to control stopping and operation of the OBS counter for the ICB.

52.4.3 PCIe-I/F Control

The SYS has the registers listed below.

These registers are used to monitor the pins supplied from the PCIe and control the pins for output to the PCIe.

Monitor registers

- PCI_FLR_REQ register
- PCI_TURN_OFF_EVENT register
- PCI_D3_EVENT register
- PCI_PME_STS_CLR register

Control registers

- PCI_FLR_RST register
- PCI_INTX_EP register
- PCI_EXTMSI_VAL register
- PCI_EXTMSI_SET0 register
- PCI_EXTMSI_SET1 register
- PCI_EXTMSI_SET2 register
- PCI_EXTMSI_SET3 register
- PCI_EXTMSI_SET4 register
- PCI_ALLOW_ENTER_L1 register
- PCI_PME_TIM register
- PCI_TURN_OFF_EVENT_ACK register
- PCI_D3_EVENT_ACK register
- PCI_PME_STS register
- PCI_MODE register
- PCI_MODE_EN_B register

52.4.4 RAMA Initialization Function

Register control by the SYS is required at the time of RAMA initialization.

For details of the functions, refer to the section of RAMA.

52.4.5 Monitoring of MD0 to MD7 Pins

The SYS has functionality to monitor the values of the MD0 to MD7 pins by using the MD_MON register (offset: 100h).

52.4.6 LSI Version Register

The SYS includes a register to check the version number of this LSI chip.

52.4.7 General-purpose 32-Bit Readable/Writable Registers

The SYS includes four general-purpose registers which are readable and writable in 32 bits. These registers have no special function for use in debugging, etc.

52.4.8 WDT Counter Stop Control

The SYS outputs WDT counter STOP signal WDT_CNTSTOP[1:0]. Signal WDT_CNTSTOP[1:0] is logical OR of the values of the CST_HLTDBG[1:0] input pin from the CST and the WDT_CNTSTOP register of the SYS (offset: 130h).

0b: Counting by the WDT is possible.
1b: Stops counting by the WDT.

This function is used to stop the WDT counter so that WDT reset is not performed during a break in device debugging using the ICE.

Stop the counter upon a break and operate the counter in the RUN state.

Figure 52.4-1 shows the WDT_CNTSTOP[1:0] output signal generation circuit.

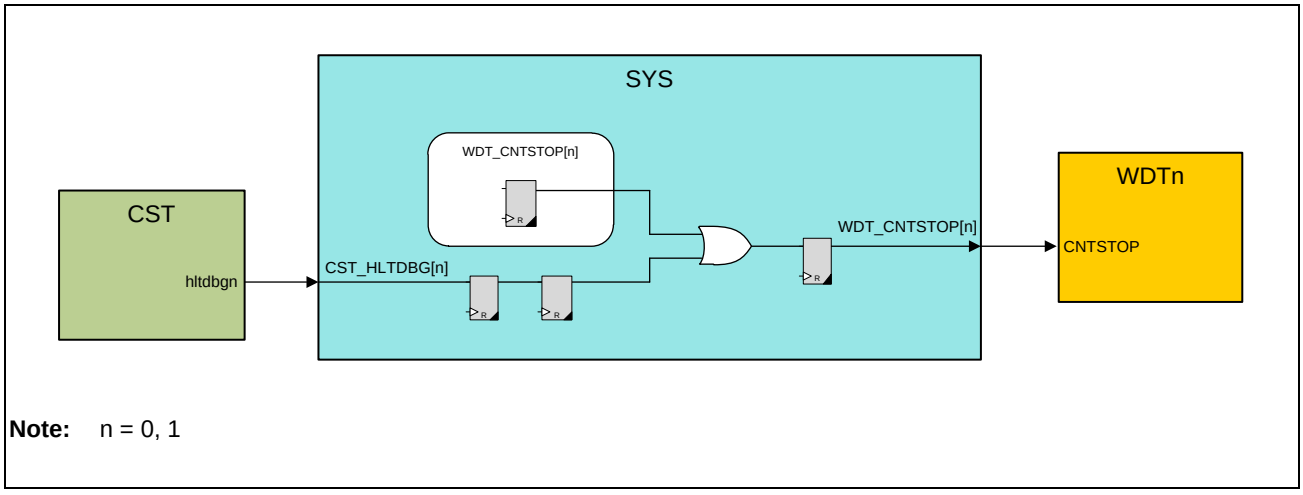


Figure 52.4-1 WDT_CNTSTOP[1:0] Output Signal Generation Circuit

52.4.9 Reading of the Temerature Sensor Reference Value

The SYS has functionality for reading the reference value of the temperature sensor.

For details of the functions of the temperature sensor, see the section of Temperature Sensor (TSU).

52.5 Operating Procedure

52.5.1 Procedure for Writing to the Bank Address Switching Register

The 16 higher-order bits of the bank address switching register are write enable and the 16 lower-order bits are normal data registers, so changing only the value of the specified bits is possible without read-modify-write operation.

When changing the value, write 1 to the bit plus 16 of the bit to be changed.

<*Example*>

To set bit[0] to 1b, write 0001_0001h. To set it to 0b, write 0001_0000h. The value of bit[15:0] is not changed when 0000_xxxxh is written

When read, the 16 higher-order bits are always read as 0b.

52.5.2 Procedure of Writing to the I/F Pin Control Registers for ICB

The procedure for writing to the bank address switching register also applies to the procedure for writing to the registers listed below.

- ETH_CACHE_C_CNT register (offset: 220h)
- ICB_OBS_SUSP register (offset: 230h)

For details, see **Section 52.5.1, Procedure for Writing to the Bank Address Switching Register**.

52.5.3 Procedure for PCIe-I/F Control

For the operating procedure, refer to the section of PCIe.

52.5.4 RAMA Initialization Procedure

See **Section 52.4.4, RAMA Initialization Function**.

52.5.5 WDT Counter Stop Control Procedure

See **Section 52.4.8, WDT Counter Stop Control**.

52.6 Usage Notes

52.6.1 Bank Address Switching

- When changing the bank address, only do so after all transactions by the target master have been completed.
  For the DMAC, changing the extended address for the corresponding DMAC number and channel is possible if the corresponding DMAC number and channel are not operating.
- When starting a transaction by the target master following bank address switching, only do so after checking that the expected value has been set in the target register after writing to it.
- Access which spans across 32-bit address boundaries is prohibited.

52.6.2 PCIe Register Control

- Changing the setting for operation as an endpoint or root complex in the PCI device type setting register (SYS: PCI_MODE) is prohibited while the PCI is operating. Be sure to make the setting while operation of the PCI is stopped.

- The PCI macro off mode setting can also be made by using a register in the PCI. When setting the PCI macro off mode with a register in the PCI, fix the EN_B bit of the PCI macro off mode setting register in the SYS (SYS: PCI_MODE_EN_B) to 0b.

- For the following registers, be sure to supply the PCI_ACLK clock before setting values.
  - PCI FLR execution instruction reset register (SYS: PCI_FLR_RST)
  - PCI MSI issuing register (SYS: PCI_EXTMSI_VAL)
  - PCI issued MSI setting register 0 (SYS: PCI_EXTMSI_SET0)
  - PCI issued MSI setting register 1 (SYS: PCI_EXTMSI_SET1)
  - PCI issued MSI setting register 2 (SYS: PCI_EXTMSI_SET2)
  - PCI issued MSI setting register 3 (SYS: PCI_EXTMSI_SET3)
  - PCI issued MSI setting register 4 (SYS: PCI_EXTMSI_SET4)

- Writing to the following registers twice or more is prohibited while PCI_ACLK is stopped (read the register value before writing a value again).
  - PCI issued MSI setting register 0 (SYS: PCI_EXTMSI_SET0)
  - PCI issued MSI setting register 1 (SYS: PCI_EXTMSI_SET1)
  - PCI issued MSI setting register 2 (SYS: PCI_EXTMSI_SET2)
  - PCI issued MSI setting register 3 (SYS: PCI_EXTMSI_SET3)
  - PCI issued MSI setting register 4 (SYS: PCI_EXTMSI_SET4)

Section 53 Debugger (CST)

This section describes functions of the debugger (CoreSight System (CST)).

53.1 Functional Overview

The CST is a system with an Arm® CoreSight™ Component. For details on the embedded debug components, refer to *the ARM CoreSight SoC-400 Technical Reference Manual*, *the ARM CoreSight STM-500 System Trace Macrocell Technical Reference Manual*, and *the CoreSight Trace Memory Controller Technical Reference Manual. Manual*, and *the CoreSight Trace Memory Controller Technical Reference Manual*.

Table 53.1-1 lists the debug system functions.

Table 53.1-1 Debug System Functions (1/2)

Item	Functions
Embedded debug components	• *ARM CoreSight SoC-400 (r3p2)* – DAP – ROM table – TPIU – Trace funnel – Replicator – Timestamp generator – CTI – CTM • *ARM CoreSight STM-500 system trace macrocell (r0p1)* – STM • *CoreSight trace memory controller (r0p1)* – ETF (64-KB RAM) – ETR • ARM embedded trace macrocell – ETM in CA53 (ETMv4)*1
Functions incorporated	• JTAG interface – Supports JTAG and SWD • TRACE interface – Supports trace data output of 16 bits × 100 Mbps (50-MHz DDR) • Debugger control function (DAP function) – Reset control of debug components by setting the debug port (DP) register • Trace data support – CPU trace output (ETMv4 trace generation) – Trace output using STM (STPv2 (MIPI)) – Trace data buffer mechanism using ETF – Trace data output to ICB by using ETR • Others Interlocking operations of CPU, WDT, SYC, and debug components by cross-triggering

Table 53.1-1 Debug System Functions (2/2)

Item	Functions
External interface (Arm® AMBA® interface)	• Interface with CPU (CA53) – ATB 32-bit slave port: Cortex-A53 Core0 trace port – ATB 32-bit slave port: Cortex-A53 Core1 trace port – APB3 32-bit master port: Cortex-A53 debug APB • Interface with the system bus (ICB) – AXI4 64-bit master port: AXI-AP – AXI3 32-bit master port: ETR – AXI4 64-bit slave port: STM – APB3 32-bit slave port: DAP – ATB 64-bit slave port: Probe

Note 1. For the functions supported by ETM, see the Technical Reference Manual of the applicable CPU.

The following functions are disabled in this LSI.

(1) Low power control function (Q channel and others)

This LSI implements the low power control function by CPG/PMC.
Therefore, the low power control function specific to individual components of CoreSight SoC-400 and CoreSight STM-500 is not available.

(2) Hardware event trace function of CoreSight STM-500 (Hardware event interface)

This LSI does not use the hardware event interface.
Therefore, the hardware event tracing is disabled.

(3) DMA request function of CoreSight STM-500 (DMA request interface)

This LSI does not use the DMA request interface.
Therefore, it is impossible to activate an external DMAC for tracing.

53.2 Block Diagram

Figure 53.2-1 shows a block diagram of the CST.

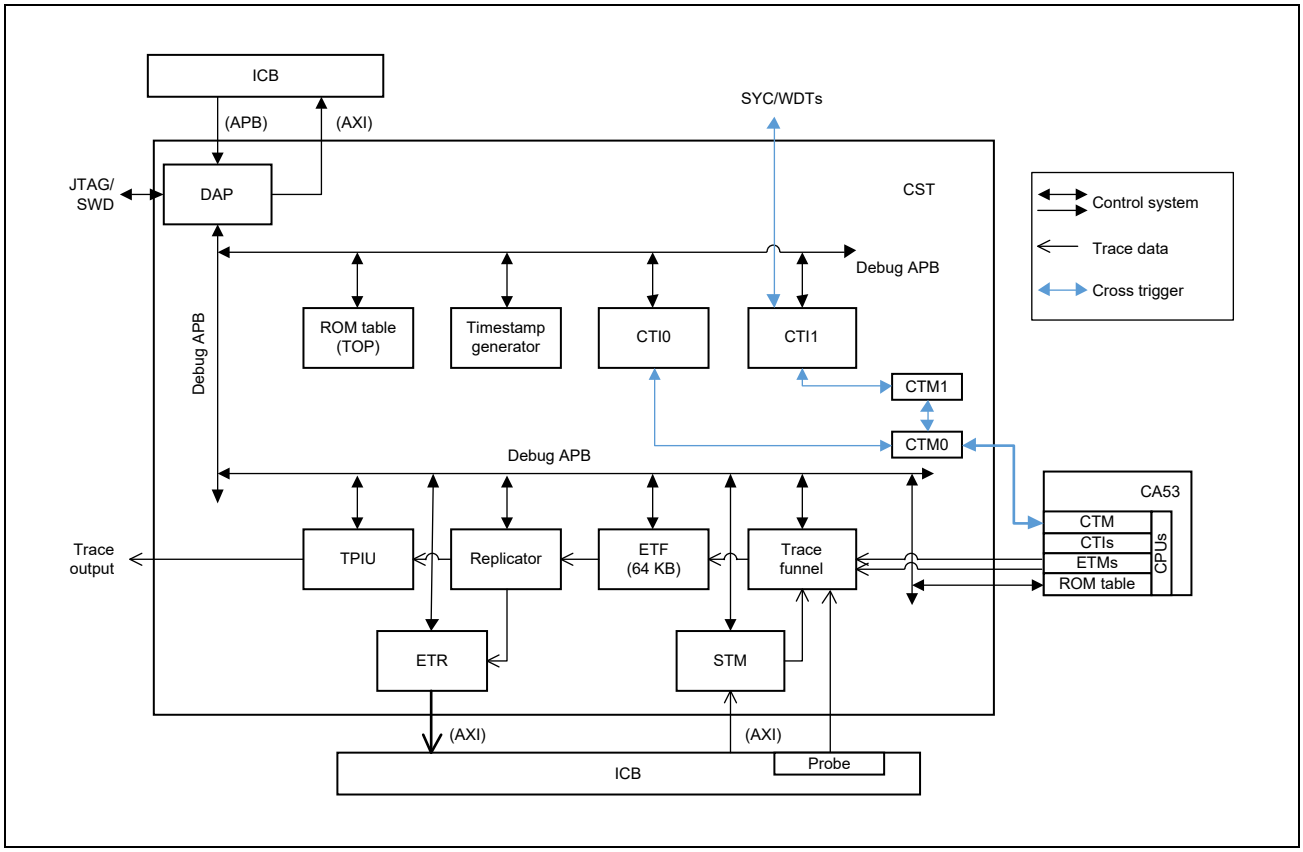
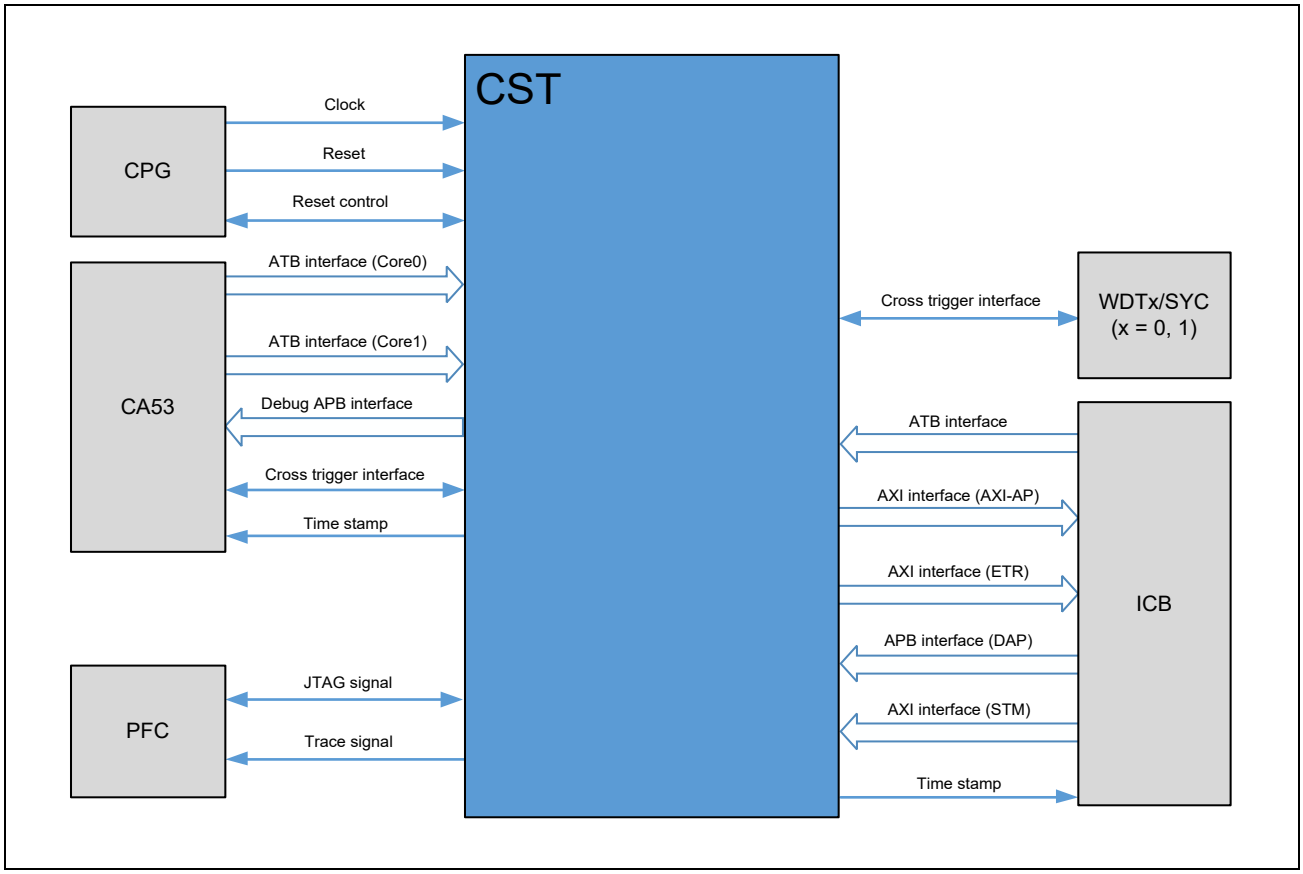


Figure 53.2-1 Block Diagram

53.3 Connection Configuration

Fiugre 53.3-1 shows the connection configuration.



Fiugre 53.3-1 Connection Configuration

53.4 Pin Functions

53.4.1 List of External Pins

Table 53.4-1 lists the external pins of the CST.

Table 53.4-1 List of External Pins

Classification	Pin name	I/O	Function
Debugger interface	DETCK	Input	JTAG TCK
	DETDI	Input	JTAG TDI
	DETDO	Output	JTAG TDO
	DETMS	IO	JTAG TMS
	DETRSTN	Input	JTAG TRST (active low)
	DESRSTN	Input	System reset from debugger (active low)
TRACE interface (TRACE)	TRDAT15 to TRDAT0	Output	Trace data [15:0]
	TRCLK	Output	Trace clock
	TRCTL	Output	Trace control

53.5 Address Space

The CST has an address space of the debug system (CST_S0) and a 16-Mbyte STM stimulus port space (CST_S1). **Table 53.1-1** lists the address space of the debug system (CST_S0). For the address space of STM, see *the ARM CoreSight STM-500 Trace Macrocell Technical Reference Manual*.

Table 53.5-1 Address Space of the Debug System (CST_S0)

Offset Address	Access Target*1
CST Debug Components*2	
00_0000h to 00_FFFFh	CST: ROM table
01_0000h to 01_FFFFh	CST: Timestamp generator
02_0000h to 02_FFFFh	CST: TPIU
03_0000h to 03_FFFFh	CST: ETR
04_0000h to 04_FFFFh	CST: Replicator
05_0000h to 05_FFFFh	CST: ETF
06_0000h to 06_FFFFh	CST: Reserved
07_0000h to 07_FFFFh	CST: Trace Funnel
08_0000h to 08_FFFFh	CST: Reserved
09_0000h to 09_FFFFh	CST: STM
0A_0000h to 0A_FFFFh	CST: CTI0
0B_0000h to 0B_FFFFh	CST: CTI1
0C_0000h to 0C_FFFFh	CST: CTI2
0D_0000h to 1F_FFFFh	CST: Reserved
CA53 Debug Components*2	
20_0000h to 20_FFFFh	CA53: ROM table
21_0000h to 21_FFFFh	CA53: Core0 Debug
22_0000h to 22_FFFFh	CA53: Core0 CTI
23_0000h to 23_FFFFh	CA53: Core0 PMU
24_0000h to 24_FFFFh	CA53: Core0 ETM
25_0000h to 30_FFFFh	CA53: Reserved
31_0000h to 31_FFFFh	CA53: Core1 Debug
32_0000h to 32_FFFFh	CA53: Core1 CTI
33_0000h to 33_FFFFh	CA53: Core1 PMU
34_0000h to 34_FFFFh	CA53: Core1 ETM
35_0000h to 3F_FFFFh	CA53: Reserved

Note 1. Access to the reserved registers is prohibited. If such access is attempted, correct operation is not guaranteed.

Note 2. The components are allocated on 16-Kbyte boundaries according to the ARMv8 Debug memory map. The first 4 Kbytes are actually effective.

53.6 Register Descriptions

The CST is a debugging system with Arm® CoreSight™ components.

The revision number for the component is as follows.

- *ARM CoreSight SoC-400 (r3p2)*
- *ARM CoreSight STM-500 System Trace Macrocell (r0p1)*
- *CoreSight Trace Memory Controller (r0p1)*

For details on these registers, refer to the ARM manuals listed below.

- *ARM CoreSight SoC-400 Technical Reference Manual*
- *ARM CoreSight STM-500 System Trace Macrocell Technical Reference Manual*
- *CoreSight Trace Memory Controller Technical Reference Manual*

53.7 Functional Description

53.7.1 DAP

The DAP includes SWJ-DP as a debug port (DP).

53.7.2 Tracing

53.7.2.1 Data Flow

In CST, all trace data is gathered once at the trace funnel and output to the external pins and/or ICB, by the replicator in the latter stage. Depending on the path of the trace data, this port number must be set to the trace funnel and replicator. The port number for the trace funnel is shown in **Table 53.7-1** and the port number for the replicator is shown in **Table 53.7-2**.

Table 53.7-1 Port Number for theTrace Funnel

Port Number	Source Components
port-0	CA53: Core0 ETM
port-1	CA53: Core1 ETM
port-2	Reserved
port-3	Reserved
port-4	ICB: Probe
port-5	STM

Table 53.7-2 Port Number for the Replicator

Port Number	Destination Components
port-0	TPIU
port-1	ETR

53.7.2.2 STM

The trace data written to the STM stimulus port is converted to STPv2 packets and output. STPv2 uses the master ID to identify the source component of the written source. **Table 53.7-3** lists the master IDs. In addition, a cross-trigger can be detected as a hardware event. **Table 53.7-4** lists hardware events.

Table 53.7-3 List of Master IDs

Master ID (8 bits)*1	Source Components
0x000000b	CA53: Core0
0x000001b	CA53: Core1
0x000010b	Reserved

Note 1. “x” reflects the security information (AWPROT[1]).

Table 53.7-4 Hardware Event

Event Number	Source Components	Edge / Level
0	CTI0: CTITRIGOUT[6]	Edge
1	CTI0: $\overline{\text{CTITRIGOUT[6]}}$	Edge
2	CTI0: CTITRIGOUT[7]	Edge
3	CTI0: $\overline{\text{CTITRIGOUT[7]}}$	Edge

53.7.2.3 Timestamp

When including time information in the trace data, the timestamp generator can be used. **Table 53.7-5** lists the bit widths of timestamp. The 64-bit timestamp output by the timestamp generator is commonly used in all trace components. Note that only the ICB probe uses the extended timestamp, so be careful when outputting the time information.

Table 53.7-5 Bit Width of Timestamp

Source Components	Input Timestamp	Control
CA53: Core0/1 ETM, CST: STM	64 bits	Uses 64-bit input (with synchronization)
ICB: Probe	48 bits	Uses the lower 48-bit input as an extension

53.7.3 Cross Trigger

The cross trigger interface (CTI) provided respectively in CST and CA53 is used to pass debug events.

53.7.3.1 Cross Trigger Connection of CST

The CST has three CTIs (CST CTI0, CST CTI1, CST CTI2). **Table 53.7-6** to **Table 53.7-11** show their respective connection specifications.

Table 53.7-6 CST CTI0 Trigger Inputs

Trigger input bit	Source Components	Connect Signal
[7]	STM	TRIGOUTSW
[6]	STM	TRIGOUTSPTE
[5]	STM	TRIGOUTHETE
[4]	STM	ASYNCOUT
[3]	ETR	FULL
[2]	ETR	ACQCOMP
[1]	ETF	FULL
[0]	ETF	ACQCOMP

Table 53.7-7 CST CTI0 Outputs

Trigger output bit	Destination Components	Connect Signal
[7]	STM	$\overline{\text{HWEVENT[3]}}$, HWEVENT[2]
[6]	STM	$\overline{\text{HWEVENT[1]}}$, HWEVENT[0]
[5]	TPIU	TRIGIN
[4]	TPIU	FLUSHIN
[3]	ETR	TRIGIN
[2]	ETR	FLUSHIN
[1]	ETF	TRIGIN
[0]	ETF	FLUSHIN

Table 53.7-8 CST CTI1 Trigger Input (Not Used)

Trigger input bit	Source Components	Connect Signal
[7:0]	—	00000000b

Table 53.7-9 CST CTI1 Trigger Outputs

Trigger output bit	Destination Components	Connect Signal
[7]	Reserved	—
[6]	Reserved	—
[5]	WDT1	$\overline{\text{CNTSTOP}}$*1
[4]	WDT1	CNTSTOP*1,*2
[3]	WDT0	$\overline{\text{CNTSTOP}}$*1
[2]	WDT0	CNTSTOP*1,*2
[1]	SYC	$\overline{\text{HALTREQ}}$*1
[0]	SYC	HALTREQ*1,*2

Note 1. When trigger outputs in the active and non-active directions occur at the same time, operation is in the active direction.

Note 2. The acknowledge signal is fixed to 0b. Use software (the CTIINTACK register of CTIO) to issue the signal.

Table 53.7-10 CST CTI2 Trigger Input (Not Used)

Trigger input bit	Source Components	Connect Signal
[7:0]	—	00000000b

Table 53.7-11 CST CTI2 Trigger Output (Not Used)

Trigger output bit	Destination Components	Connect Signal
[7:0]	—	—

53.7.3.2 Cross Trigger Connection of CA53

The CA53 has two CTIs (CA53 core 0 CTI, CA53 Core1 CTI). **Table 53.7-12** to **Table 53.7-15** show their respective connection specifications.

Table 53.7-12 CA53 Core 0 CTI Trigger Inputs

Trigger input bit	Source Components	Connect Signal
[7]	CA53: Core0 ETM	EXTOUT[3]
[6]	CA53: Core0 ETM	EXTOUT[2]
[5]	CA53: Core0 ETM	EXTOUT[1]
[4]	CA53: Core0 ETM	EXTOUT[0]
[3]	—	0b
[2]	—	0b
[1]	CA53: Core0 PMU	PMUIRQ[0]
[0]	CA53: Core0 Debug	DBGTRIGGER[0]

Table 53.7-13 CA53 Core 0 CTI Trigger Outputs

Trigger output bit	Destination Components	Connect Signal
[7]	CA53: Core0 ETM	EXTIN[3]
[6]	CA53: Core0 ETM	EXTIN[2]
[5]	CA53: Core0 ETM	EXTIN[1]
[4]	CA53: Core0 ETM	EXTIN[0]
[3]	—	—
[2]	External (interrupt control circuit)	CTIIRQ[0]*1
[1]	CA53: Core0 Debug	DBGRESTART[0]
[0]	CA53: Core0 Debug	EDBGRQ[0]*1

Note 1. The acknowledge signal is fixed to 0b. Use software (the CTIINTACK register of CTI) to issue the signal.

Table 53.7-14 CA53 Core 1 CTI Trigger Inputs

Trigger input bit	Source Components	Connect Signal
[7]	CA53: Core1 ETM	EXTOUT[3]
[6]	CA53: Core1 ETM	EXTOUT[2]
[5]	CA53: Core1 ETM	EXTOUT[1]
[4]	CA53: Core1 ETM	EXTOUT[0]
[3]	—	0b
[2]	—	0b
[1]	CA53: Core1 PMU	PMUIRQ[1]
[0]	CA53: Core1 Debug	DBGTRIGGER[1]

Table 53.7-15 CA53 Core 1 CTI Trigger Outputs

Trigger output bit	Destination Components	Connect Signal
[7]	CA53: Core1 ETM	EXTIN[3]
[6]	CA53: Core1 ETM	EXTIN[2]
[5]	CA53: Core1 ETM	EXTIN[1]
[4]	CA53: Core1 ETM	EXTIN[0]
[3]	—	—
[2]	External (interrupt control circuit)	CTIIRQ[1]*1
[1]	CA53: Core1 Debug	DBGRESTART[1]
[0]	CA53: Core1 Debug	EDBGRQ[1]*1

Note 1. The acknowledge signal is fixed to 0b. Use software (the CTIINTACK register of CTI) to issue the signal.

Section 54 Electrical Characteristics

This section describes the electrical characteristics of this LSI.

54.1 Absolute Maximum Ratings

Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Table 54.1-1 Absolute Maximum Ratings (1/3)

Item	Symbol	Min.	Max.	Unit
VDD08 core power supply	V_{DD08}	−0.4	1.2	V
RTC core power supply	RTV_{DD08}	−0.4	1.2	V
RTC I/O, 1.5-V OSC power supply	RTV_{DD}	−0.4	2.5	V
PWC core power supply	PWV_{DD08}	−0.4	1.2	V
PWC I/O power supply	PWV_{DD}	−0.4	2.5	V
PORT01(A), PORT03 pre-driver power supply	$PAPREDV_{DD}$	−0.4	2.5	V
PORT01(A), PORT03 I/O power supply	$PAMODV_{DD}$	−0.4	3.8	V
PORT01(B), PORT04, PORT07, PORT21 pre-driver power supply	$PBPREDV_{DD}$	−0.4	2.5	V
PORT01(B), PORT04, PORT07, PORT21 I/O power supply	$PBMODV_{DD}$	−0.4	3.8	V
PORT06 pre-driver power supply	$PCPREDV_{DD}$	−0.4	2.5	V
PORT06 I/O power supply	$PCMODV_{DD}$	−0.4	3.8	V
PORT10 pre-driver power supply	$IM0PREDV_{DD}$	−0.4	2.5	V
PORT10 I/O power supply	$IM0MODV_{DD}$	−0.4	3.8	V
PORT11 pre-driver power supply	$IM1PREDV_{DD}$	−0.4	2.5	V
PORT11 I/O power supply	$IM1MODV_{DD}$	−0.4	3.8	V
PORT00 pre-driver power supply	$NAPREDV_{DD}$	−0.4	2.5	V
PORT00 I/O power supply	$NAMODV_{DD}$	−0.4	3.8	V
PORT08 pre-driver power supply	$SD0PREDV_{DD}$	−0.4	2.5	V
PORT08 I/O power supply	$SD0MODV_{DD}$	−0.4	3.8	V
PORT09 pre-driver power supply	$SD1FV_{DD}$	−0.4	2.5	V
PORT09 I/O power supply	$SD1FMODV_{DD}$	−0.4	3.8	V
PORT15, PORT16, PORT17 pre-driver power supply	$GEPREDV_{DD}$	−0.4	2.5	V
PORT15, PORT16, PORT17 I/O power supply	$GEMODV_{DD}$	−0.4	3.8	V

Table 54.1-1 Absolute Maximum Ratings (2/3)

Item	Symbol	Min.	Max.	Unit
VDD18 group I/O power supply (PORT02 I/O, PORT05 I/O, PORT20 I/O, 1.8-V OSC, RSTN I/O, debugger I/O, MD0-7 I/O)	V_{DD18}	−0.4	2.5	V
VDD33 group pre-driver power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	$PREDV_{DD33}$	−0.4	2.5	V
VDD33 group I/O power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	V_{DD33}	−0.4	3.8	V
PLL ch. 1, 2, 3, 4, 6, 7 0.8-V power supply	$PLDV_{DD08n}$ (n = 1, 2, 3, 4, 6, 7)	−0.4	1.2	V
PLL ch. 1, 2, 3, 4, 6, 7 1.8-V power supply	PLV_{DDn} (n = 1, 2, 3, 4, 6, 7)	−0.4	2.5	V
OTP 0.8-V power supply	OTV_{DD08}	−0.4	1.2	V
OTP 1.8-V power supply	OTV_{DD18}	−0.4	2.5	V
TSU ch. 0 0.8-V power supply	$TS0DV_{DD08A}$	−0.4	1.2	V
TSU ch. 1 0.8-V power supply	$TS1DV_{DD08A}$	−0.4	1.2	V
TSU ch. 0 1.8-V power supply	$TS0AV_{DD18}$	−0.4	2.5	V
TSU ch. 1 1.8-V power supply	$TS1AV_{DD18}$	−0.4	2.5	V
ADC unit A 1.8-V power supply	$AD0AV_{CCA}$	−0.4	2.5	V
ADC unit B 1.8-V power supply	$AD1AV_{CCA}$	−0.4	2.5	V
CIF PHY 0.8-V power supply	$LVRXAV_{DD}$	−0.4	1.2	V
CIF PHY 1.8-V power supply	$LVRXAV_{CC}$	−0.4	2.5	V
LPDDR4 core 0.8-V power supply	LPV_{DD}	−0.4	1.2	V
LPDDR4 PLL 1.8-V power supply	LPV_{AA}	−0.4	2.5	V
LPDDR4 I/O 1.1-V power supply	LPV_{DDQ}	−0.4	1.5	V
HDMI PHY 1.8-V power supply	$HDAV_{DD18}$	−0.4	2.5	V
HDMI PHY 0.8-V power supply	$HDAV_{DD08}$	−0.4	1.2	V
MIPI DSI Tx PHY 1.8-V power supply	$DSMSV_{DD18}$	−0.4	2.5	V
MIPI DSI Tx PHY 1.2-V power supply	$DSMV_{DD12}$	−0.4	2.5	V
MIPI DSI Tx PHY 0.8-V power supply	$DSMSV_{DD0P8}$	−0.4	1.2	V
PCIe PHY 0.8-V power supply	PCV_{DD08}	−0.4	1.2	V
PCIe PHY 1.8-V power supply	PCV_{DD18}	−0.4	2.5	V
USB PHY HS section 3.3-V power supply	USV_{D330}	−0.4	3.8	V
USB PHY HS section 1.8-V power supply	USV_{DDH}	−0.4	2.5	V
USB PHY HS section 0.8-V power supply	$USDV_{DD}$	−0.4	1.2	V

Table 54.1-1 Absolute Maximum Ratings (3/3)

Item	Symbol	Min.	Max.	Unit
USB PHY SS section 0.8-V power supply	USV_P	−0.4	1.2	V
USB PHY SS section 3.3-V power supply	USV_{PH}	−0.4	3.8	V
USB3.0 transmitter power supply	USV_{PTX}	−0.4	1.2	V
Input voltage (1.1-V I/O)	V_{in11}	−0.4	LPV_{DDQ}+0.3*3	V
Input voltage (1.5-V I/O)	V_{in15}	−0.4	RTV_{DD} + 0.3*4	V
Input voltage (1.8-V I/O)*1	V_{in18}	−0.4	V_{18} + 0.3*5	V
Input voltage (1.8-V I/O (3.3-V tolerant))*2	V_{in18_tol}	−0.4	3.6	V
Input voltage (3.3-V I/O)	V_{in33}	−0.4	V_{33} + 0.3*6	V
Analog input voltage (ADC unit A AIN)	V_{ain18_0}	0	$AD0AV_{CCA}$	V
Analog input voltage (ADC unit B AIN)	V_{ain18_1}	0	$AD1AV_{CCA}$	V
Junction temperature	T_j	−40	125	°C
Storage temperature	T_{stg}	−40	150	°C

Note 1. 1.8-V I/O (except for PORT02 I/O and PORT05 I/O)

Note 2. 1.8-V I/O (PORT02 I/O and PORT05 I/O)

Note 3. The voltage to be applied must be within the absolute maximum rating (1.5 V).

Note 4. The voltage to be applied must be within the absolute maximum rating (2.5 V).

Note 5. The voltage to be applied must be within the absolute maximum rating (2.5 V). V18 indicates the power supply voltage for 1.8-V I/O pins.

Note 6. The voltage to be applied must be within the absolute maximum rating (3.8 V). V33 indicates the power supply voltage for 3.3-V I/O pins.

54.2 Recommended Operating Range

Table 54.2-1 Recommended Operating Range (1/2)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
VDD08 core power supply	V_{DD08}	0.76	0.8	0.84	V	
RTC core power supply	RTV_{DD08}	0.76	0.8	0.84	V	
RTC I/O, 1.5-V OSC power supply	RTV_{DD}	1.425	1.5	1.575	V	
PWC core power supply	PWV_{DD08}	0.76	0.8	0.84	V	
PWC I/O power supply	PWV_{DD}	1.71	1.8	1.89	V	
PORT01(A), PORT03 pre-driver power supply	$PAPREDV_{DD}$	1.71	1.8	1.89	V	
PORT01(A), PORT03 I/O power supply	$PAMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT01(B), PORT04, PORT07, PORT21 pre-driver power supply	$PBPREDV_{DD}$	1.71	1.8	1.89	V	
PORT01(B), PORT04, PORT07, PORT21 I/O power supply	$PBMODV_{DD}$/	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT06 pre-driver power supply	$PCPREDV_{DD}$	1.71	1.8	1.89	V	
PORT06 I/O power supply	$PCMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT10 pre-driver power supply	$IM0PREDV_{DD}$	1.71	1.8	1.89	V	
PORT10 I/O power supply	$IM0MODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT11 pre-driver power supply	$IM1PREDV_{DD}$	1.71	1.8	1.89	V	
PORT11 I/O power supply	$IM1MODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT00 pre-driver power supply	$NAPREDV_{DD}$	1.71	1.8	1.89	V	
PORT00 I/O power supply	$NAMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT08 pre-driver power supply	$SD0PREDV_{DD}$	1.71	1.8	1.89	V	
PORT08 I/O power supply	$SD0MODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT09 pre-driver power supply	$SD1FV_{DD}$	1.71	1.8	1.89	V	
PORT09 I/O power supply	$SD1FMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
PORT15, PORT16, PORT17 pre-driver power supply	$GEPREDV_{DD}$	1.71	1.8	1.89	V	
PORT15, PORT16, PORT17 I/O power supply	$GEMODV_{DD}$	3.135/1.71	3.3/1.8	3.465/1.89	V	3.3-V/1.8-V selectable
VDD18 group I/O power supply (PORT02 I/O, PORT05 I/O, PORT20 I/O, 1.8-V OSC, RSTN I/O, debugger I/O, MD0-7 I/O)	V_{DD18}	1.71	1.8	1.89	V	
VDD33 group pre-driver power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	$PREDV_{DD33}$	1.71	1.8	1.89	V	

Table 54.2-1 Recommended Operating Range (2/2)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
VDD33 group I/O power supply (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	V_{DD33}	3.135	3.3	3.465	V	
PLL ch. 1, 2, 3, 4, 6, 7 0.8-V power supply	$PLDV_{DD08n}$ (n = 1, 2, 3, 4, 6, 7)	0.76	0.8	0.84	V	
PLL ch. 1, 2, 3, 4, 6, 7 1.8-V power supply	PLVDDn (n = 1, 2, 3, 4 ,6, 7)	1.71	1.8	1.89	V	
OTP 0.8-V power supply	OTV_{DD08}	0.76	0.8	0.84	V	
OTP 1.8-V power supply	OTV_{DD18}	1.71	1.8	1.89	V	
TSU ch. 0 0.8-V power supply	$TS0DV_{DD08A}$	0.76	0.8	0.84	V	
TSU ch. 1 0.8-V power supply	$TS1DV_{DD08A}$	0.76	0.8	0.84	V	
TSU ch. 0 1.8-V power supply	$TS0AV_{DD18}$	1.71	1.8	1.89	V	
TSU ch. 1 1.8-V power supply	$TS1AV_{DD18}$	1.71	1.8	1.89	V	
ADC unit A 1.8-V power supply	$AD0AV_{CCA}$	1.71	1.8	1.89	V	
ADC unit B 1.8-V power supply	$AD1AV_{CCA}$	1.71	1.8	1.89	V	
CIF PHY 0.8-V power supply	$LVRXAV_{DD}$	0.76	0.8	0.84	V	
CIF PHY 1.8-V power supply	$LVRXAV_{CC}$	1.71	1.8	1.89	V	
LPDDR4 core 0.8-V power supply	LPV_{DD}	0.76	0.8	0.84	V	
LPDDR4 PLL 1.8-V power supply	LPV_{AA}	1.71	1.8	1.89	V	
LPDDR4 PHY 1.1-V power supply	LPV_{DDQ}	1.06	1.1	1.17	V	
HDMI PHY 0.8-V power supply	$HDAV_{DD08}$	0.76	0.8	0.84	V	
HDMI PHY 1.8-V power supply	$HDAV_{DD18}$	1.71	1.8	1.89	V	
MIPI DSI Tx PHY 0.8-V power supply	$DSMSV_{DD0P8}$	0.76	0.8	0.84	V	
MIPI DSI Tx PHY 1.8-V power supply	$DSMSV_{DD18}$	1.71	1.8	1.89	V	
MIPI DSI Tx PHY 1.2-V power supply	$DSMV_{DD12}$	1.14	1.2	1.26	V	
PCIe PHY 0.8-V power supply	PCV_{DD08}	0.76	0.8	0.84	V	
PCIe PHY 1.8-V power supply	PCV_{DD18}	1.71	1.8	1.89	V	
USB PHY SS section 0.8-V power supply	USV_{P}	0.76	0.8	0.84	V	
USB PHY HS section 1.8-V power supply	USV_{DDH}	1.71	1.8	1.89	V	
USB PHY HS section 3.3-V power supply	USV_{D330}	3.135	3.3	3.465	V	
USB PHY HS section 0.8-V power supply	$USDV_{DD}$	0.76	0.8	0.84	V	
USB PHY SS section transmitter power supply	USV_{PTX}	0.76	0.8	0.84	V	
USB PHY SS section 3.3-V power supply	USV_{PH}	3.135	3.3	3.465	V	
Junction temperature	T_j	—	—	103	°C	

54.3 Power-On/Off Procedures

54.3.1 Power-On/Off Sequence (RTC/PWC)

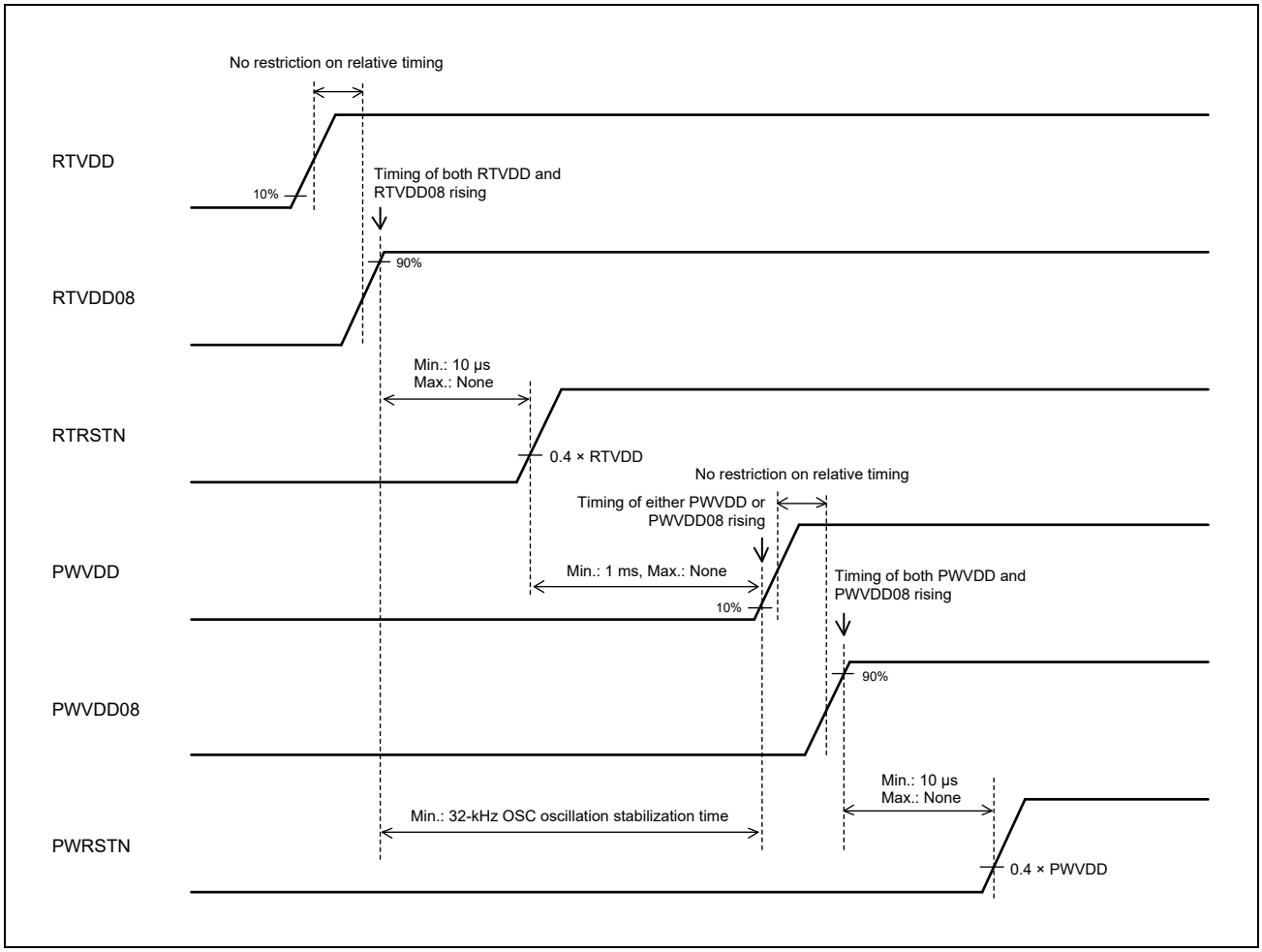


Figure 54.3-1 Power-On Sequence (RTC/PWC)

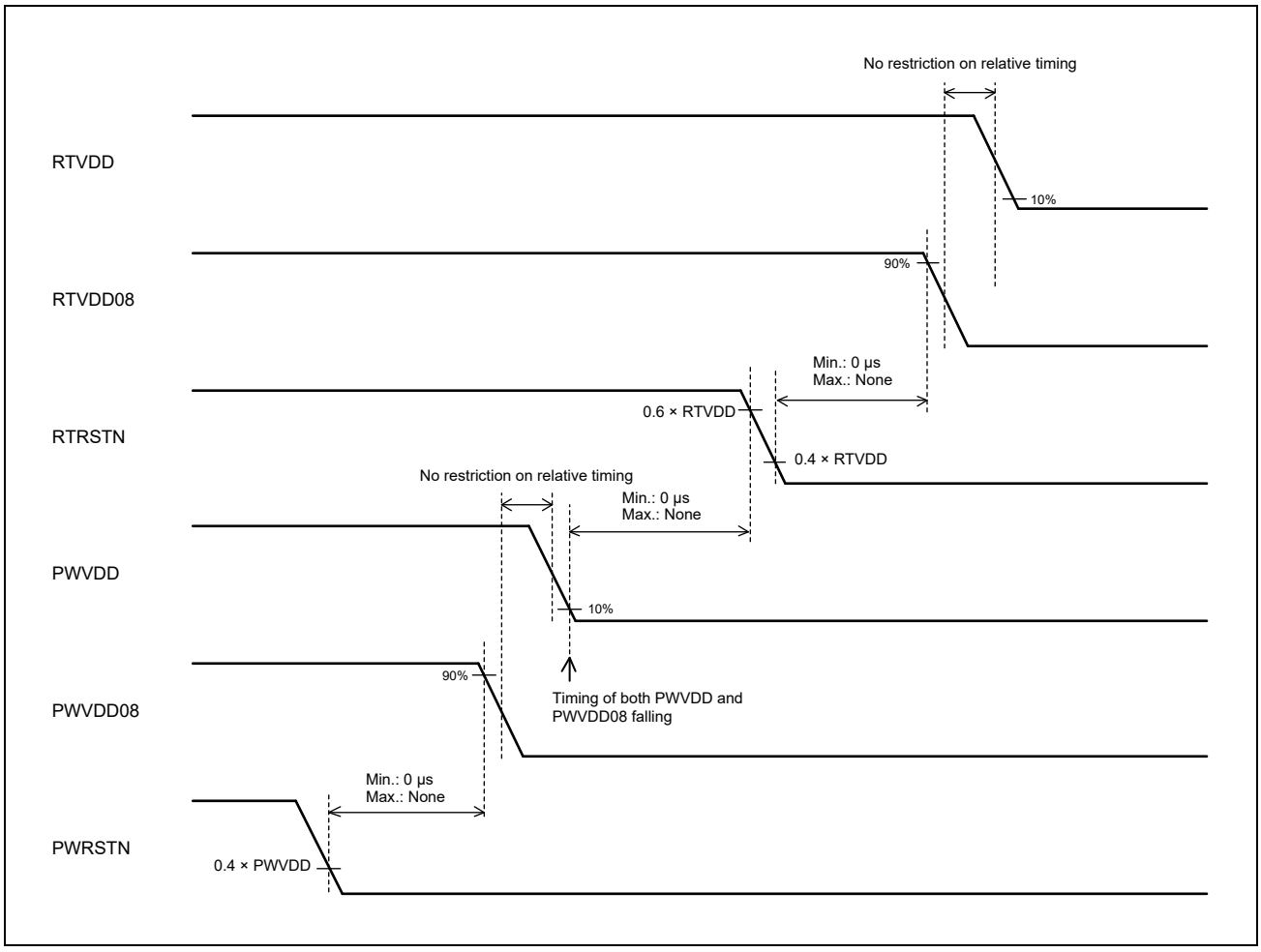
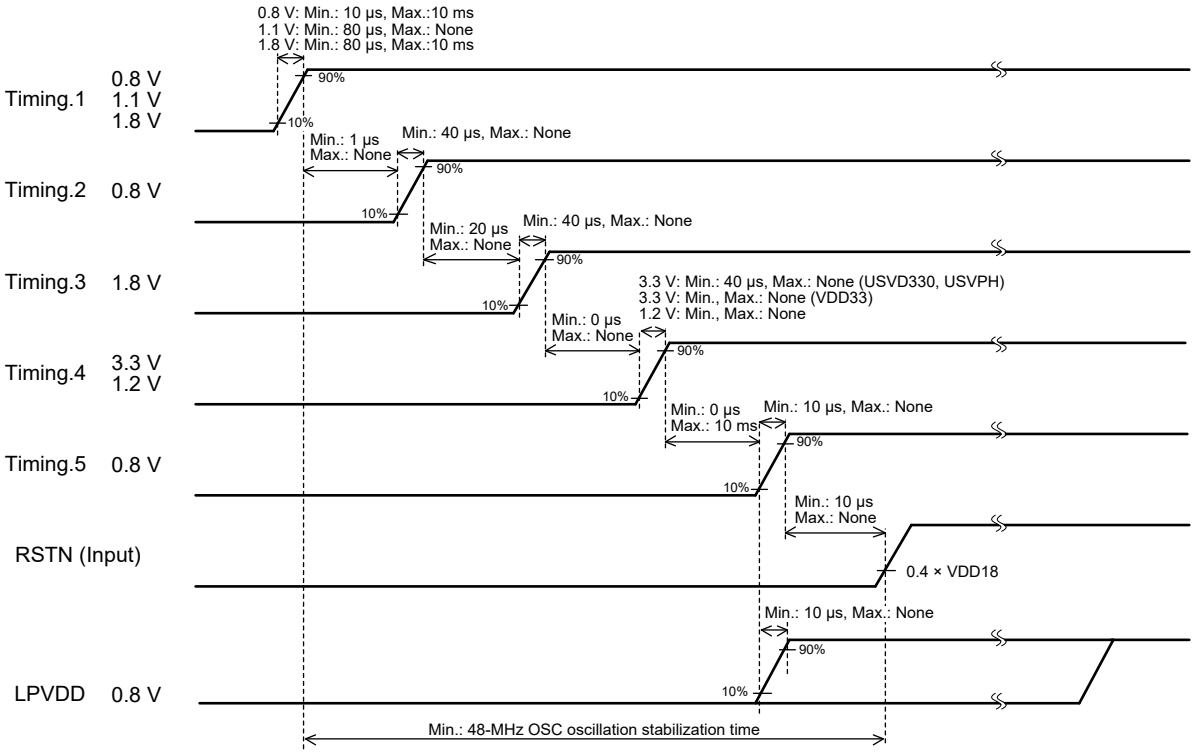


Figure 54.3-2 Power-Off Sequence (RTC/PWC)

54.3.2 Power-On/Off Sequence (other than for RTC/PWC)

54.3.2.1 Power-On Sequence (other than for RTC/PWC)



Note: See **Table 54.3-1**, **Table 54.3-2**, and **Table 54.3-3** for the power supplies which are turned on with the given timing.

Figure 54.3-3 Power-On Sequence (other than for RTC/PWC)

Table 54.3-1, **Table 54.3-2**, and **Table 54.3-3** show the correspondence between the power supplies and the power-on (off) timings.

Table 54.3-1 Various Power Supplies and Power On/Off Timings

Power Voltage	Power Supply Name	Timing
0.8 V	VDD08	Timing.1
1.1 V	LPVDDQ	
1.8 V	VDD18, LPVAA	
0.8 V	DSMSVDD0P8, PCVDD08, HDAVDD08, OTVDD08, LVRXAVDD	Timing.2
1.8 V	DSMSVDD18, PCVDD18, HDAVDD18, OTVDD18, LVRXAVCC, USVDDH	Timing.3
3.3 V	VDD33, USVD330, USVPH	Timing.4
1.2 V	DSMVDD12	
0.8 V	USDVDD, USVP, USVPTX, LPVDD*1	Timing.5

Note 1. When not controlled by the System FW, the power is on (off) at Timing.5.
When controlled by the System FW, connect the 0.8-V power supply to the LPVDD pin of this LSI via the power switch. In addition, connect the PWMEMSWIENA pin of this LSI to an enable pin of this power switch.

Table 54.3-2 Various Power Supplies and Power On/Off Timings (PLL, TSU, ADC, etc.)

Power Voltage	Power Supply Name	Timing
0.8 V	PLDVDD08n (n = 1, 2, 3, 4, 6, 7), TSnDVDD08A (n = 0, 1)	Timing.1 or Timing.2
1.8 V	PLVDDn (n = 1, 2, 3, 4, 6, 7), TSnAVDD18 (n = 0, 1), ADnAVCCA (n = 0, 1), PREDVDD33	Timing.1 or Timing.3

Table 54.3-3 Various Power Supplies and Power On/Off Timings (1.8-V/3.3-V Switching I/O)

I/O Voltage	Power Supply Name	Case	Timing
Used as the 1.8-V I/O	Pre-driver power supply*1	1	Timing.1
	I/O power supply*2		
	Pre-driver power supply*1	2	Timing.1
	I/O power supply*2		Timing.3
	Pre-driver power supply*1	3	Timing.3
	I/O power supply*2		
Used as the 3.3-V IO	Pre-driver power supply*1	4	Timing.1
	I/O power supply*2		Timing.4
	Pre-driver power supply*1	5	Timing.3
	I/O power supply*2		Timing.4

Note 1. NAPREDVDD, PAPREDVDD, PBPREDVDD, PCPREDVDD, SD0PREDVDD, SD1FVDD, IM0PREDVDD, IM1PREDVDD, GEPREDVDD

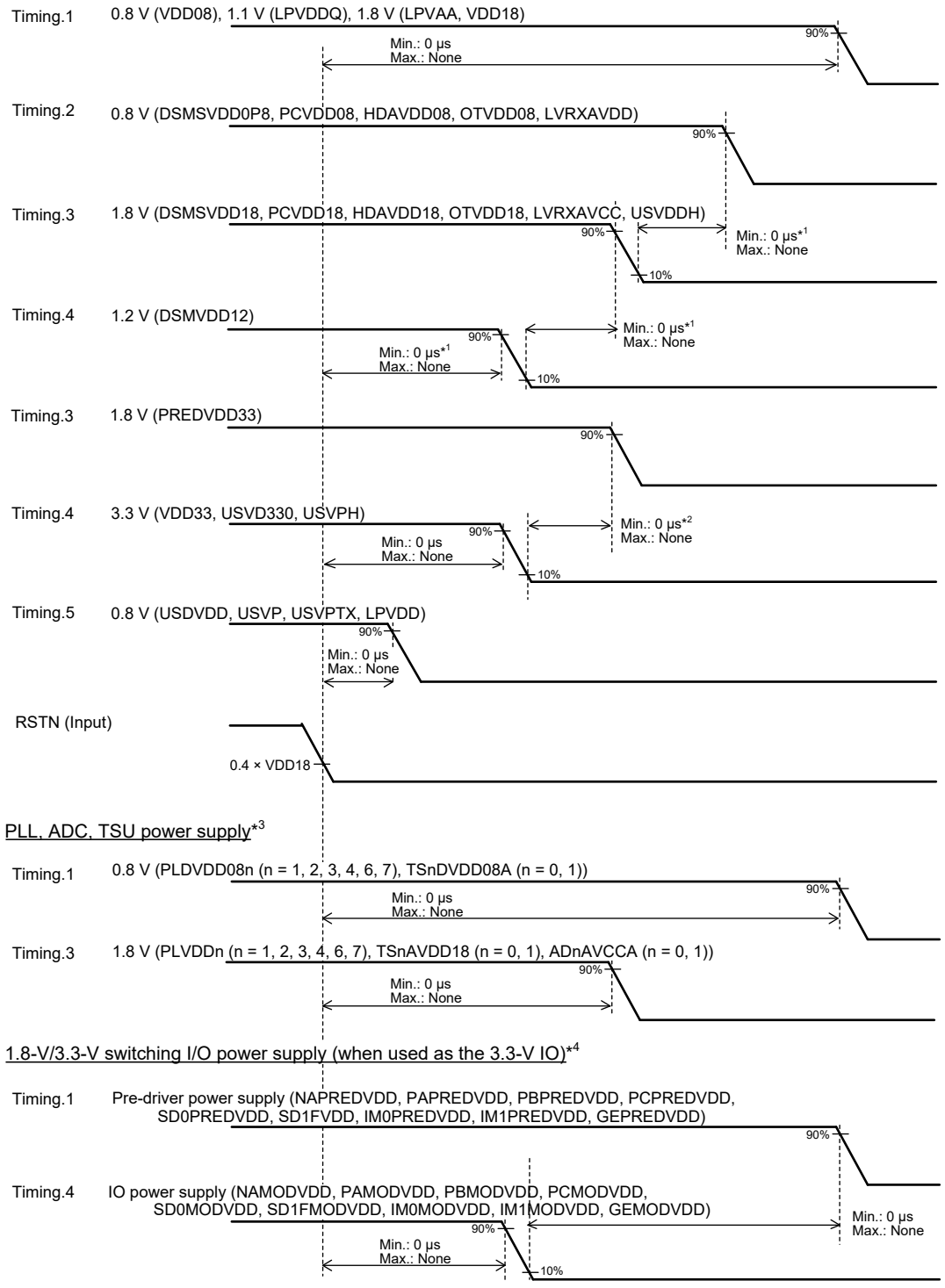
Note 2. NAMODVDD, PAMODVDD, PBMODVDD, PCMODVDD, SD0MODVDD, SD1FMODVDD, IM0MODVDD, IM1MODVDD, GEMODVDD

The following restrictions apply to the order of turning on the pre-driver power supply and the I/O power supply for the power supply of the 1.8-V/3.3-V switching I/O.

- When used as the 1.8-V I/O, “the pre-driver power supply and the I/O power supply are turned on at the same time” or “the pre-driver power supply is turned on first and then the I/O power supply”.
- When used as the 3.3-V I/O, “the pre-driver power supply is turned on first and then the I/O power supply”.

When used as the 1.8-V I/O, the pre-driver power supply and the I/O power supply must be turned on or off in case 1, 2, or 3. When used as the 3.3-V I/O, they must be turned on or off in case 4 or 5.

54.3.2.2 Power-Off Sequence (other than for RTC/PWC)



Note: The power off time difference must be minimized.

Note 1. The power supply in the case of Timing.2 (0.8 V) must be turned off no less than 0 ns after the power supply in the case of Timing.3 (1.8 V) is turned off and the power supply in the case of Timing.3 (1.8 V) must be turned off no less than 0 ns after the power supply in the case of Timing.4 (1.2 V) is turned off.

(*Continuation of the previous page*)

Note 2. The power supply in the case of Timing.3 (1.8 V) must be turned off no less than 0 ns after the power supply in the case of Timing.4 (3.3 V) is turned off.

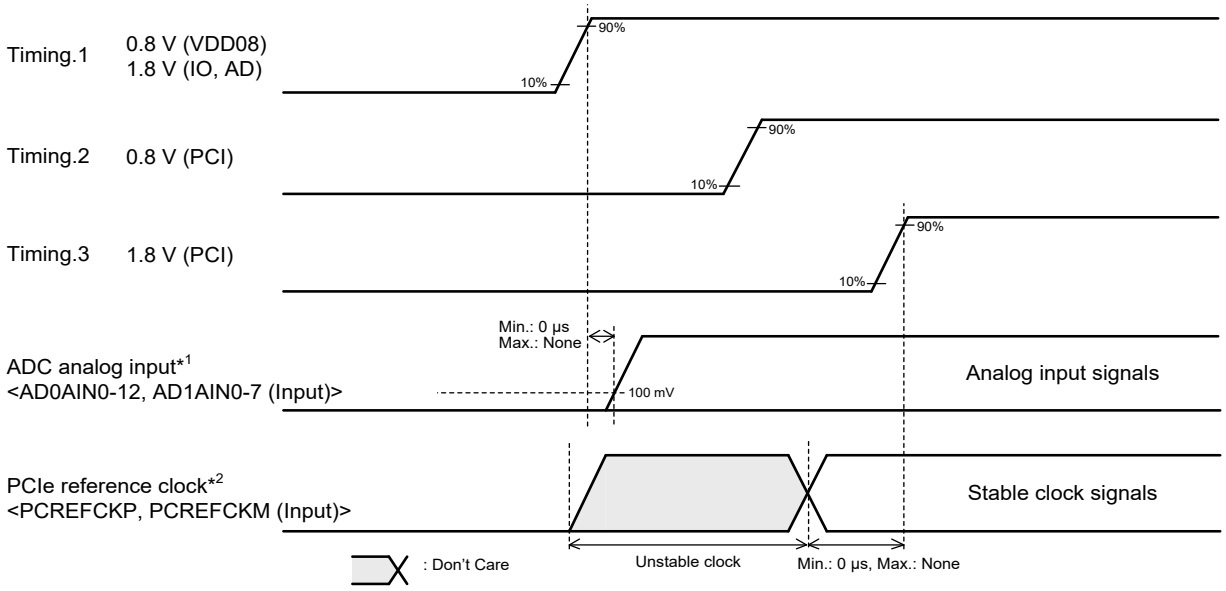
Note 3. The 0.8-V power supply and the 1.8-V power supply are indicated in the case of Timing.1 and Timing.3, respectively.
No restrictions apply to the order of turning off the 0.8-V power supply and the 1.8-V power supply.

Note 4. This is used as the 3.3-V I/O, and the pre-driver power supply and the I/O power supply are indicated in the case of Timing.1 and Timing.4, respectively.
The pre-driver power supply must be turned off no less than 0 ns after the I/O power supply is turned off.
When used as the 1.8-V I/O, no restrictions apply to the order of turning on the pre-driver power supply and the I/O power supply.

Figure 54.3-4 Power-Off Sequence (other than for RTC/PWC)

54.3.3 Timing Limitations when Power is being Turned On

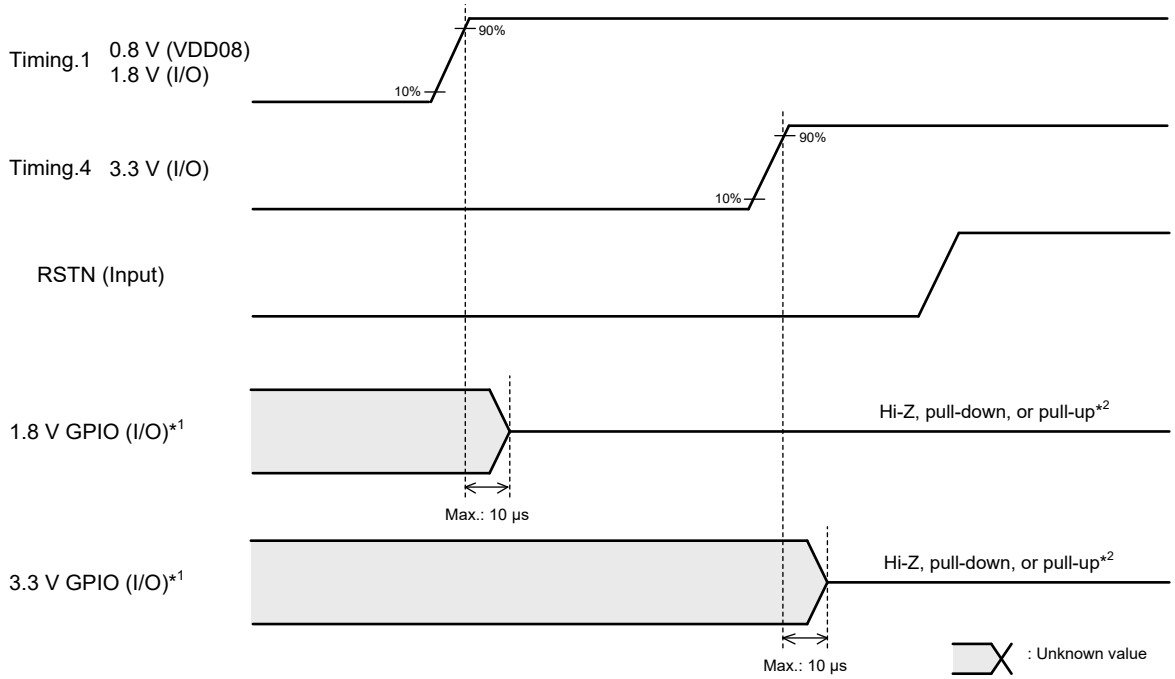
Control the input signals according to the timing limitations for power being turned on.



Note 1. Only apply analog input voltages after the ADC 1.8-V power supply voltages (AD0AVCCA, AD1AVCCA) have risen. Analog input voltages should be kept below 100 mV before the ADC 1.8-V power supplies have risen.

Note 2. For the PCIe reference clock, input the clock signal after the oscillation stabilization before the PCI 1.8-V power supply (PCVDD18) is risen.

Figure 54.3-5 ADC Analog Inputs at Power-On/PCI Reference Clock Input Timing



Note 1. After both the internal power and I/O power supply voltages (1.8 V or 3.3 V) have risen, the reset is effective by the time 10 µs (max.) have elapsed and the pin states are stable. The pin states are not guaranteed between the supply voltages rising and the reset becoming effective.

Note 2. The state depends on the pin. For the initial states of the respective pins, refer to “Initial Value after POR” in the list of external pins.

Figure 54.3-6 GPIO Timing at Power-On

54.4 DC Characteristics

54.4.1 Supply Current

54.4.1.1 Maximum Supply Current

Conditions for the supply current: Power supply voltage = Max. value, Tj = −40 to 125ºC

Table 54.4-1 Max. Supply Currents during Operation (1/2)

Item	Symbol	Max.	Unit	Note
VDD08 core power supply current	I_{DD08}	4770	mA	The current must be within the maximum supply current.
RTC core power supply current	$I_{DDRTVDD08}$	700	µA	RTV_{DD08}*1
RTC I/O, 1.5-V OSC power supply current	$I_{DDRTVDD}$	300*3	µA	RTV_{DD}*2
PWC core power supply current	$I_{DDPWVDD08}$	1	mA	PWV_{DD08}
PWC I/O power supply current	$I_{DDPWVDD}$	3	mA	PWV_{DD}
PORT01(A), PORT03 pre-driver power supply current	$I_{DDPAPRE}$	2	mA	$PAPREDV_{DD}$: PWM0 - 7, CSI0, TRDAT6 - 15
PORT01(A), PORT03 I/O power supply current	$I_{DDPAMOD}$	23	mA	$PAMODV_{DD}$: PWM0 - 7, CSI0, TRDAT6 - 15
PORT01(B), PORT04, PORT07, PORT21 pre-driver power supply current	$I_{DDPBPRE}$	1	mA	$PBPREDV_{DD}$: PWM8 - 15, TRACE0 - 6, AUI
PORT01(B), PORT04, PORT07, PORT21 I/O power supply current	$I_{DDPBMOD}$	16	mA	$PBMODV_{DD}$: PWM8 - 15, TRACE0 - 6, AUI
PORT06 pre-driver power supply current	$I_{DDPCPRE}$	1	mA	$PCPREDV_{DD}$: P0600 - 11
PORT06 I/O power supply current	$I_{DDPCMOD}$	11	mA	$PCMODV_{DD}$: P0600 - 11
PORT10 pre-driver power supply current	$I_{DDIM0PRE}$	1	mA	$IM0PREDV_{DD}$
PORT10 I/O power supply current	$I_{DDIM0MOD}$	4	mA	$IM0MODV_{DD}$
PORT11 pre-driver power supply current	$I_{DDIM1PRE}$	1	mA	$IM1PREDV_{DD}$
PORT11 I/O power supply current	$I_{DDIM1MOD}$	4	mA	$IM1MODV_{DD}$
PORT00 pre-driver power supply current	$I_{DDNAPRE}$	2	mA	$NAPREDV_{DD}$: eMMC HS200
PORT00 I/O power supply current	$I_{DDNAMOD}$	10	mA	$NAMODV_{DD}$: eMMC HS200
PORT08 pre-driver power supply current	$I_{DDSD0PRE}$	1	mA	$SD0PREDV_{DD}$: SDIO SDR104
PORT08 I/O power supply current	$I_{DDSD0MOD}$	16	mA	$SD0MODV_{DD}$: SDIO SDR104
PORT09 pre-driver power supply current	I_{DDSD1F}	1	mA	$SD1FV_{DD}$: SDIO SDR104
PORT09 I/O power supply current	$I_{DDSD1MOD}$	16	mA	$SD1FMODV_{DD}$: SDIO SDR104
PORT15, PORT16, PORT17 pre-driver power supply current	$I_{DDGEPRE}$	1	mA	$GEPREDV_{DD}$
PORT15, PORT16, PORT17 I/O power supply current	$I_{DDGEMOD}$	17	mA	$GEMODV_{DD}$
VDD18 group I/O power supply current (PORT02 I/O, PORT05 I/O, PORT20 I/O. 1.8-V OSC, RSTN I/O, debugger I/O, MD0-7 I/O)	I_{DD18}	3	mA	V_{DD18}: IIC0 - 1, DEBUG

Table 54.4-1 Max. Supply Currents during Operation (2/2)

Item	Symbol	Max.	Unit	Note
VDD33 group pre-driver power supply current (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	$I_{DDPRE33}$	2	mA	$PREDV_{DD33}$
VDD33 group I/O power supply current (PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O)	I_{DD33}	20	mA	V_{DD33}
PLL ch. 1, 2, 3, 4, 6, 7 0.8-V power supply current	I_{DDPL08}	16	mA	Total of $PLDV_{DD081}$, $PLDV_{DD082}$, $PLDV_{DD083}$, $PLDV_{DD084}$, $PLDV_{DD086}$, $PLDV_{DD087}$
PLL ch. 1, 2, 3, 4, 6, 7 1.8-V power supply current	I_{DDPL18}	14	mA	Total of PLV_{DD1}, PLV_{DD2}, PLV_{DD3}, PLV_{DD4}, PLV_{DD6}, PLV_{DD7}
OTP 0.8-V power supply current	I_{DDOT08}	9	mA	OTV_{DD08}
OTP 1.8-V power supply current	I_{DDOT18}	60	mA	OTV_{DD18}
TSU ch. 0 0.8-V power supply current	I_{DDTS08}	1	mA	$TS0DV_{DD08A}$
TSU ch. 1 0.8-V power supply current	I_{DDTS08}	1	mA	$TS1DV_{DD08A}$
TSU ch. 0 1.8-V power supply current	I_{DDTS18}	4	mA	$TS0AV_{DD18}$
TSU ch. 1 1.8-V power supply current	I_{DDTS18}	4	mA	$TS1AV_{DD18}$
ADC unit A 1.8-V power supply current	I_{DDAD0}	1	mA	$AD0AV_{CCA}$
ADC unit B 1.8-V power supply current	I_{DDAD1}	1	mA	$AD1AV_{CCA}$
CIF PHY 0.8-V power supply current	$I_{DDLVVDD}$	127	mA	$LVRXAV_{DD}$
CIF PHY 1.8-V power supply current	$I_{DDLVVCC}$	81	mA	$LVRXAV_{CC}$
LPDDR4 core 0.8-V power supply current	$I_{DDLPVDD}$	800	mA	LPV_{DD}: 3200 Mbps
LPDDR4 PLL 1.8-V power supply current	$I_{DDLPVAA}$	6	mA	LPV_{AA}: 3200 Mbps
LPDDR4 PHY 1.1-V power supply current	$I_{DDLPVDDQ}$	314	mA	LPV_{DDQ}: 3200 Mbps
HDMI PHY 0.8-V power supply current	I_{DDHD08}	24	mA	$HDAV_{DD08}$
HDMI PHY 1.8-V power supply current	I_{DDHD18}	10	mA	$HDAV_{DD18}$
MIPI DSI Tx PHY 0.8-V power supply current	$I_{DDDSM08}$	2	mA	$DSMSV_{DD0P8}$
MIPI DSI Tx PHY 1.8-V power supply current	$I_{DDDSM18}$	30	mA	$DSMSV_{DD18}$
MIPI DSI Tx PHY 1.2-V power supply current	$I_{DDDSM12}$	8	mA	$DSMV_{DD12}$
PCIe PHY 0.8-V power supply current	I_{DDPC08}	188	mA	PCV_{DD08}
PCIe PHY 1.8-V power supply current	I_{DDPC18}	132	mA	PCV_{DD18}
USB PHY 0.8-V power supply current	I_{DDUS08}	88	mA	Total of $USDV_{DD}$, USV_{P}, USV_{PTX}
USB PHY 1.8-V power supply current	I_{DDUS18}	21	mA	USV_{DDH}
USB PHY 3.3-V power supply current	I_{DDUS33}	57	mA	Total of USV_{D330}, USV_{PH}

Note 1. Reference value for the RTC core power supply current (at normal temperature at 0.8 V): 35 µA

Note 2. Reference value for the RTC I/O, 1.5-V OSC power supply current (at normal temperature at 1.5 V): 10 µA

Note 3. In normal operation (when the power supplies other than for the RTC power domain are turned on), current flows to the PWISO pin via a pull-up resistor, so this amount of current must be taken into account when the current drawn is estimated.
[*Example*] When the pull-up resistance is 10 kΩ, 1.5 V/10 kΩ = 150 µA

54.4.2 Standard I/O Characteristics

For the I/O groups, refer to the multiplexed pin group numbers in the list of external pins.

Table 54.4-2 DC Characteristics

V_{DD} = 1.35 V to 1.65 V (I.5-V I/O group), V_{DD} = 1.65 V to 1.95 V (1.8-V I/O groups 1, 2, 3, and 4), V_{DD} = 1.65 V to 3.60 V (3.3/1.8-V switching I/O groups 1 and 2), V_{DD} = 3.00 V to 3.60 V (3.3-V I/O group)

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
External voltage tolerance	1.8-V I/O group 3*4	V_{TOL}	—	—	3.6	V	V_{DD} power-off & on
High-level input voltage	—	V_{IH}	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
Low-level input voltage	—	V_{IL}	−0.3	—	0.3 × V_{DD}	V	—
Hysteresis voltage	1.5-V I/O group*1	ΔV	0.1 × V_{DD}	—	—	V	—
	1.8-V I/O group 1*2 1.8-V I/O group 2*3	ΔV	0.1 × V_{DD}	—	—	V	
	1.8-V I/O group 3*4	ΔV	0.08 × V_{DD}	—	—	V	
	3.3/1.8-V switching I/O group 1*6	ΔV	0.08 × V_{DD}	—	—	V	
	3.3/1.8-V switching I/O group 2*7	ΔV	0.1 × V_{DD}	—	—	V	
	3.3-V I/O group*8	ΔV	0.08 × V_{DD}	—	—	V	
High-level input current (Non-tolerant input buffer)	1.5V I/O group*1	I_{IH}	−12	—	12	μA	V_{in15} = V_{DD} max & V_{DD} power-on
	1.8-V I/O group 1*2 1.8-V I/O group 2*3 1.8-V I/O group 4*5	I_{IH}	−12	—	12	μA	V_{in18} = V_{DD} max & V_{DD} power-on
	3.3/1.8-V switching I/O group 1*6 3.3/1.8-V switching I/O group 2*7	I_{IH}	−12	—	12	μA	Vin_{33} = V_{DD} max & V_{DD} power-on
	3.3-V I/O group*8	I_{IH}	−12	—	12	μA	
High-level input current (Tolerant input buffer)	1.8-V I/O group 3*4	I_{IH}	−12	—	12	μA	V_{in18_tol} = V_{DD} max & V_{DD} power-on
High-level input current (Input buffer with pull-down resistor)	1.8-V I/O group 3*4 1.8-V I/O group 4*5	I_{IH}	25	—	200	μA	V_{in18} = V_{DD} max
	3.3/1.8-V switching I/O group 1*6	I_{IH}	25	—	200	μA	V_{in33} = V_{DD} max
	3.3/1.8-V switching I/O group 2*7	I_{IH}	35	—	150	μA	
	3.3-V I/O group*8	I_{IH}	25	—	200	μA	
Low-level input current (Non-tolerant input buffer)	1.5-V I/O group*1	I_{IL}	−12	—	12	μA	V_{in15} = V_{SS}
	1.8-V I/O group 1*2 1.8-V I/O group 2*3	I_{IL}	−12	—	12	μA	V_{in18} = V_{SS}
	1.8-V I/O group 4*5	I_{IL}	−18	—	18	μA	
	3.3/1.8-V switching I/O group 1*6	I_{IL}	−18	—	18	μA	V_{in33} = V_{SS}
	3.3/1.8-V switching I/O group 2*7	I_{IL}	−12	—	12	μA	
	3.3-V I/O group*8	I_{IL}	−18	—	18	μA	
Low-level input current (Tolerant input buffer)	1.8-V I/O group 3*4	I_{IL}	−18	—	18	μA	V_{in18_tol} = V_{SS}
Low-level input current (Input buffer with pull-down resistor)	1.8-V I/O group 2*3	I_{IL}	−9	—	−180	μA	V_{in18} = V_{SS}
	1.8-V I/O group 3*4 1.8-V I/O group 4*5	I_{IL}	−25	—	−200	μA	
	3.3/1.8-V switching I/O group 1*6	I_{IL}	−25	—	−200	μA	V_{in33} = V_{SS}
	3.3/1.8-V switching I/O group 2*7	I_{IL}	−35	—	−190	μA	
	3.3-V I/O group*8	I_{IL}	−25	—	−200	μA	

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
High-level output voltage	1.5-V I/O group*1	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −1.8 mA-
	1.8-V I/O group 1*2	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −3.8 mA
	1.8-V I/O group 2*3	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −1.8/−3.8/−7.8/−11 mA (drive strength X1/X2/X4/X6)
	1.8-V I/O group 3*4	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −1.6/−3.2/−6.4/−9.6 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 1 (1.8 V)*6	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −1.6/−3.2/−6.4/−9.6 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 1 (3.3 V)*6	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −2/−4/−8/−12 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 2 (1.8 V)*7	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −5/−6/−7/−10 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 2 (3.3 V)*7	V_{OH}	0.8×V_{DD}	—	V_{DD}	V	I_{OH} = −9/−11/−13/−18 mA (drive strength X1/X2/X4/X6)
	3.3-V I/O group*8	V_{OH}	0.8 × V_{DD}	—	V_{DD}	V	I_{OH} = −2/−4/−8/−12 mA (drive strength X1/X2/X4/X6)
Low-level output voltage	1.5-V I/O group*1	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 1.8 mA
	1.8-V I/O group 1*2	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 3.8 mA
	1.8-V I/O group 2*3	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 1.8/3.8/7.8/11 mA (drive strength X1/X2/X4/X6)
	1.8-V I/O group 3*4	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 1.6/3.2/6.4/9.6 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 1 (1.8 V)*6	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 1.6/3.2/6.4/9.6 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 1 (3.3 V)*6	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 2/4/8/12 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 2 (1.8 V)*7	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 5/6/7/10 mA (drive strength X1/X2/X4/X6)
	3.3/1.8-V switching I/O group 2 (3.3 V)*7	V_{OL}	0	—	0.2×V_{DD}	V	I_{OL} = 9/11/13/18 mA (drive strength X1/X2/X4/X6)
	3.3-V I/O group*8	V_{OL}	0	—	0.2 × V_{DD}	V	I_{OL} = 2/4/8/12 mA (drive strength X1/X2/X4/X6)
Pull-up resistance	1.8-V I/O group 2*3	R_{PU}	11	—	47	kΩ	—
	1.8-V I/O group 3*4 1.8-V I/O group 4*5	R_{PU}	11	—	49	kΩ	—
	3.3/1.8-V switching I/O group 1 (1.8 V)*6	R_{PU}	11	—	49	kΩ	—
	3.3/1.8-V switching I/O group 1 (3.3 V)*6	R_{PU}	15	—	83	kΩ	—
	3.3/1.8-V switching I/O group 2 (1.8 V)*7	R_{PU}	12	—	92	kΩ	—
	3.3/1.8-V switching I/O group 2 (3.3 V)*7	R_{PU}	18	—	72	kΩ	—
	3.3-V I/O group*8	R_{PU}	15	—	83	kΩ	—

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Pull-down resistance	1.8-V I/O group 3*4 1.8V I/O group 4*5	R_{PD}	12	—	45	kΩ	—
	3.3/1.8-V switching I/O group 1 (1.8 V)*6	R_{PD}	12	—	45	kΩ	—
	3.3/1.8-V switching I/O group 1 (3.3 V)*6	R_{PD}	20	—	75	kΩ	—
	3.3/1.8-V switching I/O group 2 (1.8 V)*7	R_{PD}	13	—	92	kΩ	—
	3.3/1.8-V switching I/O group 2 (3.3 V)*7	R_{PD}	24	—	87	kΩ	—
	3.3-V I/O group*8	R_{PD}	20	—	75	kΩ	—
Input capacitance	—	C_{in}	—	—	10	pF	

Note 1. Target I/O group: 1.5-V OSC, RTC I/O

Note 2. Target I/O group: PWC I/O

Note 3. Target I/O group: PORT20 I/O, RSTN I/O, 1.8-V OSC

Note 4. Target I/O group: PORT02 I/O, PORT05 I/O

Note 5. Target I/O group: MD0-7 I/O, debugger I/O

Note 6. Target I/O group:
PORT01(A) I/O, PORT03 I/O, PORT01(B) I/O, PORT04 I/O, PORT07 I/O, PORT21 I/O, PORT06 I/O, PORT10 I/O, PORT11 I/O

Note 7. Target I/O group:
PORT00 I/O, PORT08 I/O, PORT09 I/O, PORT15 I/O, PORT16 I/O, PORT17 I/O

Note 8. Target I/O group:
PORT12 I/O, PORT13 I/O, PORT14 I/O, PCIe I/O, USB I/O, LSI test I/O

54.5 AC Characteristics

AC characteristics measurement conditions

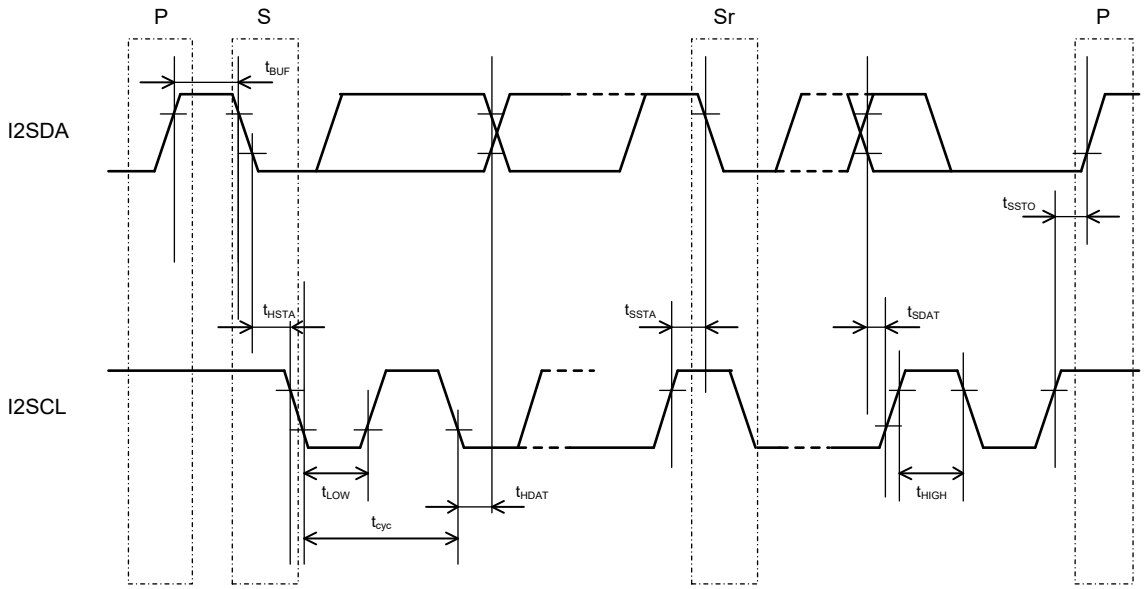
- I/O signal reference levels:
  $V_{DD18}/2$, $V_{DD33}/2$, NAMODV$_{DD}/2$, PAMODC$_{DD}/2$, PBMODV$_{DD}/2$, PCMODV$_{DD}/2$, SD0MODV$_{DD}/2$, SD1FMODV$_{DD}/2$, IM0MODV$_{DD}/2$, GEMODV$_{DD}/2$, IM1MODV$_{DD}/2$, V_{IH}, V_{OH} (min.), V_{IL}, V_{OL} (max.)
  (Refer to the corresponding timing charts.)
- Output load: C_L = 20 pF if not otherwise stated

54.5.1 IIC Bus Interface

Table 54.5-1 IIC Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
I2SCLn cycle time	t_{cyc}	2500	—	—	ns	
I2SCLn low level width	t_{LOW}	1300	—	—	ns	
I2SCLn high level width	t_{HIGH}	600	—	—	ns	
Bus free time (time from start to stop condition)	t_{BUF}	1300	—	—	ns	
Start condition hold time	t_{HSTA}	600	—	—	ns	
Restart condition setup time	t_{SSTA}	600	—	—	ns	
Stop condition setup time	t_{SSTO}	600	—	—	ns	
I2SDAn setup time	t_{SDAT}	100	—	—	ns	
I2SDAn hold time	t_{HDAT}	0	—	900	ns	

Note: n = 0 to 3



Note: S: START condition
P: STOP condition
Sr: Repeated START condition

Figure 54.5-1 IIC Timing

54.5.2 Clocked Serial Interface (CSI)

54.5.2.1 Master Mode

Table 54.5-2 Master Mode Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
CSSCLKn cycle time	t_{cyc}	41.66	—	—	ns	
CSSCLKn output low level width	t_{LOW}	18	—	—	ns	Falling edge mode*1
CSSCLKn output high level width	t_{HIGH}	18	—	—	ns	Rising edge mode*1
CSRXDn setup time (CSSCLKn rising and falling edges)	t_{SRXD}	t_{LOW} − 9	—	—	ns	
CSRXDn hold time (CSSCLKn rising and falling edges)	t_{HRXD}	5.0	—	—	ns	
CSTXDn output delay time (CSSCLKn rising and falling edges)	t_{DTXD}	−5.0	—	7.5	ns	*1

Note: n = 0 to 5

Note 1. The 3-wire serial interface (CSI) should be used with a drive strength of at least X2.
Select one of the drive strengths listed below according to the load capacitance.
X2@C_L = 15 pF, X4@C_L = 20 pF

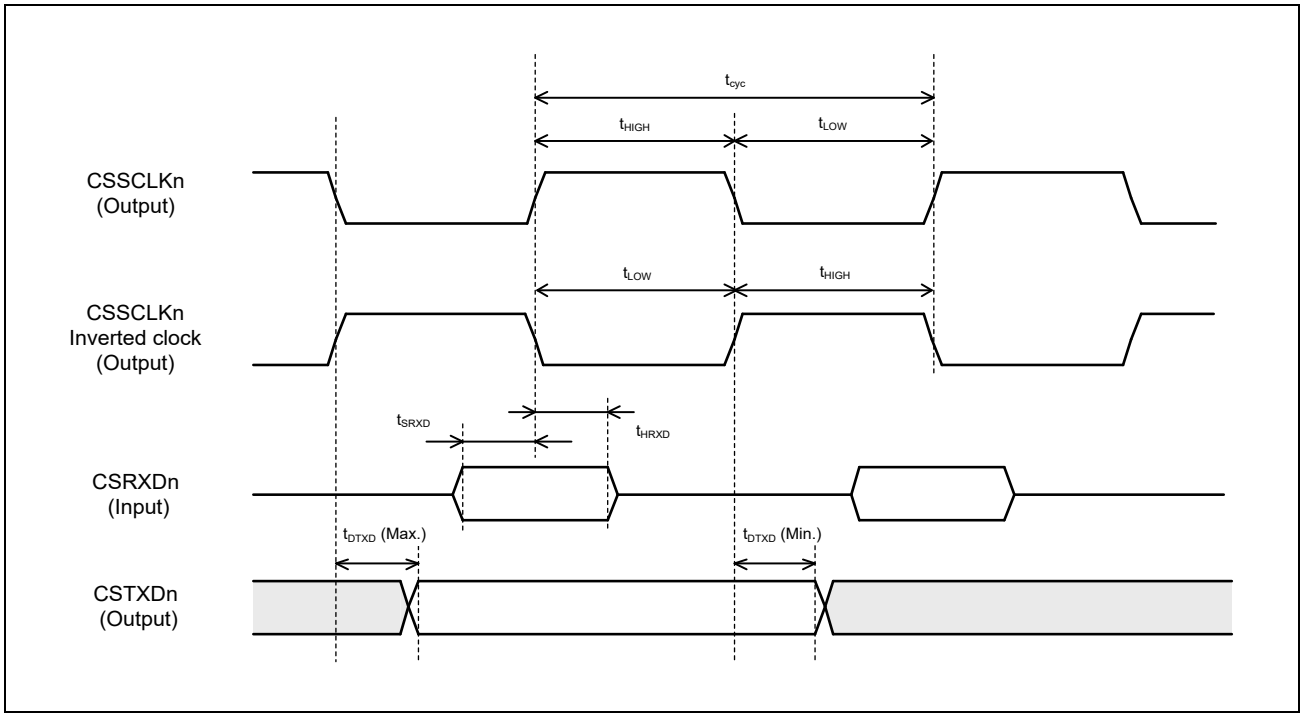


Figure 54.5-2 Master Mode Timing

54.5.2.2 Slave Mode

Table 54.5-3 Slave Mode Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
CSSCLKn cycle time	t_{cyc}	41.66	—	—	ns	
CSSCLKn input low level width	t_{LOW}	18	—	—	ns	Falling edge mode
CSSCLKn input high level width	t_{HIGH}	18	—	—	ns	Rising edge mode
CSRXDn setup time (CSSCLKn rising and falling edges)	t_{SRXD}	7.5	—	—	ns	
CSRXDn hold time (CSSCLKn rising and falling edges)	t_{HRXD}	5.0	—	—	ns	
CSCSn setup time (CSSCLKn rising and falling edges)	t_{SCS}	84	—	—	ns	
CSCSn hold time (CSSCLKn rising and falling edges)	t_{HCS}	21	—	—	ns	
CSTXDn output delay time (CSSCLKn rising and falling edges)	t_{DTXD}	−5.0	—	10.5	ns	*1

Note: n=0 to 5

Note 1. The 3-wire serial interface (CSI) should be used with a drive strength of at least X2.
Select one of the drive strengths listed below according to the load capacitance.
X2@C_L = 15 pF, X4@C_L = 20 pF

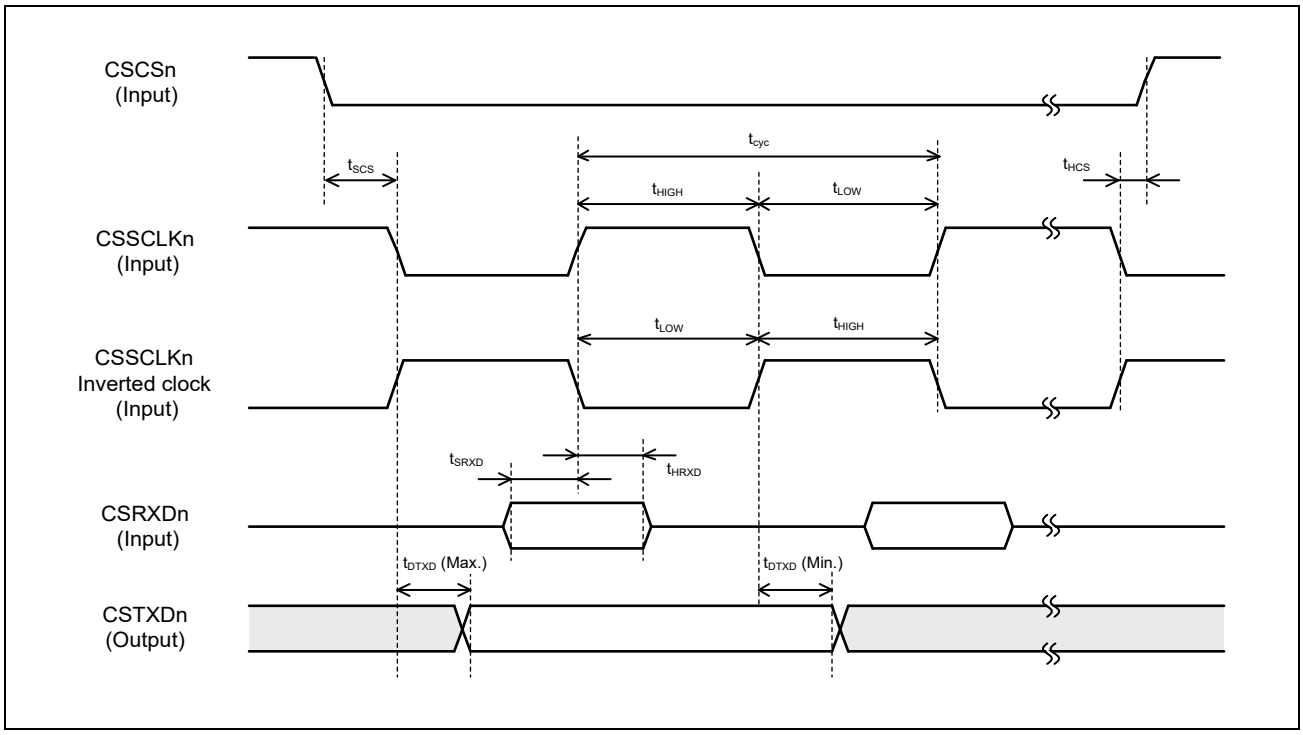


Figure 54.5-3 Slave Mode Timing

54.5.3 Ethernet MAC interface (ETHER)

54.5.3.1 100-Mbps Ethernet Mode

Table 54.5-4 100-Mbps Ethernet Mode Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
GETXC cycle time	t_{Tcyc}	39.5	40	40.5	ns	
GETXEN output delay time	t_{DTXE}	0	—	25	ns	
GETXD output delay time	t_{DTXD}	0	—	25	ns	
GERXC cycle time	t_{Rcyc}	39.5	40	40.5	ns	
GERXDV setup time	t_{SRXV}	10	—	—	ns	
GERXDV hold time	t_{HRXV}	10	—	—	ns	
GERXD setup time	t_{SRXD}	10	—	—	ns	
GERXD hold time	t_{HRXD}	10	—	—	ns	
GERXER setup time	t_{SRER}	10	—	—	ns	
GERXER hold time	t_{HRER}	10	—	—	ns	

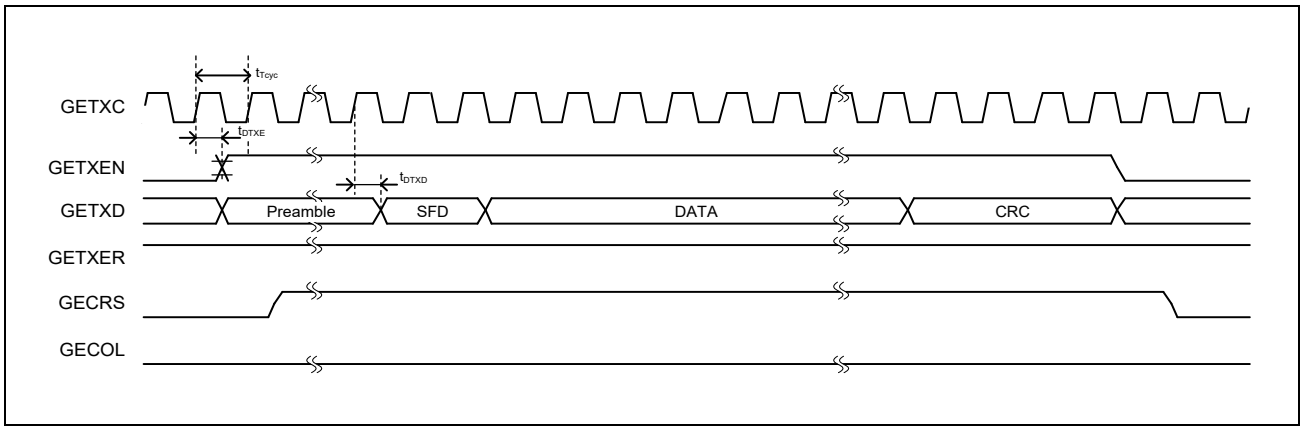


Figure 54.5-4 Transmission Timing

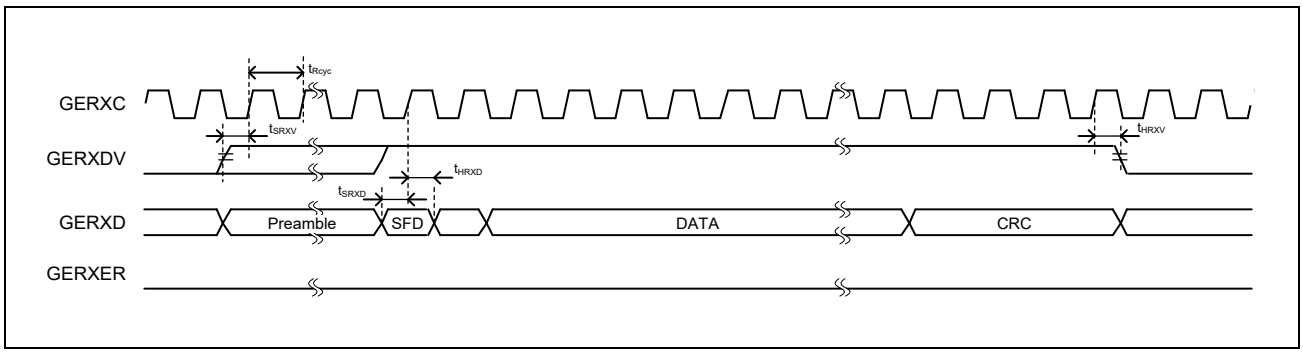


Figure 54.5-5 Reception Timing (Normal)

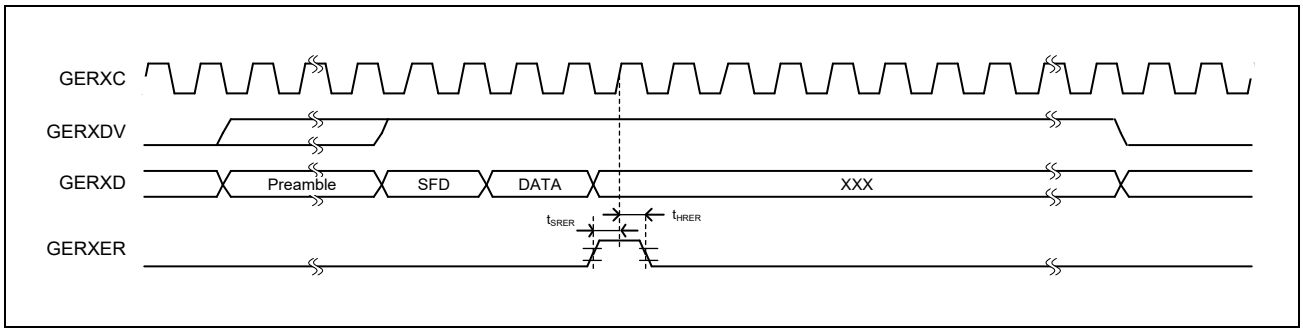


Figure 54.5-6 Reception Timing (in Cases of Error)

54.5.3.2 1-Gbps Ethernet Mode

Table 54.5-5 1-Gbps Ethernet Mode Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
GECLK input frequency	$f_{REF125CK}$	125 − 100 ppm	—	125 + 100 ppm	MHz	
GECLK input duty ratio	I_{DUTY}	45	50	55	%	
GEGTXCLK cycle time	t_{GTcyc}	7.5	8	8.5	ns	
GETXEN output delay time	t_{DGTXE}	0.5	—	5.5	ns	
GETXD output delay time	t_{DGTXD}	0.5	—	5.5	ns	
GERXC cycle time	t_{GRcyc}	7.5	8	8.5	ns	
GERXDV setup time	t_{SGRXV}	2.5	—	—	ns	
GERCDV hold time	t_{HGRXV}	0.5	—	—	ns	
GERXD setup time	t_{SGRXD}	2.5	—	—	ns	
GERXD hold time	t_{HGRXD}	0.5	—	—	ns	
GERXER setup time	t_{SGRER}	2.5	—	—	ns	
GERXER hold time	t_{HGRER}	0.5	—	—	ns	

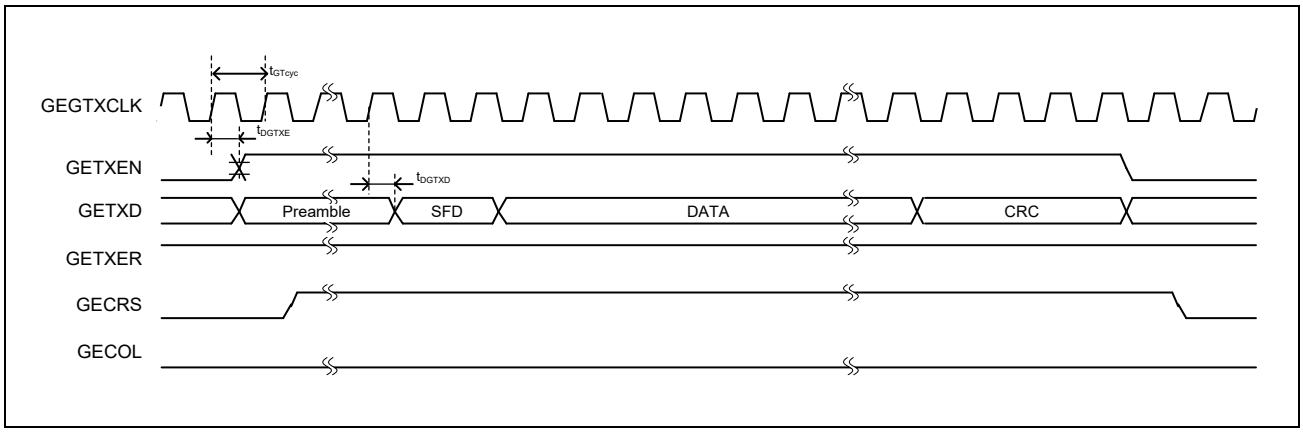


Figure 54.5-7 Transmission Timing

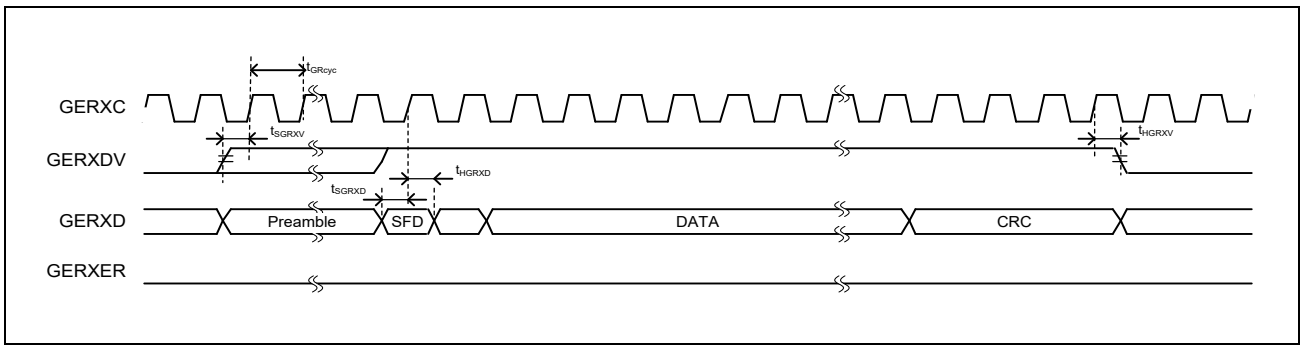


Figure 54.5-8 Reception Timing (Normal)

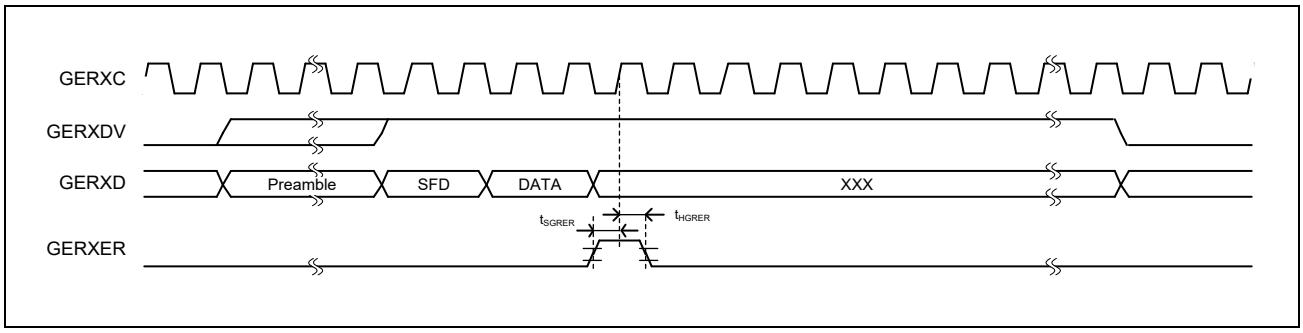


Figure 54.5-9 Reception Timing (in Cases of Error)

54.5.4 SD Host Interface (SDI)

This LSI includes the SD host interfaces that are compliant with *the SD specification version 3.01*.

54.5.5 eMMC Interface (eMMC)

The eMMC interface should be used with a drive strength of at least X2.

Table 54.5-6 HS200 Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
MMCLK cycle time	t_{cyc}	5	—	10	ns	C_L = 15 pF V_{OH} = 0.65 × V_{DD}(NAMODV$_{DD}$) V_{OL} = 0.35 × V_{DD}(NAMODV$_{DD}$)
MMCLK output low level width	t_{LOW}	1.5	—	—	ns	
MMCLK output high level width	t_{HIGH}	1.5	—	—	ns	
MMCLK rise time	t_r	—	—	1	ns	
MMCLK fall time	t_f	—	—	1	ns	
MMCMD/ MMDAT output delay time	t_{DDAT}	−1.5	—	0.9	ns	
MMCMD/ MMDAT setup time*1	t_{SDAT}	—	—	—	ns	
MMCMD/ MMDAT hold time*1	t_{HDAT}	—	—	—	ns	
MMCMD/ MMDAT data width*1	t_{WDAT}	2.88	—	—	ns	

Note 1. In HS200 mode, the sampling clock controller (SCC) must be used for tuning.

Table 54.5-7 High Speed Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
MMCLK cycle time	t_{cyc}	20	—	—	ns	C_L = 30 pF 1.8-V operation: V_{OH} = 0.65 × V_{DD}(NAMODV$_{DD}$) V_{OL} = 0.35 × V_{DD}(NAMODV$_{DD}$) 3.3-V operation: V_{OH} = 0.625 × V_{DD}(NAMODV$_{DD}$) V_{OL} = 0.25 × V_{DD}(NAMODV$_{DD}$)
MMCLK output low level width	t_{LOW}	6.5	—	—	ns	
MMCLK output high level width	t_{HIGH}	6.5	—	—	ns	
MMCLK rise time	t_r	—	—	3	ns	
MMCLK fall time	t_f	—	—	3	ns	
MMCMD/ MMDAT output delay time	t_{DDAT}	−6.5	—	2.5	ns	
MMCMD/ MMDAT setup time	t_{SDAT}	4.0	—	—	ns	
MMCMD/ MMDAT hold time	t_{HDAT}	2.0	—	—	ns	

Table 54.5-8 Backward Compatible Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
MMCLK cycle time	t_{cyc}	40	—	—	ns	C_L = 30 pF 1.8-V operation: V_{OH} = 0.65 × V_{DD}(NAMODV$_{DD}$) V_{OL} = 0.35 × V_{DD}(NAMODV$_{DD}$) 3.3-V operation: V_{OH} = 0.625 × V_{DD}(NAMODV$_{DD}$) V_{OL} = 0.25 × V_{DD}(NAMODV$_{DD}$)
MMCLK output low level width	t_{LOW}	10	—	—	ns	
MMCLK output high level width	t_{HIGH}	10	—	—	ns	
MMCLK rise time	t_r	—	—	10	ns	
MMCLK fall time	t_f	—	—	10	ns	
MMCMD/ MMDAT output delay time	t_{DDAT}	−7.5	—	2.5	ns	
MMCMD/ MMDAT setup time	t_{SDAT}	4.0	—	—	ns	
MMCMD/ MMDAT hold time	t_{HDAT}	2.0	—	—	ns	

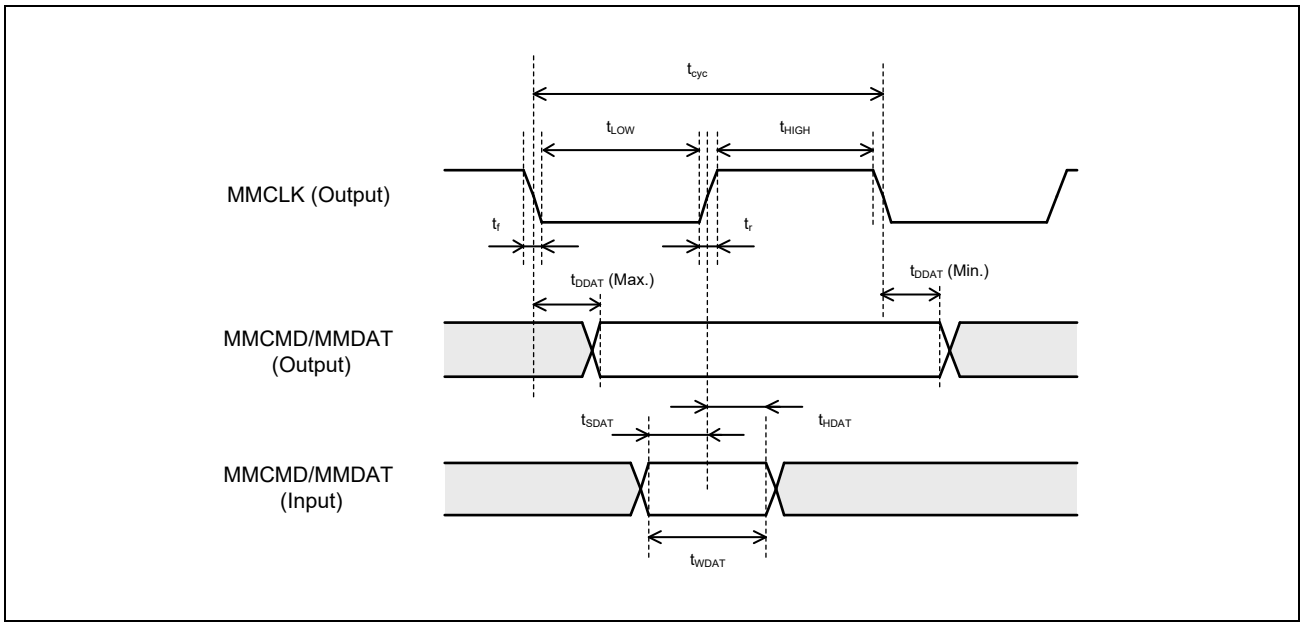


Figure 54.5-10 eMMC Timing

54.5.6 Image Sensor Timing Generator (STG)

54.5.6.1 Clock Synchronous Serial Interface

Table 54.5-9 Clock Synchronous Serial Data I/O Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
IMnSCLK cycle time	t_{cyc}	26.9	—	—	ns	
IMnSCLK output low level time	t_{LOW}	t_{cyc} × 0.45	—	t_{cyc} × 0.55	ns	
IMnSCLK output high level time	t_{HIGH}	t_{cyc} × 0.45	—	t_{cyc} × 0.55	ns	
IMnTXD output delay time	t_{DTXD}	−3	—	3	ns	C_L = 15 pF
IMnRXD setup time	t_{SRXD}	t_{cyc} − 12	—	—	ns	
IMnRXD hold time	t_{HRXD}	0	—	—	ns	

Note: n = 0, 1

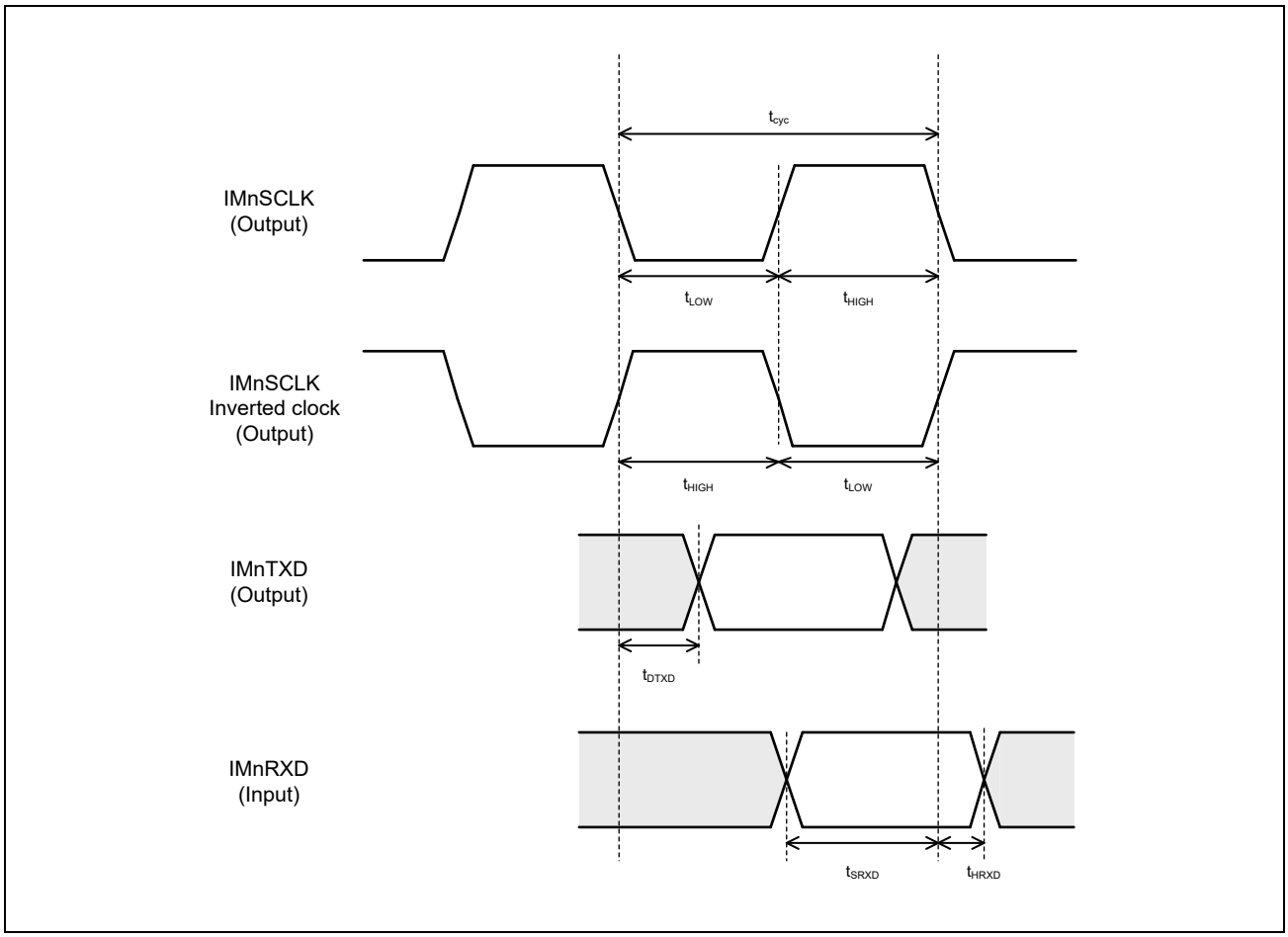


Figure 54.5-11 Clock Synchronous Serial Data I/O Timing

Table 54.5-10 Clock Synchronous HS/VS/SIG0 Signal Output Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
IMnSCLK cycle time	t_{cyc}	13.4	—	—	ns	
IMnSCLK output low level time	t_{LOW}	t_{cyc} × 0.45	—	t_{cyc} × 0.55	ns	
IMnSCLK output high level time	t_{HIGH}	t_{cyc} × 0.45	—	t_{cyc} × 0.55	ns	
IMnHS/IMnVS/IMnSIG0 output delay time	t_{DSIG}	−3	—	3	ns	C_L = 15 pF

Note: n = 0, 1

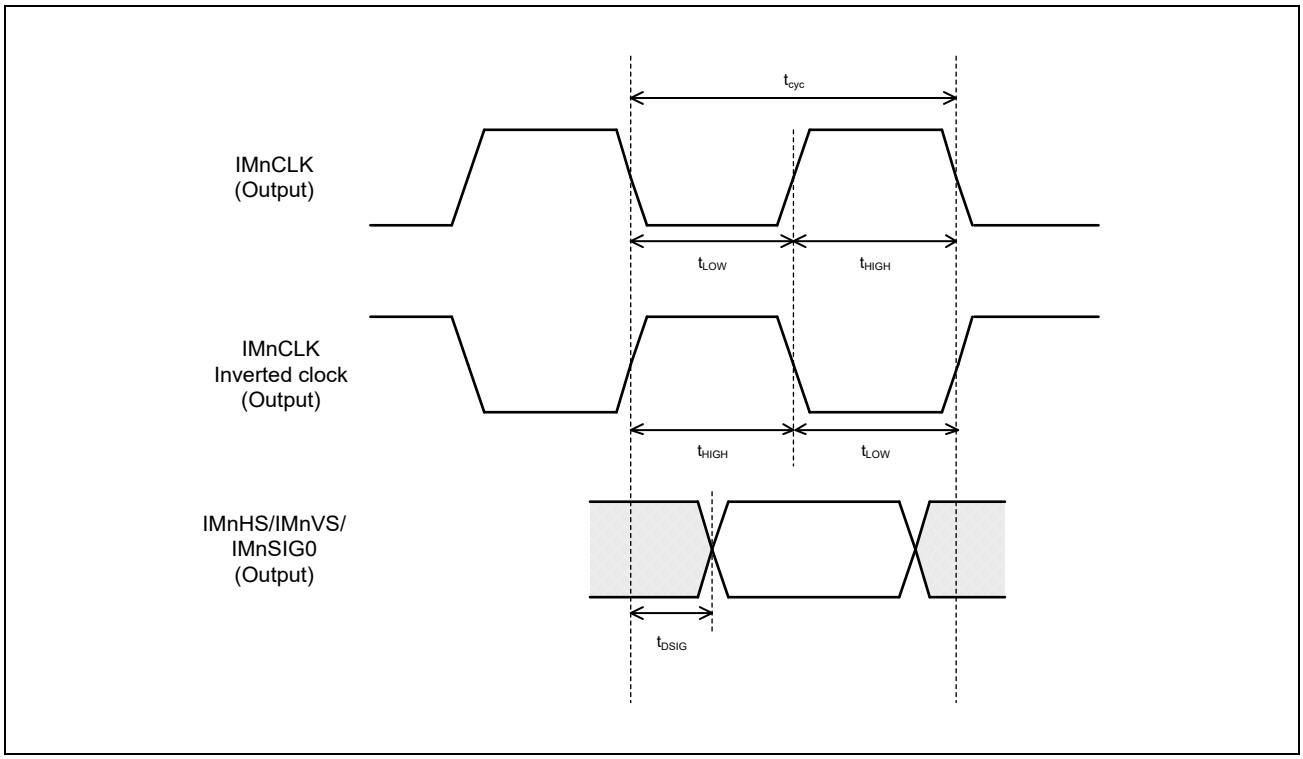


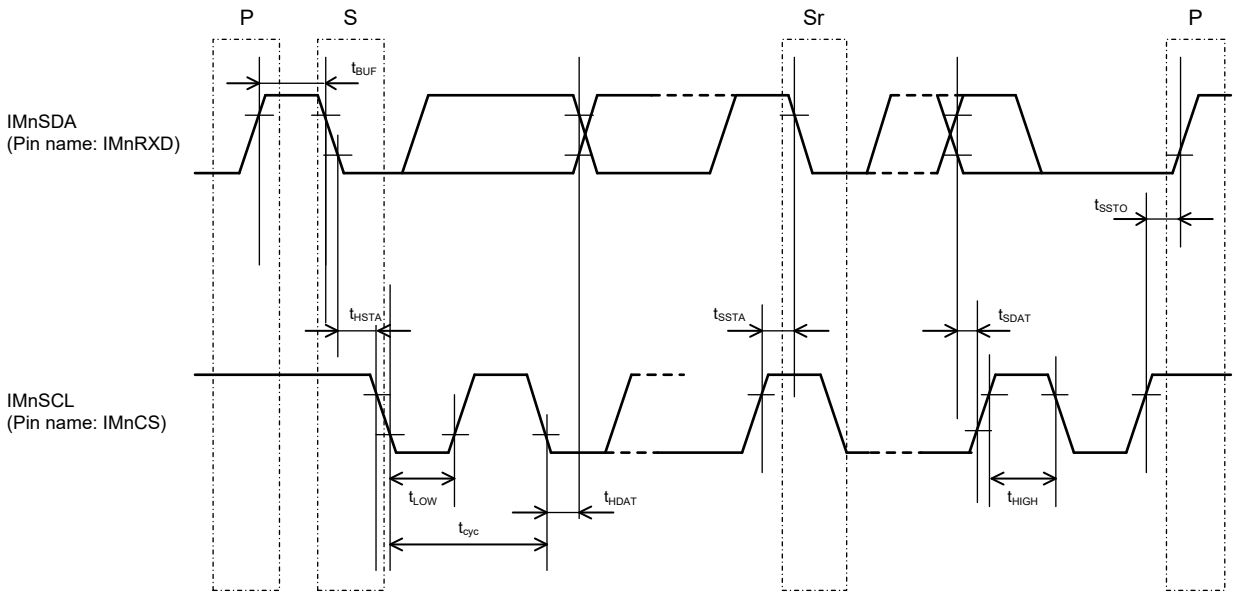
Figure 54.5-12 Clock Synchronous HS/VS/SIG0 Signal Output Timing

54.5.6.2 IIC Interface

Table 54.5-11 IIC Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
IMnSCL cycle time	t_{cyc}	2500	—	—	ns	
IMnSCL low level width	t_{LOW}	1300	—	—	ns	
IMnSCL high level width	t_{HIGH}	600	—	—	ns	
Bus free time (time from start to stop condition)	t_{BUF}	1300	—	—	ns	
Start condition hold time	t_{HSTA}	600	—	—	ns	
Restart condition setup time	t_{SSTA}	600	—	—	ns	
Stop condition setup time	t_{SSTO}	600	—	—	ns	
IMnSDA setup time	t_{SDAT}	100	—	—	ns	
IMnSDA hold time	t_{HDAT}	0	—	900	ns	

Note: n = 0, 1



Note: S: START condition
P: STOP condition
Sr: Repeated START condition

Figure 54.5-13 IIC Timing

54.5.7 Motor Controller (MTR)

Table 54.5-12 Clock Synchronous Serial Data I/O Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
MTSCLKn cycle time	t_{cyc}	41.6	—	—	ns	
MTSCLKn output low level time	t_{LOW}	t_{cyc} × 0.45	—	t_{cyc} × 0.55	ns	
MTSCLKn output high level time	t_{HIGH}	t_{cyc} × 0.45	—	t_{cyc} × 0.55	ns	
MTTXDn output delay time	t_{DTXD}	−5	—	5	ns	C_L = 15 pF
MTRXDn setup time	t_{SRXD}	t_{cyc} − 25	—	—	ns	
MTRXDn hold time	t_{HRXD}	0	—	—	ns	

Note: n = 0, 1

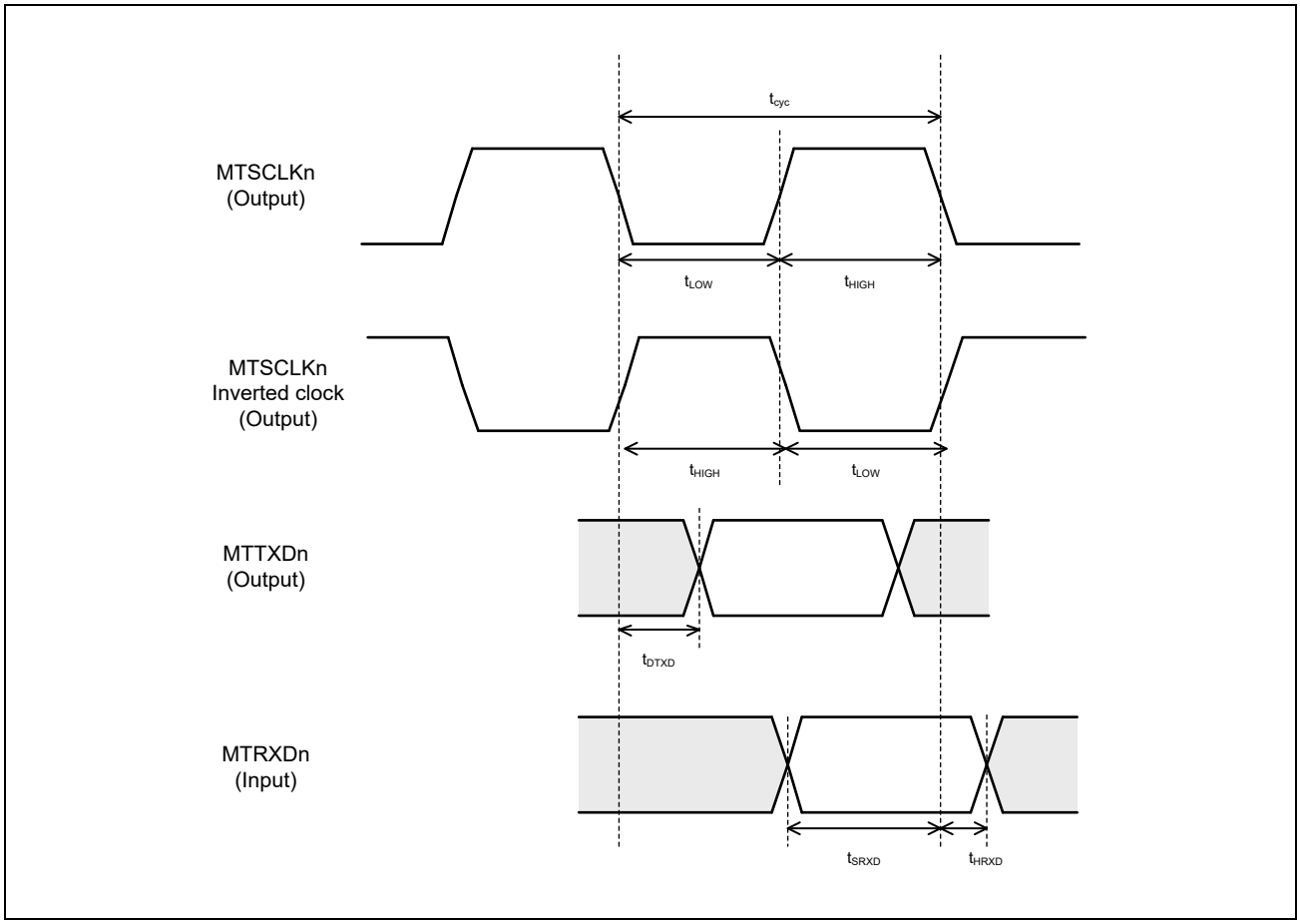


Figure 54.5-14 Clock Synchronous Serial Data I/O Timing

54.5.8 Environment Sensor Interface (ESI)

Table 54.5-13 Clock Synchronous Serial Data I/O Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
SDTSCLK cycle time	t_{cyc}	41.6	—	—	ns	
SDTSCLK output low level time	t_{LOW}	t_{cyc} × 0.45	—	t_{cyc} × 0.55	ns	
SDTSCLK output high level time	t_{HIGH}	t_{cyc} × 0.45	—	t_{cyc} × 0.55	ns	
SDTTXD output delay time	t_{DTXD}	−5	—	5	ns	C_L = 15 pF
SDTRXD setup time	t_{SRXD}	t_{cyc} − 25	—	—	ns	
SDTRXD hold time	t_{HRXD}	0	—	—	ns	

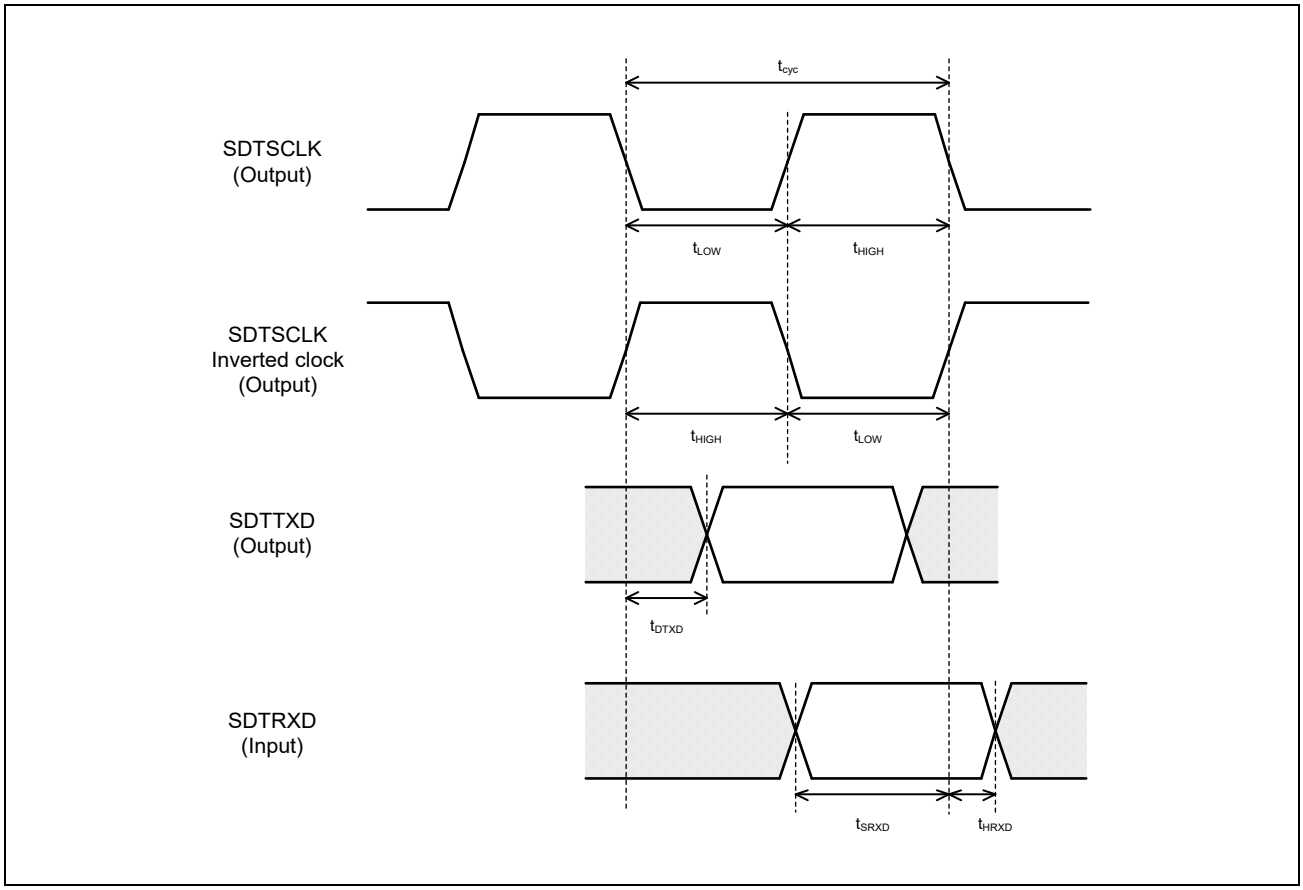


Figure 54.5-15 Clock Synchronous Serial Data I/O Timing

54.5.9 Audio Interface (AUI)

Table 54.5-14 Audio Interface Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
AUBICK cycle time	t_{cyc}	325.5	—	—	ns	
AUBICK low level time	t_{LOW}	t_{cyc} × 0.45	—	t_{cyc} × 0.55	ns	
AUBICK high level time	t_{HIGH}	t_{cyc} × 0.45	—	t_{cyc} × 0.55	ns	
AUDO output delay time	t_{DAU}	41.6	—	79.5	ns	C_L = 15 pF
AUDI/AULRCK setup time	t_{SAU}	26.9	—	—	ns	
AUDI/AULRCK hold time	t_{HAU}	26.9	—	—	ns	

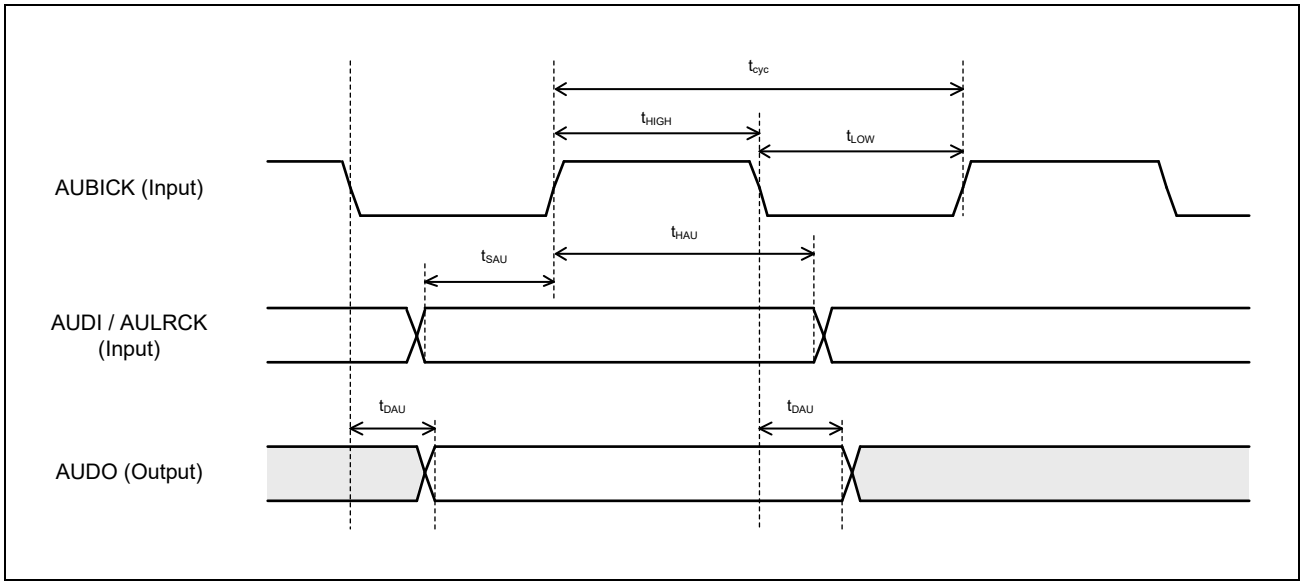


Figure 54.5-16 Audio Interface Timing

54.5.10 Debugger Interface

54.5.10.1 JTAG

Table 54.5-15 JTAG Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
DETCK cycle time	t_{cyc}	20	—	—	ns	
DETDI/ DETMS setup time	t_{STDI}	5	—	—	ns	
DETDI/ DETMS hold time	t_{HTDI}	5	—	—	ns	
DETDO output delay time	t_{DTDO}	2	—	8	ns	

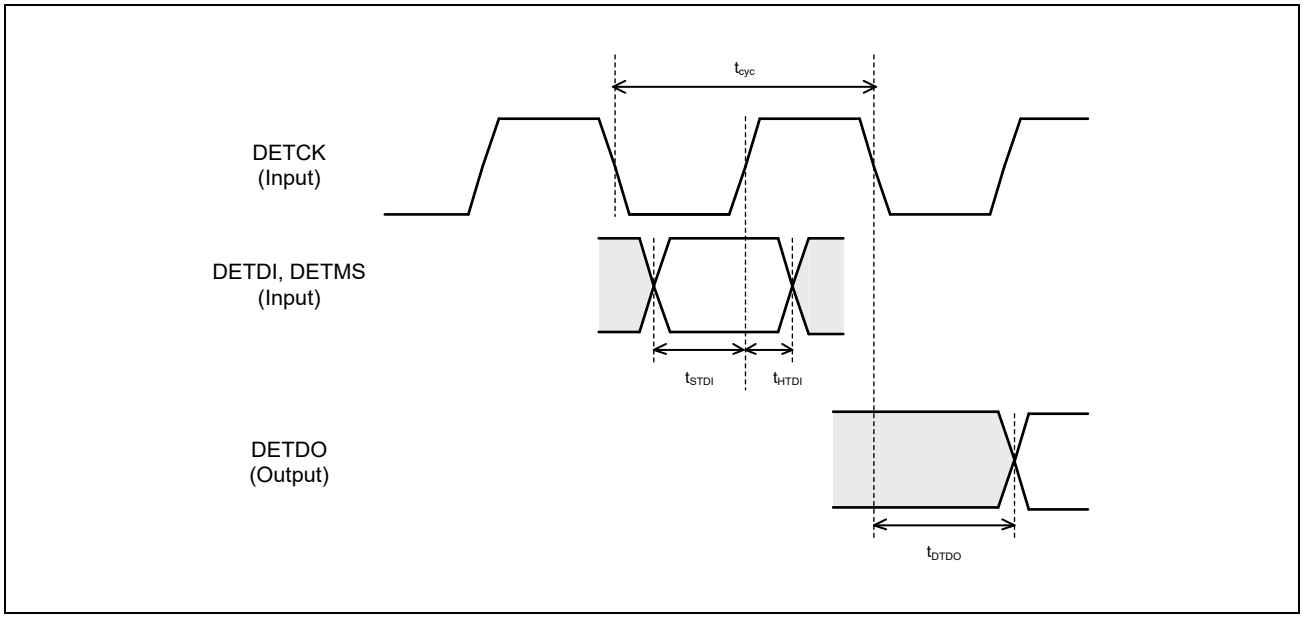


Figure 54.5-17 JTAG Timing

54.5.10.2 SWD (Serial Wire Debugging)

Table 54.5-16 SWD Interface Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
DETCK cycle time	t_{cyc}	20	—	—	ns	
DETMS setup time	t_{STMS}	5	—	—	ns	
DETMS hold time	t_{HTMS}	5	—	—	ns	
DETMS output delay time	t_{DTMS}	2	—	8	ns	

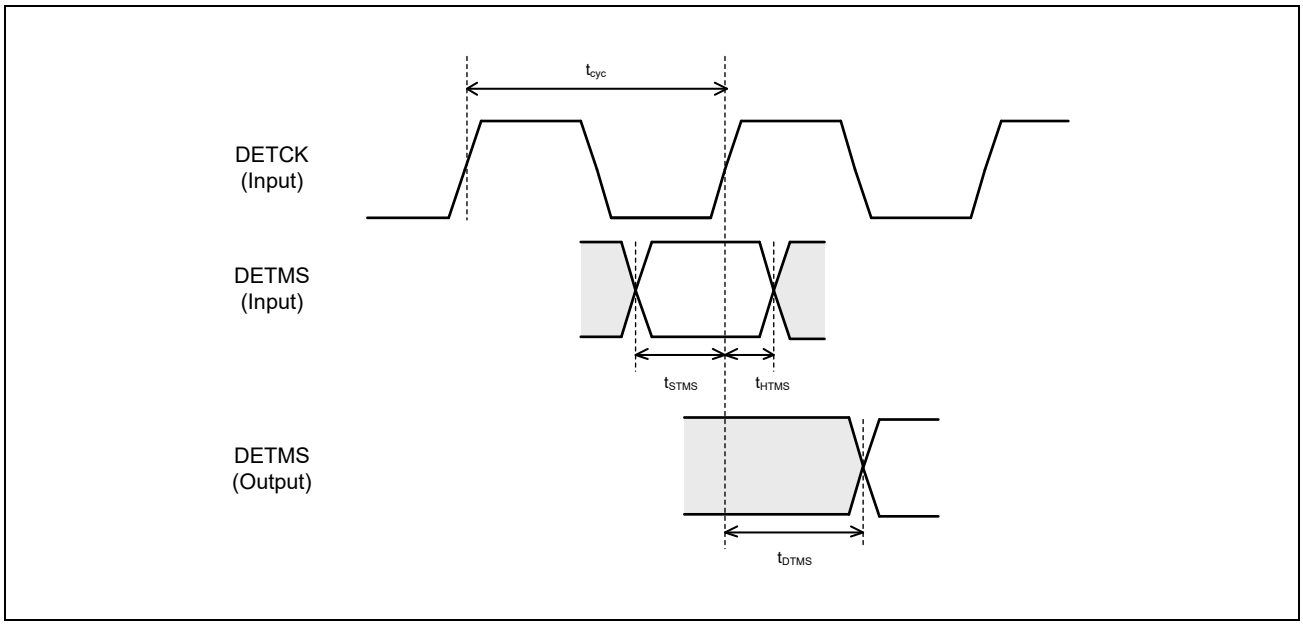


Figure 54.5-18 SWD Interface Timing

54.5.11 TRACE Interface (TRACE)

Table 54.5-17 TRACE Interface Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Note
TRCLK cycle time	t_{cyc}	20	—	—	ns	
TRCLK output low level width	t_{LOW}	9	—	—	ns	
TRCLK output high level width	t_{HIGH}	9	—	—	ns	
TRCTL/TRDAT output delay time (TRCLK rising edge)	t_{DRDAT}	2	—	7	ns	
TRCTL/TRDAT output delay time (TRCLK falling edge)	t_{DFDAT}	2	—	7	ns	

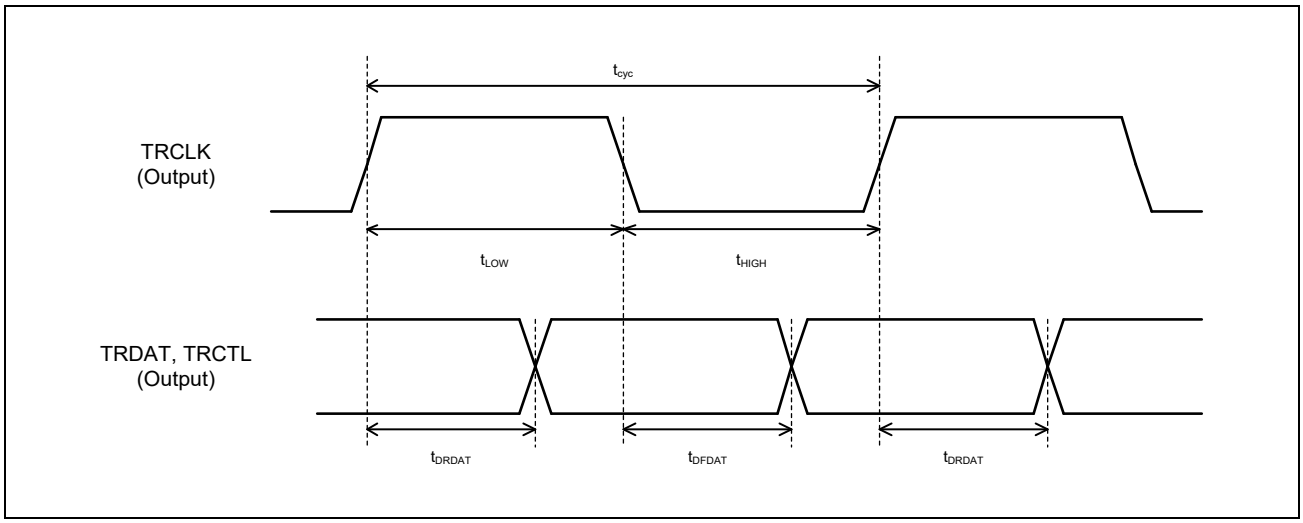


Figure 54.5-19 TRACE Interface Timing

54.6 Various Analog Characteristics

54.6.1 MIPI CSI-2 PHY Characteristics

The MIPI CSI-2 Rx D-PHY of this LSI is equivalent to the MIPI CSI-2 Ver.1.2/D-PHY Ver.1.2. For details, refer to the MIPI specification.

54.6.2 MIPI DSI Tx D-PHY Characteristics

The MIPI DSI Tx D-PHY of this LSI is compliant with the MIPI DSI Ver.1.3.1/ D-PHY Ver.1.1.

54.6.3 HDMI Tx PHY Characteristics

The HDMI Tx PHY of this LSI is compliant with the following HDMI 1.4a standard:

Version 1.4a of *the High-Definition Multimedia Interface Specification*, released on March 4, 2010

54.6.4 LPDDR4 PHY Characteristics

The LPDDR4 PHY of this LSI is compliant with the JEDEC 209-4A standard.

54.6.5 USB PHY Characteristics

The USB PHY of this LSI is compliant with the following USB 3.1 GEN1 standard:

Universal Serial Bus 3.1 Specification

54.6.6 PCI Express PHY Characteristics

The PCI Express PHY of this LSI is compliant with the following PCIe standard:

Revision 4.0 of *the PCI Express® Base Specification* for Gen1/Gen 2

54.6.7 ADC Characteristics

Table 54.6-1 DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Resolution	—	—	12	—	Bit	
Differential non-linearity	DNL	—	±1.0	±3.0	LSB	FAIN = 100 kHz, Ramp wave
Integral non-linearity	INL	—	±2.0	±6.0	LSB	
Top offset voltage	EOT	—	±10	±20	LSB	
Bottom offset voltage	EOB	—	±10	±20	LSB	

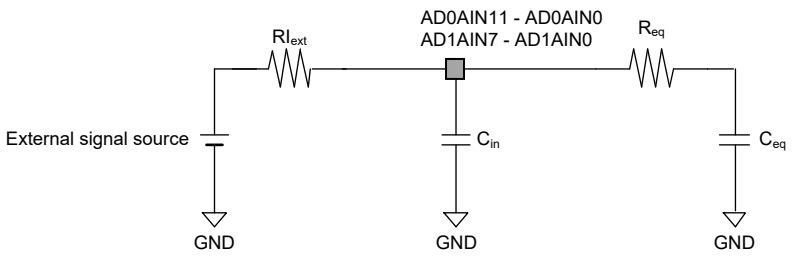
Table 54.6-2 AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Main clock duty ratio	—	45	50	55	%	
Analog input frequency (AD0AIN11-AD0AIN0, AD1AIN7-AD1AIN0)	FAIN	DC	—	100k	Hz	

Table 54.6-3 Recommended External Input Resistance

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
External Input Resistance*1 (AD0AIN11-AD0AIN0, AD1AIN7-AD1AIN0)	RI_{ext}	—	—	2	kΩ	FCLK = 10 MHz

Note 1. Output resistance of signal generator + Series parasitic resistance between signal source and ADC input



Note: Analog input equivalent resistance (R_{eq}): 2 kΩ
Analog input equivalent capacitance (C_{eq}): 5 pF
Analog input pin capacitance (C_{in}): 2 pF

Figure 54.6-1 ADC Input Equivalent Circuit

54.6.8 Temperature Sensor Characteristics

Table 54.6-4 Temperature Sensor Characteristics

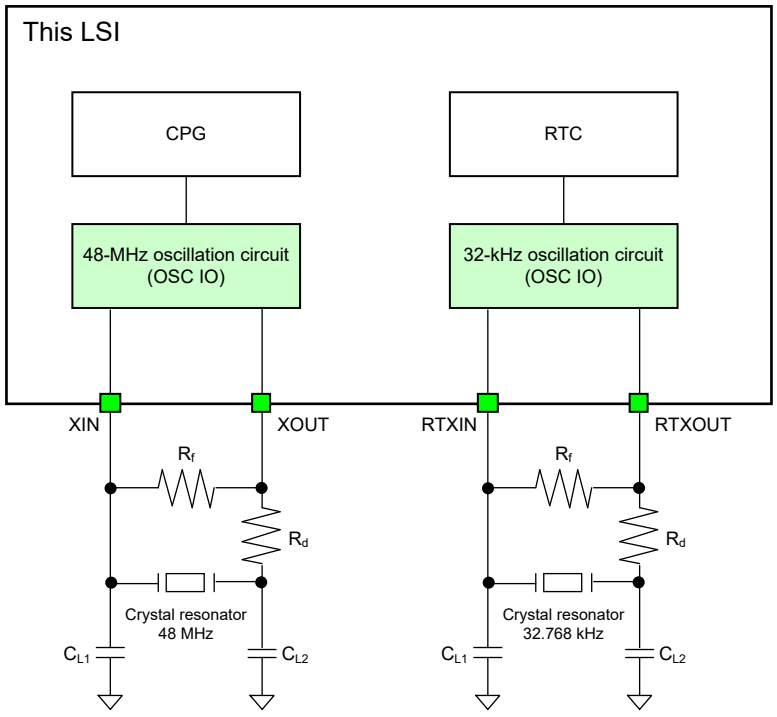
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Accuracy from 70°C to 125°C	Acc70_125	—	±2.0	±3.0	°C	
Accuracy from −40°C to 70°C	Accm40_70	—	±3.0	±5.0	°C	

54.7 Oscillation Circuits for Connecting Crystal Resonators (OSC)

This LSI chip includes two oscillation circuits (OSC) for connection to crystal resonators, specifically a 48-MHz crystal resonator for the system clock and a 32.768-kHz crystal resonator for the real-time clock. **Table 54.7-1** lists the pins for connecting the crystal resonators and the clock frequencies. **Figure 54.7-1** shows an example of the connections with crystal resonators.

Table 54.7-1 Pins for Connecting Crystal Resonators and Clock Frequency

External Pin Name	I/O	Clock Frequency
For the system clock		
XIN	Input	48 MHz (frequency deviation: ±50 ppm, frequency temperature characteristic: ±30 ppm)
XOUT	Output	48 MHz
For the real-time clock		
RTXIN	Input	32.768 kHz (frequency deviation: ±20 ppm)
RTXOUT	Output	32.768 kHz



Note: R_f: Feedback resistor
R_d: Dumping resistor
C_{load} (load capacitance of the crystal): See below for the formula.

$$C_{load} = \{C_{L1} \times C_{L2} / (C_{L1} + C_{L2})\} + \text{PCB's floating capacitance}$$

Figure 54.7-1 Example of Connections with Crystal Resonators

Place the crystal resonators and the capacitors C_{L1} and C_{L2} as close as possible to the pins to connect crystal resonators. To avoid interference and to ensure correct oscillation, the grounding points of the capacitors appended to the crystal resonators should be shared, and no wiring patterns should be placed near these components.

The characteristics of the crystal resonators are closely related to the design of the user board. Therefore, the user should sufficiently evaluate them with reference to the example of connection of crystal resonators in **Figure 54.7-1**.

The circuit rating of a crystal resonator depends on the crystal resonator and the stray capacitance of the mounting circuit. Therefore, contact the manufacturer of the crystal resonator before deciding upon the circuit rating. The user should thoroughly evaluate and then set the parameters (resistor and capacitor values).

Table 54.7-2 is a list of recommended values for the crystal resonators.

Table 54.7-2 Recommended Model Values for the Crystal Resonators

	Model Values for the Crystal Resonators			
Clock Frequency	Max. ESR*1	Max. C_L*2	Max. C_0*3	Max. Drive Level
32.768 kHz	70 kΩ	12.5 pF	1.4 pF	1 µW
48 MHz	50 Ω	10 pF	7 pF	100 µW

Note 1. ESR means the equivalent series resistor of the crystal resonator.

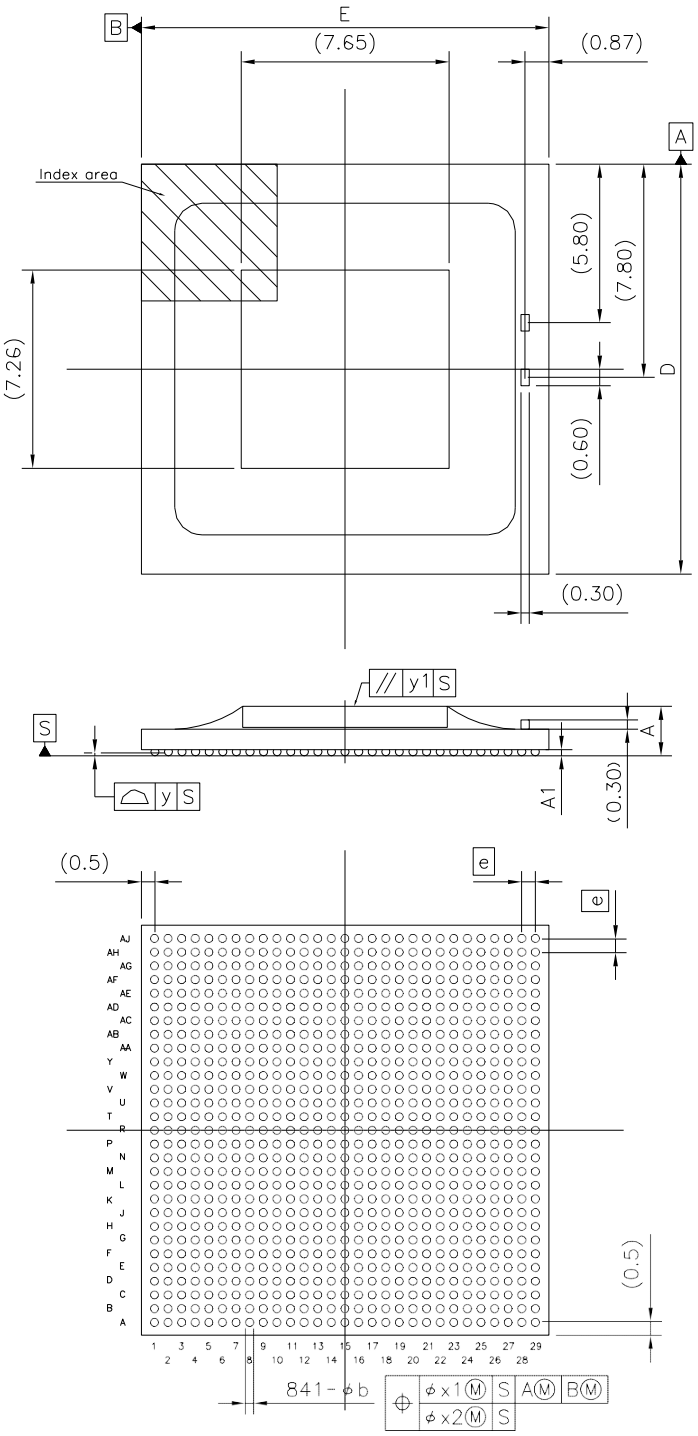
Note 2. C_L is the load capacitance of the crystal resonator.

Note 3. C_0 is the parallel capacitance of the crystal resonator.

Appendix A Package Dimensions

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA841-15x15-0.50	PRBG0841KA-A	–	0.71

Unit:mm



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	14.85	15.00	15.15
E	14.85	15.00	15.15
e	–	0.50	–
A	(1.70)	(1.90)	2.10
A1	0.15	(0.25)	–
b	0.25	0.30	0.35
x1	–	–	0.20
x2	–	–	0.05
y	–	–	0.12
y1	–	–	0.20

Appendix A.1 Package Dimensions

REVISION HISTORY	RZ/V2M User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.00	Jun 30, 2021	—	First edition issued
1.10	Sep 17, 2021	Section 1 Overview	
		44	Table 1.3-1 Overview of Functions (2/4) Video & graphics: JPEC codec → JPEG codec
		Section 2 Pin	
		74	Table 2.2-1 List of External Pins: Note 4 added, Note 4 → Note 5
		91	Table 2.3-1 List of Pin Functions: Note 2 added, Note 2 → Note 3, Note 3 → Note 4
		Section 3 Clock	
		All	LSI chip → LSI
		106	Table 3.1-4 List of Unit Clocks Note 2: CGC → Clock Gating cells
		108	3.4.3 Clock Gating Cells: CG → Clock Gating
		Section 4 Reset	
		All	LSI chip → LSI
		110	4.2.1 Configuration of Hardware Resets (External Pin Resets): eternal → external
		Section 6 Address Map	
		All	LSI chip → LSI
		Section 8 Power Supply	
		All	LSI chip → LSI
		Section 9 System Function	
		159	Table 9.1-1 Selection of Operation Mode MD6 = 1, MD5 = x (Forced write mode): The description of Operation in Outline, modified
		163	9.1.2.3 (2) Forced Write Mode: The description on the data specifications obtained with an SD card in the load sequence, added
		Section 10 CPU	
		173	Table 10.1-2 Cortex-A53 Configuration Core 0 reset vector position, Core 1 reset vector position: 0_8000_0000h → 00_8000_0000h
		Section 11 System Counter (SYC)	
		179	11.2 Block Diagram: The section title, changed. The description, modified.
		179	Figure 11.2-1 Block Diagram: The figure title, changed
		Section 16 Compare-Match Timer (TIM)	
		All	Binary notation "b" added: 0 → 0b, 1 → 1b
		Section 17 Pulse-Width Modulation Timer (PWM)	
		248	Figure 17.2-2 Interrupt Output Timing, modified
		258, 259	17.4.1 PWM Signal Output The description, modified: 00_0000h → 0000_0000h, 0 → 0b
		259	Figure 17.4-2 PWM Output Timing Details, modified
		260	17.4.2 Changing the Duty Cycle The description, modified: 00_0000H → 0000_0000h
		Section 19 DMA Controller (DMAC)	
		298	Table 19.5-11 DMAA_DMACn_CHSTAT_m Register Contents (4/4) The description on Bit Position 1 (RQST), modified: 0 → 0b
		316	Figure 19.6-1 Overview of Register Normal Mode, modified

Rev.	Date	Description	
		Page	Summary
1.10	Sep 17, 2021	Section 28 H.265/H.264 Multi Codec (VCD)	
		389	Figure 28.2-1 Configuration Diagram of VCD Connection, modified
		Section 31 LPDDR4 Interface (LPDDR4)	
		393	31.1 Overview 12- and 16-Gb → 12-Gb and 16-Gb
		Section 35 USB3.1 Gen1 Interface (USB)	
		402	Table 35.1-1 Functions in Outline The description on the USB3PERI function, modified: 1.5 MHz → 1.5 Mbps
		Section 36 PCI Express 2.0 Interface (PCIe)	
		All	Binary notation “b” added: 0 → 0b, 1 → 1b
		804	36.3 Block Diagram The section title, changed. The description, modified.: the unit → PCI
		804	Figure 36.3-1 Block Diagram: The figure title, changed
		968	Table 36.5-2 PCI Express Configuration Registers (Type0) (2/5) The abbreviation of the Base Address Register Mask00 (Upper) (Function #0), modified: PCI_EP_DEVCS2_F0 → PCI_EP_BARMSK00U_F0
		970	Table 36.5-2 PCI Express Configuration Registers (Type0) (4/5) The abbreviation of the Base Address Register Mask00 (Upper) (Function #1), modified: PCI_EP_DEVCS2_F1 → PCI_EP_BARMSK00U_F1
		1184	36.8.3.1 BAR Specification (Two-Function Configuration) CAUTION, modified: 4-gigabyte → 4-Gbyte
		1200	36.8.5 PCIe Initialization Procedure, added
		Section 38 IIC Bus Interface (IIC)	
		All	Binary notation “b” added: 0 → 0b, 1 → 1b
		Section 39 Clocked Serial Interface (CSI)	
		1347	39.3.2.1 CSI Mode Control Register (CSIm_CSI_MODE) The description, modified: 0 → 0b
		Section 40 Universal Asynchronous Receiver/Transmitter (UART)	
		1439	40.1.2 Connection Configuration: The section title, changed. The description, modified.
		1439	Figure 40.1-1 Connection Configuration: The figure title, changed
		1444	40.3.2.1 Receiver Buffer Register (when reading received data) (URTm_RBR) / Transmitter Holding Register (when writing transmission data) (URTm_THR): 1 → 1b
		Section 50 External Power Sequence Controller (PWC)	
		2026	Figure 50.5-2 Timing of the Outputs from the PWENn (n: 0 to 5) and PWSYSRSTN Pins: Note added
		Section 53 Debugger (CST)	
		2132	53.2 Block Diagram: The section title, changed. The description, modified.
		2132	Figure 53.2-1 Block Diagram: The figure title, changed
		2133	Figure 53.3-1 Connection Configuration, modified
1.20	Dec 24, 2021	Section 1 Overview	
		44	Table 1.3-1 Overview of Functions (2/4) Video & graphics: 265/H.264 multi codec: The functional description in “Support encoding/decoding standard”, modified
		Section 5 Interrupt	
		122	Table 5.4-1 Interrupt list of GIC (GIC-400 for CA53) (1/10) ID32 (IRQS[0]), ID33 (IRQS[1]), ID38 (IRQS[6]) to 41 (IRQS[7]): Modified to Reserved in “Output Pin Name”
		131	Table 5.4-1 Interrupt list of GIC (GIC-400 for CA53): Note 2, added; Note 2 → Note 3

Rev.	Date	Description	
		Page	Summary
1.20	Dec 24, 2021	Section 8 Power Supply	
		152	Figure 8.2-1 Power Domain Diagram: The layout of the CIF, GRP, STG functional blocks, modified
		Section 9 System Function	
		169, 170	9.1.2.6 Supplementary Notes on Specifications, added
		171	9.1.3 CA53 Core1 Startup Setting, added
		Section 10 CPU	
		177	Table 10.2-1 List of Registers Cortex-A53 pin control register, added “Offset Address” of Reserved: 418h to FFFh → 418h to FFCh
		178	10.2.2.1 CA53 Core1 Reset Vector Address Configuration Register L (CA53_RVA1CRL), added
		179	10.2.2.2 CA53 Core1 Reset Vector Address Configuration Register H (CA53_RVA1CRH), added
		180	10.2.2.3 CA53 Processor Power Status Configuration Register (CA53_PSCR), added
		Section 21 CMOS Image Sensor Interface (CIF)	
		385	Table 21.1-1 Function Overview: Note 1, added; Note 1 → Note 2
		Section 28 H.265/H.264 Multi Codec (VCD)	
		394	28.1 Functional Overview: H.264/AVC baseline/main/high profile supported → H.264/AVC constrained baseline/main/high profile supported H.264/AVC constrained baseline/main/high profile supported: The description, modified
		Section 35 USB3.1 Gen1 Interface (USB)	
		539	Table 35.5-57 USB_HOST_ERSTBAH Register Contents 31 to 0 in “Bit Position”: Modified in “Bit Name” and “Description”
		Section 38 IIC Bus Interface (IIC)	
		1216	Table 38.4-1 List of Registers Offset Address: The layout order of the 20h, 24h, and 28h, modified
		1237	38.5.10.1 Setting the Transfer Clock by the IICB0WL and IIVB0WH Registers, added
		Section 48 Clock Pulse Generator (CPG)	
		1959	48.5.2.68 Reset Control Register 6 (CPG_RST6): “*” is deleted from Bit 29 (UNIT13_RSTWEN)
		1959	Table 48.5-64 CPG_RST6 Register Contents (1/3): “*” is deleted from Bit Position 29
		1964	48.5.2.70 Reset Control Register 8 (CPG_RST8): The description of a caution when using the ISP support package, deleted
		Section 51 Internal Power Domain Controller (PMC)	
		2036	Table 51.1-1 List of Functions Function (Major Category): CPU standby control, added
		2038	Table 51.2-1 List of Registers CPU Standby Monitor Register (040h), CA53 SRAM SDM Configuration Register (090h), CA53 SRAM RS Control Register (094h), CA53 SRAM RS Status Register (098h), added
		2051	51.2.2.12 CPU Standby Monitor Register (PMC_CPU_MON), added
		2052	51.2.2.13 Interrupt Status Register (PMC_INT_STS) L2_STBY (Bit 5), CPU1_STBY (Bit 4), CPU0_STBY (Bit3), added
		2053	51.2.2.14 Interrupt Clear Register (PMC_INT_CLR) L2_STBY (Bit 5), CPU1_STBY (Bit 4), CPU0_STBY (Bit3), added
		2054	51.2.2.15 Interrupt Mask Register (PMC_INT_MSK) L2_WEN (Bit 21), CPU1_WEN (Bit 20), CPU0_WEN (Bit 19), L2_STBY (Bit 5), CPU1_STBY (Bit 4), CPU0_STBY (Bit 3), added
		2056	51.2.2.16 CA53 SRAM SDM Configuration Register (PMC_CA53_SDM_CFG), added

Rev.	Date	Description	
		Page	Summary
1.20	Dec 24, 2021	2057	51.2.2.17 CA53 SRAM RS Control Register (PMC_CA53_RS_CTL), added
		2058	51.2.2.18 CA53 SRAM RS Status Register (PMC_CA53_RS_STS), added
		2066	51.3.5 CPU Standby Detection, added
		2067 to 2069	51.3.6 CPU Standby Control, added

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