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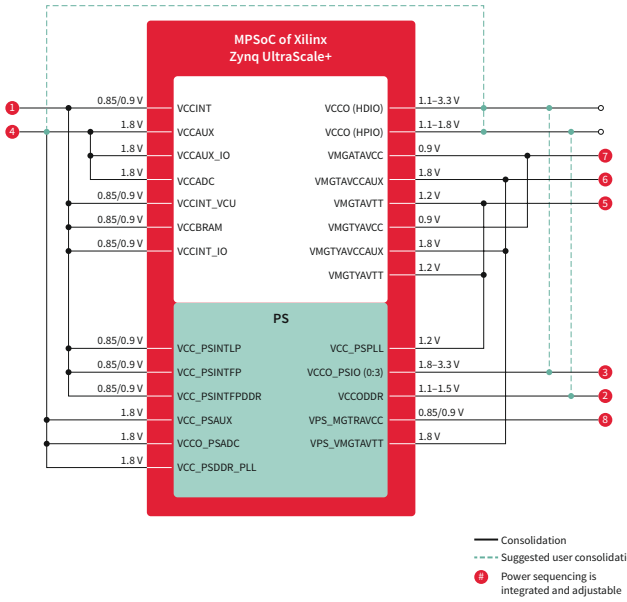
IRPS5401 PMIC ready to go designs for Zynq® UltraScale+™ MPSoC by Xilinx

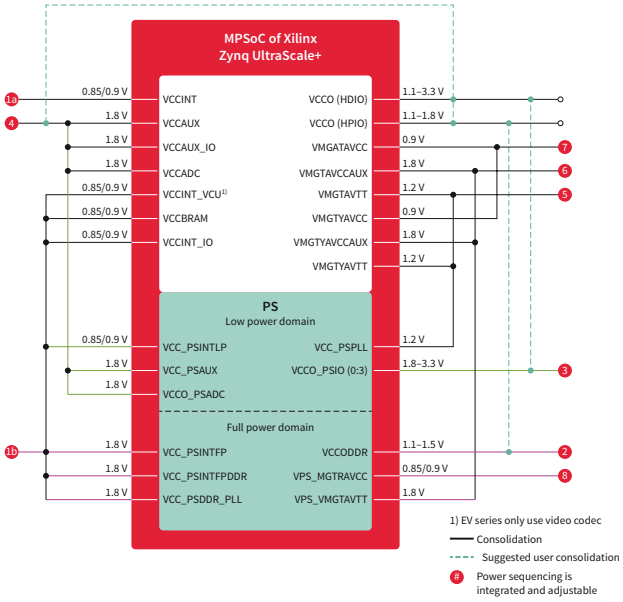
Configuration	Reference board provided by Avnet	Xilinx use case	Integrated sequencing	Schematics	Layout	BOM
1	UltraZED Zu03/Zu02	4[3]	Yes	Yes	Yes	Yes
2	UltraZED Zu03/Zu02	4[3]	Yes	Yes	Yes	Yes
3	UltraZED Zu03/Zu02	4[3]	Yes	Yes	Yes	Yes
4	Zu02/03/04/05 – CG/EG/EV	1	Yes	Yes	Yes	Yes
5	Zu06/07/09 – CG/EG/EV[2]	1	Yes	Yes	Yes	Yes
6	Zu02/03/04/05/06/07/09 – CG/EG/EV SERDES	SERDES power	Yes	Yes	Yes	Yes
7	Zu04EV/Zu05EV	2	Yes	Yes	Yes	Yes
8	Zu07EV	2	Yes	Yes	Yes	Yes
9	Zu04EV/Zu05EV/Zu07EV – No SERDES	2	Yes	Yes	Yes	Yes
10	Zu04EV/Zu05EV – SERDES	SERDES power	Yes	Yes	Yes	Yes
11	Zu04/05 – CG/EG	2	Yes	Yes	Yes	Yes
12	Zu06/07/09 – CG/EG[2]	2	Yes	Yes	Yes	Yes

1) Some Zynq US+ require 2 PMICs
2) Zu11/15/17/19 - EG with modification to channel A to work to 40 A+ from base Zu09 design, contact Infineon for design modification note
3) Power design example to separate the PS and PL power rails for low power and full power control modes

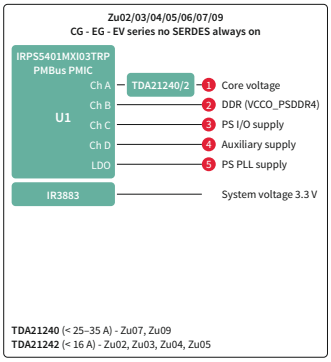
ZYNQ UltraScale+ always on rail consideration



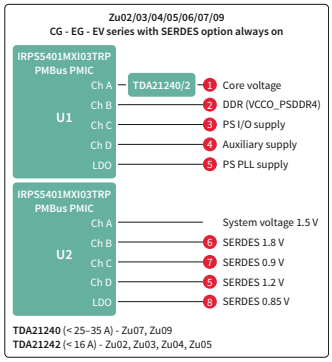
ZYNQ UltraScale+ always on – power efficiency separate core voltage at 0.72 V rail consideration



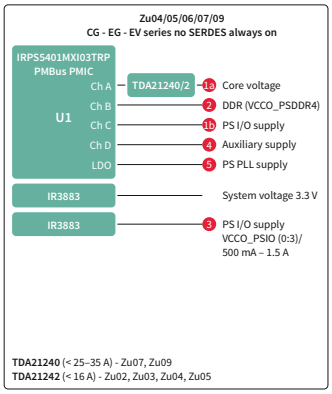
Zu02/03/04/05/06/07/09 CG - EG - EV series no SERDES always on



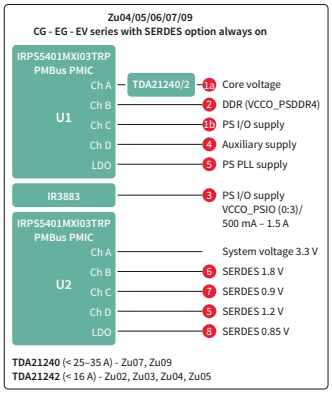
Zu02/03/04/05/06/07/09 CG - EG - EV series with SERDES option always on



Zu04/05/06/07/09 CG - EG - EV series no SERDES always on

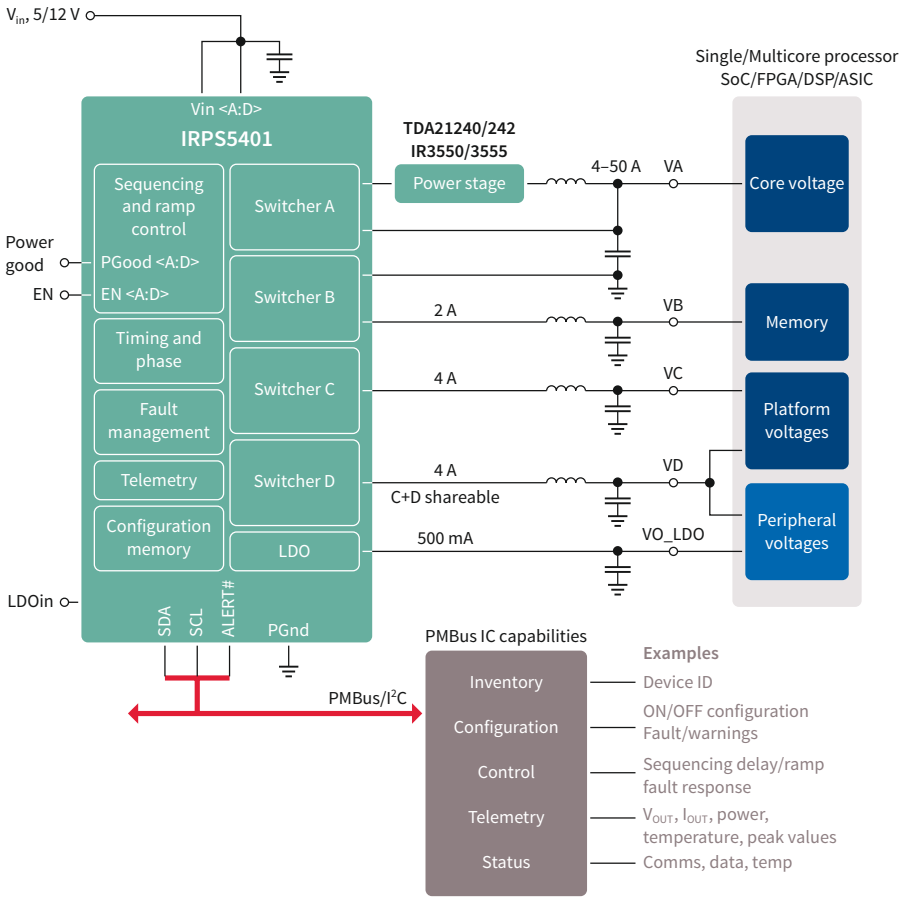


Zu04/05/06/07/09 CG - EG - EV series with SERDES option always on



Multi-output PMIC with integrated sequencer IRPS5401

The IRPS5401 is an integrated power management IC ideal for tight board space requirements; for example, FPGAs, system on chip ASICs and multi-core processors containing several voltages that require precision accuracy and voltage sequencing.



Key features

- Multi-output DC/DC with integrated FETs and sequencer
- 4 switchers and 1 LDO in one package
  - Output A: 2 A (without), 50 A (with powerstage)
  - Output B: 2 A
  - Outputs C, D: 4 A
  - Linear regulator: ±0.5 A
- Full PMBus: Margining, Fault Management, Telemetry

Key benefits

- Simplified BOM: Replace many regulators with one PMIC
- Design re-use: One design is scalable to cover wide range of FPGAs and ASICs
- Lower total solution cost: Eliminates external sequencer
- 35 percent board area reduction: High level integration and component reduction

Part number	Application	Status
IRPS5401MTRPBF	Blank, unprogrammed part for general use	Active & preferred
IRPS5401MXI03TRP	Pre-programmed for Xilinx Zynq UltraScale+ZU02 to ZU09	Coming soon

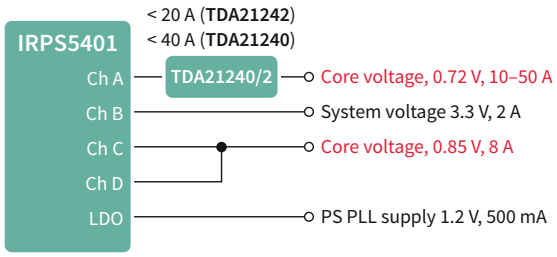
Industry reference designs

IRPS5401 is designed to support several industry ASICs, FPGAs and SOCs

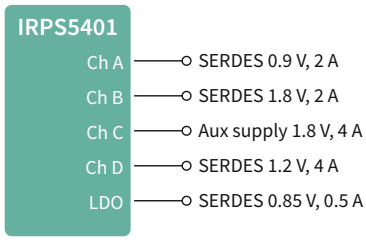
Scalable power options for power design flexibility

IRPS5401's flexibility easily addresses dierent types of ASICs and FPGAs. With the addition of an external power stage shown in example 1, it can easily address high current requirements.

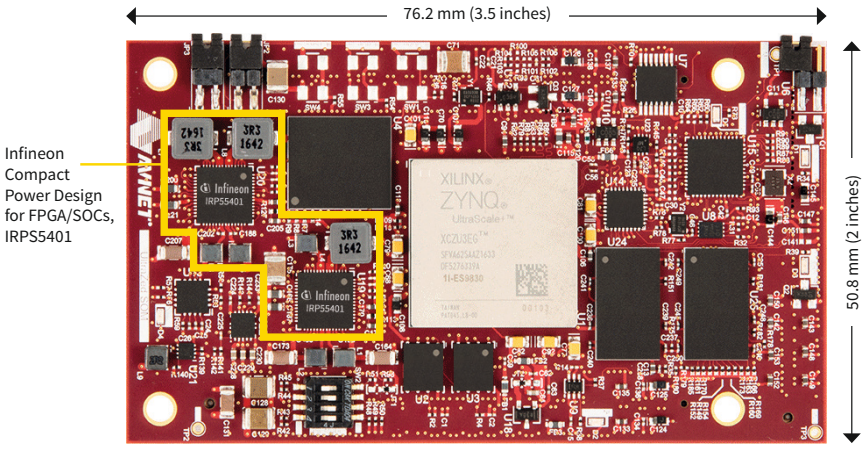
Example PMIC configuration 1



Example PMIC configuration 2

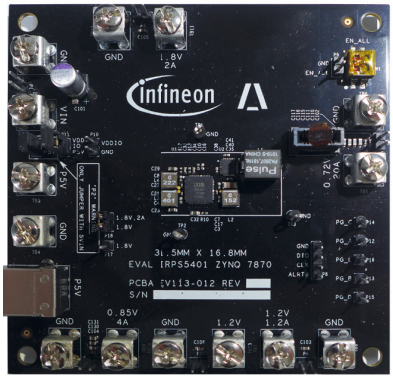


Avnet UltraZed, Zu02/Zu03 Zynq UltraScale+ reference design using IRPS5401 and Xilinx Zynq

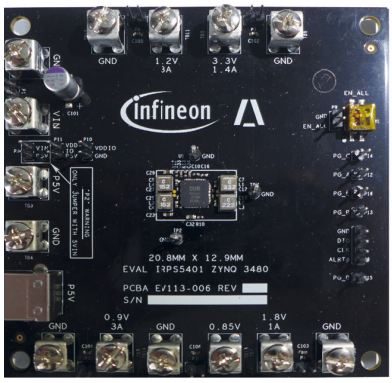


www.infineon.com/Power_Configurations_4_Zynq_ultrascale+

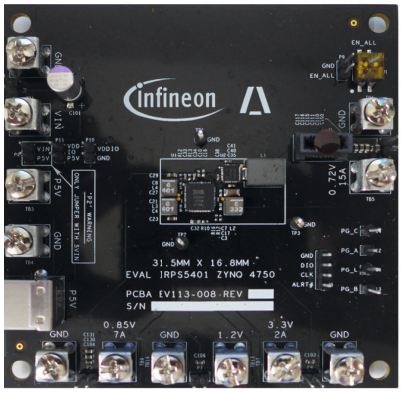
Power solution for Xilinx Zu09 EG/CG. Scalable to Zu11/Zu15/Zu17/Zu19



Compact SERDES power solution for Xilinx Zu02 to Zu09/Zu15



Power solution for Xilinx Zu07EV



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