How to Control Motor in Traveo II Family

About this document

Scope and purpose

AN220268 describes how to control a three-phase brushless DC (BLDC) motor with Hall IC by 120-degree commutation control technique using Cypress Traveo™ II family. The application note also shows examples of system configuration and peripheral settings.

Associated Part Family

Traveo II Family CYT2B5/B7 Series

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1 Introduction

Traveo II family can control a BLDC motor by 120-degree commutation technique using a Hall IC. This document shows an example of system configuration, peripheral setting, and motor control method. A BLDC motor consists of a rotor, which is a permanent magnet and three stators, which are coils. The three stators are defined as U- phase, V-phase, and W-phase, respectively.

Target products are Traveo II family CYT2B5000 Series and CYT2B7000 Series MCUs.

2 120-degree Commutation Control for Three Phase BLDC Motor

Figure 1 shows the block diagram with 120-degree commutation control and **Figure 2** shows the timing chart for clockwise (CW) rotation with 120-degree commutation control. Generally, in 120-degree commutation control using a Hall IC, a motor rotates by controlling the direction and strength of the current flowing in the motor based on the rotational position of the motor from the Hall IC.

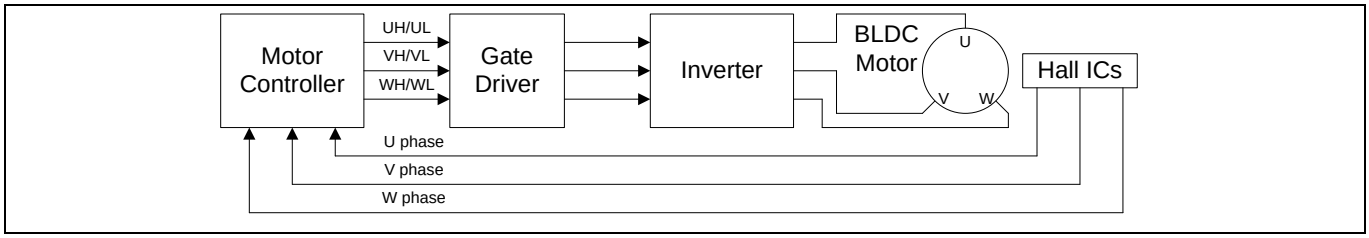

Figure 1 Block Diagram with 120-degree Commutation Control

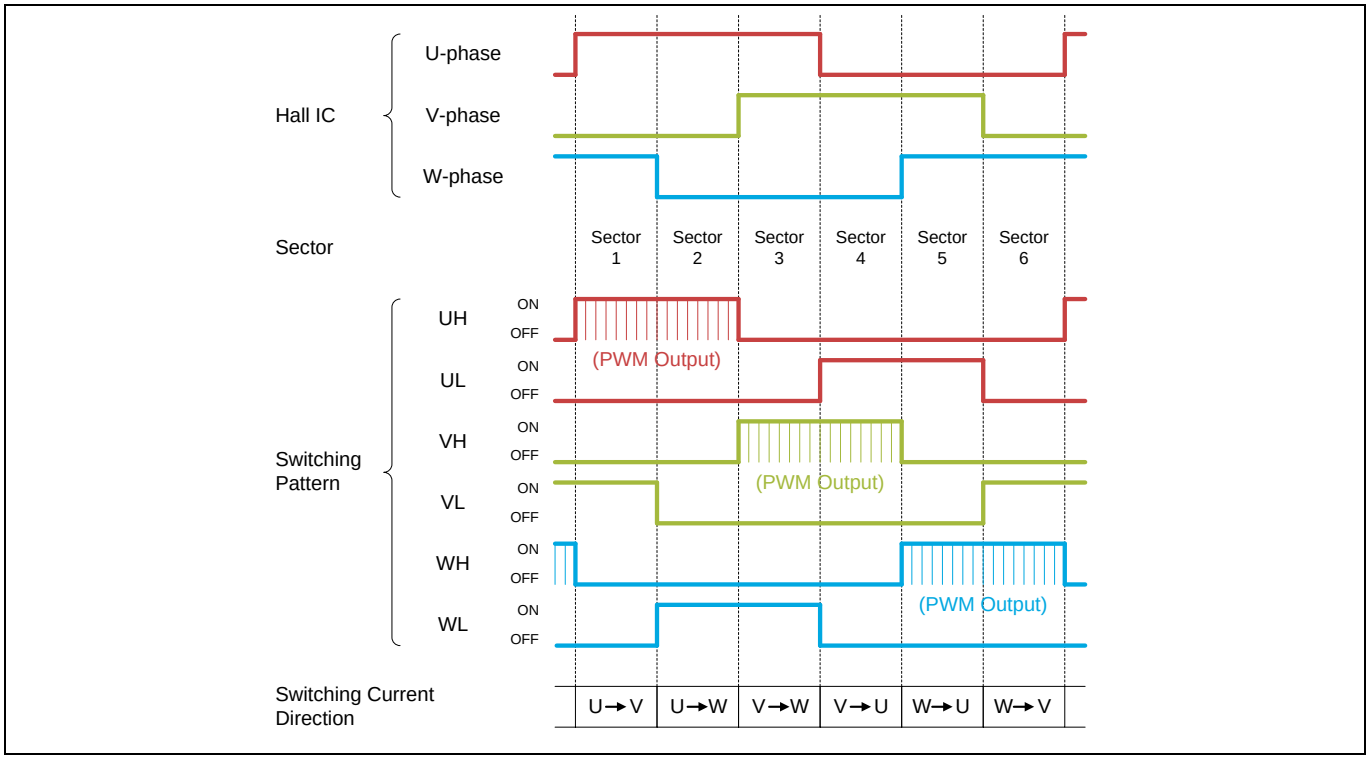

Figure 2 Timing Chart with 120-degree Commutation Control (for CW)

In **Figure 2**, the output of Hall IC shows the motor rotational position. Three Hall IC (U-phase, V-phase, and W-phase) are implemented on the motor at every 120-degree. Therefore, the six patterns that are output at every 60-degree depend on the rotation position. The sectors (1 to 6) are determined according to the output pattern from the Hall IC, and the direction of the current is determined according to the sector.

The switching pattern shows the control signal outputs from the Traveo II family to the motor. The control signal consists of six signals of UH/UL/VH/VL/WH/WL. The direction and strength of the current applied to the motor is controlled by combining these signals.

In general, these signals control the current to the motor via the inverter circuit. Current direction flows from Hi-side to Low-side. In sector 1 in **Figure 2**, UH and VL are ON. Therefore, the current flows from U-phase to V-phase (switching the current direction in **Figure 2** shows the current flow in each sector.)

120-degree Commutation Control for Three Phase BLDC Motor

The three high-side signals (UH/VH/WH) output a PWM signal, and control the strength of the current according to the duty of the PWM signal. The three low-side signals (UL/VL/WL) output a HIGH or LOW according to the current sector.

First, if the output from the Hall IC is [U-phase, V-phase, W-phase] = [1, 0, 1], that is, sector 1, the motor controller outputs [UH, UL, VH, VL, WH, WL] = [PWM, 0, 0, 1, 0, 0]. The current of the motor flows from U-phase to V-phase at this time; as a result, the motor rotates.

Next, the output of the Hall IC changes to [U - phase, V - phase, W - phase] = [1, 0, 0] (sector 2) by the rotation of this motor. When the motor controller detects this condition, it outputs [UH, UL, VH, VL, WH, WL] = [PWM, 0, 0, 0, 0, 1]. The current of the motor flows from U-phase to W-phase; the motor rotates. The motor rotates by sequentially executing this operation from sector 1 to sector 6.

Finally, when control of sector 6 is completed, the control repeats from section 1.

3 120-degree Commutation Control in Traveo II Family

3.1 Configuration

Figure 3 shows an example for configuring 120-degree commutation control using Hall ICs with Traveo II family. This application note explains the use case shown in **Figure 2**.

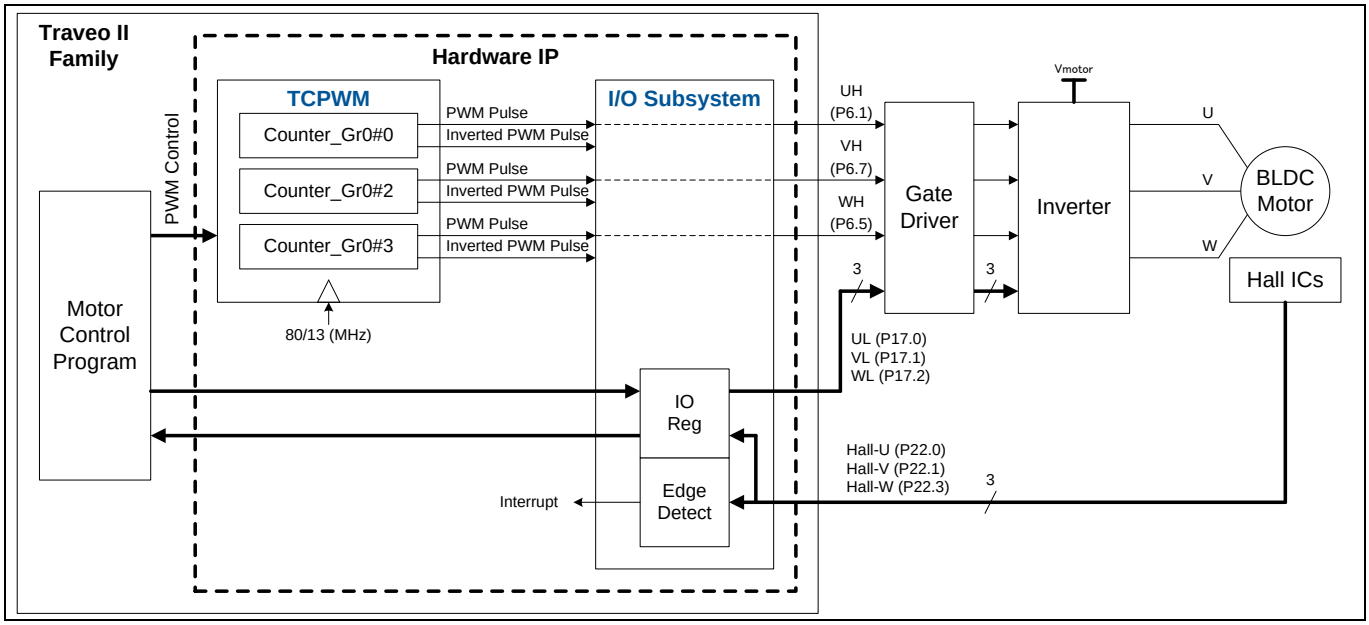

Figure 3 Example for Configuring 120-degree Commutation Control Using Hall ICs with Traveo II Family

The BLDC motor control system generally consists of the BLDC motor, an inverter, the gate driver, and the MCU. The control signal output from the MCU is connected to the gate driver; the gate driver drives the inverter to supply current to the motor. Hall IC outputs are directly connected to the MCU. The motor power supply (Vmotor) is connected to the inverter, and the MCU control signal is converted to the motor supply voltage.

The PWM output of the high-side signals (UH/VH/WH) is generated by three TCPWM channels. TCPWM has a PWM functionality and can output PWM pulses for each channel. Low-side signals (UL/VL/WL) use the I/O System. The interrupt function is used to detect signal change from Hall ICs. For details, refer to the TCPWM and I/O System sections in the **Architecture Technical Reference Manual (TRM)**.

120-degree Commutation Control in Traveo II Family

The following summarizes the peripheral functions to be used in this use case:

1. Use Traveo II family
   - CYT2B5/B7 series
2. TCPWM
   - Operation mode: PWM mode
   - Counter clock: 80/13 MHz
   - PWM period: 39 µs
   - Using TCPWM channel: TCPWM Group = 0, Channel 0 (for UH)
     Channel 3 (for VH)
     Channel 2 (for WH)
3. I/O System
   - High-side output pins: UH (P6.1), VH (P6.7) and WH (P6.5)
   - Low-side output pins: UL (P17.0), VL (P17.1) and WL (P17.2)
   - Hall ICs input pins: Hall-U (P22.0), Hall-V (P22.1) and Hall-W (P22.3) with edge detection

Note: *For details, see the CPU interrupt handing sections in the **Architecture TRM**.*

Note: *The contents of this application note are the result of verification in an evaluation environment. In the user environment, it may be necessary to change the setting.*

3.2 Motor Control Operation

Figure 4 shows an example of 120-degree commutation control using Hall ICs in this use case. In this case, change of the rotational position by the Hall IC is detected using interrupts.

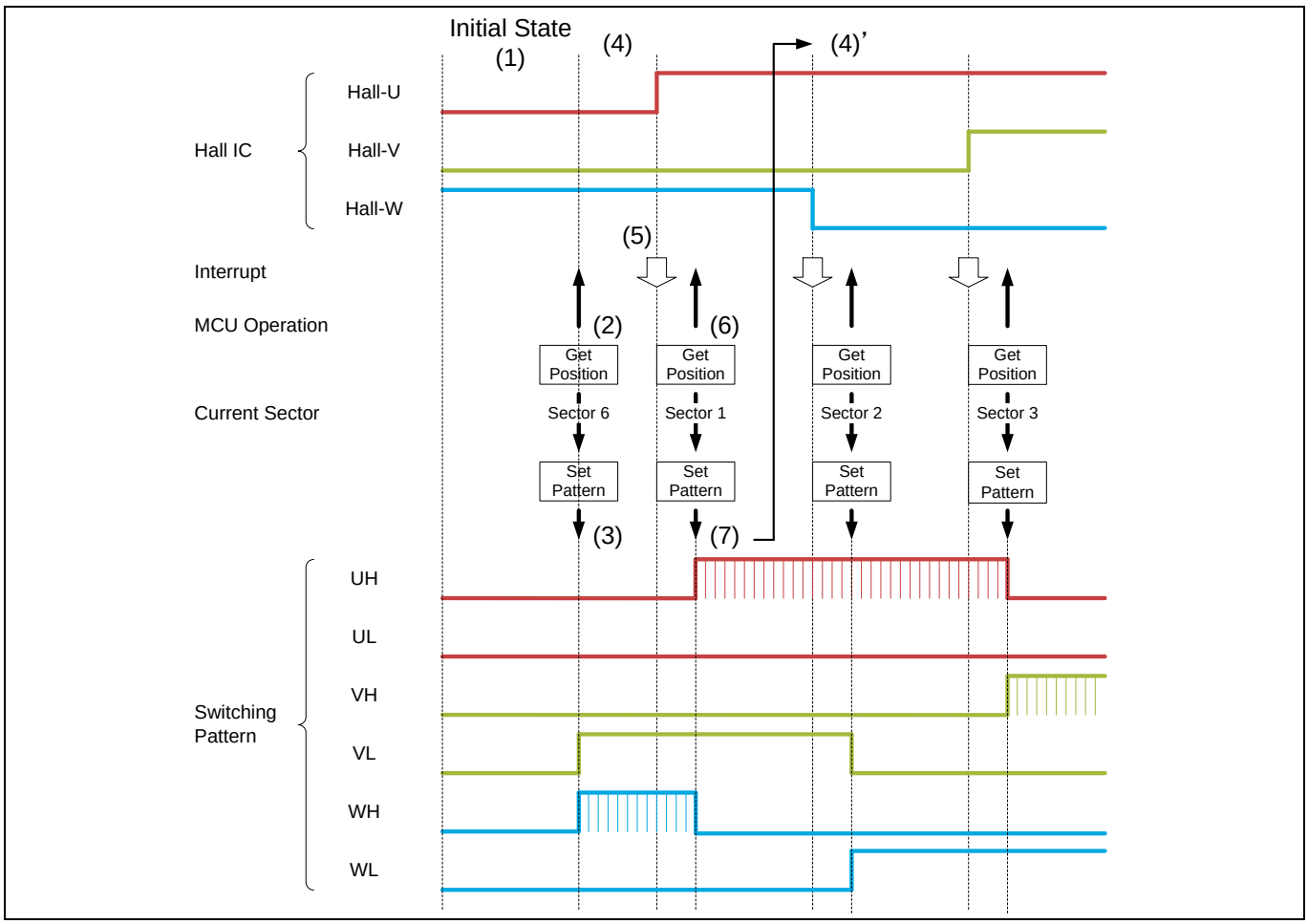

Figure 4 Operation Example of 120-degree Commutation Control

(1) In the initial state, motor is stopped.

(2) In this case, when the MCU starts motor control, the MCU reads the current rotational position of the motor without interrupt occurrence (in this example, the initial state is sector 6).

(3) The current rotational position is sector 6, so the MCU uses the lookup table (LUT[1]) to set the control signals (UH, UL, VH, VL, WH, WL) corresponding to sector 6 to TCPWM and I/O System.

(4) When the control signals are driven out, current is supplied to the motor. As a result, the motor starts rotating and transitions to the next sector.

(5) When the motor transitions to the next sector, the rotation position signal from the Hall IC changes to the next sector state. An interrupt is generated by this state change.

[1] In 120-degree commutation control, the switching pattern corresponding to the sector number is uniquely determined. Therefore, it helps to improve the performance of the motor control processing by preparing the LUT of the switching pattern corresponding to the sector in advance.

(6) The MCU detects that the change in the sector state of the motor by an external interrupt and reads the current sector.

(7) The MCU uses the LUT to set the control signal corresponding to the current sector to the TCPWM and I/O System

(8) Steps (4) to (7) are repeated.

3.3 Flow of Initial Setting and Motor Control

Figure 5 shows an example of initial setting and control flow for 120-degree commutation control using Hall ICs in this use case.

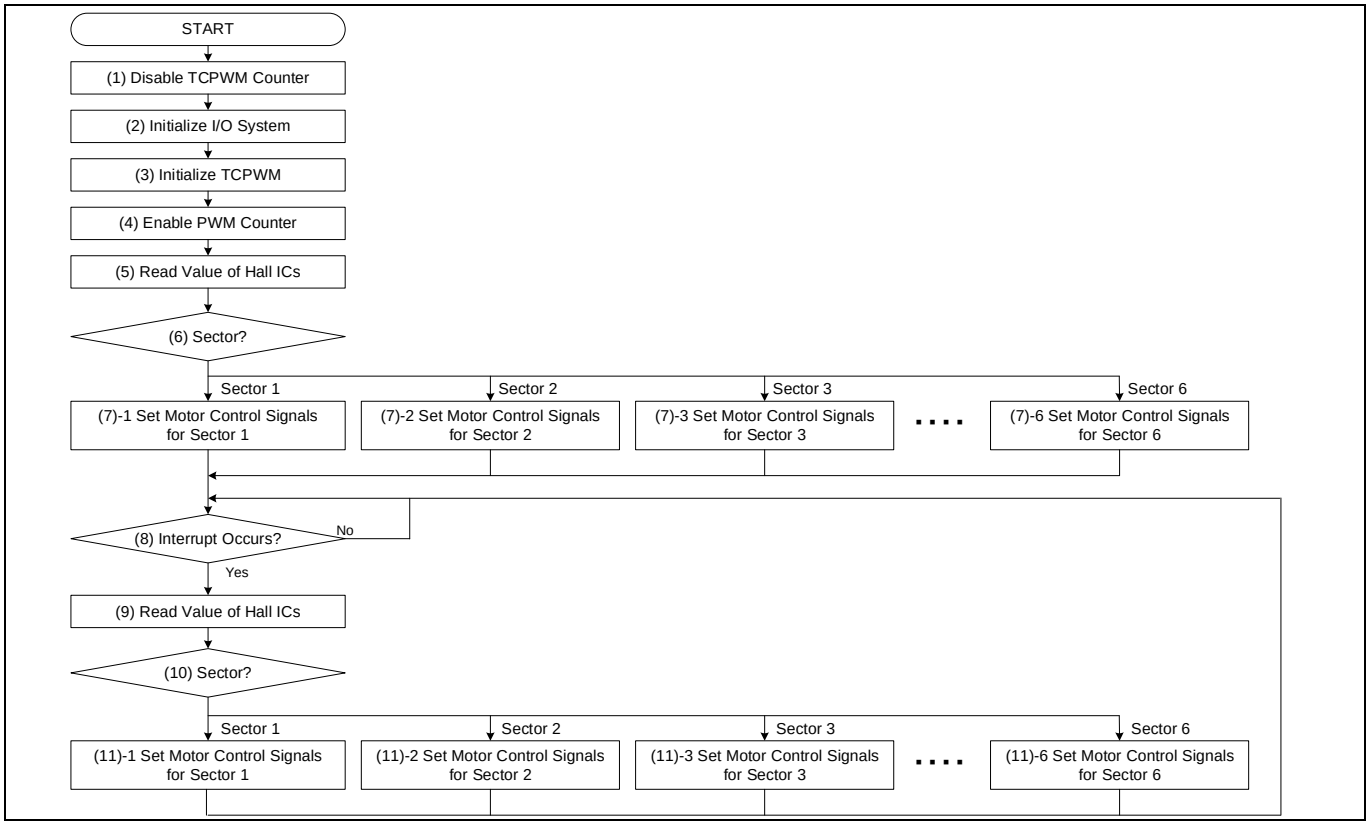

Figure 5 Example of Initial Setting and Control and Setting Flow

(1) Disable the counter of TCPWM to prevent unintentional output of the PWM pulse.
Write TCPWM0_GRP0_CNT0_CTRL.ENABLE = “0” (Disable counter_GR0#0)
Write TCPWM0_GRP0_CNT2_CTRL.ENABLE = “0” (Disable counter_GR0#2)
Write TCPWM0_GRP0_CNT3_CTRL.ENABLE = “0” (Disable counter_GR0#3)

(2) Set the interface condition of the pins in the I/O System. See sections **4.1.1 Motor Control Signals** and **4.1.2 Hall IC Signals**.

(3) Set the operation mode and trigger condition in the TCPWM. See section **4.2.1 Initial Setting**.

(4) Enable the counter of TCPWM
Write TCPWM0_GRP0_CNT0_CTRL.ENABLE = “1” (Enable counter_GR0#0)
Write TCPWM0_GRP0_CNT3_CTRL.ENABLE = “1” (Enable counter_GR0#3)
Write TCPWM0_GRP0_CNT2_CTRL.ENABLE = “1” (Enable counter_GR0#2)

(5) Read the Hall IC values. see **Table 8**.
Read GPIO_PRT22.IN0 register bit for U-phase hall IC value
Read GPIO_PRT22.IN1 register bit for V-phase hall IC value
Read GPIO_PRT22.IN3 register bit for W-phase hall IC value

(6) Determine the sector from Hall IC values. See **Table 1** to determine the sector number from Hall IC values in this use case.
When [U-phase, V-phase, W-phase] is [0, 0, 1], sector number is 6.

(7) Set control signals depending on the sector number. See **Table 1** for the mapping between the sector number and output signals in this use case. An example of sector 1 is shown below:
Write TCPWM0_GRP0_CNT0_TR_CMD.Reload = "1" (UH)
Write TCPWM0_GRP0_CNT3_TR_CMD.Stop/kill = "1" (VH)
Write TCPWM0_GRP0_CNT2_TR_CMD.Stop/kill = "1" (WH)
Write GPIO_PRT17_OUT[0] = "0" (UL)
Write GPIO_PRT17_OUT[1] = "1" (VL)
Write GPIO_PRT17_OUT[2] = "0" (WL)
See section **Note:** for more details on setting the TCPWM output.

(8) Wait for interrupt by rotational position change.

(9) When the interrupt occurs, read the Hall IC values. See step (5).

(10) Determine the sector from Hall IC values. See step (6).

(11) Set control signals depending on the sector number. See Step (7).
Wait for the interrupt caused by the change in the rotational position. Repeat steps (8) to (11).

Table 1 lists Hall IC values, sector number, and output signals in this use case. These are uniquely determined when Hall IC values are determined, and used as a LUT in motor control. Note that Hall IC values and output signals differ depending on the motor used.

Table 1 Commutation Table of Switching Pattern

Sector	Hall IC Value			Output Signals					
	U	V	W	UH	UL	VH	VL	WH	WL
1	1	0	1	PWM[2]	0	0	1	0	0
2	1	0	0	PWM[2]	0	0	0	0	1
3	1	1	0	0	0	PWM[2]	0	0	1
4	0	1	0	0	1	PWM[2]	0	0	0
5	0	1	1	0	1	0	0	PWM[2]	0
6	0	0	1	0	0	0	1	PWM[2]	0

[2] PWM means output of PWM pulses.

4 Setting and Operation Example

4.1 I/O System

4.1.1 Motor Control Signals

(1) Initial Setting of UH/VH/WH

UH, VH, and WH are connected to the TCPWM counter_GR0#0 output, counter_GR0#2 output, and counter_GR0#3 output, respectively. In this section, an example for assigning PWM_0, PWM_2, and PWM_3 to the highlighted parts of **Figure 6** is shown. For the TCPWM output setting, refer to the **TCPWM** section in this document.

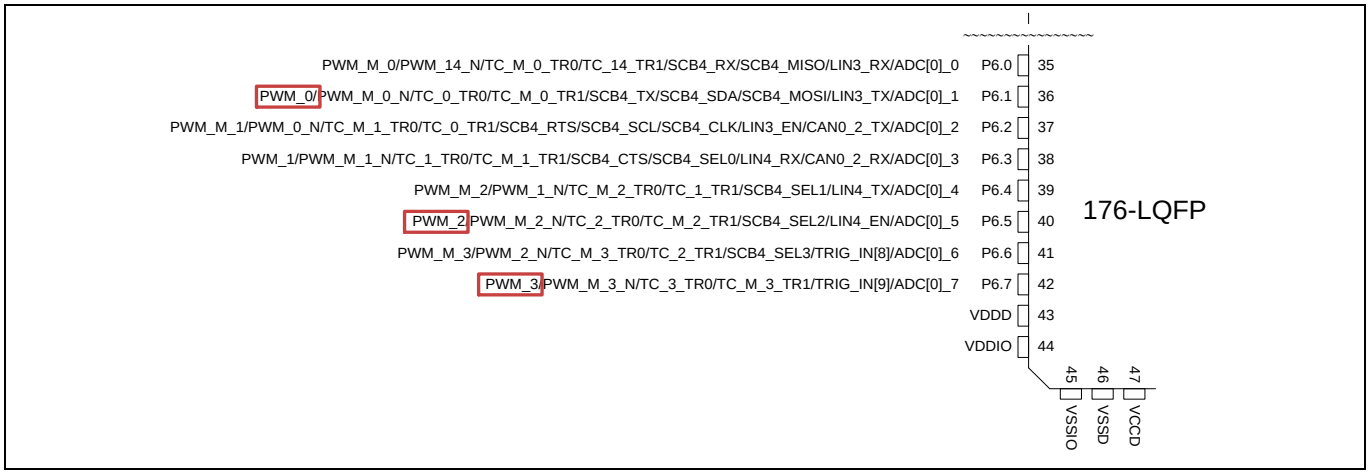

Figure 6 Pin Assignments of Motor Control Signals

Table 2 and **Table 3** show setting examples for assigning PWM_0, PWM_2, and PWM_3 as shown in **Figure 6**.

Table 2 GPIO Setting of Motor Control Signals

Register				Description	Initial Setting
Name		Bits			
GPIO_PRT6	CFG	[6:4]	DRIVE_MODE1	0x0: HIGHZ 0x1: RESERVED 0x2: PULLUP 0x3: PULLDOWN 0x4: OD_DRIVESLOW 0x5: OD_DRIVESHIGH 0x6: STRONG 0x7: PULLUP_DOWN	0x6 (UH, PWM_0)
		[22:20]	DRIVE_MODE5		0x6 (WH, PWM_2)
		[30:28]	DRIVE_MODE7		0x6 (VH, PWM_3)
	CFG_IN	[1]	VTRIP_SEL1_0	0: CMOS 1: TTL	0 (UH, PWM0)
		[5]	VTRIP_SEL5_0		0 (WH, PWM2)
		[7]	VTRIP_SEL7_0		0 (VH, PWM3)

*Note: For details, refer to the I/O System section in the **Architecture TRM**.*

Setting and Operation Example

Table 3 HSIOM Setting of Motor Control Signals

Output Pin	Register				Description	Initial Setting
	Name		Bits			
P6.1	HSIOM_PRT6	PORT_SEL0	[12:8]	IO1_SEL	0x0: GPIO: GPIO controls “out” : 0x8: ACT_0: Active functionality 0 0x9: ACT_1: Active functionality 1 0xa: ACT_2: Active functionality 2 0xb: ACT_3: Active functionality 3 : 0x1f: DS_7: DeepSleep functionality 7	0x8 (UH, PWM_0)
P6.5		PORT_SEL1	[12:8]	IO5_SEL		0x8 (WH, PWM_2)
P6.7			[28:24]	IO7_SEL		0x8 (VH, PWM_3)

*Note: For details, refer to the Alternate Function Pin Assignments sections in the Datasheet and **Registers TRM**.*

(2) Initial Setting of UL/VL/WL

UL, VL, and WL signals are output from terminals P17.0, P17.1, and P17.2. Here, an example for assigning UL, VL, and WL to the highlighted values in **Figure 7** is shown.

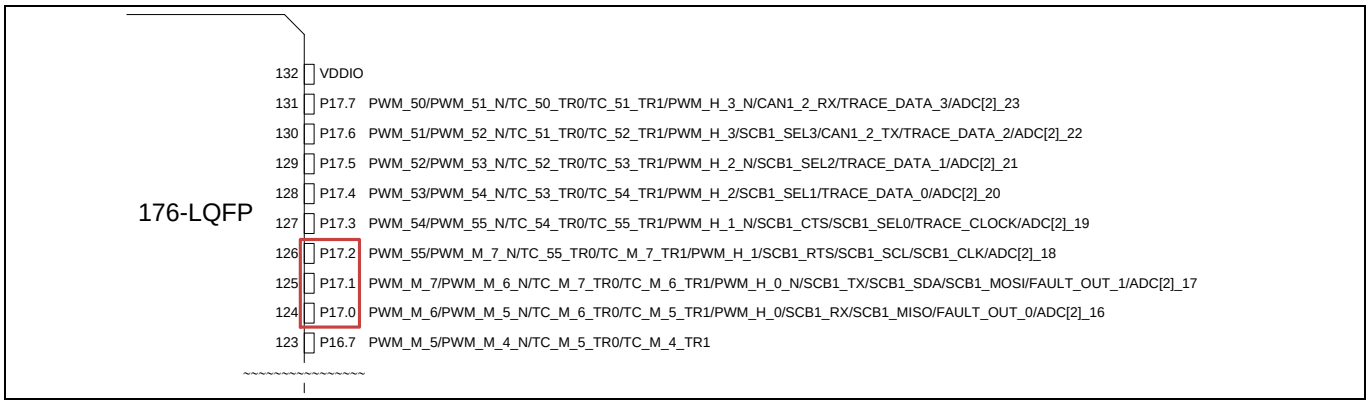

Figure 7 Pin Assignments of Motor Control Signals

Setting and Operation Example

Table 4 and **Table 5** show setting examples for assigning UL, VL, and WL.

Table 4 GPIO Setting of Motor Control Signals

Register				Description	Initial Setting
Name		Bits			
GPIO_PRT17	OUT	[7:0]	OUT7:0	'0': Output state set to '0' '1': Output state set to '1'	0 (For details of operation, refer to section **3.3 Flow of Initial Setting and Motor Control** in this document.)
	CFG	[3]	IN_EN0	'0': Input buffer disabled '1': Input buffer enabled	0 (UL)
		[7]	IN_EN1		0 (VL)
		[11]	IN_EN2		0 (WL)
		[2:0]	DRIVE_MODE0	0x0: HIGHZ 0x1: RESERVED 0x2: PULLUP 0x3: PULLDOWN 0x4: OD_DRIVESLOW 0x5: OD_DRIVESHIGH 0x6: STRONG 0x7: PULLUP_DOWN	0 (UL)
		[6:4]	DRIVE_MODE1		0 (VL)
		[10:8]	DRIVE_MODE2		0 (WL)
	CFG_IN	[0]	VTRIP_SEL0_0	0: CMOS 1: TTL	0 (UL)
		[1]	VTRIP_SEL1_0		0 (VL)
		[2]	VTRIP_SEL2_0		0 (WL)

*Note: For details, refer to the I/O System section in the **Architecture TRM**.*

Setting and Operation Example

Table 5 HSIOM Setting of Motor Control Signals

Output Pin	Register				Description	Initial Setting
	Name		Bits			
P17.0	HSIOM_PRT17	PORT_SEL0	[4:0]	IO0_SEL	0x0: GPIO: GPIO controls “out” : 0x8: ACT_0: Active functionality 0 0x9: ACT_1: Active functionality 1 0xa: ACT_2: Active functionality 2 0xb: ACT_3: Active functionality 3 : 0x1f: DS_7: DeepSleep functionality 7	0x0 (UL)
P17.1						
P17.2						

*Note: For details, refer to the Alternate Function Pin Assignments sections in the **Datasheet** and **Registers TRM**.*

4.1.2 Hall IC Signals

Hall IC signals are input to terminals Hall-U (P22.0), Hall-V (P22.1), and Hall-W (P22.3). Here, an example for assigning the signals of Hall IC to P22.0, P22.1, and P22.3 is shown in **Figure 8**.

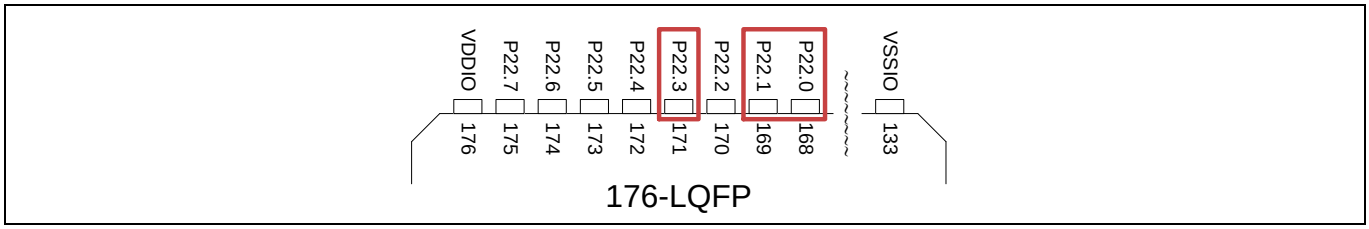

Figure 8 Pin Assignments of Hall ICs Output Signals

Table 6 and **Table 7** show setting examples for assigning Hall-U, Hall-V, and Hall-W.

Table 6 GPIO Setting of Hall ICs Output Signals

Register				Description	Initial Setting
Name		Bits			
GPIO_PRT22	INTR_CFG	[1:0]	EDGE0_SEL	0x0: DISABLE 0x1: RISING 0x2: FALLING 0x3: BOTH	0x3 (Hall-U)
		[3:2]	EDGE1_SEL		0x3 (Hall-V)
		[7:6]	EDGE3_SEL		0x3 (Hall-W)
	CFG	[3]	IN_EN0	'0': Input buffer disabled '1': Input buffer enabled	1 (Hall-U)
		[7]	IN_EN1		1 (Hall-V)
		[15]	IN_EN3		1 (Hall-W)

Setting and Operation Example

Register				Description	Initial Setting
Name		Bits			
		[2:0]	DRIVE_MODE0	0x0: HIGHZ 0x1: RESERVED 0x2: PULLUP 0x3: PULLDOWN 0x4: OD_DRIVESLOW 0x5: OD_DRIVESHIGH 0x6: STRONG 0x7: PULLUP_DOWN	0x0 (Hall-U)
		[6:4]	DRIVE_MODE1		0x0 (Hall-V)
		[14:12]	DRIVE_MODE3		0x0 (Hall-W)
	CFG_IN	[0]	VTRIP_SEL0_0	0: CMOS 1: TTL	0 (Hall-U)
		[1]	VTRIP_SEL1_0		0 (Hall-V)
		[3]	VTRIP_SEL3_0		0 (Hall-W)

*Note: For details, refer to the I/O System section in the **Architecture TRM**.*

Table 7 HSIOM Setting of Hall ICs Output Signals

Input Pin	Register				Description	Initial Setting
	Name		Bits			
P22.0	HSIOM_PRT22	PORT_SEL0	[4:0]	IO0_SEL	0x0: GPIO: GPIO controls “out” : 0x8: ACT_0: Active functionality 0 0x9: ACT_1: Active functionality 1 0xa: ACT_2: Active functionality 2 0xb: ACT_3: Active functionality 3 : 0x1f: DS_7: DeepSleep functionality 7	0x0 (Hall-U)
P22.1			[12:8]	IO1_SEL		0x0 (Hall-V)
P22.3			[28:24]	IO3_SEL		0x0 (Hall-W)

*Note: For details, refer to the Alternate Function Pin Assignments sections in the **Datasheet** and **Registers TRM**.*

Setting and Operation Example

The Hall IC output value can be confirmed with the registers listed in **Table 8**. When the values are set as shown in **Table 6** and **Table 7**, MCU causes an interrupt according to the change in Hall IC output. When an interrupt occurs, the software can detect the rotor position by reading the registers in **Table 8**.

Table 8 HSIOM Setting of Hall ICs Output Signals

Input Pin	Register				Description	Remarks
	Name		Bits			
P22.0	GPIO_PRT22	IN	[0]	IN0	Port input state register	No (Hall-U)
P22.1			[1]	IN1		No (Hall-V)
P22.3			[3]	IN3		No (Hall-W)

*Note: For details, refer to the I/O System section in the **Architecture TRM**.*

4.2 TCPWM

4.2.1 Initial Setting

Table 9 shows an example of TCPWM configuration in this use case.

Table 9 Setting of PWM Mode for 120-degree Commutation Control

Target Counter		Register		Description	Initial Setting
Group	No	Name	Bits		
Group [0]	CNT0,2,3	CTRL	AUTO_RELOAD_CC0 [0]	0: Never switch. 1: Switch ON a terminal count event with an actively pending switch event.	0
			AUTO_RELOAD_PERIOD [1]	0: Never switch. 1: Switch ON a terminal count event with and actively pending switch event.	0
			PWM_IMM_KILL [8]	0: Synchronous kill activation 1: Immediate kill activation	0
			PWM_STOP_ON_KILL [9]	0: Kill event does NOT stop counter 1: Kill event stops counter	0
			PWM_SYNC_KILL [10]	1: Synchronous kill mode 0: Asynchronous kill mode	0

Setting and Operation Example

Target Counter		Register		Description	Initial Setting
Group	No	Name	Bits		
			UP_DOWN_MODE [17:16]	0x0: COUNT_UP 0x1: COUNT_DOWN 0x2: COUNT_UPDN1 0x3: COUNT_UPDN2	0x0
			MODE [26:24]	0x0: TIMER 0x1: Reserved 0x2: CAPTURE 0x3: QUAD 0x4: PWM 0x5: PWM_DT 0x6: PWM_PR 0x7: SR	0x4
		CC0	CC0 [31:0]	Compare value	0x40 see "**Note:**"
		PERIOD	PERIOD [31:0]	PWM period	0xEF (39 µs) see "**Note:**"
		DT	DT_LINE_OUT_L [7:0]	0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8 0x4: Divide by 16 0x5: Divide by 32 0x6: Divide by 64 0x7: Divide by 128	0x00
		TR_IN_SEL0	CAPTURE0_SEL [7:0]	0x00: 0 fixed 0x01: 1 fixed 0x02 to 0xff: one of the 254 input triggers	0x00
			COUNT_SEL [15:8]		0x01
			RELOAD_SEL [23:16]		0x00
			STOP_SEL [31:24]		0x00
		TR_IN_EDGE_SEL	CAPTURE0_EDGE [1:0]	0x0: RISING_EDGE 0x1: FALLING_EDGE 0x2: ANY_EDGE 0x3: NO_EDGE	0x3
			COUNT_EDGE [3:2]		0x3
			RELOAD_EDGE [5:4]		0x3
			STOP_EDGE [7:6]		0x3
			START_EDGE [9:8]		0x3
			CAPTURE1_EDGE [11:10]		0x3
		TR_PWM_CTRL	CC0_MATCH_MODE [1:0]	0x0: SET (Set to '1') 0x1: CLEAR (Set to '0') 0x2: INVERT 0x3: No Change	0x1
			OVERFLOW_MODE [3:2]		0x0
			UNDERFLOW_MODE [5:4]		0x3
			CC1_MATCH_MODE [7:6]		0x3

Setting and Operation Example

*Note: For details, refer to the TCPWM section in the **Architecture TRM**.*

4.2.2 Operation of PWM Output (UH/VH/WH)

In PWM mode, the counter for generating the PWM pulse is controlled by the control signals highlighted in **Figure 9**.

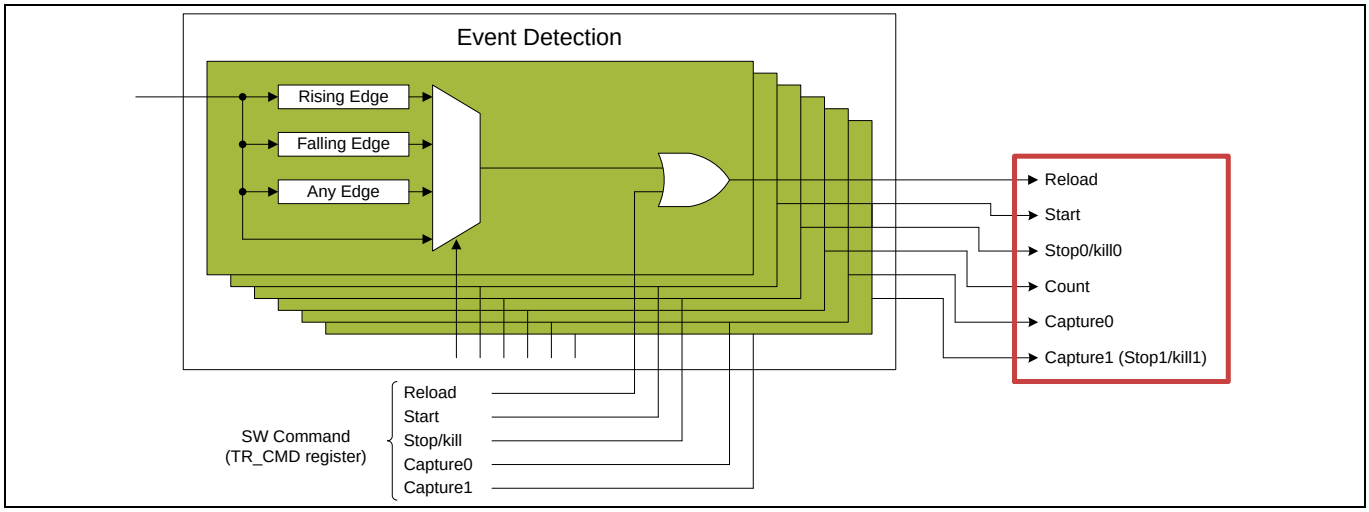

Figure 9 Counter Control Signals and Software Commands

- Reload: Sets the counter value and starts the counter.
- Start: Starts the counter.
- Stop0/kill0: Stops the counter and suppress the output signals.
- Count: Count event increments or decrements the counter.
- Capture0: This event acts as a switch event.
- Capture1 (Stop1/kill1): This event acts as a second stop/kill event.

The PWM pulse output can be turned ON/OFF using the Reload and Stop0/kill0 signal. The Reload and Stop0/kill0 signals can be easily generated using the TCPWM block software command (SW command).

SW commands can be generated by operating "TR_CMD register" in **Table 10**.

- When the “Reload bit” of TR_CMD register is set to ‘1’, the “Reload signal” is input to the counter. The counter initializes and starts, and the PWM pulse is output.
- When the “Stop/kill bit” of TR_CMD register is set to ‘1’, the “Stop0/kill0 signal” is input to the counter. PWM pulses are suppressed.

Table 10 Operation of TR_CMD Register

Target Counter		Register		Description
Group	No	Name	Bits	
Group [0]	CNT0,2,3	TR_CMD	CAPTURE0 [0]	This event acts as a switch event. This bit is not used here.
			Reload [2]	When this bit is set to ‘1’, the counter starts and the PWM output signal is output.
			Stop/kill [3]	When this bit is set to ‘1’, the PWM output signal is suppressed to ‘0’.

Setting and Operation Example

Target Counter		Register		Description
Group	No	Name	Bits	
			START [4]	Starts the counter. The counter is not initialized by hardware This bit is not used here.
			CAPTURE1 [5]	This event acts as a second stop/kill event. It has the same function as the stop1/kill1 event. This bit is not used here.

*Note: For details, refer to the TCPWM section in the **Architecture TRM**.*

The period and duty of the PWM output are determined by the setting of the PERIOD register and CC0 register respectively. The counter cycle is determined by the period of the PERIOD register, and the output duty changes with the compare value of the CC0 register (**Figure 10**). For details, refer to the TCPWM section in the **Architecture TRM**.

If using speed control, the compare value must be determined by software according to the number of revolutions and set in the CC0 register.

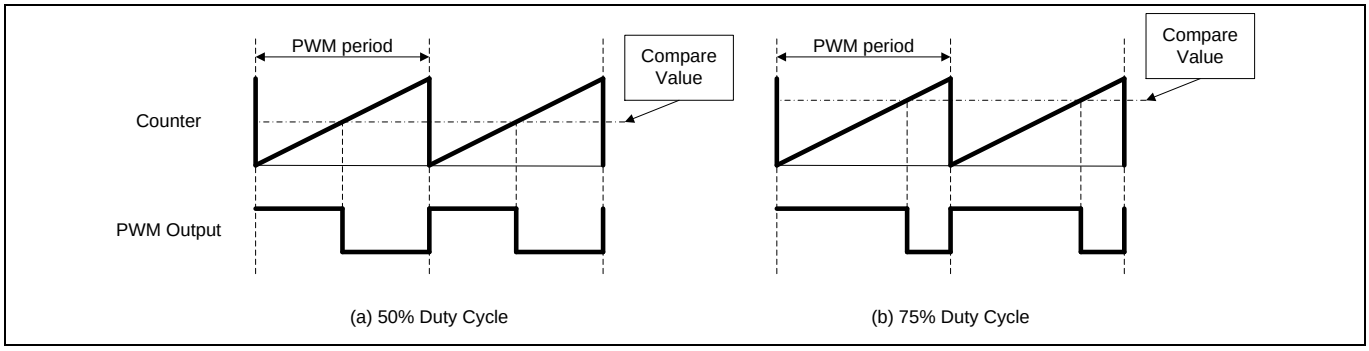

Figure 10 Duty Control for PWM Pulse

5 Glossary

Table 11 Glossary

Terms	Description
BLDC Motor	Brushless DC Motor
CW	Clockwise
GPIO	General-Purpose Input/Output
HSIOM	High-Speed I/O Matrix
IP	Intellectual Property
LQFP	Low profile Quad Flat Package
LUT	Lookup Table
PWM	Pulse Width Modulation
SW Command	Software Command
TCPWM	Timer, Counter, and Pulse Width Modulator. See the Timer, Counter, and PWM chapter of the **Architecture TRM** for details.
UH/UL	High-side signal of U-phase/Low-side signal of U-phase
VH/VL	High-side signal of V-phase/Low-side signal of V-phase
WH/WL	High-side signal of W-phase/Low-side signal of W-phase

6 Related Documents

- Datasheet
  - CYT2B5/B7 Series Datasheet (Contact **Technical Support**)
- Technical Reference Manuals
  - Traveo™ II Automotive Body Controller Entry Family Architecture Technical Reference Manual (Contact **Technical Support**)
  - Traveo™ II Automotive Body Controller Entry Registers Technical Reference Manual (Contact **Technical Support**)

Revision history

Document version	Date of release	Description of changes
**	2018-09-28	New application note.
*A	2021-04-28	Updated to Infineon template.

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