SRK1000 / SRK1000A /SRK1000B

Datasheet

Adaptive synchronous rectification controller for flyback converter

SOT23-6L

Features

- Secondary side synchronous rectification controller optimized for flyback converter.
- Suitable for QR and mixed CCM/DCM fixed frequency operation.
- Wide V_{cc} operating voltage range 3.75 to 32 V.
- CC regulation operation down to 2 V output supported.
- Very low quiescent current in low consumption mode (160 µA).
- High-voltage sensing input for SR MOSFET drain-source voltage (100 V AMR).
- Operating frequency up to 300 kHz.
- High-current gate-drive output for N-MOSFET.
- Fast turn-on with minimum delay time and adaptive turn-off logic.
- Programmable min. T_{ON} and fixed min. T_{OFF} (3 options: SRK1000, SRK1000A, SRK1000B).
- Low consumption mode entry by primary side burst-mode detection or by detection of SR MOSFET conduction lower than programmed min T_{ON}.
- SOT23-6L package.

Application

- Battery chargers / quick chargers
- Adapters
- USB power delivery (profile 3)

Product status link
SRK1000 / SRK1000A /SRK1000B

Product summary	
Order code	SRK1000 SRK1000ATR SRK1000BTR
Package	SOT23-6L
Packing	Tape and reel

Product label
SUSTAINABLE TECHNOLOGY

Description

SRK1000 / SRK1000A /SRK1000B are controllers intended for secondary side synchronous rectification (SR) in flyback converters, suitable for operation in QR and mixed CCM/DCM fixed frequency circuits.

They provide a high-current gate-drive output, capable of driving N-channel Power MOSFETs.

The control scheme of this IC is such that the SR MOSFET is switched on as soon as current starts flowing through its body diode and it is then switched off as current approaches zero.

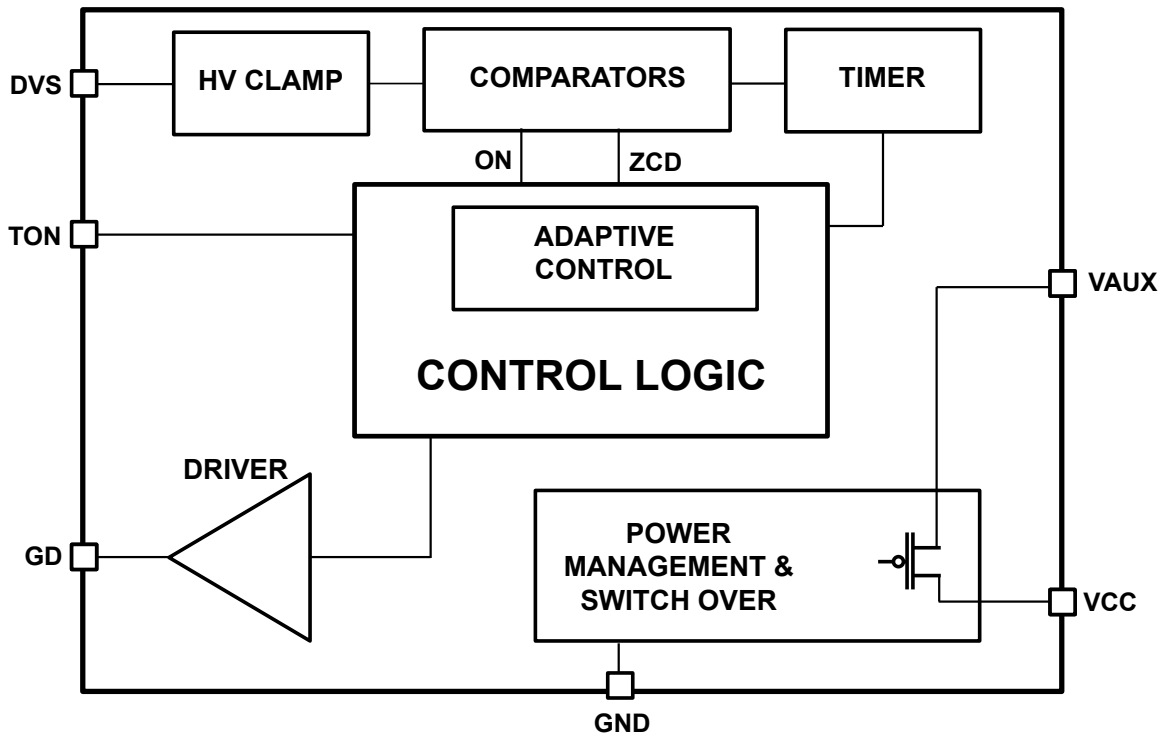
The fast turn-on, with minimum delay, and the innovative adaptive turn-off logic allow maximizing the conduction time of the SR MOSFET and eliminating the effect of parasitic inductance in the circuit.

The device enters low consumption mode when it detects primary controller burst-mode operation, or when the SR MOSFET conduction becomes lower than the programmed minimum T_{ON}. In this way, converter efficiency improves at light load where synchronous rectification is no longer beneficial.

After the converter restarts switching or the IC detects that the current conduction in the rectifiers has increased 20% above the min T_{ON} programmed value, the IC exits low consumption mode and resumes switching operation.

1 Block diagram

Figure 1. **Internal block diagram**



2 Pin description

Figure 2. **Pin pin configuration**

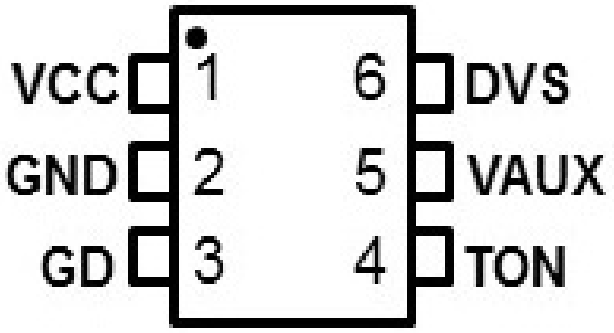


Table 1. **Pin description (top view)**

No.	Name	Function
1	VCC	Supply voltage of the device. A bypass capacitor to GND, located as close to IC's pins as possible, helps to get a clean supply voltage for the internal control circuitry and acts as an effective energy buffer for the pulsed gate drive current.
2	GND	Return of the device bias current and return of the gate drive current. Route this pin close to the source terminal of synchronous rectifier MOSFET.
3	GD	Gate driver output. Totem pole output stage is able to drive power MOSFET with high peak current levels. To avoid excessive gate voltages in case the device is supplied with a high VCC, the high level voltage of this pin is clamped to about 11.6 V (typ. value). The pin has to be connected directly to the SR MOSFET gate terminal.
4	TON	Programming pin for blanking time after turn-on. A resistor connected from this pin to GND, supplied by an internal current source, sets a voltage V_{TON}; depending on this voltage level, the user can choose the blanking time after turn-on, suitable to mask ZCD comparator output and avoid premature turn-off due to parasitic voltage oscillation on DVS pin. In tracking with V_{TON}, the thresholds to enter/exit automatic sleep mode are derived. A capacitor larger than 60 pF (100 pF typ.) between this pin and GND sets the internal timer mode for SR MOSFET turn-off in mixed CCM/DCM operation. If no capacitor is used, timer mode is set for turn-off in QR or DCM operation.
5	VAUX	Auxiliary supply voltage of the device. When VCC voltage is lower than UVLO voltage threshold ($V_{CC\_SO\_On}$), the bypass capacitor on VCC pin (coupled to application V_{OUT} through a diode) is supplied by VAUX pin, if this is connected to an auxiliary winding or to an external capacitor sourced by a DVS voltage rectifier. If the functionality is not used, VAUX pin has to be connected to VCC pin.
6	DVS	Drain voltage sensing. This pin has to be connected to the drain terminal of the synchronous rectifier MOSFET through a series resistor of at least of 300 Ω.

3 Maximum ratings and thermal data

The absolute maximum rating is the maximum stress that can be applied to a device without causing permanent damage. However, extended exposure to maximum ratings may affect long-term device reliability.

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
VCC	1	DC supply voltage	-0.3 to 36	V
VTON	4	TON pin voltage rating	-0.3 to 3.6	V
VAUX	5	Auxiliary DC supply voltage	-0.3 to 100	V
DVS	6	Drain sense voltage referred to GND	-3 to 100	V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Junction-to-ambient thermal resistance (1)	200	°C/W
$R_{th\ j\text{-}case}$	Junction-to-case thermal resistance (1)	60	°C/W
P_{tot}	Power dissipation at T_{amb} = 50°C	0.5	W
T_j	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

1. *With pin 2 soldered to a dissipating copper area of 10 mm ^{2}, 35 µm thickness (PCB material FR4 1.6 mm thickness)*

4 Typical application schematics

Figure 3. **QR flyback charger with CV-CC regulation**

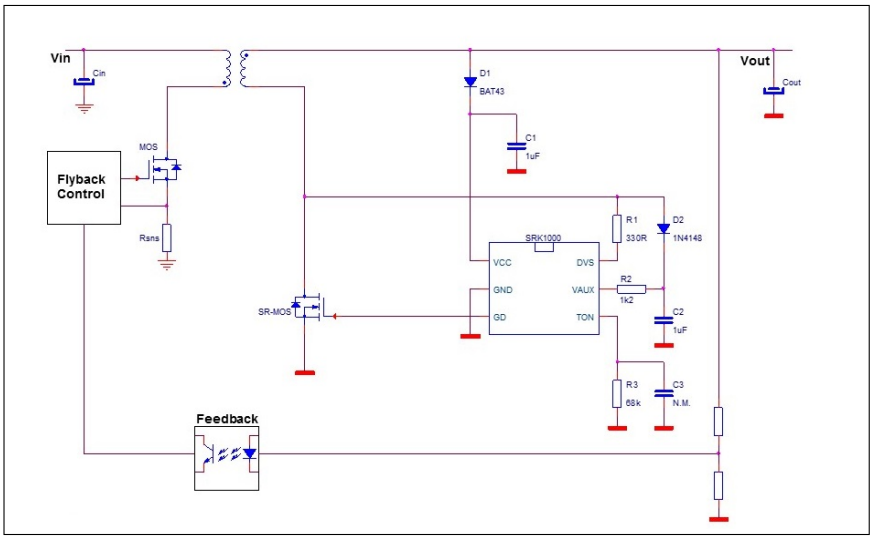


Figure 4. **QR flyback adapter (CV regulation)**

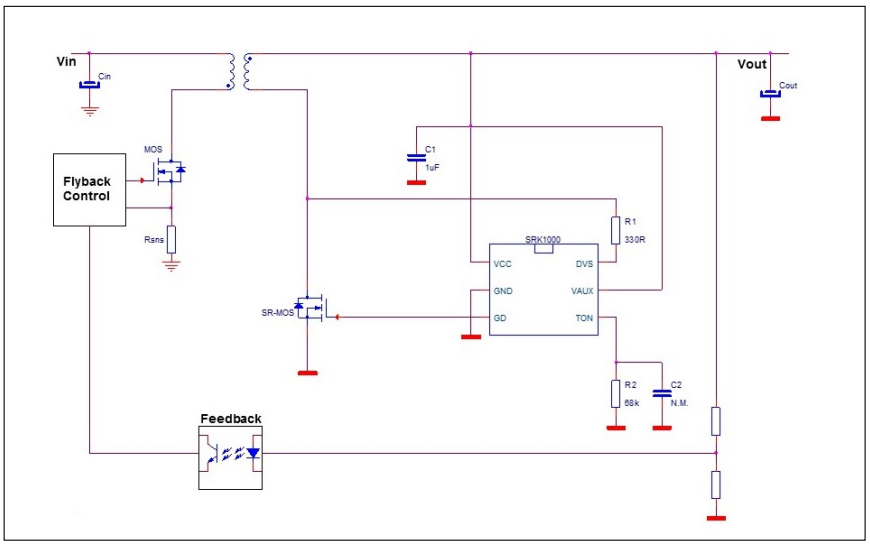
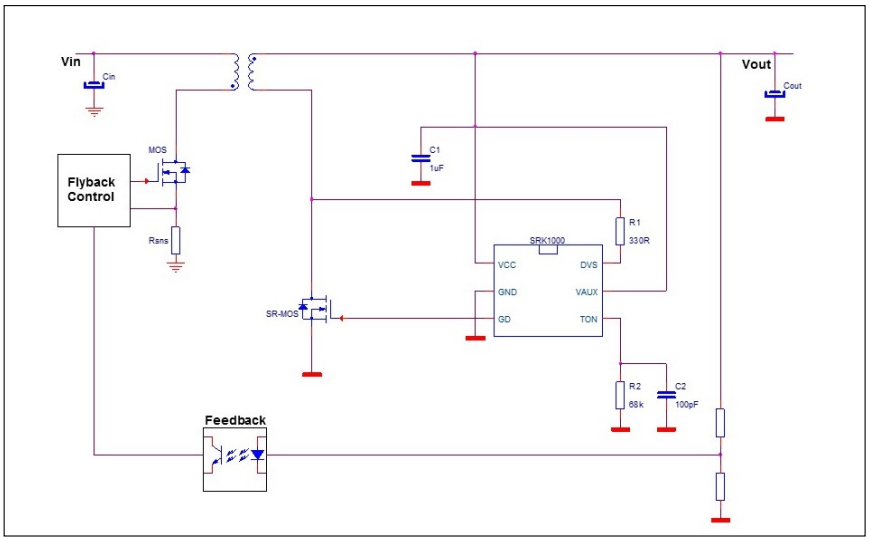


Figure 5. **Fixed frequency CCM flyback adapter (CV regulation)**



5 Electrical characteristics

Table 4. Electrical characteristics

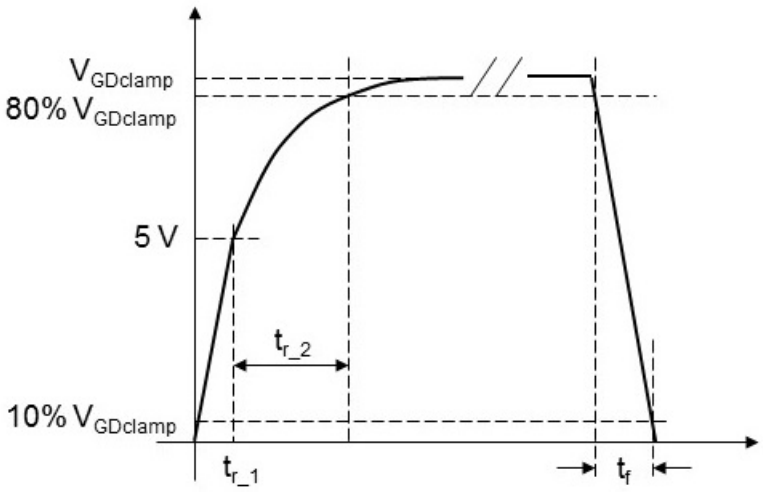
(T_j = -25°C to 125°C, V_{CC} = 12 V, C_{GD} = 4.7 nF; unless otherwise specified, typical values refer to T_j = 25°C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply section						
V_{AUX}	VAUX operating voltage				90	V
V_{CC}	Operating voltage range	After turn-on	3.75		32	V
V_{CC_On}	Turn-on supply voltage	Voltage rising (1)	4.18	4.3	4.42	V
$V_{CC\_SO\_On}$	Turn-on supply voltage for VAUX switch activation	Voltage falling (1)	3.75	3.95	4.15	
V_{CC_Off}	Turn-off supply voltage	Voltage falling (1)	3.3	3.5	3.7	V
$V_{CC\_AGD\_en}$	V_{CC} voltage above which adaptive drive is enabled	On V_{CC} rising edge (2)		7.4		V
$V_{CC\_AGD\_dis}$	V_{CC} voltage below which adaptive drive is disabled	On V_{CC} falling edge (2)		6.5		V
I_{q_run}	Current consumption in run mode	After turn-on (excluding SR MOS gate driving) @ 100 kHz		600		µA
I_{CC}	Operating supply current	@ 300 kHz		17		mA
I_q	Quiescent current	Burst- mode operation, DVS pin not switching, Tj = -25°C to 85°C		160	210	µA
R_{on}	VAUX switch resistance			40		Ω
Drain-source sensing input and synch functions						
V_{DS}	DVS operating voltage				90	V
V_{TH_A}	Cycle comparator threshold		70	100	130	mV
$V_{ZCD\_OFF\_MIN}$	Minimum ZCD comparator threshold	(2)		-20		mV
T_{diode_off}	Body diode residual conduction time after turn-off		230	330	430	ns
T_{D_On}	Turn-on delay		55	85	105	ns
T_{ant_timer}	Anticipation time referred to DVS rising edge to force turn off of SR MOSFET	DVS switching Low level on DVS pin = -1 V	180	280	380	ns
T_{timer_step}	Timer step every 4 switching cycles (in FF operation)	With 100pF on TON pin, during switching period increase		56		ns
T_{ON_MAX}	Max turn-on duration		45	60		µs
Blanking time after turn-on and after turn-off						
T_{ON_MIN}	Minimum turn-on time programmable by R_{TON} in the range [33 kΩ - 250 kΩ]	R_{TON_MIN} = 33 kΩ	0.28	0.4	0.52	µs
		R_{TON_MAX} = 250 kΩ	2.1	3.0	3.9	
I_{TON}	Sourced current	In run mode		8		µA
T_{OFF_MIN}	Fixed blanking time after turn-off (with DVS voltage continuously above V_{TH_A})	SRK1000	0.35	0.5	0.65	µs
		SRK1000A	1.4	2	2.6	
		SRK1000B	2.1	3	3.9	

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Low consumption mode						
$T_{ON\_sleep\_in}$	Minimum operating current conduction time to enter sleep-mode: $T_{ON\_sleep\_in} = T_{ON\_MIN} + 300$ ns	R_{TON_MIN} = 33 kΩ	0.49	0.7	0.91	µs
		R_{TON_MAX}= 250 kΩ	2.31	3.3	4.29	
$T_{ON\_sleep\_out}$	Restart current conduction time from sleep-mode: $T_{ON\_sleep\_out} = 1.2\ T_{ON\_MIN} + 300$ ns	R_{TON_MIN} = 33 kΩ	0.55	0.78	1	µs
		R_{TON_MAX}= 250 kΩ	2.73	3.9	5.07	
T_{stop}	Switching stop time interval detection to enter low consumption mode (primary controller burst-mode)		80	120	160	µs
Gate drivers						
I_{source_pk}	Output source peak current	See (2)		0.6		A
I_{sink_pk}	Output sink peak current	See (2)		1		A
t_{r_1}	Rise Time (see Figure 6)	V_{CC} = 20V, C_{GD} = 4.7 nF		45		ns
		V_{CC} = 20V, C_{GD} = 10 nF		75		
t_{r_2}	Rise Time (see Figure 6)	V_{CC} = 20V, C_{GD} = 4.7 nF		140		ns
		V_{CC} = 20V, C_{GD} = 10 nF		140		
t_f	Fall Time (see Figure 6)	V_{CC} = 20V, C_{GD} = 4.7 nF		60		ns
		V_{CC} = 20V, C_{GD} = 10 nF		120		
$V_{GDclamp}$	Drive clamp voltage	V_{CC} = 20V (3)	10.6	11.6	12.6	V
$V_{GD\_ad\text{-}step}$	Adaptive driving step voltage	V_{CC} = 20V (3)		400		mV
V_{GDL_UVLO}	UVLO saturation	V_{CC} = 0 to $V_{\_On,\ I\ sink}$ = 5 mA		1	1.3	V

1. *Parameters tracking each other.*
2. *Parameter guaranteed by design.*
3. *Parameters tracking each other.*

Figure 6. Rise and fall time definition



6 Operation description

The SRK1000/A/B (see Figure 1) are controllers specifically designed for synchronous rectification in flyback converters operating in QR or mixed CCM/DCM fixed frequency. This IC basically turns on the SR MOSFET with a minimum delay when the rectified current starts flowing through the body diode, and turns off the SR MOSFET when current approaches zero, using an adaptive mechanism that leads the body diode residual conduction time after turn-off to the target value T_{diode_off} (refer to Electrical characteristics : for the various parameter values).

The adaptive turn-off method presents some advantages, compared to a standard one based on a comparator with fixed threshold. The first advantage is that the adaptive method automatically compensates stray inductances L_S in series to rectified current path: this parasitic (mainly the SR MOSFET package inductances in series to drain and source terminals) normally produces an offset on the sensed voltage across MOSFET R_{DS_ON} that anticipates by $T_X = L_S/R_{DS\_ON}$ the turn-off in case of standard comparator.

The second aspect to consider is that a standard comparator with fixed threshold turns off at a current level I_{OFF} that depends on R_{DS_ON} of the chosen SR MOSFET. Referring to the image in Figure 7 and considering a fixed comparator threshold V_{TH} = -5 mV, the turn-off current in the rectifier can be calculated. In an application with an SR MOSFET having channel resistance R_{DS_ON} = 2.5 mΩ and package stray inductance L_S = 2.5 nH, where the current slope is di/dt = -3 A/µs (for example starting from a peak current of 15 A with 5 µs transformer demagnetization), the turn-off current is:

$I_{OFF} = - V_{TH}/R_{DS\_ON} - T_X$ di/dt = 5 A, for comparator turn-off.

$I_{OFF\_AD} = - T_{diode\_off}$ di/dt = 0.9 A, for adaptive turn-off.

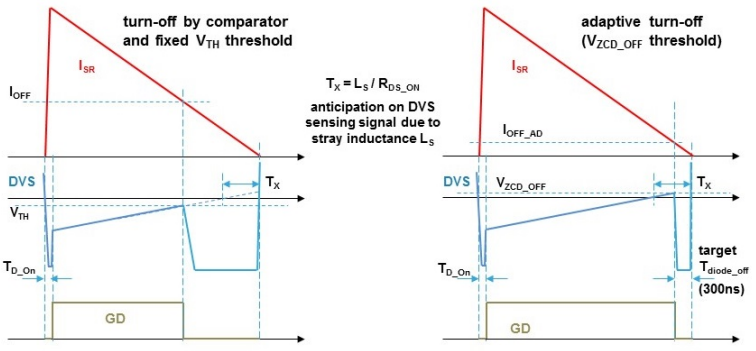
Furthermore, the adaptive turn-off method has a better behavior also in applications with CC regulation, where the standard comparator with fixed threshold anticipates more and more the turn-off during load impedance decreasing (since current slope continues to decrease too), while adaptive method fixes T_{diode_off}.

The SRK1000/A/B controllers start operation when the VCC pin voltage surpasses the turnon threshold V_{CC_On}; then it stops operation when the V_{CC} voltage drops below the turn-off threshold V_{CC_Off}.

In order to guarantee SR switching even with low V_{CC} supply voltage, in the case of chargers operating in CC regulation, the device is provided with the VAUX pin. When the V_{CC} voltage decreases below the threshold $V_{CC\_SO\_On}$ (> V_{CC_Off}), an internal switch is turned on allowing the VCC pin capacitor to be charged up to the turn-on threshold V_{CC_On} by a current drawn through the VAUX pin connected, for example, to the rectified SR MOSFET drain voltage or to another auxiliary voltage of the flyback transformer.

For the maximum flexibility in different applications and to overcome noise and ringing problems that may arise after SR MOSFET turn-on, the SRK1000/A/B allow the user to program the blanking time after turn-on through a resistor connected between the TON pin and GND. The blanking time after turn-off is instead internally fixed to T_{OFF_MIN}.

Figure 7. Comparison between adaptive turn-off and comparator based turn-off



6.1 Drain voltage sensing

The drain voltage of the SR MOSFET is sensed through the DVS pin: this is a high-voltage pin and needs to be properly routed to the MOSFET drain, through a resistor of at least 300 Ω (in order to limit dynamic current injection in any condition).

The DVS signal is used to detect when current flows through the MOSFET body diode and for the internal timings.

6.2 Turn-on

After the flyback converter primary switch has been turned off, the voltage across the transformer reverses and the SR MOSFET drain voltage quickly decreases and goes negative ($-V_F$), allowing the rectifier current to flow. Consequently, triggered on the falling edge of the DVS signal (when it decreases below the cycle comparator threshold V_{TH_A}), the controller turns on the SR MOSFET, with a very short delay T_{D_On}. After turn-on, the sensed DVS signal passes from the (negative) body diode forward voltage to the drop across the MOSFET channel resistance (R_{DS_ON}).

This drop is generally affected by some amount of noise, associated with the flyback transformer leakage inductance, and this could trigger a premature turn-off of the SR MOSFET.

6.3 Minimum TON programming

In order to avoid premature turn-off of the SR MOSFET due to ringing and oscillations, the IC allows the user to program a blanking time after turn-on. The circuit bases on an internal timing capacitance and an external resistor R_{TON} connected from the TON pin to ground.

The blanking time settlement is done according to the following expression:

$$T_{ON-MIN} = 12 \ \ 10^{-12} \ R_{TON} \quad (1)$$

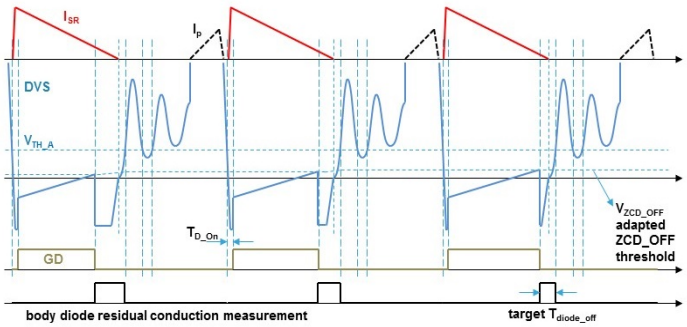
(with R_{TON} expressed in ohm and T_{ON_MIN} in seconds, starting when the DVS signal goes below V_{TH_A}). This blanking time of course sets a minimum turn-on time of the SR MOSFET as well: hence, when by reducing the load the SR MOSFET conduction time would become shorter than the programmed blanking time, the IC must stop driving the SR MOSFET to avoid current inversion (see Section 6.7 Low consumption mode operation: sleep mode and burst mode).

6.4 Adaptive turn-off and timer

The SR MOSFET can be turned off through two coexisting mechanisms (whichever triggers first); the first based on an adaptive algorithm, the second on the internal timer.

The adaptive turn-off consists of a ZCD_OFF comparator, where the DVS signal is compared to an adapting threshold. This threshold is adapted in such a way that, at steady state, the measured residual conduction time of the SR MOSFET body diode after turn-off meets the target value T_{diode_off} (as shown in Figure 8). The residual conduction time of the body diode is measured between the falling edge of the driving signal and the rising edge of the DVS signal (first time surpassing the threshold V_{TH_A}).

Figure 8. ZCD_OFF threshold adapting for body diode target conduction



The internal timer basically turns off the SR MOSFET with a fixed anticipation time T_{ant_timer} with respect to the first rising edge of the DVS signal. The IC has two different timer operating modes, selectable by the user, optimized for fixed frequency mixed CCM/DCM converters or for QR/DCM applications. The selection of the proper timer mode is done through a 100 pF capacitor across the TON pin: if it is present, mixed CCM/DCM operation is assumed; if the capacitor is not present, QR/DCM operation is assumed.

Here below the various operating modes are described.

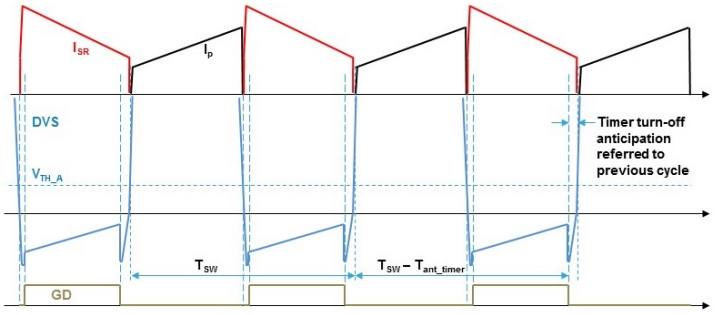
Fixed frequency mixed DCM/CCM operation:

In fixed frequency operation, the SR MOSFET turn-off is triggered by ZCD_OFF adaptive mechanism at load levels where DCM operation occurs, while it is triggered by timer at higher loads, where CCM operation occurs. The latter consists in turning off the SR MOSFET with a fixed anticipation time T_{ant_timer} with respect to the first rising edge of the DVS signal, basing on a switching period T_{SW} estimate, (over few previous cycles) as illustrated in Figure 9.

Turn-off by timer may take over also during low-to-high load transients, where the ZCD_OFF comparator threshold is in the adapting phase (close to the zero crossing and could not turn-off per time), preventing undesired current inversions.

Most of the flyback controllers available on the market, in order to help optimize the EMI filter, use operating frequency modulation. For correct operation of the SRK1000/A/B timer, the maximum rate of change of modulated frequency must be limited, so that the switching period increase from current to next cycle results much shorter than the timer anticipation T_{ant_timer} (14 ns maximum). In fact, the timer anticipation adapting during switching period increase is limited to T_{timer_step} every 4 cycles and with a switching period increase longer than 14 ns from one cycle to the next, the timer turn-off would progressively anticipate (increasing the body diode conduction).

Figure 9. Timer anticipation for fixed frequency CCM operation (100 pF mounted on TON pin)



QR operation (with valley skipping):

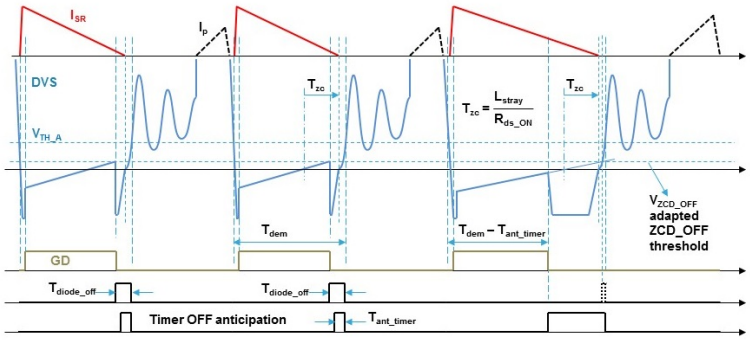
In QR flyback application the circuit works at variable frequency and, after transformer demagnetization, a resonance occurs due to primary inductance and total parasitic capacitance across primary switch. In this case, at steady state, SR MOSFET turn-off is triggered by ZCD_OFF adaptive mechanism.

During load transitions or during CC regulation operation (where output voltage may decrease), turn-off by adaptive ZCD_OFF comparator would be too late (since the threshold needs to adapt to the new slope of current flowing into the SR MOSFET), while turn-off by internal timer prevents current inversion.

The timer for fixed frequency CCM is not suitable in QR operation (that inherently operates at variable frequency). In this case, the timer operating mode consists in turning off the SR MOSFET with a fixed anticipation time T_{ant_timer} with respect to the first rising edge of the DVS signal, based on the duration of the previous demagnetization time of transformer T_{dem}, as shown in Figure 10.

Looking at the image in Figure 10, during the first two switching cycles (steady state operation) the turn-off is triggered by the ZCD_OFF comparator. This is because the DVS signal reaches the adapted ZCD_OFF threshold before the timer OFF event (since target diode T_{diode_off} is larger than timer anticipation T_{ant_timer}). In the third switching cycle, as a consequence of the transient, the turn-off is instead triggered by the timer, since current slope has decreased and the ZCD_OFF threshold would be reached too late. In the following cycle (not shown in the figure) the timer settles the anticipation to the duration of the demagnetization period of the third cycle.

Figure 10. Timer anticipation for QR operating circuit (no capacitor mounted on TON pin)



Fixed frequency DCM operation:

In fixed frequency circuits designed to operate always in DCM in all line and load conditions, the SRK1000/A/B operate basically like in the case of QR operation: the turn-off is accomplished by adaptive mechanism in steady state operation, while timer turn-off is invoked to protect against current inversion during load transitions and in CC regulation. In this case, the timer mode can be either the one for FF CCM or the one for QR application; the preferred one is the latter, as it is less expensive (no capacitor on the TON pin is required).

6.5 Minimum TOFF

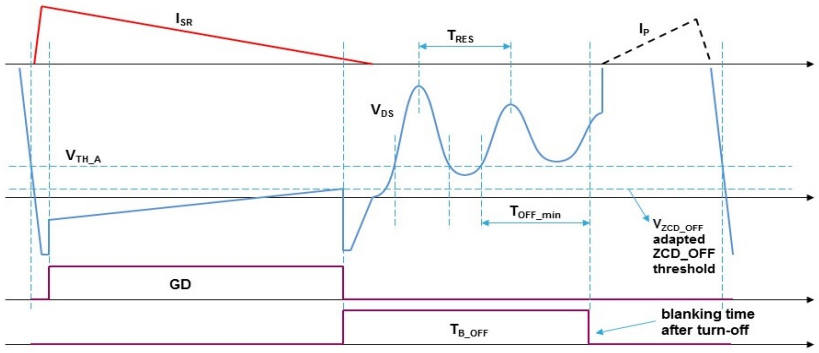
In flyback applications operating in DCM and QR with valley skipping, a resonance takes place across transformer windings after demagnetization, whose period T_{RES} depends on the transformer primary inductance and on the total capacitance across primary switch.

In order to avoid this ringing affecting SRK1000/A/B internal timings, an internally fixed blanking time (T_{OFF_MIN}) after turn-off is provided.

Referring to Figure 11, the circuit provides a blanking time from the falling edge of the driving signal to the time instant occurring after the DVS pin voltage, (V_{DS}) is permanently higher than V_{TH_A} for T_{OFF_MIN}.

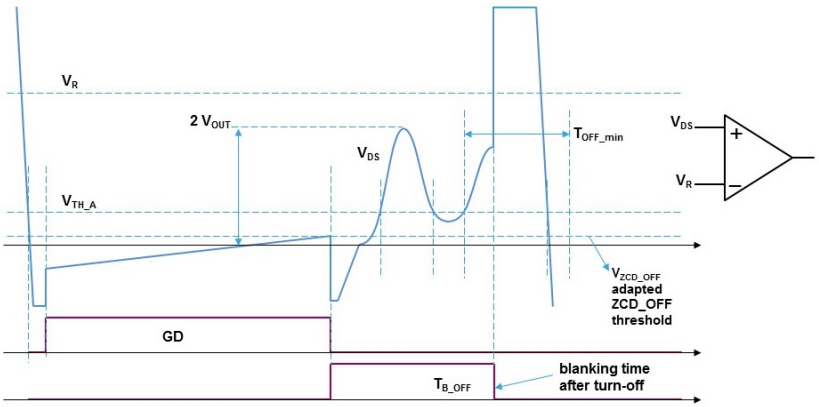
The device allows for three different choices of blanking after turn-off, according to the selected option (SRK1000, SRK1000A and SRK1000B): for correct operation, the user must select the device option with $T_{OFF\_min} > T_{RES}$ (the ringing period).

Figure 11. Blanking time after turn-off



Furthermore, referring to Figure 12, an internal comparator referenced to a voltage V_R higher than 2 V_{OUT} senses the DVS pin voltage (where V_R and V_{DS} are conveniently scaled). When the V_{DS} voltage gets higher than V_R, the comparator triggers and the blanking time is terminated. This helps during constant voltage regulation operation, at high input voltage levels (where typically the conduction time of the primary MOSFET is short), avoiding that the blanking time determined by T_{OFF_min} might delay the SR MOSFET turn-on. The internal threshold V_R is fixed to 2.83 V_{CC} (where V_{CC} equals V_{OUT} or V_{OUT-VF}, depending on whether VAUX functionality is used or not; see Section 6.8 VAUX pin operation in CC regulation).

Figure 12. Comparator for blanking time termination



6.6 Start-up phase

At converter startup, after the VCC pin voltage has surpassed the turn-on threshold V_{CC_On}, the SRK1000/A/B enter the pinstrap phase (lasting 5 switching cycles), where it checks whether a 100 pF capacitor is present on the TON pin or not and internally stores this information as long as V_{CC} voltage stays above the turn-off threshold V_{CC_Off}. After pinstrap, the SRK1000/A/B enter sleep-mode state and, when it detects that the demagnetization time is longer than the programmed sleep-mode exiting threshold (see Section 6.7 Low consumption mode operation: sleep mode and burst mode below), finally it enters run mode and starts adapting the turn-off (with the ZCD comparator threshold starting from the minimum level $V_{ZCD\_OFF\_MIN}$).

6.7 Low consumption mode operation: sleep mode and burst mode

By progressively reducing the load, SR MOSFET conduction time (the transformer demagnetization time) decreases as well: when the conduction time approaches the programmed minimum T_{ON}, the IC stops switching, reduces its consumption and enters automatic sleep-mode state. The SR MOSFET conduction time to enter sleep mode (measured between the falling and the rising edge of the DVS signal across V_{TH_A}) is:

$$T_{ON\_sleep\ in} = T_{ON\_MIN} + 300\ ns \quad (2)$$

The IC resumes operation when the load is increased and the conduction time of the SR MOSFET body diode becomes a fixed amount longer than the programmed minimum T_{ON}:

$$T_{ON\_sleep\ out} = 1.2\ T_{ON\_MIN} + 300\ ns \quad (3)$$

Both $T_{ON\_sleep\_in}$ and $T_{ON\_sleep\_out}$ are measured from the time instant when the DVS signal falls below V_{TH_A} and the time instant when it rises above V_{TH_A} the first time. The device, once the condition is detected, only takes one cycle to enter/exit sleep-mode operation.

The controller enters low consumption mode also when it detects primary controller burstmode operation, that is, when a switching stop occurs for more than T_{stop} (i.e. V_{DS} is sensed higher than V_{TH_A} for more than T_{stop}). On converter operation resuming, the SRK1000/A/B sleep-out transition takes place after the first negative going edge of the DVS voltage (falling below the threshold V_{TH_A}): in this first cycle, the gate driving is skipped; in the next cycle, the driving signal width equals the programmed minimum T_{ON}.

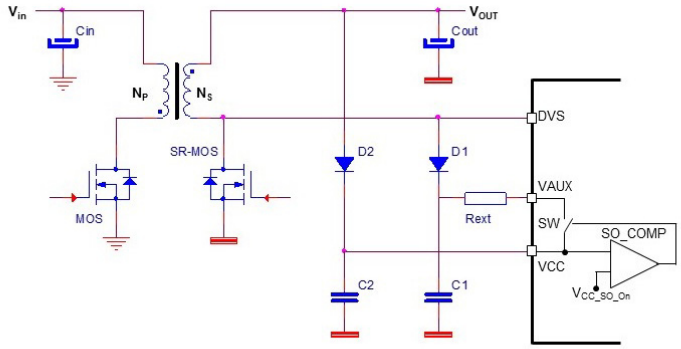
It may happen that the SRK1000/A/B enter sleep mode first and then (after further load reduction) it detects primary controller burst-mode operation: in this case, when primary side switching operation restarts, the SRK1000/A/B resume SR MOSFET driving after it detects the body diode conduction time is larger than the sleep out value $T_{ON\_sleep\_out}$ for one cycle.

6.8 VAUX pin operation in CC regulation

In charger applications operating in CC regulation, the output voltage V_{OUT} (which is also used to supply the SRK1000/A/B) may considerably decrease while output current is kept constant at progressively reduced load impedance. For example, a 10 W charger, set at +5 V output in CV regulation, may be required to operate down to 2 V output while it is regulating the output current to somewhat more than 2 A in CC regulation.

In order to guarantee SR MOSFET switching even with low V_{CC} supply voltage, the SRK1000/A/B are provided with the VAUX pin. Referring to the schematic in Figure 13, when the V_{CC} voltage decreases below the threshold $V_{CC\_SO\_On}$ (> V_{CC_Off}), an internal switch is turned on allowing the capacitor C2 placed on the VCC pin to be charged up to the turn-on threshold V_{CC_On} by a current drawn through the VAUX pin.

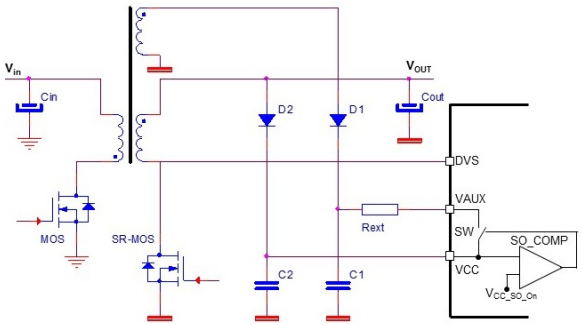
Figure 13. VAUX supply for CC regulation operation (from rectified SR MOSFET drain)



The VAUX pin may be connected, for example, to the rectified SR MOSFET drain voltage, like in Figure 13 or to another auxiliary voltage of the flyback transformer as shown in Figure 14.

In either case, a (Schottky) decoupling diode (D2) is necessary to avoid the VAUX pin charging the output capacitor. An external resistor R_{ext} may be used in series to the VAUX pin in order to dissipate externally some power amount that, without that resistor, would be totally dissipated inside the SRK1000/A/B.

Figure 14. VAUX supply for CC regulation operation from auxiliary winding



Considering the circuit in Figure 13, the following exemplification is provided to calculate the value of R_{ext} resistor and power dissipation, in the case of a +5 V charger with operation down to 2 V in CC regulation and transformer secondary-to-primary reflected voltage of 75V:

- a) Measure or estimate the IC current consumption during CC regulation operation as below:
  - $I_{CC} = I_{q\_run} + V_{CC\_avg}\ C_{iss}\ F_{sw}$ = 0.7 mA + 4.1 V 5 nF 50 kHz = 1.725 mA

    where I_q is the IC quiescent current, V_{CC_avg} is the average voltage across the VCC pin (mean value between V_{CC_On} and $V_{CC\_SO\_On}$), C_{iss} is the SR MOSFET input capacitance and F_{sw} is the operating frequency.

- b) Calculate the maximum and minimum voltage available at the VAUX pin:
  - $V_{AUX\_min} = V_{o.CC} + V_{in.min}$ (NS/NP) - V_F= 2 V + 75 V (1/15) - 0.35 V = 6.65 V

    $V_{AUX\_max} = V_{o.CC} + V_{in.max}$ (NS/NP) - V_F= 2 V + 375 V (1/15) - 0.35 V = 26.65 v

    where $V_{o.CC}$ is the output voltage in CC regulation, $V_{in.min}$/ $V_{in.maxis}$ the converter minimum/maximum input DC voltage, N_S/N_P is the transformer turn ratio, and VF is the voltage drop of D1.

- c) Calculate the power dissipation of the SRK1000/A/B, including device consumption and driving:
  - $P_{d\_CC} = V_{CC\_avg}\ I_{CC}$ = 4.1 V 1.725 mA = 7.072 mW

    where V_{CC_avg} is the mean value between V_{CC_On} and $V_{CC\_SO\_On}$.

- d) Calculate the maximum external resistance in series to the VAUX pin:
  - $R_{ext\_MAX} = (V_{AUX\_min} - V_{CC\_On}) / I_{CC} - R_{on}$ = (6.65 V - 4.3 V) / 1.725 mA - 40 Ω = 1.322 kΩ

    => R_{ext} = 1.2kΩ Rtot = Rext + Ron = 1.2 kΩ +40 Ω = 1.24 kΩ

    where R_{on} is the resistance of the internal VAUX switch.

- e) Calculate the maximum and minimum current from the VAUX pin:
  - $I_{AUX\_min} = (V_{AUX\_min} - V_{CC\_On}) / R_{tot}$ = (6.65 V - 4.3 V) / 1.24 kΩ = 1.89 mA

    $I_{AUX\_max} = (V_{AUX\_max} - V_{CC\_On}) / R_{tot}$ = (26.65 V - 4.3 V) / 1.24 kΩ = 18.02 mA

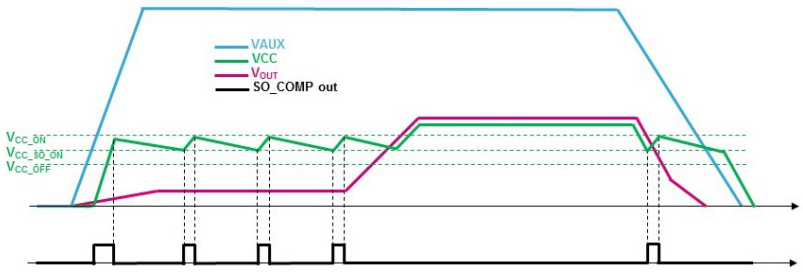
- f) Calculate the maximum power dissipation from VAUX at maximum input voltage ($V_{in.max}$):
  - $P_{d\_AUX} = V_{AUX\_max}\ I_{CC}$ = 26.65 V 1.725 mA = 45.971 mW

- g) Calculate the maximum power dissipation on external resistance and inside SRK1000/A/B:
  - $P_{d\_Rext} = (P_{d\_AUX} - P_{d\_CC})\ R_{ext} / R_{tot}$ = (45.971 mW -7.072 mW) 1.2 kΩ / 1.24 kΩ = 37.64 mW

    $P_{d\_SRK} = P_{d\_AUX} - P_{d\_Rext}$ = 45.971 mW - 37.64 mW = 8.33 mW

The Figure 15 shows VAUX pin operation during the various circuit phases (start- up phase, CC-CV regulation and mains turn-off).

Figure 15. VAUX pin operation



6.9 Operation in CC regulation and short-circuit

During CC regulation operation in QR applications, the demagnetization time progressively increases while reducing the load impedance and the output voltage consequently reduces. Therefore, the conduction duty cycle of SR MOSFET driving increases: the SRK1000/A/B fix the maximum driving pulse width level to T_{ON_MAX} and after this time interval has elapsed, it turns off the SR MOSFET. This means that, for the rest of the demagnetization time after T_{ON_MAX}, the rectified current continues to flow through the body diode.

If CC regulation is extended down to short-circuit condition, (i.e. the output current is regulated also during short-circuit and the primary controller does not enter hiccup protection), some care must be taken to avoid temperature increase of the SR MOSFET (i.e. a proper thermal design or the usage of an external Schottky diode).

6.10 Adaptive gate drive

The IC is provided with a low-noise, high-current gate-drive output, capable of directly driving N-channel Power MOSFETs.

The high-level voltage provided by the driver is in fact clamped at $V_{GDclamp}$ (11.6 V typ.) through an accurate circuitry; this avoids excessive voltage levels on the gate in case the device is supplied with a high V_{CC}, thus minimizing the gate charge provided in each switching cycle.

Furthermore, the gate driver has a pull-down capability that ensures the SR MOSFET cannotbe spuriously turned on even at low V_{CC}: in fact, the driver has a 1 V (typ.) saturation level at V_{CC} below the turn-on threshold.

In order to optimize efficiency at low load levels (where driving losses may be relevant with respect to conduction losses), the high-level of driver output is adapted, decreasing with decreasing demagnetization time. The adaptive gate drive changes the driving high-level V_{HIGH} n 16 steps of 400 mV, corresponding to 16 steps of detected demagnetization time T_D of the transformer, as described by the following relationships:

$$T_D = 300\ ns + T_{ON\_min}(n + 6)/6 \quad (4)$$

where $V_{GD\_ad\_step}$ is the voltage step and n (= 1 to 16) is the step number.

The voltage step increase/decrease is done after the demagnetization time interval T_D has been detected increasing/decreasing by one step for 32 cycles consecutively.

The driver voltage level V_{HIGH} is of course limited by the supply voltage on the VCC pin and, in any case, when V_{CC} voltage supply is detected lower than a threshold, the driver high- level modulation is disabled. A comparator with hysteresis enables adaptive drive when V_{CC} supply increases above $V_{CC\_AGD\_en}$ and disables it as V_{CC} goes below $V_{CC\_AGD\_dis}$.

This means that, if the V_{CC} supply is low (but higher than $V_{CC\_AGD\_dis}$), the driver high-level V_{HIGH} is the minimum between the value of above formula and a value equal to:

- -V_{CC} supply → if VAUX function is used (and VAUX pin voltage is larger than V_{CC} - 1.2 V).
- or to V_{CC}-1.2 V → if VAUX function is not used; in which case the VAUX pin has to be connected to the V_{CC} pin.

The adaptive gate drive is disabled also when the circuit enters burst-mode operation: at resuming operation from burst mode, the gate drive always starts from the highest voltage level; then it continues progressively adapting it according to the sensed demagnetization period.

In the case of sleep mode, the behavior is different: when the load (after entering sleep mode) increases and the SRK1000/A/B resume switching operation, the gate drive starts from lower level and then it progressively adapts with step $V_{GD\_ad\_step}$ according to the sensed demagnetization period.

It is worth noting that, generally speaking, an SR MOSFET is always switched on after current starts flowing through its body diode, when the drain-source voltage is already low (equal to V_F); therefore, there is no Miller effect nor switching losses at MOSFET turn-on. This is true also at turn-off, since rectifier current, after SR MOSFET is switched off, continues flowing into the body diode. Consequently, the required gate charge the driver must provide each cycle for ON-OFF switching is rather lower than in the case of hard switching and can be easily found/estimated from the MOSFET datasheet in order to calculate the driver power dissipation.

7 Layout guidelines

The GND pin is the return of the bias current of the device and return for gate drive current: it should be routed in the shortest way possible to the common point where the source terminal of the SR MOSFET and output capacitor negative terminal are connected. When laying out the PCB, care must be taken to keep the source terminal of the SR MOSFET as close to output capacitor negative terminal as possible.

DVS connection to SR MOSFET drain terminal is not critical (since adaptive turn-off algorithm automatically compensates for stray inductances in the SR MOSFET current path); nevertheless, it should be preferred to sense the MOSFET voltage as close to its drain terminal as possible.

The usage of bypass capacitors between the VCC pin and GND pin is recommended. They should be low-ESR, low-ESL type and located as close to the IC pins as possible.

Sometimes, a series resistor (in the tens ohm) between the converter's output voltage and the VCC pin, forming an RC filter along with the bypass capacitor, is useful to obtain a cleaner V_{CC} voltage.

Since theTON pin sourced current is relatively low, this pin may be affected by current injections coming from close tracks with high dV/dt (i.e. drain sense signals); therefore, the TON pin should be kept away from SR MOSFET drain tracks, with a proper layout.

In case of large noise, a capacitor can be used on TON pin for filtering; since it is also used for internal timer setting according to user selected operation (quasi-resonant or fixed frequency), the allowed capacitance C_{ON} is as follows:

max 22pF	➡	for quasi-resonant operation
min 100pF and time constant R_{ON} C_{ON} < 100 µs	➡	for fixed frequency operation

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 SOT23-6L package information

Table 5. SOT23-6L mechanical data

Symbol	Milimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.90		1.45	0.035		0.057
A1	0.00		0.15	0.000		0.006
A2	0.90		1.30	0.035		0.051
b	0.30		0.50	0.012		0.020
c	0.14		0.20	0.006		0.009
D		2.90			0.114	
E		1.60			0.063	
e		0.95			0.037	
H		2.8			0.110	
L	0.30		0.60	0.012		0.022
θ (degrees)	0°		8°	0°		8°

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

Figure 16. **SOT23-6L package outline top and side view**

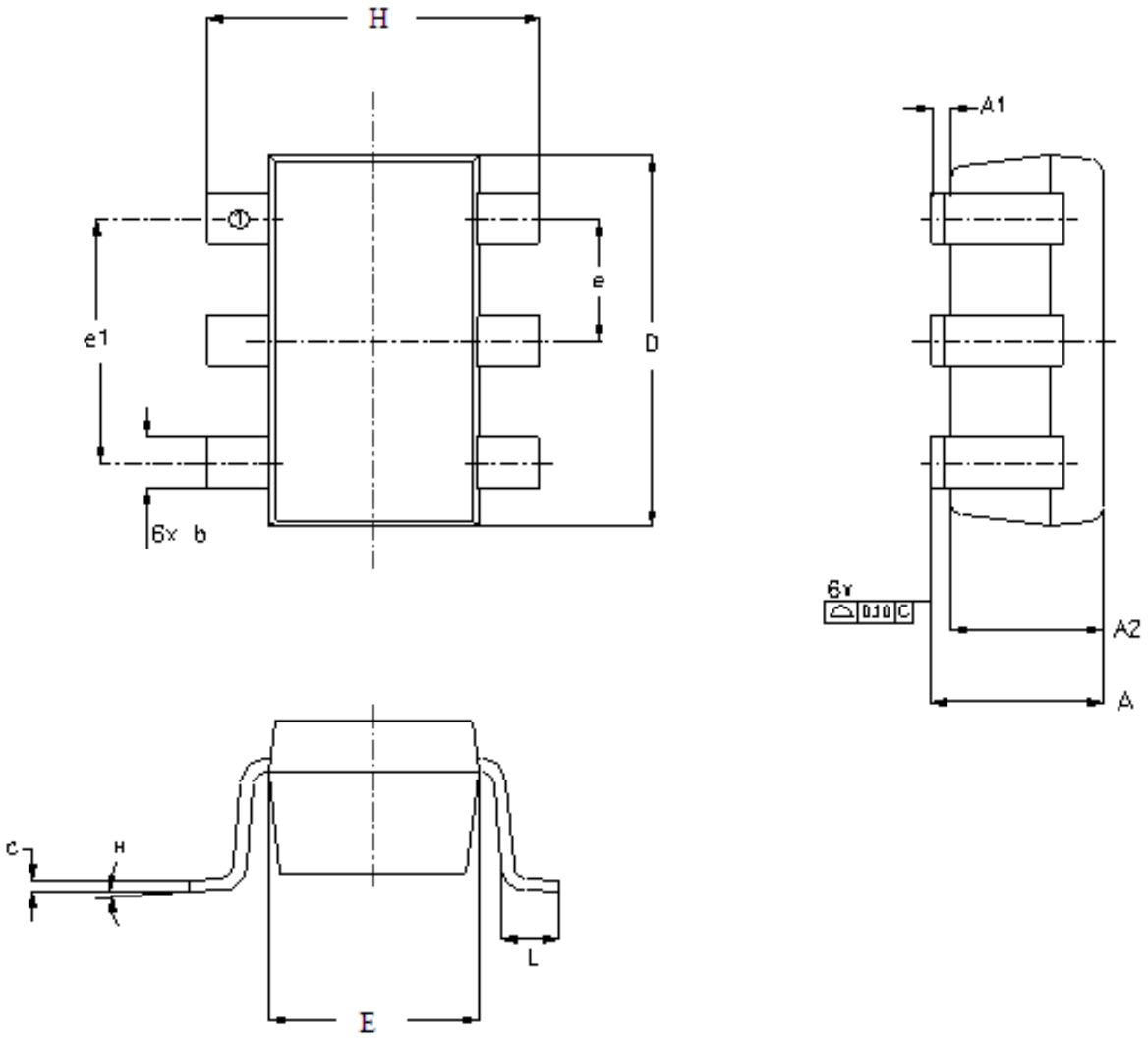
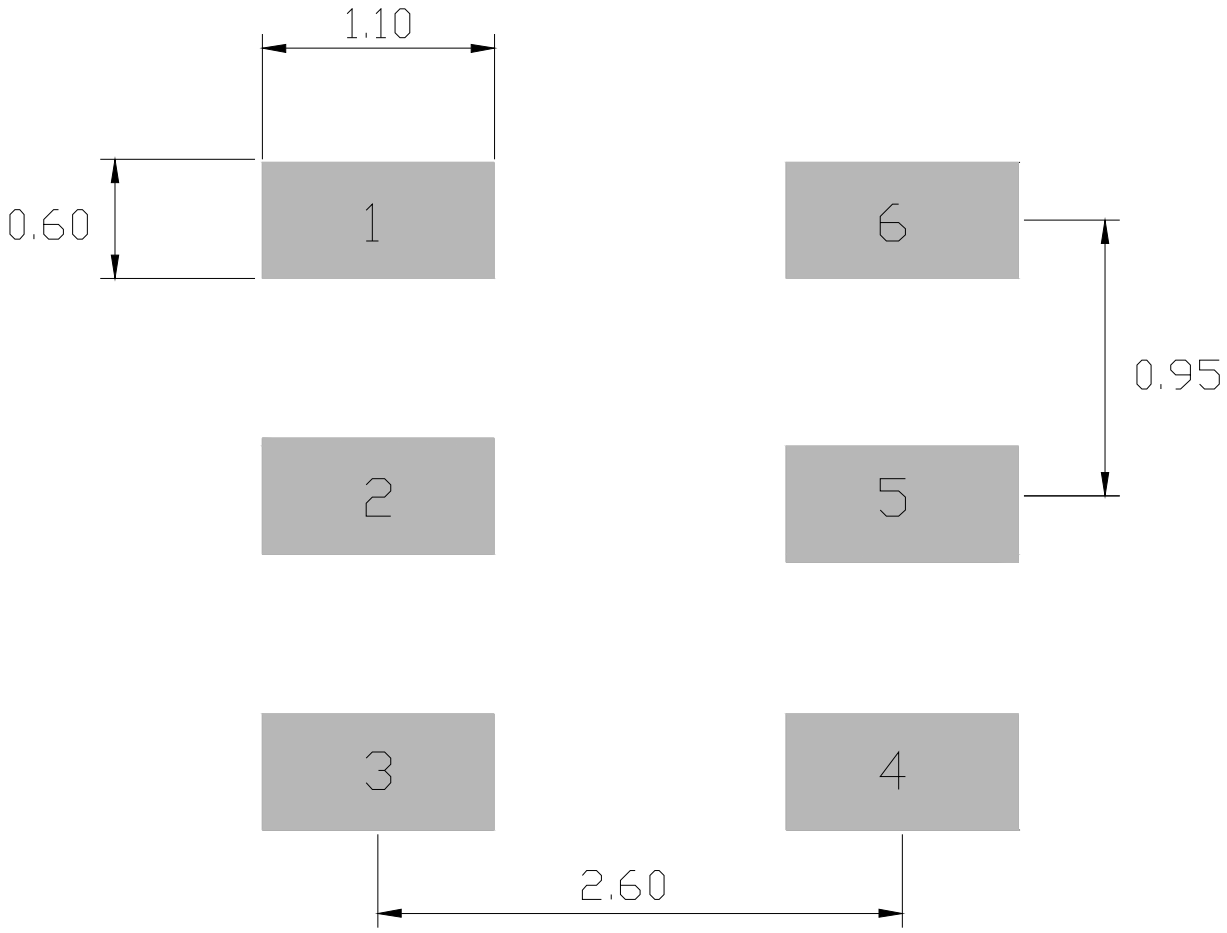


Figure 17. **SOT23-6L package outline bottom view**



Revision history

Table 6. Document revision history

Date	Version	Changes
16-Oct-2018	1	Initial release.
11-Jan-2019	2	Updated *Product summary* .
23-Jul-2019	3	Change made to Electrical characteristics table and text added to Section 7 Layout guidelines.
04-May-2020	4	SRK1000 changed to SRK1000/A/B throughout document.
19-Nov-2021	5	Table Electrical characteristics updated

Contents

List of tables

List of figures