SPECIFICATION

CUSTOMER PART NO. : XEA-055A01-DI9509-G020
PRODUCT NO. : **TCXD055MBLMT-76**
VERSION : **Ver 1.0**
ISSUED DATE : **2022-12-05**

This module uses ROHS material

FOR CUSTOMER： _____
□：APPROVAL FOR SPECIFICATION
■：APPROVAL FOR SAMPLE

DATE	APPROVED BY

Xinli Optoelectronics ：

Presented by	Reviewed by	Organized by
宋鈺龍	趙春曉	王俊傑

Note:

1.Xinli Optronics reserves the right to make changes without further notice to any products herein to improve reliability, function or design.

1. Record of Revision

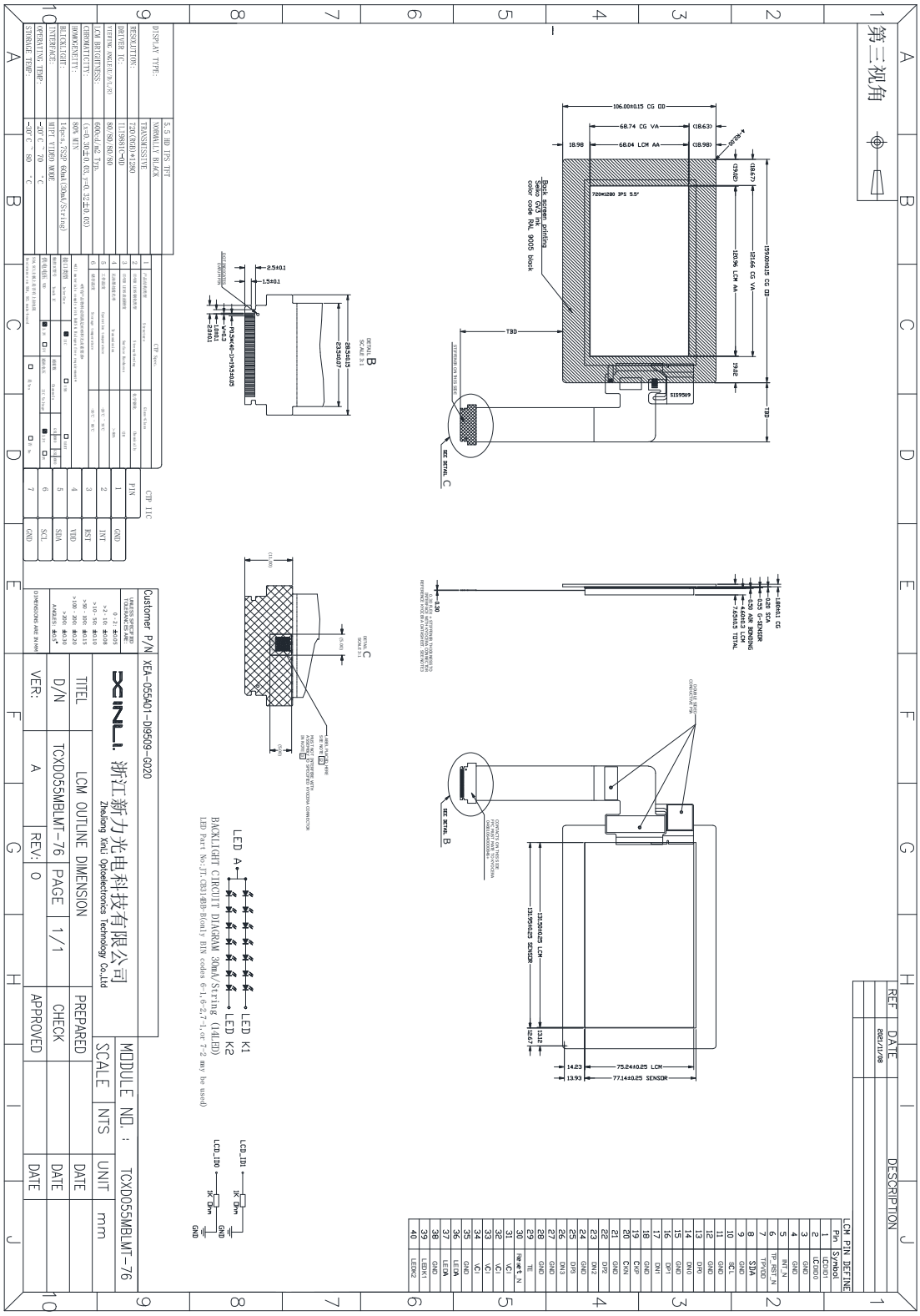
Revision	Description	Date
1.0	Initial Release	2022/12/05

2. General Description and Features

The 5.5 inch Module named TCXD055MBLMT-76 is a-Si TFT-LCD module, which is the type of transmissive. It is consisted of TFT-LCD Panel, one Driver IC, FPC, one Back-Light and one Touch Panel unit. Features of this product are listed in the following table.

NO	Item	Contents	Unit
(1)	Module Outline	159(H)*106(V)*7.65(T)	mm
(2)	LCD Active area	68.04(H)*120.96(V)	mm
(3)	Dot Number	720 RGB*1280	/
(4)	Dot size	0.0945*0.0945	mm
(5)	LCD type	TFT Transmissive	/
(6)	Display Color	16.7M	/
(7)	Viewing direction	Free	/
(8)	Backlight Type	14 Chip-White LEDs	/
(9)	Power Supply	3.3(TYP)	V
(10)	Drive IC	ILI9881C-0D	/
(11)	Interface	FPC 0. 5mm_Pitch 40pin	/
(12)	Interface type	MIPI interface	/
(13)	Module weight	TBD	g

3. Mechanical Dimension



4.Interface Pin Connection

Connectors required:046810640000846+(Kyocera),
specifications:https://www.mouser.com/datasheet/2/909/6810-1602176.pdf
LCM interface Pin:

No.	Symbol	I/O Properties	I/O	Function
1	LCDID1	/	O	LCDID configuration interface , Internal connect 1K Ω resistor to GND.
2	LCDID0	/	P	Not connect（DNP)
3	GND	/	P	Ground
4	GND	/	P	Ground
5	INT_N	Open Drain	O	TP Indicate coordinate ready
6	TP_RST_N	Connect 10K resistor to TPVDD Connect 1uF capacitor to GND	I	TP Reset Pin
7	TPVDD	/	P	TP Power Supply
8	SDA	Open Drain (no pullup resistor included)	I/O	TP I2C:serial data
9	GND	/	P	Ground
10	SCL	Open Drain (no pullup resistor included)	I	TP I2C:serial clock
11	GND	/	P	Ground
12	GND	/	P	Ground
13	DP0	/	I/O	MIPI data Input
14	DN0	/	I/O	MIPI data Input
15	GND	/	P	Ground
16	DP1	/	I	MIPI data Input
17	DN1	/	I	MIPI data Input
18	GND	/	P	Ground
19	CKP	/	I	MIPI clock Input
20	CKN	/	I	MIPI clock Input
21	GND	/	P	Ground
22	DP2	/	I	MIPI data Input
23	DN2	/	I	MIPI data Input

24	GND	/	P	Ground
25	DP3	/	I	MIPI data Input
26	DN3	/	I	MIPI data Input
27	GND	/	P	Ground
28	GND	/	P	Ground
29	TE	/	O	Tearing Effect pin
30	RESET_N	Connect 10K resistor to VCI Connect 1uF capacitor to GND	I	LCD Reset pin
31	VCI	/	P	A power supply for analog circuit
32	VCI	/	P	A power supply for analog circuit
33	VCI	/	P	A power supply for analog circuit
34	VCI	/	P	A power supply for analog circuit
35	GND	/	P	Ground
36	LEDA	/	P	Led anode
37	LEDA	/	P	Led anode
38	GND	/	P	Ground
39	LEDK1	/	P	Led cathode
40	LEDK2	/	P	Led cathode

5. Maximum Rating

Item	Symbol	Rating	Unit
Operating temperature	Top	-20 to 70	℃
Storage temperature	Tst	-30 to 80	℃
Power supply for analog circuit	VCI	-0.3~ 7.0	V

6. Electrical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply for analog circuit		VCI	-	2.5	2.8	6.6	V
Logic input signal Voltage	H level	V_{IH1}	-	0.7*VCI	-	VCI	V
	L level	V_{IL1}		-0.3	-	0.3*VCI	V

7. Backlight Characteristics

Item	syb	Min	Typ	Max	Unit	Condition
Voltage（LED A）	Vf	18.9	21	23.1	V	IF=60mA(30mA/LED)
Luminance(module)	Lv	-	600	-	cd/m2	
Number of LED	-	14			pcs	-
LED life-span	-	(25000)	-	-	Hrs	-

LED Part No:JT.CB314BB-B.

Remarks:In order to control the voltage within the range,only BIN codes 6-1,6-2,7-1,or 7-2 may be used.

8.Timing Characteristics

8.1 AC Characteristics

8.1.1 high speed mode – clock timing

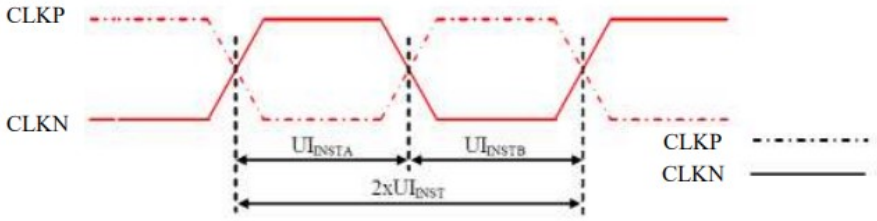


Figure 116: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

8.1.2 high speed mode – clock/data timing

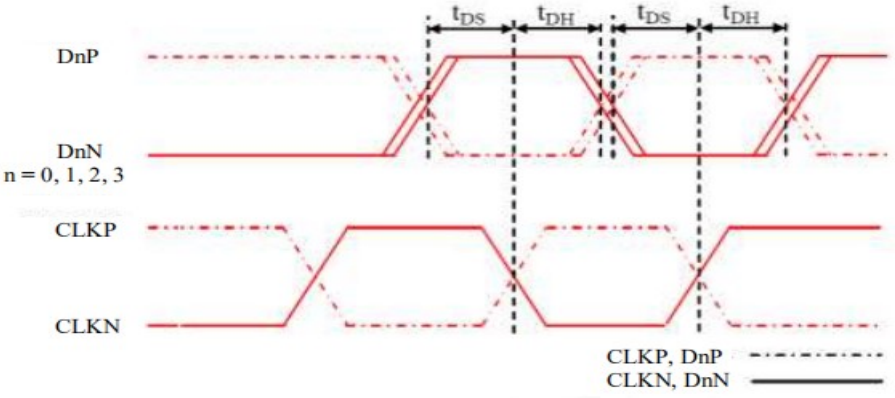


Figure 117: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

8.1.3 high speed mode – rising and falling timing

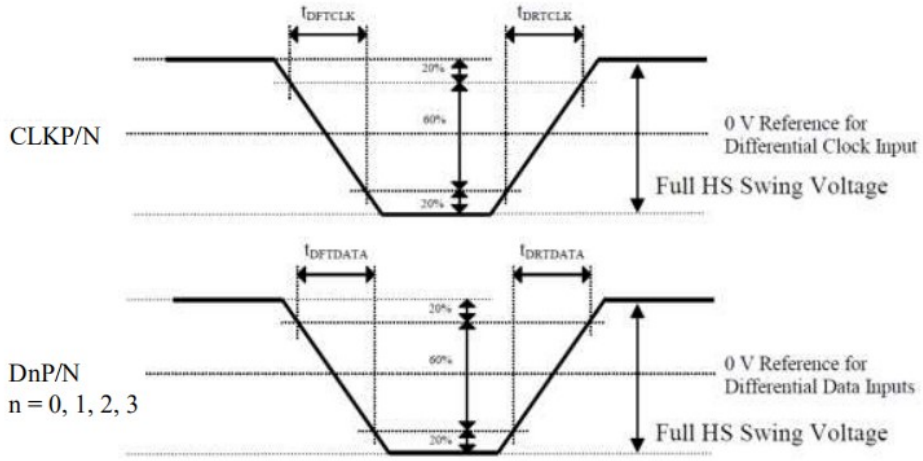


Figure 118: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

8.1.4 Low Speed Mode - Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C-0D) are illustrated for reference purposes below.

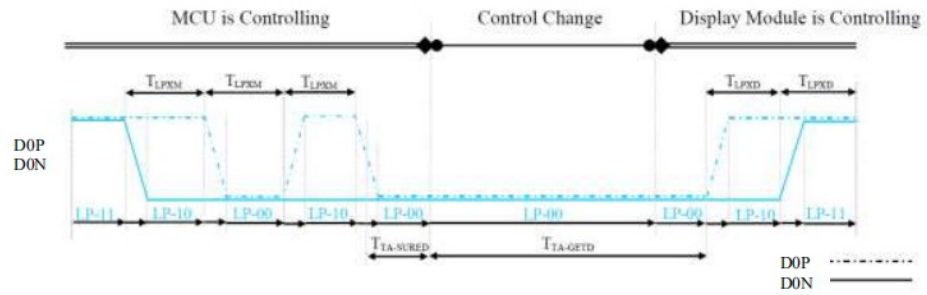


Figure 119: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C-0D) to the MCU are illustrated for reference purposes below.

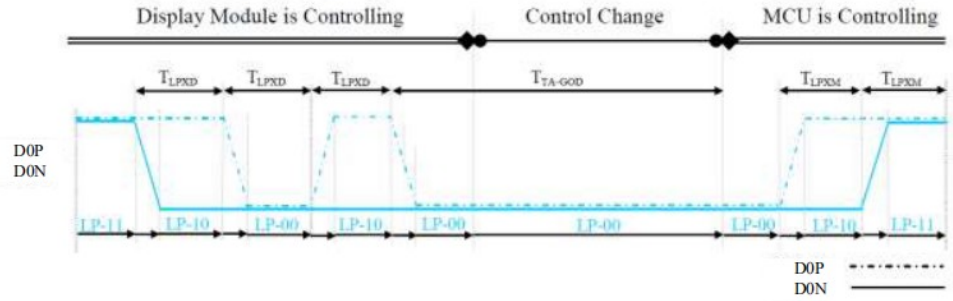


Figure 120: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881C-0D)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C-0D) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C-0D) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C-0D)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

8.1.5 Data Lanes from Low Power Mode to High Speed Mode

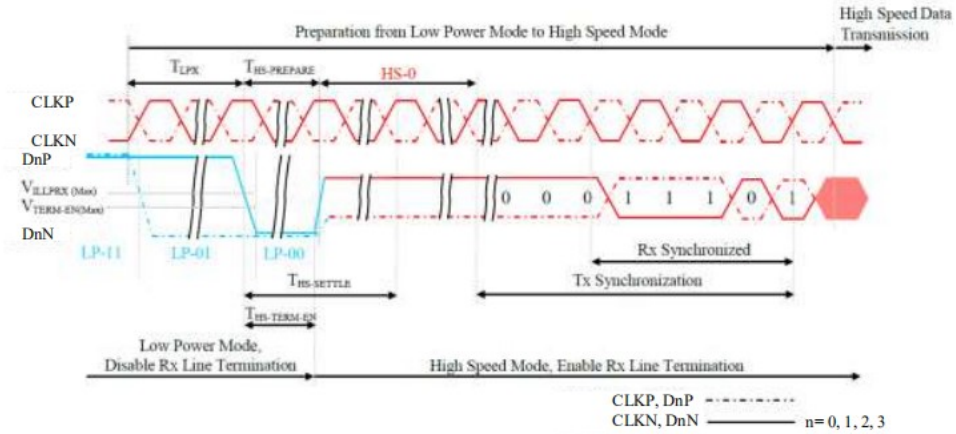


Figure 121: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

8.1.6 Data Lanes from High Speed Mode to Low Power Mode

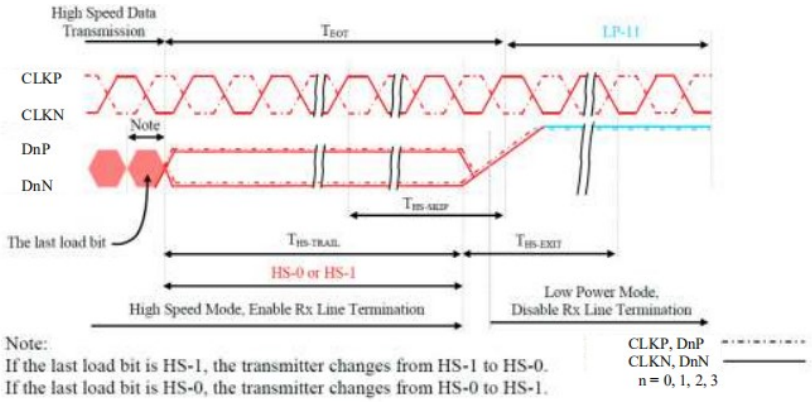


Figure 122: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C-0D) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

8.1.7 DSI Clock Burst – High speed mode to /from Low Power Mode

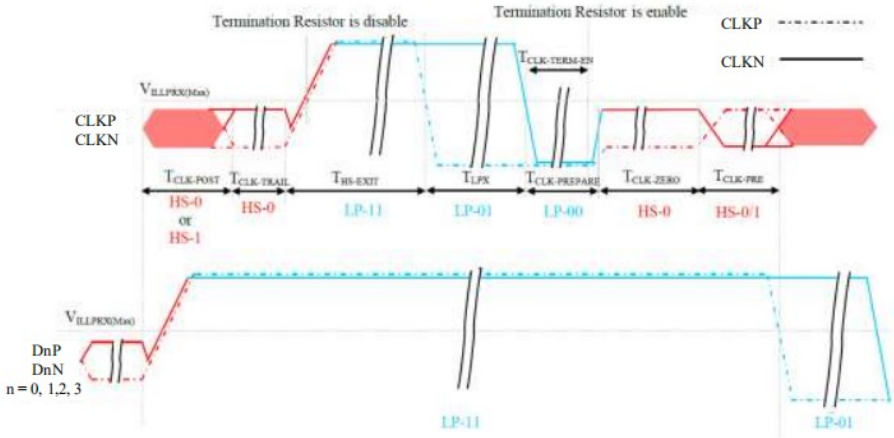
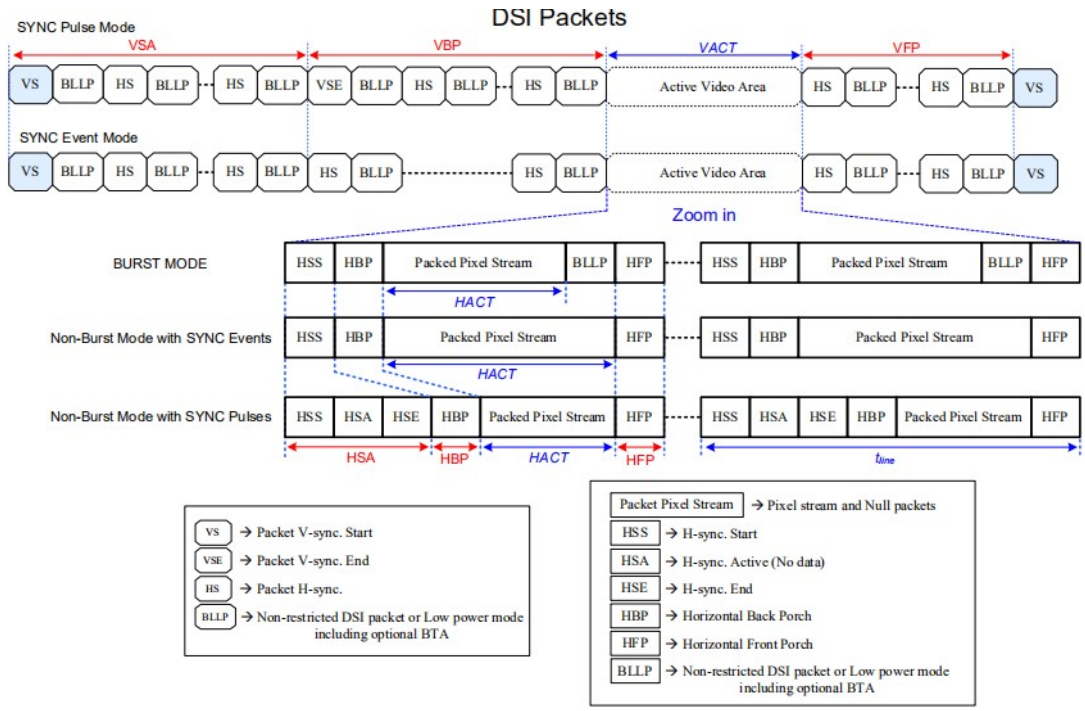


Figure 123: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

8.1.8 Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example：BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.1DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to “Table 39: Limited Clock Channel Speed”.
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

8.2 Reset timing

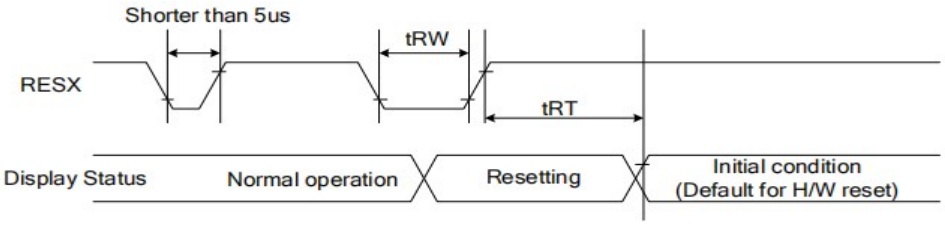


Figure 124: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

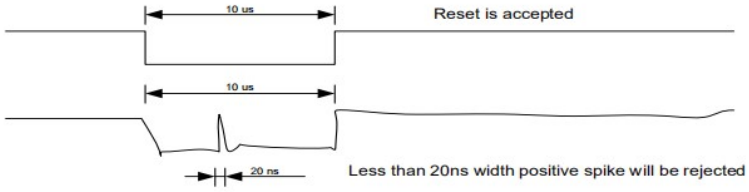


Figure 125: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

9. Initial Code

Please consult our technical department for detail information.

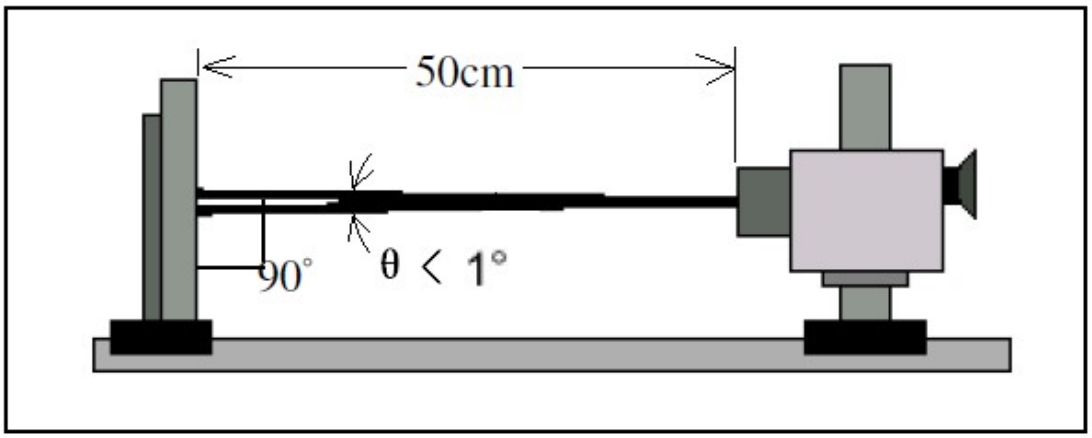
10. Electro-Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Response time	Tr+Tf	θ =0° ∅=0° Ta=25℃	-	25	40	ms	4
Uniformity （Five point）	δ WHITE		-	80	-	%	7
Contrast ratio	Cr		700	1000	-	-	3 ,5
Surface Luminance (Without CTP)	Lv		-	600	-	-	3 ,7
Viewing angle range	θ	∅ = 90°	70	80	-	deg	6
		∅ = 270°	70	80	-	deg	
		∅ = 0°	70	80	-	deg	
		∅ = 180°	70	80	-	deg	
Color chromaticity (CF only, light source is C light, CIE 1931)	R_X	θ = ϕ = 0°	TBD.	TBD.	TBD.		7
	R_Y		TBD.	TBD.	TBD.		
	G_X		TBD.	TBD.	TBD.		
	G_Y		TBD.	TBD.	TBD.		
	B_X		TBD.	TBD.	TBD.		
	B_Y		TBD.	TBD.	TBD.		
	Wx		TBD.	TBD.	TBD.		
	Wy		TBD.	TBD.	TBD.		
NTSC(CF only, light source is C light, CIE 1931)	%	CIE1931	60	70	-	%	

Note 1: Ambient temperature=25℃±2℃

Note 2: To be measured in the dark room with backlight unit.

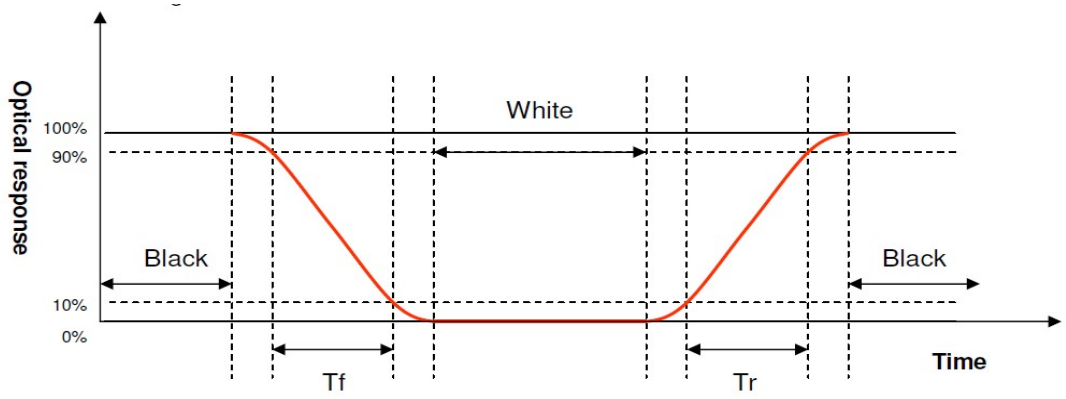
Note 3: To be measured at the center area of panel with a viewing cone of 1 by Topcon luminance meter BM-7A, after 10 minutes operation (module).



Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "black" to "white" (rising time) and from "white" to "black" (falling time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.

Refer to figure as below.



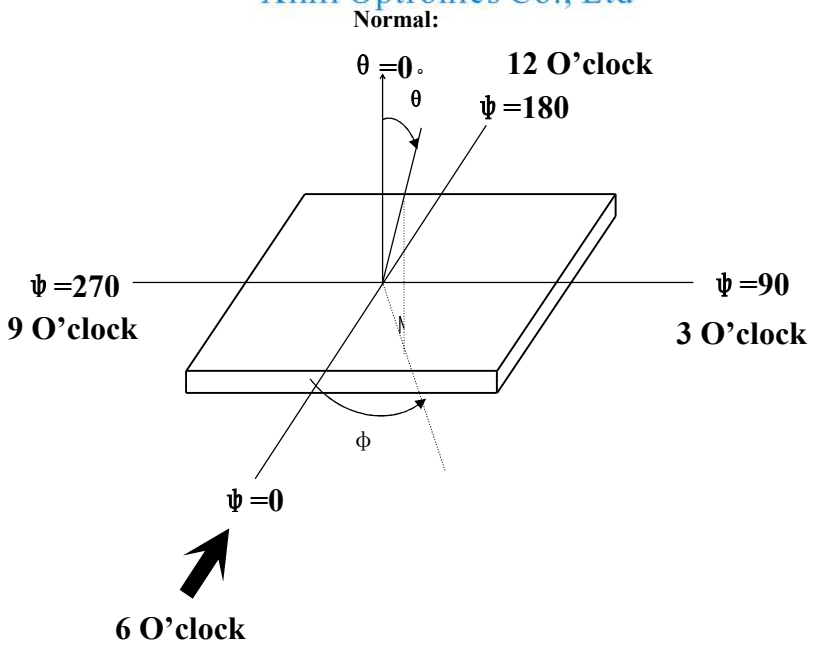
Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

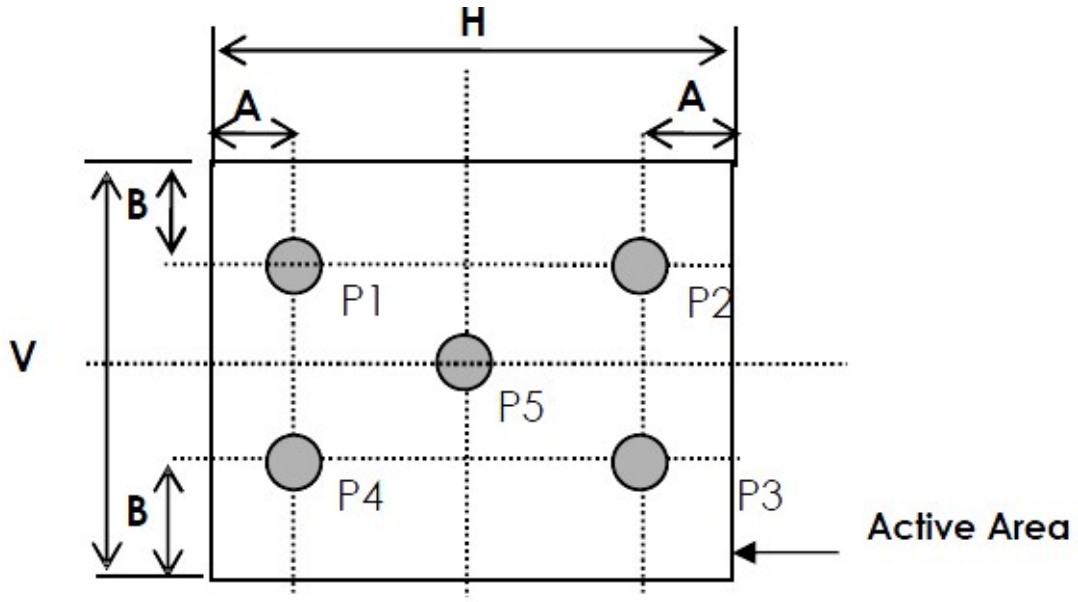
Note 6. Definition of viewing angle

Viewing angle is the angle at which the contrast ratio is greater than 10 for TFT module. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.



Note 7. Surface luminance is the LCD surface from the surface with all pixels displaying white. Refer to figure as below.

Measuring method for Contrast ratio, surface luminance, Luminance uniformity，CIE (x, y) chromaticity



A : 5 mm B : 5 mm H,V : Active Area

Light spot size Æ=7mm, 500mm distance from the LCD surface to detector lens measurement instrument is TOPCON's luminance meter BM-7A

Uniformity definition= [min of 5point/max of 5points]x100%

Lv = Surface Luminance with all white pixels (P5)

11. Quality Assurance

TBD.

12. Reliability Test

This standard reliability test is done only for the first lot of MP products.
Customer and supplier must hold a discussion if other reliability test is requested by customer.

NO.	Test Item	Description	Test Condition
1	High temperature storage	Endurance test applying the high storage temperature for a long time	80℃,240 H
2	Low temperature storage	Endurance test applying the low storage temperature for a long time	-30℃,240H
3	High temperature operation	Endurance test applying the electric stress under high temperature for a long time	70℃,240H
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time	-20℃,240H
5	High temperature /humidity storage	Endurance test applying the high temperature and high humidity storage for a long time	60℃,90% RH, 240H
6	Temperature Cycle (Non operation)	Endurance test applying the low and high temperature cycle -30℃← →25℃ ← →80℃ 30min←→5min←→30min ◄——————————► one cycle	-30℃/80℃, 100 cycles

13. Precautions for Operation and Storage

1. Precautions for Operation

(1)Since LCD panel made of glass,in order to prevent from glass broken or color tone change,please do not apply any mechanical shock or impact or excessive force to it when installing the LCD module.

(2)If LCD panel is broken and liquid crystal substance leaks out and contact your skin or clothes,please immediately wash it off by using soap and water.

(3)The polarizer on the LCD surface is soft and easily scratched.Please be careful when handling.

(4)If LCD surface becomes contaminated,please wipe it off gently by using moisten soft cloth with normal hexane,do not use acetone,ketone,ethanol, alcohol or water.If there is saliva or water on the LCD surface,please wipe it off immediately.

(5)When handing LCD module,please be sure that the body and the tools are properly grounded.And do not touch I/F pins with bare hands or contaminate I/F pins.

(6)Do not attempt to disassemble or process the LCD module.

(7)LCD module should be used under recommended operating conditions shown in chapter 6 and 7.

(8)Response time will be extremely slower at lower temperature than at specified temperature and LCD will show different color when at higher temperature.The phenomenon will disappear when returning to specified condition.

(9)Foggy dew,moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage,the deteriorated display quality and electrochemical reaction then leads to the shorter life time and permanent damage to the module probably.Please pay attention to the environmental temperature and humidity.

2.Precautions for Storage

(1)Please store LCD module in a dark place,avoid exposure to sunlight,the light of fluorescent lamp or any ultraviolet ray.

(2)Keep the environment temperature at between 10℃and 35 ℃ and at normal humidity.Avoid high temperature,high humidity or temperature below 0℃.

(3)That keeps the LCD modules stored in the container shipped from supplier before using them is recommended.

(4)Do not leave any article on the LCD module surface for an extended period of time.

3.Warranty period

Warrants for a period of 12 Months from the shipping date when stored or used under normal condition.

14.Package Specification

TBD