CeraLink™

Capacitor for fast-switching semiconductors

Series/Type:	**Low profile (LP) series**
Ordering code:	**B58031***
Date:	2016-07-28
Version:	3.0

EPCOS AG is a TDK Group Company.

Applications

- Power converters and inverters
- DC link/ snubber capacitor for power converters and inverters

Features

- High ripple current capability
- High temperature robustness
- Low equivalent serial inductance (ESL)
- Low equivalent serial resistance (ESR)
- Low power loss
- Low dielectric absorption
- Optimized for high frequencies up to several MHz
- Increasing capacitance with DC bias up to operating voltage
- High capacitance density
- Minimized dielectric loss at high temperatures
- High reliability
- Qualification based on AEC-Q200 rev. D
- Suitable for reflow soldering only

Construction

- RoHS-compatible PLZT ceramic (lead lanthanum zirconium titanate)
- Copper inner electrodes
- Silver outer electrodes
- Silver coated copper-invar lead frame
- Epoxy resin adhesive

Electrical specifications V_R = 500 V

Maximum peak operating voltage @ $V_{pk,max}$, 25 °C, 7 s	$V_{pk,max}$	**= 650 V**
Rated voltage Reference DC voltage for reliability tests	V_R	**= 500 V**
Operating voltage at maximum attenuation capability	V_{op}	**= 400 V**
Typical nominal capacitance @ V_{op}, quasistatic, 25 °C. See glossary (page 21) for definition of the nominal capacitance.	$C_{nom,typ}$	**> 1 µF**
Typical effective capacitance @ V_{op}, 0.5 V_{RMS}, 1 kHz, 25 °C	$C_{eff,typ}$	**= 0.6 µF**
Initial capacitance @ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C	C_0	**= 0.35 µF ± 20%**
Dissipation factor @ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C	tan δ	**< 0.02**
Insulation resistance @ V_{op}, t > 240 s, 25 °C	$R_{ins,typ}$	**> 1 GΩ**
Operating device temperature	T_{device}	**-40 °C... +150 °C**
Weight of device		**approx. 1.3 g**

Typical values

ESR 0 V_{DC}, 0.5 V_{RMS}, 25 °C, 1 MHz	ESR 0 V_{DC}, 0.5 V_{RMS}, 25 °C, 1 kHz	ESL	I_{op} [1)] 100 kHz T_A = 85 °C	I_{op} [1)] 100 kHz T_A = 105 °C
mΩ	**Ω**	**nH**	**A_{RMS}**	**A_{RMS}**
12	3.3	2.5	7.5	5.2

[1)] Normal operating current without forced cooling at T_{device} = 125 °C. Higher values permissible at reduced lifetime.

Ordering codes

Packaging	Packaging unit pcs.	Ordering code	Rated voltage	Terminal style
Cardboard box	100	B58031I5105M002 B58031U5105M002	500 V 500 V	L J
330-mm reel	1000	B58031I5105M062 B58031U5105M062	500 V 500 V	L J

Electrical specifications V_R = 700 V

Maximum peak operating voltage @ $V_{pk,max}$, 25 °C, 7 s	$V_{pk,max}$	**= 1000 V**
Rated voltage Reference DC voltage for reliability tests	V_R	**= 700 V**
Operating voltage at maximum attenuation capability	V_{op}	**= 600 V**
Typical nominal capacitance @ V_{op}, quasistatic, 25 °C. See glossary (page 21) for definition of the nominal capacitance.	$C_{nom,typ}$	**> 0.5 µF**
Typical effective capacitance @ V_{op}, 0.5 V_{RMS}, 1 kHz, 25 °C	$C_{eff,typ}$	**= 0.25 µF**
Initial capacitance @ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C	C_0	**= 0.14 µF ± 20%**
Dissipation factor @ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C	tan δ	**< 0.02**
Insulation resistance @ V_{op}, t > 240 s, 25 °C	$R_{ins,typ}$	**> 1 GΩ**
Operating device temperature	T_{device}	**-40 °C... +150 °C**
Weight of device		**approx. 1.3 g**

Typical values

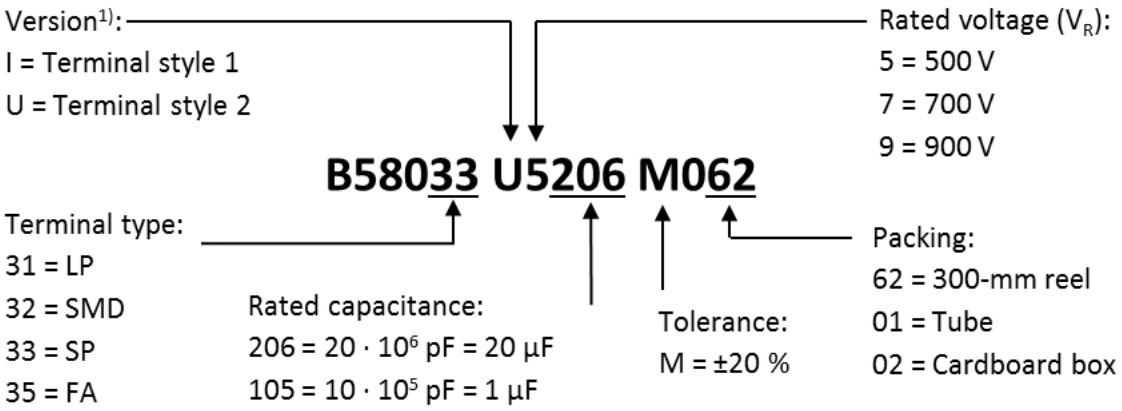
ESR 0 V_{DC}, 0.5 V_{RMS}, 25 °C, 1 MHz	**ESR** 0 V_{DC}, 0.5 V_{RMS}, 25 °C, 1 kHz	**ESL**	**I_{op}** [1)] 100 kHz T_A = 85 °C	**I_{op}** [1)] 100 kHz T_A = 105 °C
mΩ	**Ω**	**nH**	**A_{RMS}**	**A_{RMS}**
28.7	9	2.5	5.4	4.4

[1)] Normal operating current without forced cooling at T_{device} = 125 °C. Higher values permissible at reduced lifetime.

Ordering codes

Packaging	Packaging unit pcs.	Ordering code	Rated voltage	Terminal style
Cardboard box	100	B58031I7504M002	700 V	L
330-mm reel	1000	B58031I7504M062	700 V	L

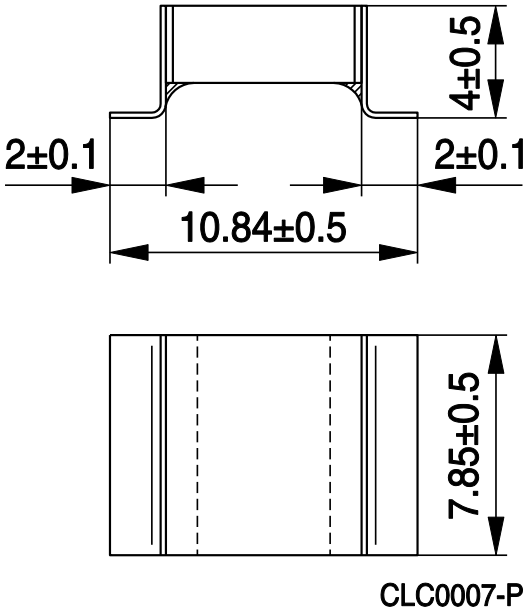
Code construction CeraLink™



1) LP series: Terminal style 1 = L-style terminal, Terminal style 2 = J-style terminal

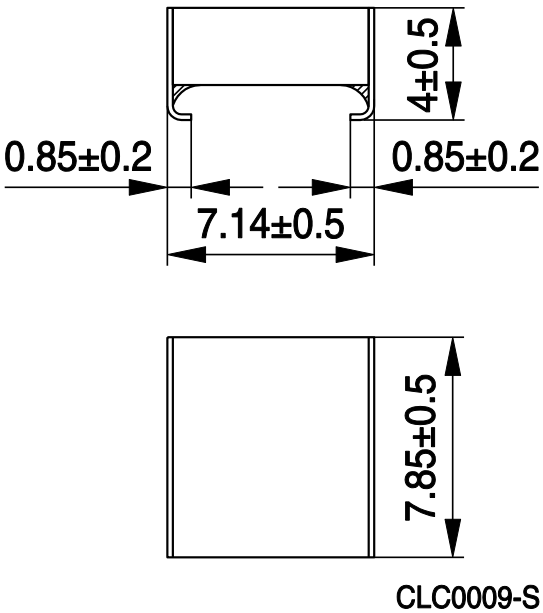
Dimensional drawings

L-style terminal



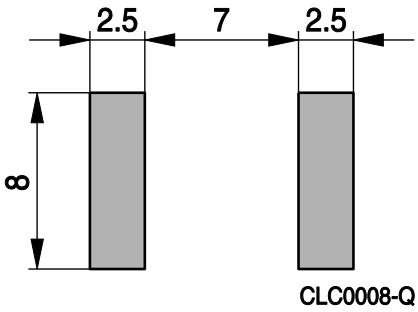
CLC0007-P

J-style terminal

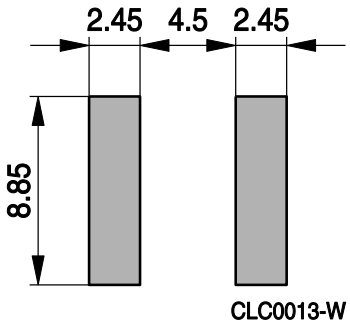


CLC0009-S

Recommended solder pads



CLC0008-Q

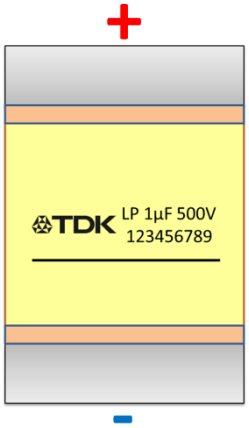


CLC0013-W

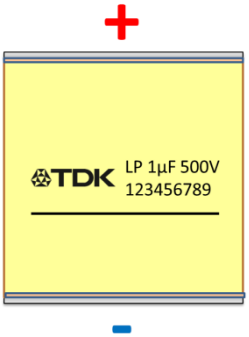
Dimensions in mm

Polarity

L-style terminal



J-style terminal



Marking of components

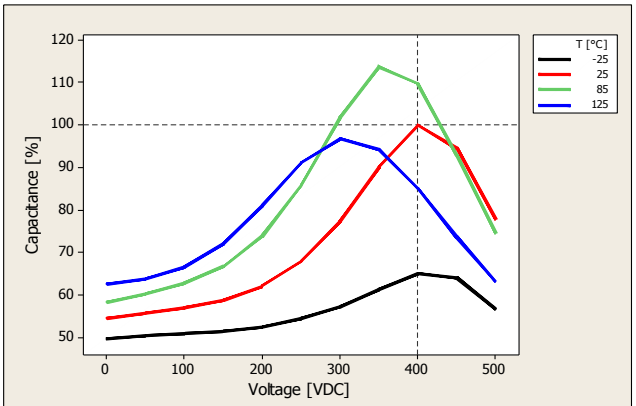
Manufacturer's logo
CeraLink™ type
Nominal capacitance
Rated voltage
Lot number, 9 digits

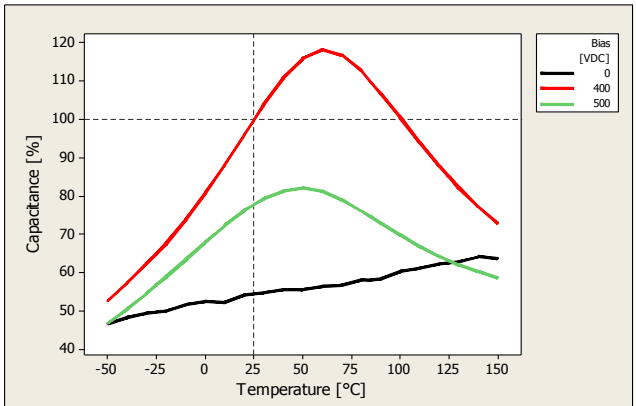
Typical characteristics as a function of temperature and voltage V_R = 500 V

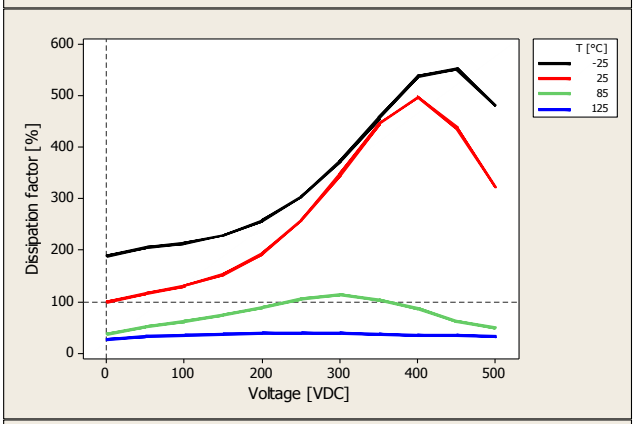
(V_{AC} = 0.5 V_{RMS}, frequency = 1 kHz)

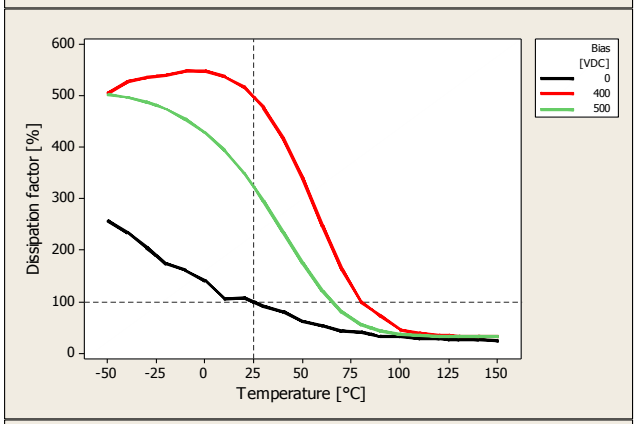
All given temperatures are device temperatures.

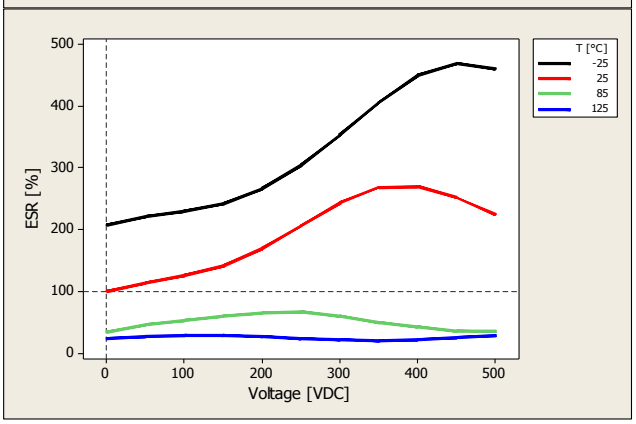
The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to $C_{eff,typ}$ and tan δ which are given on page 3 of this data sheet.

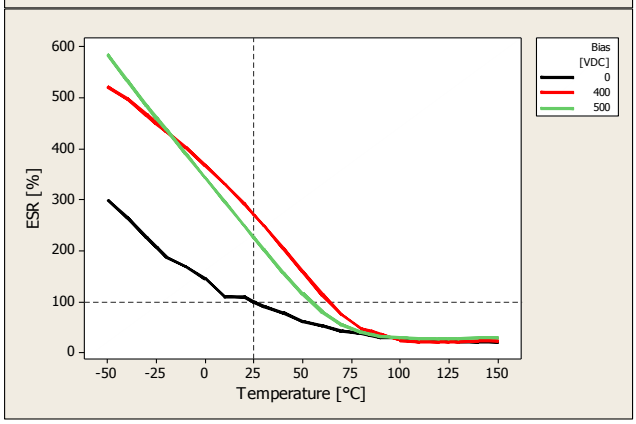




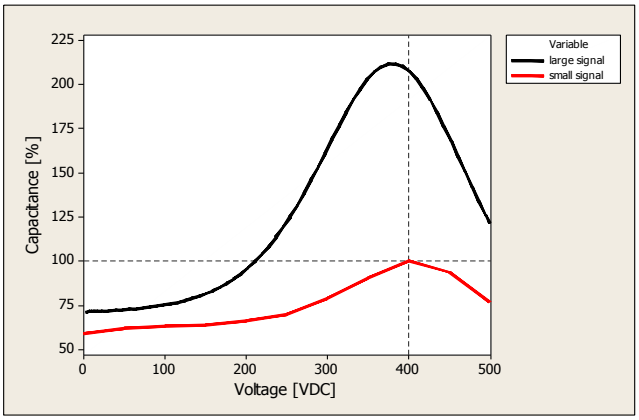








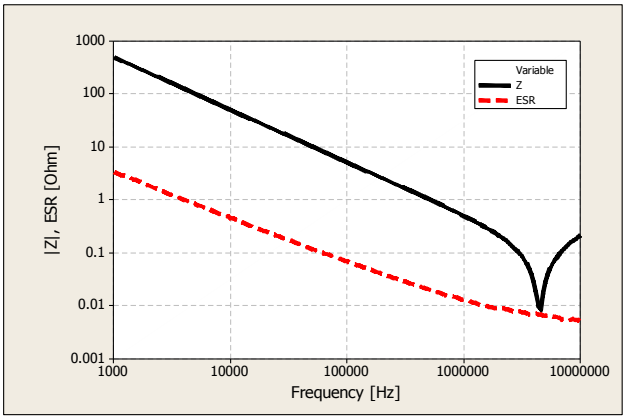
Typical capacitance values as a function of voltage V_R = 500 V



Large signal capacitance:
Quasistatic (slow variation of the voltage), 25 °C
The nominal capacitance is defined as the large signal capacitance at V_{op}.
See glossary for further information.

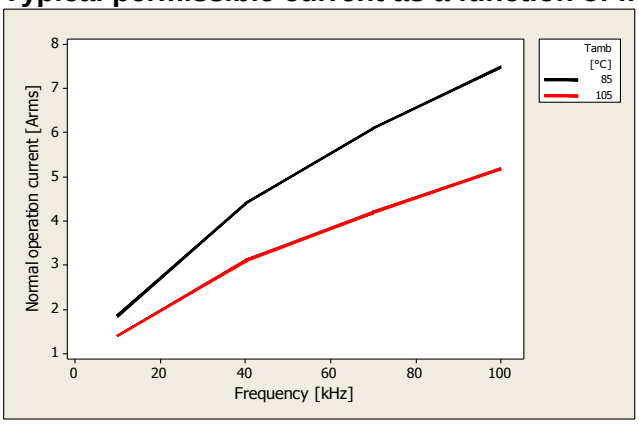
Small signal capacitance:
0.5 V_{RMS}, 1 kHz, 25 °C
The effective capacitance is defined as the small signal capacitance at V_{op}.

Typical impedance and ESR as a function of frequency V_R = 500 V



V_{DC} = 0 V, V_{AC} = 0.5 V_{RMS}, T_{device} = 25 °C

Typical permissible current as a function of frequency V_R = 500 V



Measurement performed at V_{op}.
The values correspond to a device temperature of 125 °C.
No forced cooling was used.

Aging

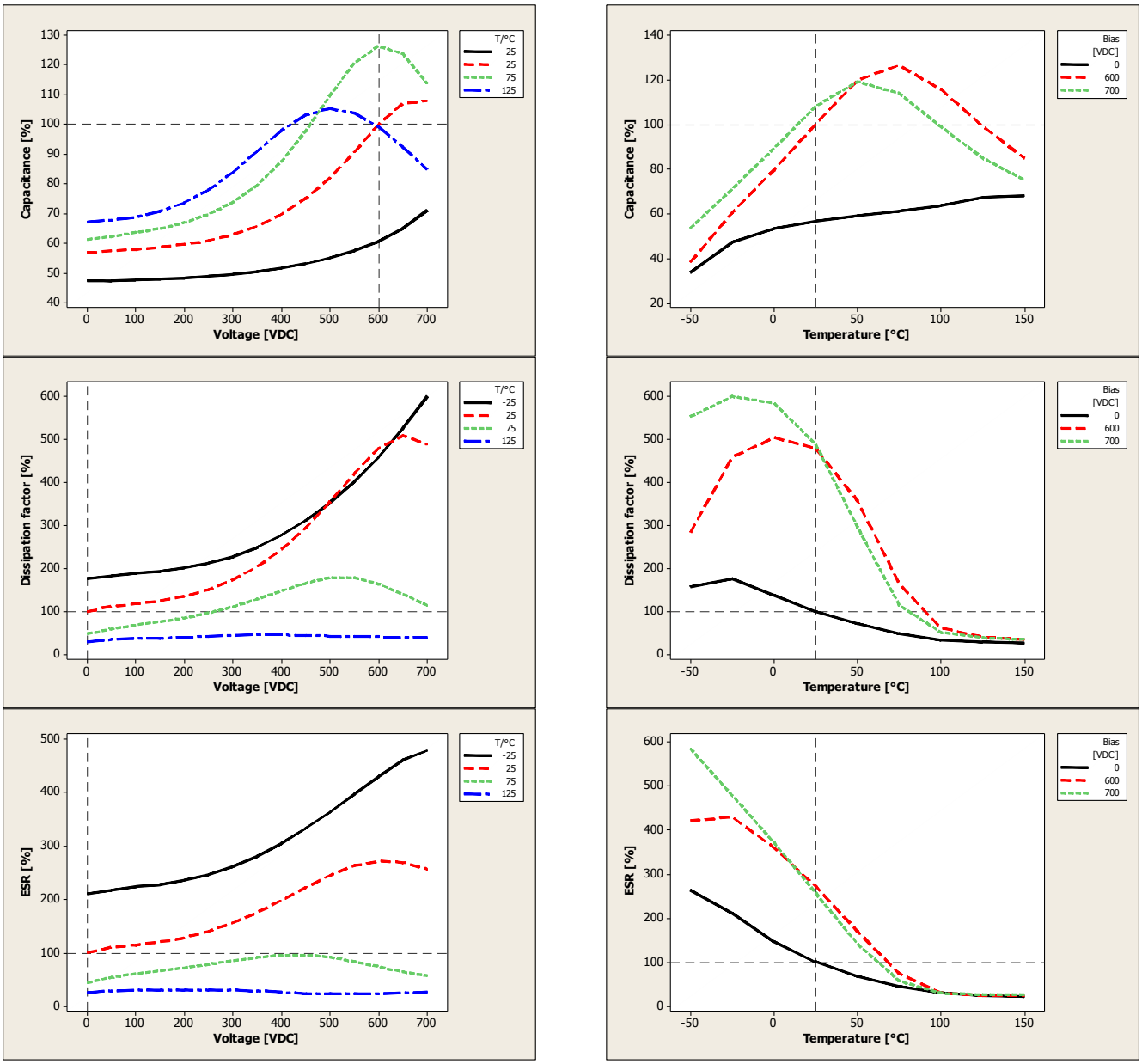
The capacitance has an aging behavior which shows a decrease of capacitance with time.
The typical aging rate is about 2.5% per logarithmic decade in hours.

Typical characteristics as a function of temperature and voltage V_R = 700 V

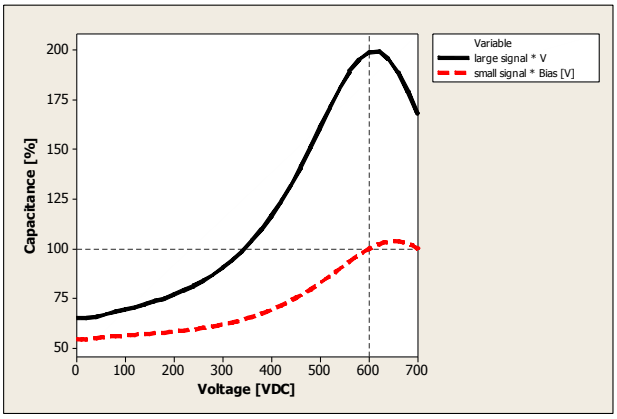
(V_{AC} = 0.5 V_{RMS}, frequency = 1 kHz)

All given temperatures are device temperatures.

The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to $C_{eff, typ}$ and tan δ which are given on page 4 of this data sheet.



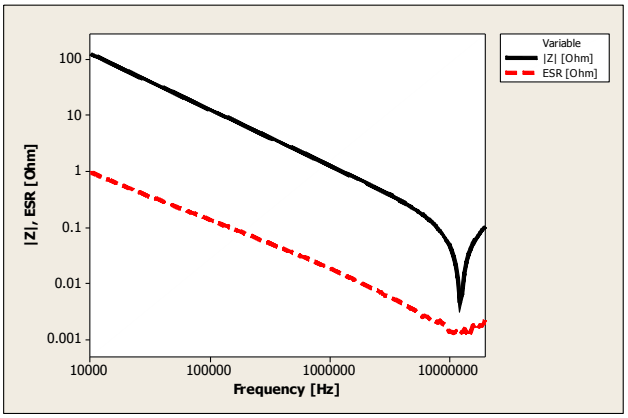
Typical capacitance values as a function of voltage V_R = 700 V



Large signal capacitance:
Quasistatic (slow variation of the voltage), 25 °C
The nominal capacitance is defined as the large signal capacitance at V_{op}.
See glossary for further information.

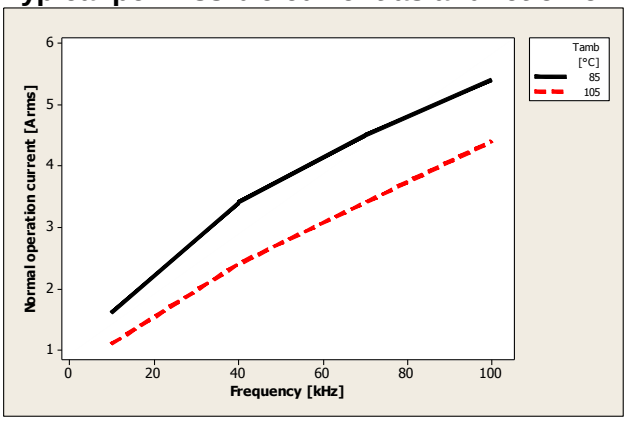
Small signal capacitance:
0.5 V_{RMS}, 1 kHz, 25 °C
The effective capacitance is defined as the small signal capacitance at V_{op}.

Typical impedance and ESR as a function of frequency V_R = 700 V



V_{DC} = 0 V, V_{AC} = 0.5 V_{RMS}, T_{device} = 25 °C

Typical permissible current as a function of frequency V_R = 700 V



Measurement performed at V_{op}.
The values correspond to a device temperature of 125 °C.
No forced cooling was used.

Aging

The capacitance has an aging behavior which shows a decrease of capacitance with time.
The typical aging rate is about 2.5% per logarithmic decade in hours.

Reliability

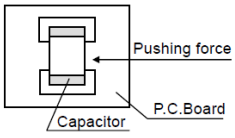
A. Preconditioning:

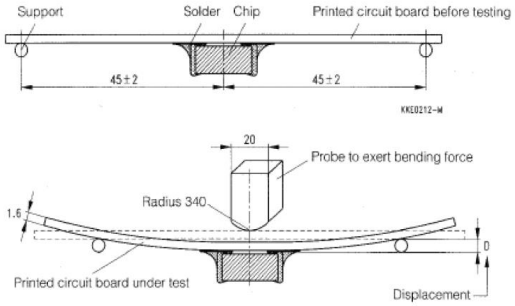
- Reflow solder the capacitor on a PCB using the recommended soldering profile
- Check of external appearance
- Measurement of electrical parameters R_{ins}, C_0, tan δ
    - Apply $V_{pk,max}$ for 7 seconds and measure R_{ins} at room temperature:
      Isolation resistance (@ $V_{pk,max}$, 7 s, 25 °C) **R_{ins} > 100 MΩ**
    - Measure C_0 and tan δ within 10 minutes to 1 hour afterwards:
      Initial capacitance (@ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C)
      Dissipation factor (@ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C)

B. Performance of a specific reliability test.

C. After performing a specific test:

- Check the external appearance again
- Repeat the measurement of the electrical parameters
    - Apply $V_{pk,max}$ for 7 seconds and measure R_{ins} at room temperature:
      Isolation resistance (@ $V_{pk,max}$, 7 s, 25 °C) **R_{ins} > 10 MΩ**
    - Measure C and tan δ:
      Change of initial capacitance (@ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C) **| Δ C / C_0 | < 15%**
    - Dissipation factor (@ 0 V_{DC}, 0.5 V_{RMS}, 1 kHz, 25 °C) **tan δ < 0.05**

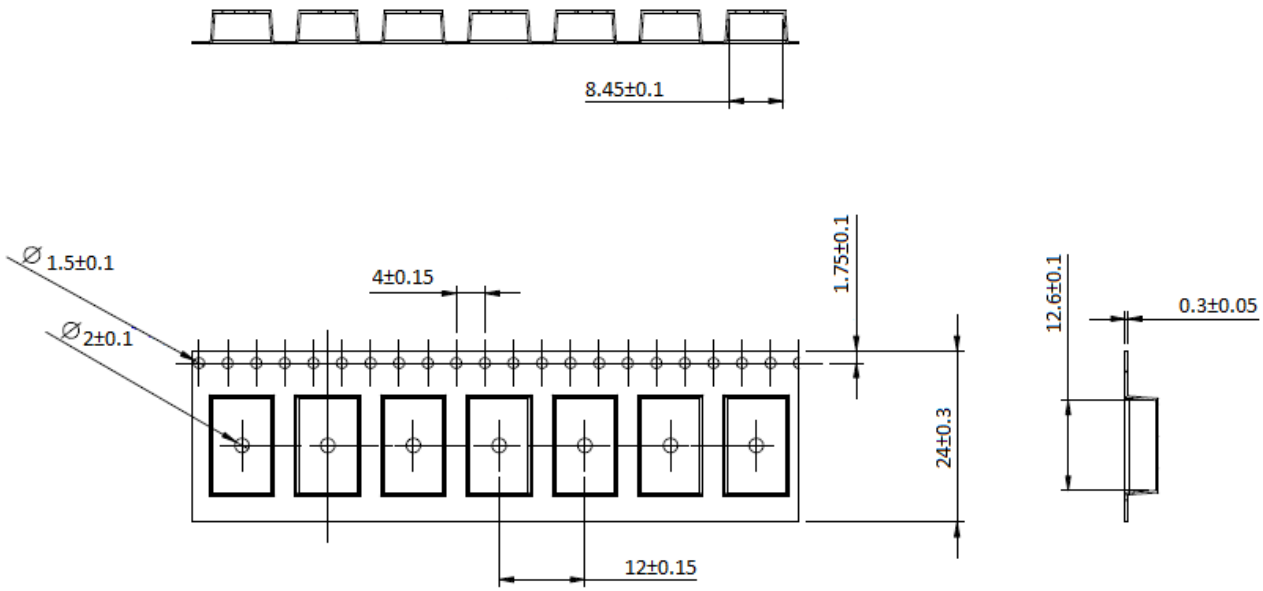
Test	Standard	Test conditions	Criteria
External appearance		Visual inspection with magnifying glass	No defects that might affect performance
High temperature operating life	MIL-STD-202, method 108	150 °C, V_R, 1000 hours	No mechanical damage | Δ C / C_0 |, tan δ and R_{ins} within defined limits
Biased humidity	MIL-STD-202, method 103	85 °C, 85% rel. hum., V_R, 1000 hours	No mechanical damage | Δ C / C_0 |, tan δ and R_{ins} within defined limits
Temperature shock	IEC 60384-9, 4.8	-55 °C to +150 °C 20 seconds transfer time 15 minutes dwell time 1000 cycles	No mechanical damage | Δ C / C_0 |, tan δ and R_{ins} within defined limits
Terminal strength test	AEC-Q200-005	Apply a force of 17.7 N for 60 seconds 	No detaching of termination. No rupture of ceramic | Δ C / C_0 |, tan δ and R_{ins} within defined limits

Test	Standard	Test conditions	Criteria
Tensile strength test (unsoldered)		Apply a force of 10 N in the shown direction Ceramic body is clamped 	No detaching of termination. No rupture of ceramic $\lvert \Delta C / C_0 \rvert$, tan δ and R_{ins} within defined limits
Board flex	AEC-Q200-005	Bending of 2 mm for 60 seconds.  Dimension drawing in mm.	No mechanical damage $\lvert \Delta C / C_0 \rvert$, tan δ and R_{ins} within defined limits
Vibration	MIL-STD-202, method 204	5 g/ 20 min, 12 cycles, 3 axis 10 Hz to 2000 Hz	No mechanical damage $\lvert \Delta C / C_0 \rvert$, tan δ and R_{ins} within defined limits
Mechanical shock	MIL-STD-202, method 213	Acceleration 400 m/s² Half sine pulse duration 6 milliseconds 4000 bumps	No mechanical damage $\lvert \Delta C / C_0 \rvert$, tan δ and R_{ins} within defined limits
Reflow test		3 times recommended reflow soldering profile	No mechanical damage Proper solder coating of contact areas $\lvert \Delta C / C_0 \rvert$, tan δ and R_{ins} within defined limits
Leaching test (lead frame only)	MIL-STD-202, method 210, condition B	Dip test of contact areas in solder bath (260 °C for 10 seconds)	No damage of lead frame silver coating
Solderability (lead frame only)	J-STD-002, method A @ 235 °C, category 3	Dip test of contact areas in solder bath (235 °C for 5 ± 0.5 seconds)	> 95% wettability of lead frame
Resistance to solvent		Dipping and cleaning with isopropanol	Marking must be legible $\lvert \Delta C / C0 \rvert$, tan δ and Rins within defined limits
Geometry		Using a caliper	Within specified tolerance in the chapter construction

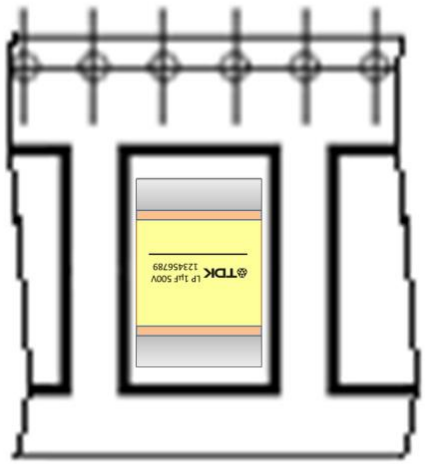
Packaging

The CeraLink™ will be delivered in a blister tape (taping to IEC 60286-3).

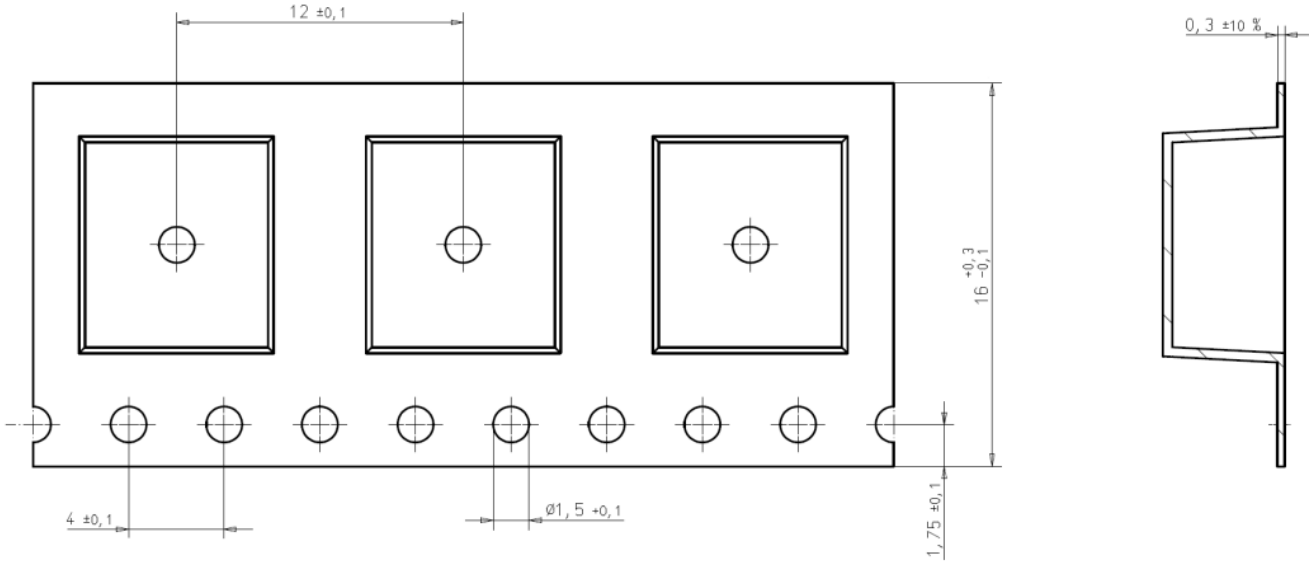
Blister tape for L-style terminal



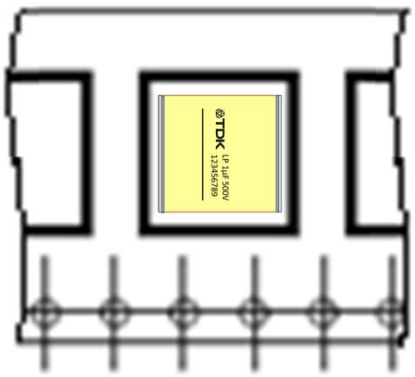
Part orientation



Blister tape for J-style terminal



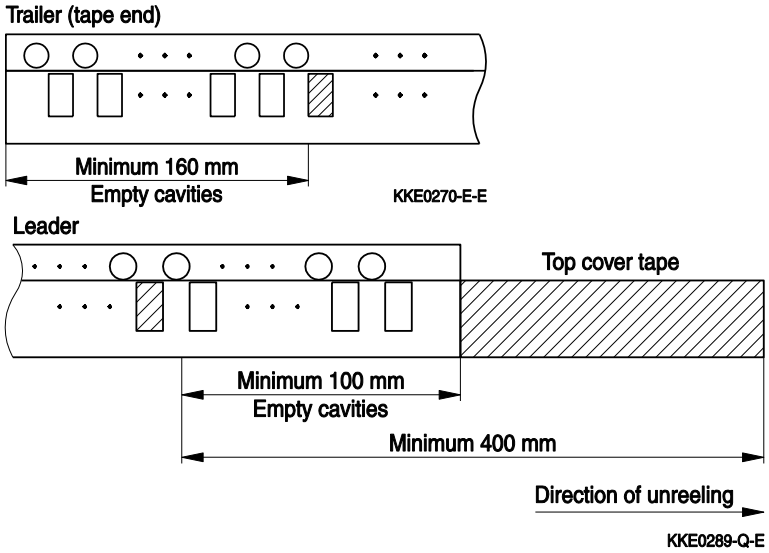
Part orientation



Taping information

Trailer: There is a minimum of 160 mm of carrier tape with empty compartments and sealed by the cover tape.

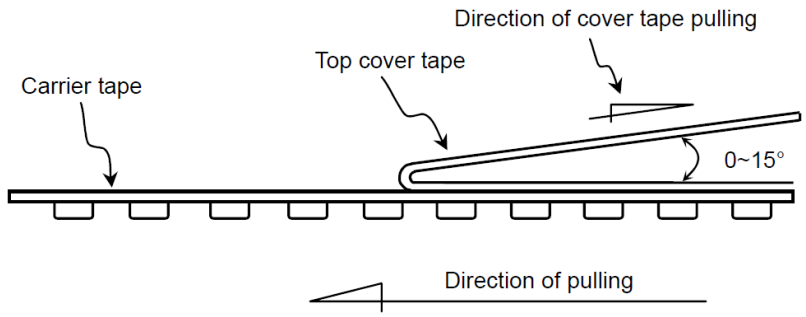
Leader: There is a minimum of 400 mm of cover tape, which includes at least 100 mm of carrier tape with empty compartments.



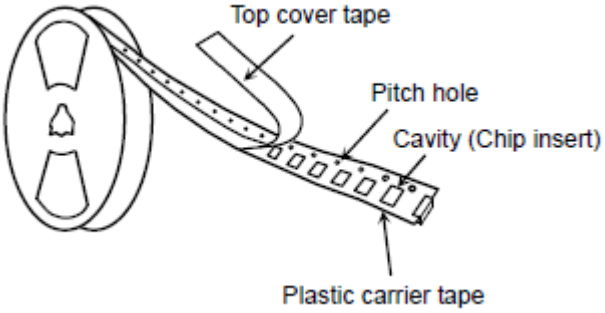
Dimensions in mm

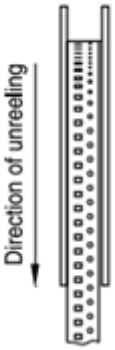
Fixing peeling strength (top tape)

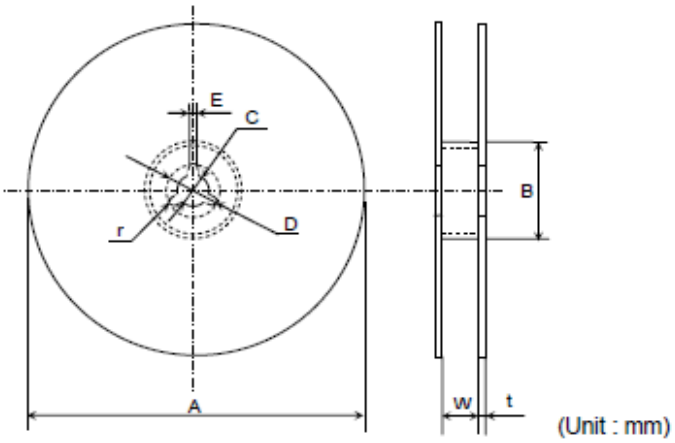
The peeling strength is 0.1 … 1.3 N.



Reel packing



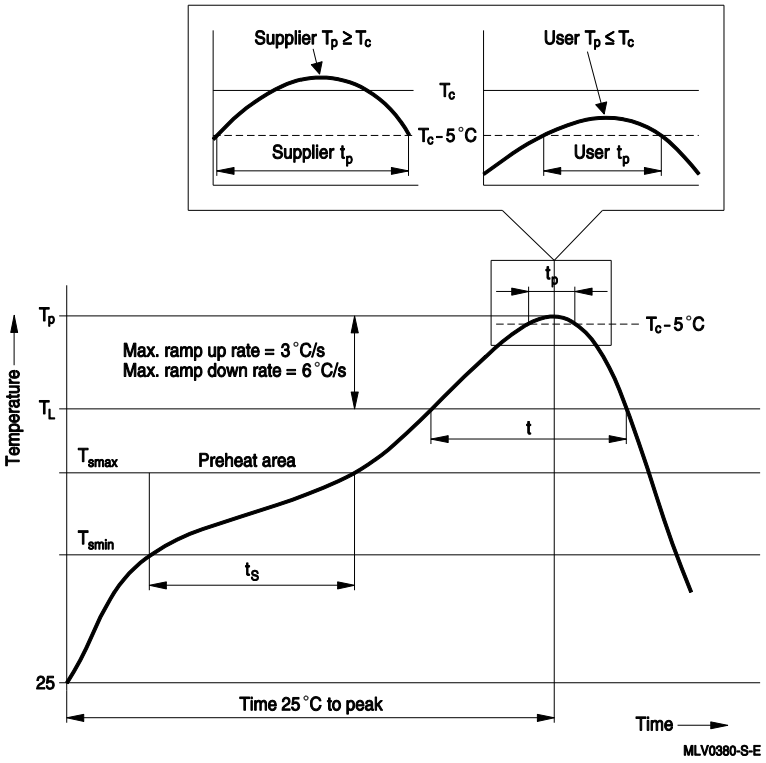




	L-style terminal	J-style terminal
A	330 ±2	330 ±2
B	100 ±1	62 ±1
C	13 +0.5/ -0.2	12.8 +0.7
D	20.2 min.	19.1 min.
E	2.2 ±0.2	1.6 ±0.5
W	24.2 +2	16.4 +2

Dimensions in mm

Recommended reflow soldering profile



Profile feature		SAC, Sn95.5Ag3.8Cu0.7 @ N_2 atmosphere
Preheat and soak		
- Temperature min	T_{smin}	150 °C
- Temperature max	T_{smax}	200 °C
- Time	t_{smin} to t_{smax}	60 … 180 seconds
Average ramp-up rate	T_{Smax} to T_p	3 °C/ second max.
Liquidus temperature	T_L	217 °C
Time at liquidus temperature	t_L	60 … 150 seconds
Peak package body temperature	T_p [1)]	245 °C … 260 °C max.[2)]
Time (t_p)[3)] within 5 °C of specified classification temperature (T_c)		30 seconds[3)]
Average ramp-down rate	T_p to T_{Smax}	6 °C/ second max.
Time 25 °C to peak temperature		maximum 8 minutes

1) Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

2) Depending on package thickness. For details please refer to JEDEC J-STD-020D.

3) Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Notes:

All temperatures refer to topside of the package, measured on the package body surface.

Max. number of reflow cycles: 3

After the soldering process, the capacitance is lowered. Applying V_R to the device will re-establish the capacitance.

The components are suitable for reflow soldering to JEDEC J-STD-020D.

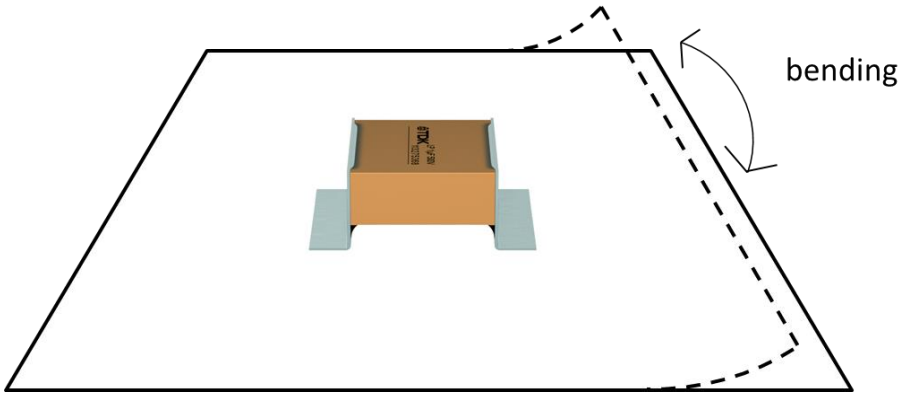
General technical information

Storage

- Only store CeraLink™ capacitors in their original packaging. Do not open the package prior to processing.
- Storage conditions in original packaging: temperature −25 °C to +45 °C, relative humidity ≤ 75% annual average, maximum 95%, dew precipitation is inadmissible.
- Do not store CeraLink™ capacitors where they are exposed to heat or direct sunlight. Otherwise the packaging material may be deformed or CeraLink™ may stick together, causing problems during mounting.
- Avoid contamination of the CeraLink™ surface during storage, handling and processing.
- Avoid storing CeraLink™ devices in harmful environments where they are exposed to corrosive gases (e.g. SOx, Cl).
- Use CeraLink™ as soon as possible after opening factory seals such as polyvinyl-sealed packages.
- Solder CeraLink™ components within 6 months after shipment from EPCOS.

Handling

- Do not drop CeraLink™ components or allow them to be chipped.
- Do not touch CeraLink™ with your bare hands - gloves are recommended.
- Avoid contamination of the CeraLink™ surface during handling.
- The CeraLink™ was tested to withstand the board flex test defined in the AEC-Q200 rev. D, method 005.
- The CeraLink™ uses copper lead frames to prevent mechanical stress to the ceramic. Too much bending causes open mode. Avoid high mechanical stress like twisting after soldering on a PCB.

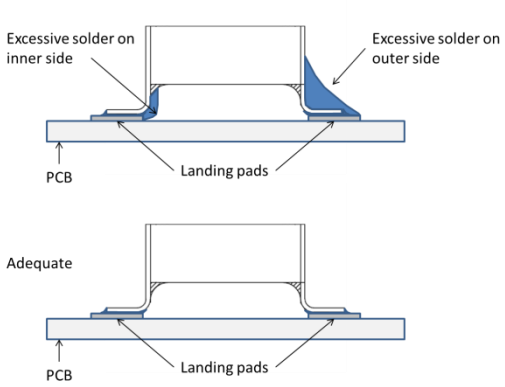


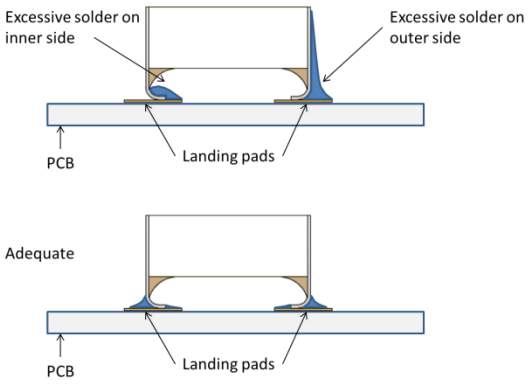
Mounting

- Do not subject CeraLink™ devices to mechanical stress when encapsulating them with sealing material or overmolding with plastic material. Encapsulation may lead to worse heat dissipation too. Please ask for further information.
- Do not scratch the electrodes before, during or after the mounting process.
- Make sure contacts and housings used for assembly with CeraLink™ components are clean before mounting.
- The surface temperature of an operating CeraLink™ can be higher than the ambient temperature. Ensure that adjacent components are placed at a sufficient distance from a CeraLink™ to allow proper cooling.
- Avoid contamination of the CeraLink™ surface during processing.

Soldering guidelines

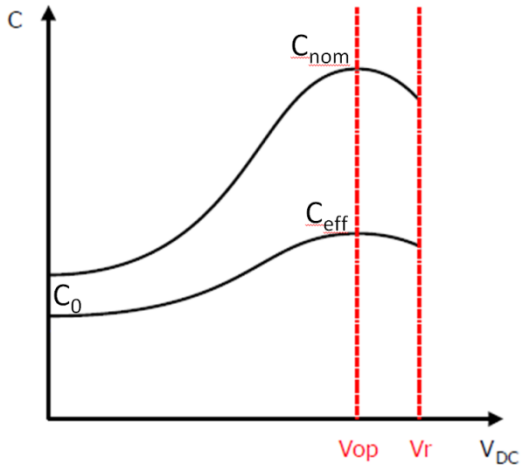
- The use of mild, non-activated fluxes for soldering is recommended, as well as proper cleaning of the PCB.
- Complete removal of flux is recommended to avoid surface contamination that can result in an instable and/or high leakage current.
- Use resin-type or non-activated flux.
- Bear in mind that insufficient preheating may cause ceramic cracks.
- Rapid cooling by dipping in solvent is not recommended, otherwise a component may crack.
- Excessive usage of solder paste can reduce the mechanical robustness of the device, whereas insufficient solder may cause the CeraLink™ to detach from the PCB. Use an adequate amount of solder paste, but on the landing pads only.





- If an unsuitable cleaning fluid is used, flux residue or foreign particles may stick to the CeraLink™ surface and deteriorate its insulation resistance. Insufficient or improper cleaning of the CeraLink™ may cause damage to the component.
- Excessive washing like ultrasonic cleaning, can affect the connection between the ceramic chip and the outer electrode. To avoid this, we give the following recommendation:
  - Power: 20 W/l max.
  - Frequency: 40 kHz max.
  - Washing time: 5 minutes max.

Glossary



Initial capacitance C_0:	Is the value at the origin of the hysteresis without any applied direct voltage.
Effective capacitance C_{eff}:	Occurs at V_{op} and is measured with an applied ripple voltage of 0.5 V_{RMS} and 1 kHz. The CeraLink™ is designed to have its highest capacitance value at the operating voltage V_{op}.
Nominal capacitance C_{nom}:	Is the value derived by the tangent of the mean hysteresis as the derivation of the mean hysteresis is dQ/dV ~ C.

Symbols and terms

AC	Alternating current
C_0	Initial capacitance
$C_{eff,typ}$	Typical effective capacitance
$C_{nom,typ}$	Typical nominal capacitance
DC	Direct current
ESL	Equivalent serial inductance
ESR	Equivalent serial resistance
I_{op}	Operating ripple current, root mean square value of sinusoidal AC current
LP	Low profile
PCB	Printed circuit board
PLZT	Lead lanthanum zirconium titanate
R_{ins}	Insulation resistance
SAC	Tin silver copper alloy; lead-free solder paste
T_A	Ambient temperature
tan δ	Dissipation factor
T_{device}	Device temperature. $T_{device} = T_A + \Delta T$ (ΔT defines the self-heating of the device due to applied current).
V_{op}	Operating voltage
V_R	Rated voltage
V_{RMS}	Root mean square value of sinusoidal AC voltage
$V_{pk,max}$	Maximum peak operating voltage
ΔT	Increase of temperature during operation

Cautions and warnings

General

Not for use in resonant circuits, where a voltage of alternating polarity occurs.

Not for AC applications. Consult your EPCOS representative for further details.

If used in snubber circuits, ensure that the sum of all voltages remains at the same polarity.

Some parts of this publication contain statements about the suitability of our CeraLink™ components for certain areas of application, including recommendations about incorporation/design-in of these products into customer applications. The statements are based on our knowledge of typical requirements often made of our CeraLink™ devices in the particular areas. We nevertheless expressly point out that such statements cannot be regarded as binding statements about the suitability of our CeraLink™ components for a particular customer application. As a rule, EPCOS is either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always incumbent on the customer to check and decide whether the CeraLink™ devices with the properties described in the product specification are suitable for use in a particular customer application.

- Do not use EPCOS CeraLink™ components for purposes not identified in our specifications.
- Ensure the suitability of a CeraLink™ in particular by testing it for reliability during design-in. Always evaluate a CeraLink™ component under worst-case conditions.
- Pay special attention to the reliability of CeraLink™ devices intended for use in safety-critical applications (e.g. medical equipment, automotive, spacecraft, nuclear power plant).

Design notes

- Consider derating at higher operating temperatures. As a rule, lower temperatures and voltages increase the life time of CeraLink™ devices.
- If steep surge current edges are to be expected, make sure your design is as low-inductive as possible.
- In some cases the malfunctioning of passive electronic components or failure before the end of their service life cannot be completely ruled out in the current state of the art, even if they are operated as specified. In applications requiring a very high level of operational safety and especially when the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention, life-saving systems, or automotive battery line applications such as clamp 30), ensure by suitable design of the application or other measures (e.g. installation of protective circuitry, fuse or redundancy) that no injury or damage is sustained by third parties in the event of such a malfunction or failure.
- Specified values only apply to CeraLink™ components that have not been subject to prior electrical, mechanical or thermal damage. The use of CeraLink™ devices in line-to-ground applications is therefore not advisable, and it is only allowed together with safety countermeasures such as thermal fuses.

Operation

- Use CeraLink™ only within the specified operating temperature range.
- Use CeraLink™ only within specified voltage and current ranges.
- The CeraLink has to be operated in a dry atmosphere, which must not contain any additional chemical vapors or substances.
- Environmental conditions must not harm the CeraLink™. Use the capacitors under normal atmospheric conditions only. A reduction of the oxygen partial pressure to below 1 mbar is not permissible.
- Prevent a CeraLink™ from contacting liquids and solvents.
- Avoid dewing and condensation.
- During operation, the CeraLink™ can produce audible noise due to its piezoelectric characteristic.
- EPCOS CeraLink™ components are mainly designed for encased applications. Under all circumstances avoid exposure to:
    - direct sunlight
    - rain or condensation
    - steam, saline spray
    - corrosive gases
    - atmosphere with reduced oxygen content

This listing does not claim to be complete, but merely reflects the experience of EPCOS AG.

Display of ordering codes for EPCOS products

The ordering code for one and the same EPCOS product can be represented differently in data sheets, data books, other publications, on the EPCOS website, or in order-related documents such as shipping notes, order confirmations and product labels. **The varying representations of the ordering codes are due to different processes employed and do not affect the specifications of the respective products**. Detailed information can be found on the Internet under www.epcos.com/orderingcodes

Important notes

The following applies to all products named in this publication:

1. Some parts of this publication contain **statements about the suitability of our products for certain areas of application**. These statements are based on our knowledge of typical requirements that are often placed on our products in the areas of application concerned. We nevertheless expressly point out **that such statements cannot be regarded as binding statements about the suitability of our products for a particular customer application.** As a rule, EPCOS is either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always ultimately incumbent on the customer to check and decide whether an EPCOS product with the properties described in the product specification is suitable for use in a particular customer application.
2. We also point out that **in individual cases, a malfunction of electronic components or failure before the end of their usual service life cannot be completely ruled out in the current state of the art, even if they are operated as specified.** In customer applications requiring a very high level of operational safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health (e.g. in accident prevention or life-saving systems), it must therefore be ensured by means of suitable design of the customer application or other action taken by the customer (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of malfunction or failure of an electronic component.
3. **The warnings, cautions and product-specific notes must be observed.**
4. In order to satisfy certain technical requirements, **some of the products described in this publication may contain substances subject to restrictions in certain jurisdictions (e.g. because they are classed as hazardous)**. Useful information on this will be found in our Material Data Sheets on the Internet (www.epcos.com/material). Should you have any more detailed questions, please contact our sales offices.
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