ACPL-337J

Infineon EasyPIM™ 1B IGBT Module EB600-337J Evaluation Board

Reference Manual
Version 1.0

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Chapter 1: About This Document

1.1 Scope and Purpose

This document describes how to use Broadcom® EB600-337J evaluation board in a proper and safe way. The EB600-337J evaluation board contains a power integrated module (PIM), which includes a three-phase diode bridge, a brake-chopper IGBT/diode, and a three-phase IGBT inverter, together with the gate driver circuit and DC bus capacitors. The voltage rating of the power module is 600V. The evaluation board features an ACPL-337J isolated gate driver that drives IGBT switches and an ACPL-C87A isolated amplifier that measures the NTC temperature of the power module. The evaluation board supports the power integrated moduled (PIMd) FP30R06W1E3 and FP15R06W1E3, but other PIMs with the same pin layout can be used as well. The integrated DC bus feature enables customers to evaluate the ACPL-337J isolated gate driver in conditions similar to actual applications, such as an industrial inverter.

The EB600-337J board is a gate driver evaluation board and it is *not* intended to be used as the continuously operating inverter or as the part of some other series product. Thus, it is *not* intended to be used for the continuous inverter operation; it enables customers to evaluate driving and other characteristics of Broadcom's ACPL-337J gate drivers that are aimed for high-performance power electronics conversion systems. For the short time inverter operation evaluation, additional heatsinks must be mounted.

The EB600-337J evaluation board can be either supplied with DC current by accessing DC bus terminals, or with AC current by using the input rectifier of the power module. In case an AC supply is used, ensure that an additional pre-charge circuit is added. Line chokes and a filter should also be placed. Additional boards with line input filters can be ordered separately.

If you need more information on the additional line filter board, or more specific data on the inverter operation evaluation, contact info@kinestas.com.

1.2 Warnings

The board operates at high voltages. Take special care to avoid the risk of injury and life endangering injuries. Consider, and take seriously, all of the following safety precautions when operating with this board:

- If the board is powered up, do not touch the board, especially exposed metal parts.
- Pay attention to the maximum ratings.
- Use of a protection cover made of insulating materials is mandatory.
- After powering off, wait at least 10 seconds for the DC bus capacitors to discharge, and check the DC bus voltage before touching the board.
- If board is used to drive a continuous load, the power module must be mounted on a heatsink. The board temperature may rise to high values. Therefore, any contact with the human body must be avoided.
- The board does *not* have a pre-charge circuit nor the EMC filter features. Thus, do *not* power-on the board directly from the three-phase AC grid if those features are not provided externally. For laboratory testing purposes, alternatives might be the usage of a three-phase autotransformer. Large inrush currents can cause failure and explosion of electrolytic capacitors, which can cause serious injuries.
- It is strongly recommended to place fuses at the input when powering up the board.
- It is strongly recommended to connect a –DC_BUS terminal to ground prior to applying power to the board.
- Whenever a change in the test setup is done (for example, changing the probe position), turn off the DC bus and the +24V supply to avoid injuries and the destruction of the board.
- The board itself does not provide dead-time generation. The recommended minimal dead time is 5 µs.

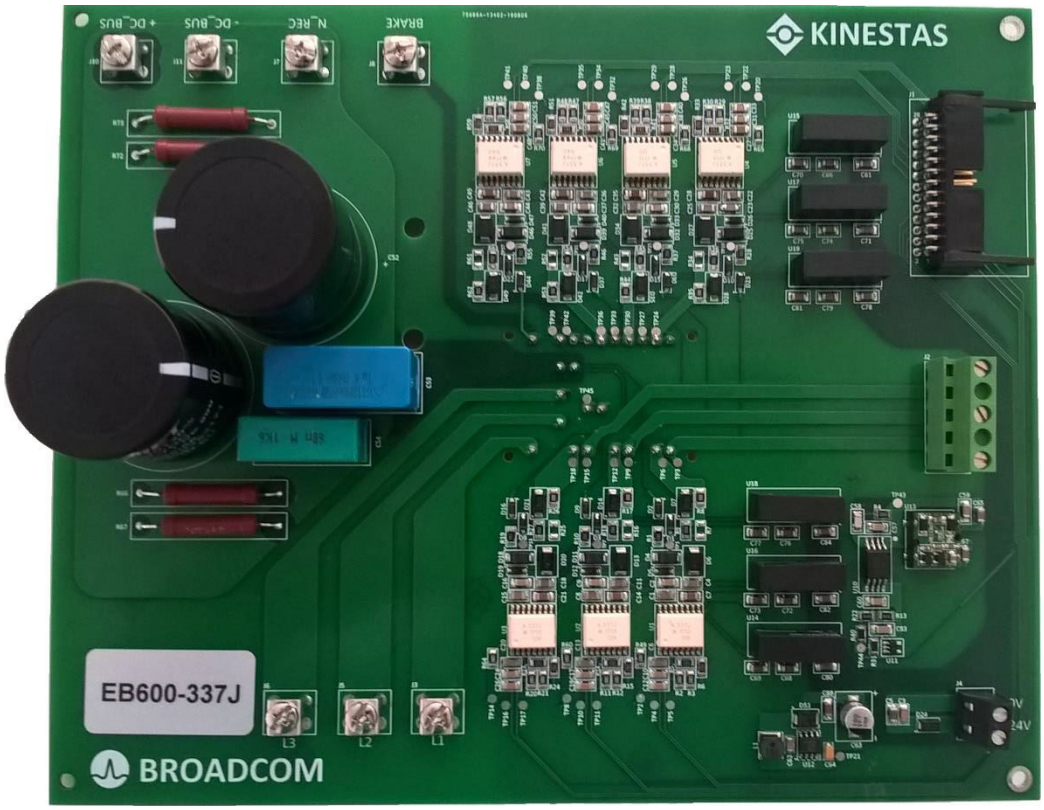
WARNING! Due to the technical requirements, high voltage components are used, and some of them could contain dangerous substances. Because the failure of such components can harm the user and even endanger the user's life, it is necessary to take all necessary precautions and safety measures prior to the evaluation of the EB600-337J.

Chapter 2: Introduction

The EB600-337J evaluation driver board with integrated DC bus, shown in Figure 1, is developed to support Broadcom customers during their first steps in designing inverter applications with the ACPL-337J gate drivers. Board properties and typical performance are described in this reference manual. Information related to design is given with an aim to enable customers to copy and modify the design specifics according to their technical requirements and use it in their own designs (see Section A.4, Disclaimer).

The design is tested, as described in this document, at the temperature of 25°C, but it is not qualified regarding operation in the entire operating ambient temperature range of ACPL-337J, or its lifetime. The board is subjected to functional testing only. Electrical components used in this design are selected to be suitable for lead-free reflow soldering.

Figure 1: Evaluation Gate Driver Board EB600-337J



2.1 Design Features

The EB600-337J includes the following main features:

- Seven isolated ACPL-337J gate drivers with the following features:
  - DESAT (short circuit protection)
  - Undervoltage lock out (UVLO)
  - Active Miller clamp
  - Fault and UVLO status feedback signal

- The ACPL-C87A optical amplifier enables isolated temperature measurement with the following features:
  - 0 to 2V nominal input range
  - 100-kHz bandwidth
  - 3V to 5.5V wide supply range for the output side
  - 15-kV/µs common-mode transient immunity
- Electrically and mechanically suitable for 600V EasyPIM™ modules (FP30R06W1E3/FP15R06W1E3).
- 24V/5V DC-DC power supply with current limit protection and thermal shutdown.
- Isolated power supplies for gate drivers.
- Access to PWM input signals.
- Access to drivers' fault and UVLO output signals for protection and control development purposes.
- An integrated DC bus with access to DC bus terminals.
- Access to the brake chopper terminal.
- Easy access to leg current using a Rogowski coil probe for switching characteristics evaluation.

2.2 Target Applications

The Broadcom ACPL-337J gate driver targets the following applications:

- Isolated IGBT/Power MOSFET gate drives
- Renewable energy applications
- AC and brushless DC motor drives
- Industrial inverters
- Switching power supplies

Chapter 3: System Description

This chapter provides the EB600-337J specifications and functional description, interfaces, and mechanical details.

3.1 Key Specifications

Table 1 lists the absolute maximum ratings of the EB600-337J. Note that Table 1 contains only key parameters. Constraints from ACPL-337J data sheet as well as specifications of other key components must be considered when the EB600-337J is used.

Table 1: Absolute Maximum Ratings

Parameter	Values			Units	Note
	Min.	Typ.	Max.		
V_{dc+} to V_{dc-} when the DC bus supplied externally	—	300	400	V	Limited by the voltage overshoot during turn-off transient. DC bus capacitors voltage rating is 450V.
Input rectifier line to line RMS voltage	—	208	240	V	N_REC terminal should be shorted with -DC_BUS terminal, and one of the following conditions should be satisfied if the board is powered through three-phase AC lines (L1, L2, L3): ■ Pre-charge circuit is added externally. ■ Powering the board through an autotransformer enables smooth charging of the DC bus.
Brake chopper current	—	—	—	A	Limited by the power module ratings.
Inverter IGBT peak current	—	—	—	A	Limited by the power module ratings.
Continuous RMS current	—	—	—	A	Limited by the power module ratings and the heatsink characteristics.
V_{CC} input voltage	21.6	24	26.4	V	External DC input power supply for the digital circuitry.
PWM input logic level	0	3.3	5	V	External PWM inputs for the gate drivers; thresholds are defined in the ACPL-337J data sheet.
Fault output logic level	0	—	5	V	Logic output signal, refer to the ACPL-337J data sheet.
UVLO output logic level	0	—	5	V	Logic output signal, refer to the ACPL-337J data sheet.

3.2 Functional Block Diagram

Figure 2 shows the functional block diagram and Figure 3 shows the disposition of the functional blocks of the EB600-337J gate evaluation board. In the middle of the system is a power integrated module (yellow), and its DC terminals are connected to a DC bus capacitor bank (blue). The DC bus can be supplied with an AC power source by using an integrated three-phase diode rectifier, or externally through the DC bus terminals. If a diode rectifier is used, the negative side of the diode rectifier (N_REC) and the negative side of the DC bus (–DC_BUS) must be shorted. The DC bus terminals as well as other power terminals are shown in grey in Figure 2. Low-voltage side connectors aimed for signal interface and power supply of digital side of ACPL-337J drivers are presented in green.

Figure 2: EB600-337J Functional Block Diagram

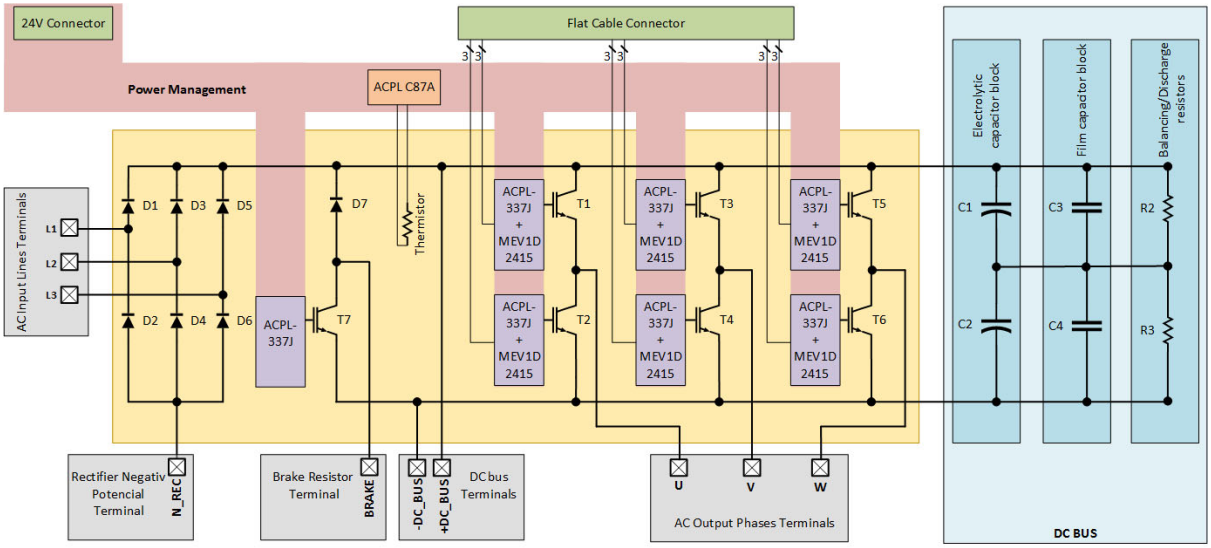
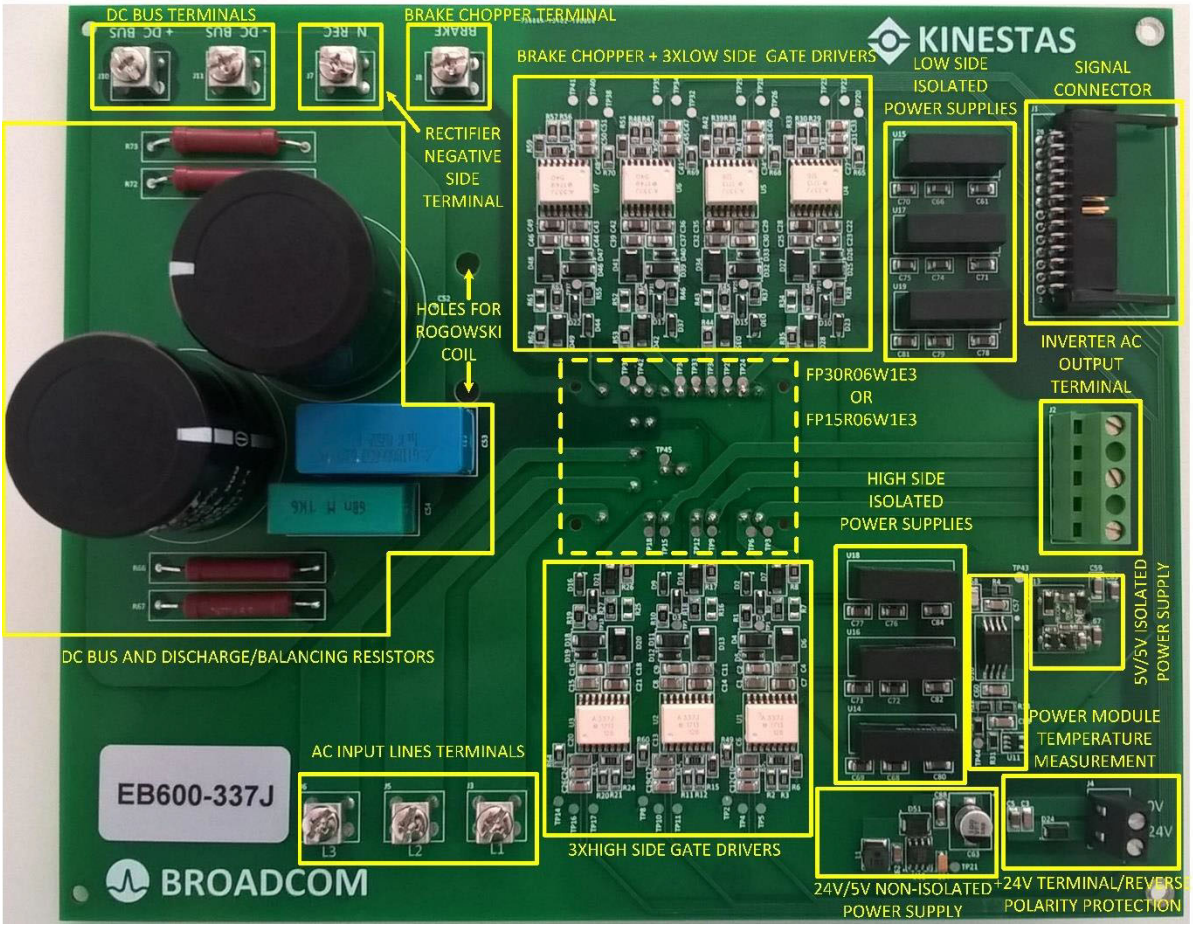


Figure 3: Functional Block Disposition of the EB600-337J



3.3 Pin Assignments

This section describes the pin assignments of signal and power interface on the EB600-337J. Part numbers and mechanical details of each connector can be found using manufacturer part numbers provided in Section A.3, BOM.

3.3.1 Signal Interface

Table 2 shows pin assignment for the signal connector J1. The schematic and layout of this connector are shown in Appendix A, Schematics, Layout, and BOM.

Table 2: Pinout of Connector J1

Pin	Label	Function	Direction
1	PWM.U	PWM signal for high-side power switch in phase 1	Input
2	PWM.X	PWM signal for low-side power switch in phase 1	Input
3	PWM.V	PWM signal for high-side power switch in phase 2	Input
4	PWM.Y	PWM signal for low-side power switch in phase 2	Input
5	PWM.W	PWM signal for high-side power switch in phase 3	Input
6	PWM.Z	PWM signal for low-side power switch in phase 3	Input
7	GND	Ground	Bidirectional
8	GND	Ground	Bidirectional
9	PWM.B	PWM signal for brake power switch	Input
10	UVLO.B	UVLO signal for brake power switch	Output
11	FAULT.B	Fault signal for brake power switch	Output
12	UVLO.U	UVLO signal for high-side power switch in phase 1	Output
13	FAULT.U	Fault signal for high side power switch in phase 1	Output
14	UVLO.V	UVLO signal for high-side power switch in phase 2	Output
15	FAULT.V	Fault signal for high-side power switch in phase 2	Output
16	UVLO.W	UVLO signal for high-side power switch in phase 3	Output
17	FAULT.W	Fault signal for high-side power switch in phase 3	Output
18	UVLO.X	UVLO signal for low-side power switch in phase 1	Output
19	FAULT.X	Fault signal for low side power switch in phase 1	Output
20	UVLO.Y	UVLO signal for low-side power switch in phase 2	Output
21	FAULT.Y	Fault signal for low-side power switch in phase 2	Output
22	UVLO.Z	UVLO signal for low-side power switch in phase 3	Output
23	FAULT.Z	Fault signal for low side power switch in phase 3	Output
24	GND	Ground	Bidirectional
25	GND	Ground	Bidirectional
26	TEMP	Isolated temperature measurement signal	Output

3.3.2 Power Interface

Description of the power terminals are provided in Table 3.

Table 3: Power Interface, Connectors Description

Label	Connector Description	Value
+DC_BUS	DC bus positive rail input	M4 screw terminal
-DC_BUS	DC bus negative rail input	
N_REC	Negative diode rectifier output rail	
BRAKE	Brake chopper IGBT – collector	
L1, L2, L3	Diode rectifier phase inputs	
U, V, W	Inverter phases	PCB screw terminal
0 V, 24 V	Isolated power supply input for digital circuitry	PM5.08/2/90, 26 AWG, 14 AWG

3.4 Mechanical Data

Table 4 provides a complete list of the mechanical data.

Table 4: Mechanical Data of the EB600-337J

Description	Value
Number of layers	4
PCB copper thickness	70 µm – top and bottom layer 35 µm – inner layers
PCB Insulating material	FR4
Board weight without PIM	370 g
Board length	225 mm
Board width	185 mm
Board height	48.6 mm
PCB thickness	1.6 mm

Chapter 4: Circuit Description

This chapter provides an in-depth insight of the features of the EB600-337J gate driver evaluation board.

4.1 Auxiliary Power Management

Figure 4 shows the auxiliary power management block diagram of the EB600-337J, and Figure 5 shows the EB600-337J power supply circuitry. The evaluation board is supplied from an external +24V source. The main 24V/5V power supply, based on LM2674 DC-DC switching regulator, is shown in Figure 5a. The +5V output of this power supply is used to supply the ACPL-337J gate drivers and the ACPL-C87A voltage sensor low-voltage side. An isolated 5V/5V voltage regulator, R1SX-0505-R, provides an isolated 5V for the ACPL-C87A high-voltage side, as shown in Figure 5b. The EB600-337J has six isolated power supplies 24V/+15V/–15V, which provide separated +15V and –15V for each gate driver high-voltage side. This circuitry is shown in Figure 6. Note that the ACPL -337J driver dedicated to drive the brake chopper IGBT shares a secondary side power supply with the ACPL-337J that drives low-side power switch.

Figure 4: Power Management Block Diagram

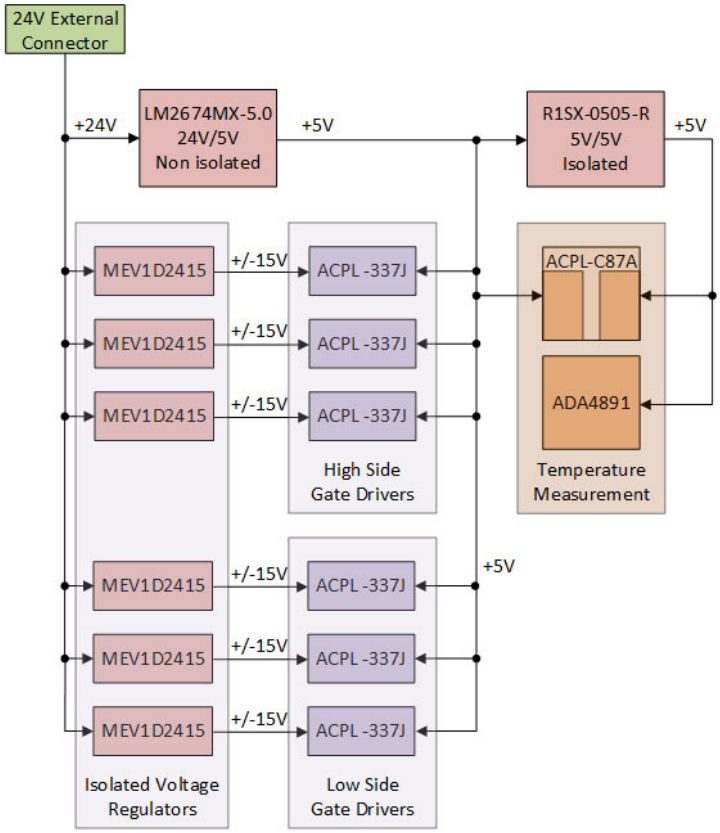


Figure 5: (a) 24V/5V Power Supply of the EB600-337J Board, and (b) the Isolated 5V/5V Power Supply

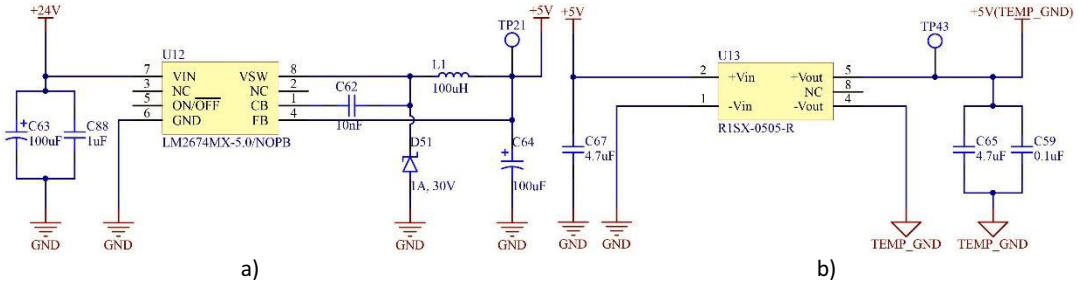
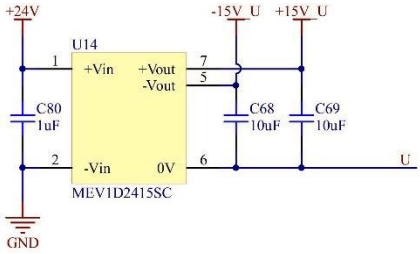


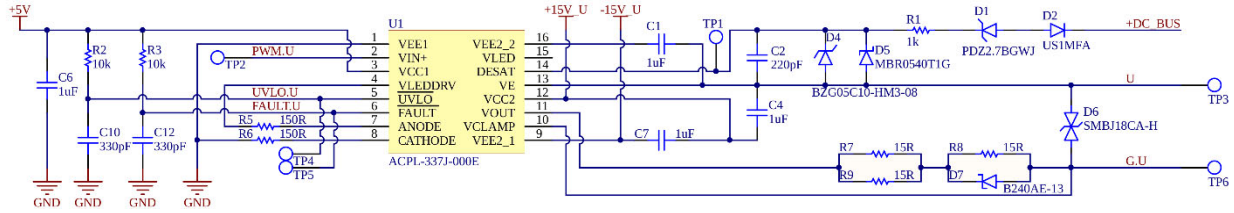
Figure 6: 24V/+15V/–15V Isolated Gate Driver High-Voltage Side Power Supply



4.2 Gate Driver Circuit

The used optocoupler-based IGBT gate drivers, ACPL-337J, feature fast signal propagation, desaturation detection, soft shutdown protection, active clamping, and fault feedback. Figure 7 shows the both the low-voltage and high-voltage side gate driver circuit.

Figure 7: Isolated Gate Drive Based on ACPL-337J

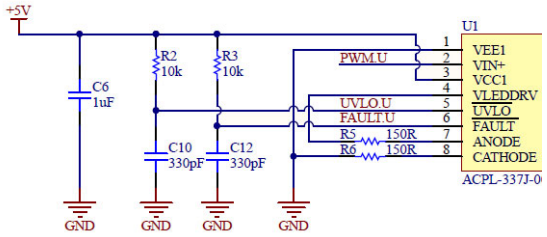


4.2.1 Gate Driver Circuit: Low-Voltage Side

Figure 8 shows the low-voltage (digital) side of the driver circuitry. The low-voltage side of the driver is supplied with +5V on the VCC1 pin. The UVLO and FAULT signals are pulled up to +5V with 10-kΩ resistors. These signals are active high when driver is working in the specified range of operation. Two 330-pF capacitors are added as a support for these signals according to the data sheet. The low-voltage side of the gate driver IC optocoupler contains an integrated LED driver with high-impedance input for interfacing with the controller. The LED driver output must be connected to the recommended split resistors to the anode pin to achieve the rated common mode rejection. It is recommended to have 1:1 split ratio. These resistors help balance the common mode impedances at the anode and cathode. This equalizes the common mode voltage changes at these pins therefore ensuring high common mode rejection performance. According to the data sheet, 150Ω resistors are connected on the ACPL-337J anode and cathode pins.

ATTENTION: Signals dedicated for high-side and low-side drivers, in one inverter leg, need to have proper dead time. The board itself does not provide dead-time generation. The recommended minimal dead time is 5 µs.

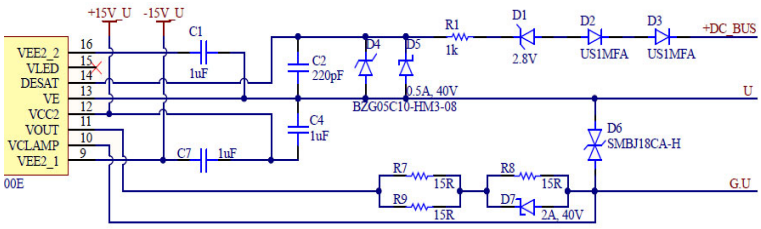
Figure 8: Isolated Gate Driver ACPL-337J Primary Side



4.2.2 Gate Driver Circuit: High-Voltage Side

Figure 9 shows the high-voltage side of the gate driver circuitry. It consists of bypass capacitors, a DESAT protection circuit, and a driver output stage. The DESAT protection circuit is described in Section 4.2.3, Protection Features. The output stage of the ACPL-337J is supplied with +15V and –15V. These voltages are supported with 1-µF bypass capacitors that provide large transient currents that occur during switching transition. The VOUT pin supplies the gate of the IGBT with the necessary voltage and current. In series with this pin, an appropriate gate resistor is added. Selection criteria for the gate resistors is described in Section 4.5, Temperature Measurement. There are three positions on every gate driver where gate resistors are placed. This is done to enable the customer to quickly adjust gate resistance. Also, this circuitry features a turn-off diode that serves to adjust turn-on and turn-off gate resistance separately. Equivalent turn-on gate resistance is defined by two parallel resistors (R7 and R9 in Figure 9) in series with the third resistor (R8 in Figure 9). Similarly, turn-off gate resistance is defined only by two resistors connected in parallel (R7 and R9) because the third is bypassed by the diode (D7 in Figure 9). In case of a faulty power supply or unexpected overvoltage, the TVS diode placed between the gate and the emitter of the IGBT, and it ensures that no damage is done to the IGBT gate structure. Voltage is limited to ± 18V.

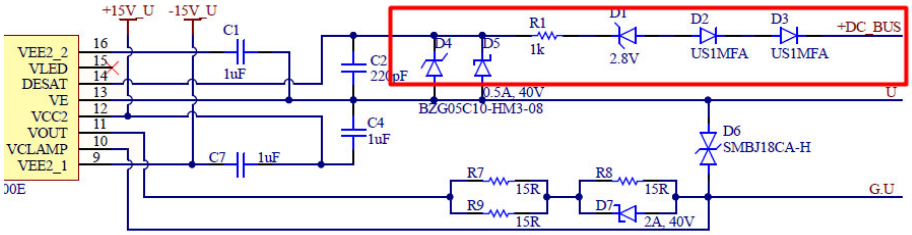
Figure 9: Isolated Gate Driver ACPL-337J High-Voltage Side



4.2.3 Protection Features

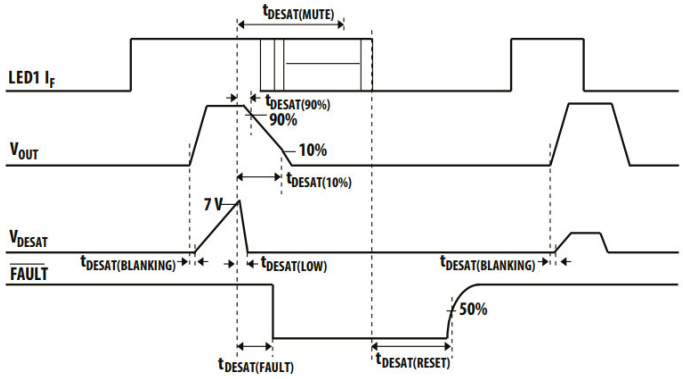
A typical power stage of the three-phase inverter is susceptible to several types of failures, related to the short circuit, which can potentially cause destruction of the IGBT. To prevent damage to the inverter, fault detection must be implemented to turn off the IGBTs in case of an overcurrent event. The ACPL-337J provides an ideal solution combining local desaturation detection and soft shutdown with high-speed current output and high-voltage optical isolation. The DESAT part of the gate circuit is marked with a red rectangle in Figure 10.

Figure 10: DESAT Circuitry at ACPL-337J High-Voltage Side



Fault detection implemented in the ACPL-337J monitors the collector-emitter voltage of the IGBT and triggers a local fault shutdown sequence if the collector-emitter voltage exceeds the predefined threshold. A soft turn-off gate discharge device slowly reduces the IGBT short circuit current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is turned off. During the off state of the IGBT, the fault detection circuitry is disabled to prevent false 'fault' signals. The DESAT fault detection circuitry must remain disabled for a short time period following the turn-on of the IGBT, to allow the collector voltage to fall below the DESAT threshold. This time period, called the DESAT blanking time, is controlled by the internal DESAT charge current, the DESAT voltage threshold, and the external DESAT capacitor. The nominal blanking time is calculated in terms of external capacitance, FAULT threshold voltage (V_{DESAT}), and DESAT charge current (I_{CHG}) in addition to an internal DESAT blanking time ($t_{DESAT(BLANKING)}$). Figure 11 shows a diagram describing the operation of the driver during a DESAT fault condition.

Figure 11: DESAT Protection Sequence. Diagram is the same as in the ACPL-337J data sheet.



The DESAT terminal monitors the voltage between the collector and the emitter (V_{CE}) of the IGBT. When this voltage exceeds 7V, a weak pull-down in the output stage turns on to softly turn off the IGBT. When the gate voltage falls below V_{EE} + 2V, the Miller clamp turns on to clamp the IGBT gate to V_{EE}. After this event, the FAULT output goes low. When $t_{DESAT(MUTE)}$ expires, the LED input needs to be kept low for $t_{DESAT(RESET)}$ before the fault condition is cleared. Afterwards, the FAULT status returns to high. The output stage responds to the input only after the input fault condition has been cleared.

To isolate the collector from the gate driver circuit when the IGBT is off and to be able to adjust the sensed saturation voltage between the collector and the emitter, DESAT diodes (D2 and D3 in Figure 10) are added in the circuit. By changing the forward voltage value of the mentioned diodes, the user can modify threshold level of the saturation voltage. This configuration can be also changed by retaining only one diode and placing a 0Ω resistor in place for the other diode. By increasing the total forward voltage (the sum of the forward voltages of both diodes), the user can decrease the DESAT threshold voltage. When using two diodes instead of one, the same type of diodes must be used, and the blocking voltage rating of these diodes can be half of the maximum reverse voltage. Additionally, the DESAT threshold voltage is adjusted by adding a low-voltage Zener diode (D1 in Figure 10).

When IGBT is switching off, a reverse current flows for a short time, which prevents the diode from achieving its blocking capability until the charge in the junction is depleted. During this time, the positive voltage slope between the collector and the emitter results in current that tends to charge the blanking capacitor. The minimization of this current and the avoidance of false DESAT triggering are achieved with fast diodes. Aside from DESAT and Zener diodes in series, there is one more component that ensures the safety of the driver—a 1-kΩ resistor (R1 in Figure 10) in series with the previous components. This resistor limits the current caused by negative voltage spikes (generated by inductive loads or reverse recovery spikes of the free-wheeling diode) on the DESAT pin, thus preventing damage to the driver. To additionally prevent false fault signals caused by negative voltage spikes on the DESAT pin, connect the Zener and Schottky diode between the DESAT and the V_E pin.

4.2.4 Gate Resistor Consideration

The first step in choosing the appropriate gate resistor is to calculate its minimal value from the $I_{O(PEAK)}$ specification. The IGBT and the gate resistor can be analyzed as a simple RC circuit with a voltage supplied by the ACPL-337J.

$$R_G \geq \frac{V_{CC} - V_{EE}}{I_{O(PEAK)}} - R_{DS(MIN)}$$

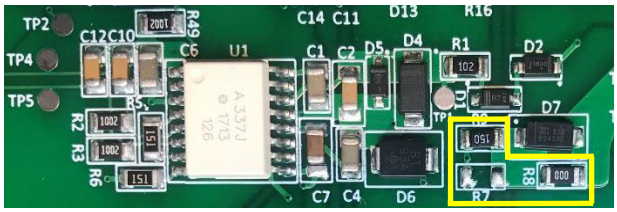
Note that $R_{DS(MIN)}$ can be different for high-side and low-side power switches. Therefore, calculations for both are necessary. This external gate resistor combined with an internal minimal turn-on resistance ensures that the output current does not exceed the device absolute maximum rating of 4A.

The next step in choosing the correct gate resistor is to check the power dissipation of the ACPL-337J gate driver. If the power dissipation is too high, the resistance of the gate resistor should be increased. For detailed instructions on choosing the gate resistor, refer to the ACPL-337J data sheet.

The final step in the turn-off gate resistor selection is ensuring that during turn-off, the transient at the maximal allowed collector current, IGBT collector-emitter voltage does not exceed the blocking voltage on the IGBT device. The criteria for the turn-on gate resistor are the maximal collector current peak, related to the reverse recovery of the opposite freewheeling diode. This peak must not exceed double the value of the nominal collector current.

To ensure the constraints described previously, the EB600-337J comes with a 15Ω gate resistor as a default assembled variant. In addition, the evaluation board is designed to enable Broadcom customers to evaluate switching characteristics of the semiconductors by changing or combining turn-on/turn-off resistors (as described in Section 4.2.2, Gate Driver Circuit: High-Voltage Side). Figure 12 shows the disposition of the gate resistors.

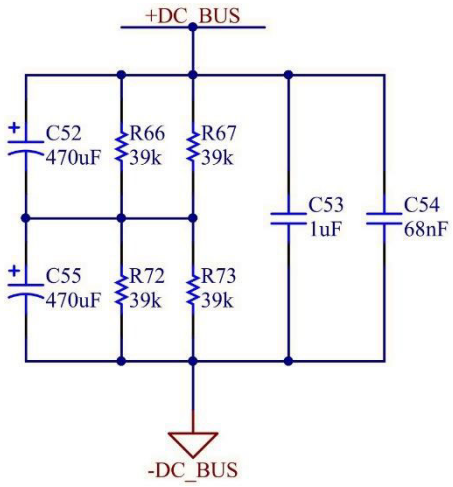
Figure 12: Disposition of the Gate Resistors



4.3 DC Bus and Discharge Resistors

The DC bus capacitor bank on the EB600-337J consists of 2 × 470-µF, 450V electrolytic capacitors in series connection, a 1-µF, 850V film capacitor, and a 68-nF, 1200V ceramic capacitor, as shown in Figure 13. These components are added to the design to simplify the evaluation of the gate driver and the semiconductor switching characteristics and to provide a high-quality DC bus for full inverter utilization. For an appropriate voltage sharing on series-connected electrolytic capacitors and safety discharging purposes, two ceramic 39-kΩ resistors are connected in parallel to each electrolytic capacitor (Figure 13).

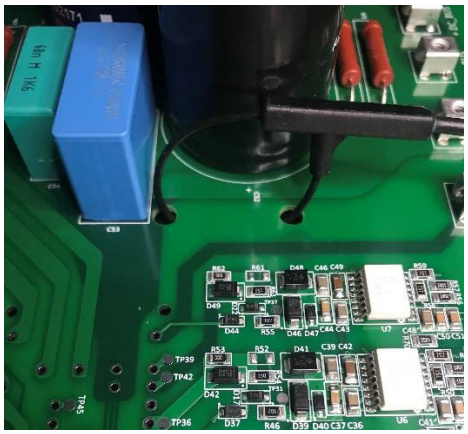
Figure 13: Disposition of the Gate Resistors



4.4 IGBT Current Measurement

To enable users to obtain a semiconductor current waveform during switching instances, the board is designed with two dedicated holes mechanically positioned to cover the traces connecting the low-side emitters and the negative potential of the DC bus capacitors, as shown in Figure 14. Holes with ϕ = 5 mm enable using a Rogowski current probe for current measurement purposes.

Figure 14: Dedicated Holes Enable Users to Measure the Current of the Single IGBT



4.5 Temperature Measurement

The EB600-337J contains the temperature measurement circuit shown in Figure 15. The voltage drop on the PIM's negative temperature coefficient (NTC) thermistor is amplified using an ACPL-C87A isolated linear optocoupler and additionally buffered using an operation amplifier. Figure 16 shows the typical temperature response of the measurement circuit. Note that the output voltage range can be adjusted by changing the value of the feedback resistor R4 as well as resistors R31 and R40 in the amplifier circuit.

Figure 15: EB600-337J Isolated Temperature Measurement Circuit

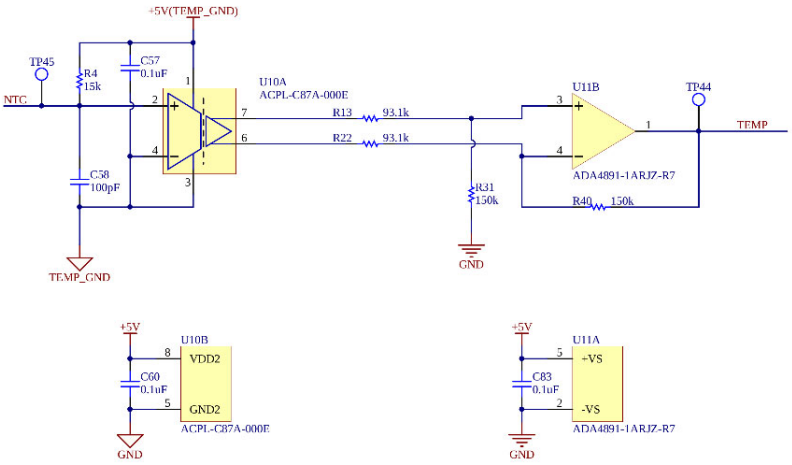
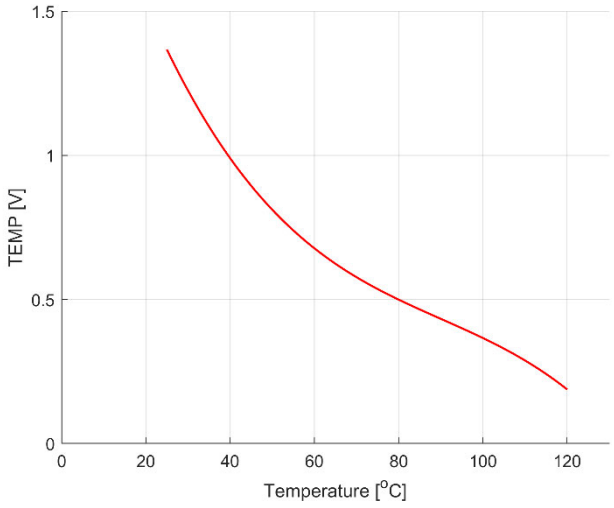


Figure 16: Typical Temperature Measurement Characteristic



Chapter 5: Setup

WARNING! The EB600-337J board is designed to work with up to 300V and thus requires that all safety precautions and national accident prevention rules must be undertaken and observed by skilled technical personnel, related to a board installation, use, and maintenance. There is a danger of serious injury and damage of property if the board is improperly used or installed. It is strongly recommended that a system aimed to supply the evaluation board is equipped with control and protection devices, in agreement with the applicable safety standards.

5.1 Installation of the EB600-337J

Before evaluating the board, perform these installation steps:

1. Before any installation, make a visual inspection of the board to make sure it contains all components assembled except the PIM module. See Section A.3, BOM, for the list of components. The EB600-337J, by default, does not contain an assembled PIM module to avoid damage of the module and the evaluation board during transport, as well as to provide the customer an option to use other modules with the same footprint.
2. Ground the board. Connect the –DC_BUS terminal to earth potential.
3. Connect the signal connector. The PWM signals as well as the ACPL-337J output fault signals can be connected to any control board with 5V/3.3V logic.
4. Connect a 24V external power supply. The EB600-337J requests a 24V external power supply to enable 5V digital operations and a ±15V gate driver high-voltage side power supply. Although the polarity is marked, the board is reverse protected regarding the 24V external.
5. Turn on power to the board by performing these steps:
   – Case 1, with DC voltage:
     a. Connect the DC power supply on terminals +DC_BUS and –DC_BUS.
   – Case 2, with three-phase AC voltage:
     a. Use terminals N_REC and –DC_BUS to connect the external pre-charge circuit.

NOTE: **Precautions:** Due to technical requirements, the evaluation board does not comprise a pre-charge circuit that enables soft DC bus charging. In the case that the three-phase autotransformer is not used, an external pre-charge circuit must be installed to avoid DC bus capacitor failure, which would cause injury and damage to property.

b. Use terminals L1, L2, and L3 to connect the three-phase AC power supply.

ATTENTION: The maximum allowed input AC voltage is 240V.

5.2 Evaluation of the EB600-337J

The EB600-337J enables users to evaluate the following items:

- ACPL-337J driver features
- ACPL-C87A voltage sensor features
- Switching characteristics of the semiconductors within the PIM module
- Inverter basic features

To evaluate semiconductor switching characteristics with the EB600-337J, perform a double pulse test, and measure the transients related to the semiconductor and the ACPL-337J driver circuit.

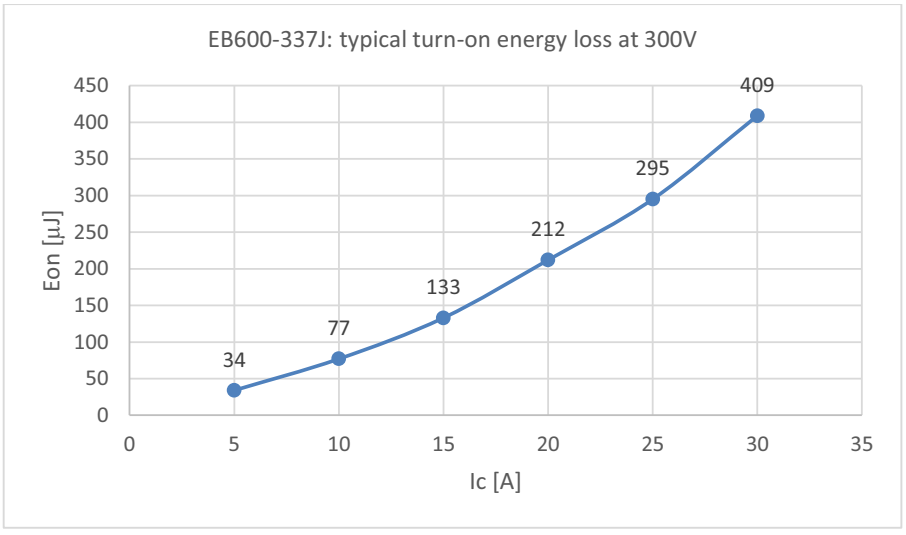
Chapter 6: Typical Switching and DESAT Protection Characteristics

6.1 Typical Switching Losses

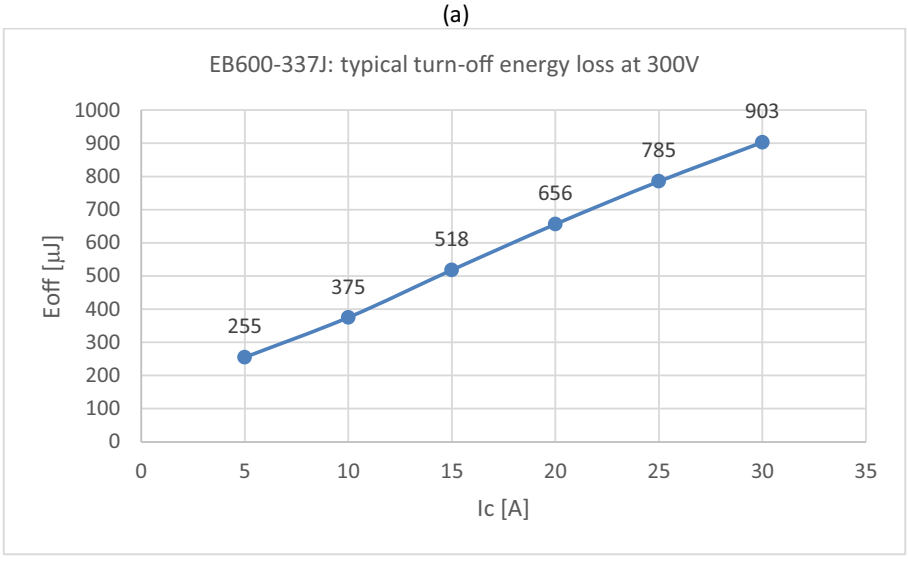
Because the EB600-337J has integrated a DC bus capacitor bank, the worst-case commutation inductance (measured for the switch with the longest path to the DC bus capacitors) is a constant 47 nH and does not vary from the setup used to characterize switching characteristic, but only from an assembled PIM.

As an example, Figure 17 shows the obtained turn-on and turn-off losses at 25°C for PIM FP50R06KT4G.

Figure 17: (a) Turn-On (E_{on}) and (b) Turn-Off (E_{off}) Switching Energy



(a)



(b)

6.2 Typical Switching Waveforms

Switching waveforms during hard switching of the semiconductors are measured with an oscilloscope using the standard double-pulse test procedure. Figure 18 shows the turn-on switching transient, while in Figure 19, the turn-off switching transient is depicted.

Figure 18: Oscilloscope Screenshot of Turn-On Transient, V_{dc} = 300V, I_c = 30A, CH1 (Yellow) V_{ce}, CH3 (Blue) V_{ge}, CH4 (Green) V_{dc}, F6 (Red) I_c

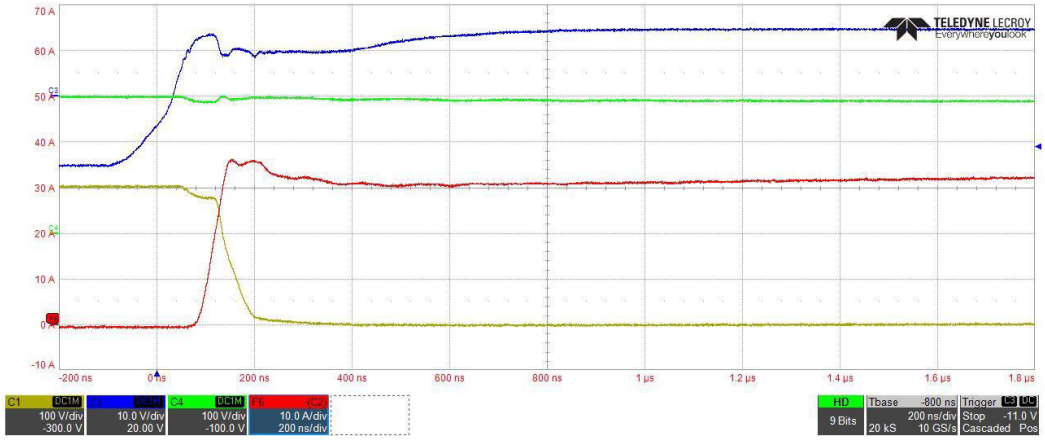
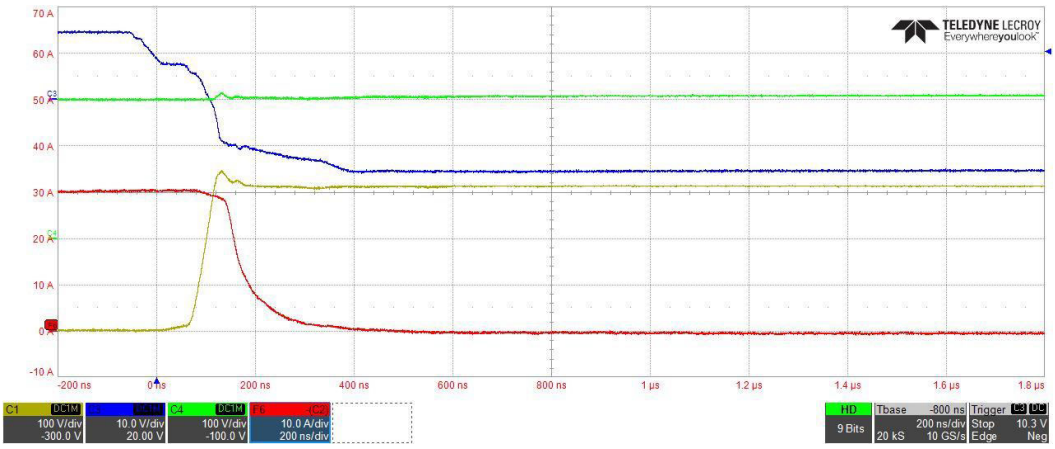


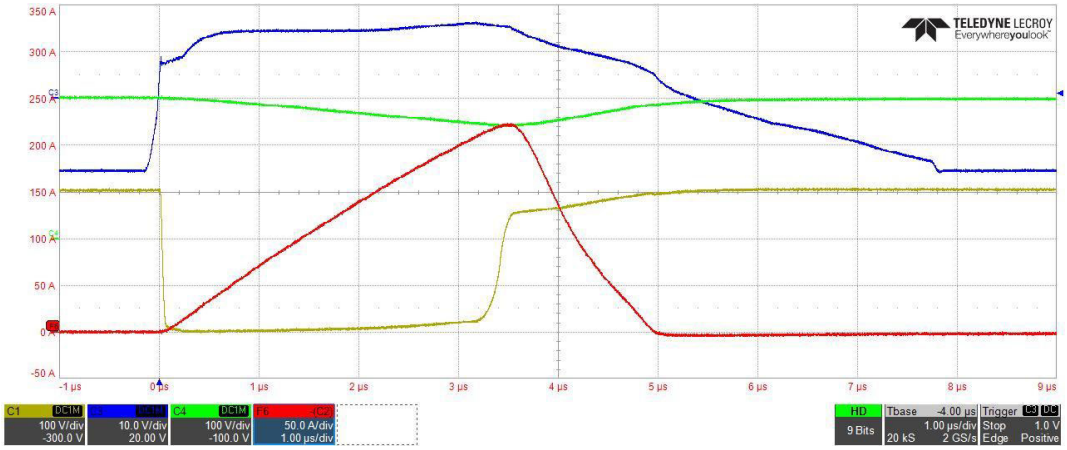
Figure 19: Oscilloscope Screenshot of Turn-Off Transient, V_{dc} = 300V, I_c = 30A, CH1 (Yellow) V_{ce}, CH3 (Blue) V_{ge}, CH4 (Green) V_{dc}, F6 (Red) I_c



6.3 Typical DESAT Protection Performance

The functioning of the DESAT protection is obtained by performing the direct short circuit on one of the bridge legs. Figure 20 shows the results of this measurement.

Figure 20: Measurement Results from DESAT Detection, Direct Short Circuit at V_{dc} = 300V, CH1 (Yellow) V_{ce}, CH3 (Blue) V_{ge}, CH4 (Green) V_{dc}, F6 (Red) I_c



Appendix A: Schematics, Layout, and BOM

This appendix includes full schematics, layout, and bill of materials of the EB600-337J. This information helps customers to modify, copy, and qualify the design for production, according to specific requirements.

A.1 Schematics

Figure 21: EB600-337J Top-Level Sheet

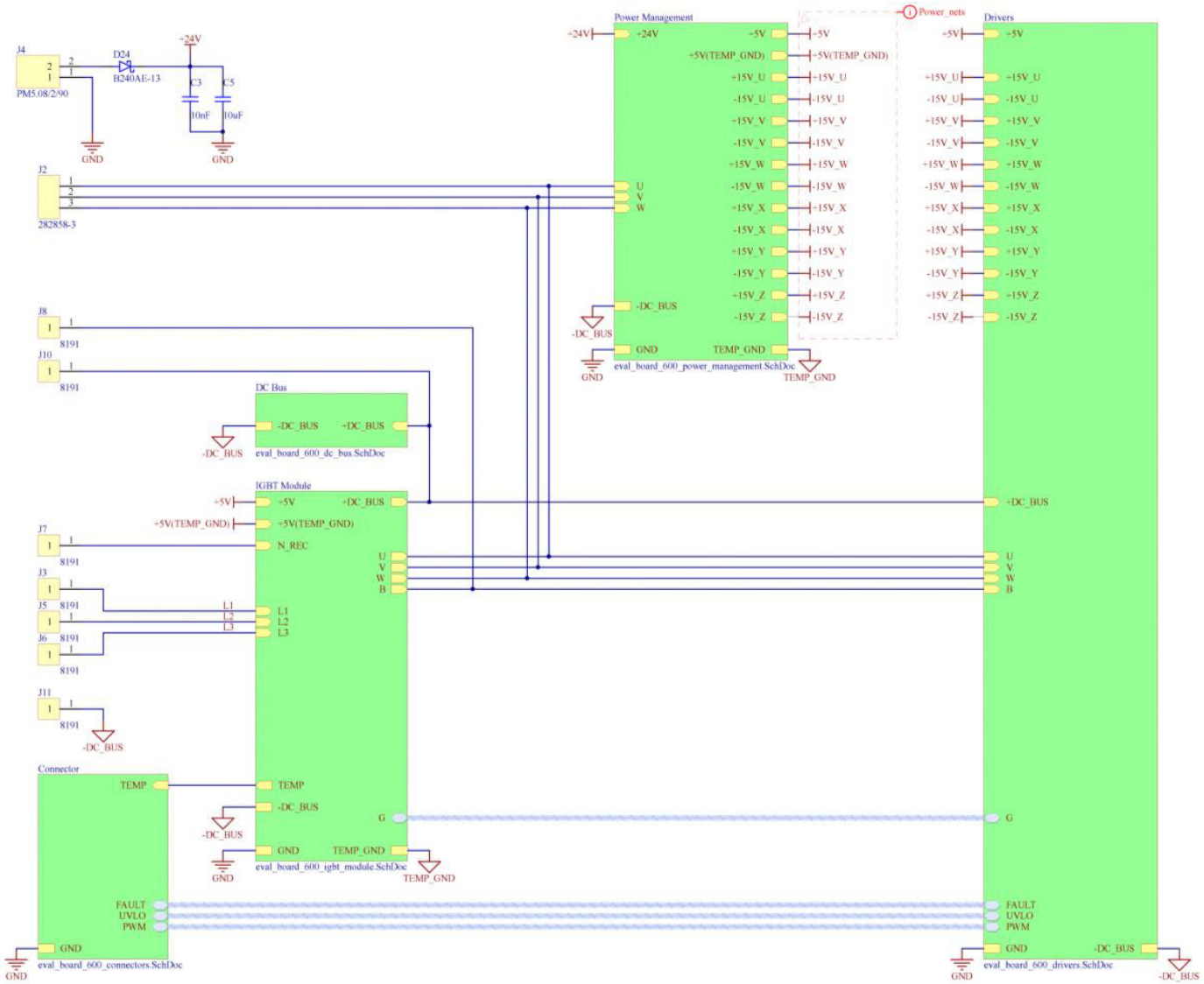


Figure 22: EB600-337J, Sheet 1, Connector

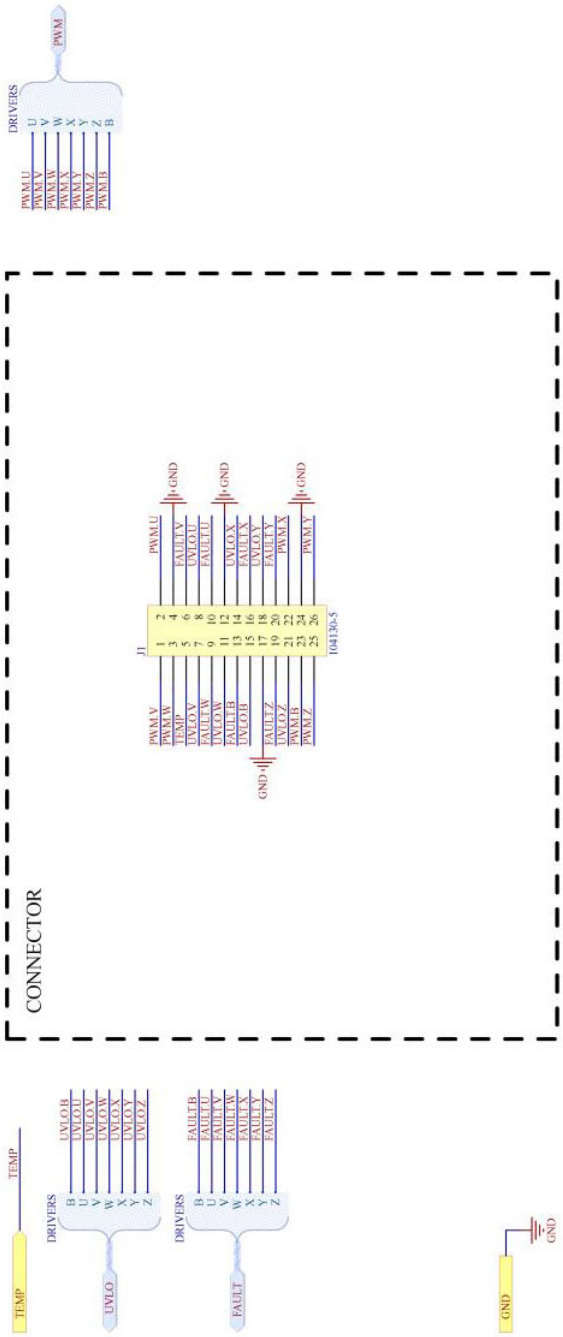


Figure 23: EB600-337J, Sheet 2, DC Bus

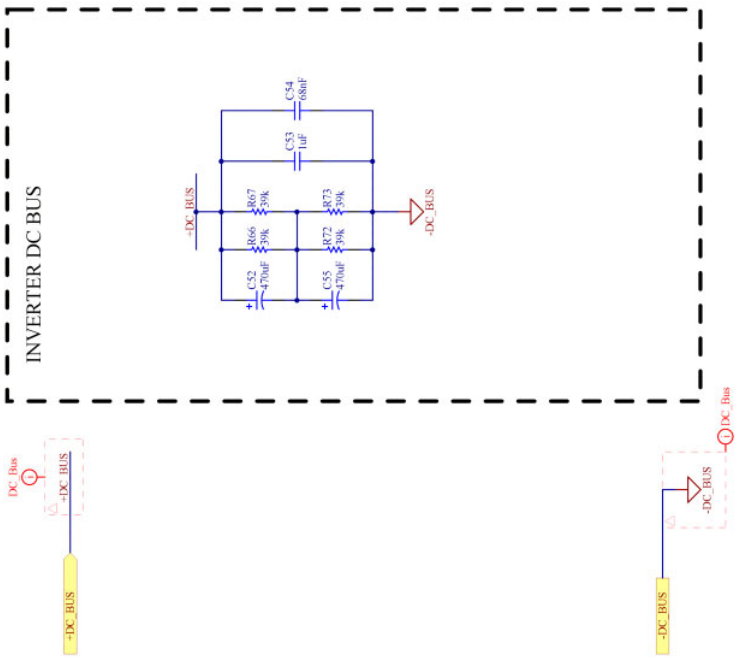


Figure 24: EB600-337J, Sheet 3, Drivers

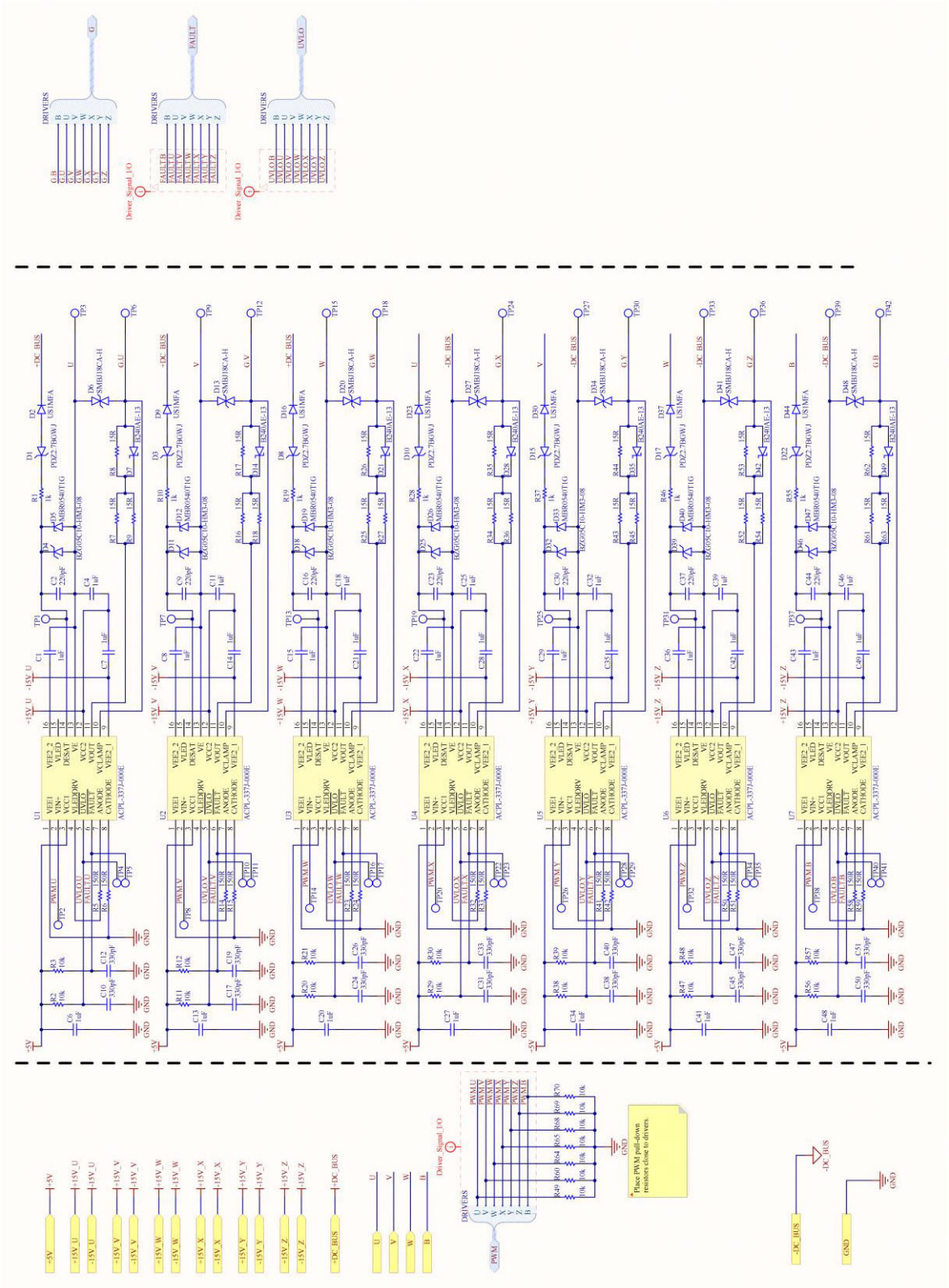


Figure 25: EB600-337J, Sheet 4, IGBT Module

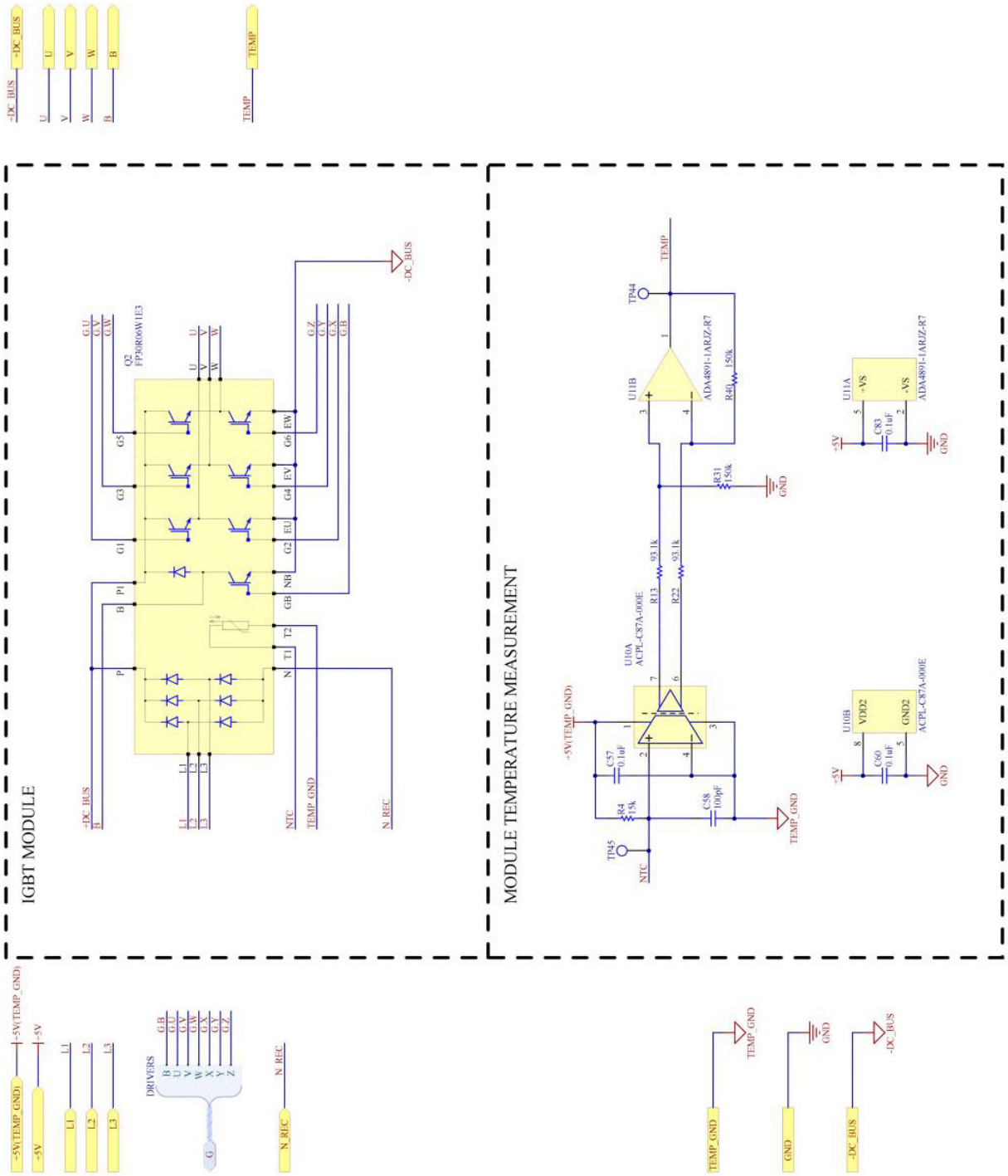
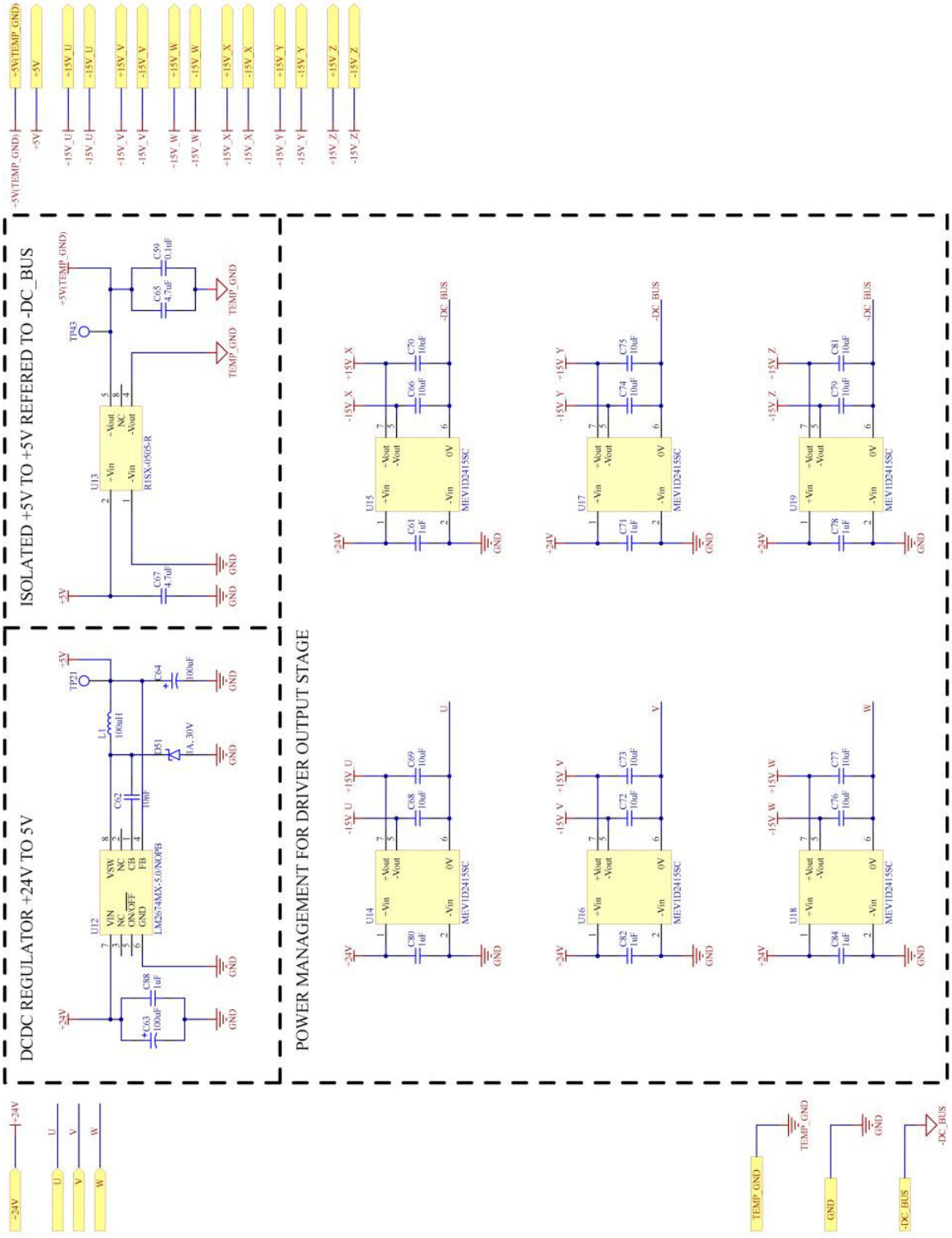


Figure 26: EB600-337J, Sheet 5, Power Management



A.2 Layout

Figure 27: EB600-337J, Assembly Drawing

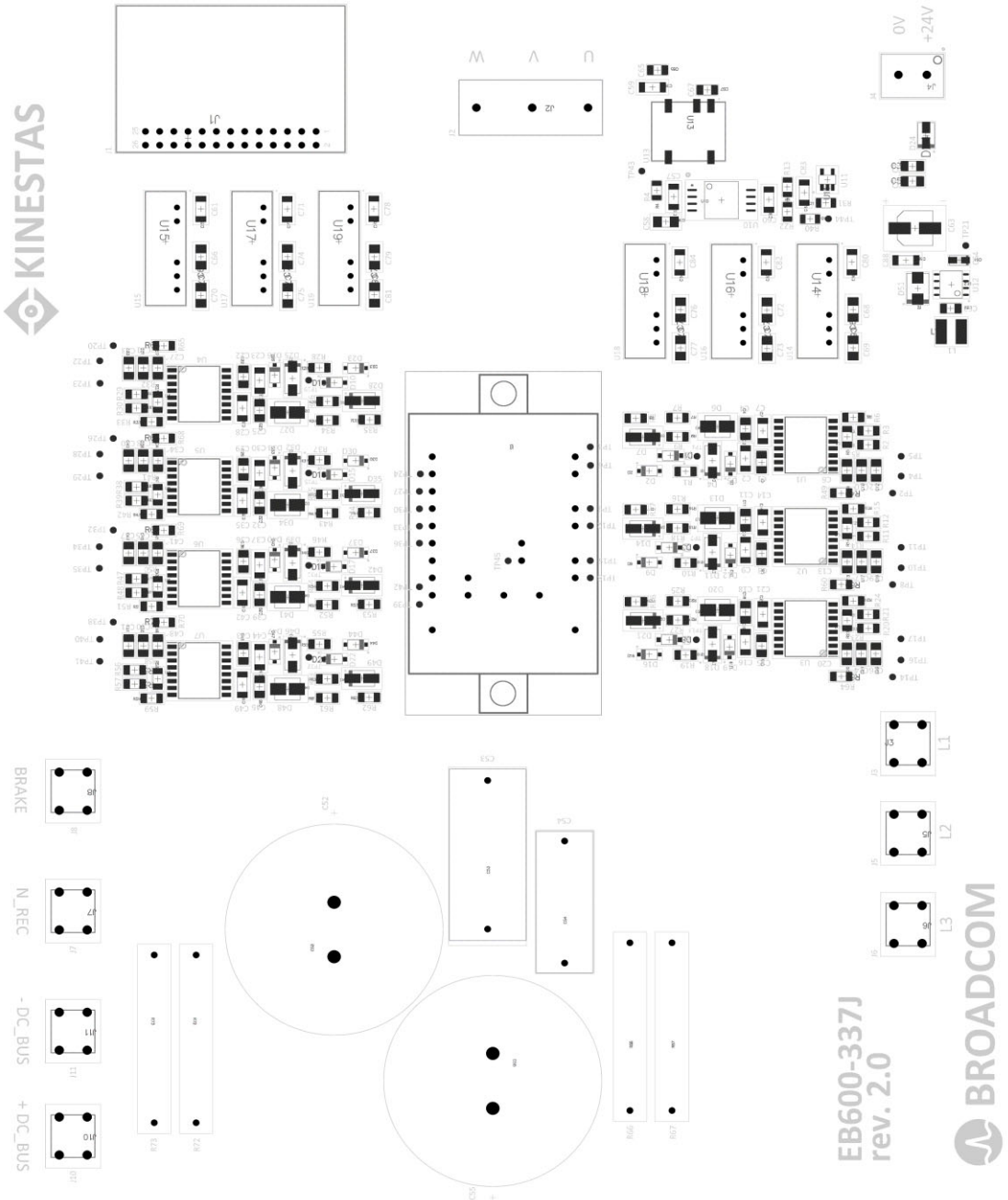


Figure 28: EB600-337J, Top Layer

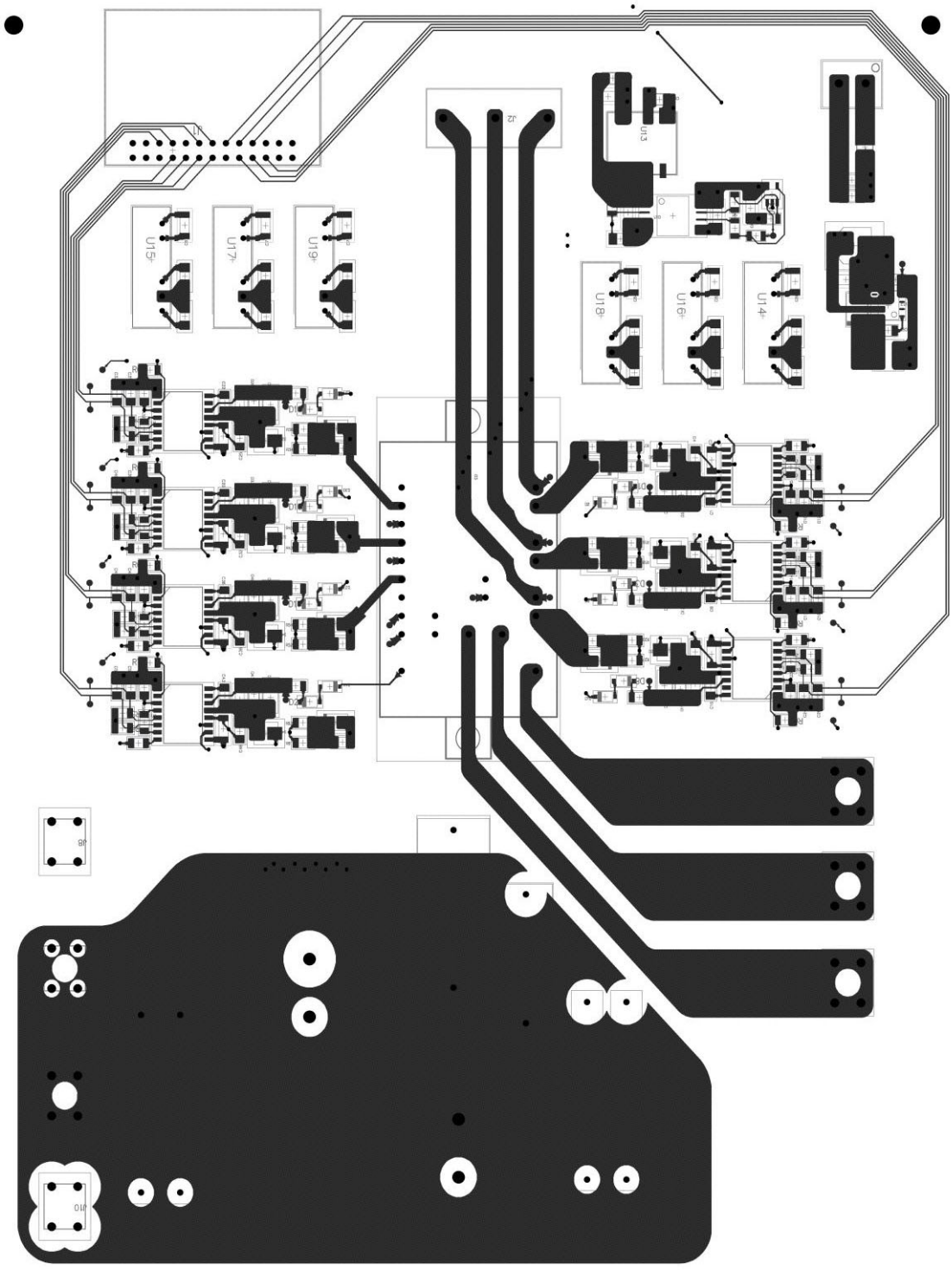


Figure 29: EB600-337J, Signal Layer 1

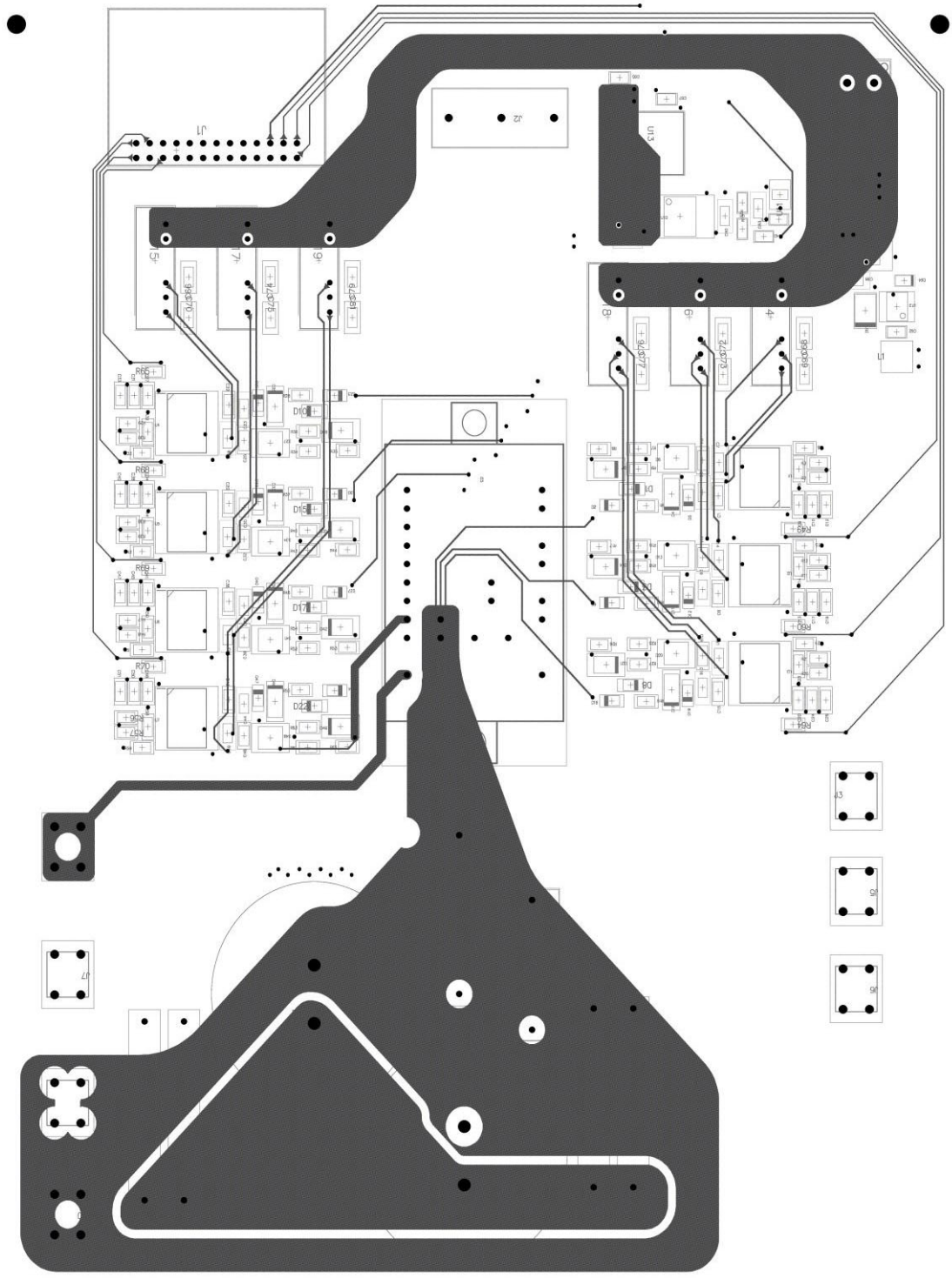


Figure 30: EB600-337J, Signal Layer 2

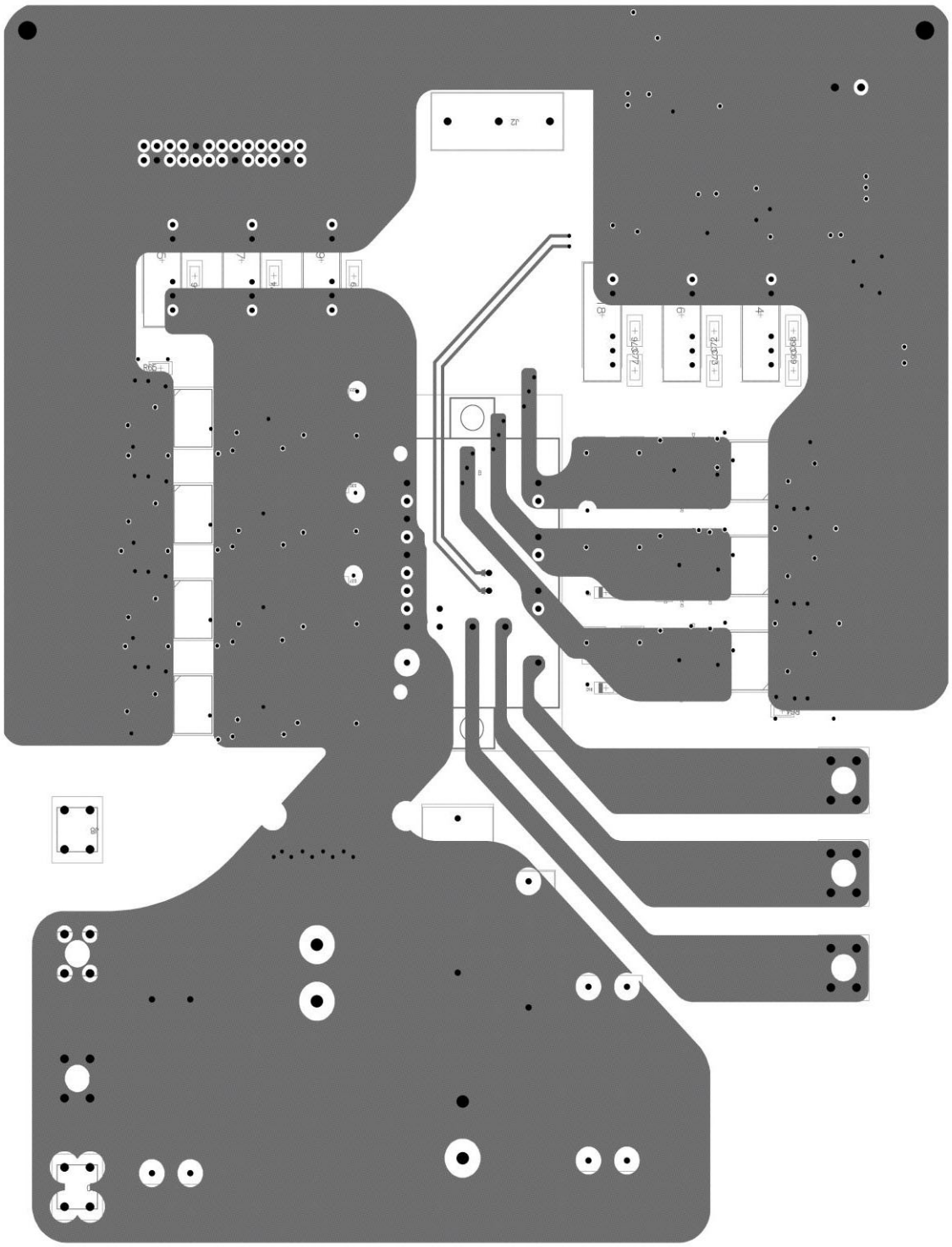
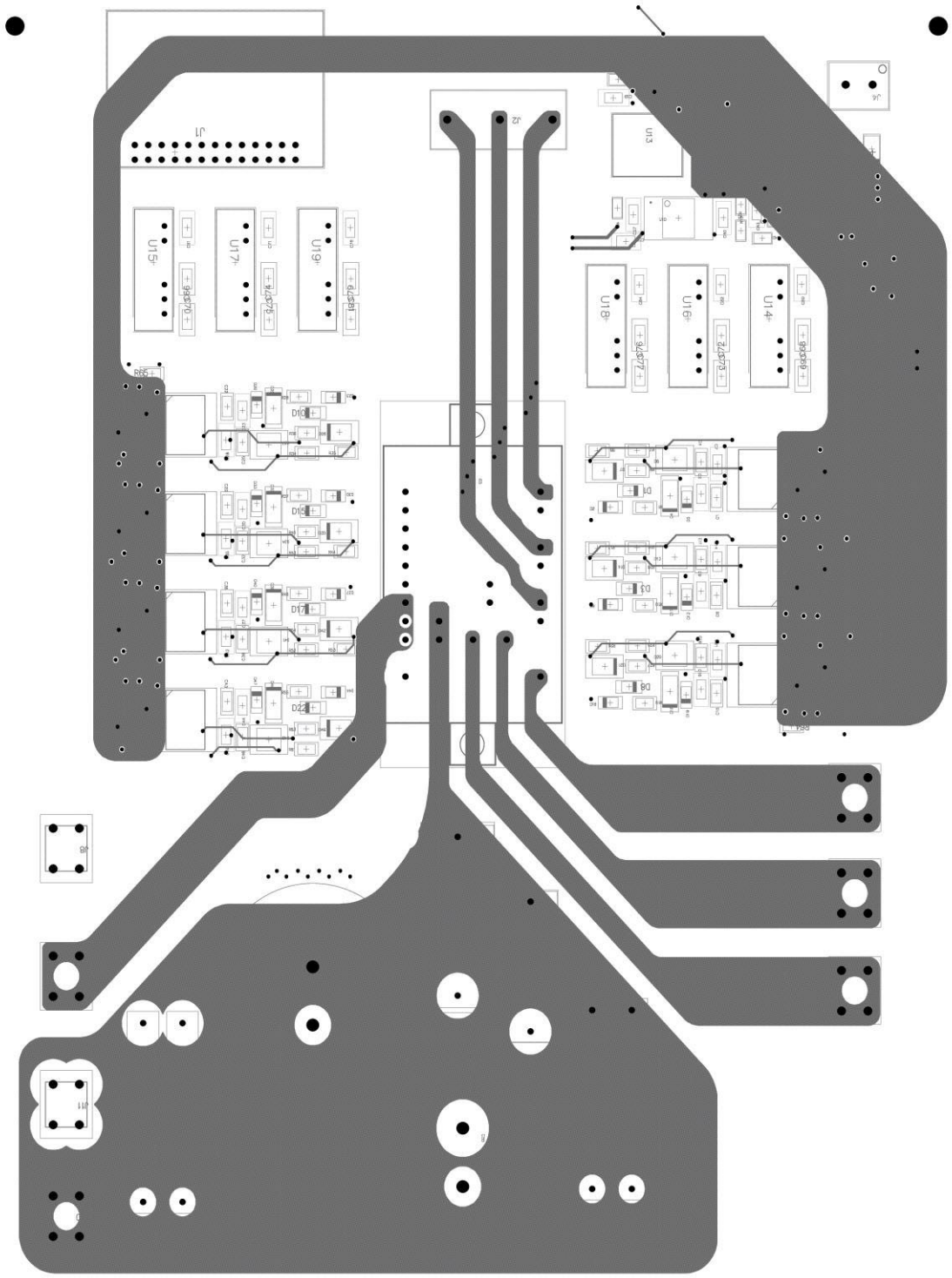


Figure 31: EB600-337J, Bottom Layer



A.3 BOM

Table 5 shows the bill of materials for the EB600-337J.

Table 5: Bill of Materials for the EB600-337J

Designator	Manufacturer Part Number
C1, C4, C6, C8, C11, C13, C15, C18, C20, C22, C25, C27, C29, C32, C34, C36, C39, C41, C43, C46, C48	VJ1206Y105MXJTW1BC
C2, C9, C16, C23, C30, C37, C44	885012208071
C3, C62	VJ1206Y103JXAMC
C5	GMK316BJ106KL-T
C7, C14, C21, C28, C35, C42, C49, C61, C71, C78, C80, C82, C84, C88	CC1206ZRY5V9BB105
C10, C12, C17, C19, C24, C26, C31, C33, C38, C40, C45, C47, C50, C51	VJ1206A331KXQPW1BC
C52, C55	ALA7DA471DE500
C53	B32674D8105K
C54	F462DO683M1K6Z
C57, C59, C60, C83	VJ1206Y104JXQCW1BC
C58	VJ1206A101JXQCW1BC
C63	EEE-FT1V101AP
C64	TLJA107M010R1400
C65, C67	885012208017
C66, C68, C69, C70, C72, C73, C74, C75, C76, C77, C79, C81	TMK316BJ106KL-T
D1, D3, D8, D10, D15, D17, D22	PDZ2.7BGWJ
D2, D9, D16, D23, D30, D37, D44	US1MFA
D4, D11, D18, D25, D32, D39, D46	BZG05C10-HM3-08
D5, D12, D19, D26, D33, D40, D47	MBR0540T1G
D6, D13, D20, D27, D34, D41, D48	SMBJ18CAHE3/52
D7, D14, D21, D24, D28, D35, D42, D49	B240AE-13
D51	MBRS130LT3G
J1	104130-5
J2	282858-3
J3, J5, J6, J7, J8, J10, J11	8191
J4	PM5.08/2/90
L1	VLS5045EX-101M
Q2	FP30R06W1E3
R1, R10, R19, R28, R37, R46, R55	CRCW12061K00JNEA
R2, R3, R11, R12, R20, R21, R29, R30, R38, R39, R47, R48, R49, R56, R57, R60, R64, R65, R68, R69, R70	CRCW120610K0FKEAC
R4	RCG120615K0FKEA
R5, R6, R14, R15, R23, R24, R32, R33, R41, R42, R50, R51, R58, R59	CR1206-JW-151ELF
R7, R8, R9, R16, R17, R18, R25, R26, R27, R34, R35, R36, R43, R44, R45, R52, R53, R54, R61, R62, R63	CRCW120615R0JNEA
R13, R22	CRCW120693K1FKEA
R31, R40	CRCW1206150KFKEA
R66, R67, R72, R73	HPC2C393K
U1, U2, U3, U4, U5, U6, U7	ACPL-337J-000E

Table 5: Bill of Materials for the EB600-337J (Continued)

Designator	Manufacturer Part Number
U10	ACPL-C87A-000E
U11	ADA4891-1ARJZ-R7
U12	LM2674MX-5.0/NOPB
U13	R1SX-0505-R
U14, U15, U16, U17, U18, U19	MEV1D2415SC

A.4 Disclaimer

THIS APPLICATION NOTE CONTAINS INFORMATION THAT SHOULD SERVE ONLY AS A FIRST STEP FOR EVALUATION AND IMPLEMENTATION OF THE BROADCOM INC. TECHNOLOGIES. KINESTAS DOO DOES NOT TAKE RESPONSIBILITY FOR USING AND IMPLEMENTING BROADCOM TECHNOLOGIES IN OTHER DESIGNS.

Revision History

Version 1.0, October 2, 2019

- Initial release of the document.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