Application Note

AEAT-8811-Q24

Magnetic Encoder IC: 10-Bit to 16-Bit Programmable Angular Magnetic Encoder with No Offset Calibration

Overview

AEAT-8811-Q24 is a CMOS magnetic sensor structure that is suitable for contactless 360° encoding based on the Hall effect. It provides an angle output up to 16 bits of resolution and simultaneous incremental output of up to 4096 CPR. An integrated Hall structure at the core of the device uses a single 2-pole disc magnet to convert the magnetic field vector in the chip plane into an AC signal whose amplitude and phase correspond to the magnitude and direction of the field.

An internal digital signal-processing unit then processes and conditions the raw AC signal from the sensor. The output signals are available in three different forms:

- Pulse-width modulation (PWM)
- Absolute 16-bit position through the 3 wire or 2 wire Serial Synchronous Interface (SSI)
- Incremental output (ABI and UVW signals)

These features can be programmed by configuring the internal registers in program mode.

More information about the AEAT-8811-Q24 product specifications is available in the product data sheet.

Operation Mode

The AEAT-8811-Q24 features two types of operational modes: normal operation mode and one-time programming (OTP) mode.

Normal Operation Mode

Normal mode is the normal operating mode of the chip. The absolute output (10-bit, 12-bit, 14-bit, or 16-bit absolute position data) is available through SSI pins (DO, CLK, and NCS). The following are the output signal conditions during AEAT-8811-Q24 initialization:

- PWM signals all 0s.
- ABI signals all 1s.
- UVW signals all 0s.

The incremental positions are indicated on ABI and UVW signals with user-configurable CPR 32, 50, 64, 100, 128, 256, 200, 400, 512, 800, 1000, 1024, 2000, 2048, 4000, and 4096 of ABI signals and pole pairs from 1 to 8 (2 to 16 poles) for UVW commutation signals.

Figure 2 shows the recommended circuit diagram for AEAT-8811-Q24.

OTP Programming Mode

AEAT-8811-Q24 is an OTP ASIC. OTP registers are 0 by default.

During OTP programming, the VDD voltage is recommended to be at the minimum of 5.5V, typical of 5.6V, and maximum of 5.7V.

Programming of AEAT-8811-Q24 can be performed with the HEDS-8999 programming kit or any tester/programmer device using the guidelines provided.

Figure 2 shows the recommended circuit diagram for AEAT-8811-Q24.

Absolute and Incremental Programming

The absolute resolution can be set to 10, 12, 14, or 16 bits. For incremental selection, ABI or UVW can be selected by following the instructions in the following sections. The PWM output is available as well.

The OTP shadow registers are programmable using the SPI protocol. Writing specific commands to specific addresses of the internal registers will program values of OTP shadow registers to OTP permanently.

Memory Map

The Broadcom AEAT-8811-Q24 uses nonvolatile OTP as shown in the tables that follow.

The memory is separated into 8 bits per address. During OTP programming, the VDD voltage is recommended at a minimum of 5.5V, typical of 5.6V, and maximum of 5.7V.

Nonvolatile Register (OTP)

1. OTP is one-time programmable only. Any OTP bit with a value of 0 can be written to 1, but not vice versa. Do not program 1 to the same address bit twice.
2. OTP shadow registers are volatile registers that are loaded with corresponding OTP values after power-on.
3. All bits (except addresses 0x00–0x03 and 0x10–0x12) are in LOCK mode by default after power-on. To enter UNLOCK mode (to be able to write to the OTP shadow registers or registers), write 0xAB to address 0x10.
4. In UNLOCK mode, you may write to any OTP shadow registers or registers. Values written will remain until power-off.
5. The UNLOCK state is maintained until the power supply is turned off or any value (except 0xAB) is written to address 0x10.
6. All OTP memory is programmable by writing only the appropriate commands to addresses 0x11–0x13 and 0x1B (see Programming Customer Reserved OTP and Programming User Configuration OTP).

OTP Shadow Registers

1. OTP shadow registers are volatile (upon power-up, reload values from OTP) and are not written to OTP automatically.
2. To write OTP shadow registers values to OTP (nonvolatile) memory, see Programming Customer Reserved OTP and Programming User Configuration OTP.
3. The OTP shadow registers will be from address 0x00 to address 0x0D.

The tables that follow show the registers.

Customer Reserve and Zero Reset Registers

Address	Bit(s)	Name	Description	Default
0x00	[7:0]	Customer Reserve 0	User programmable	8'h0
0x01	[7:0]	Customer Reserve 1	User programmable	8'h0
0x02	[7:0]	Zero Reset0	Zero Reset Position [7:0]	8'h0
0x03	[7:0]	Zero Reset1	Zero Reset Position [15:8]	8'h0

Customer Configuration Registers

These registers are required to be unlocked, which is done by writing 8'hAB to address 0x10 and then writing to the OTP shadow register.

Table 1: Customer Configuration 0 Registers

Address	Bit(s)	Name	Description	Default
0x04	[7]	UVW Select	1: Select UVW mode 0: Select PWM mode	0
	[6:5]	Reserved	00: Reserved factory	00
	[4:3]	I-width Setting	11: (ABI) I-width = 360 electrical deg (e.deg) 10: (ABI) I-width = 270 electrical deg (e.deg) 01: (ABI) I-width = 180 electrical deg (e.deg) 00: (ABI) I-width = 90 electrical deg (e.deg)	00
	[2:0]	UVW/PWM Setting[a]	111: UVW = 2 pole pairs / PWM period = 2049 µs 110: UVW = 1 pole pairs / PWM period = 1025 µs 101: UVW = 8 pole pairs / PWM period = 8193 µs 100: UVW = 7 pole pairs / PWM period = 4097 µs 011: UVW = 6 pole pairs / PWM period = 2049 µs 010: UVW = 5 pole pairs / PWM period = 1025 µs 001: UVW = 4 pole pairs / PWM period = 8193 µs 000: UVW = 3 pole pairs / PWM period = 4097 µs	000

a. Set UVW Select to 1 to set UVW Setting and 0 to set PWM Setting.

Table 2: Customer Configuration 1 Registers

Address	Bit(s)	Name	Description	Default
0x05	[7]	Reserve	0: Reserved factory	0
	[6:3]	CPR Setting1	1111: (ABI) 0512 CPR 1110: (ABI) 0256 CPR 1101: (ABI) 0128 CPR 1100: (ABI) 0064 CPR 1011: (ABI) 0032 CPR 1010: (ABI) 4000 CPR 1001: (ABI) 2000 CPR 1000: (ABI) 1000 CPR 0111: (ABI) 0800 CPR 0110: (ABI) 0400 CPR 0101: (ABI) 0200 CPR 0100: (ABI) 0100 CPR 0011: (ABI) 0050 CPR 0010: (ABI) 4096 CPR 0001: (ABI) 2048 CPR 0000: (ABI) 1024 CPR	0000
	[2:0]	Hysteresis Setting	111: 0.18 mechanical degree (mº) 110: 0.08 mechanical degree (mº) 101: 0.04 mechanical degree (mº) 100: 0.02 mechanical degree (mº) 011: 0.01 mechanical degree (mº) 010: 0.00 mechanical degree (mº) 001: 0.70 mechanical degree (mº) 000: 0.35 mechanical degree (mº)	000

Table 3: Customer Configuration 2 Registers (Read the Important Notes Highlighted in the Table)

Address	Bit(s)	Name	Description	Default
0x06	[7]	Dir[a]	1: Count up in a counterclockwise rotation 0: Count up in a clockwise rotation	0
	[6]	Zero Latency Mode[b]	1: Zero latency is ON 0: Zero latency is OFF	0
	[5:4]	Absolute Resolution	11: 14-b absolute resolution (SSI) 10: 16-b absolute resolution (SSI) 01: 10-b absolute resolution (SSI) 00: 12-b absolute resolution (SSI)	0
	[3]	SSI Select	1: Data 1st clock edge[c] 0: Default	0
	[2:0]	CPR Setting2[d]	111: 32, 64, 128, 256, 50, 100, 200, 400 CPR 011: 2048, 4096, 2000, 4000 CPR 001: 512, 1024, 800, 1000 CPR[e] 000: 512, 1024, 800, 1000 CPR	000

a. See Figure 1 for the direction definition.

b. When Zero Latency Mode is ON, the user must set CPR setting 2 in 0x06 to 010 for all the applicable CPR (32–4096).

c. Initial Data Output tri-state.

d. Incremental: The CPR setting 1 in address 0x05 must match the CPR setting 2 in 0x06.
Absolute: For absolute only application, set CPR setting 2 in 0x06 to 010.

e. For better dynamic performance, a higher latency setting is required.

Programming Customer Reserved OTP

Perform the following steps to program Customer Reserved OTP shadow registers to OTP.

1. Write the desired values to the Customer Reserved OTP shadow registers (0x00–0x01).
2. Read back the Customer Reserved OTP shadow registers (0x00–0x01) to confirm that the correct values are stored.
3. Write 8'hA1 to address 0x11 to program the Customer Reserved OTP shadow registers (0x00–0x01) to OTP.
4. Perform a power supply cycle (power off and power on) and read back the Customer Reserved OTP shadow registers (0x00–0x01) to confirm that the correct values are stored into OTP.

Programming User Configuration OTP

Perform the following steps to program User Configuration OTP shadow registers to OTP.

1. Write the desired values to the User Configuration OTP shadow registers (0x04–0x06).
2. Read back the User Configuration OTP shadow registers (0x04–0x06) to confirm that the correct values are stored.
3. Write 8'hA3 to address 0x13 to program the User Configuration OTP shadow registers (0x04–0x06) to OTP.
4. Perform a power supply cycle (power off and power on) and read back the User Configuration OTP shadow registers (0x04–0x06) to confirm that the correct values are stored into OTP.

Zero Reset

Zero Reset Programming

AEAT-8811-Q24 allows users to configure a zero reset position. This value is stored at OTP 0x02 (lower 8-b) and 0x03 (upper 8-b). To set to the zero reset position, for example, position X, use a procedure similar to the following.

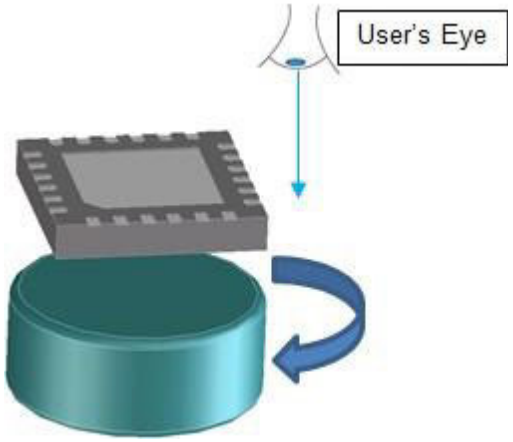
NOTE: You should decide the desired direction or orientation (as outlined in Figure 1) before setting the zero reset position.

1. Stop the motor at position X.
2. Read the 16-b value of position X using the SSI protocol (for example, read 16'hABCD).
3. Write the lower 8-b (from the preceding example, 8'hCD) to the OTP shadow registers 0x02 using SPI.
4. Write the upper 8-b (from the preceding example, 8'hAB) to the OTP shadow registers 0x03 using SPI.
5. Confirm that the correct zero reset value is written to the OTP shadow registers by rereading the motor position value using SSI. Make sure that the current position read is 16'h0000 (excluding step jumps incurred by noise).
6. To permanently save this zero reset value, write 8'hA2 to internal registers 0x12.
7. Power-cycle (power off and power on) the chip.
8. Confirm that the correct zero reset value is written to OTP by rereading the motor position value using SSI. Make sure that the current position read is 16'h0000 (excluding the step jumps incurred by noise).

Direction

The direction must be defined to count up clockwise or counterclockwise per rotation. Per the default setting, if the magnet is spinning at a clockwise position, based on the user's line of sight as shown in Figure 1, AEAT-8811-Q24 counts up.

Figure 1: Direction Definition When Magnet Rotates



Safety Alarm

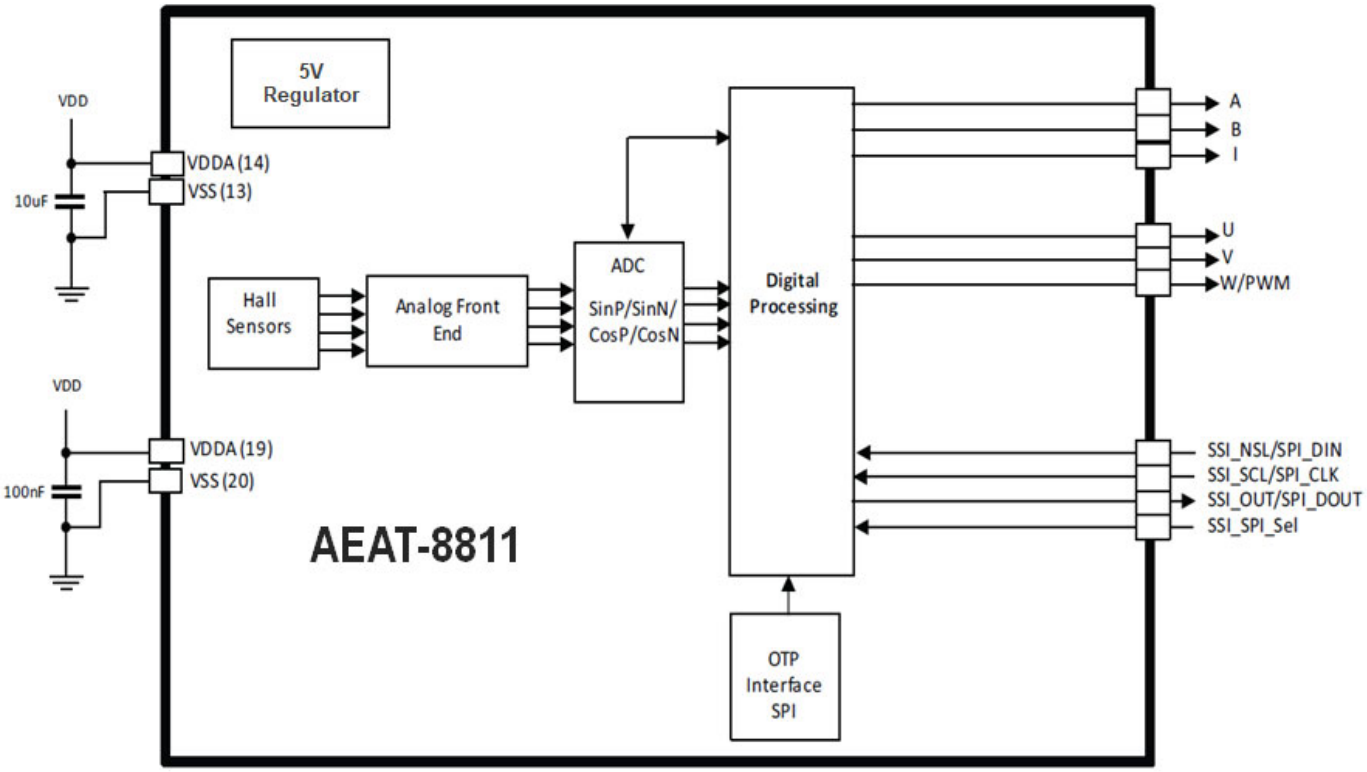
AEAT-8811-Q24 provides following safety alarms:

- Magnet High (MHI) error: This error indicates that the magnet strength detected by the chip is too strong. When this is consistently flagged as high, change to a weaker magnet, or increase the distance between the chip and the magnet.
- Magnet Low (MLO) error: This error indicates that the magnet strength detected by the chip is too weak. When this is consistently flagged as high, change to a stronger magnet, or decrease the distance between the chip and the magnet.

These alarms are read out from SSI interface as described in the "Absolute Output Format" section of the data sheet.

AEAT-8811-Q24 Circuit Diagram

Figure 2: Recommended Circuit Diagram for AEAT-8811-Q24 during Normal Operation and OTP Programming



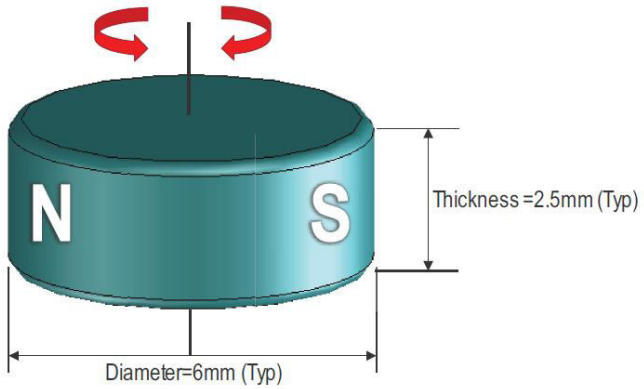
NOTE:

- For OTP programming, refer to the "Programming the AEAT-8811-Q24" section in the data sheet.
- Connect the 10-µF and 100-nF capacitors as close to the individually assigned power and ground pins as possible.

Recommended Magnetic Input Specifications

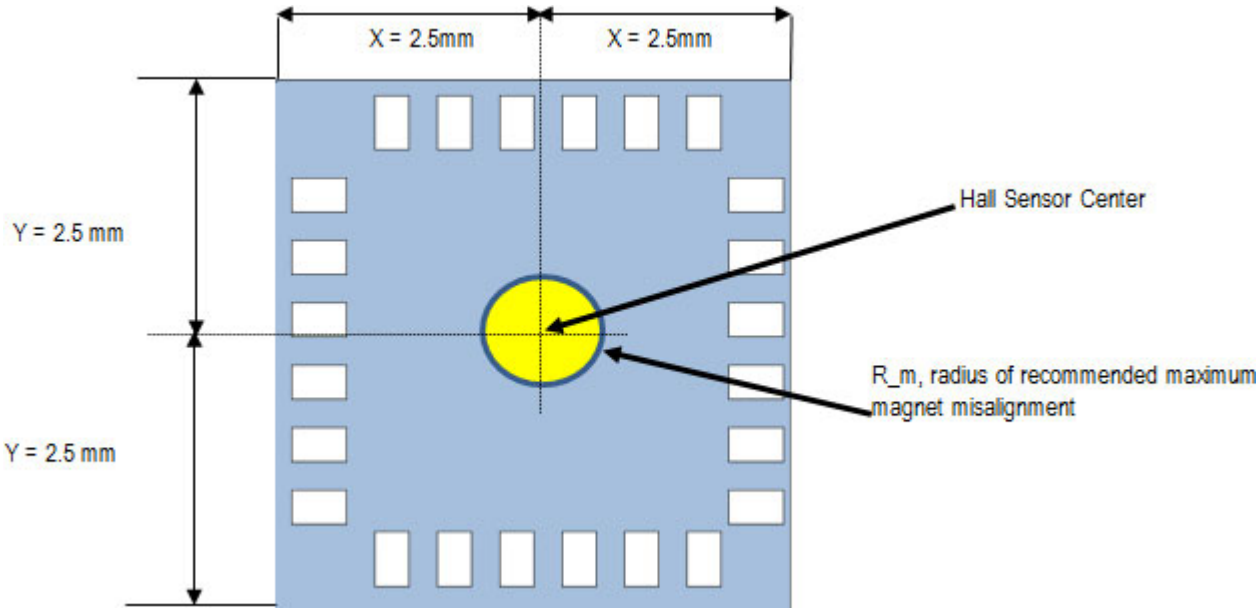
	Parameter	Symbol	Min.	Typ.	Max.	Units	Units
1.	Diameter	d	—	6	—	mm	Recommended magnet: Cylindrical magnet, diametrically magnetized, and 1 pole pair.
2.	Thickness	t	—	2.5	—	mm	
3.	Magnetic input field magnitude	Bpk	45	—	75	mT	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle.
4.	Magnet displacement radius	R_m	—	—	0.25	mm	Displacement between the magnet axis and the device center.
5.	Recommended magnet material and temperature drift	—	—	–0.12	—	%/K	NdFeB (Neodymium Iron Boron), grade N35SH. For better performance, consider an SmCo (Samarium Cobalt) magnet.

Diametrically Magnetized Magnet



Magnet and IC Package Placement

Figure 3: Defined Chip Sensor Center and Magnet Displacement Radius

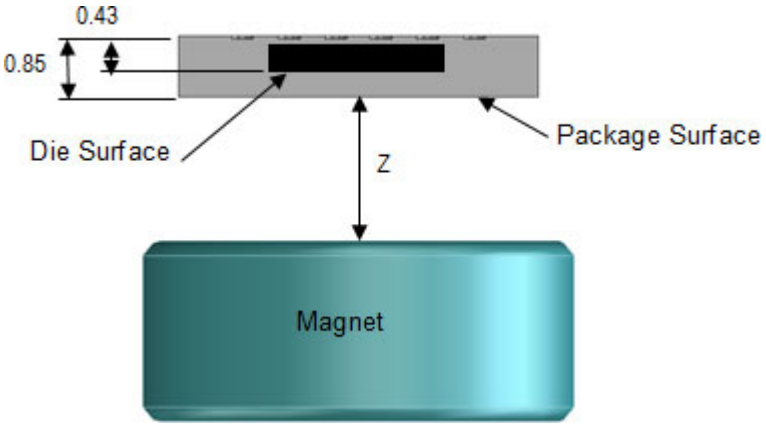


The magnet's center axis should be aligned within a displacement radius of 0.25 mm from the defined hall sensor center.

The magnet should be put facing the sensor. The Z gap varies depending on the magnetic strength on the die surface, with the recommended magnet material and dimension.

The typical distance Z is 0.75 mm to 1.25 mm. However, larger distances are possible as long as the magnetic strength is within the defined limit. It is important not to put magnetic material close to the magnet as it will affect the magnetic field and increase the INL. The magnet must be mounted on a nonmagnetic part.

Figure 4: Vertical Placement of the Magnet



AEAT-8811-Q24 Pin Assignment and Description

Figure 5: AEAT-8811-Q24: Pin Assignment and Description

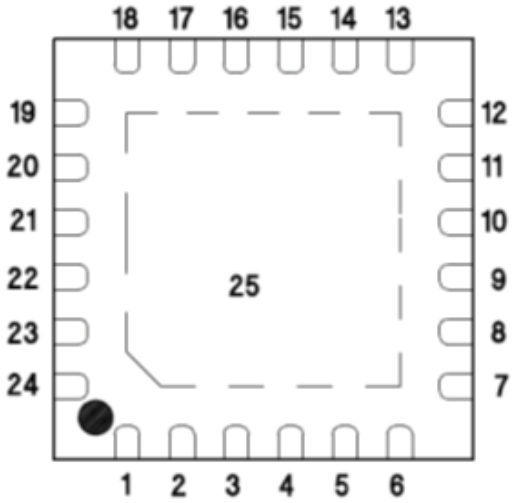


Table 4: Pin Assignment

Pin	Symbol	Description
1–6	NC	No Connection
7	I	Index output (ABI mode)
8	B	Incremental B output (ABI mode)
9	A	Incremental A output (ABI mode)
10	SSI_SCL_SPI_CLK	SSI/SPI clock input
11	SSI_NSL_SPI_DI	SSI/SPI data input
12	SSI_DO_SPI_DO	SSI/SPI data out
13	VSS	Supply Ground
14	VDDA	5V Supply input
15	NC	No Connection
16	NC	No Connection
17	NC	No Connection
18	NC	No Connection
19	VDDA	5V Supply input
20	VSS	Supply Ground
21	SSI_SPI_SEL	SSI/SPI select pin
22	U	U Commutation output (UVW mode)
23	V	V Commutation output (UVW mode)
24	W or PWM	W Commutation (UVW mode)/PWM output
25	VSS	Supply Ground

Absolute Output Format

The AEAT-8811-Q24 provides SSI 3 wires and PWM outputs to indicate the absolute position of the motor.

SSI 3 Wires (SSI): Default

The SSI protocol uses three pins and is shared between SSI and SPI protocols. Use SSI_SPI_SEL (the input pin) to select either protocol at a time. Assert 1 on SSI_SPI_SEL to select the SSI protocol, which supports up to 10-MHz clock rates.

- SSI_NSL_SPI_DIN → NSL (enable) signal for the SSI protocol, input to AEAT-8811-Q24
- SSI_SCL_SPI_CLK → SCL (clock) signal for the SSI protocol, input to AEAT-8811-Q24
- SSI_DO_SPI_DO → DO (data out) signal for the SSI protocol, output from AEAT-8811-Q24

NOTE: Notes for the timing diagram in the following figure:

- NSL must be held high for at least 3 ms after power-up.
- NSL = 1 means that it is in load mode and is used to obtain the position of the magnet.
- NSL = 0 is shift mode of the registers and with the SCL (clock) pin; the register will be clocked.
- tREQ ≥ 300 ns.
- tNSLH ≥ 200 ns.

The user is advised to read from the SSI falling edge.

Figure 6: SSI Protocol Timing Diagram

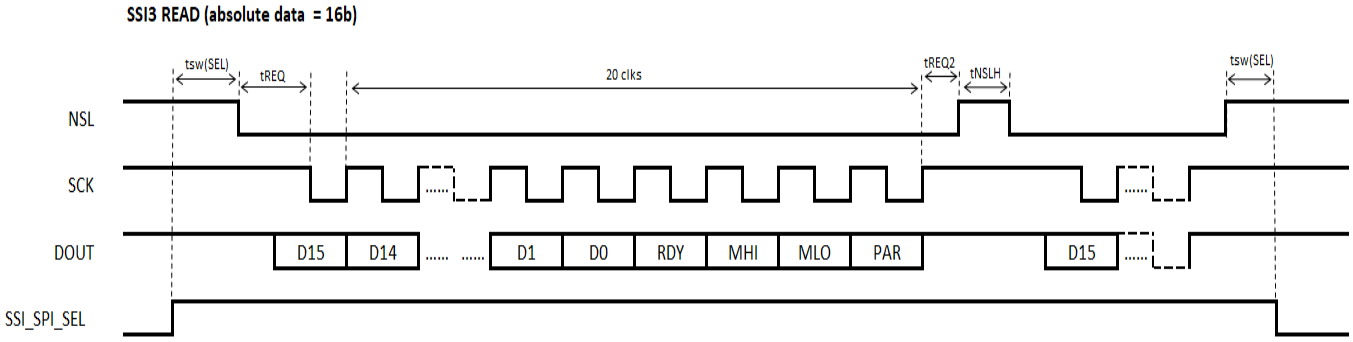


Table 5: Symbols and Description

Symbol	Description	Min.	Typ.	Max.	Unit
tsw(SEL)	SSI_SPI_SEL switch time	1	—	—	µs
tREQ	SCL high time between NLS falling edge and first SCL falling edge	300	—	—	ns
tREQ2	NSL low time after rising edge of last clock period for an SSI read	200	—	—	ns
tNSLH	NSL high time between 2 successive SSI reads	200	—	—	ns

NOTE: CLK=1 when inactive; DIN=1 when inactive.

ATTENTION: Make sure that CLK is high when switching between SSI and SPI modes.

- **Configurable: Data readout with 2 wire SSI (SSI2 mode), up to 2-MHz clock rates**

NOTE: NSL must be held *low* upon power-cycle.

Assert 1 on SSI_SPI_SEL to select the SSI protocol (data readout)

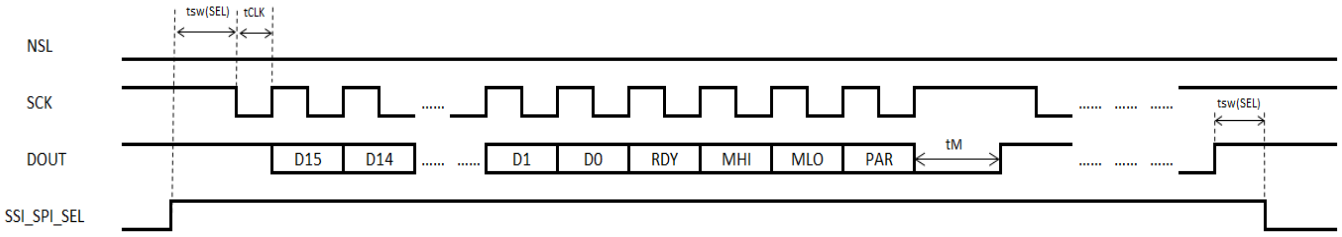


Table 6: Symbols and Description

Symbol	Description	Min.	Typ.	Max.	Unit
tsw(SEL)	SSI_SPI_SEL switch time	1	—	—	µs
tClk	NSL low time after rising edge of last clock period for an SSI read	250	—	tM/2	ns
tM	NSL high time between 2 successive SSI reads	—	16.5	18.0	µs

NOTE: NSL must be held *low* upon power-cycle (NSL high will turn the IC into the default SSI3 mode).

- **User-programmable register option: Initial data output tri-state (high impedance) to logic high to initiate the read-out, up to 10-MHz clock rates**

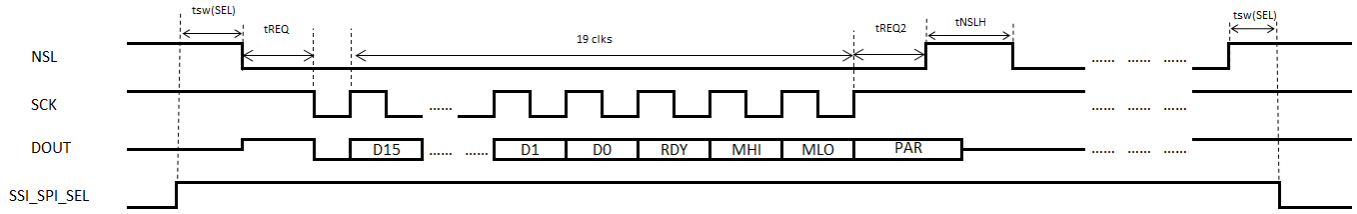


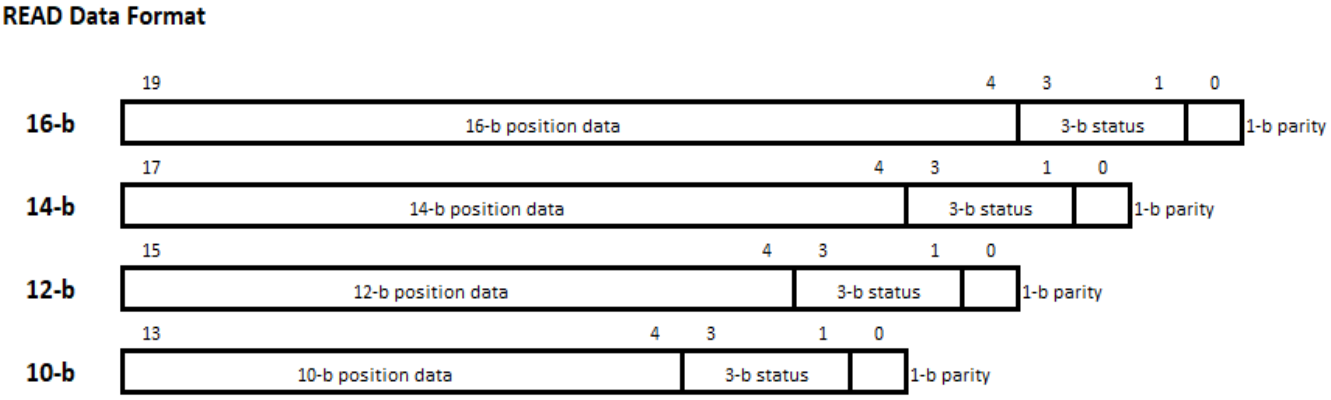
Table 7: Symbols and Description

Symbol	Description	Min.	Typ.	Max.	Unit
tsw(SEL)	SSI_SPI_SEL switch time	1	—	—	µs
tREQ	SCL high time between NLS falling edge and first SCL falling edge	300	—	—	ns
tREQ2	NSL low time after rising edge of last clock period for an SSI read	200	—	—	ns
tNSLH	NSL high time between 2 successive SSI reads	200	—	—	ns

SSI data format may vary depending on the different settings on absolute resolution (16 bits, 14 bits, 12 bits, or 10 bits). The total data length is shown in the following figure.

Three bits status is for Ready, MHI, and MLO.

Figure 7: SSI Output Format for Different Absolute Resolution Settings



NOTE:

- Total data length: 16-b pos → 20-b, 14-b pos → 18-b, 12-b pos → 16-b, 10-b pos → 14-b
- 3-b status: {Ready, MHI, MLO}

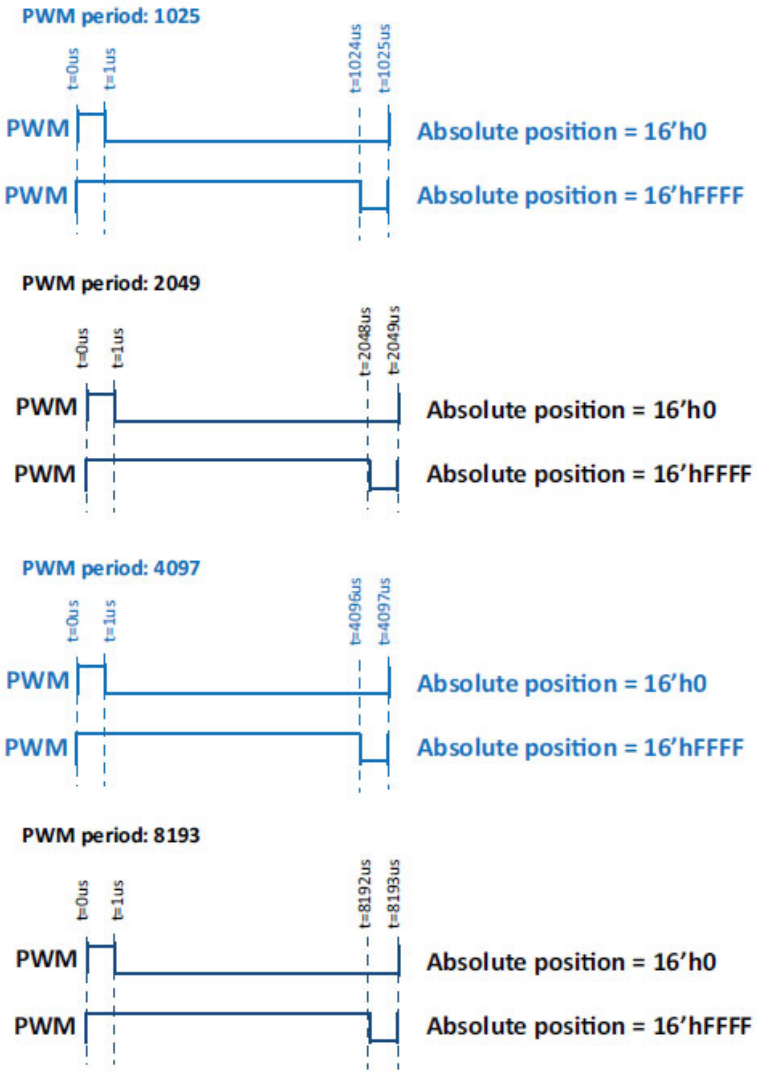
- **Magnet High (MHI) Error:** This indicates that the magnet strength detected by the chip is too strong. When this is consistently flagged as high, change to a weaker magnet or increase the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error:** This indicates that the magnet strength detected by the chip is too weak. When this is consistently flagged as high, change to a stronger magnet or decrease the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Ready:** The chip is ready, and the ready value is 1.

  1-b parity is even parity.

PWM

The PWM protocol uses one output pin (W_PWM) from AEAT-8811-Q24. Note that W_PWM pin is shared between the UVW and PWM protocols. The PWM signals are configurable to have a period of 1025, 2049, 4097, or 8193 µs. During power-up, the PWM signal is 0 before chip ready.

Figure 8: PWM Signals (Period = 1025/2049/4097/8193 µs)



Incremental Output Format

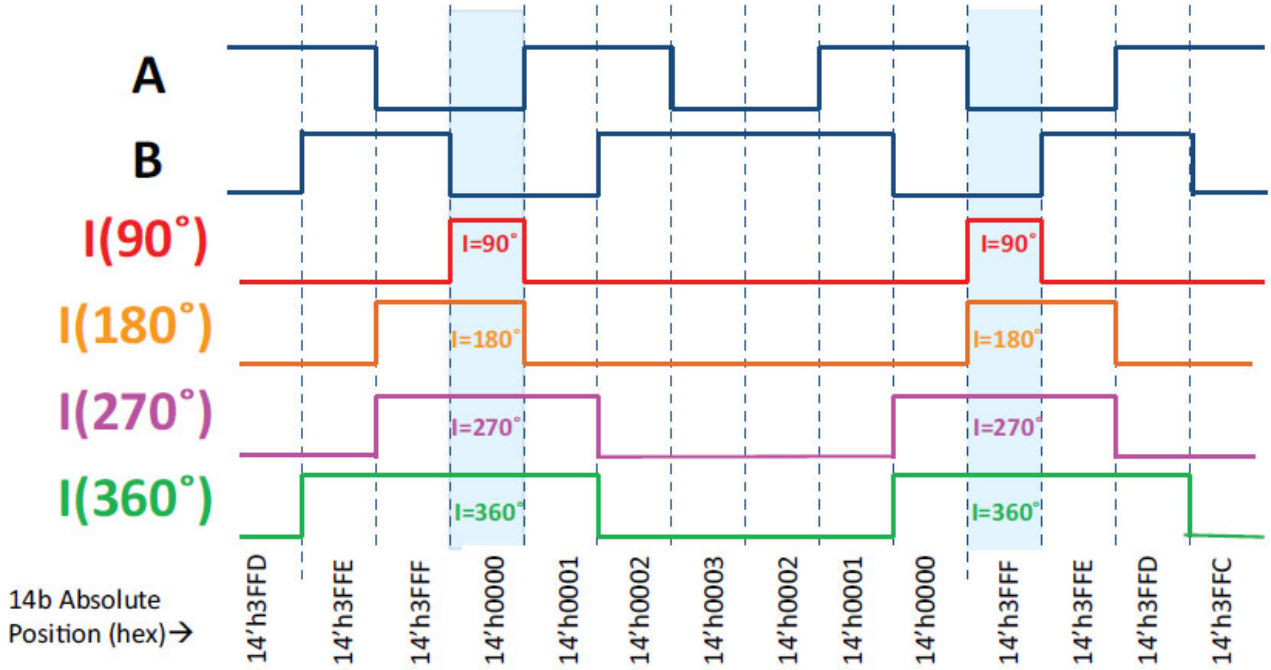
The AEAT-8811-Q24 provides ABI and UVW signals to indicate the incremental position of the motor.

ABI

The ABI incremental interface is available to provide position data and direction data from the three output pins (A, B, and I). The index signal marks the absolute angular position and typically occurs once per revolution. The ABI signal is configurable using the memory map registers. It supports the following configuration:

- Programmable CPR: 32, 50, 64, 100, 128, 200, 256, 400, 512, 800, 1000, 1024, 2000, 2048, 4000, or 4096
- Programmable I-width: 90, 180, 270, or 360 electrical degrees (e.deg)

Figure 9: ABI Signal (4096 CPR, with Different I-Width Settings), Assuming User Sets Hysteresis at 0.02 Mechanical Degrees

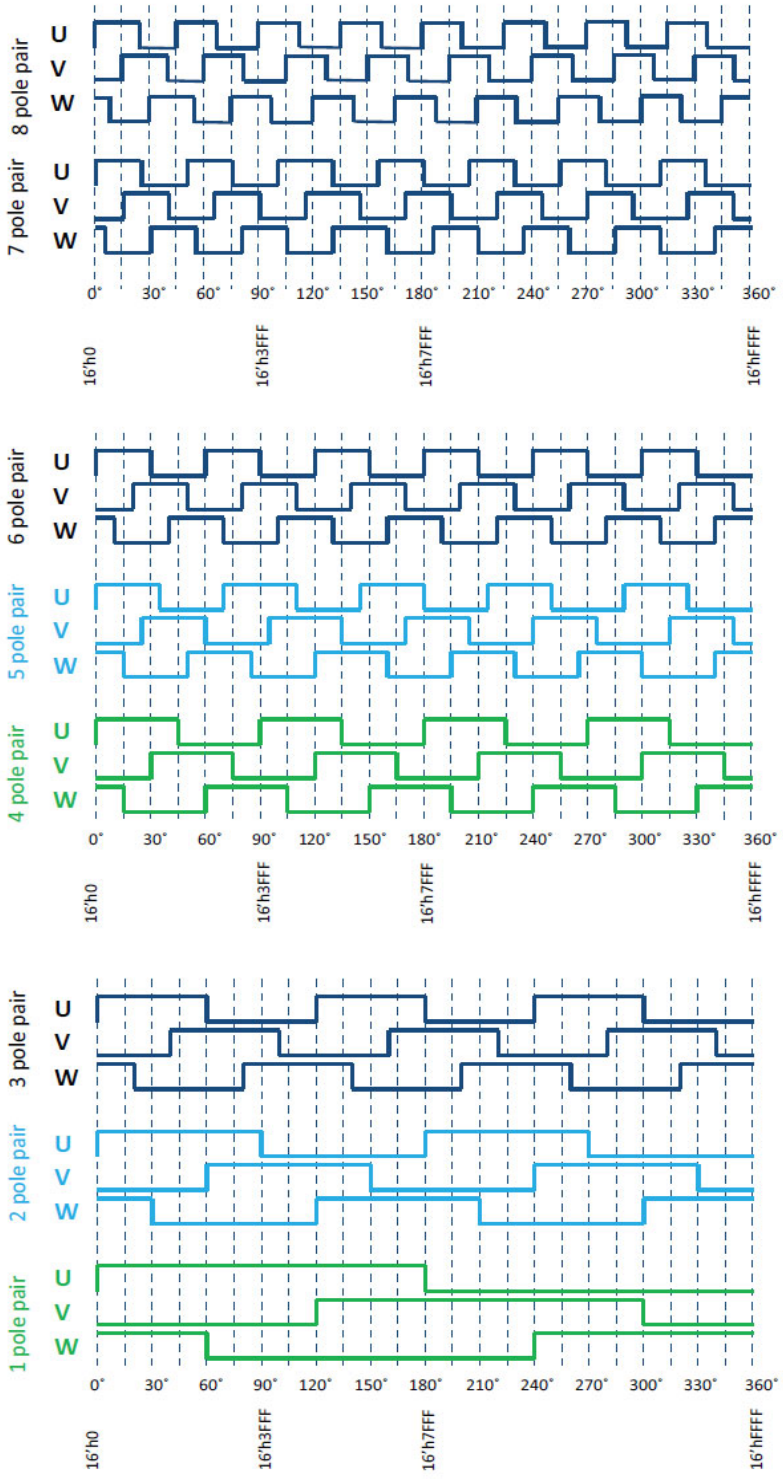


UVW

Three-channel integrated commutation output (U, V, W) emulates Hall sensor feedback and is available using three output pins. Note that the W_PWM pin is shared between the UVW and PWM protocols.

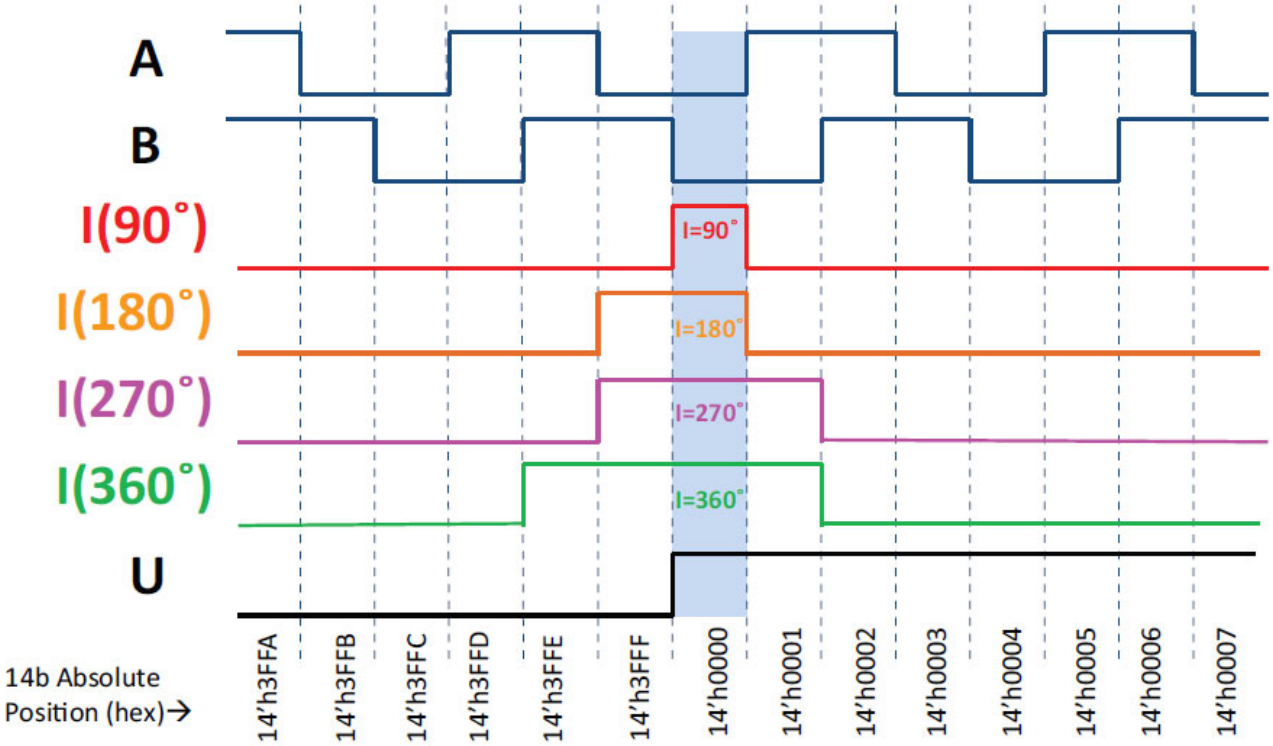
The AEAT-8811-Q24 can configure pole pairs from 1 to 8 (equivalent to 2 to 16 poles).

Figure 10: UVW Signals (1 to 8 Pole Pairs)



Note that signal U from the UVW protocol is tagged to signal I from the ABI protocol, as shown in the following figure.

Figure 11: U-to-I Tagging



Programming the AEAT-8811-Q24

The OTP shadow registers and internal registers are programmable using the SPI protocol. Writing specific commands to specific addresses of internal registers will program values of OTP shadow registers to OTP permanently.

SPI Protocol (For Programming Use Only)

The SPI protocol uses three pins from the AEAT-8811-Q24. These three pins are shared between the SSI and SPI protocols. SSI_SPI_sel (input pin) selects either protocol at a time. Assert 0 on SSI_SPI_sel to select the SPI protocol. The AEAT-8811-Q24 supports the SPI protocol from 10 kHz to 1 MHz.

- SSI_NSL_SPI_DIN → DIN (data in) signal for the SPI protocol, input to AEAT-8811-Q24
- SSI_SCL_SPI_CLK → CLK (clock) signal for the SPI protocol, input to AEAT-8811-Q24
- SSI_DO_SPI_DO → DO (data out) signal for the SPI protocol, output from AEAT-8811-Q24

To read an address using SPI:

DIN: Read<2'b10>Address<5:0>; from 8 bits DIN

Read 8-bit data on DO by clocking 8 SPI_CLK clock.

NOTE: The user should read output data at the rising edge of SPI_CLK.

Figure 12: SPI Read Timing Diagram

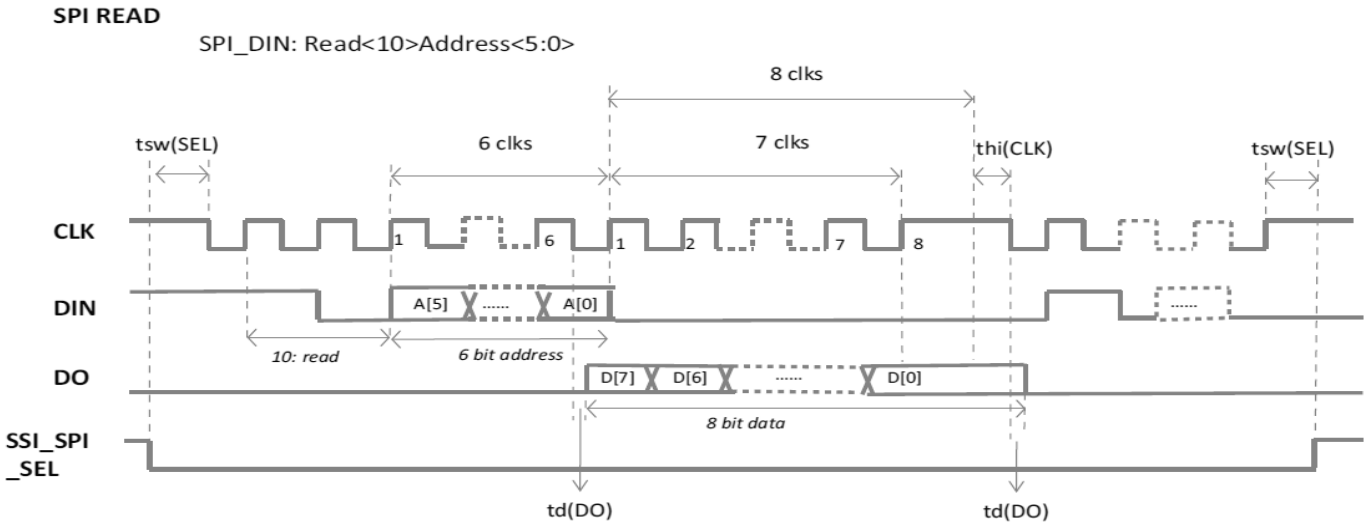


Table 8: Symbols and Description

Symbol	Description	Min.	Typ.	Max.	Unit
tsw(SEL)	SSI_SPI_SEL switch time.	1	—	—	µs
td(DO)	DO data valid after the falling edge of CLK The user should read output data at the rising edge of the SPI_CLK.	—	—	200	ns
thi(CLK)	CLK high time after the end of the last clock period for an SPI read/write command.	300	—	—	ns

NOTE:

- CLK=1 when inactive; DIN=1 when inactive.
- Important: Make sure that CLK is high when switching between SSI and SPI modes.

To write to an address using SPI:

Write <2'b01>Address<5:0>; from 8 bits DIN

SPI_DIN: Write<01>Address<5:0>Data<7:0>

Write is specified as 2 bits (01) in the MSB of the address bus, followed by the 6-bit address, and lastly by the 8-bit data.

NOTE: The user should read back the data to confirm that it was written successfully.

Figure 13: SPI Write Timing Diagram

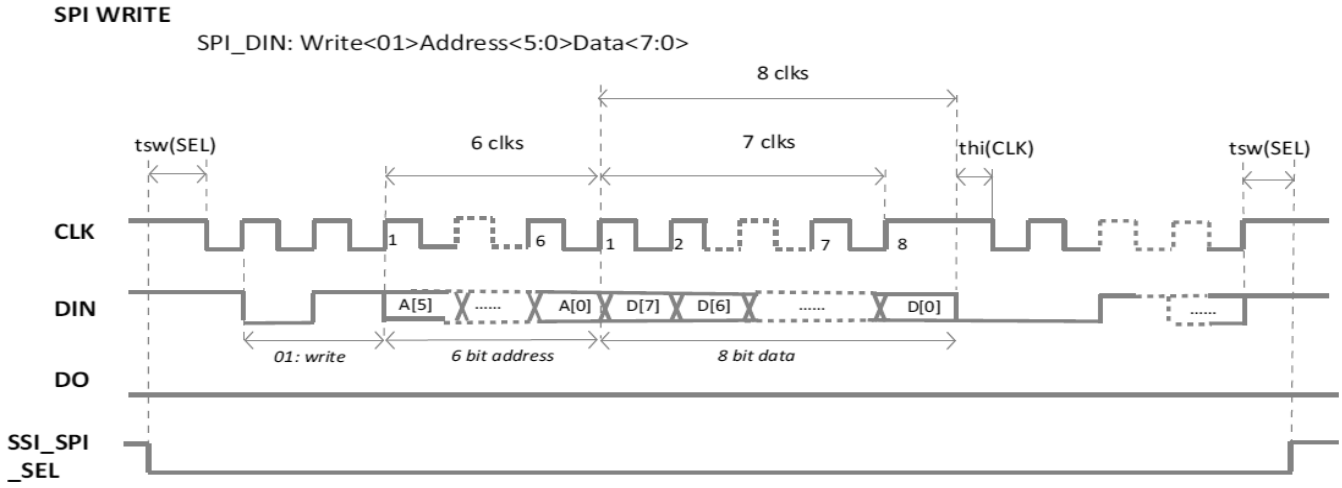


Table 9: Symbols and Description

Symbol	Description	Min.	Typ.	Max.	Unit
tsw(SEL)	SSI_SPI_SEL switch time.	1	—		µs
thi(CLK)	CLK high time after the end of the last clock period for an SPI read/write command.	300	—	—	ns

NOTE:

- CLK=1 when inactive; DIN=1 when inactive.
- Important: Make sure that CLK is high when switching between SSI and SPI modes.

Programming OTP via SPI

Here are the steps to permanently program the OTP nonvolatile memory.

Change the voltage at the VDDA pin to 5.6V ± 0.1V for OTP programming.

See the memory map address as described in Memory Map.

Table 10: Details of Register 0x10 to 0x1B

Address	Bits	Name	Description	Default
0x10	7:0	Unlock Registers	Write 0xAB to this address to unlock all OTP shadow registers and internal registers (except 0x00–0x03, 0x10, 0x11, 0x12, and 0x1B, which are not locked).	8'h0
0x11	7:0	Program Customer Reserved OTP (0x00, 0x01)	Write 0xA1 to this address to program Customer Reserved OTP (0x00, 0x01) to OTP.	8'h0
0x12	7:0	Program ST Zero Reset OTP (0x02, 0x03)	Write 0xA2 to this address to program ST Zero Reset OTP (0x02, 0x03) to OTP.	8'h0
0x13	7:0	Program Customer Configuration OTP (0x04, 0x05, 0x06)	Write 0xA3 to this address to program Customer Configuration OTP (0x04, 0x05, 0x06) to OTP.	8'h0

Package Drawings (in mm)

Figure 14: AEAT-8811-Q24 QFN Dimensions

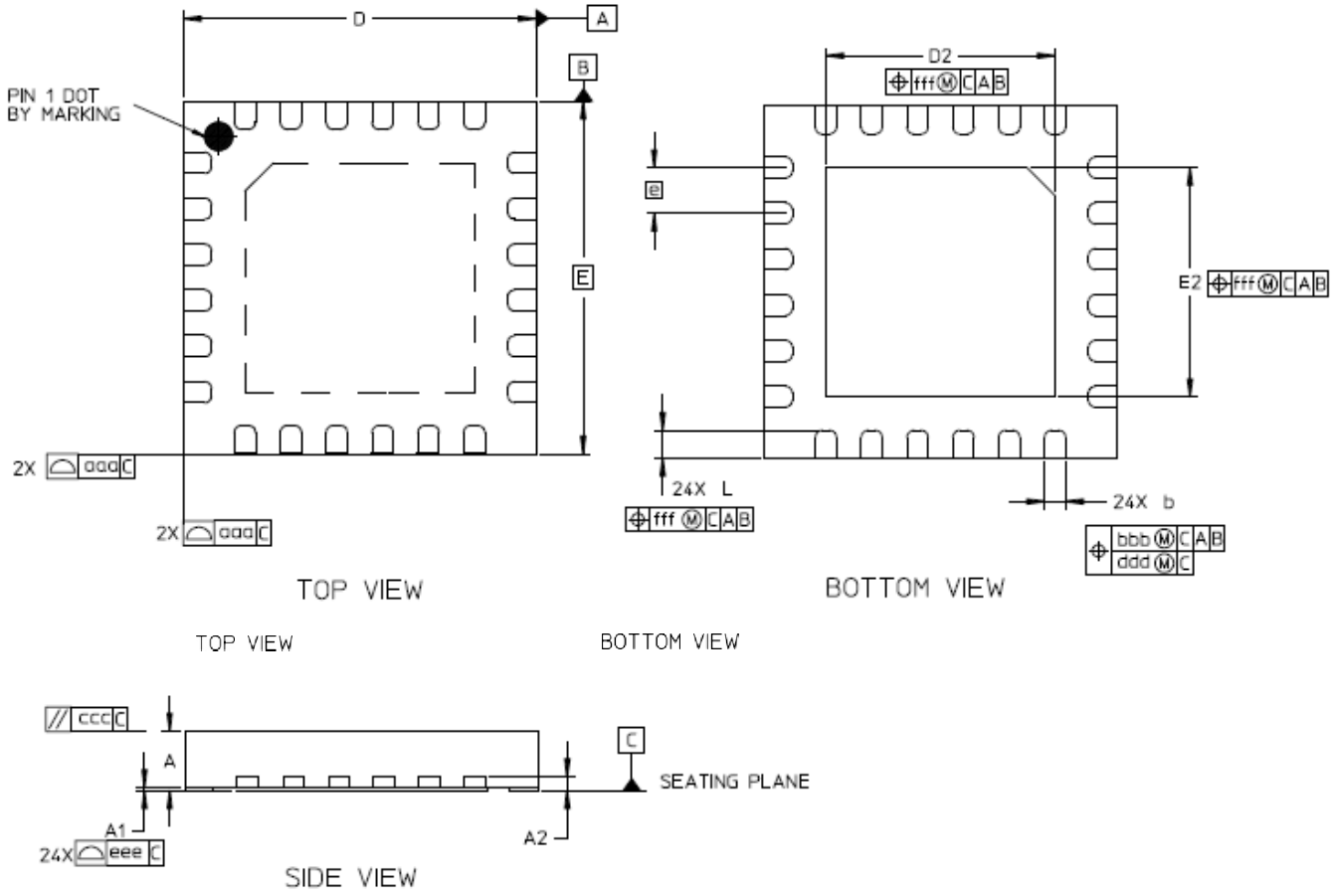


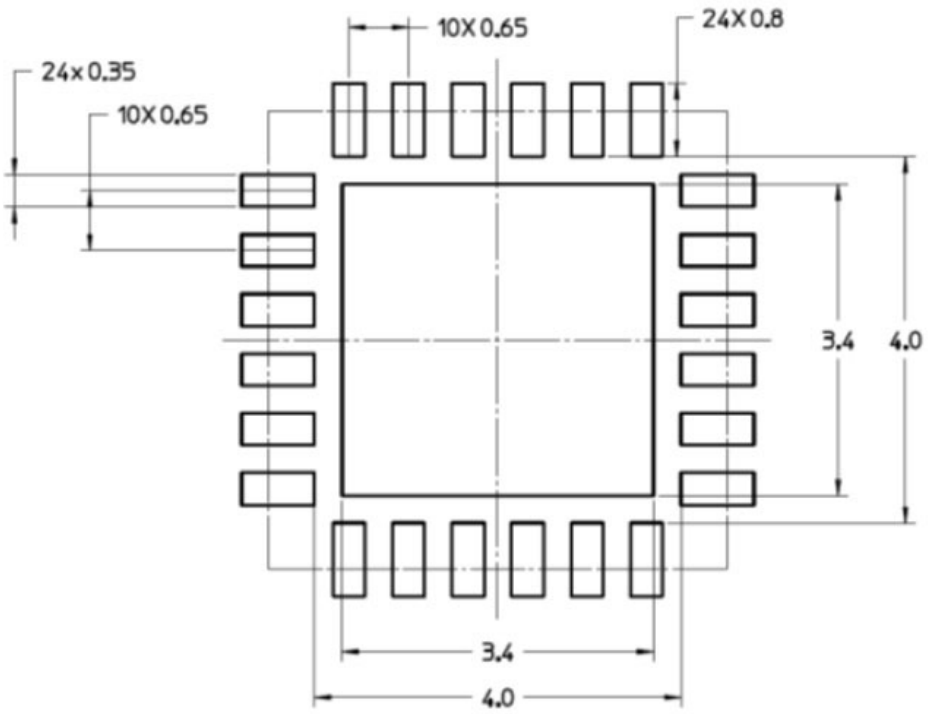
Table 11: Dimensions and Tolerances

Dimension Reference			
REF	**Min.**	**Nom.**	**Max.**
A	0.800	0.850	0.900
A1	0.000	—	0.050
A2	0.203 REF		
D	5.000 BSC		
E	5.000 BSC		
D2	3.200	3.250	3.300
E2	3.200	3.250	3.300
b	0.250	0.300	0.350
e	0.650 BSC		
L	0.350	0.400	0.450

Dimension Tolerance	
REF	**Tolerance**
aaa	0.100
bbb	0.100
ccc	0.050
ddd	0.050
eee	0.080
fff	0.050

Recommended PCB Land Pattern (in mm)

Figure 15: Land Pattern Dimensions



Recommended Lead-Free Solder Reflow

Figure 16: Reflow Soldering Temperature Profile