BROADCOM

Product Brief

ACPL-736J

Optically Isolated ±50 mV Sigma-Delta Modulator with CMOS Interface

Key Features

- 5 MHz to 21 MHz external clock input range
- CMOS clock and data interface.
- 1-bit, second-order sigma-delta modulator
- 16 bits resolution no missing codes (12 bits ENOB)
- 80 dB typical SNR and 78 dB typical SNDR
- 1.0 µV/°C maximum offset drift
- ±1% maximum gain error
- ±50 mV linear range with single 5V supply (±80 mV full scale range)
- –40°C to +110°C operating temperature range
- SO-16 package
- 25 kV/µs common-mode transient immunity
- Safety and regulatory approval (pending):
  - IEC/EN/DIN EN 60747-5-5: 1414 Vpeak working insulation voltage
  - UL 1577: 5000 Vrms/1 min double protection rating
  - CSA: Component Acceptance Notice #5

Applications

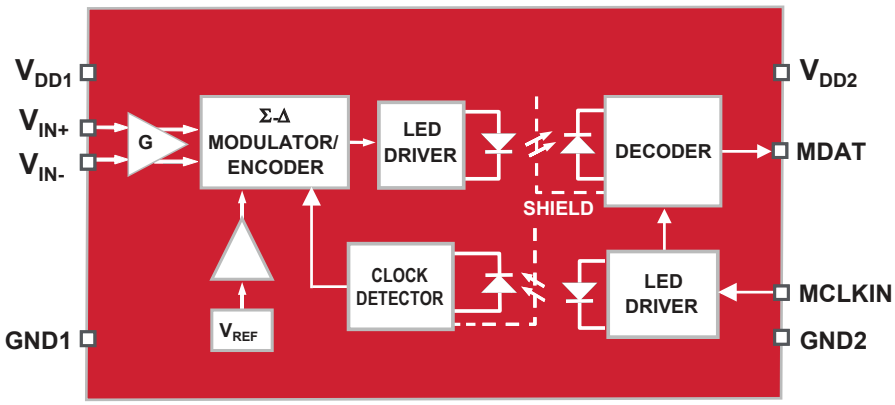
- Motor phase and rail current sensing
- Power inverter current sensing
- Industrial process control
- Data acquisition systems
- General-purpose current sensing
- Traditional current transducer replacement

Overview

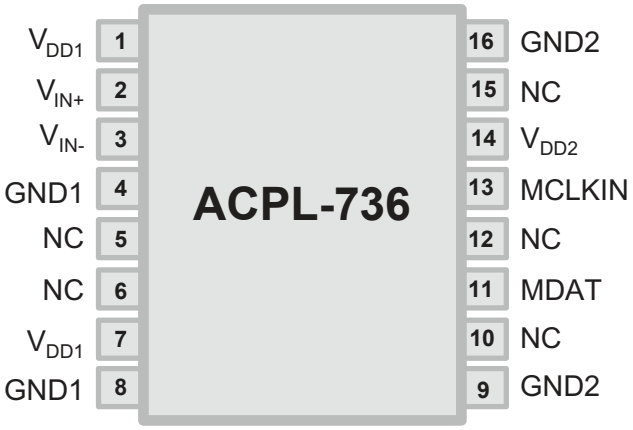
The Broadcom® ACPL-736J is a 1-bit, second-order sigma-delta (Σ-Δ) modulator that oversamples an analog input signal into a high-speed data stream with galvanic isolation based on optical coupling technology. The ACPL-736J operates from a 5V power supply with dynamic range of 80 dB with an appropriate digital filter. The differential inputs of ±50 mV (full scale ±80 mV) are ideal for direct connection to shunt resistors or other low-level signal sources in applications such as motor phase current measurement.

The analog input is continuously sampled by means of sigma-delta oversampling using an external clock, coupled across the isolation barrier, which allows synchronous operation with any digital controller. The signal information is contained in the modulator data, as a density of ones with a data rate up to 21 MHz. The data are encoded and transmitted across the isolation boundary where they are recovered and decoded into a high-speed data stream of digital ones and zeros. The original signal information can be reconstructed with a digital filter. The ACPL-736J comes with a CMOS interface on both clock inputs and data outputs for better signal integrity.

Figure 1: Functional Block Diagram



ACPL-736 Pin Configuration



Pin Number	Symbol	Description
1, 7	V_{DD1}	Supply voltage for input side relative to GND1.
2	V_{IN+}	Positive analog input, recommended input range ±50 mV.
3	V_{IN-}	Negative analog input, recommended input range ±50 mV (normally connected to GND1).
4, 8	V_{IN-}	Supply ground for signal input side.
5, 6, 10, 12, 15	NC	Leave the pins unconnected. Do not connect to V_{DD1}, GND1 or V_{DD2}, GND2.
9, 16	GND2	Supply ground for data output side (digital side).
11	MDAT	Modulator data output.
13	MCLKIN	Modulator clock input.
14	V_{DD2}	Supply voltage for output side, referenced to GND2.

ACPL-736J-PB100 May 29, 2020