AN90005

Understanding Power GaN FET data sheet parameters

Rev. 1.1 — 13 February 2019 application note

Document information

Information	Content
Keywords	GaN FET, parameters, data sheet
Abstract	This appplication note explains the content of Nexperia Power GaN FET data sheets. Nomenclature, pinning and key parameters are detailed.

nexperia

1. Introduction

This application note examines in detail the data sheet for the GAN063-650WSA GaN FET device from Nexperia. Visit the product information page on Nexperia.com to download the latest version of the full data sheet.

2. Nomenclature

The device name (type number) is shown at the top of the data sheet. The name contains some important information about the device. In the below example for GAN063-650WSA, the maximum on-state resistance and the limiting drain-source voltage are specified, together with letter codes indicating the package, the mounting base electrical connection and the technology generation.

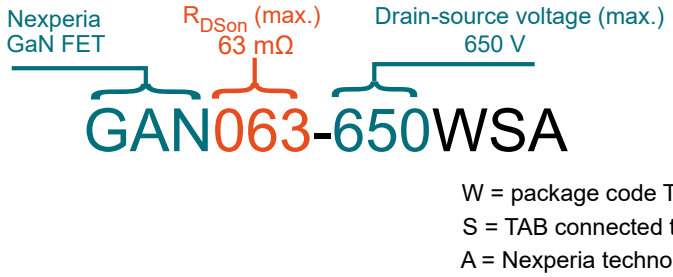


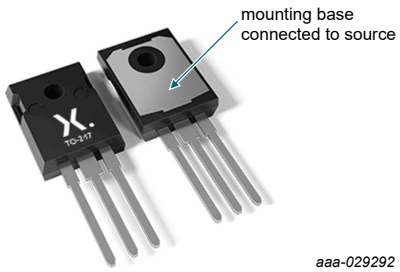
Fig. 1. GaN FET Nomenclature

3. Pinning information

Table 1. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb 1 2 3 TO-247 (SOT429)	D G S aaa-028116
2	S	source		
3	D	drain		
mb	S	mounting base; connected to source		

The Nexperia GAN063-650WSA is packaged in a TO247 (SOT429) package with a source tab. The traditional TO-247 provides excellent heat transfer, and therefore excellent power-handling capability.



Note: the pin functions are different from a standard MOSFET: pin 1 is the gate, pin 2 is the source and pin 3 is the drain.

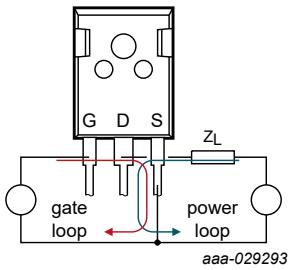


Fig. 2. Conventional pin assignment

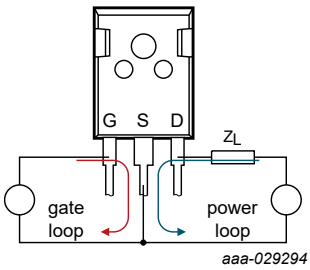
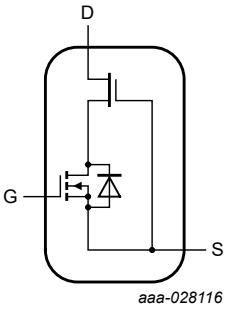


Fig. 3. Nexperia pin assignment

Using pin 2 as the source pin allows the circuit designer to keep the gate loop and the power loop separate. This facilitates a very clean design and greatly reduces or eliminates cross coupling. The PCB design can be optimised to take advantage of this feature.

4. Two-chip, integrated, normally-off power switch

The full graphic symbol of a GaN FET is shown in the pinning information section of the data sheet. Note that the symbol includes two devices:



- Low-voltage Si MOSFET with a p-n body diode
- High-voltage GaN FET without a p-n body diode

The full graphic symbol shows that the device is a two chip integrated switch. Functionally the switch is normally off. Internally the device is built with two chips. The high-voltage GaN HEMT or FET is normally on, which is the type most naturally made with GaN, and is combined with a high performance normally-off Si MOSFET specifically developed to complement the GaN HEMT. The two chips are integrated with absolute minimum inductance between them.

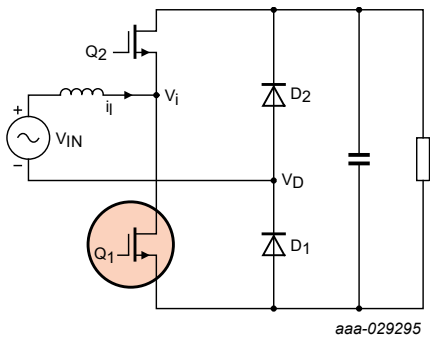


Fig. 4. Simplified GaN FET symbol

In circuit schematics where just the basic switching function is important, a simple N-channel FET symbol is used to represent the complete, integrated switch (see Q1 circled in red above). When you see the simple symbol, understand that it represents this two-chip integrated combination.

5. GaN FET limiting values

The limiting values table provides the range of operating conditions allowed for the GaN FET. The conditions are defined in accordance with the *Absolute Maximum Rating System (IEC 60134)*.

Operation outside of these conditions is not guaranteed, so it is recommended that these values are never exceeded. Doing so risks immediate device failure or reduced lifetime of the GaN FET. To calculate how the limiting values change with temperature de-rating curves are provided.

The limiting values table for the GAN063-650WSA is given as an example of a standard limiting values table, in Table 2.

Table 2. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 175 °C		-	650	V
V_{TDS}	transient drain to source voltage	pulsed; t_p = 1 µs; δ_{factor} = 0.01		-	800	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 9		-	143	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	34.5	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	24.4	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	150	A
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C; V_{GS} = 0 V		-	34.5	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	150	A

5.1. Drain-source voltage, V_{DS}

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 175 °C		-	650	V
V_{TDS}	transient drain to source voltage	pulsed; t_p = 1 µs; δ_{factor} = 0.01		-	800	V

This 650 V rating is the maximum value that will give you the desired product life.

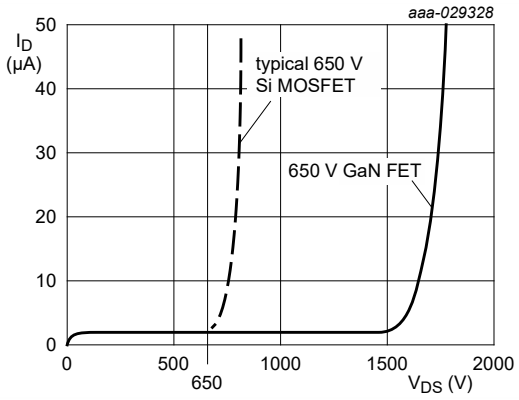


Fig. 5. Nexperia GaN FET leakage as a funtion of drain-source voltage

As can be seen in Fig. 5 above, GaN FETs do not have an avalanche breakdown mechanism. The Nexperia GaN FET does not typically show any significant leakage current until a V_{DS} greater than 1500 V is reached. So, there is an extra margin in V_{DS} before excess leakage occurs. If the GaN FET is subjected to a voltage greater than 1500 V, then because there is no clamping mechanism damage and or failure will occur. Since GaN FETs do not have an avalanche breakdown mechanism they are very immune to cosmic radiation and so no further de-rating is required.

- V_{DS} is the maximum voltage the device is guaranteed to block between drain and source terminals in the off-state.
- V_{DS} is a DC rating
- V_{DS} not limited by avalanche breakdown; rating can be applied over entire operating range of -55 °C to 175 °C in contrast to V_{DS} for Si MOSFET must be de-rated below 25 °C

5.2. Transient drain-source voltage, V_{TDS}

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 175 °C		-	650	V
V_{TDS}	transient drain to source voltage	pulsed; t_p = 1 µs; δ_{factor} = 0.01		-	800	V

V_{TDS} is the **Maximum** repetitive transient voltage the device is guaranteed to block between drain and source in the off state. This transient rating, applies over the entire operating temperature range.

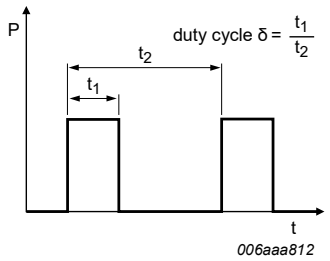


Fig. 6. Duty Cycle Definition

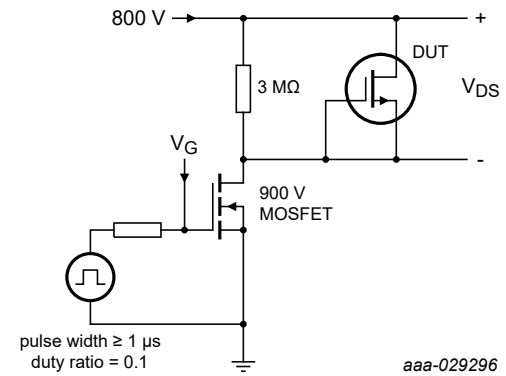


Fig. 7. V_{TDS} test circuit

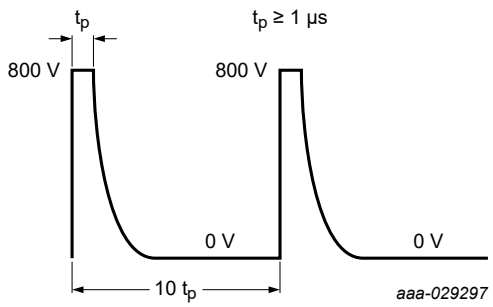


Fig. 8. V_{TDS} waveform

5.3. Gate source voltage, V_{GS} and total power dissipation, P_{tot}

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 175 °C		-	650	V
V_{TDS}	transient drain to source voltage	pulsed; t_p = 1 µs; δ_{factor} = 0.01		-	800	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C		-	143	W

V_{GS}

Maximum voltage the device is guaranteed to block between the gate and source terminals. This is a DC rating, and applies over the entire operating temperature range.

P_{tot}

P_{tot} is the Total Power dissipation is the maximum for a device with a mounting base temperature of 25 °C.

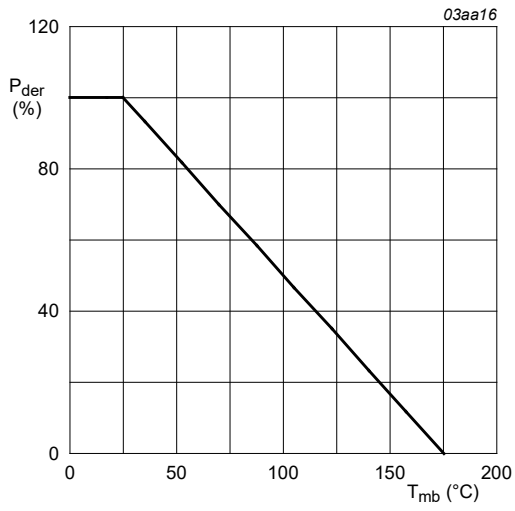


Fig. 9. Normalised total power dissipation as a function of mounting base temperature

Power dissipation is calculated as that which would take the device to the maximum allowed junction temperature while keeping the mounting base at 25 °C.

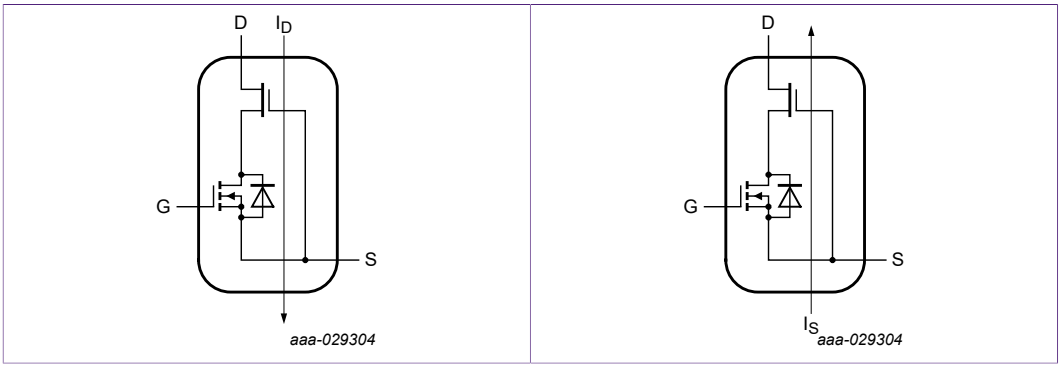
5.4. Continuous and pulsed currents, I_D, I_{DM}, I_S and I_{SM},

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 175 °C		-	650	V
V_{TDS}	transient drain to source voltage	pulsed; t_p = 1 µs; δ_{factor} = 0.01		-	800	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C		-	143	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	34.5	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	24.4	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	150	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C; V_{GS} = 0 V		-	34.5	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	150	A

The 25 °C current ratings are the same for both current directions (I_D and I_S).



The maximum current at any T_{mb} is the current which increases T_j to the maximum allowed temperature (175 °C).

6. GaN FET static characteristics

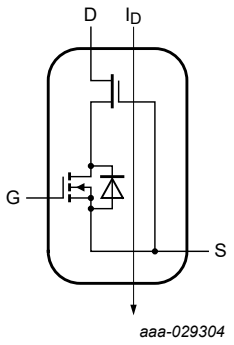
These are the device parameters that explain how the GaN FET behaves in it normal operating conditions

6.1. Gate-source threshold voltage, $V_{GS(th)}$

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		3.5	3.9	4.4	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		2.3	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	-	5	V
I_{DSS}	drain leakage current	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C		-	2	25	µA
		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 175 °C		-	25	-	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA

Gate-source threshold voltage for the GaN FET device is the gate-source threshold voltage of the Si MOSFET. This gate threshold is 3.9 V typically, with a negative temperature co-efficient.



I_D = 1 mA; V_{GS} = $V_{GS(th)}$

Fig. 10. GaN FET gate-source threshold voltage

6.2. Drain-source on-state resistance, R_{DSon}

R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	50	60	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C		-	120	-	mΩ

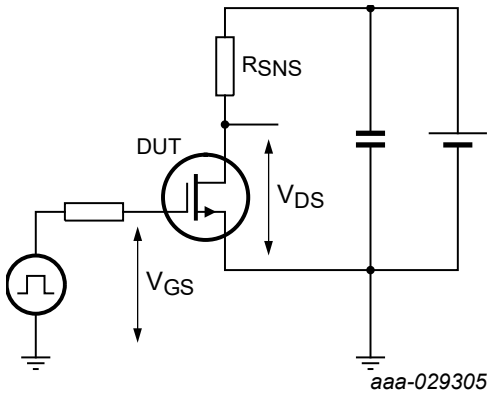


Fig. 11. Test circuit for dynamic R_{DSon}

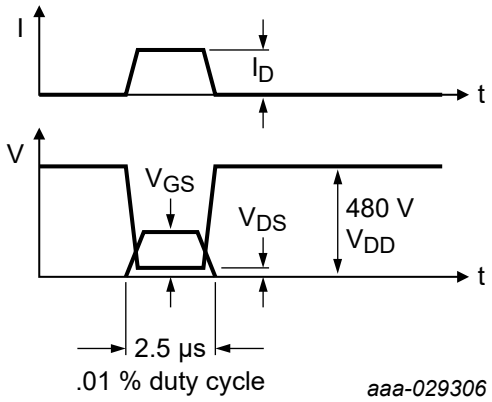


Fig. 12. Dynamic R_{DSon} waveform

R_{DSon} is the drain-to-source on-state resistance of the GaN FET. This has a dynamic value for GaN FETs. When R_{DSon} is measured immediately after turn-on, following period of blocking high-voltage, this value will be slightly higher than normal. This is due to temporary charge trapping in the device structure. Nexperia have optimised the device so that charge trapping and dynamic R_{DSon} are minimised.

As can be seen in Fig. 13, R_{DSon} is shown as a normalised function of junction temperature.

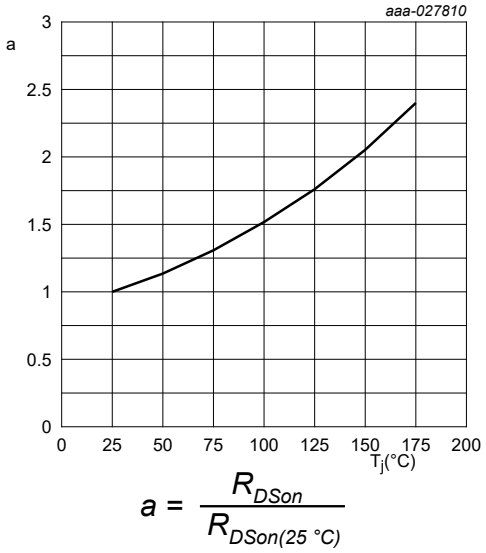


Fig. 13. Normalised drain-source on-state resistance as a funtion of junction temperature

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7. GaN FET dynamic characteristics

These are the device parameters that explain how the GaN FET behaves in its normal operating conditions

7.1. Gate charge $Q_{G(tot)}$, Q_{GS} and Q_{GD}

Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 400 V; V_{GS} = 10 V; T_j = 25 °C		-	15	-	nC
Q_{GS}	gate-source charge			-	6	-	nC
Q_{GD}	gate-drain charge			-	4	-	nC

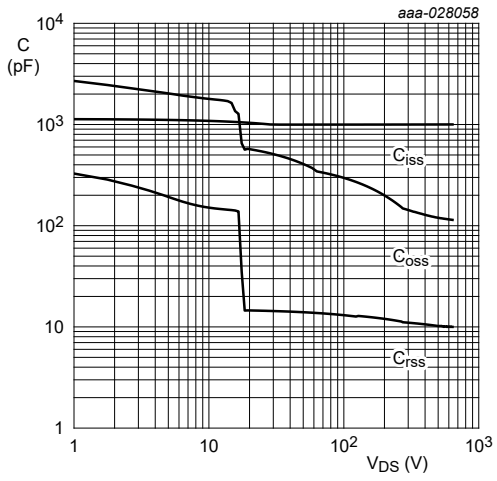
Gate charge for GaN FET is defined in the same way as a normal MOSFET, because the cascode arrangement of a GaN FET means that the gate is in fact the gate of a LV MOSFET. Since the LV MOSFET is a relatively small device it has a small gate charge suited to high speed switching.

7.2. Capacitances C_{iss}, C_{oss} and C_{rss}

C_{iss}	input capacitance	V_{DS} = 400 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		-	1000	-	pF
C_{oss}	output capacitance			-	130	-	pF
C_{rss}	reverse transfer capacitance			-	8	-	pF

Traditional small signal capacitance is shown in Fig. 14. The discontinuity (step change) in Fig. 14 is where GaN HEMT pinches off. Capacitance relates charge to voltage and energy to voltage. For a linear capacitance, the following fundamental equations apply:

$$Q = CV \qquad E = \frac{CV^2}{2}$$



V_{GS} = 0 V; f = 1 MHz

Fig. 14. Input, output and reverse transfer capacitance as a funtion of drain-source voltage; typical values

The capacitances $C_{o(er)}$ and $C_{o(tr)}$ attempt to capture these relationships for a nonlinear capacitance.

7.3. Effective output capacitance (energy related), $C_{o(er)}$

$C_{o(er)}$	effective output capacitance, energy related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C		-	190	-	pF
$C_{o(tr)}$	effective output capacitance, time related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C		-	310	-	pF

The GaN FET capacitance parameter $C_{o(er)}$ is the effective output capacitance (energy-related) dependent on the drain voltage

Note that 0 ≤ V_{DS} ≤ 400 V shown above, means as the voltage rises from 0 V to 400 V.

$$E_{oss} = \int_0^{Q_{oss}} V_{DS} \cdot dq = \int_0^{V} V_{DS} \cdot C\left(V_{DS}\right) \cdot dV_{DS}$$

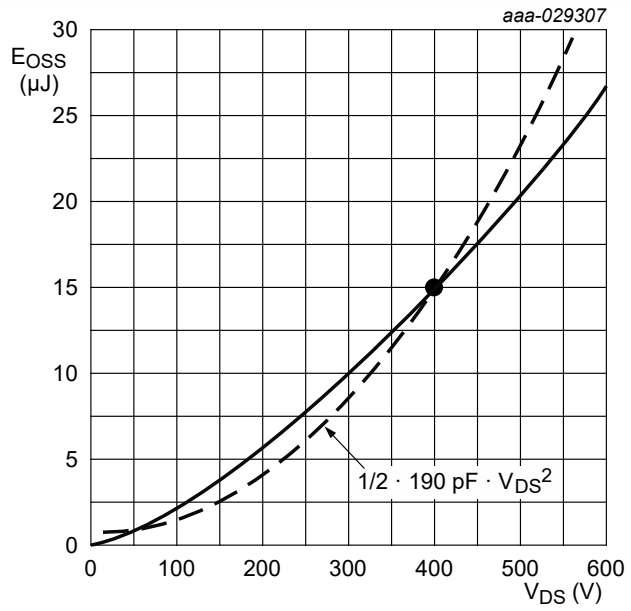


Fig. 15. E_{OSS} as a function of V_{DS}

At a specific V_{DS}, a unique value of C_{oss} satisfies the equation:

$$E_{oss} = {}^{1}\!/_{2} \cdot \mathrm{Co(er)} \cdot {V_{DS}}^2$$

e.g.

$$E_{oss} = {}^{1}\!/_{2} \cdot 190\mathrm{pF} \cdot 400^2 = 15.2\mu\mathrm{J}$$

By integrating C_{OSS} with respect to V_{DS}, the result will be Q_{OSS}. If we then integrate Q_{OSS} with respect to V_{DS}, we will then arrive at E_{OSS}.

E_{OSS} * switching frequency will give the switching power loss in Watts.

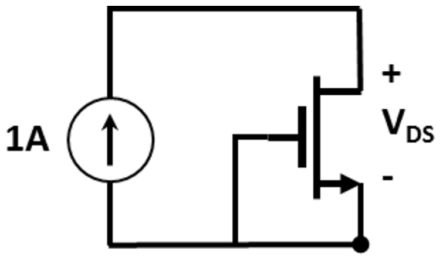
7.4. Effective output capacitance (time related), $C_{o(tr)}$

$C_{o(er)}$	effective output capacitance, energy related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C		-	190	-	pF
$C_{o(tr)}$	effective output capacitance, time related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C		-	310	-	pF

The GaN FET capacitance parameter $C_{o(tr)}$ is the equivalent capacitance to give same charging time, as V_{DS} rises from 0 V to 400 V. This can also be described as a constant current being used to charge the output capacitance, giving a time related effective value.

$$Q_{oss} = \int_0^{Q_{oss}} dq = \int_0^V C\left(V_{DS}\right) \cdot dV_{DS}$$

At a specific V_{DS}, a unique value of C_{oss} satisfies the equation:



$$V_{ds} = \frac{Q_{oss}}{C_{(tr)}} = \frac{1}{C_{o(tr)}} \int_0^t i(t) \cdot dt$$

e.g.

$$400V = \frac{1}{310pF} \cdot \int_0^{120ns} 1.0A \cdot dt$$

$$Q_{oss} = 124nC$$

7.5. Output charge and stored energy, Q_{oss} and E_{oss}

Rather than using the $C_{o(tr)}$ and $C_{o(er)}$ parameters, it is much easier to use the graphs shown below that are also available in the data sheet. The respective Q_{OSS} and E_{OSS} values can be read directly for the required V_{DS}.

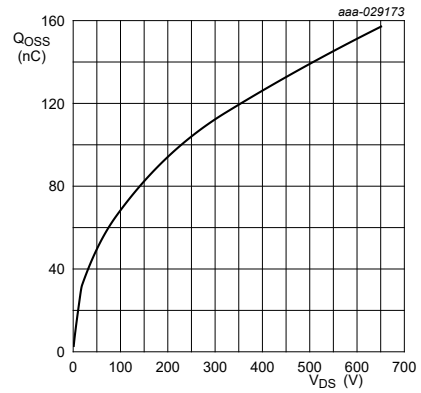


Fig. 16. Typical Q_{OSS}

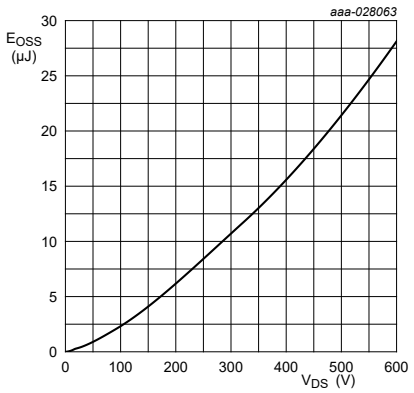


Fig. 17. Typical C_{OSS} stored energy

7.6. GaN FET switching time characteristics

$t_{d(on)}$	turn-on delay time	V_{DS} = 400 V; R_L = 16 Ω; V_{GS} = 12 V; $R_{G(ext)}$ = 40 Ω		-	55	-	ns
t_r	rise time			-	10	-	ns
$t_{d(off)}$	turn-off delay time			-	88	-	ns
t_f	fall time			-	11	-	ns

Nexperia GaN FETs in TO247 package have an integral Ferrite bead in the gate path. This serves to de-“Q” the gate-source loop and improve the switching stability. The Ferrite bead effectively provides damping impedance at frequencies > 100 MHz. The Ferrite bead does introduce a small propagation delay which can be seen in the values for $t_{d(on)}$ and $t_{d(off)}$, however, it does not introduce any additional loss.

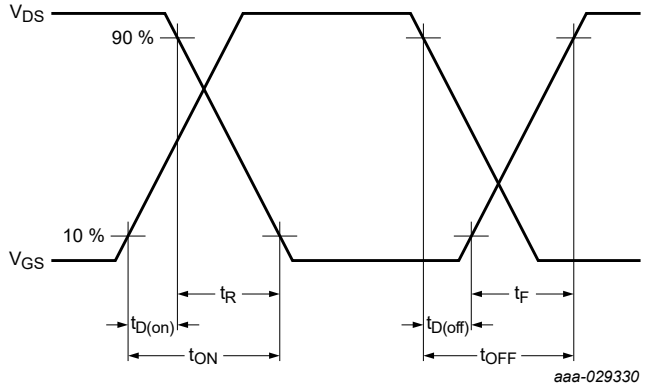


Fig. 18. Switching time waveform

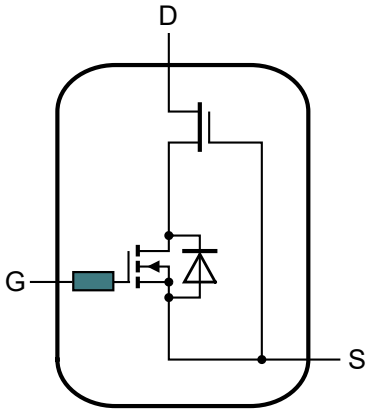
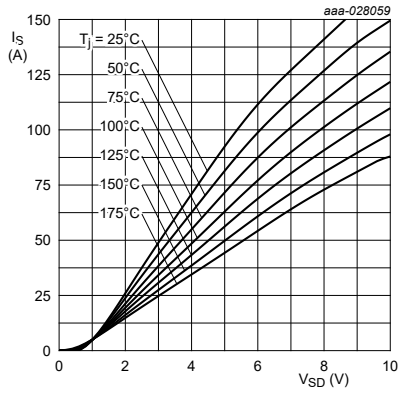


Fig. 19. Internal Ferrite bead

7.7. Source-drain voltage, V_{SD}

Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	1.9	-	V
		I_S = 12.5 A; V_{GS} = 0 V; T_j = 25 °C		-	1.35	-	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -1000 A/µs; V_{GS} = 0 V; V_{DS} = 400 V		-	54	-	ns
Q_r	recovered charge			-	125	-	nC

This device parameter source-drain voltage refers to the GaN FET device when it is acting as a two terminal device when not enhanced with the gate V_{GS} = 0 V.



V_{GS} = 0 V

Fig. 20. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

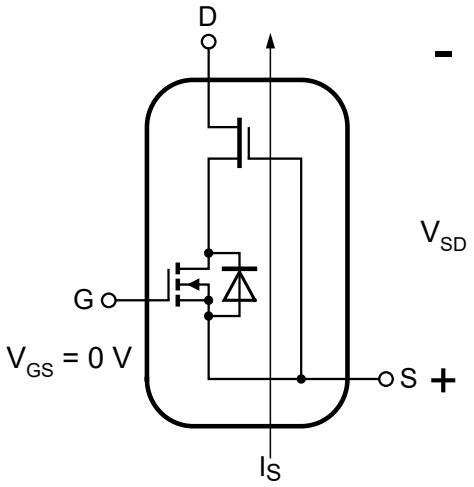


Fig. 21. Source-drain (diode forward) voltage

V_{SD} is the voltage developed whilst GaN FET conducts in reverse direction (e.g. acting as a rectifier carrying freewheeling current) Here the voltage V_{SD} comprises the forward voltage of the Silicon MOSFET body diode and the voltage drop across the 2 DEG channel of the GaN HEMT.

8. Q_r for GaN FET switches

Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 400 V; V_{GS} = 10 V; T_j = 25 °C		-	15	-	nC
Q_{GS}	gate-source charge			-	6	-	nC
Q_{GD}	gate-drain charge			-	4	-	nC
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 400 V		-	125	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	1.9	-	V
		I_S = 12.5 A; V_{GS} = 0 V; T_j = 25 °C		-	1.35	-	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -1000 A/µs; V_{GS} = 0 V; V_{DS} = 400 V		-	54	-	ns
Q_r	recovered charge			-	125	-	nC

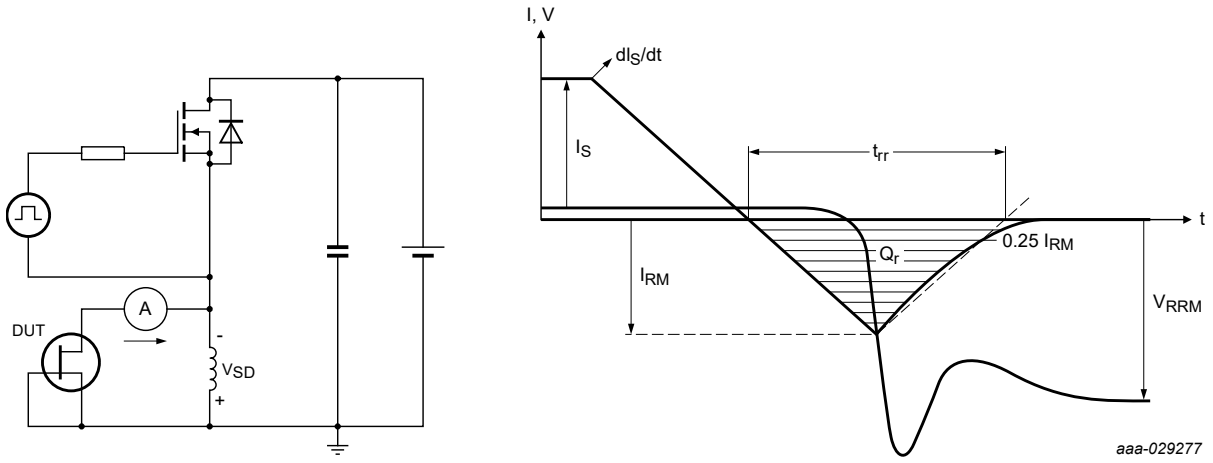


Fig. 22. Recovered charge test circuit and measurement waveforms

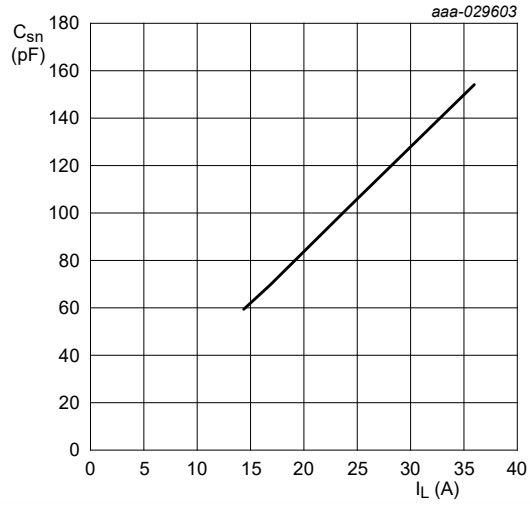
The Device Under Test (DUT) is carrying a freewheeling current. The switch in the high side of the test circuit in Fig. 22 will then turn on and force a transition at the switching node from low voltage to high voltage. This will cause the current in the DUT to change from freewheeling current to some negative current up until the point that the DUT is blocking the full DC supply voltage. If you integrate the negative current you will get the minority carrier stored change plus any output capacitance charge.

For GaN FETs, the charge on the output capacitance Q_{OSS} is the dominant component of the reverse recovery charge Q_r. Hence the reason that the datasheet for the Nexperia GaN FET specifies the same value for both Q_{OSS} and Q_r.

Some GaN device manufacturers will claim to have zero reverse recovery charge Qr because they do not have a PN junction body diode. However, they will still have Q_{OSS}.

9. Switching-node snubber

To achieve maximum efficiency and stability when switching high currents, a switching node RC snubber (R, C_{sn}) is recommended. For I_L < 14 A, a switching-node snubber is not required.



R_G = 30 Ω; τ = R_{SN} × C_{SN} = 1 ns

Fig. 23. Snubber capacitance as function of Load current

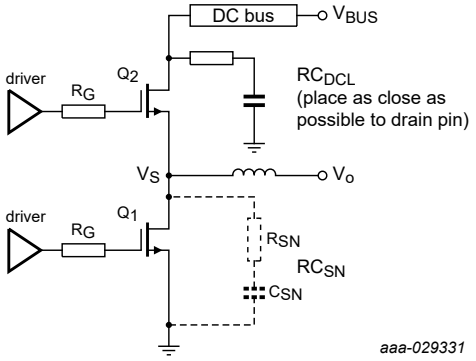


Fig. 24. DC-link snubber circuit

Note: a DC-link snubber is recommended in all cases. Optimal is 20 nF in series with 4 Ω, most easily achieved with parallel combination 10 nF and 8 Ω. This snubber lowers the Q factor of any resonance in the bus. That resonance will act as a load on the high gain amplifier that is the GaN FET and can lead to instability. For very high current, an RC snubber is recommended for the switching node. This will increase switching loss, so this is only recommended at high power levels where the losses are a very small percentage of the total power.

10. Revision history

Table 3. Revision history

Revision number	Date	Description
1.1	2019-02-13	Initial version
1.0	2018-11-09	Preliminary version

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