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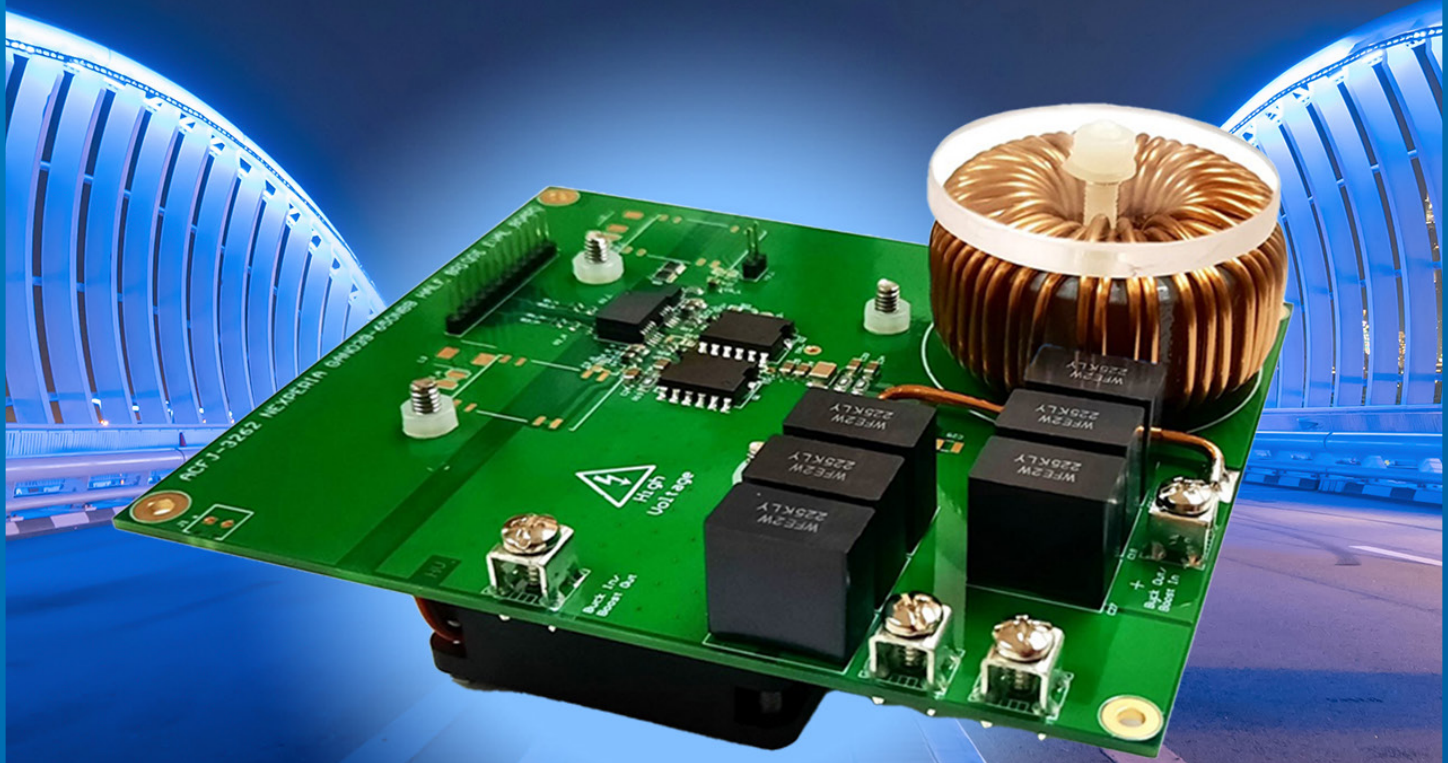

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Chapter 1: Introduction

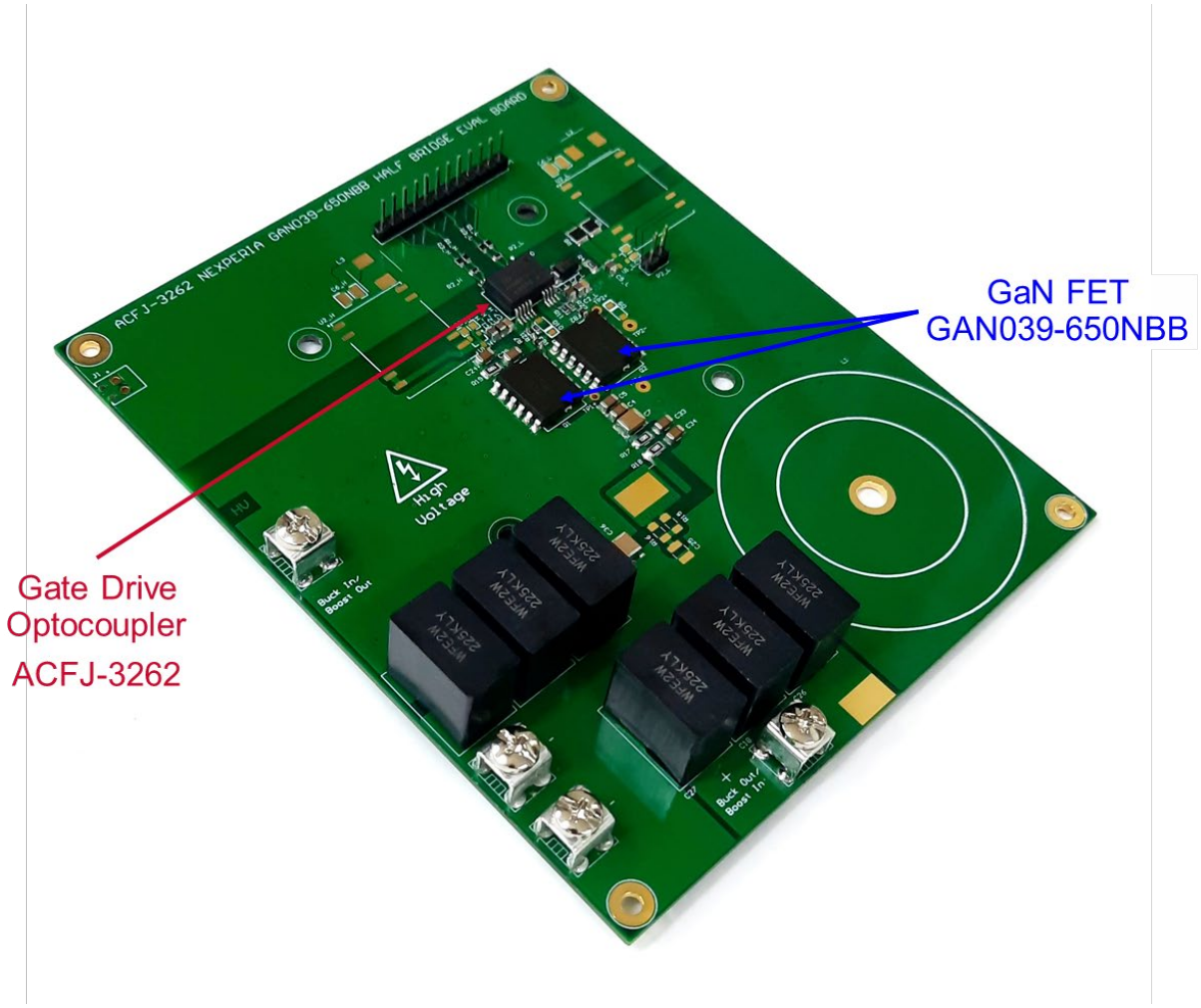
1.1 GaN Power Semiconductor

Gallium Nitride (GaN) power semiconductor is rapidly emerging into the commercial market delivering huge benefits over conventional Silicon-based power semiconductors. GaN can improve overall system efficiency with lower on-resistance and the higher switching capability can reduce the overall system size and costs. The technical benefits coupled with lower costs have increased the fast adoption of GaN power semiconductors in applications like industrial power supplies and renewable energy inverters.

Broadcom gate drive optocouplers have been used extensively in driving Silicon-based semiconductor like IGBT. This reference design will discuss how gate drive optocoupler, ACFJ-3262 can be used to drive GaN FET.

The half bridge evaluation board will feature ACFJ-3262, 10A dual channel gate drive optocoupler and Nexperia's GAN039-650NBB FET. The half bridge evaluation board enable the basic study of the switching characteristics and efficiency, by means of configuring for synchronous rectification, in either buck or boost mode. The high voltage input and output can operate at up to 400 V_{DC}, with the current limit of the inductor at 15-16A, dependent upon cooling, ambient temperature and switching frequency.

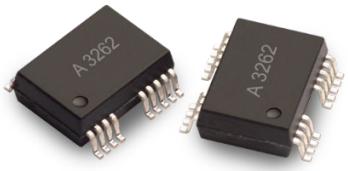
Figure 1 ACFJ-3262 Nexperia GAN039-650NBB Half Bridge Evaluation Board



1.2 Design Features

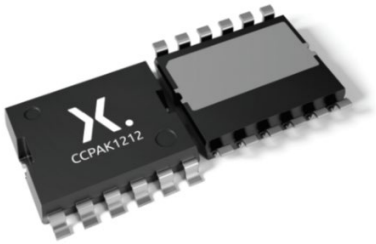
The ACFJ-3262 Nexperia GAN039-650NBB half bridge evaluation feature:

One ACFJ-3252 gate drive optocoupler



- 10A peak (typical), rail-to-rail output
- Separate source and sink outputs
- 95 ns max. propagation delay
- 100 kV/µs min. common mode rejection (CMR) at V_{CM} = 1000 V
- 8.6 V UVLO with hysteresis
- Wide operating V_{DD} Range: 10 to 25 V
- Wide Automotive temperature range: -40 ºC to 125º C
- Dual Channel in SO-24 package
- CTI>600V,
- >2.8mm channel-to-channel separation
- Safety Approval:
  - UL Recognized 5000 V_{RMS} for 1min.
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 1230 V_{PEAK}

Two GAN039-650NBB GaN FET



- Simplified driver design as standard level MOSFET gate drivers can be used:
  - 0 V to 12 V drive voltage
  - Gate threshold voltage V_{GSth} of 4 V
- Robust gate oxide with ±20 V V_{GS} rating
- High gate threshold voltage of 4 V for gate bounce immunity
- Low body diode V_f for reduced losses and simplified dead-time adjustments
- Transient over-voltage capability for increased robustness
- CCPAK package technology:
  - Improved reliability, with reduced $R_{th(j-mb)}$ for optimal cooling
  - Lower inductances for lower switching losses and EMI
  - 175 °C maximum junction temperature
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joints

Chapter 2: Board Description

2.1 Functional Block Diagram

The eval board has a half-bridge topology as shown in figure 2. Two pairs of high voltage ports, J2/J3 and J5/J7 serve as either high voltage input or output, depending on whether it is buck or boost configuration. In either case, one GaN FET acts as the active power switch while the other carries the freewheeling current. The latter device may be enhanced, as a synchronous rectifier, or not. With GaN FETs, the reverse recovery charge is low and there is no need for additional freewheeling diodes.

The high and low side PWM signals are connected to connector P1 which are used to drive the LEDs of ACFJ-3262 directly.

An inductor is provided as a starting point for investigation. This is a 330µH toroid intended to demonstrate a reasonable compromise between size and efficiency with the current limited at 15-16A and at a switching frequency of 100 kHz.

Figure 2 Half Bridge Evaluation Board Functional Block Diagram

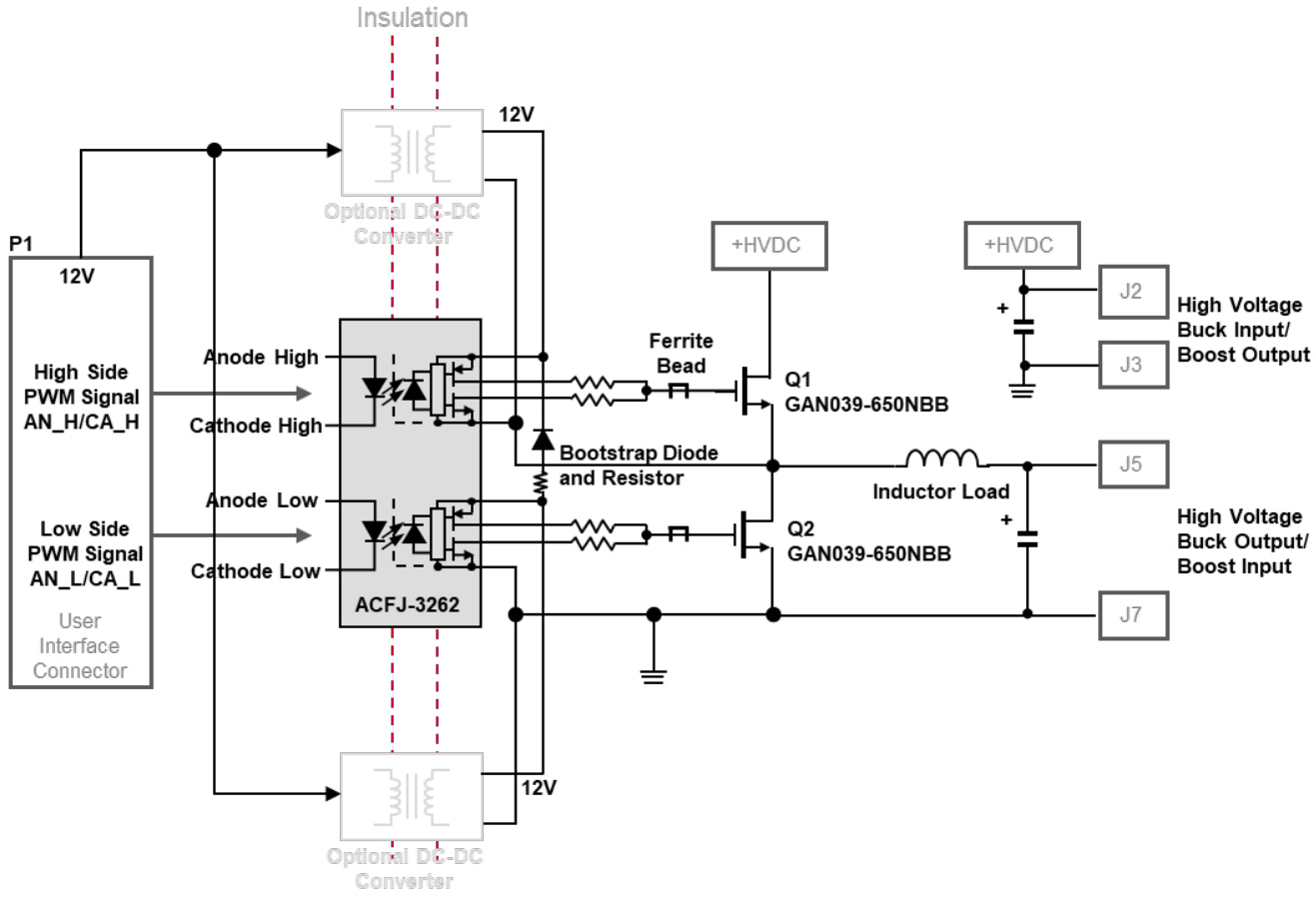
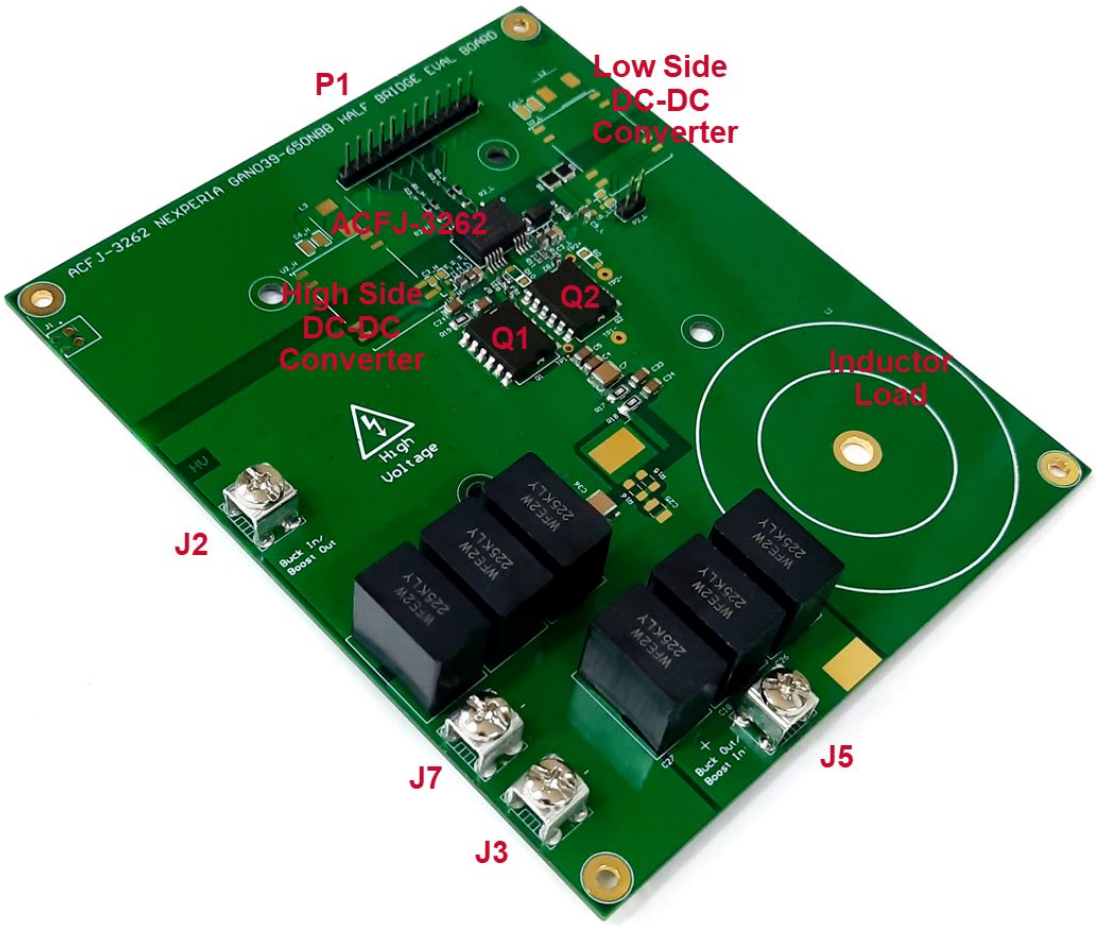


Figure 3 Functional Block Disposition on the Evaluation Board



2.2 Pin Assignment

Pin assignment for P1 connector is shown in table 1.

Table 1 Pin assignment of connector P1 (user interface connector)

Label	Function	Direction
DC12VIN	12V power supply. If DC-DC converter is not used, the 12V input can be applied either at P1 or J1, and R8 and R9 populated with 0Ω for the low side supply. High side supply can then be derived from the bootstrap circuit, D1 and R4. Alternatively, the 12V can also be used with DC-DC converter MGJ1D121505MPC-R7 to provide isolated power supply.	Input
NC	No connection.	NA
GND	Reference ground for the 12V power supply.	Input

NC	No connection.	NA
AN_L	5V PWM input signal for the low side driver. Connects to the anode of the low side gate driver.	Input
NC	No connection.	NA
CA_L	Reference ground for the low side driver PWM input signal. Connects to the cathode of the low side gate driver.	Input
NC	No connection.	NA
AN_H	5V PWM input signal for the high side driver. Connects to the anode of the high side gate driver.	Input
NC	No connection.	NA
CA_H	Reference ground for the high side driver PWM input signal. Connects to the cathode of the high side gate driver.	Input
NC	No connection.	NA

Pin assignment for P2, gate driver power supply connector is shown in table 2.There is no connection needed if DC-DC converters are used.

Table 2 Pin assignment of connector P2_L for gate driver, ACFJ-3262 power supply

Label	Function	Direction
P2_L, VDDL	Output stage low side power supply. Recommended 10 to 12V for the V_{GS} of the GaN FET. High side supply can then be derived from the bootstrap circuit, D1 and R4. DC-DC converters MGJ1D121505MPC-R7 are not needed if this power supply scheme is used.	Input
P2_L, PGND	Reference ground for the output stage low side power supply.	Input

High voltage BUS and Load connections are shown in table 3.

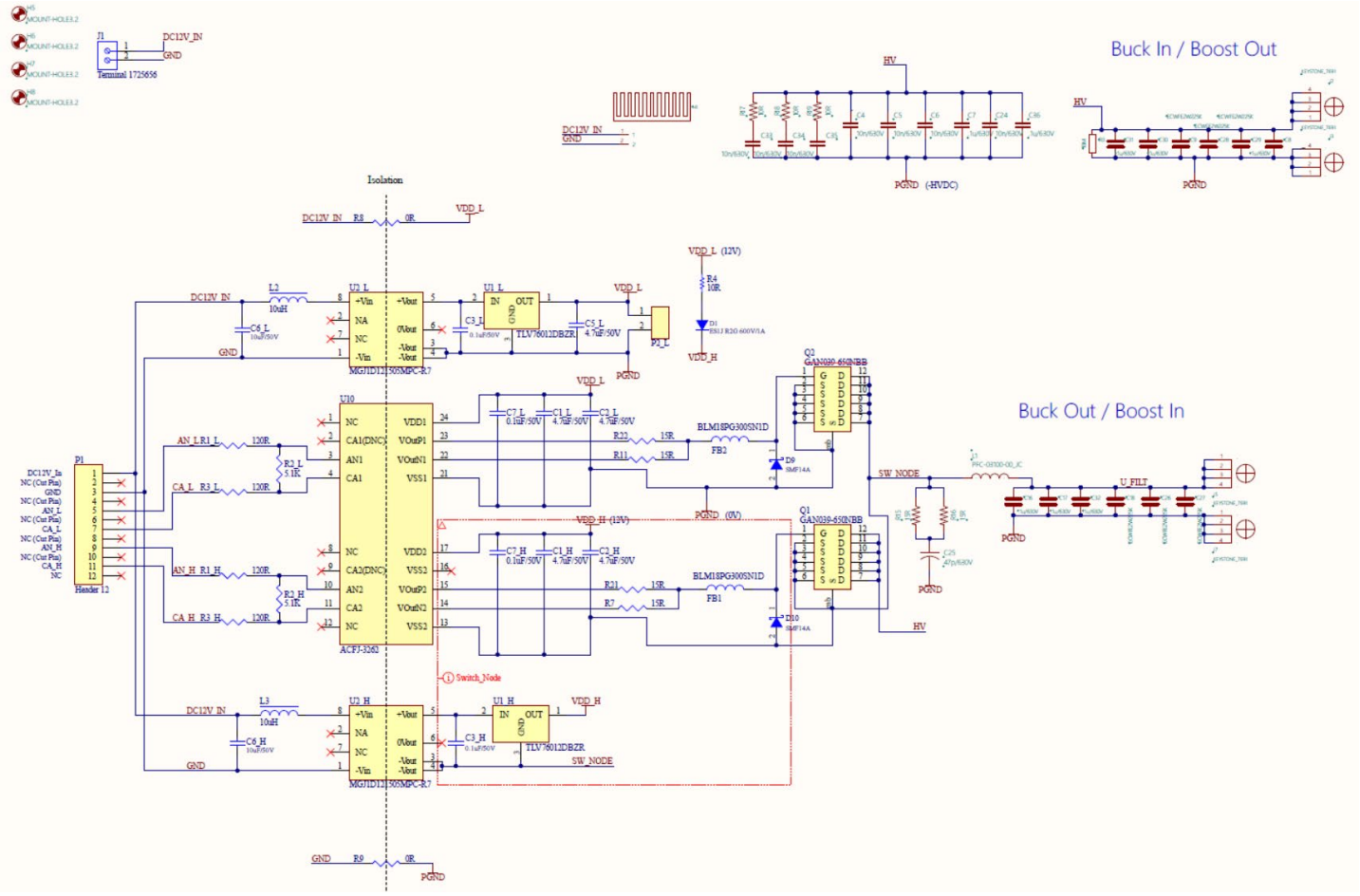
Table 3 High voltage BUS (+HVDC and –HVDC) and Load connection

Label	Function	Direction
J2(+HVDC), J5	High voltage input for Buck mode or high voltage output for Boost mode. The high voltage input and output can operate at up to 400V_{DC}.	Input/Output
J3, J7	Reference ground for the high voltage input or output.	Input/Output

Chapter 3: Circuit Description

The schematic of the half bridge evaluation board is shown in figure 4.

Figure 4 Schematic of the Half Bridge Evaluation Board



3.1 Input Connector and Power Supply Circuit

P1 is the 12 pins input connector that interface to the 12V supply and PWM signals.

In the standard setup where DC-DC converter is not used, the 12V input can be applied either at P1 or J1, and R8 and R9 populated with 0Ω for the low side supply. High side supply can then be derived from the bootstrap circuit, D1 and R4. Alternatively, external isolated 12V supply can also be connected to P2_L. In this case, there is no connection needed for DC12V_In at P1, and R8 and R9 should not be populated. Bootstrap power supply can then be used for the high side gate driver via bootstrap diode D1 and resistor R4.

For DC-DC converter setup, the 12V DC power supply can be connected to DC12V_In (Pin1) and GND (Pin 3) to provide isolated power supply to the secondary side via U2_L and U2_H. The Murata MGJ1D121505MPC-R7 is a 12V to +15V/-5V DC-DC converter and TLV76012DBZR is a 12v linear voltage regulator. They are used to provide 12V isolated supply to the high and low side gate driver optocoupler, U1.

3.2 Gate Driver Circuit

The half bridge evaluation board uses a dual-channel gate drive optocoupler U10, ACFJ-3262 to drive the GaN FETs directly. The ACFJ-3262 is a basic gate driver optocoupler used to isolate and drive the GaN FETs. It has a rail-to-rail output with 10A maximum output current to provide fast switching high voltage and driving current to turn-on and off the GaN efficiently.

The ACFJ-3262 has a propagation delay of less than 95ns. The very high CMR, common mode rejection of 100kV/μs(min.) is required to isolate high transient noise during the high frequency operation from causing erroneous outputs. It is certified by UL1577 for up to V_{ISO} 5000V_{RMS}/min and IEC 60747-5-5 for working voltage, V_{IORM} up to 1230V_{PEAK}.

The LED inputs of the gate driver use a split resistor network of 120ohm at the anode and cathode. This is to balance the input impedance of the LEDs to achieve the high CMR of 100kV/μs.

The ACFJ-3262 has a UVLO threshold voltage of 8.6V, suitable for 10 to 12V gate operation of the GaN FET GAN039-650NBB. It has dual output, VOutP1 and VOutP2 to control the turning on and off of the GaN FET via external 15ohm gate resistors, Rgon and Rgoff. With the 12V supply, this translates to approximate 0.8A peak current to the gate of the GaN FET.

Ferrite beads, FBL and FBH must be fitted in series with the gate of the GaN FET and should be located as close as possible to the gate pin. The gate-source loop should be kept as compact as possible to minimize the gate loop inductance. The Ferrite bead damps the resonant circuit made up of the gate source loop inductance and the GaN FET input capacitance, thus providing fast switching stability. BLM18PG300SN1D with an impedance of 30ohm @ 100 MHz is recommended.

14V TVS diodes D9 and D10, can be used to clamp and protect the gate of the GaN FET and gate driver output. However, the GaN FET does not require this diode for normal operation. The TVS diode has to be selected carefully to prevent adverse effect to the switching performance.

3.3 GaN FET Circuit

The half bridge evaluation board uses two GaN FETs, Q1 for the high side switch and Q2 for the low side switch. The GAN039-650NBB is a 650 V, 33 mΩ normally-off GaN FET that combines Nexperia’s latest high-voltage GaN HEMT H2 technology and low-voltage silicon MOSFET technologies in a CCPAK1212 package.

A DC-link snubber, which consists of R17/R18/R19 and C33/C34/C35 is recommended to lower the Q factor of any resonance in the HVDC bus. That resonance will act as a load on the high gain amplifier which is the GaN FET and can lead to instability. The remaining capacitors, C4-6/C17/C24.C36-16 are high frequency DC-link components, placed very close to the GaN FETs for fast switching half bridge operations.

Chapter 4: Buck and Boost Configurations

The buck and boost configurations are shown in figure 5 and 6. For buck mode, the HVDC input, J2/J3 is connected to the high voltage input supply and the output is taken from J5/J7. For boost mode, high voltage input supply is connected to J5/J7 and the output is taken from J2/J3.

Note that in boost mode, a load must be connected. The load current affects the output voltage up to the transition from discontinuous conduction mode(DCM) to continuous conduction mode (CCM). In buck mode the load may be an open circuit. In the case of buck mode with no load, the ripple current in the inductor is symmetric about zero, and the soft switching behaviour of the GaN FETs may be studied.

Figure 5 Schematic of the Half Bridge Evaluation Board for Buck Mode

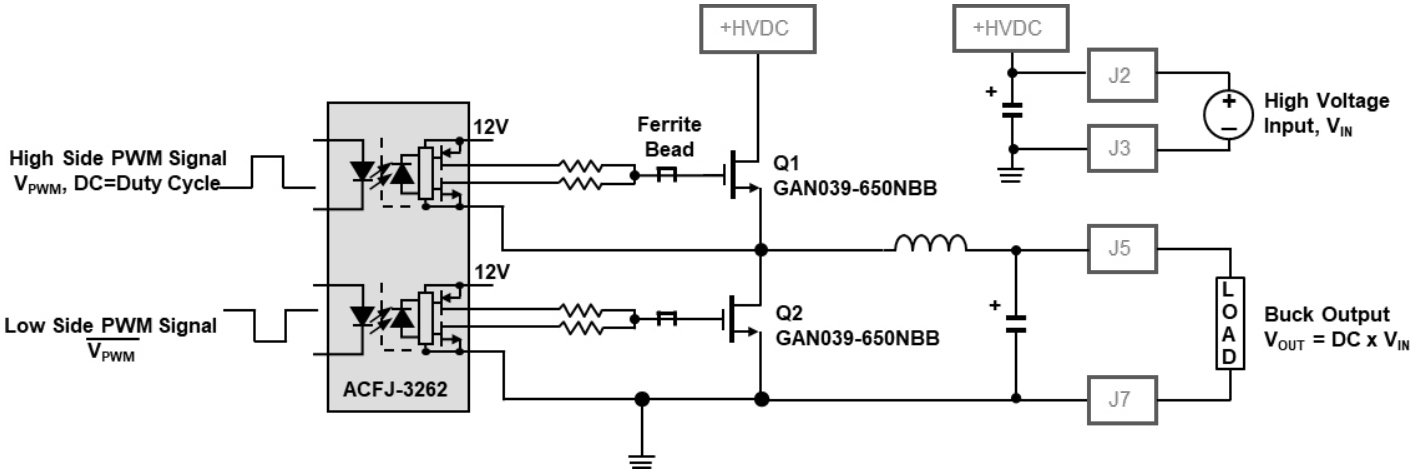
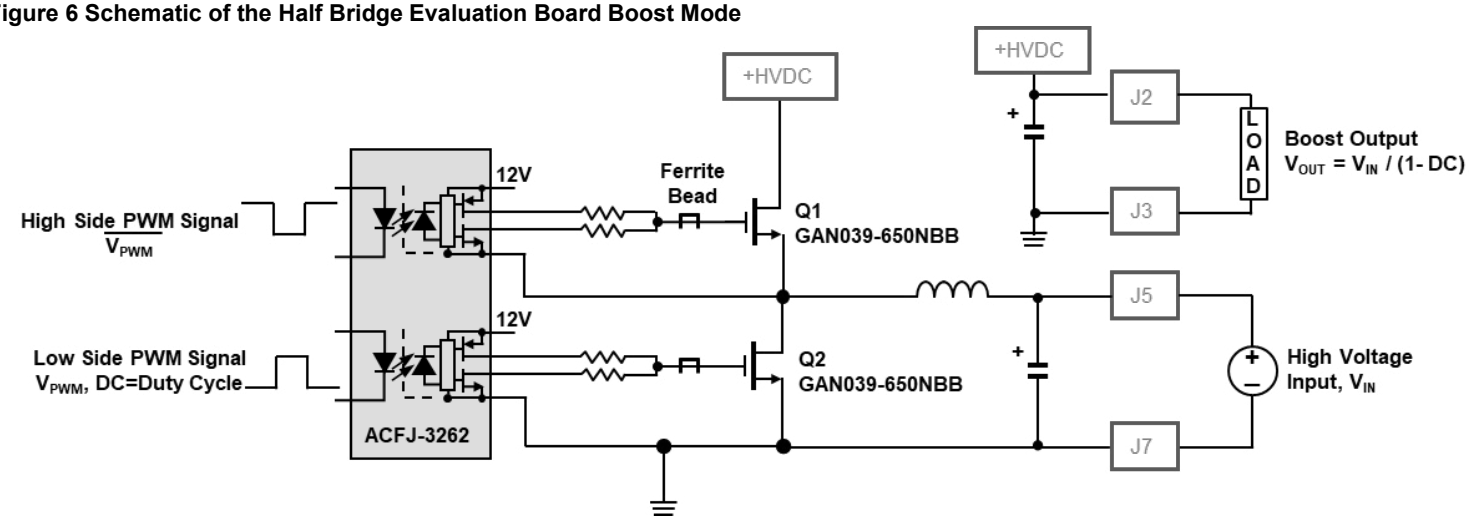


Figure 6 Schematic of the Half Bridge Evaluation Board Boost Mode



Chapter 5: Switching Waveforms and Efficiency Test

Figure 7 Multiple Pulse Tests at 400V BUS Voltage and Drain Current stepped to 60A

Figure 8 Switching Off at 28A

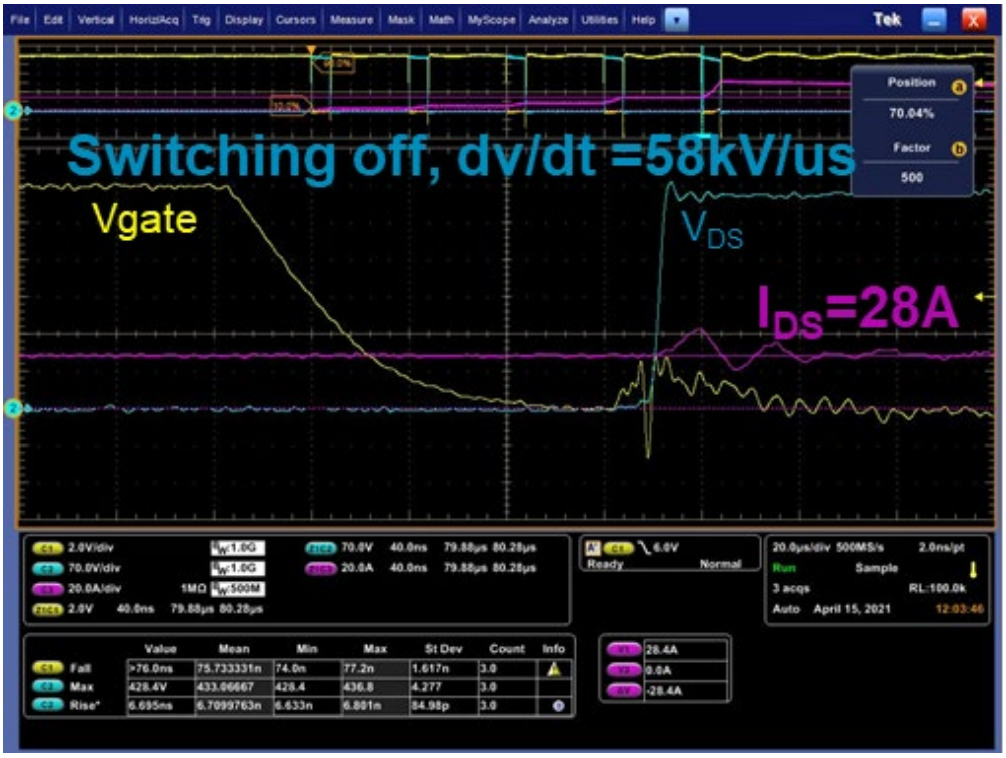
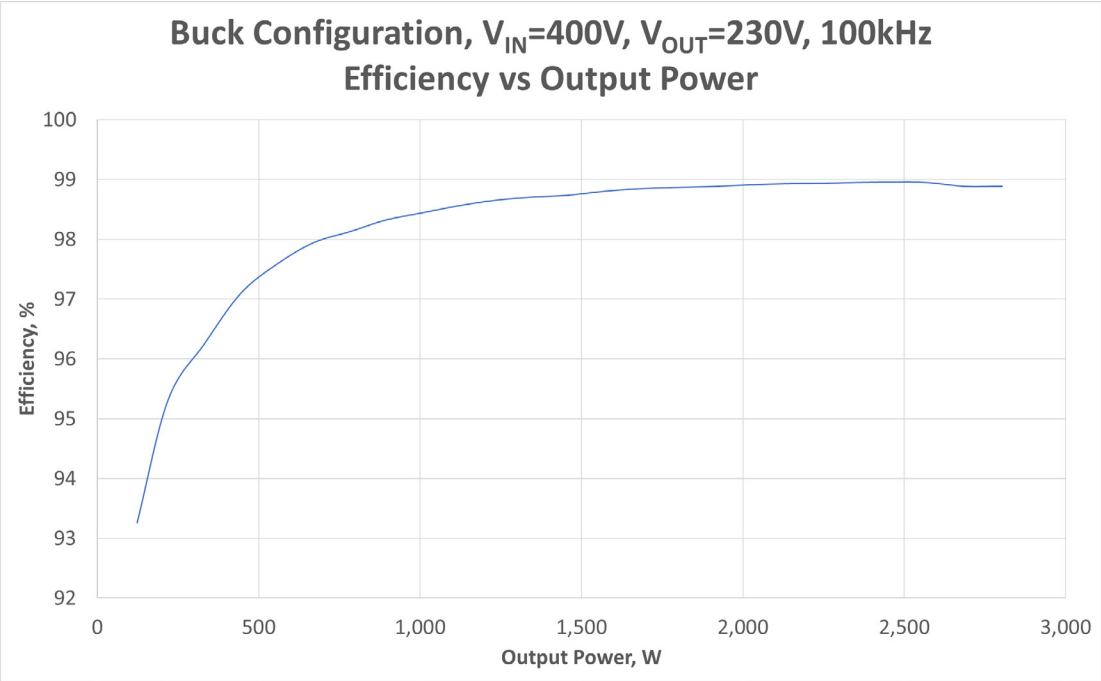


Figure 9 Switching On at 60A

Figure 10 Efficiency Sweep for Buck Conversion from 400V to 230V



Chapter 6: Schematics, Layout and BOM

This section gives full schematics, layout and bill of materials of the half bridge evaluation board. The intention behind providing this information is to enable customers to modifythe design according to specific requirements.

Figure 11 Schematic of the Half Bridge Evaluation Board

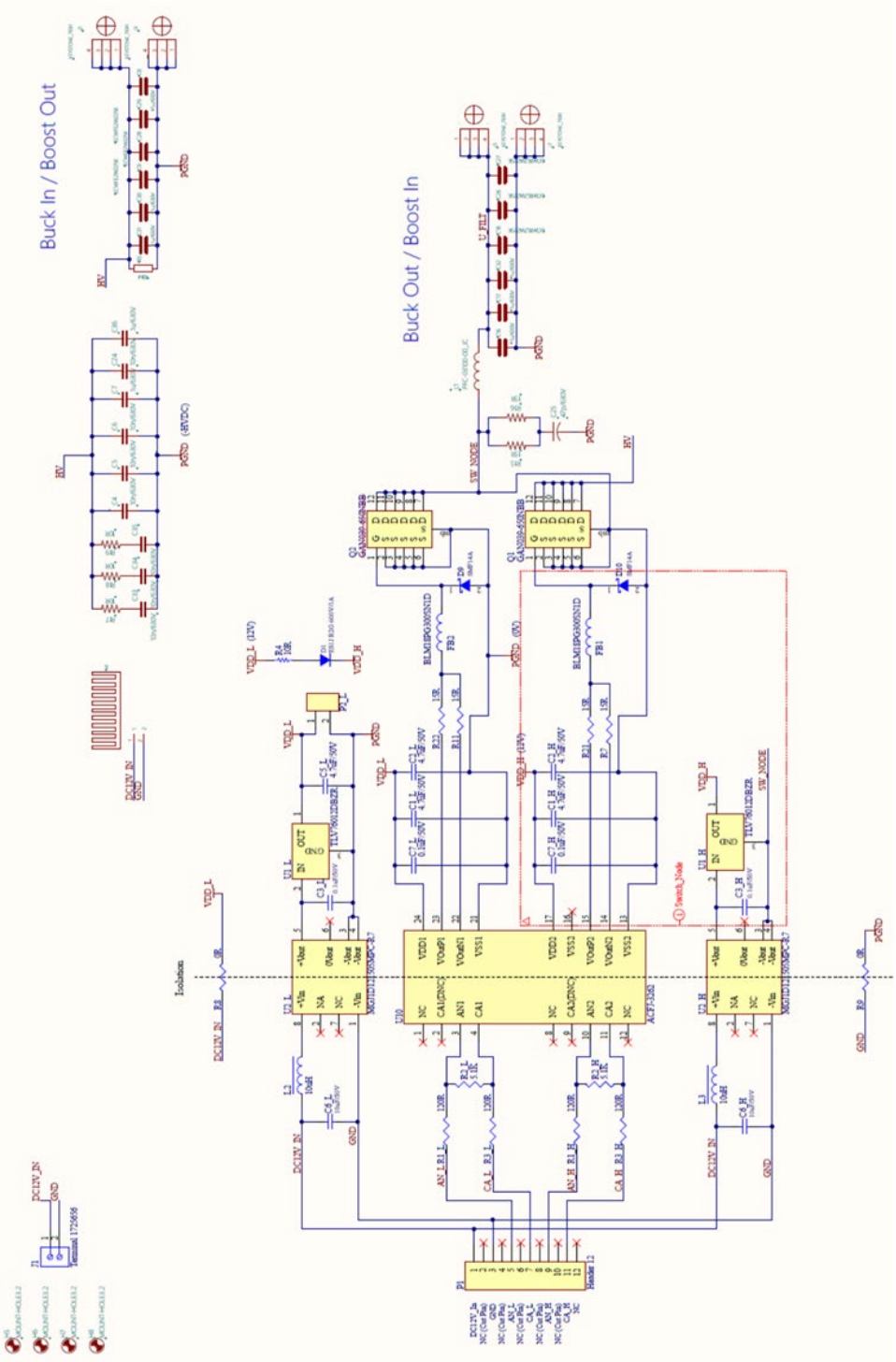


Figure 12 Top Level and Assembly Drawing

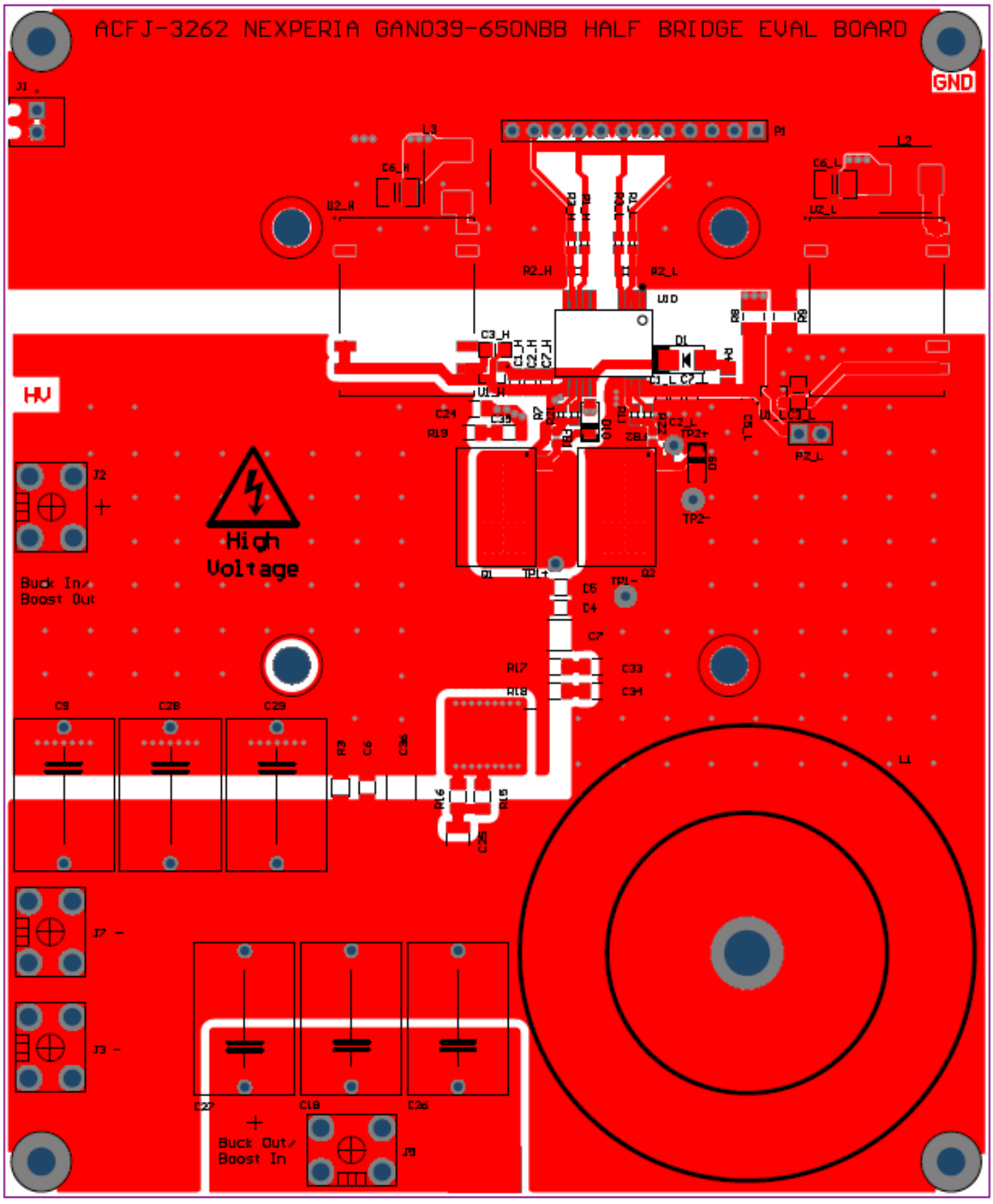


Figure 13 Signal Layer 1

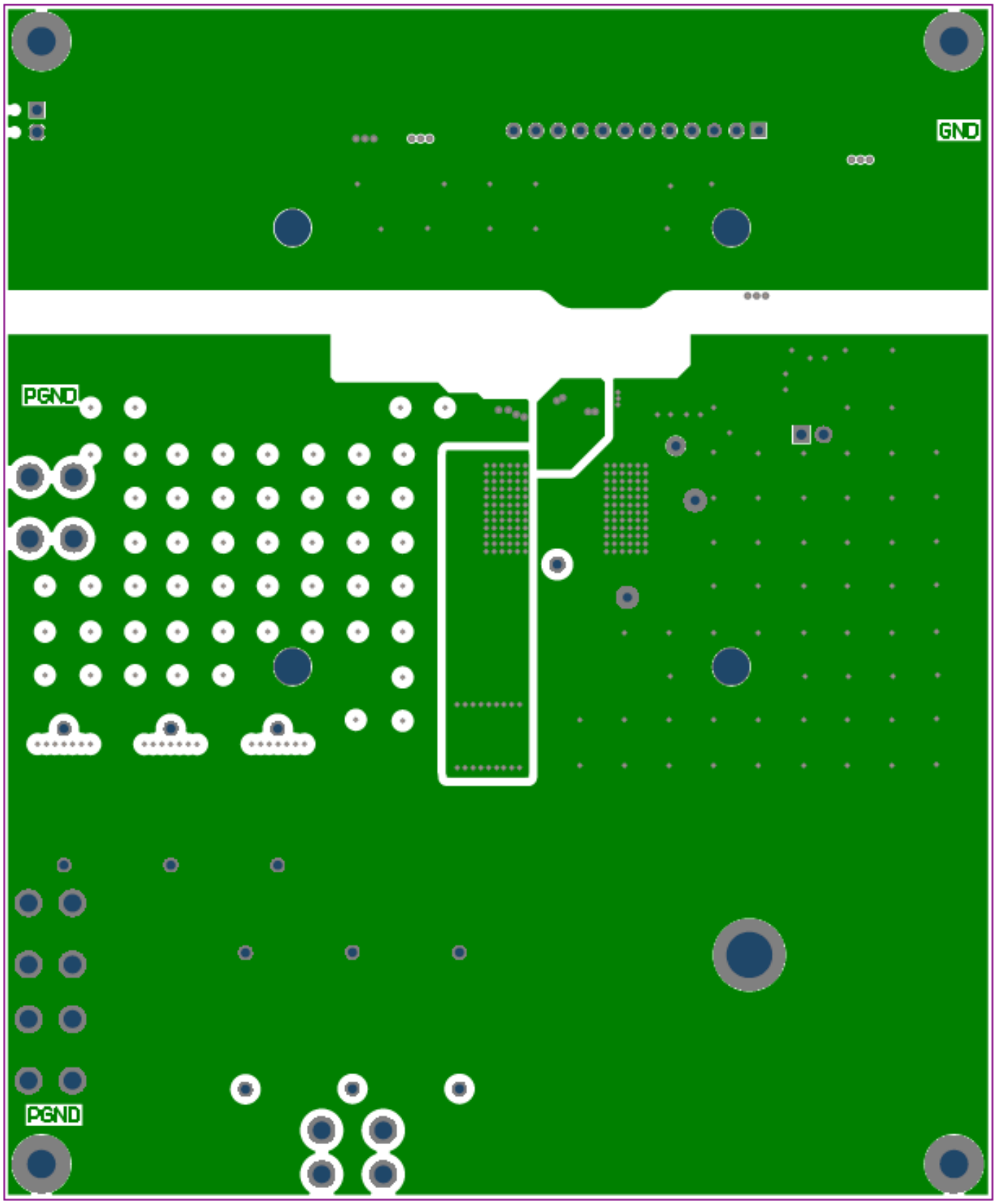


Figure 14 Signal Layer 2

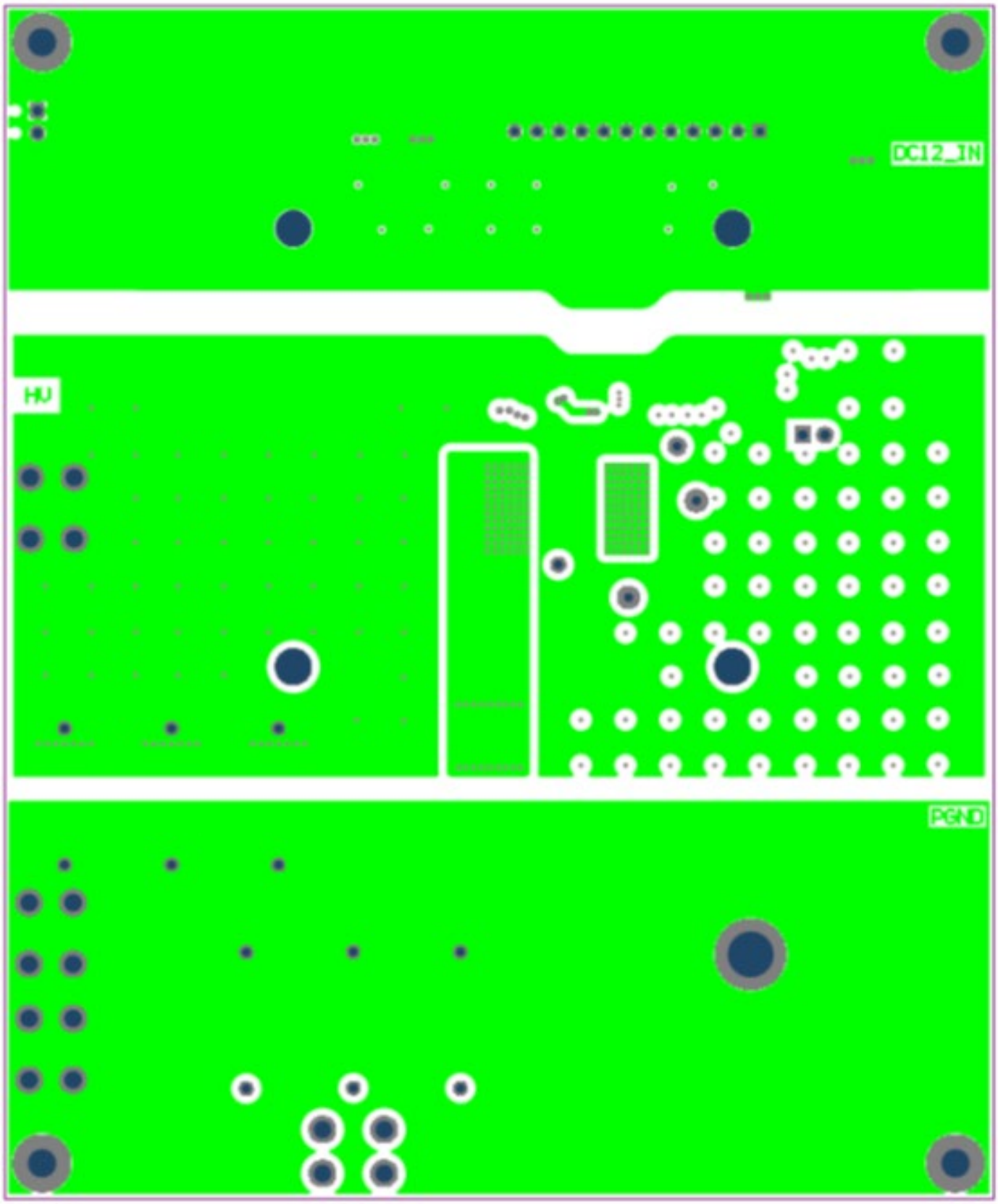


Figure 15 Bottom Layer

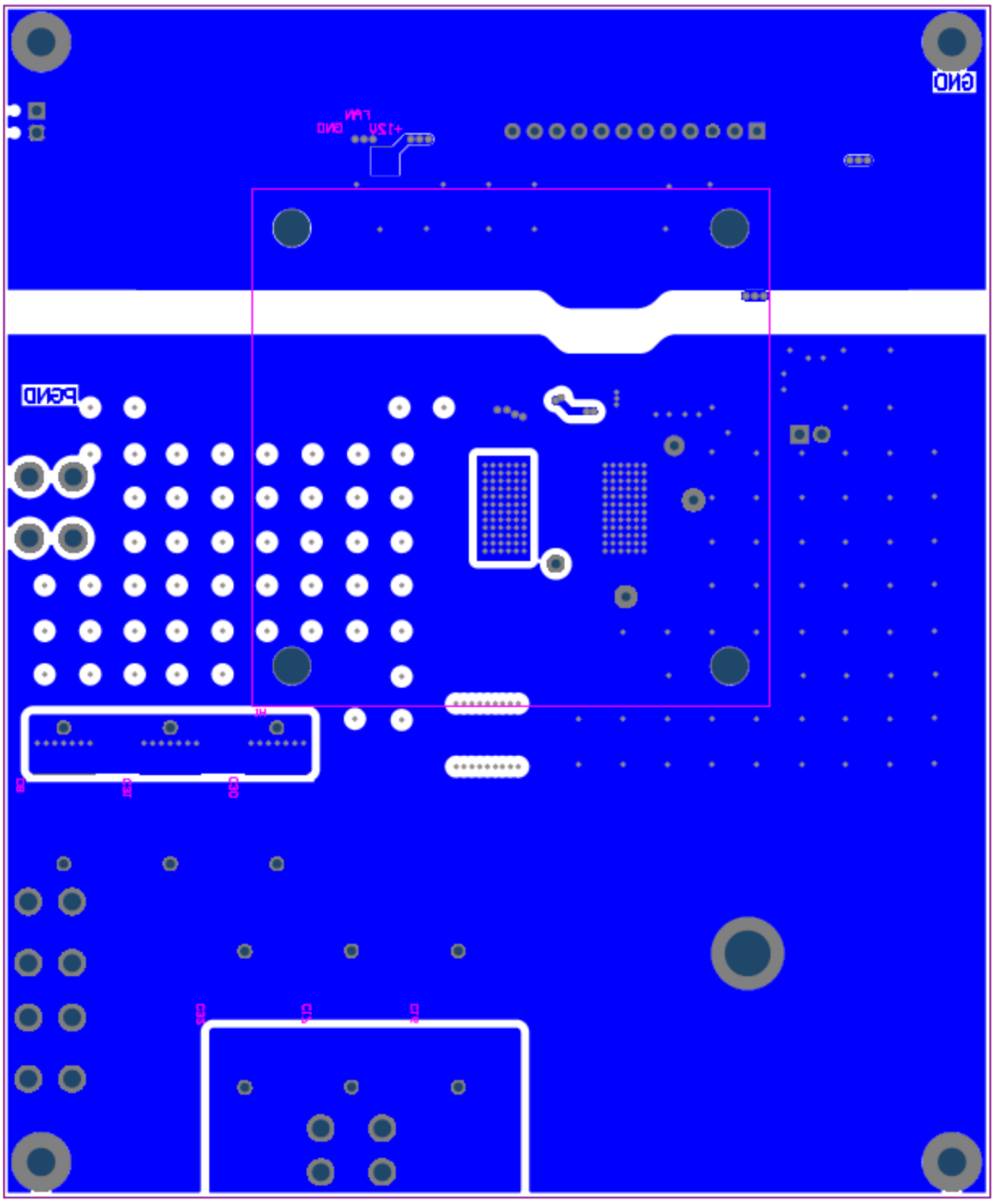


Table 4 Bill of Materials

Designator	Description	Mfr No	Footprint	Qty	Fitted
C1_H, C1_L, C2_H, C2_L, C5_L	Capacitor SMD 0805 4.7uF 50V 10% X7R	GRM21BZ71H475KE15L	C0805_N	5	Fitted
C3_H, C3_L	CAP CER 0.1UF 50V X7R 0805	C0805C104J5RACAUTO	C0805	2	Not Fitted
C4, C5, C6, C24, C33, C34, C35	10nF, 630V	SMK316B7103KF-T	C_1206_3216Metric	7	Fitted
C6_H, C6_L	Capacitor SMD 1210 10uF 50V 10% X7R	GRM32ER71H106KA12L	C1210	2	Not Fitted
C7, C36	100nF, 1000V	C1812C104KDRACTU	C_1812_4532Metric	2	Fitted
C7_H, C7_L	CAP CER 0.1UF 50V X7R 0805	C0805C104J5RACAUTO	C0805_N	2	Fitted
C8, C16, C17, C30, C31, C32	100nF, 1000V	C2220C104KDRACTU	C2220	6	Fitted
C9, C18, C26, C27, C28, C29	450V, 2.2µF	ECWFE2W225K	PHE450_2UF	6	Fitted
C25	Capacitor SMD, 47 pF, 1 Kv	MC1210N470J102CT	C_1210_3225Metric	1	Not Fitted
D1	Diode 35ns, 1A, 600V, Super Fast Recovery Rectifier	ES1J R2G	ES1J	1	Fitted
D9, D10	TVS DIODE 14V 23.2V SOD123F	SMF14A	SMF14A	2	Not Fitted
FB1, FB2	Ferrite Bead 30Ohm 1A 0603	BLM18PG300SN1D	BEADC160X80X95L40N	2	Fitted
H1	Heatsink 60x60 from Cool Innovation HS	3-282810MS76855	SR_Heatsinks	1	Fitted
	Heatsink phase change thermal material	CD-02-05-127			Fitted
	Heatsink thermal paste	120-2, 3354106			Fitted
	Heatsink M4 Nylon washer	TR NWE-34815-M4		4	Fitted
	Heatsink M4 Nylon nut	DURATOOL 1110040		4	Fitted
	Heatsink M4 x 3mm Nylon	DURATOOL DT000323		4	Fitted
	Heatsink DC Fan, 60x15mm, 12VDC,	MF60151V3-1000U-A99		1	Fitted
J1	Male Header, Pitch 2.54 mm, 1 x 2 Position, Height 9 mm, Tail Length 3.5 mm	1725656	1725656-2	1	Not Fitted
J2, J3, J5, J7	Screw Terminal	KEYSTONE_7691	KEYSTONE_7691	4	Fitted
L1	Inductor MPP Toroidal Core 125 PERM 46.7mm OD	55439A2	PFC-03100-00_JC	1	Fitted
	Inductor Nylon Nut M5 for Inductor	Duratool 1110050		1	Fitted
	Inductor Nylon Screw M5 x 40mm	TRNSE-1207-M5-40		1	Fitted
	Inductor Nylon Washer M5	TR NWE-34815-M5		1	Fitted
	Inductor Solderable PU Enamelled Copper, Unjacketed, 15 AWG, 2.08 mm^2, 105 ft, 32 m	ECW1.5			Fitted

L2, L3	Fixed Inductors 10uH 2.4A SMT	46103C	Murata 4600	2	Not Fitted
P1	Header, 12-Pin	Header 12	HDR1X12	1	Fitted
P2_L	Header Pin 0.100" 1x2Way Gold HD1X02	Header_1x2	HEADER_1X2	1	Fitted
Q1, Q2	650 V, 33 mOhm Gallium Nitride (GaN) FET	GAN039-650NBB	SOT8000	2	Fitted
R1_H, R1_L, R3_H, R3_L	Resistor SMD 0603 1/10W 1% 120R	CRCW0603120RFKEA	J1-0603	4	Fitted
R2_H, R2_L	Resistor SMD 0603 1/10W 1% 120R	ERJ-3EKF5101V	J1-0603	2	Fitted
R3	500V SMD 1206 10Mohm Resistor	ERJ-P08J106V	R_1206	1	Fitted
R4	Resistor SMD, anti-surge, 0.5W 10R	ERJP06F10R0V	R0805	1	Fitted
R7, R11, R21, R22	Resistor SMD 0.33W 1% 15R	CRCW060315R0FKEAHP	J1-0603	4	Fitted
R8, R9	0R Jumper SMD 1210 500mW 12A	CRCW12100000Z0EA	14-1210	2	Fitted
R15, R16	SMD Chip Resistor, 15 ohm, ± 1%, 660 mW	ERJUP8F15R0V	R_1206_3216Metric	2	Not Fitted
R17, R18, R19	SMD Chip Resistor, 10 ohm, ± 1%, 660 mW	ERJP08F10R0V	R_1206_3216Metric	3	Fitted
U1_H, U1_L	100-mA, 30-V wide-VIN, fixed-output linear voltage regulator	TLV76012DBZR	SOT95P245X110-3N	2	Not Fitted
U2_H, U2_L	DC DC CONVERTER 15V -5V 1W	MGJ1D121505MPC-R7	MGJ1DXXXXXXMPC	2	Not Fitted
U10	ACFJ-3262	ACFJ-3262	SO24	1	Fitted

Appendix A: Acknowledgement

Broadcom would like to thank Sebastian Klötzer (Principal Application Engineering), Scott Durkin (Senior GaN Applications Engineer) and Joyce Yu (Senior Strategic Marketing Manager), Nexperia for designing and testing the half bridge evaluation board.

Appendix B: Revision History

Version 1.0; Feb 2021

Initial document version.

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