BittWare a molex company

XUP-P3R
PCIe FPGA Board

UltraScale+ PCIe board with Quad QSFP and 512 GBytes DDR4

BittWare's XUP-P3R is a 3/4-length PCIe x16 card based on the Xilinx Virtex UltraScale+ FPGA. The UltraScale+ devices deliver high-performance, high-bandwidth, and reduced latency for systems demanding massive data flow and packet processing. The board offers extensive memory configurations supporting up to 512 GBytes of memory, sophisticated clocking and timing options, and four front panel QSFP cages, each supporting up to 100 Gbps (4x25) - including 100GbE.

The XUP-P3R also incorporates a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform integration and management. All of these features combine to make the XUP-P3R ideal for a wide range of data center applications, including network processing and security, acceleration, storage, broadcast, and SigInt.

Tool Flow Flexibility for Software- or Hardware-Based Development

BittWare OpenCL FPGA Tools

- SDAccel support for software-orientated customers
- Abstration for faster development
- Compiler, debugger, and profiler with with support for standard OpenCL APIs
- Add optimized HDL IP cores to OpenCL designs as libraries

BittWare HDL FPGA Tools

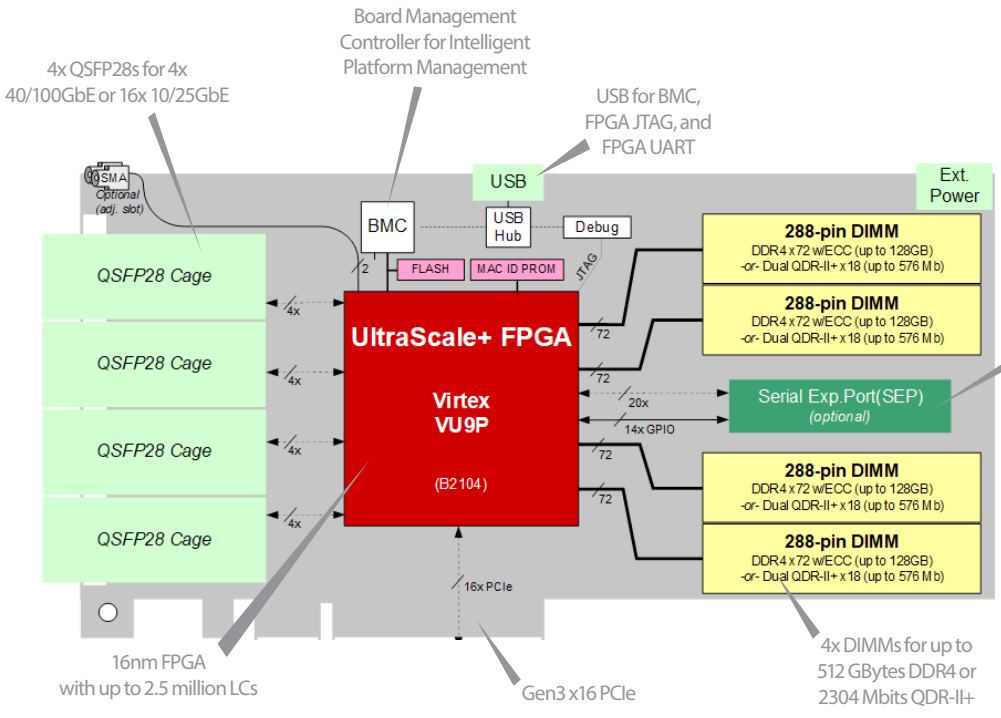
- Traditional VHDL/Verilog support for hardware-orientated customers
- Hand-code for ultimate performance
- High-Level Synthesis (HLS) available for rapid development
- FPGA card designed to support standard Xilinx IP cores for UltraScale+

key features

4x 100GbE via 4 QSFP28

Up to **512 GBytes** DDR4

Up to VU9P: **2.5 million LCs** FPGA by Xilinx



Serial Expansion Interface

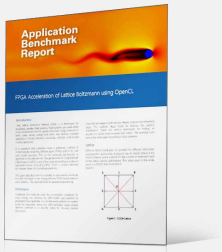
Optimize the XUP-P3R for your application with expansion:

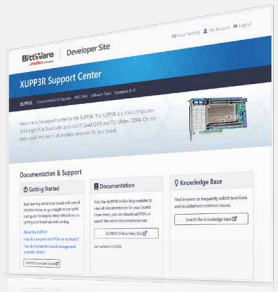
- Board-to-board interconnect
- Connect to accessory boards for customization options such as x16 PCIe or 4x 100G
- Includes GPIO

Inquire about customized Molex connectors/cables as required for your application.

Additional Services

Take advantage of BittWare's range of design, integration, and support options





Customization

Additional specification options or accessory boards to meet your exact needs.

Server Integration

Available pre-integrated in our TeraBox servers in a range of configurations.

Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.

Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

FPGA	• Virtex UltraScale+
	  • VU9P
	  • Core speed grade - 2
	• Contact BittWare for additional FPGA options

External memory	• 4 DIMM sites, each supporting*:
	  • Up to 128 GBytes DDR4 x72 with ECC
	  • Up to 576 Mbits dual QDR-II+ x18 (2 independent 288 Mbit banks)

Host interface	• x16 Gen3 interface direct to FPGA
USB header	• Micro USB: (USB 2.0) for debug and programming FPGA and Flash
Serial expansion port (SEP)	• Expansion interface to FPGA via 20x GTY transceivers (optional; requires second slot) • 14x GPIO signals to the FPGA
QSFP cages	• 4 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 16 transceivers • Each supports 100GbE, 40GbE, 4x 25GbE, or 4x 10GbE and can be combined for 400GbE
On-board Flash	• Flash memory for booting FPGA

* DIMM sites 1/2 and sites 3/4 must have the same memory type, or be empty.

Board Management Controller	• Voltage, current, temperature monitoring • Power sequencing and reset • Field upgrades • FPGA configuration and control • Clock configuration • I^2C bus access • USB 2.0 • Voltage overrides
Cooling	• Standard: double-width active fan and heatsink • Optional: double-width passive heatsink • Optional: double-width advanced passive cooling with heatpipes
Electrical	• On-board power derived from 12V PCIe slot & an AUX connector (6-pin) • Power dissipation is application dependent
Environmental	• Operating temperature 5°C to 35°C
Size	• ¾-length, standard-height PCIe dual-slot card • 9.4 x 4.37 inches

Development Tools

FPGA development	• FPGA Examples - example Vivado projects

Application development	• HDL/verilog
	  • BittWorks II Toolkit - host, command, and debug tools for BittWare hardware
	  • Xilinx Vivado® Design Suite
	• OpenCL - Xilinx SDAccel Development Environment, SDAccel Platform Release and pre-built examples for XUP-P3R

XILINX
ALLIANCE PROGRAM
CERTIFIED

To learn more, visit **www.BittWare.com**

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