GAN039-650NBB

650 V, 33 mOhm Gallium Nitride (GaN) FET in a CCPAK1212 package

28 May 2024 | Product data sheet

1. General description

The GAN039-650NBB is a 650 V, 33 mΩ Gallium Nitride (GaN) FET in a CCPAK1212 package. It is a normally-off device that combines Nexperia's latest high-voltage GaN HEMT H2 technology and low-voltage silicon MOSFET technologies — offering superior reliability and performance.

2. Features and benefits

- Simplified driver design as standard level MOSFET gate drivers can be used:
  - 0 V to 12 V drive voltage
  - Gate threshold voltage V_{GSth} of 4 V
- Robust gate oxide with ±20 V V_{GS} rating
- High gate threshold voltage of 4 V for gate bounce immunity
- Low body diode V_f for reduced losses and simplified dead-time adjustments
- Transient over-voltage capability for increased robustness
- CCPAK package technology:
  - Improved reliability, with reduced $R_{th(j-mb)}$ for optimal cooling
  - Lower inductances for lower switching losses and EMI
  - 150 °C maximum junction temperature
  - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joints

3. Applications

- Hard and soft switching converters for industrial and datacom power
- Bridgeless totempole PFC
- PV and UPS inverters
- Servo motor drives

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	-	650	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	58.5	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	250	W
T_j	junction temperature			-55	-	150	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 32 A; T_j = 25 °C; Fig. 10		-	33	39	mΩ
		V_{GS} = 10 V; I_D = 32 A; T_j = 150 °C; Fig. 11		-	73	86	mΩ

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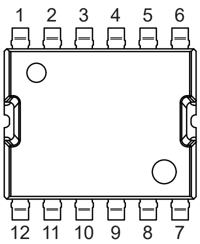
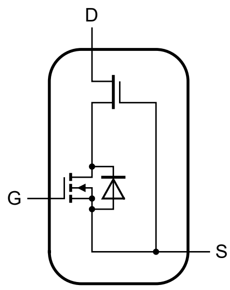
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 32 A; V_{DS} = 400 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 12; Fig. 13		-	5	-	nC
$Q_{G(tot)}$	total gate charge			-	26	-	nC
Source-drain diode							
Q_r	recovered charge	I_S = 32 A; dI_S/dt = -1000 A/µs; V_{GS} = 0 V; V_{DS} = 400 V; Fig. 20	[2]	-	187	-	nC

[1] The ID value is calculated based on the maximum thermal resistance from junction to mounting base and the RDSon
[2] Qr = Qoss +Qd where Qd is charge associated with minority carriers in the body diode of the Si mosfet of the cascode.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 **CCPAK1212 (SOT8000)**	 aaa-028116
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	S	source		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	S	mounting base; connected to source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GAN039-650NBB	CCPAK1212	Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 9.4 mm x 2.5 mm body	SOT8000

7. Marking

Table 4. Marking codes

Type number	Marking code
GAN039-650NBB	039INBB

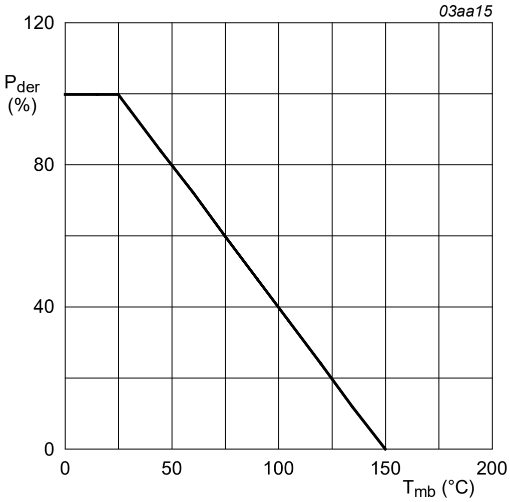
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

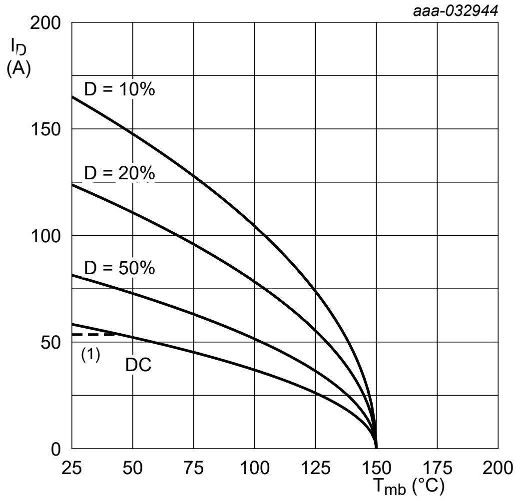
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	650	V
V_{TDS}	transient drain to source voltage	pulsed; t_p = 1 μs; δ_{factor} = 0.01		-	725	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	250	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	58.5	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	37	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C; Fig. 3		-	234	A
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C; V_{GS} = 0 V		-	58.5	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C		-	234	A

[1] The ID value is calculated based on the maximum thermal resistance from junction to mounting base and the RDSon



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

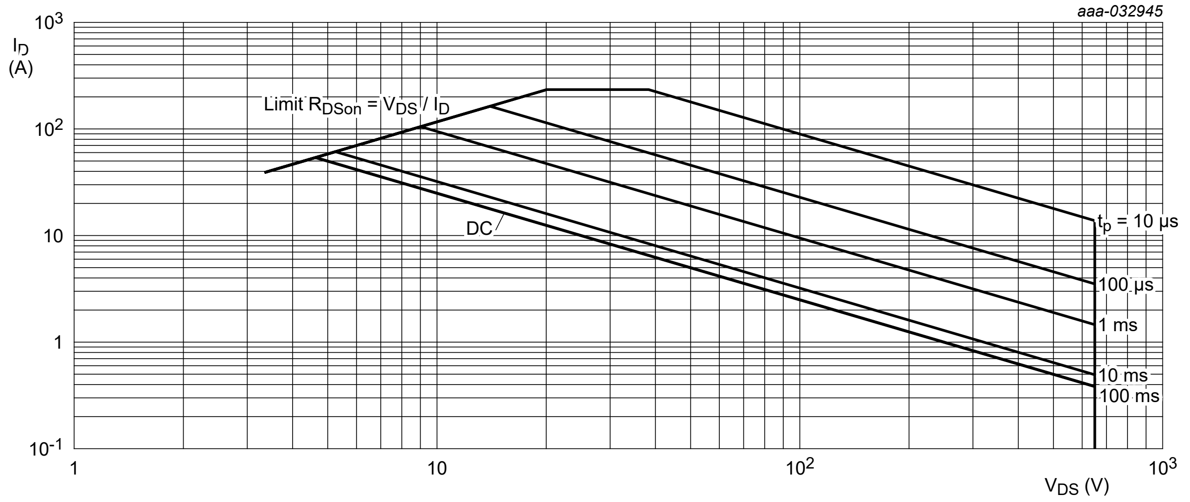
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



V_{GS} ≥ 10 V

(1) 53.5A DC continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	0.39	0.5	K/W

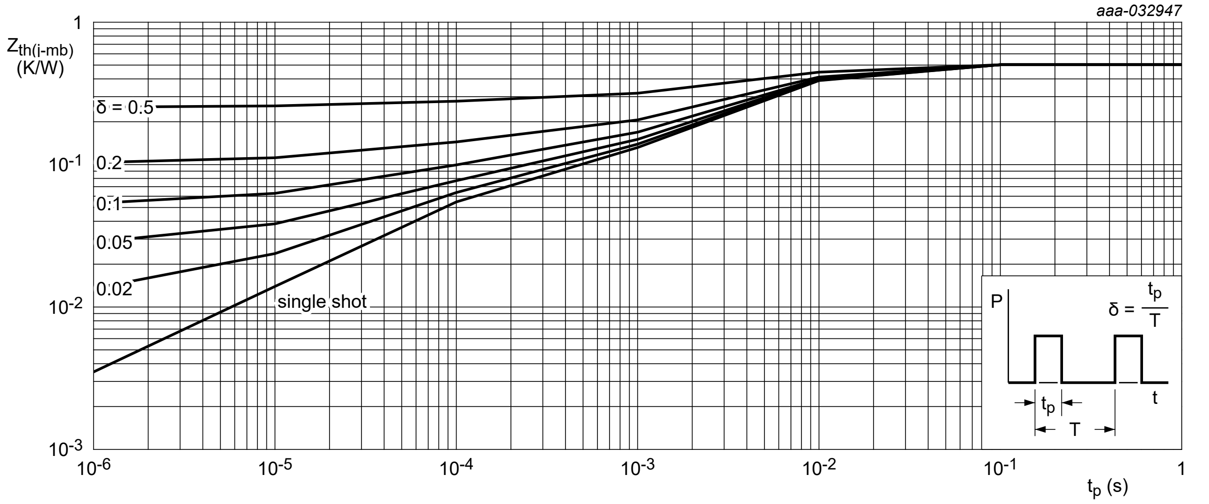


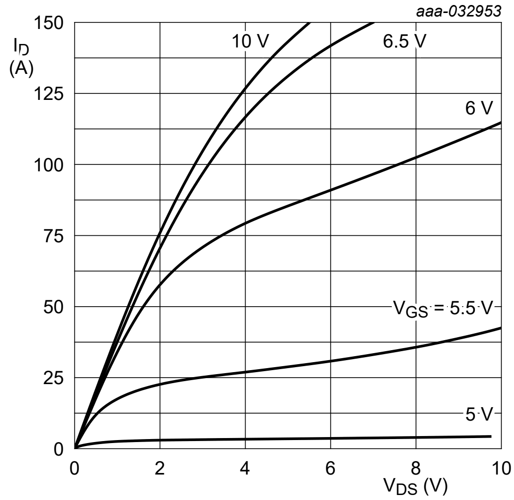
Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

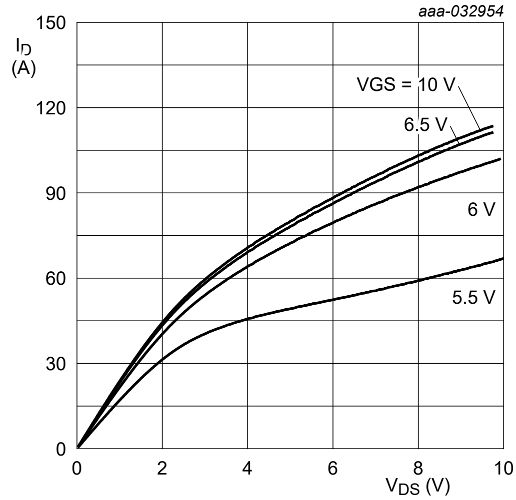
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		3.4	3.9	4.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 150 °C; Fig. 9		2.4	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 9		-	-	5.2	V
I_{DSS}	drain leakage current	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C		-	2.5	20	µA
		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 150 °C		-	6	-	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	400	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	400	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 32 A; T_j = 25 °C; Fig. 10		-	33	39	mΩ
		V_{GS} = 10 V; I_D = 32 A; T_j = 150 °C; Fig. 11		-	73	86	mΩ
R_G	gate resistance	f = 1 MHz		0.2	0.5	1.3	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 32 A; V_{DS} = 400 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 12; Fig. 13		-	26	-	nC
Q_{GS}	gate-source charge			-	10.2	-	nC
Q_{GD}	gate-drain charge			-	5	-	nC
C_{iss}	input capacitance	V_{DS} = 400 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 14		-	1980	-	pF
C_{oss}	output capacitance			-	144	-	pF
C_{rss}	reverse transfer capacitance			-	1.6	-	pF
$C_{o(er)}$	effective output capacitance, energy related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 15		-	218	-	pF
$C_{o(tr)}$	effective output capacitance, time related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		-	432	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 400 V; R_L = 12.5 Ω; V_{GS} = 12 V; $R_{G(ext)}$ = 12 Ω; Fig. 16; Fig. 17		-	17	-	ns
t_r	rise time			-	10	-	ns
$t_{d(off)}$	turn-off delay time			-	28	-	ns
t_f	fall time			-	9	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 400 V; Fig. 18		-	173	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 32 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 19		-	1.6	-	V
		I_S = 16 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 19		-	1.2	-	V
t_{rr}	reverse recovery time	I_S = 32 A; dI_S/dt = -1000 A/µs; V_{GS} = 0 V; V_{DS} = 400 V; Fig. 20		-	25	-	ns
Q_r	recovered charge		[1]	-	187	-	nC

[1] Qr = Qoss +Qd where Qd is charge associated with minority carriers in the body diode of the Si mosfet of the cascode.



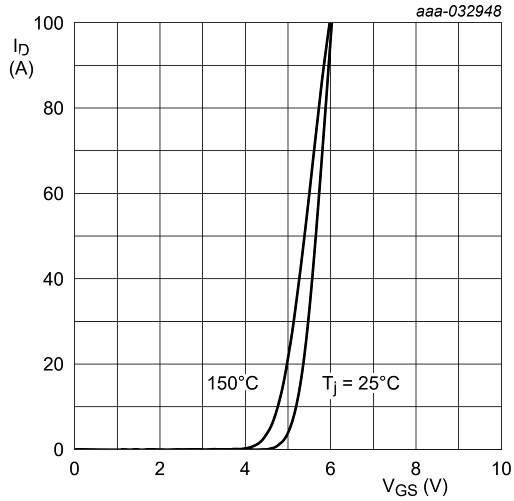
T_j = 25 °C

Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values



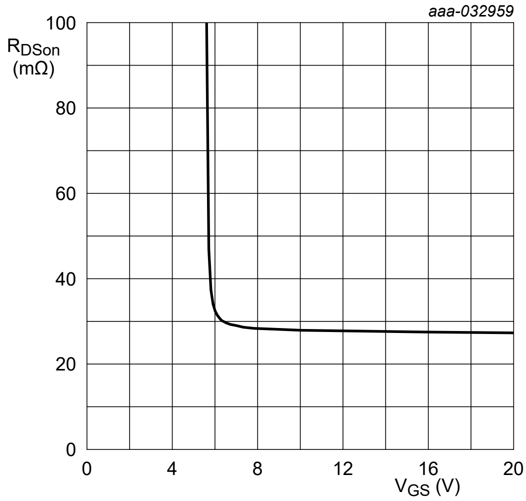
T_j = 150 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



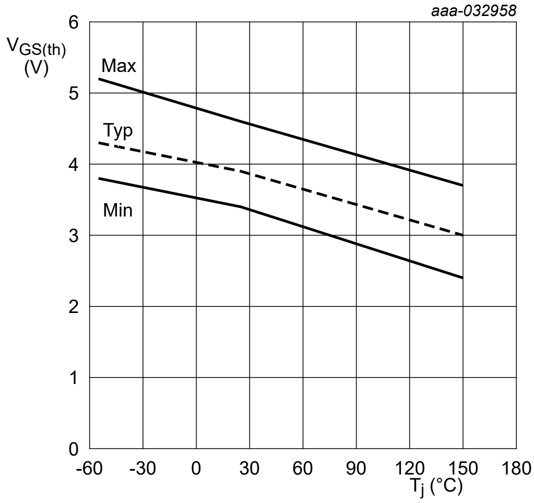
V_{DS} = 8 V

Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values



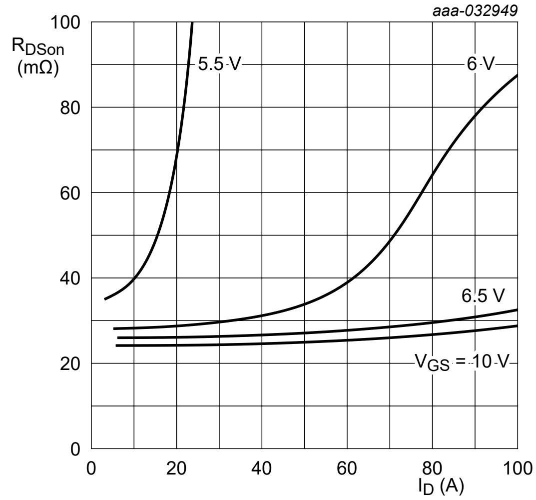
T_j = 25 °C; I_D = 32 A

Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



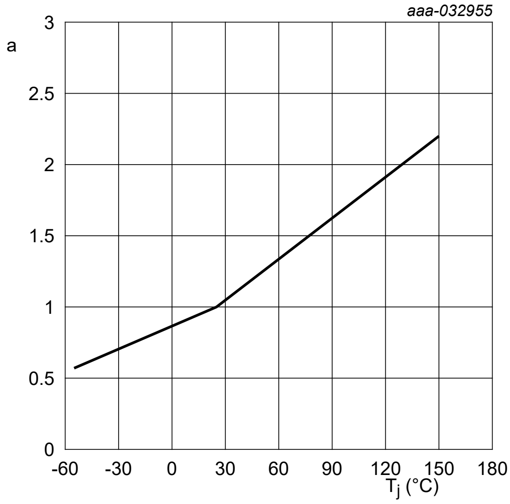
I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 9. Gate-source threshold voltage as a function of junction temperature



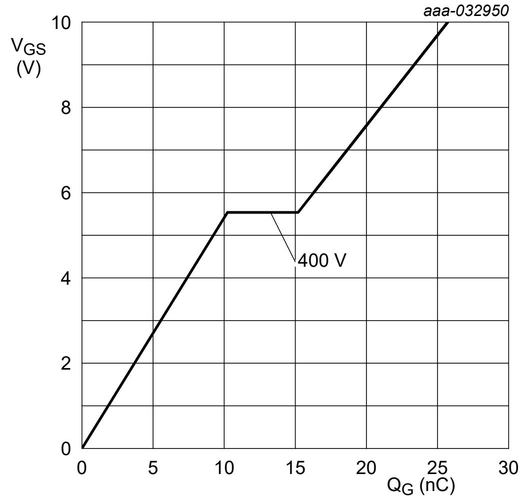
T_j = 25 °C

Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 32 A

Fig. 12. Gate-source voltage as a function of gate charge; typical values

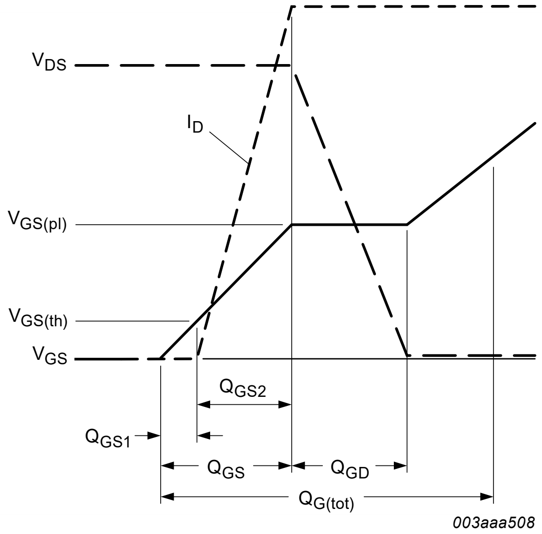


Fig. 13. Gate charge waveform definitions

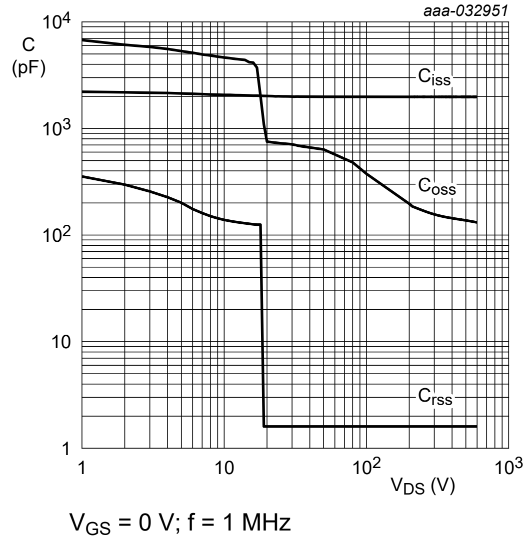


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

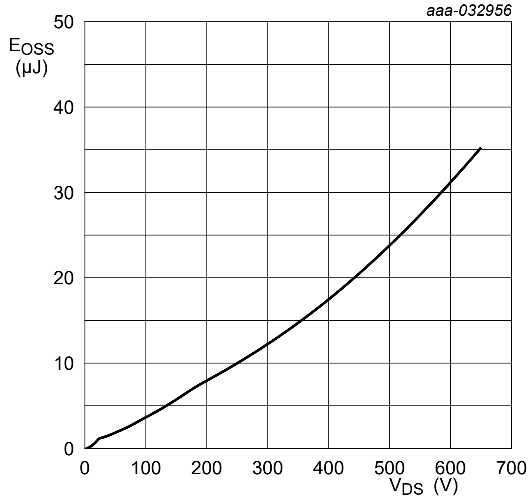


Fig. 15. Typical COSS Stored Energy

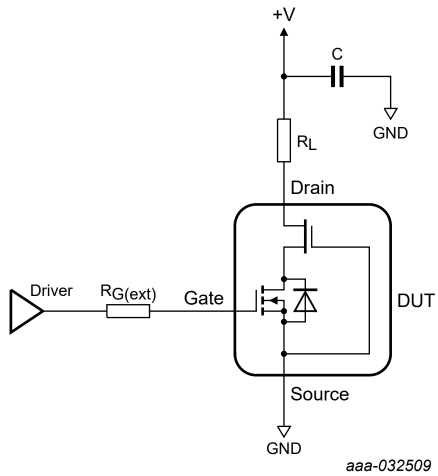


Fig. 16. Switching time test circuit

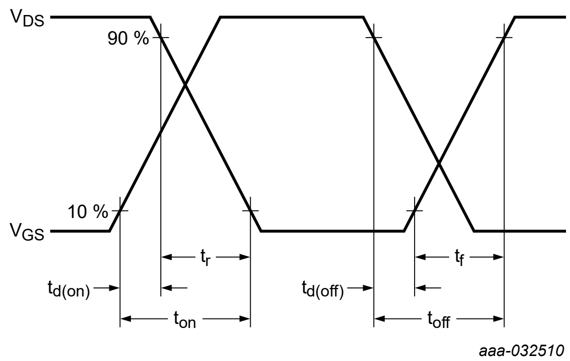


Fig. 17. Switching time waveform

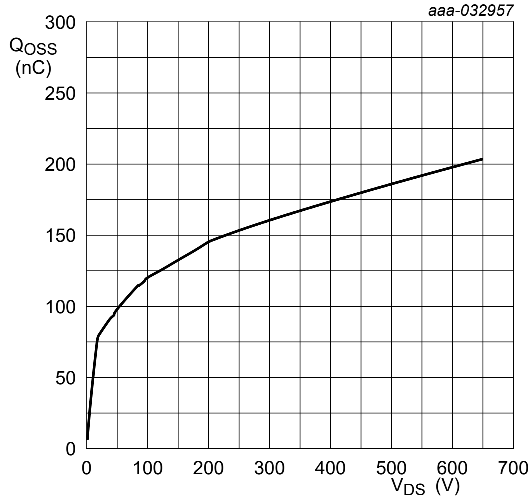
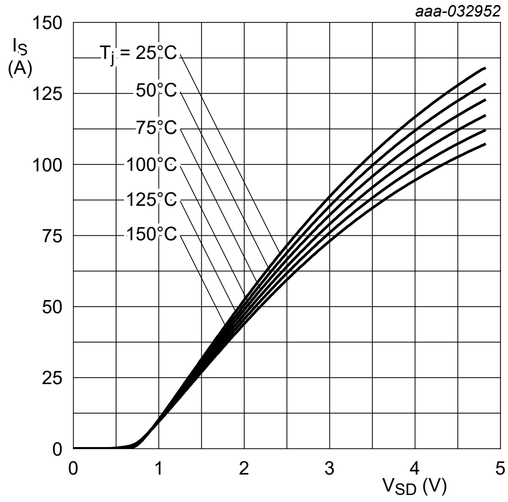


Fig. 18. Typical QOSS



V_{GS} = 0 V

Fig. 19. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

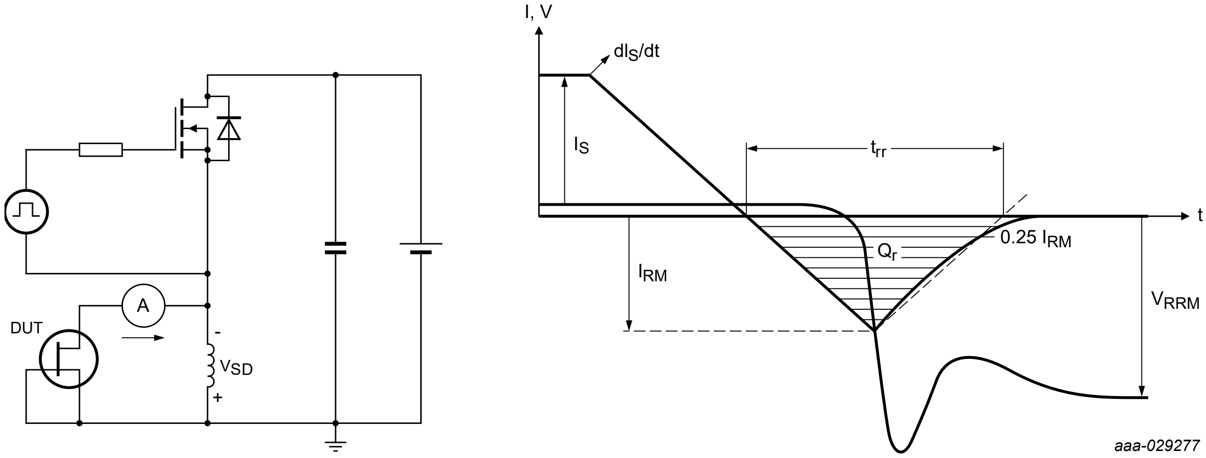


Fig. 20. Diode reverse recovery test circuit and waveform

11. Application information

A Ferrite bead must be fitted in series with the gate of the GaN FET and should be located as close as possible to the gate pin, (see figure below). Keeping the gate-source loop as compact as possible minimizes the gate loop inductance. The Ferrite bead damps the resonant circuit made up of the gate source loop inductance and the GaN FET input capacitance, thus providing fast switching stability. It is recommended that the impedance of the ferrite bead should be 30 Ω @ 100 MHz, (recommended p/n BLM18PG300SN1D). A series resistance (R_G) of 10 - 15 Ω is also recommended.

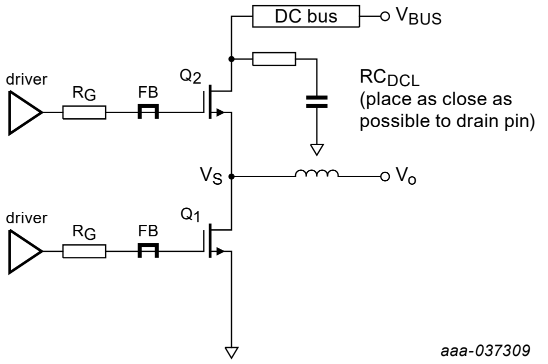


Fig. 21. Ferrite bead and RC resonance damper

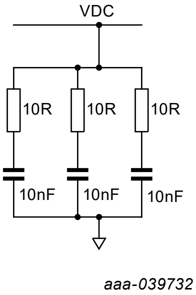
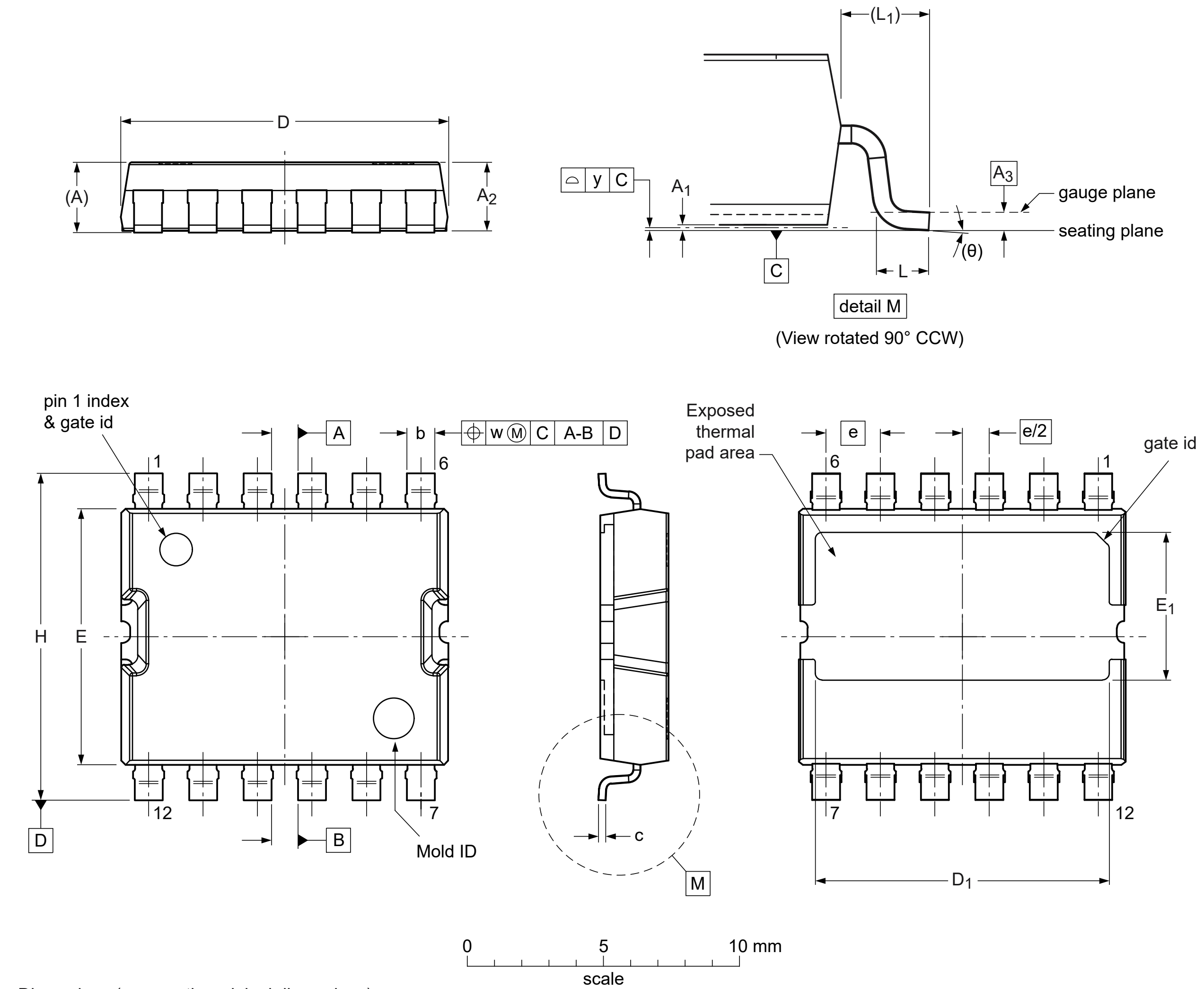


Fig. 22. Parallel RC combination

A DC-link resonance damper is recommended in all cases. Optimal is 30 nF in series with 3.3 Ω, most easily achieved with parallel combination 10 nF and 10 Ω. This resonance damper lowers the Q factor of any resonance in the bus. That resonance will act as a load on the high gain amplifier that is the GaN FET and can lead to instability.

12. Package outline

Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 9.4 mm x 2.5 mm body **SOT8000**



Dimensions (mm are the original dimensions)

Unit		$A_{(ref)}$	A_1	A_2	A_3	b	c	$D^{(1)}$	D_1	$E^{(2)}$	E_1	e	H	L	$L_{1(ref)}$	w	y	$\theta_{(ref)}$
mm	max		0.13	2.65		1.12	0.30	12.15	10.95	9.55	5.55		12.15	1				
	nom	2.75			0.25							2.0			1.3	0.20	0.1	4°
	min		0	2.4		0.93	0.22	11.85	10.65	9.25	5.25		11.85	0.6				

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included for dimension D.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included for dimension E.

sot8000_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8000						~~23-11-30~~ 24-04-17

Fig. 23. Package outline CCPAK1212 (SOT8000)

13. Soldering

Footprint information for reflow soldering of CCPAK1212 package **SOT8000**

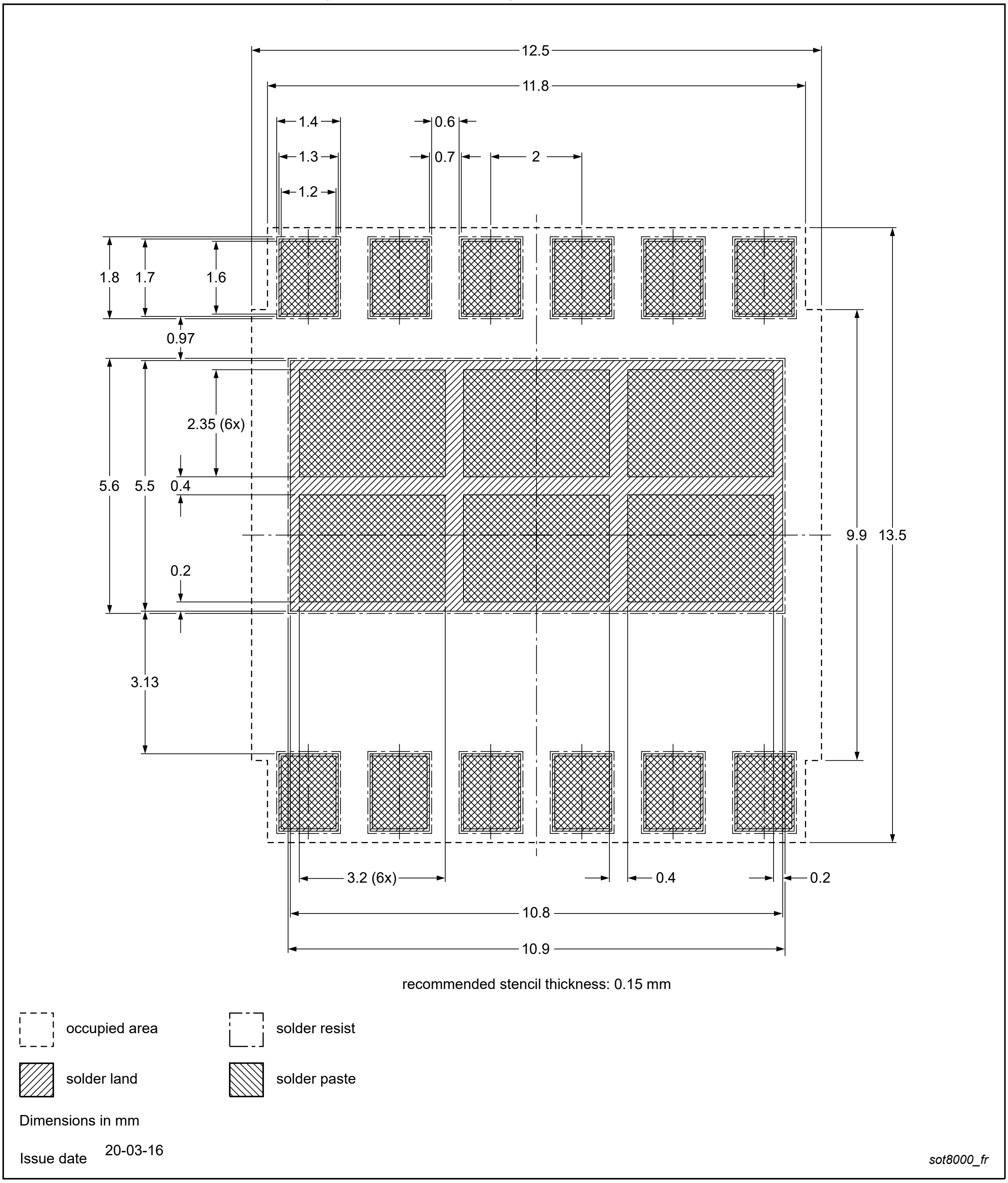


Fig. 24. Reflow soldering footprint for CCPAK1212 (SOT8000)

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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