Dual Motor Control with the dsPIC33CK White Paper

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INTRODUCTION

Microchip Technology has recently released the high-performance dsPIC33C family of DSCs, featuring a dsPIC33 "C" core with a Digital Signal Processing (DSP) engine, along with expanded, context selected registers to reduce interrupt latency, new instructions to accelerate DSP performance, tightly coupled peripherals and faster execution to enable complex, high-speed control loop implementation. Offering 100 MIPS performance, the dsPIC33C family of DSCs provides an upgrade path for users of dsPIC33E and dsPIC33F DSCs to develop more sophisticated applications, such as dual motor control, or motor control and Power Factor Correction (PFC) combined.

This White Paper explains the implementation of sensorless, Field-Oriented Control (FOC) of two (dual) Permanent Magnet Synchronous Motors (PMSM) using a single dsPIC33CK device family DSC. Many cost-sensitive applications, such as Heating, Ventilating and Air Conditioning (HVAC) systems, use Variable Speed Drives (VSDs) in order to run more than one motor to manage both compressors and fans. Most designs require separate controllers for each motor, but with the help of Microchip Technology's dsPIC33CK family of DSCs, sensorless FOC algorithms can be efficiently executed for both PMSM motors. This document focuses on the implementation of dual motor control and hence, does not describe sensorless motor control or motor control theory in detail. Please refer to the documents mentioned in the references for more details.

FEATURES OF THE dsPIC33CK DSC DEVICE

Microchip's dsPIC33CK family of Digital Signal Controllers (DSCs) features a single 100 MIPS, 16-bit dsPIC® DSC core with integrated DSP and enhanced on-chip peripherals. These DSCs enable the design of high-performance, precision motor control systems that are more energy efficient, quieter in operation and provide extended motor life. They can be used to control BLDC, PMSM, ACIM, SR and stepper motors. The dsPIC33CK DSC devices are available in different pin counts, from 28-pin to 80-pin.

For dual motor control, the following are the requirements:

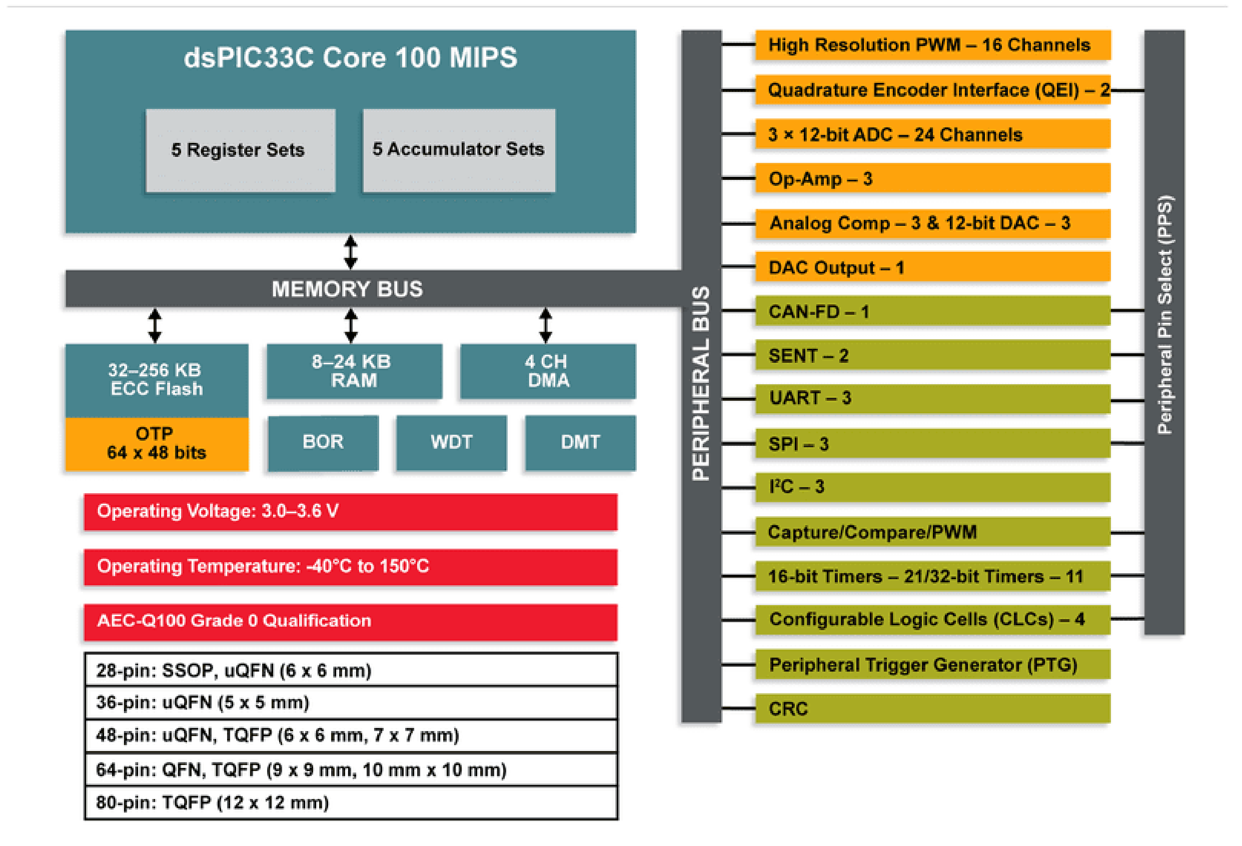
1. A minimum of 48 pins are required.
2. Six PWM generators (12 complementary outputs).
3. Three ADC cores.

The dsPIC33CK DSC block diagram is shown in Figure 1.

The key features of the dsPIC33CK DSC are:

- 3.0V to 3.6V, -40ºC to +150ºC, DC to 100 MIPS Operation
- Eight Independent PWM Pairs (16 total outputs) with Up to 250 ps Resolution
- Flexible PWM Module Trigger Configuration for ADC Triggering
- Fault and Current Limit Inputs
- Three 12-Bit, 3.5 Msps ADC Modules, Each with Two Dedicated SARs and One Shared SAR Core (Three S&Hs)
- Up to Three Op Amps with Internal Connection to the ADC Module
- Two Quadrature Encoder Interface (QEI) Modules for Optical Encoder Support
- Ten 16-Bit Timer/Counters (up to four 32-bit)
- On-Chip, 8 MHz Fast RC (FRC) and 32 kHz Low-Power RC (LPRC) Oscillators
- Three UARTs (15 Mbps) with Automated Protocol Handling for LIN/J2602, DMX and IrDA®
- Three Four-Wire SPI/I^{2}S, Up to 50 MHz with Dedicated Pins
- CAN Flexible Data-Rate (CAN FD) Module (dsPIC33CKXXXMP50X devices only)
- Code-Efficient (C and Assembly) CPU Architecture Designed for Real-Time Applications
- Different Functional Safety Hardware Features, such as Multiple Redundant Clock Sources, I/O Port Read-Back, Analog Peripheral Redundancies, Windowed Watchdog Timer, Deadman Timer, RAM BIST, Hardware Traps and ECC Flash

FIGURE 1: dsPIC33CK BLOCK DIAGRAM



28-pin: SSOP, uQFN (6 x 6 mm)
36-pin: uQFN (5 x 5 mm)
48-pin: uQFN, TQFP (6 x 6 mm, 7 x 7 mm)
64-pin: QFN, TQFP (9 x 9 mm, 10 mm x 10 mm)
80-pin: TQFP (12 x 12 mm)

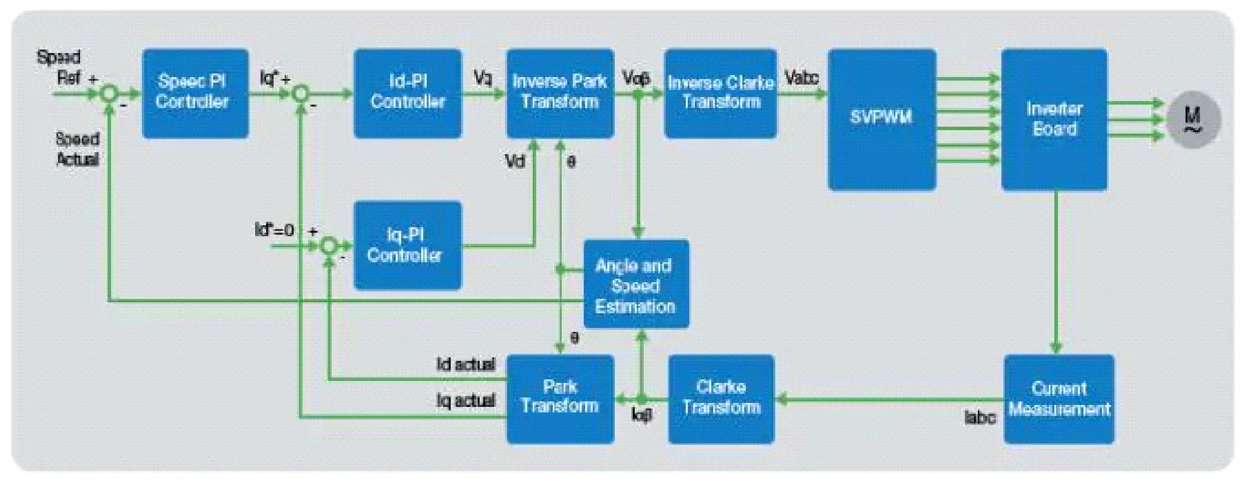
DUAL MOTOR CONTROL

In dual motor control, a single DSC core controls two motors independently. In this mode, a FOC algorithm for both motors can be executed simultaneously.

Sensorless Field-Oriented Control

The sensorless FOC implementation of a PMSM motor is shown in Figure 2 below.

FIGURE 2: FOC IMPLEMENTATION



The objective of a sensorless FOC algorithm is to control both the torque and flux components of current independently, without using a rotor position or speed sensor.

Let's look at the different components of Field-Oriented Control:

- We start from the right side of this block diagram by measuring the currents of two phases (Ia and Ib).
- By using the Clarke transformation, these two currents are then transformed from a 3-phase to a 2-phase stationary frame, called Ialpha and Ibeta.
- By using the Park transformation, currents are transformed from a stationary reference frame (Ialpha and Ibeta) to a rotating reference frame (Id and Iq). The rotor flux angle is needed for this transformation, which comes from the “Angle and Speed Estimation”. A speed or position sensor is not required for sensorless FOC.
- The resulting transformed currents are responsible for the magnetizing flux generation, Id and the torque generation, Iq.
- Ialpha, Ibeta, Valpha and Vbeta are used to estimate the position and speed of the motor.
- The speed error between the reference speed and the estimated speed is fed to a PI controller. The output of the PI controller is reference, Iq, which is responsible for torque generation.
- Since field weakening is not implemented in this example, the reference flux current component Id is kept at zero.
- Torque and flux are also compensated by current PI controllers.
- D and Q voltages (the output of the current PI controllers), which are computed in the rotating reference frame, are transformed back to the stationary reference frame using the Inverse Park Transform block producing Valpha and Vbeta.
- Valpha and Vbeta (the output of the Inverse Park Transform block) are transformed from a stationary reference frame back to three phase voltages, Vabc by the inverse Clarke transform block.
- From the three phase voltages, Vabc, a modulation technique called Space Vector Modulation is used to calculate the PWM duty cycles that drive the power inverter and motor.

System Overview

In this section, different peripherals required for dual motor control are discussed. As shown in Figure 3, each motor is controlled by its own inverter. There is no need to apply the same DC bus voltage to both inverters. For each inverter, three PWM generators (pairs) are required to give gate pulses to the MOSFETs, so for dual motor control, a total of six PWM generators (pairs) are required. The phase currents are sensed through low-side shunt resistors and high-speed op amps. The dsPIC33CK has three internal op amps and the output of each op amp is directly connected to an analog channel. For each inverter, a minimum of two phase currents needs to be measured to run the FOC algorithm, and the DC bus current needs to be measured for overcurrent protection. All three op amps on the dsPIC33CK are used to control the first motor, sensing two of its motor phase currents and checking for its bus overcurrent. For the second motor, three op amps located on the development board are used for the same purposes and their outputs are input directly in the dsPIC33CK's ADC. DC bus voltage is measured for overvoltage protection and to compensate for DC bus voltage variation. Four ADC channels are required to control a single motor, so a total of eight ADC channels are required for controlling two motors. UART communication is used to communicate with a host PC.

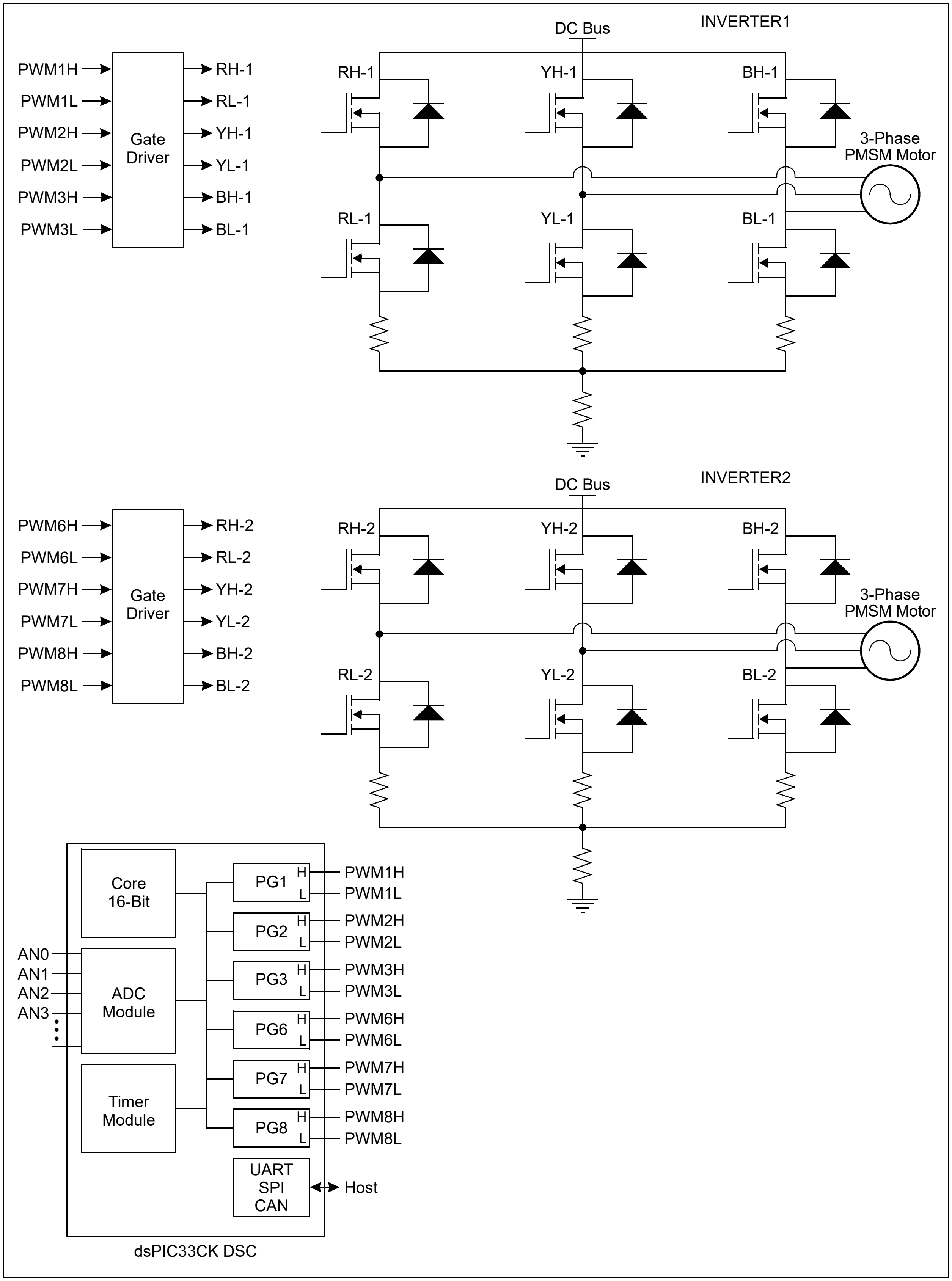
A separate timer is used for the user interface, task scheduling and implementation of periodic tasks.

As shown in Table 1, the following PWM generators are used for MC1 and MC2.

TABLE 1: PWM GENERATORS

Motor	PWM Generator
Inverter1 (MC1)	PWM1H/L, PWM2H/L, PWM3H/L
Inverter2 (MC2)	PWM6H/L, PWM7H/L, PWM8H/L

FIGURE 3: HARDWARE BLOCK DIAGRAM



Implementation Challenges

TIMING AND THE INTERRUPT SERVICE ROUTINE (ISR)

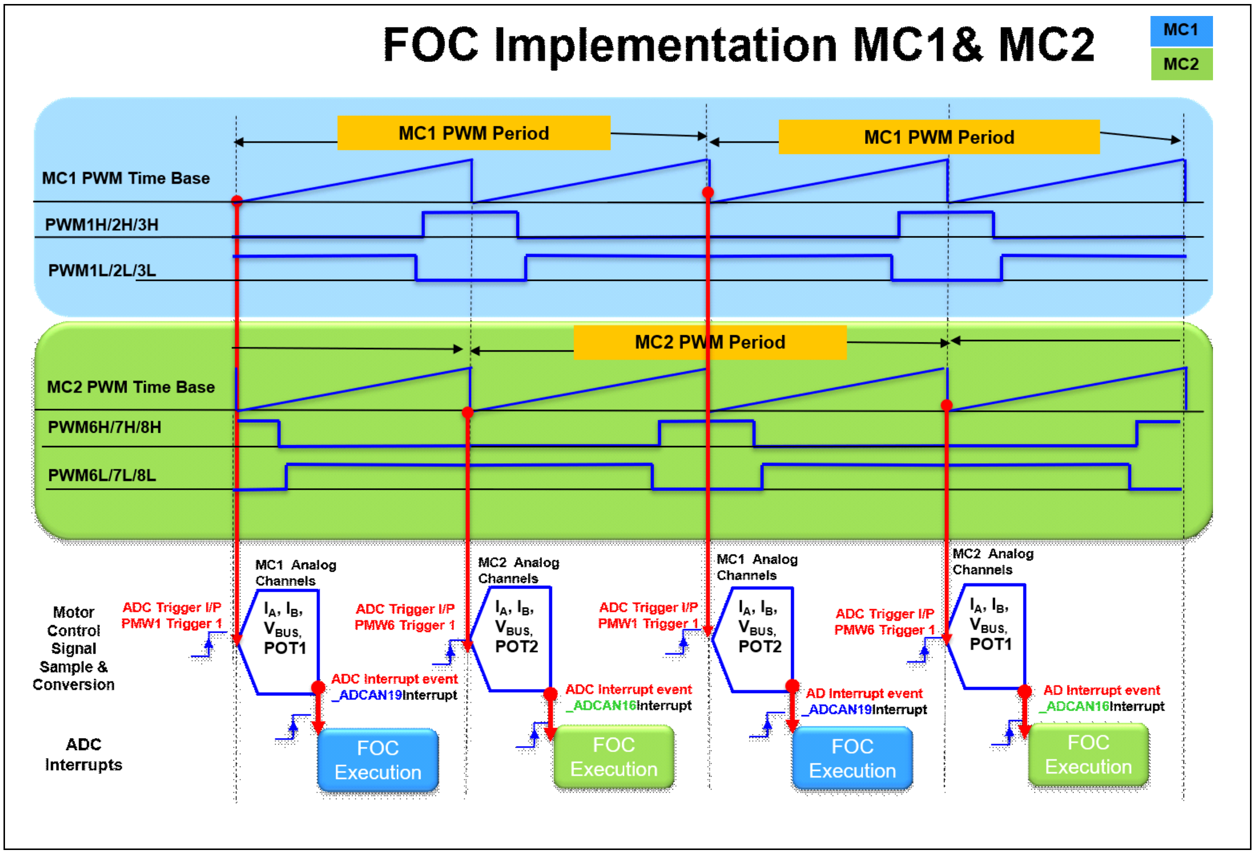
The timing of firmware execution and ADC conversion is important in motor control applications. Phase currents should be sampled at the midpoint of their zero vector as this gives an ADC reading free of any switching harmonic current. If a shunt resistor is connected in series with the lower leg, then the zero vector in this state is defined as ‘`000`’, where all the bottom side switches are turned on.

To effectively utilize the processor speed, the PWM signals to both inverters (MC1 and MC2) are phase shifted by half of the PWM period. This phase shifting distributes the execution time of the FOC algorithm for both motors in order to eliminate any overlap. Additionally, the phase shifting also reduces current ripple on the DC bus. This serializing of the FOC algorithm computation for each motor optimizes the processor processing time.

The PWMs are configured to operate in Center-Aligned PWM mode to generate complementary waveforms and to correctly trigger the ADC. Each PWM generator has the capability to trigger multiple ADCs. Each PWM generator can generate two ADC triggers: ADC Trigger 1 and ADC Trigger 2. PWM1 Trigger 1 is used to trigger analog channels corresponding to Inverter1 (MC1) and PWM6 Trigger 1 is used to trigger analog channels corresponding to Inverter2 (MC2).

In the dsPIC33CK devices, the ADC module can generate individual interrupts from a variety of sources and for each analog channel. Once the ADC conversion is completed for Inverter1, an ADC interrupt is generated and the FOC algorithm is executed in the ISR. Similarly, once the ADC conversion is completed for Inverter2, another ADC interrupt is generated and the FOC algorithm is executed in another ISR. Figure 4 depicts the phase shifting of the PWMs and generation of interrupt events for both MC1 and MC2.

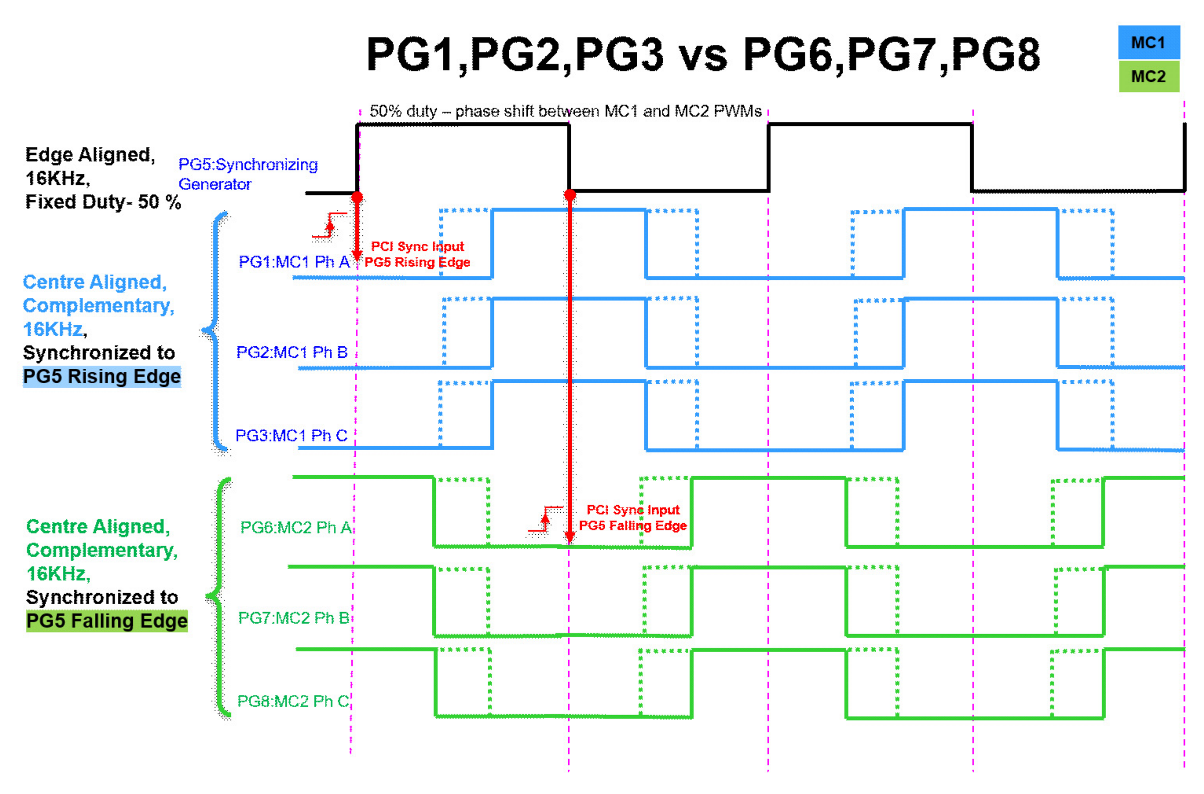
FIGURE 4: TIMING DIAGRAM



PWM SYNCHRONIZATION

The PWM generator for Inverter1 generates PWM outputs with synchronized periods (synchronized operation). Similarly, the PWM generators for Inverter2 generate PWM outputs with synchronized periods. Each PWM generator must receive a Start-of-Cycle (SOC) trigger to begin a PWM cycle. PWM generators are grouped into groups of four: PG1-PG4 and PG5-PG8. Any generator within a group of four may be used to trigger another generator within the same group. The PWM1 generator acts as a 'master' by providing the trigger for the PWM2 and PWM3 generators (for MC1). The PWM6 generator acts as a 'master' by providing the trigger for the PWM7 and PWM8 generators (for MC2). The PWM5 generator is used to create the phase shift [50% duty] between the MC1 and MC2 PWM generators. This is achieved by using PCI Sync logic. Figure 5 depicts the generation of the PWMs for MC1 and MC2, and how PWM5 is used to phase shift the PWMs for both inverters.

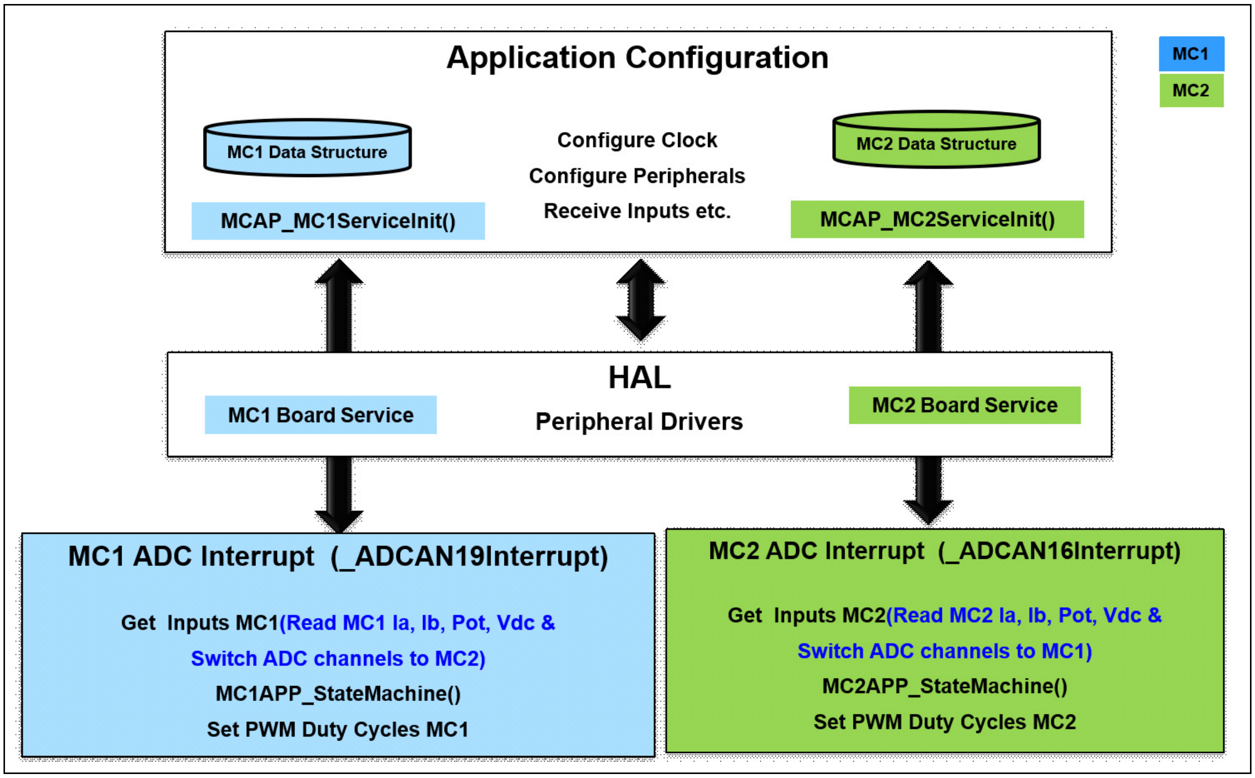
FIGURE 5: PWM SYNCHRONIZATION/PHASE SHIFT



Firmware Implementation

The firmware implementation is shown in Figure 6 below.

FIGURE 6: DUAL MOTOR CONTROL FIRMWARE OVERVIEW



APPLICATIONS

While there are multiple use cases for dual motor control, this section covers two applications as examples of implementing dual motor control with a single-core dsPIC33CK DSC.

Air Conditioners

Air conditioners are high energy consuming loads and hence, energy saving is a priority for most air conditioner manufacturers. High energy efficiency is achieved by using an inverter-based Variable Speed Drive (VSD) for both the PMSM-based compressor and condenser fan. The VSD and the sensorless Field-Oriented Control (FOC) of brushless motors allow an appliance to operate at an optimal speed (power) setting and hence, achieve higher energy savings as compared to traditional fixed speed, single-phase AC Induction Motor (ACIM) based compressors and condenser fans.

In the case of an air conditioner, the following choice of PWM generators and ADC inputs can be made for both motors using an 80-pin dsPIC33CK256MP508 DSC device.

TABLE 2: AIR CONDITIONERS – COMPRESSORS

Compressor		
Signal	**dsPIC® DSC Pin**	**Functionality**
PWMRH	1	PWM1H
PWMRL	3	PWM1L
PWMYH	78	PWM2H
PWMYL	80	PWM2L
PWMBH	73	PWM4H
PWMBL	74	PWM4L
IPHASEA_MA	16	OA1OUT
IPHASEB_MA	41	OA2OUT
IBUS_MA	23	OA3OUT
VBUS	15	AN12

TABLE 3: AIR CONDITIONERS – FANS

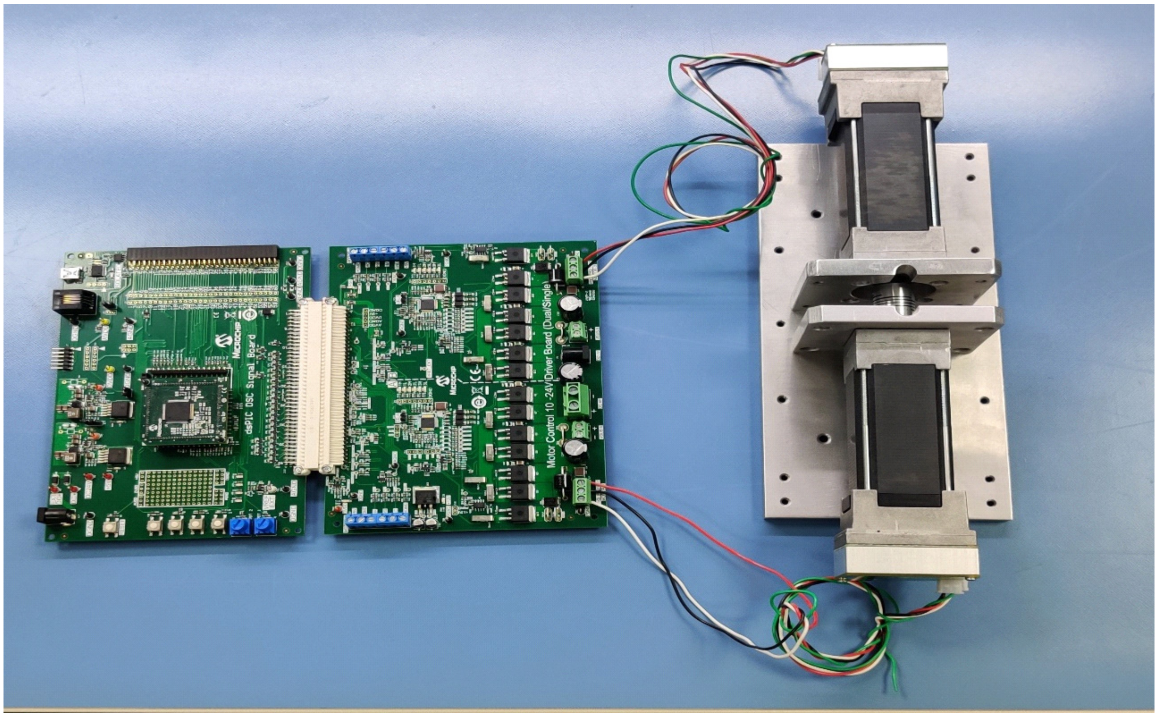
Fan		
Signal	**dsPIC® DSC Pin**	**Functionality**
PWMRH	7	PWM6H
PWMRL	8	PWM6L
PWMYH	66	PWM7H
PWMYL	67	PWM7L
PWMBH	5	PWM8H
PWMBL	6	PWM8L
IPHASEA_MB	58	AN2
IPHASEB_MB	60	AN10
IBUS_MB	38	AN18
VBUS	61	AN11
V_A	33	AN15
V_B	40	AN16
V_C	30	AN17

Active Loads

The second application covered as an example of dual motor control is called an “active load”. When a motor is tested with a load, the primary reason for testing is to verify that the motor produces torque corresponding to the nameplate parameters, such as horsepower/kilowatt, speed, voltage and current. The most common method of load testing is with a dynamometer. While a dynamometer offers many advantages and flexibility, the disadvantage of a dynamometer is that it is a very costly piece of equipment and the cost further increases with an increase in the power level. Another disadvantage is that power is dissipated in a dynamometer as heat. Both of these disadvantages can be overcome by using an active load mechanism.

In this configuration, two motors are coupled together. A primary motor runs in Motoring mode and a secondary motor runs in Regenerative Braking mode (as a load to the primary motor). The same DC bus voltage should be connected to both inverters, such that the power regenerated by the secondary motor is fed back to the primary motor and the only losses are consumed from the input DC source. In this configuration, the primary motor runs in a Speed Control mode and the secondary motor runs in a Torque Control mode, with a negative “iq” torque reference. By changing the amplitude of the negative “iq” current reference, the load on the primary motor can be varied.

FIGURE 7: ACTIVE LOAD SETUP RUNNING ON THE dsPIC33CK INTERNAL OP AMP MOTOR CONTROL PIM (MA330041-2) AND THE MICROCHIP LOW-VOLTAGE MOTOR CONTROL BUNDLE (DV330100)



Test results are shown in Figure 8 and Figure 9 when a motor setup is run in an active load setup. The same input DC source is used for both inverters, MC1 (motor) and MC2 (brake). As shown in Figure 8, MC1 consumes less current when MC2 is free-running (not operating as a brake). For the same speed, MC1 consumes more current when MC2 is operating in Regenerative Braking mode, as shown in Figure 9. To operate MC2 in Regenerative Braking mode, a negative iq torque current reference is given. The power regenerated by MC2 is given back to MC1, hence the only losses are consumed from the DC input power source.

Please note that the fixture for coupling both motors together (as shown on Figure 7) is not a standard setup provided by Microchip.

FIGURE 8: WAVEFORM WHEN MC2 IS NOT OPERATION

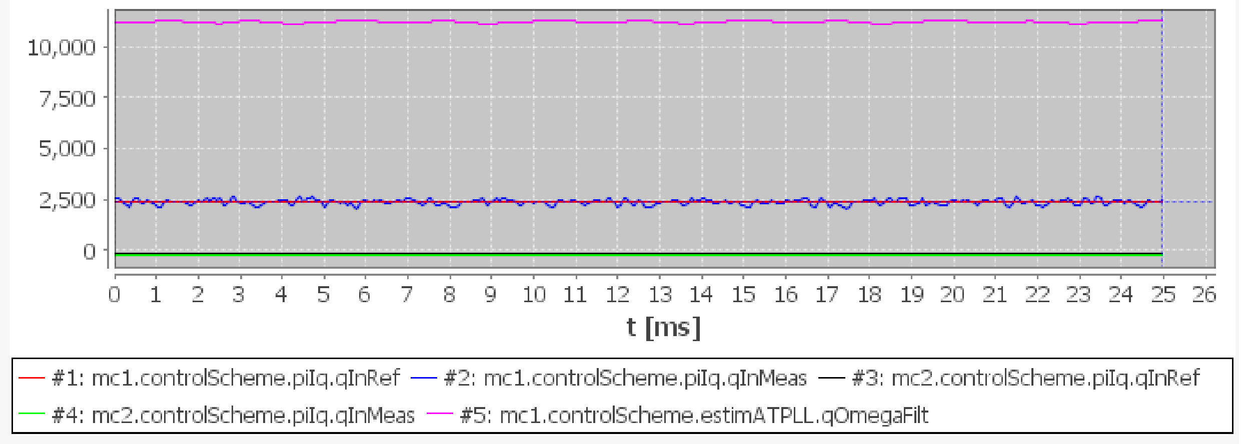
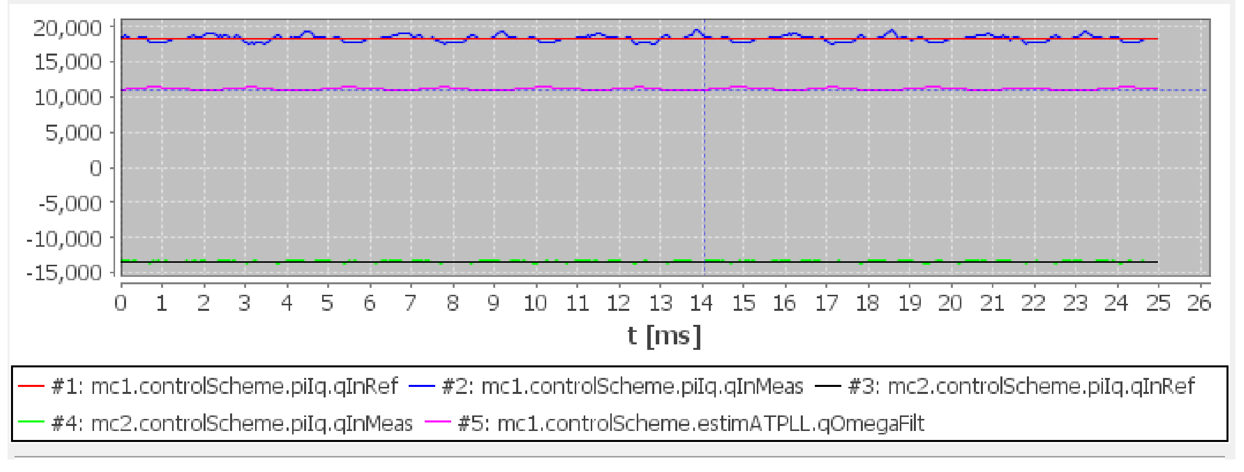


FIGURE 9: WAVEFORM WHEN MC2 IS RUNNING IN REGENERATION MODE



DEVELOPMENT TOOLS

The Low-Voltage Motor Control Development Bundle (DV330100) provided by Microchip is for evaluating and developing a dual motor control power stage targeted to drive two Brushless DC (BLDC) motors or Permanent Magnet Synchronous Motors (PMSM) concurrently. The Bundle comes with a dsPIC DSC Signal Board, which includes a dsPIC DSC Plug-In Module (PIM) and a Motor Control 10-24V Driver Board.

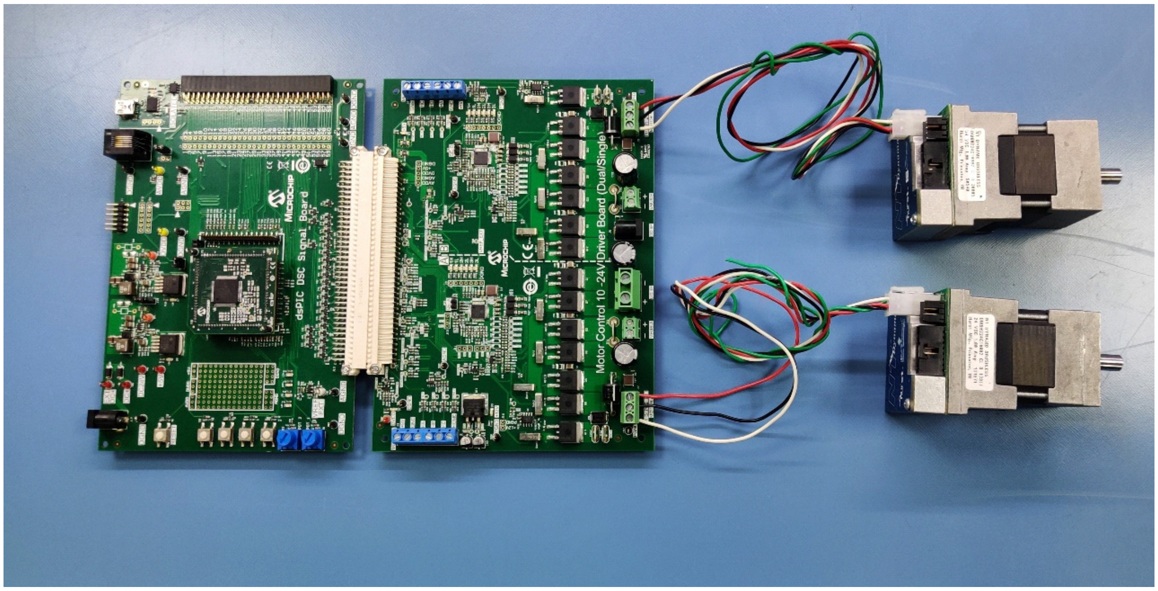
The dsPIC DSC Signal Board supports both 3.3V and 5V operated dsPIC DSC devices for various applications, several human interface features and communication ports. The dsPIC Signal Board has two major connectors, a 120-pin connector for mating with the Driver Board and a 100-pin connector for the PIM.

The Motor Control 10V-24V Driver Board, along with the compatible dsPIC DSC Signal Board, provides a software development platform to build and evaluate embedded motor control application software using Microchip's high-performance motor control Digital Signal Controllers (DSCs) and Microcontrollers (MCUs).

The dsPIC33CK256MP508 Internal Op Amp Motor Control PIM (MA330041-2), ordered separately, supports dual motor control and is compatible with the Low-Voltage Motor Control Development Bundle (DV330100).

The application firmware is developed for running two Hurst 0.75 motors (AC300020), ordered separately, using a dsPIC33CK256MP508 Internal Op Amp Motor Control PIM (MA330041-2) and the Low-Voltage Motor Control Bundle.

FIGURE 10: DUAL MOTOR CONTROL WITH THE LOW-VOLTAGE MOTOR CONTROL BUNDLE (DV330100) AND DUAL HURST MOTORS



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