ACPL-W346

Wolfspeed (CREE) SiC MOSFET C2M0080120D

Evaluation Kit

Introduction

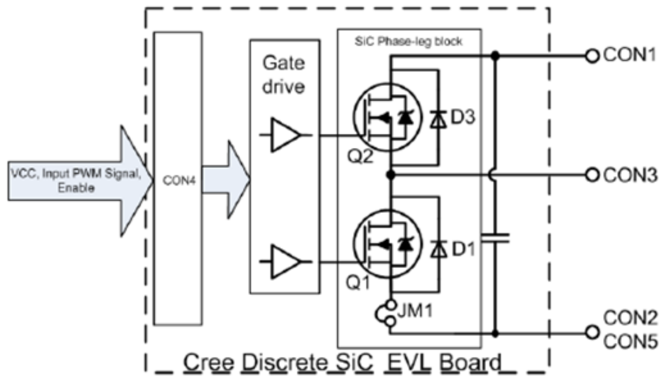
SiC devices including SiC MOSFET and SiC Schottky diodes are recognized as next generation wide bandgap devices. They can provide fast switching with less loss compared to conventional Si devices and improve overall system efficiency. The higher switching capability and frequency can reduce the overall system size and costs. The technical benefits coupled with lower costs have increased the fast adoption of SiC power semiconductors in applications like industrial motor control, induction heating and industrial power supplies and renewable energy.

Broadcom gate drive optocouplers are used extensively with Silicon-based semiconductors IGBT and Power MOSFETs can also be used for SiC operations. Optocouplers are used to provide reinforced galvanic insulation between the control circuits from the high voltages and the power semiconductors. The ability to reject high common mode noise (CMR) will prevent erroneous driving of the SiC power semiconductors during high frequency switching.

Figure 1 KIT8020CRD8FF1217P-1 SiC MOSFET Evaluation Kit

This evaluation kit, KIT8020CRD8FF1217P-1 is meant to demonstrate the high performance of Wolfspeed (CREE) 1200V SiC MOSFET (C2M0080120D) and SiC Schottky diodes (C4D20120D) in the standard TO-247 package. The kit also includes Broadcom gate drive optocouplers ACPL-W346, power supplies and all the other components needed to quickly assemble the half bridge power stage. The basic block diagram and specifications are shown in Figure 2. The assembly can be easily configured for several topologies from the basic phase-leg configuration to several other common topologies. Additional topologies like H-bridge and 3-phase inverter are possible with two or more of the evaluation kits.

Figure 2 KIT8020CRD8FF1217P-1 Basic Block Diagram



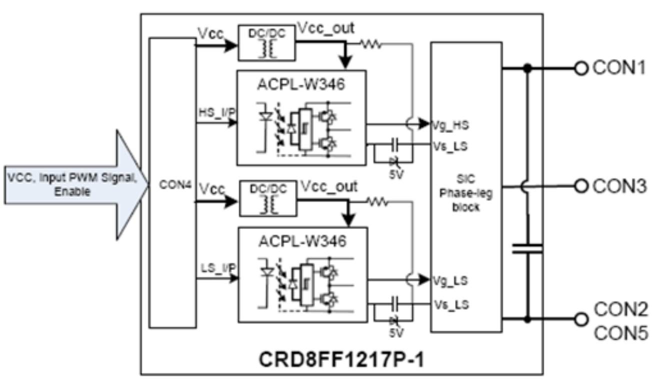
This reference design will describe the basic operation of using gate drive optcoupler ACPL-W346 for the SiC MOSFET evaluation kit. Purchase of the evaluation kit and the user's manual are available from catalogue distributors:

http://www.digikey.sg/product-detail/en/KIT8020-CRD-8FF1217P-1/KIT8020-CRD-8FF1217P-1-ND/5027643

http://www.mouser.sg/ProductDetail/Cree-Inc/KIT8020-CRD-8FF1217P-1/?qs=%2fha2pyFadugoWU85a9ES3mGSyQOWKTBmodw8qlZLPgNqDts0nlnPYD4v%252bh%2fKfVJR

Evaluation Kit Overview

Figure 3 Block Diagram with Gate Drive Optocoupler ACPL-W346

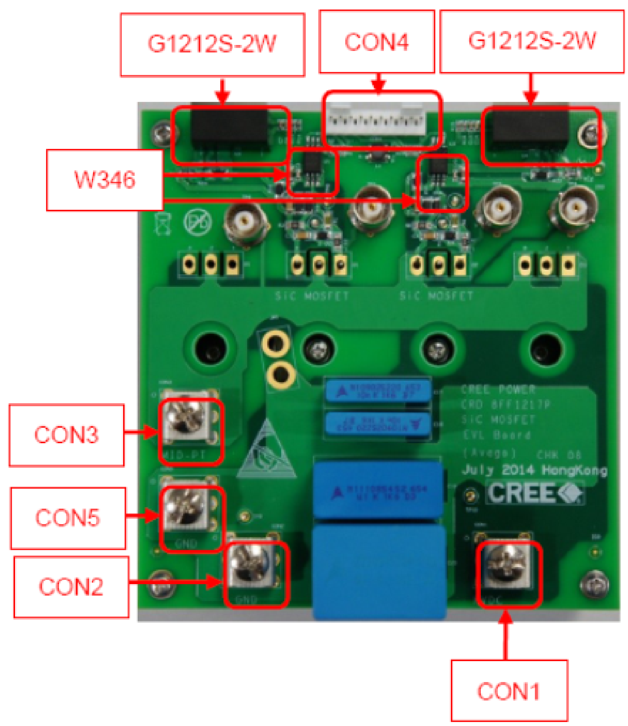


The evaluation kit uses 2 gate drive optocoupler ACPL-W346 to drive the SiC MOSFET directly in the half bridge topology. The ACPL-W346 is a basic gate driver optocoupler used to isolate and drive the SiC MOSFET operating at high DC bus voltage. It has a rail-to-rail output with 2.5A maximum output current to provide fast switching high voltage and high driving current to turn-on and off the SiC MOSFET efficiently and reliably. The unique feature of ACPL-W346, is the speed and is the industry's fastest in its class. The maximum propagation delay is 120ns and typical rise and fall times are around 10ns. The very high CMR, common mode rejection of 50kV/µs is required to isolate high transient noise during the high frequency operation from causing erroneous outputs. It can provide isolation certified by UL1577 for up to VISO 5000VRMS/min and IEC 60747-5-5 for working voltage, VIORM up to 1140VPEAK.

The 2W DC/DC converter with +12V VCC input generates +24V Vcc_out output voltage with 6kVDC isolation that is supplying voltage to ACPL-W346 on push-pull gate drive of the secondary side as shown in Figure 3. In this circuit, a 5V zener in parallel with 1uF capacitor is used to generate -5V Vgs voltage for the SiC MOSFET turn-off and turn-on Vgs voltage is equal to 24V-5V=19V. Note that SiC MOSFET can be turned off with zero voltage, and the -5V turn-off voltage helps with faster turn-off and lower turn-off losses and also improves dv/dt induced self-turn-on and noise immunity during transient periods with more margin for Vgs turn-on threshold voltage.

Hardware Description and Board Design

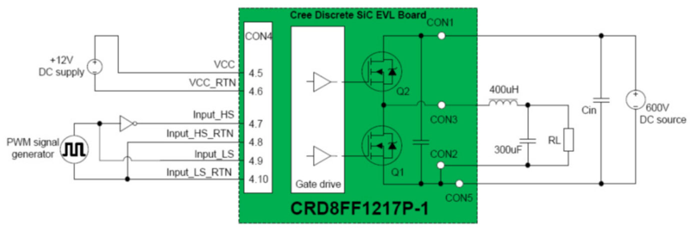
Figure 4 Evaluation Kit Key Connectors and Components



In a synchronous phase-leg Buck converter topology, CON1 connects to the positive DC BUS rail, CON2/5 connects to the negative BUS rail or GND and CON3 the output of the converter. Several topologies can be configured with this board: synchronous Buck, non-synchronous Buck (or high-side Buck), synchronous Boost, non-synchronous Boost, half phase-leg bridge converter, H bridge converter (2x EVL boards) and bi-directional buck-boost converters. Please refer to the user's manual for the details of the different topologies. CON4 is for the PWM signal/logic inputs and supply voltage for ICs.

To make testing more effective and easy, the BNC connectors are added on the board to measure both Vgs and Vds waveforms for SiC MOSFET Q1 and Q2. A current test point with two unpopulated through-hole contacts is available to measure the drain current through the low side switch.

Figure 5 Test Setup of a Synchronous Phase-leg Buck Converter Topology



SiC device is a fast switching device, and it is important to maximize SiC's high performance and minimize ringing with fast switching. The evaluation kit introduces some design approaches to minimize the ringing on the board:

-The gate drive and logic signal are put on top of the PCB board, while the main power trace and switching devices are put on the bottom layer. There is no crossover or overlap between gate signal and switching power trace, which can minimize high dv/dt and di/dt noise influence from the switching node to gate signal.

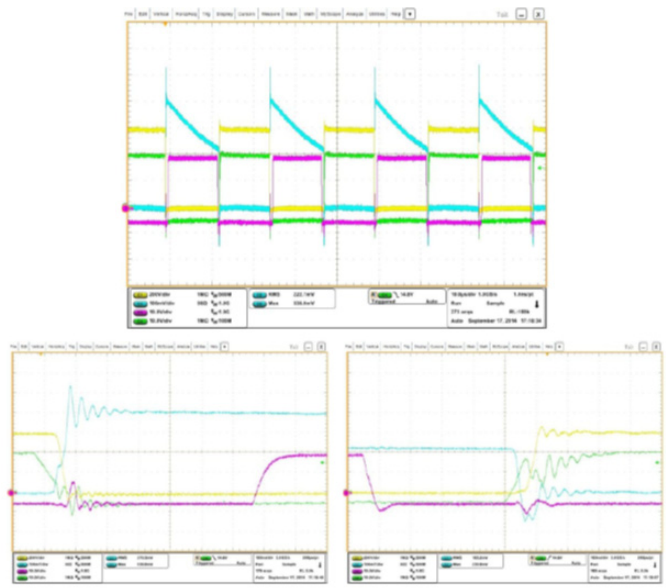
- Four de-coupling film capacitors with value 10nF, 10nF, 0.1uF and 5uFare placed close to the SiC devices, and it can reduce high frequency switching loop and bypass noise within switching loop.
- The layout of gate drive circuitry is designed with symmetric trace distance, which can introduce balance impendence on the gate drive. Also, the gate drive is placed as close as possible to the SiC MOSFETs.
- The power trace layout is optimized to reduce the switching loops.

Test Measurements

The same synchronous phase-leg Buck converter in Figure 5 is used as an example to evaluate the performance of the evaluation kit. The switching waveforms are shown in the Figure 6 and Figure 7. In the operation of the synchronous Buck converter, the low-side body diode conducts before low-side MOSFET is turned on, thus this low-side MOSFET operates in Zero Voltage Switching (ZVS) mode and high-side MOSFET operates in hard-switching mode.

The evaluation kit's maximum efficiency in this configuration is around 98.9% at 4KW half load. It includes losses from the inductor, switching devices, and capacitors. Considering the high switching frequency (40kHz) and high duty cycle (50%), the efficiency is high compared to conventional Si IGBT solutions.

Figure 6 Vgs, Id and Vds Waveforms at 9KW Loading



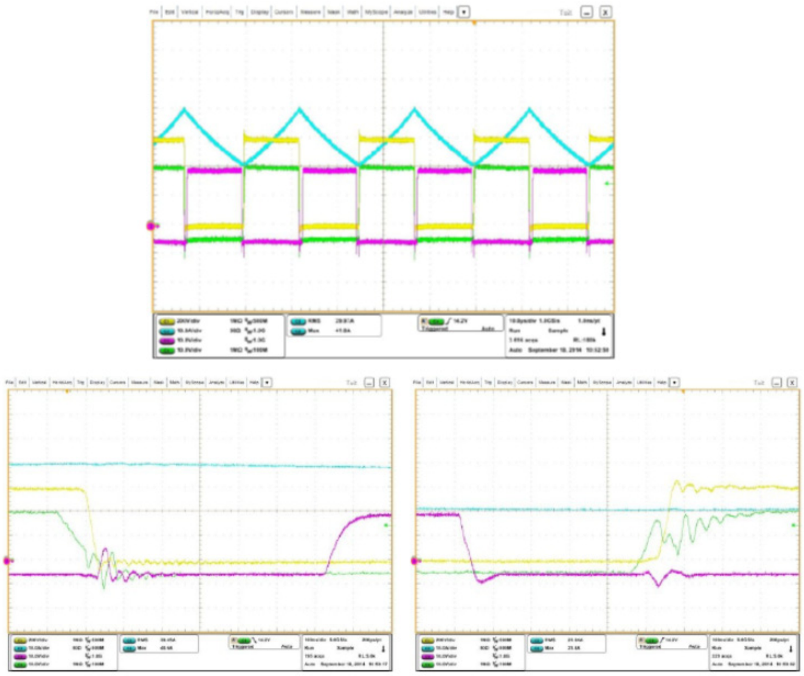
Ch1: low-side Vds yellow 200v/div

Ch2: low-side Id blue 100mv/0.0131ohm/div

Ch3: low-side Vgs pink 10v/div

Ch4: high-side Vgs green 10v/div

Figure 7 Vgs, Inductor Current IL and Vds Waveforms at 9KW Loading



Ch1: low-side Vds yellow 200v/div

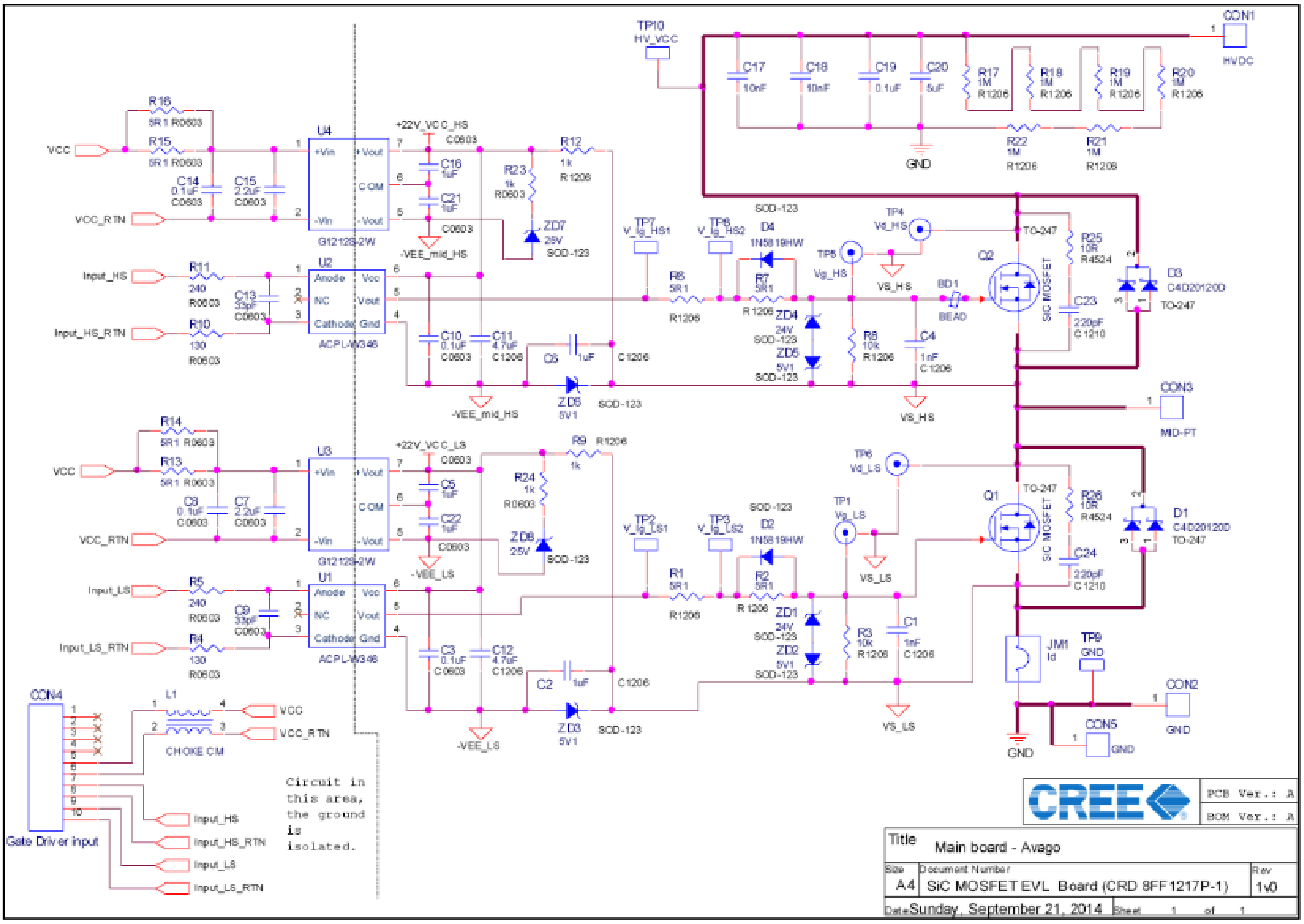
Ch2: inductor current IL 10A/div

Ch3: low-side Vgs pink 10v/div

Ch4: high-side Vgs green 10v/div

Schematic of the Gate Driver Board

Figure 8 Gate Driver Board Schematic



For product information and a complete list of distributors, please go to our web site: www.broadcom.com

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