Solving Complex Computational Challenges for Advanced Motor Power Control Electronics

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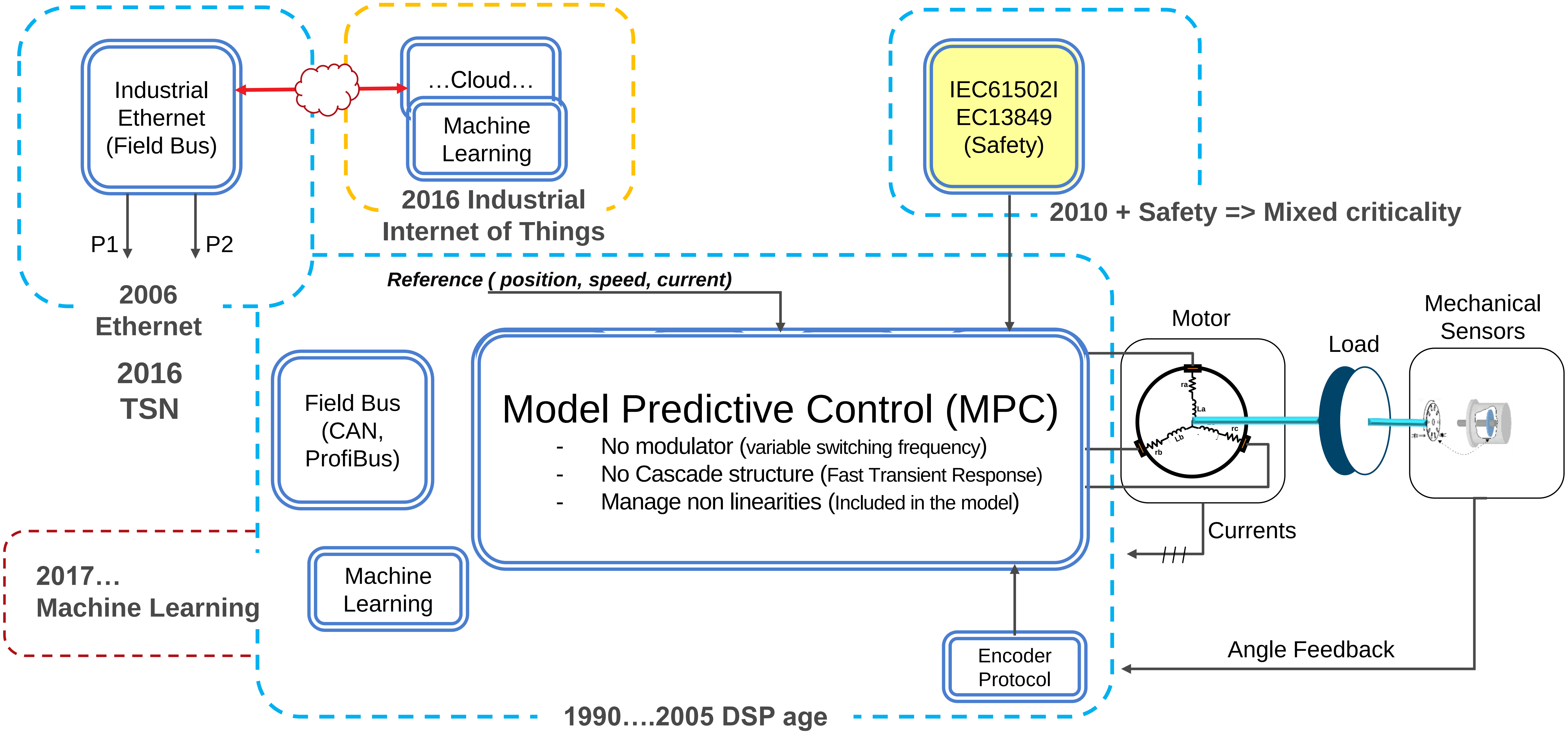
What You Will Learn in this session

- **SiC 3-Level and 2-Level inverter platform with Xilinx ZYNQ**
  - Basis for a versatile power system controller for Silicon Carbide –
  - How to use ZYNQ in modern power system controllers
  - Linux, Python and Jupyter-Notebook, Scilab, Matlab, Hardware in the loop possibilities and solutions
  - ZYNQ7000 TLIMOT inverter features
  - ZYNQ Ultrascale+ extension
- **Make you familiar with Xilinx open source EDDP and SPYN projects**
  - The project and PYNQ framework
- **Safety for drives with ZYNQ Ultrascale+**

Evolution of Typical Electric Drives



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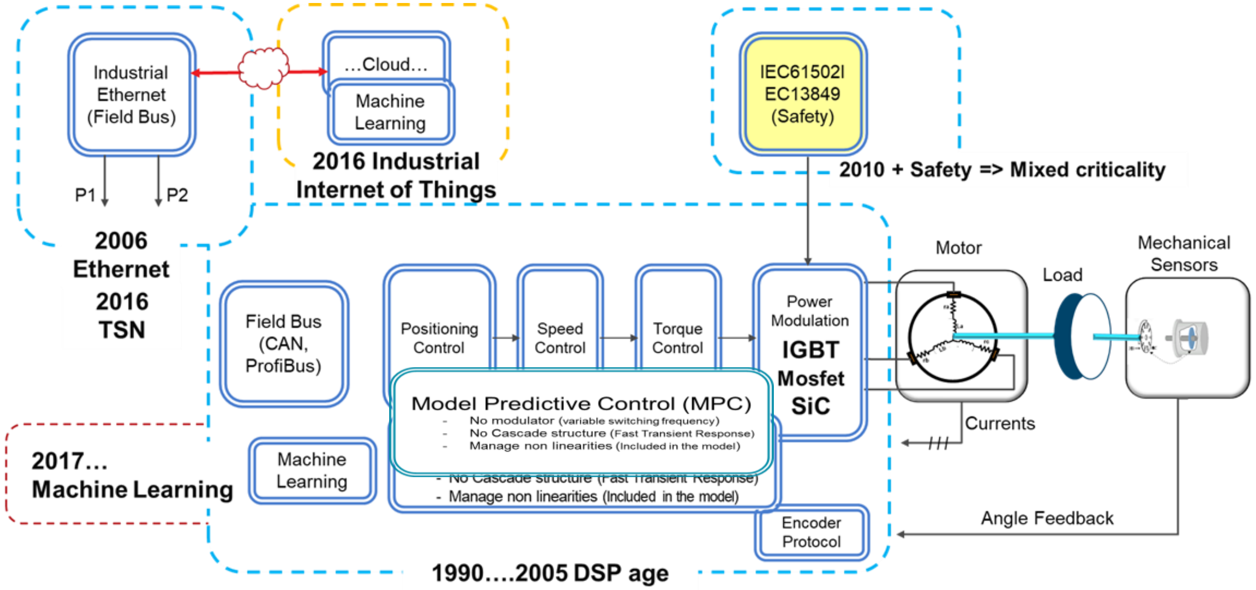
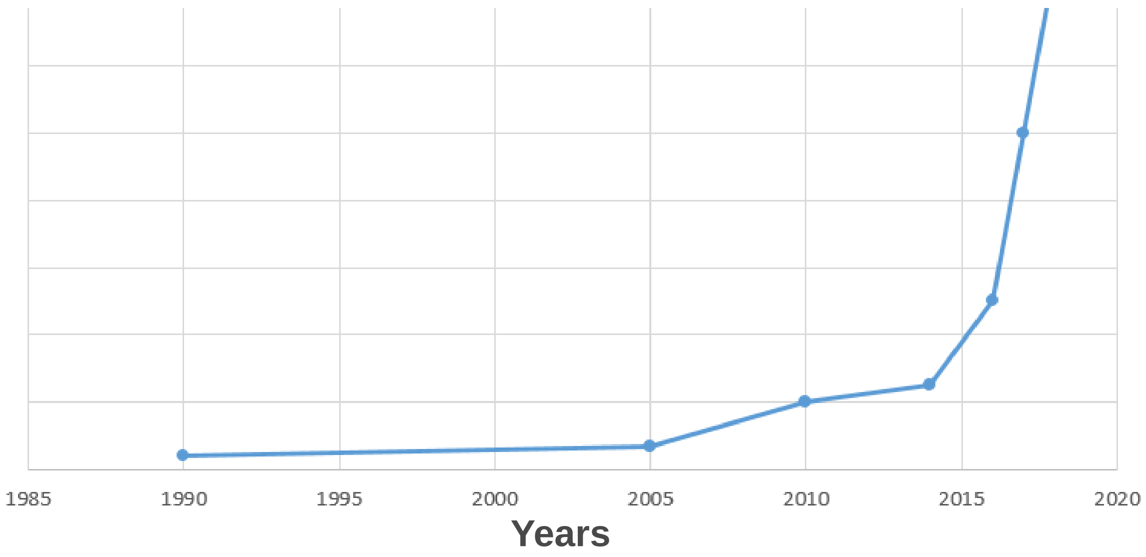
New Technologies - Software Demand on Drives



Speed of hardware technology changes and complexity



Mixed Criticality

Mostly Control | Control + Safety | A.I./ Machine Learning

Assembly 1980…1995 → **C/Assembly 1995…** → **C 2000…** → **RTOS & C++ 2005…** → **MISRA C 2010…** → **Linux / RTOS 2012** → **Python**

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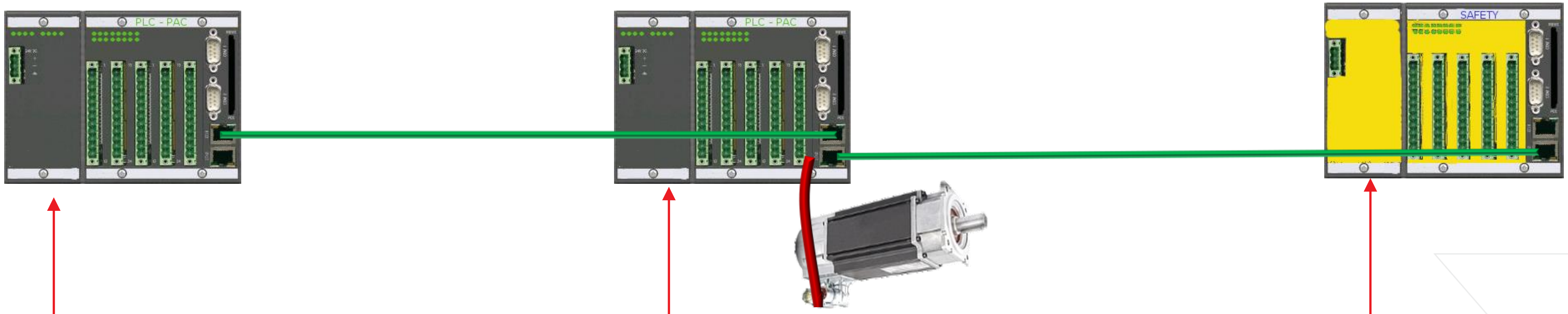
Incumbency of Mixed Criticality

PLC | Drive | Safety Logic



High performance Single Core CPU
Typically "end user application dependent"

Application 1 | Application 2 | HMI

RTOS | OS

Single CPU

Single Core CPU + Single Core DSP
Typically "time critical"

Network I/F | Motion Control | Motor Control

RTOS | Bare Metal

Single CPU | **Single DSP**

Two independent Core CPU
"safety critical"

Safety Application | Safety Application

Bare Metal | Bare Metal

Single CPU | Single CPU

Voter

Integration into Single Hardware Unit

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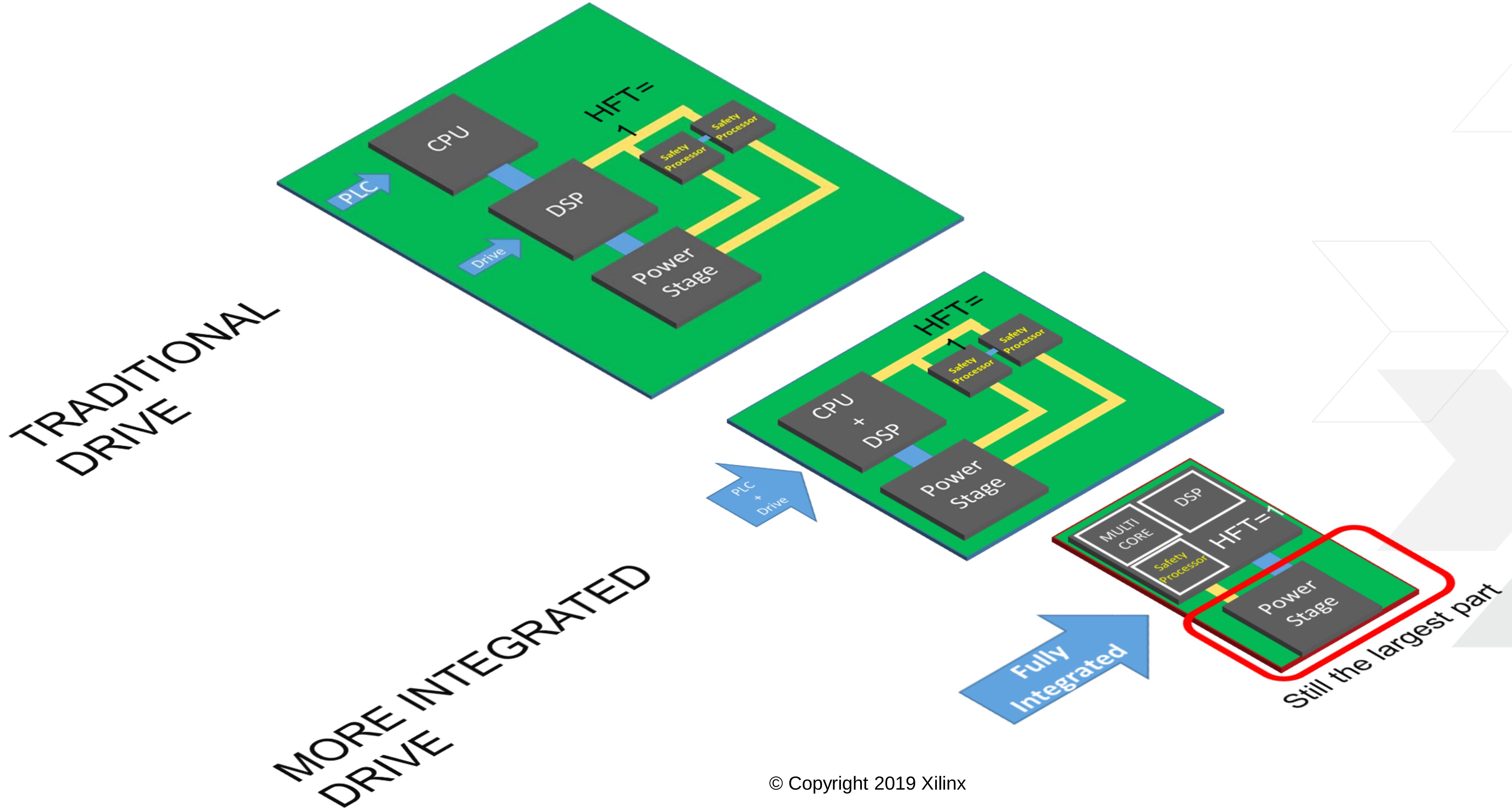
Drive systems integration evolution



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SiC Power Switches

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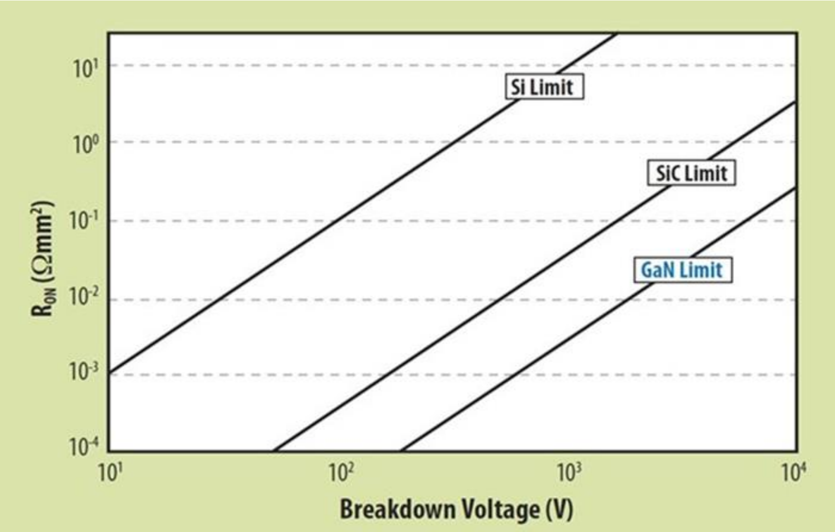
Power switches go Wide Band Gap semiconductor

MATERIAL	Band Gap
Germanium	0.66
Silicon	1.1
Gallium Arsenide	1.4
Silicon Carbide	3.3
Gallium Nitride	3.4



Wide-bandgap semiconductors permit to operate:

- At much higher voltages,
- At higher switching frequencies
- At higher temperatures than silicon and gallium arsenide

SiC Advantages

Technology

> Silicon Carbide (SiC) is a power transistor comprised of silicon (Si) and carbon (C)

> It sustains high voltages, with low series resistance, and low conduction losses

> Its high band gap allows it to switch higher voltages and currents at higher temperatures

Benefits

> Smaller inductors

> Smaller heat sinks

> Higher switching frequency than IGBT

> Smaller capacitors

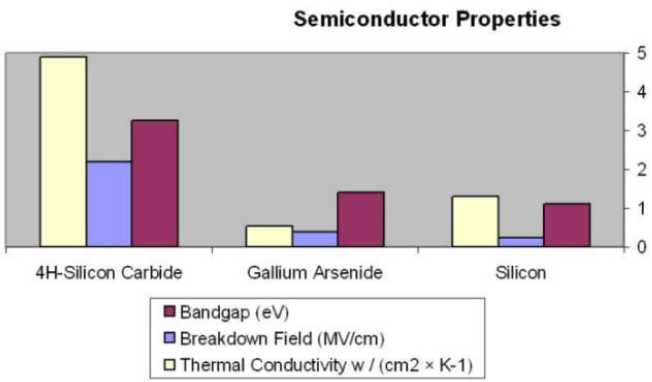
Applications

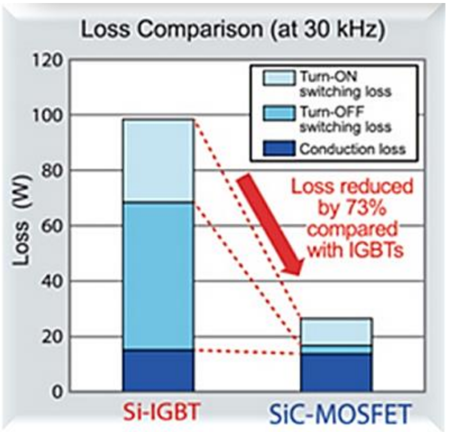
> Solar inverters

> Motor drives

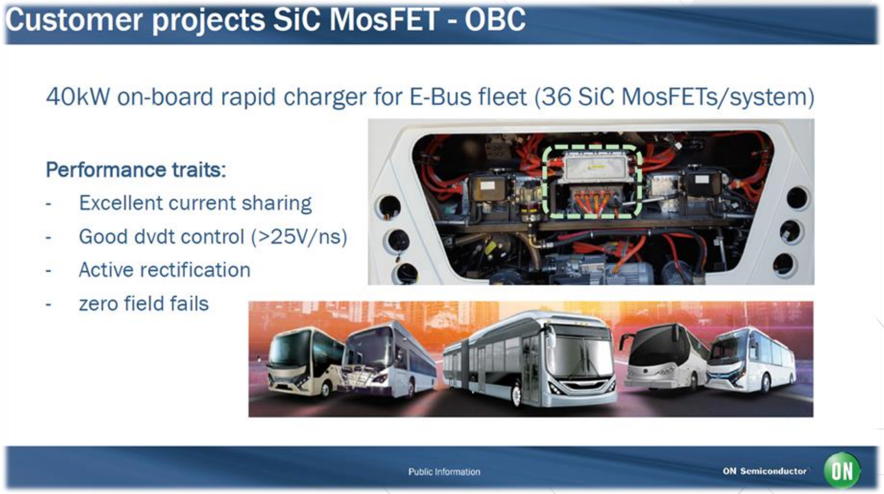
> DC-AC inverters

> Power Factor Correction





Source: Rohm Semiconductor



40KW rapid charger - Source On Semiconductor (2018)

Tesla Model 3 is using Silicon Carbide MOSFETs for its main inverter - Source PntPower.com (2019)

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General Challenges

- **SiC drive challenges**
  - Control of SiC gate rise and fall time
  - Dead time
  - Gate charge
  - dV/dt
- **Precise and fast control strategies for best SiC usage**
  - Fast FOC (Field Orientation Control)
  - Model Predictive Control (MPC)
- **Fast Acquisition and Data Logging for advanced applications**
  - Predictive maintenance
  - Machine Learning based diagnostic and optimization
- **Power Switches Topology**
  - Selection of proper topology to minimize component
  - More switches compared to 2-levels
  - Certain topologies require blocking diodes
    - Additional cost
    - Less reliability
- **Power Modulator Stage**
  - Four switches to be controlled per inverter phase instead of just two
  - More PWM compared to 2-LEVEL
  - For equally split dc-link (dc-link/2) is required an actively controlled neutral point
  - Increased control effort to balance dc_link/2
  - State space vectors 3 times more complex

Xilinx TLIMOT 3-Level and 2-Level Inverter
Experience with SiC Since 2014
System View

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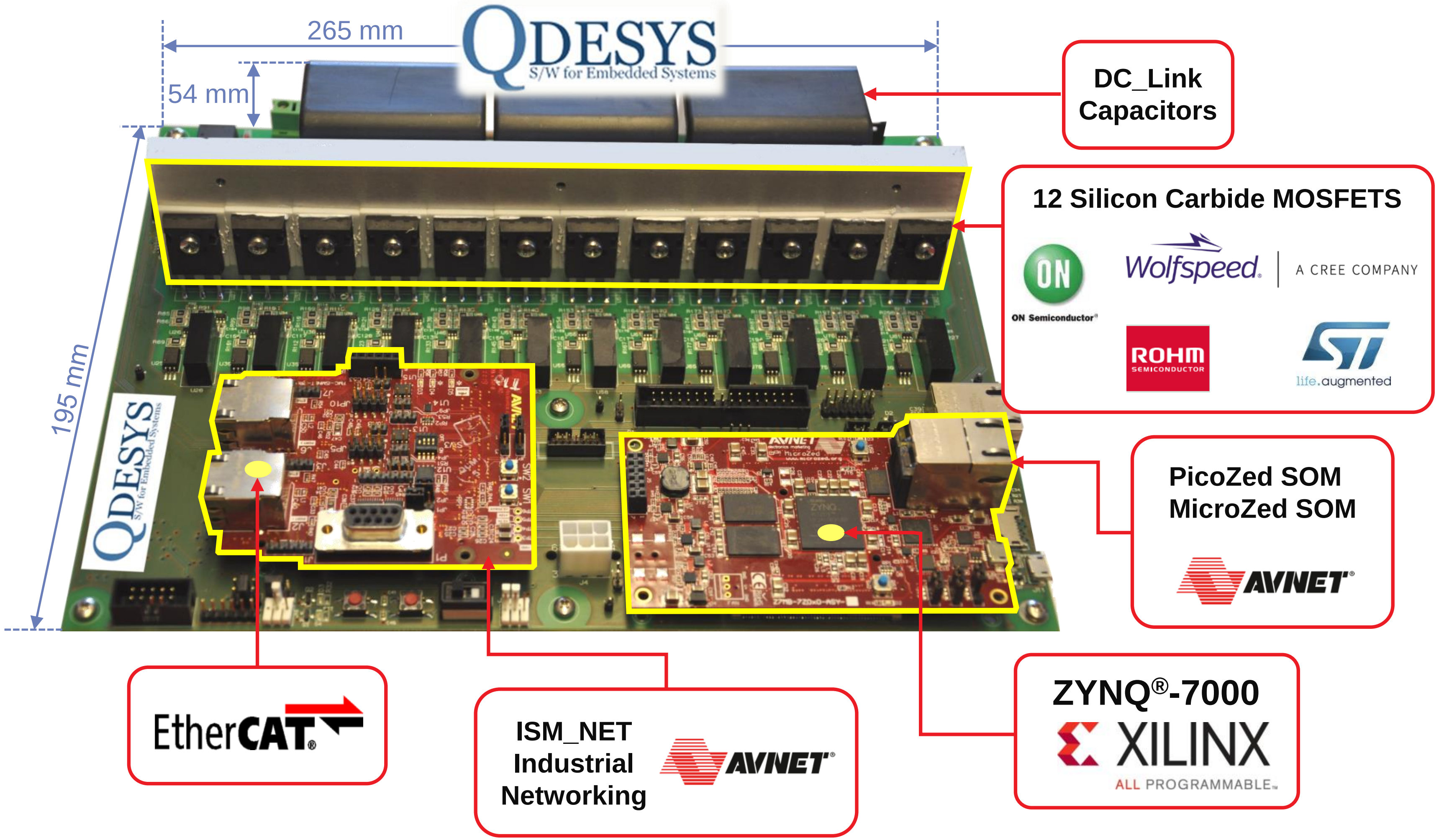
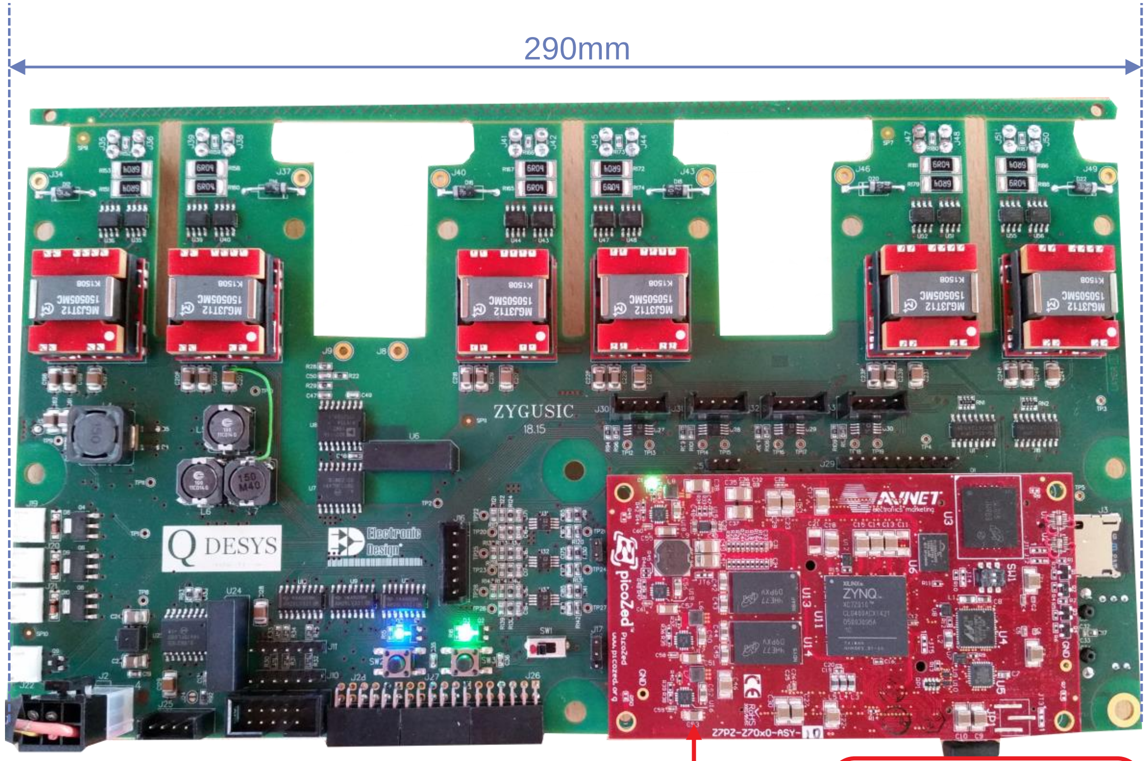
Xilinx-QDESYS SiC 3-Level, 10kW Inverter (2014)



- **High speed inverter designed in 2014**
  - Still a top notch platform
  - Extensible to ZYNQ Ultrascale+
- **Small switching losses at high frequencies, i.e., from 96 kHz to 625kHz - Tested**
- **Efficiency of Si-C inverters is found to be 99.25% even at 625kHz for the 10kW inverter - Tested**
- **Tested with PMSM motors up to 500,000 RPM.**
- **Since 2014 applied in:**
  - Avionics
  - Automotive
  - Traction
  - Industrial Drives
  - Propulsion
  - Education (Universities, Researchers)
  - Lab-tests

QDESYS Zynq-7000 160kW – 2 Level SiC800V 300A



PicoZed SOM
MicroZed SOM

AVNET

Wolfspeed | A CREE COMPANY

CAS300M12BM2
1.2kV, 5.0 mΩ All-Silicon Carbide Half-Bridge Module
C2M MOSFET and Z-Rec™ Diode

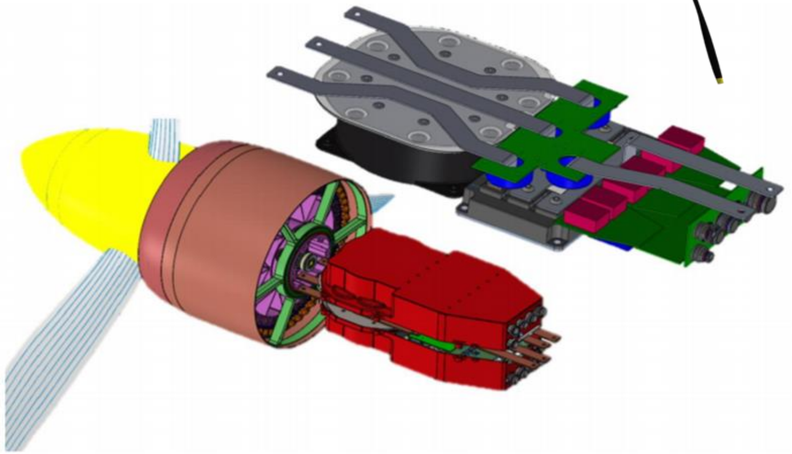
V_{DS}	1.2 kV
$E_{sw, Total\ @\ 300A}$	12.0 mJ
$R_{DS(on)}$	5.0 mΩ

Features
- Ultra Low Loss
- High-Frequency Operation
- Zero Reverse Recovery Current from Diode
- Zero Turn-off Tail Current from MOSFET
- Normally-off, Fail-safe Device Operation
- Ease of Paralleling
- Copper Baseplate and Aluminum Nitride Insulator

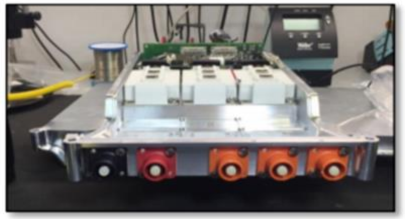
System Benefits
- Enables Compact and Lightweight Systems
- High Efficiency Operation
- Mitigates Over-voltage Protection
- Reduced Thermal Requirements
- Reduced System Cost

Package 62mm x 106mm x 30mm

Propulsion Control – 2 Level SiC Inverters (NASA X-57)

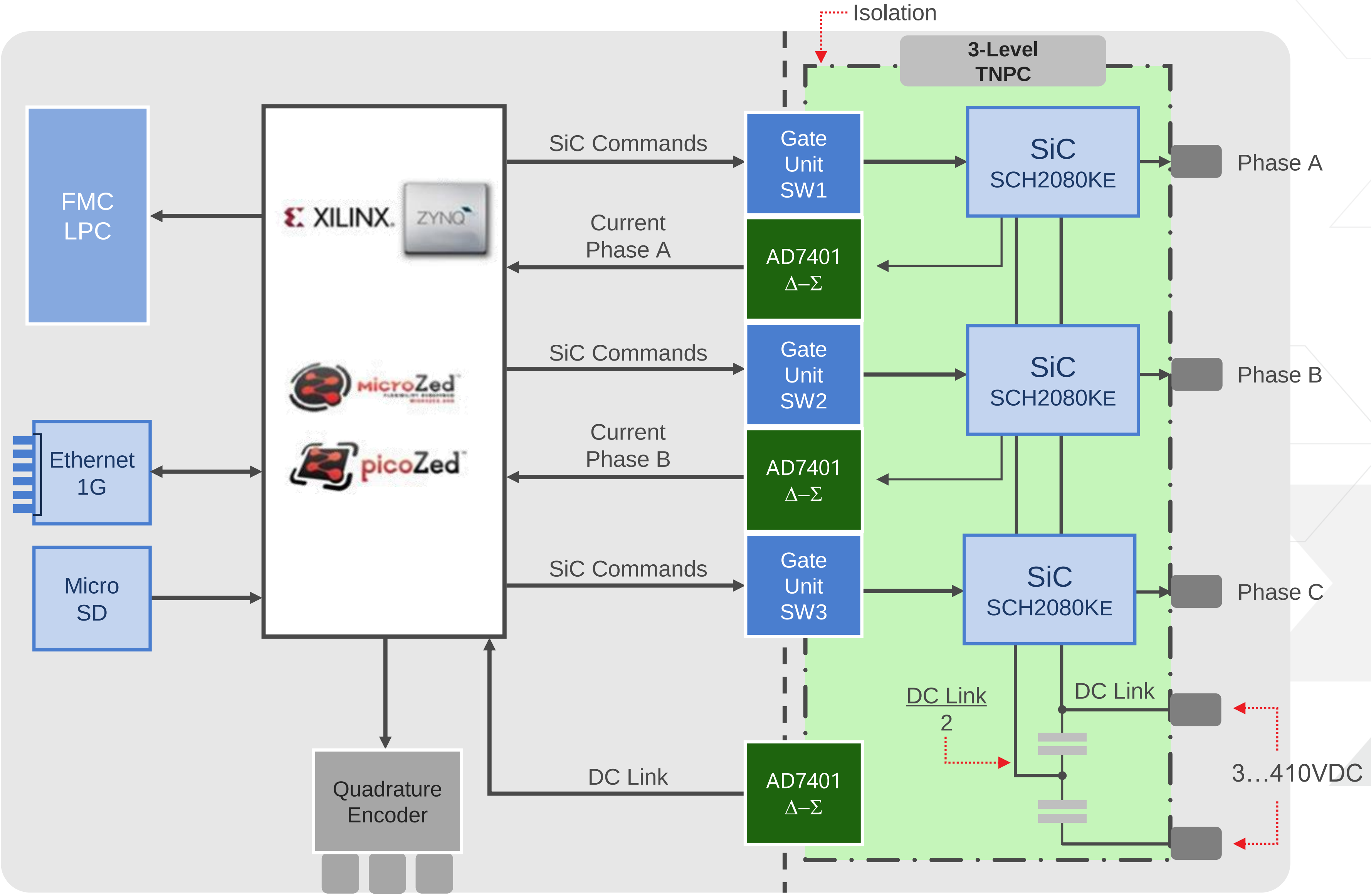


- **QDESYS Motor Control** implemented on Xilinx ZYNQ FPGA+ARM
- **Redundant Architecture:** each power train contributes half of the torque
- **Alluminium enclosure** (EMI schielding) Aerospace connectors for I/O
- Running at **200%** of power
- **Software validated**
- Environmental screening (shake and brake) completed



TLIMOT Hardware Details

TLIMOT 3-Level Inverter Block Diagram



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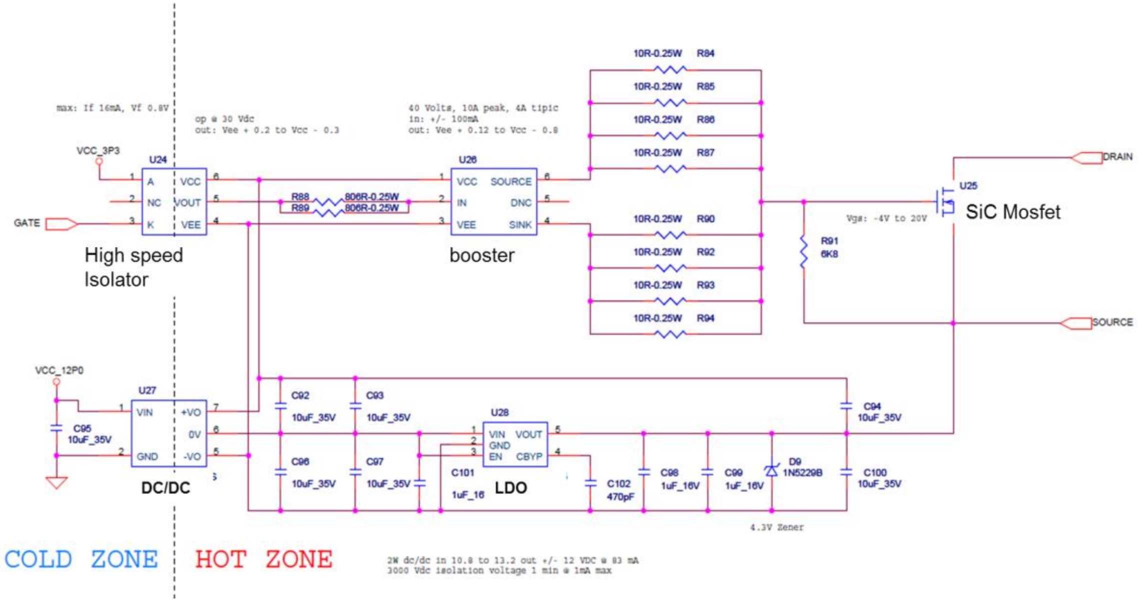
Fast Switching Needs a Good Gate Driver



> Optimization for fast switching is a challenging task.

> Major contributors to the switching behaviour:

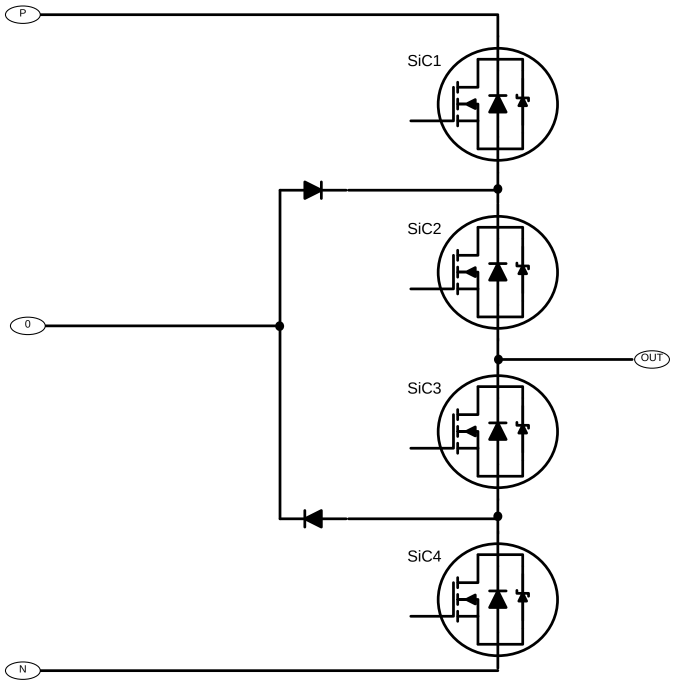
- Gate driver,
- Gate resistor,
- Voltage overshoot caused by inductive parasitics
- Bus bar behaviour
- DC-Link capacitors

This is an example only every application has its own specificity – many semiconductor manufacturers produces integrated gate drivers

Lesson learned – gate drivers designed for IGBT perform poorly with SiC – beware!

Power Switch Topology

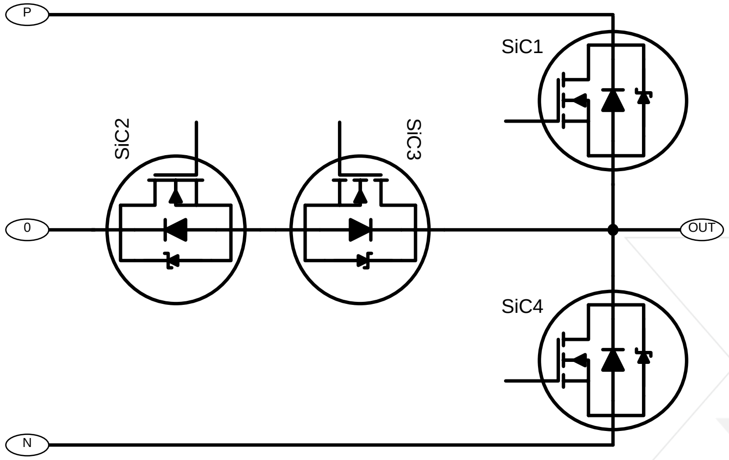
NPC (Standard)
Only 3 levels



3L NPC phase leg 10 semiconductors:

- 4 SiC
- 4 Free-Wheeling Diodes
- 2 Clamping Diodes

TNPC (Adopted configuration for TLIMOT)
2 levels and 3 levels



3L TNPC phase leg 8 semiconductors:

4 SiC

4 Free-Wheeling Diodes

Maximum DC-link voltages:

- 400VDC using 650V semiconductors,
- 800VDC using 1200V semiconductors,
- 1200VDC using 1700V semiconductors

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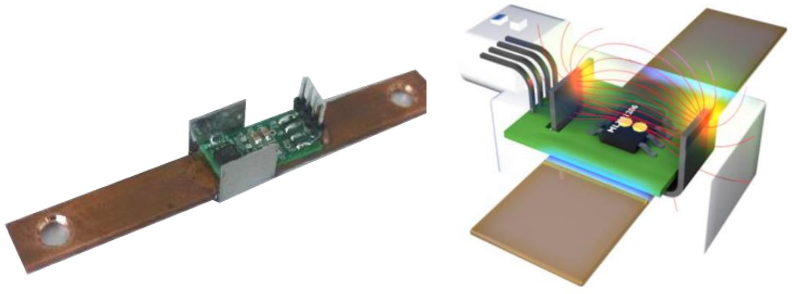
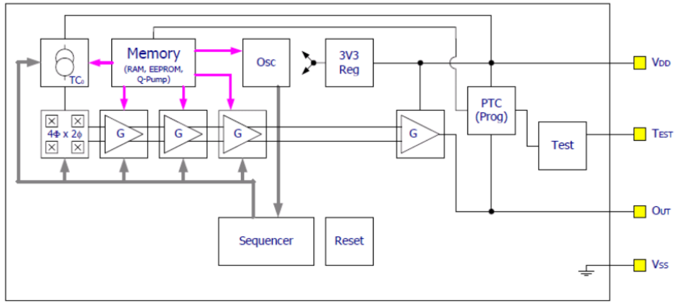
Current Sensors Used With SiC and Zynq

Melexis

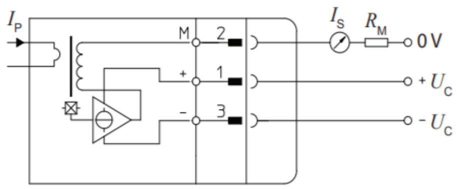
- ~250KHz Bandwidth
- +/- 7.5mT





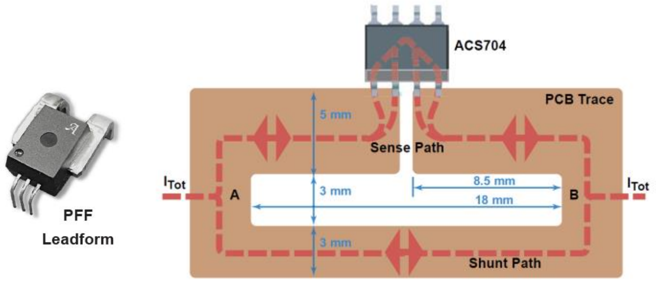
LEM

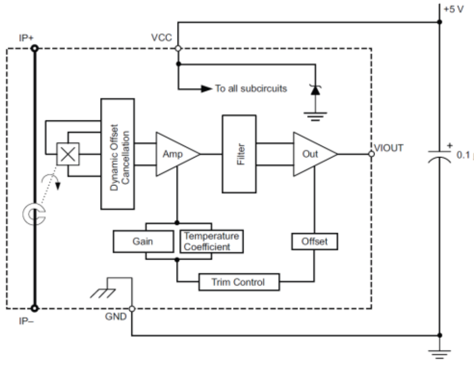
- ~240 kHz Bandwidth
- 50A…1200A



Allegro

- ~120kHz Bandwidth
- 50A…200A





Functional Block Diagram

To XADC - Sigma-Delta or external ADC

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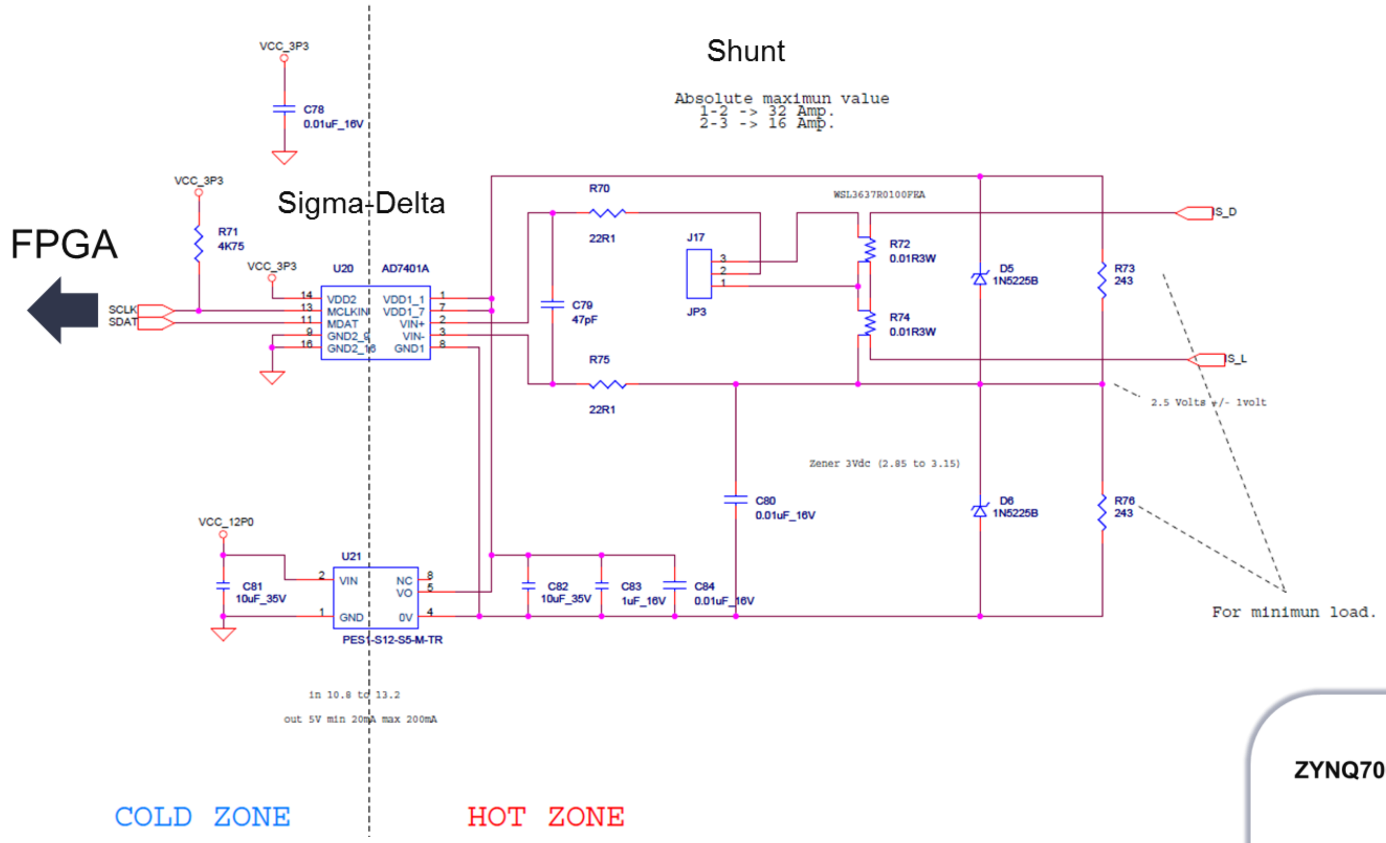
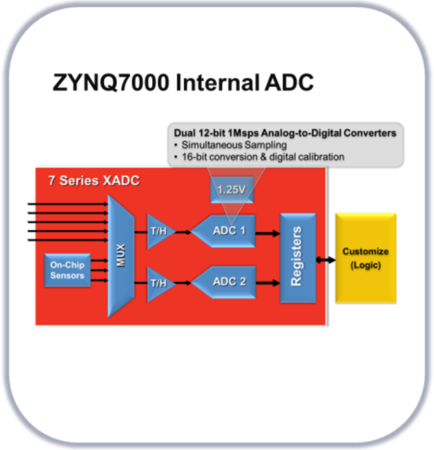
TLIMOT Sensing (Shunt)

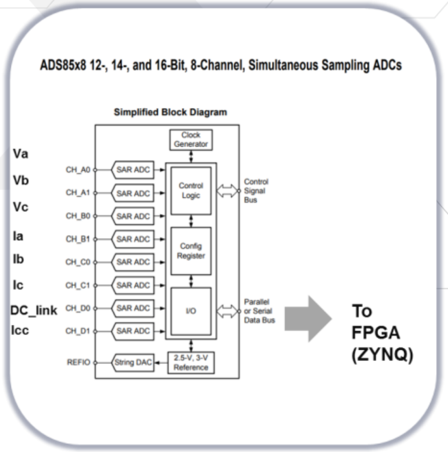


- > **Highest bandwidth (Shunt)**
- > **Low latency (response time)**
- > **Sigma-Delta modulator (in FPGA)**
  - >> Full digital A/D
  - >> Sinc3 filters for reconstruction
  - >> Polyphase Sinc3 for lower response time

Other ADC used



Acquires 2 channels simultaneously



Acquires 8 channels simultaneously

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General Architecture TLIMOT

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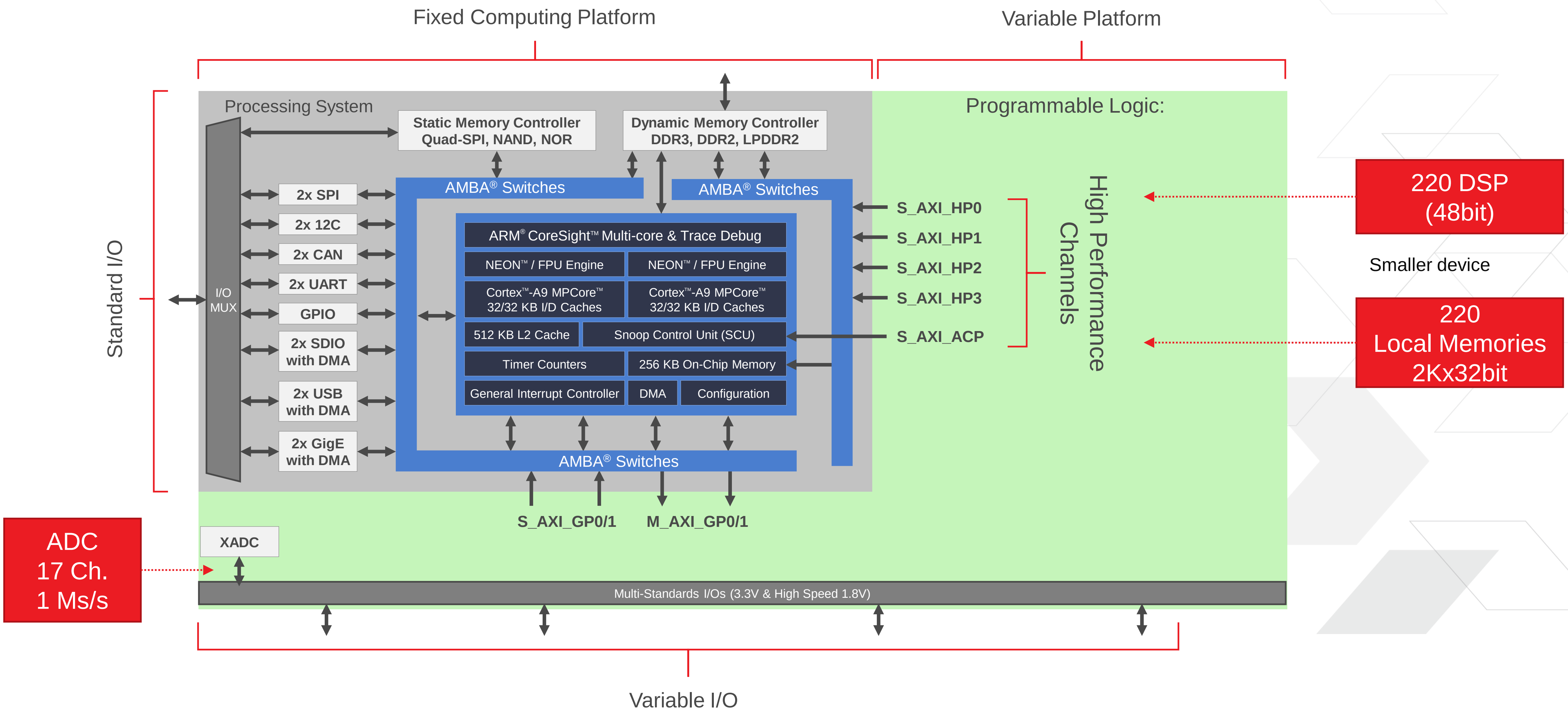
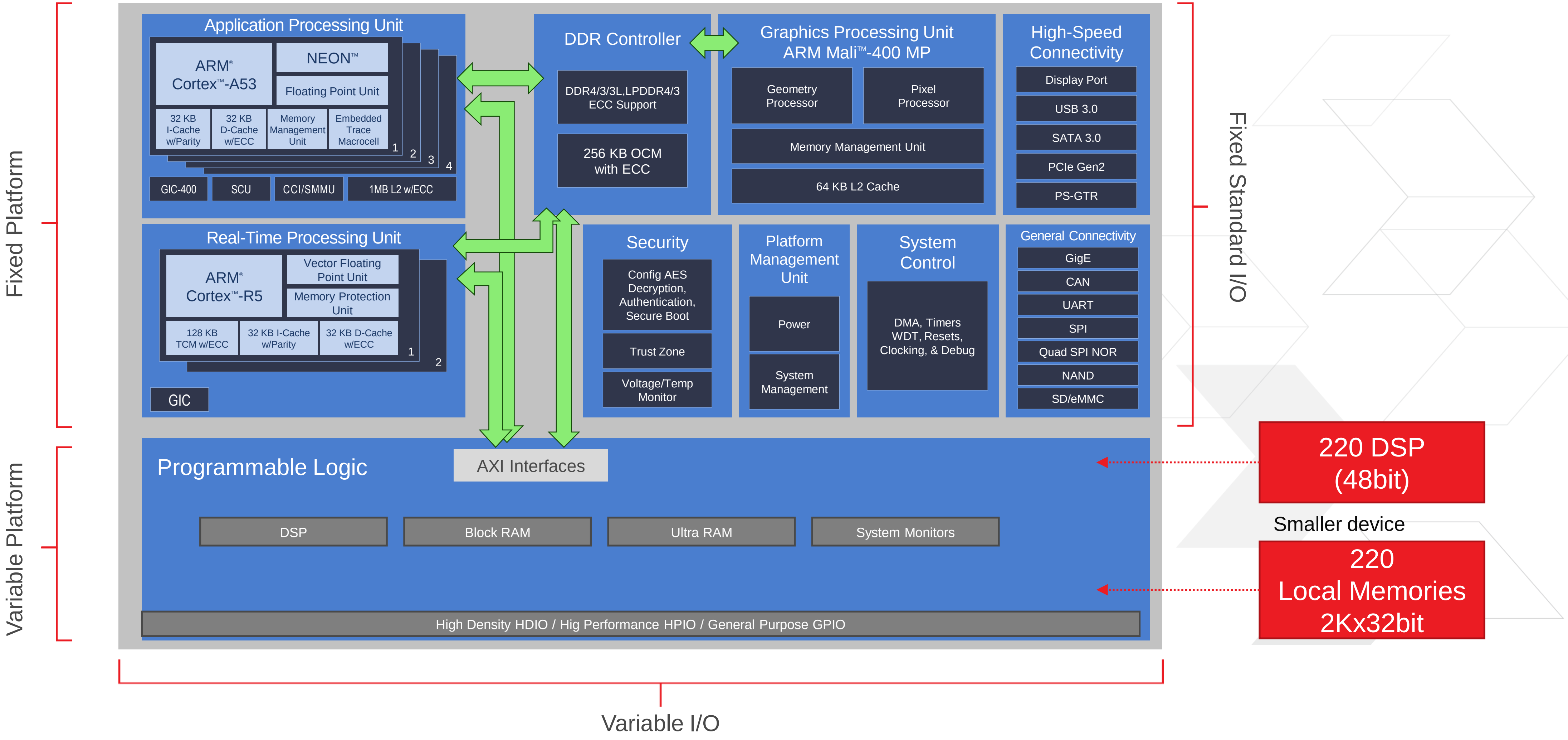
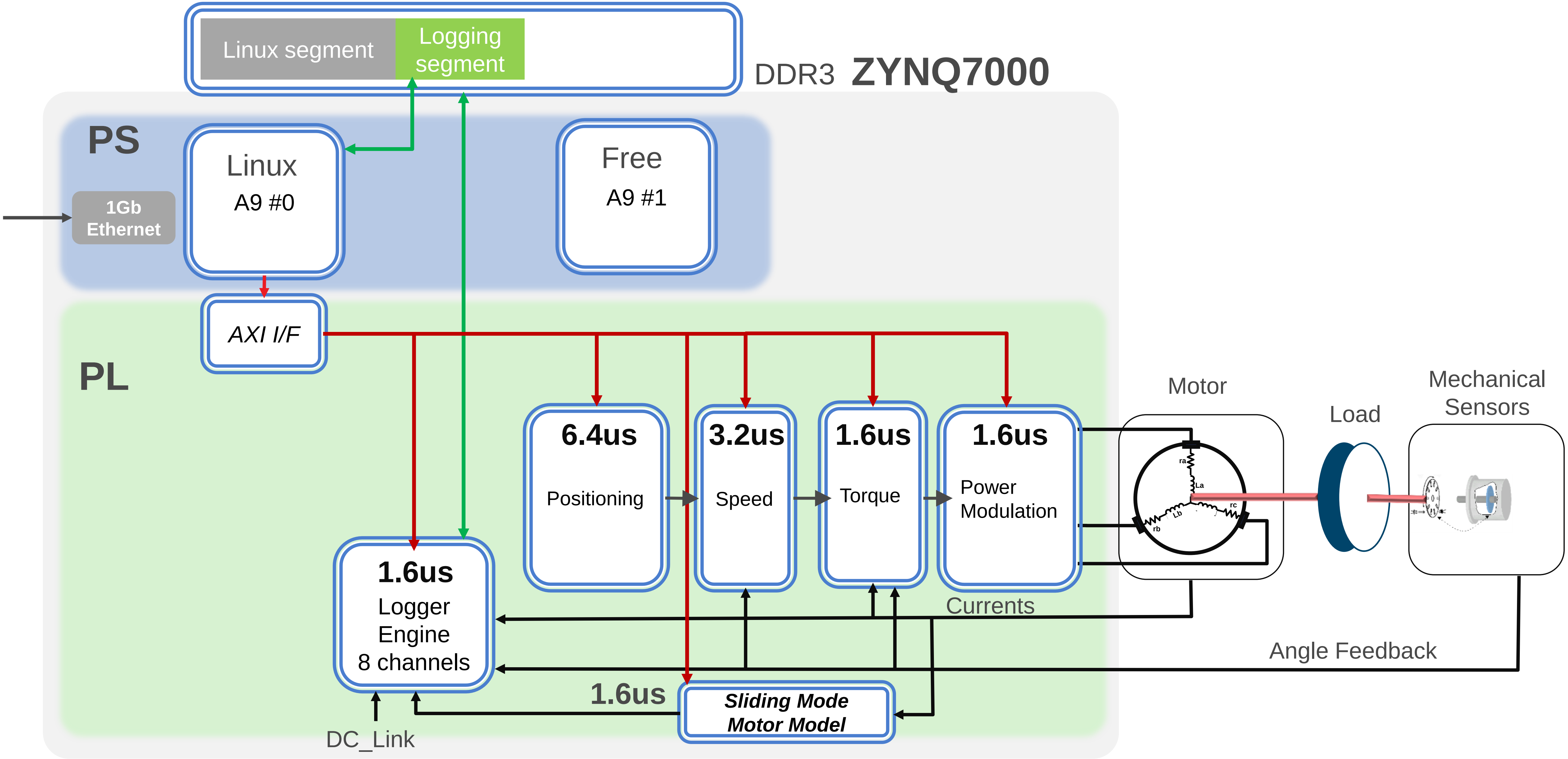
Zynq-7000 SoC
1st Generation



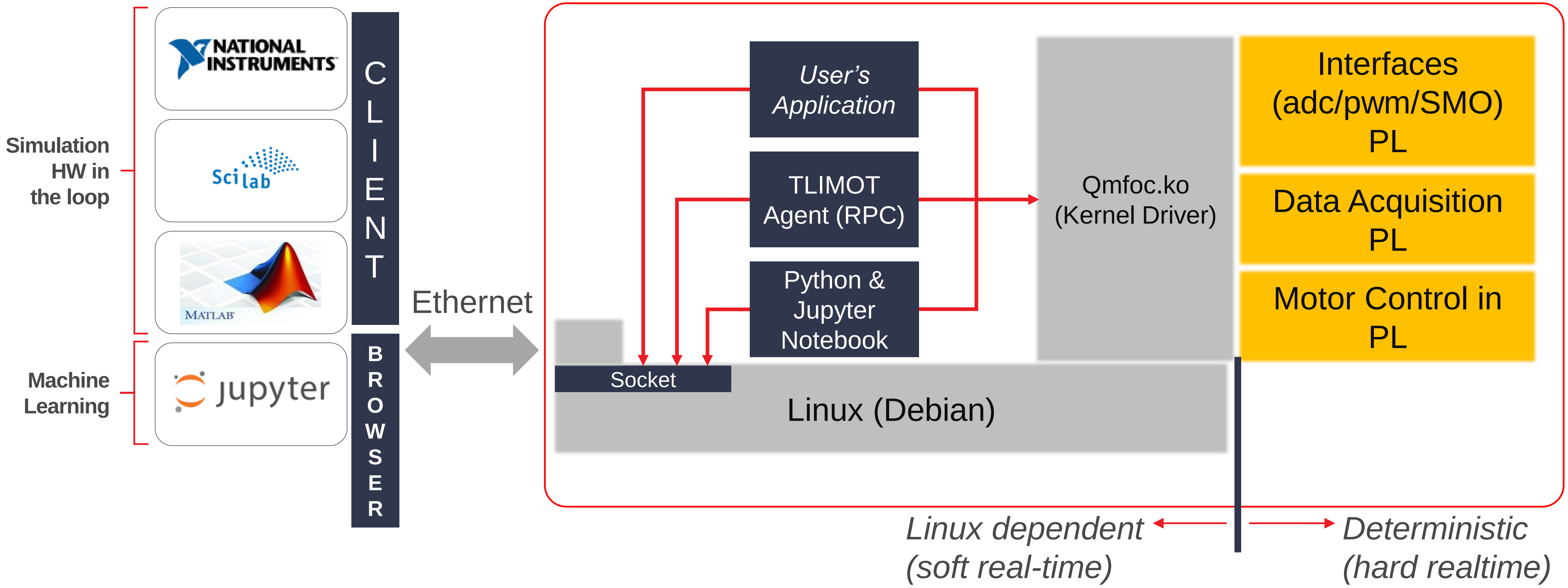
Zynq Ultrascale +
2nd Generation



General Architecture



Software Architecture – Linux-Based



GUI and Interfaces

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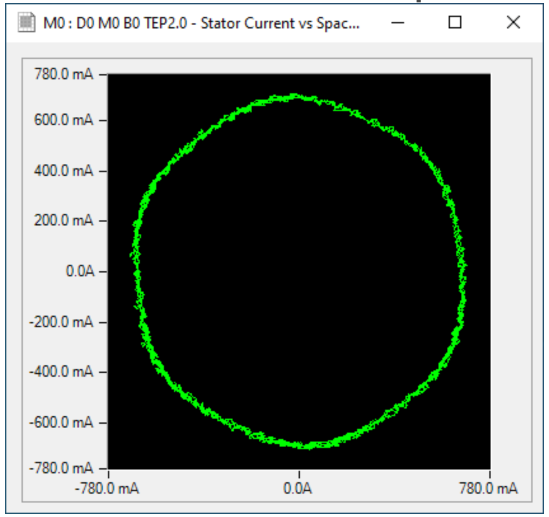
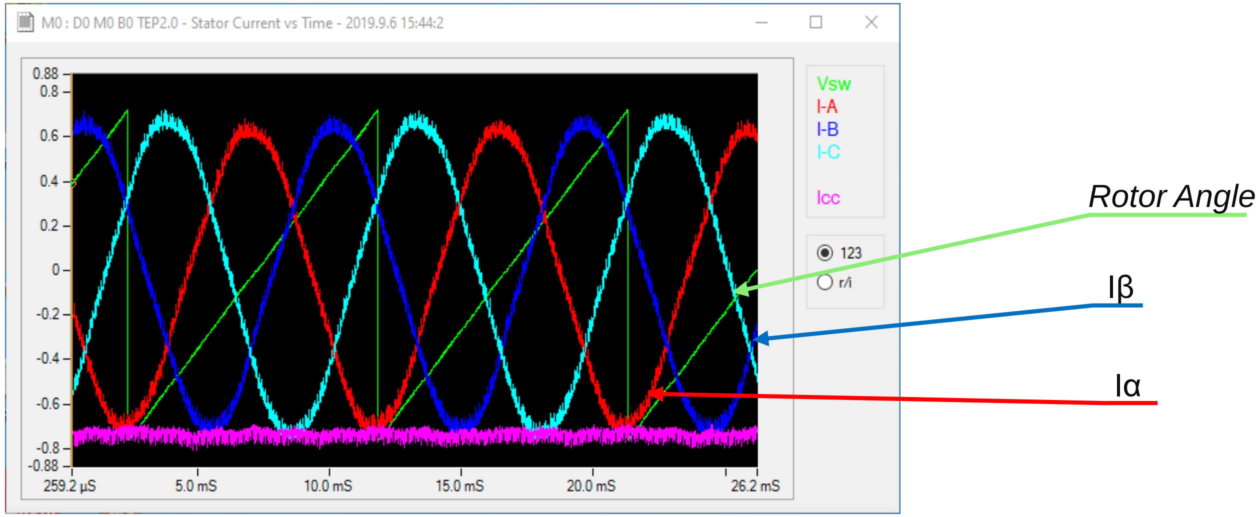
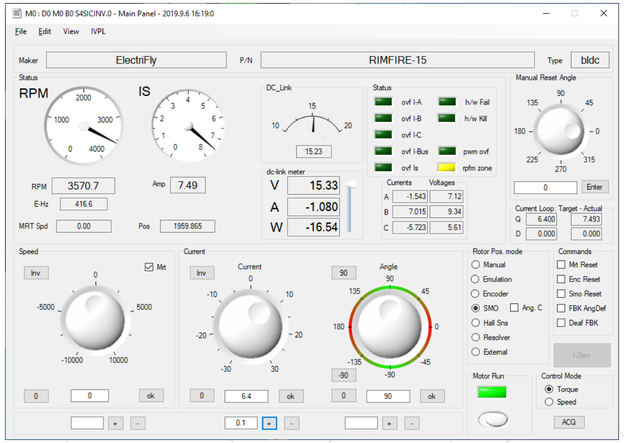
Real Time Observability with the GUI (National Instrument Labstudio)

Stator Currents Iα,Iβ

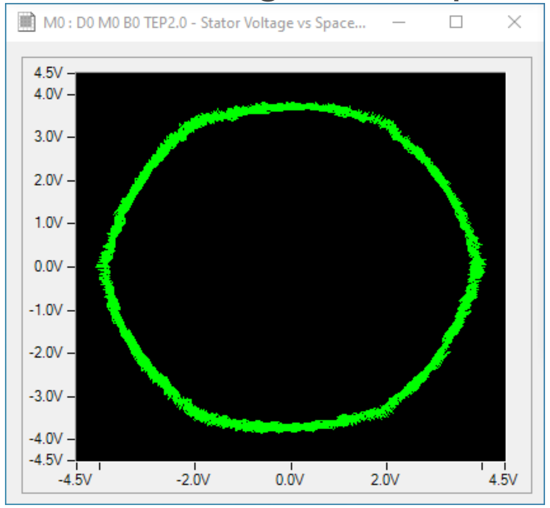


Stator Currents vs Time

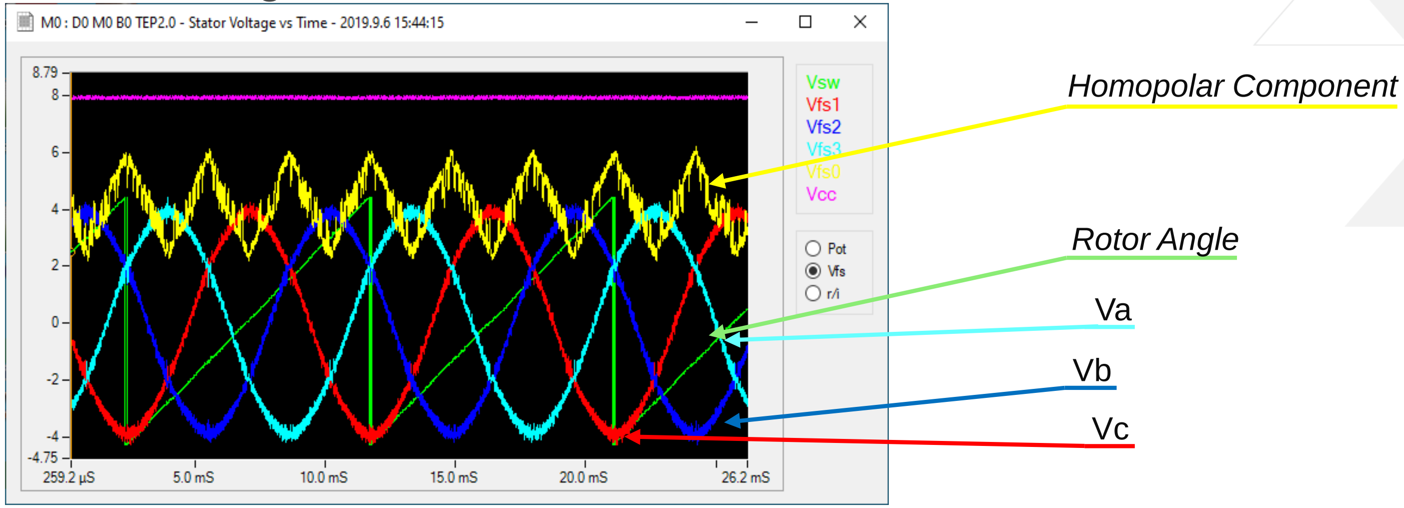




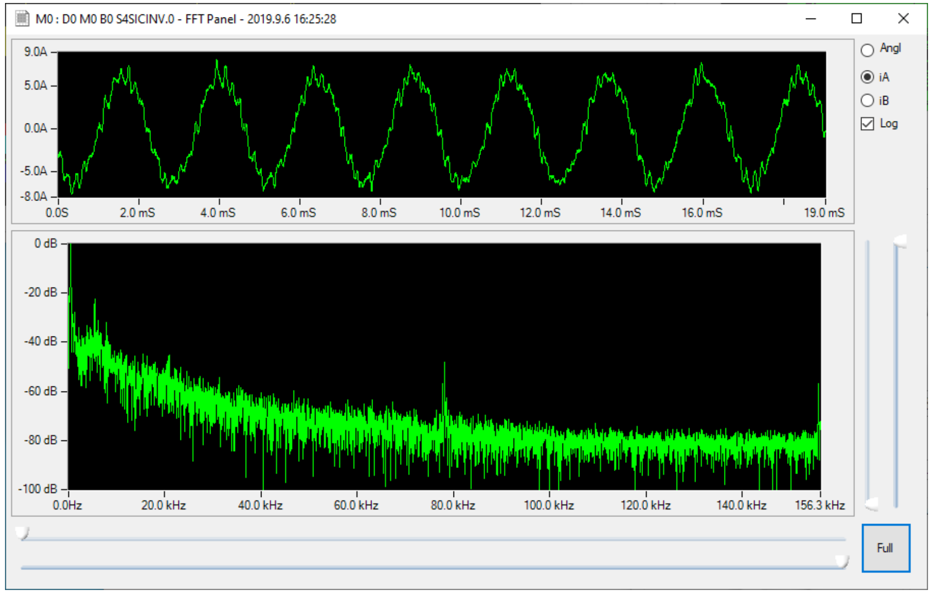
Stator Voltages Vα,Vβ

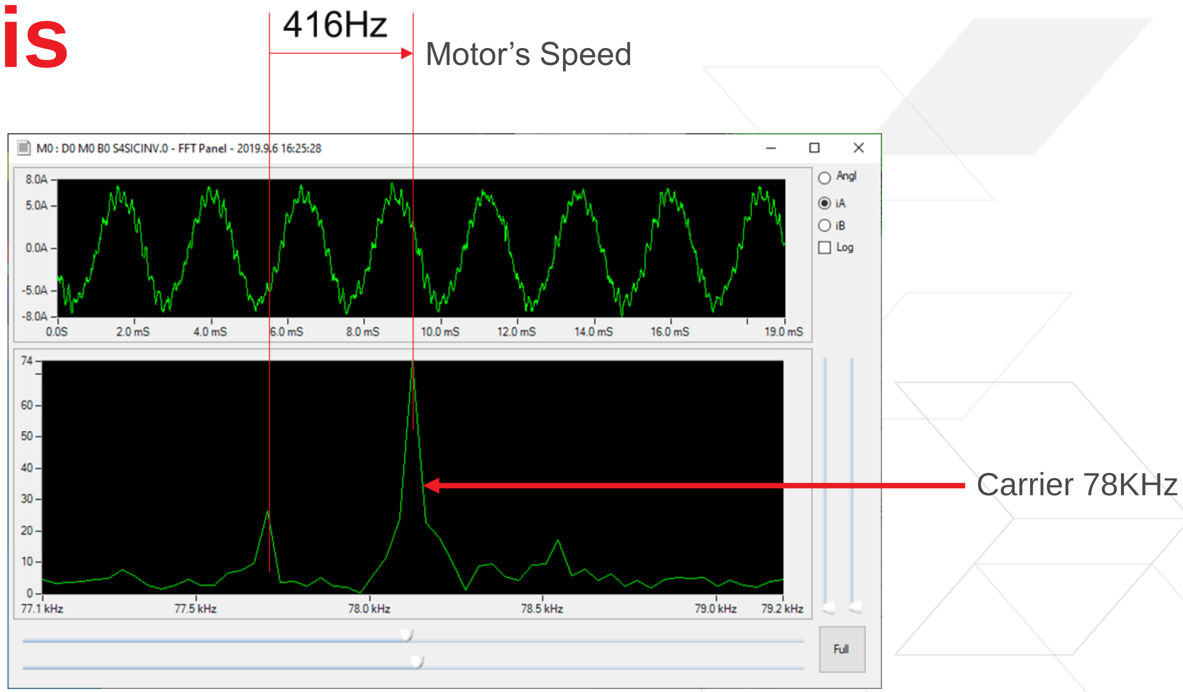


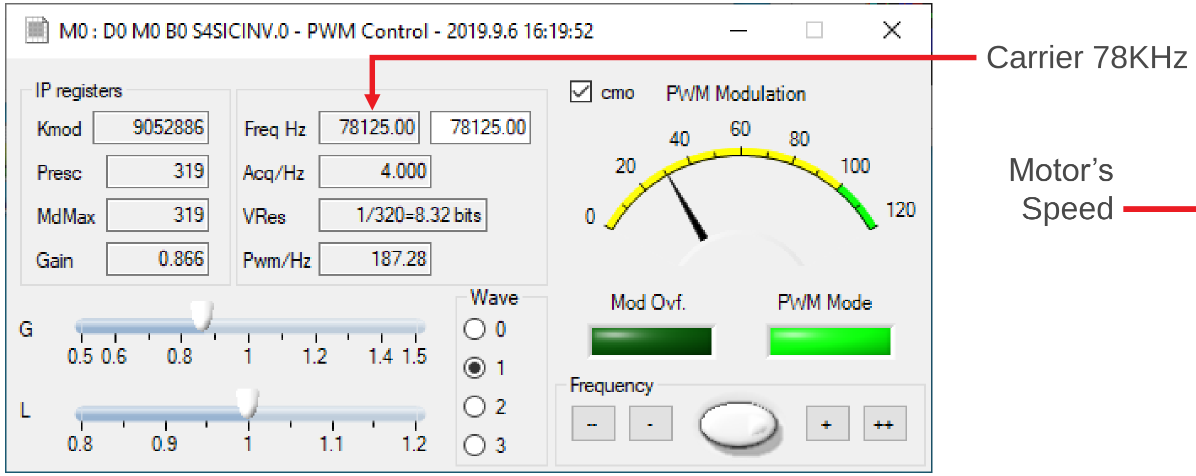
Stator Voltages vs Time

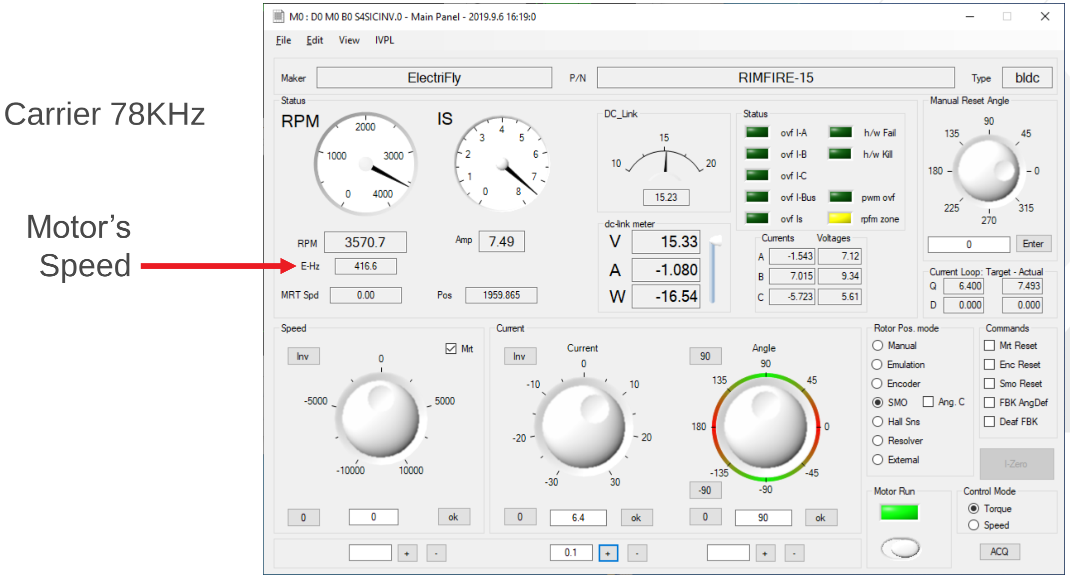


Real Time Frequency Analysis









Python Interface

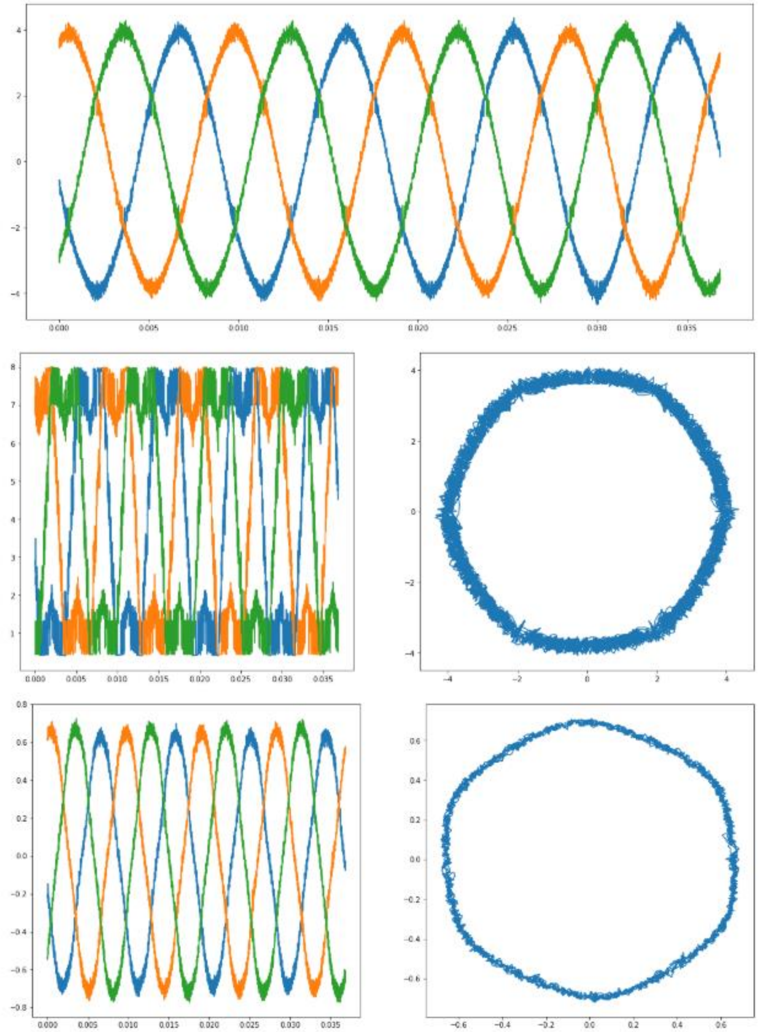
Jupyter - Notebook

```
In [1]: import time
        import math
        import matplotlib
        import numpy as np
        import matplotlib.pyplot as plt
        from mcm2arlib import mcm2arlib

In [2]: mcm=mcm2arlib()

In [3]: mcm.qmx_loadlink("")

In [4]: mcm.qmx_startup()

In [5]: print("s/w version = %s" % (mcm.qmgs_sw_version()))

        s/w version = 2.1.39

In [6]: IVPLOGGER_ACQ_CTRLST_READY=(1<<3) # acquisition ready

In [ ]:

In [7]: # LPF1 fcut to K conversion
        def lpf1_K(Ts,Fcut):
            tau=1.0/(2.0*np.pi*Fcut)
            n=tau/Ts
            T=1.0/(math.exp(1.0/n)-1.0)
            K=1.0/(1.0+T)
            return K

In [8]: # arm for ivpl acquisition
        def startivplacq(motor):

            mcm.qmpm_ivpl_synmod(motor,1) # 0=free run, 1=sync with electric angle
            mcm.qmpm_ivpl_automemsz(motor,1) # 0=manual 1=automatic sample eval
            mcm.qmpm_ivpl_numwaves(motor,4) # num of electric cycles
            mcm.qmpm_ivpl_numsmp(motor,8192) # num samples
            mcm.qmpm_ivpl_howmany(motor,-1) # unlimited

            mcm.qmx_process() # surround elab

            mcm.qmxm_ivpl_start(motor) # initiate log

In [9]: # display log data
        def dispivplacq(motor):

            # get data
            [iphs_a,iphs_b,iphs_c,ibus_x,vphs_a,vphs_b,vphs_c,vbus_x,vphs_n,angle] = mcm.qmgm_ivpl_data_s(motor)
```

Full Controllability

Displayed Results

```
In [21]: if (mcm.qmgm_ivpl_status(motor) & IVPLOGGER_ACQ_CTRLST_READY) != 0:
             dispivplacq(motor) # display
```



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Useful Links TLIMOT

- **Information** http://www.qdesys.com/pdf/MotorControlSolutions_QDESYS_Material.pdf
- **Requests to:** info@qdesys.com

EDDP Open Source (No SiC)

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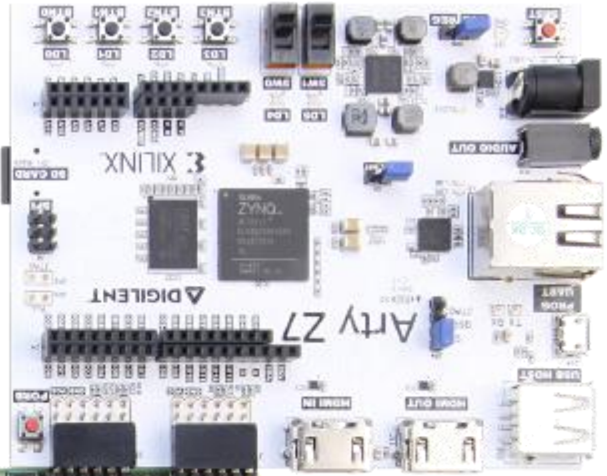
EDDP – Electric Drive Demonstration Platform

- PMOD connection between Control Board & EDPS

- Default motor – 15W BLDC
- Encoder included

- EDPS – Supports Up to 1KW

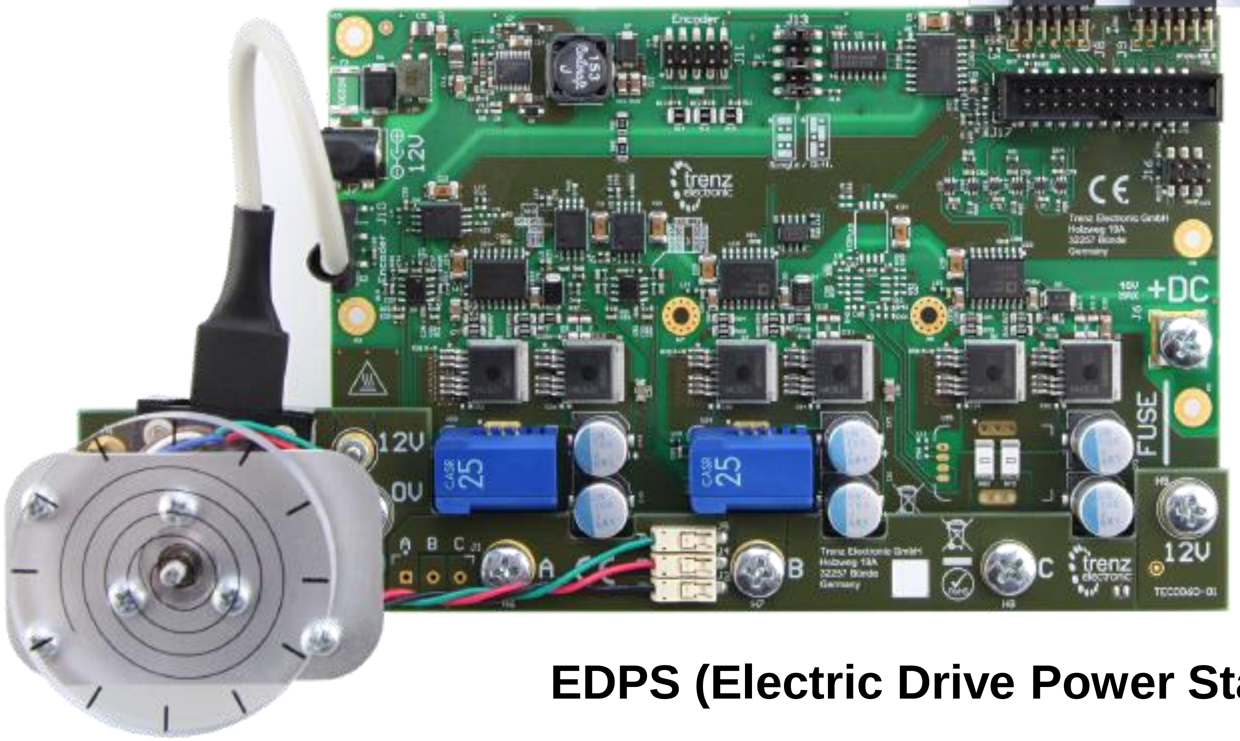
Control Board



Python Control – SPYN Project

IIoT-EDDP
+
PYNQ

- Access To Motor Control Parameter
- Request Status Information from the Motor
- Programmatic Control of Motor
- Continuous Status Capture from Motor
- Plots to Visualize Captured Data
- Storing Captured Data for Analytics
- Live Interactive Plots to Investigate Data



EDPS (Electric Drive Power Stage)

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Predictive Control

- **Use system's model for predicting the future behaviour of the controlled variables**
- **Optimal actuation according to predefined optimization criterion**

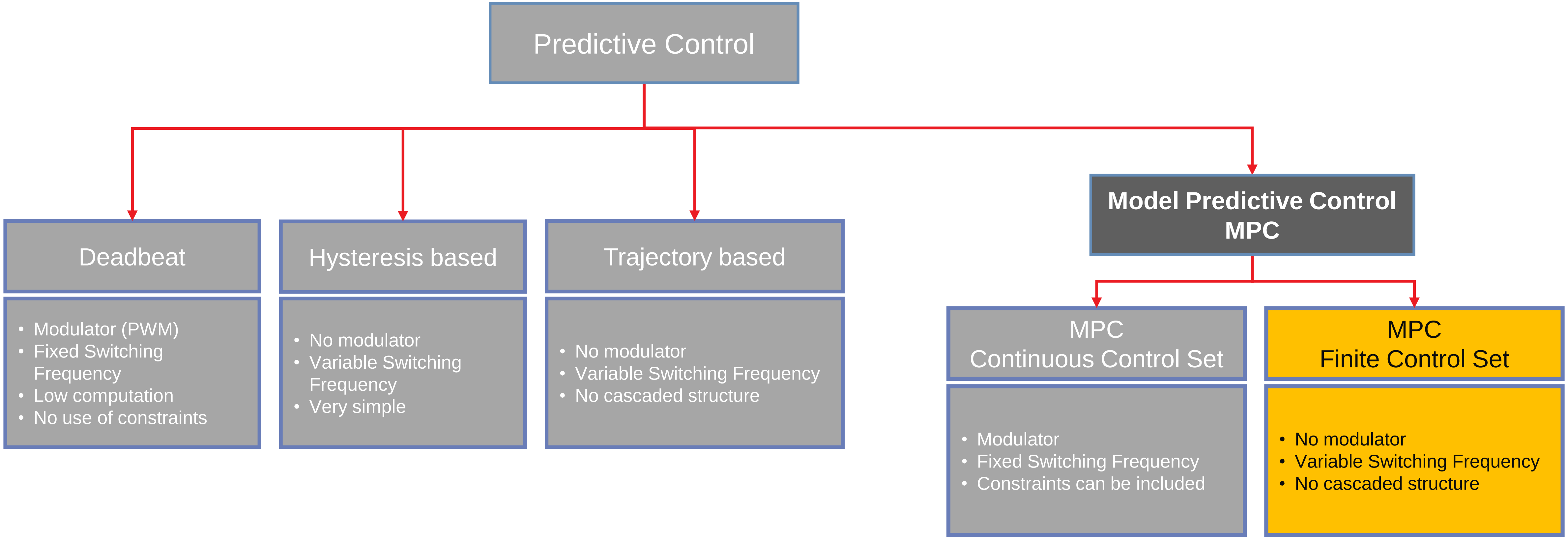


Image Source: Predictive Control in Power Electronics and Drives
IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 55, NO. 12, DECEMBER 2008

Finite Control Set Model Predictive Control – SPYN

> Jupyter as the interface to the real time controller

In [ ]: # control widgets↔

Use the hardware switch SW0 to change between FOC and MPC.

Motor   mode Current

RPM 1000 (only for FOC)

Iq in mA 880 (Iq set point for FOC and MPC)

λ_u *1000 0.00 (switch cost wheigt for MPC)

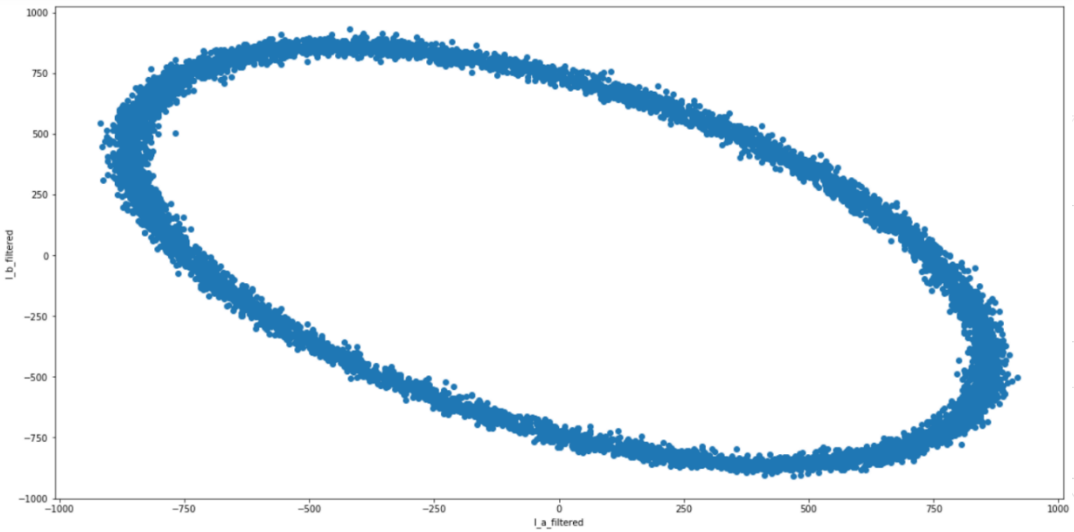
In [ ]: # Capture Interface Widgets↔

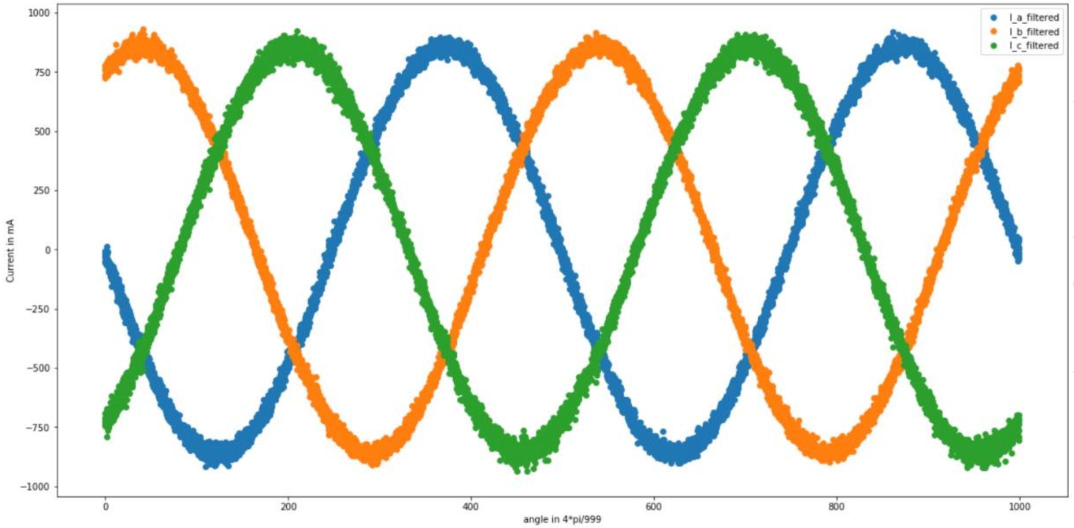
Capture: Ia / Ib (filtered) | Ia / Ib (raw) | Ialpha / Ibeta | Id / Iq | Vd / Vq | Valpha / Vbeta | Va / Vb / Vc | V_PWM

Decimation: 1   Sample Count: 4096

Ready for next Capture.   Start the Capture

Load the Capture



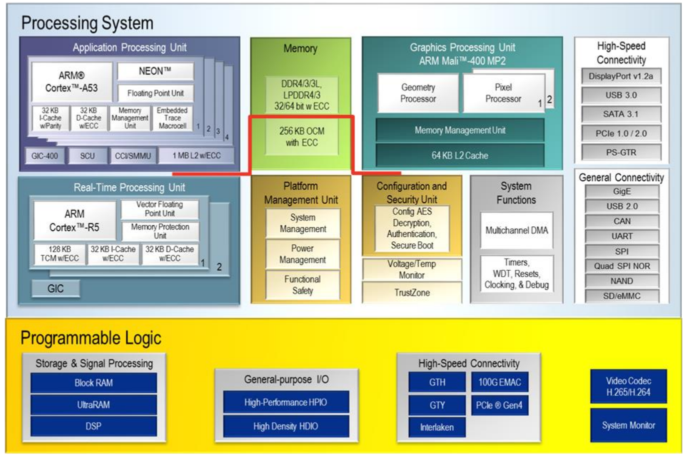


Safety

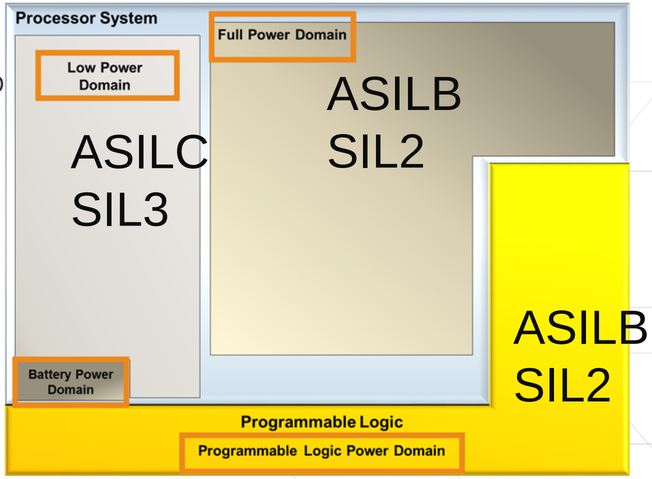
Safety capabilities

Device Domains

- Full Power Domain (FPD)
- Low Power Domain (LPD)
- Programmable Logic (PL)

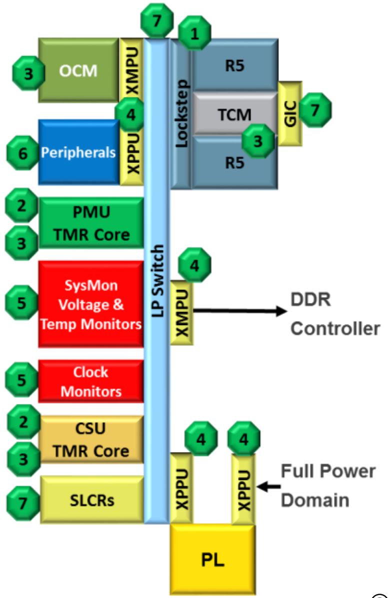


- **Isolated Domains**
  - Battery Power Domain (BPD
  - Low Power Domain (LPD)
  - Full Power Domain (FPD)
  - Programmable Logic (PL)
- **Each power domain is separated**
  - By 50x the min spacing
  - ~10 um



LOW POWER DOMAIN

1. Lockstep for R5s
2. Triple Modular Redundancy (TMR) for Platform Management Unit (PMU) and Configuration & Security Unit (CSU)
3. ECC for TCM, OCM, CSU and PMU RAMs
4. Memory & Peripheral Protection Units provide functional isolation
5. CCF coverage by clock, voltage, and temperature monitors
6. Logic Built In Self Test (LBIST) for checkers & monitors at power-on
   - Peripherals coverage by end-to-end software protocols
7. Software Test Library (STL) for GIC, interconnect, SLCRs & error injection



SIL3 HFT = 1


Certificate / Certificat
Zertifikat / 合格証
XILINX 1502011 C001
exida hereby confirms that the:
Zynq UltraScale+ MPSoC
Xilinx, Inc.
San Jose, CA, USA
Has been assessed per the relevant requirements of:
ISO 26262:2011 Parts 2, 4, 5, 6, 7, 8, 9 and 10
IEC 61508:2010 Parts 1, 2 and 3
and meets requirements providing a level of integrity to:
Systematic Integrity: ASIL C and SIL 3 (HFT1)
Safety related function:
The Low Power Domain (LPD) subsystem of the Zynq UltraScale+ MPSoC supports the execution of safety related software. A failure in the LPD subsystem caused by a hardware fault shall not cause the LPD to go into an unsafe state for a time greater than the specified fault tolerance time interval.
Application restrictions:
The MPSoC shall be used per the requirements described in the Zynq UltraScale+ MPSoC Safety Manual (UG1226) and Software Safety User Guide (UG1220).
The manufacturer may use the marks:
Revision 1.3 August 14, 2018
Surveillance Audit Due October 1, 2020
ANSI Accredited Program PRODUCT CERTIFICATION
Evaluating Assessor
Certifying Assessor
Page 1 of 2

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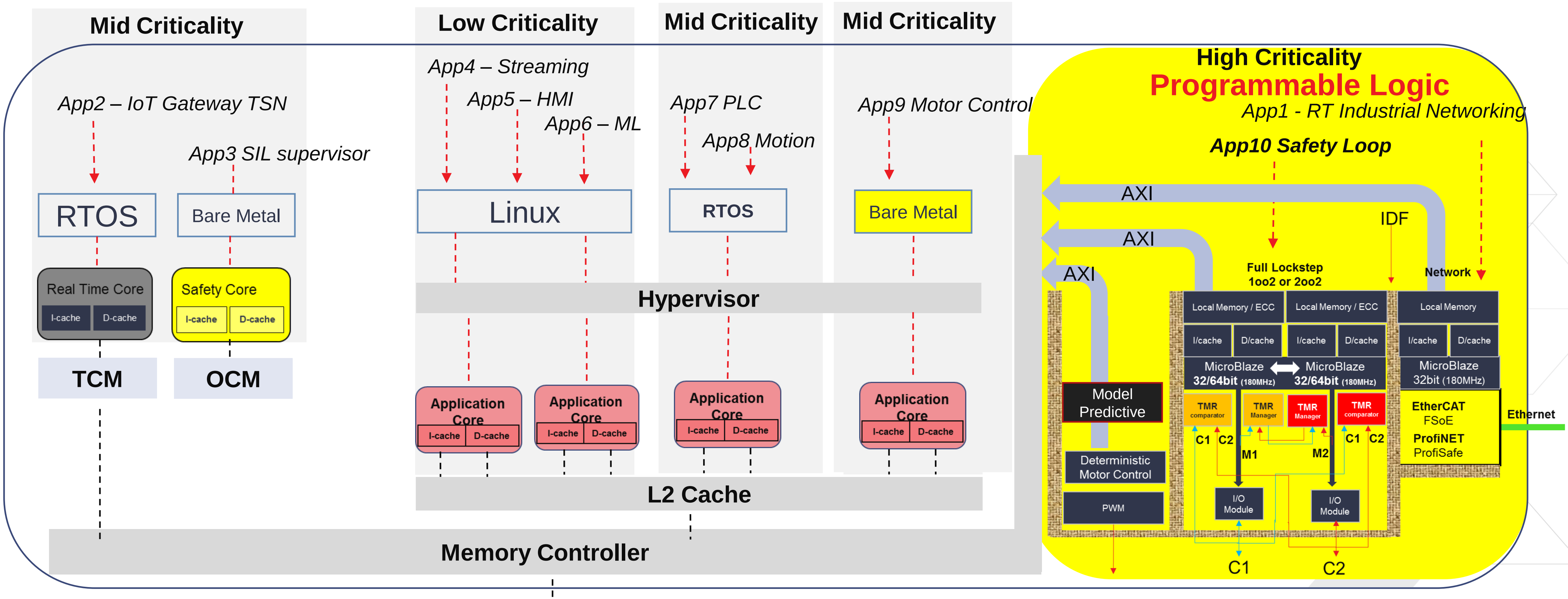
Architecture of the single chip HFT=1 Drive



External Memory

HMI = Human Machine Interface
ML = Machine Learning
TSN = Time Sensitive Network
SIL = Safety Integrity Level
OCM = On Chip Memory
TCM = Tightly Coupled Memory

Improved modularity and reduced criticality impact

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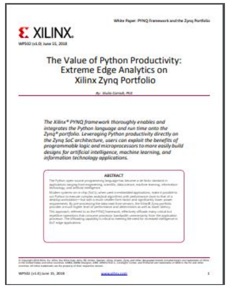
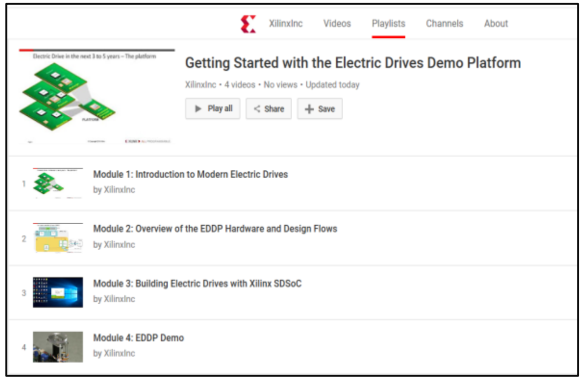
> **Learn More about EDDP, SPYN (same HW, different designs)**
  >> https://github.com/Xilinx/IIoT-EDDP
  >> https://github.com/Xilinx/IIoT-SPYN



White Paper



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